CSCE 3304 – Digital Design II
Spring 2018

Homework Assignment 1 [Weight: 5%]
Verilog RTL Modeling and Verification

Guidelines:

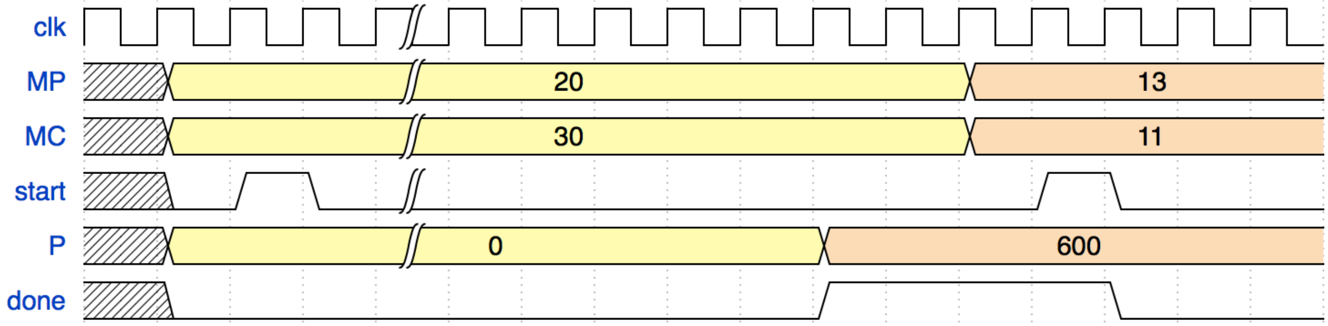
1) Use CloudV to develop, simulate and synthesize the modules.
2) The CloudV workspace has to be private. A source code similarity checker will run against your submitted code.
3) Your source files must comply with the course coding guidelines (attached).
4) You must synthesize your RTL models using the OSU035 library. The synthesis reports must be examined for errors (e.g., latches in combinational block). The best design (area and delay) for each problem will receive 20% bonus.
5) The tesbenches should be self-checking; meaning, the testbench should verify the correctness of the output generated by the DUT.
6) 50% of the grade is for the Verilog model. The other 50% is for the Verification testbenches.
7) Every problem should be delivered as a separate workspace shared with Dr. shalan and your TA (Dr. Shalan's cloudv ID: shalan). The workspace should contain the final submission only. Any files related to trials must be deleted.
8) The submission is done by sending a notification email to the TA (cc Dr. Shalan) before Feb. 21st, 11:59PM. Use the email subject: "337-SP18: ASS1". Emails with incorrect subject will be ignored.

Problem 1: Serial-Parallel Multiplier [35%]

Using Verilog, model and verify a 32-bit signed serial parallel multiplier outlined by the attached document. The design outlined by the document does not cover the interface to the multiplier. The multiplier is required to have the following interface:

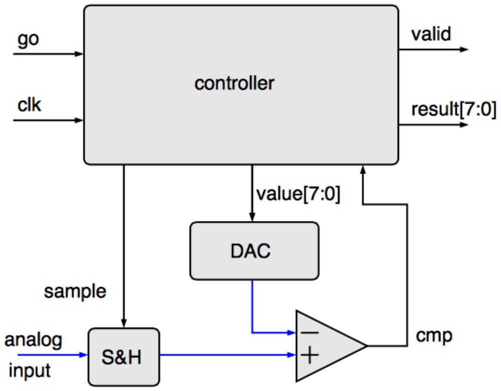
Port	Direction	Size (bits)	Description
MP	In	32	The multiplier. Is stable before the *start* is asserted and may change after *done* is asserted.
MC	In	32	The Multiplicand. Is stable before the *start* is asserted and may change after *done* is asserted.
start	In	1	Indicates that *MP* and *MC* are stable to start the multiplication (active only for 1 clock cycle)
P	Out	64	The product. Must be ready before *done* is asserted.
done	Out	1	Indicates that the product (*P*) is ready. De-asserted when *start* is de-asserted.
clk	In	1	The clock. All events are in sync w/ the clock positive edge
resetn	In	1	Asynchronous reset. Active low.

The following is an example timing diagram to make things more clear:



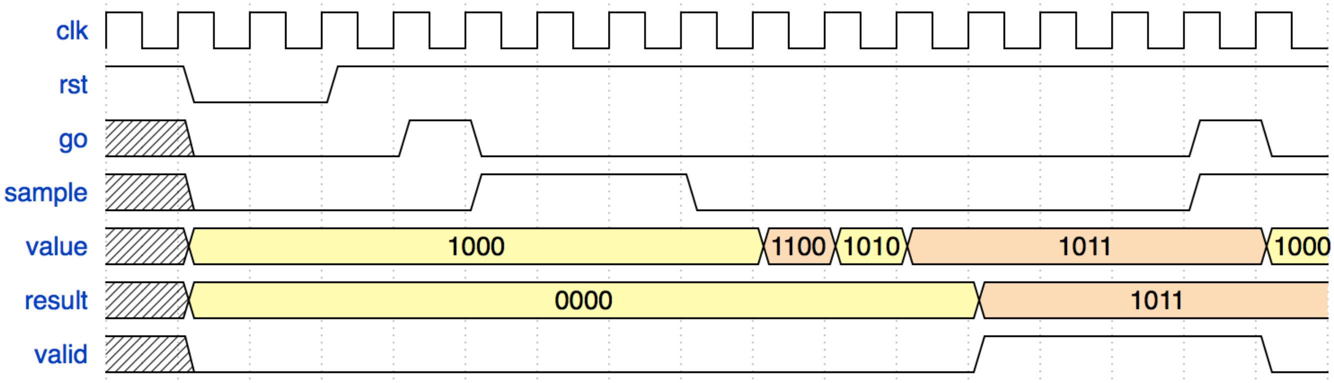
Problem 2: Successive Approximation Register (SAR) ADC Controller [30%]

The controller has to support number of bits from 8 to 16 (parameterized). The controller has an input to start the conversion (*go*) and an output (*valid*) to indicate the availability of the converted sampled data (*result*). The output *sample* controls the sample and hold circuit. To sample analog data *sample* has to be active for number of clock cycles (parameterized). The output *value* reflects the current value of the SAR. All events are synchronized w/ the rising edge of the clock. The reset signal is asynchronous and active low.



To understand how the SAR operates refer to the following link: https://www.maximintegrated.com/en/app-notes/index.mvp/id/1080

Here is a sample timing diagram to make things easier for you.



Problem 3: i2c Master [45%]

Implement an i2c master as per the design outlined at:

- http://www-ee.eng.hawaii.edu/~tep/EE260/Secret/masterblock.html
- http://www-ee.eng.hawaii.edu/~tep/EE260/Secret/task2.html

To learn more about the i2c protocol, check out: http://www.best-microcontroller-projects.com/i2c-tutorial.html

Please note that the master does not implement the whole standard as it supports only writing to a slave. The Master interface to the CPU is as follows:

Port	Size	Direction	Description
ADDR	2	In	Has the address of the I/O register to be read or to be written. There are four of them: 00: AU register (write only); 8 bits 01: DU register (write only); 8 bits 10: GO (write only); 1 bit 11: STATUS (read only); 2 bits; bit 0: done, bit 1: success
DataIn	8	In	Data bus carrying the data into the master
DataOut	8	Out	Data bus carrying the data off the master
R/W	1	In	Read (1)/Write (0) control
En	1	In	The master responds to R/W if and only if En is 1