Error Correction Encoder & Decoder

Digital Design and Logical Synthesis for Electric Computer Engineering

(36113611)

Course Project

Verification

Version 3.0

Revision Log

Rev	Description	Done By	Date
0.1	Initial document	Refael Ben Maor Tal Kapelnik	2.12.21
0.2	Digital Changes	Refael Ben Maor Tal Kapelnik	14.12.21
0.3	Functional Verification	Refael Ben Maor Tal Kapelnik	23.12.21
0.4	Synthesis	Refael Ben Maor Tal Kapelnik	30.12.21

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3. INTRODUCTION

3.1 Design Constraints Requirements

Initial system constraints to use in the synthesis flow are as follows:

Constraint Type	Value
Clock Period	At least 100KHz
Clock uncertainty	Maximum 0.1 ns
Clock transition time	Maximum 0.1 ns
Input delay	Maximum 0.2 ns
Input transition	Maximum 0.1 ns
Output delay	Maximum 0.5 ns
Design area	Smaller than 50,000,000
Wire load model	tsmc18_wl50

Table 1: Design Constraints Requirements.

3.2 The Used Constraints

False Path			
From Pin/Port	Through Pin	To Pin/Port	Comments
Clock Definitions			
Constraint Name	CLK		Comment
Period [Nano Seconds]	7.5		$Duty\ Cycle - 50\%$
Pin/Port name	clk		
Uncertainty	0.1		
Transition	0.1		
External Delay [Nano Seconds]			
Pin name	Value		Comment
All pins	0.5		

Table 2: Used Constraints

4. REPORTS & RESULTS OF SYNTHESIS FLOW

4.1 Synthesis Flow

Synthesis done by these steps:

1. Using the Ubuntu to use the DC program
2. Writing the Synthesis.tcl in Tcl for the setup and constrains
3. Move the RTL files into the DC folder
4. Compiling the program via dc_shell
5. Using the report output files for further analyze

4.2 Area Report

```
****************************************
Report : area
Design : ECC_ENC_DEC
Version: O-2018.06-SP4
Date   : Tue Dec 28 13:26:29 2021
****************************************

Library(s) Used:

    slow (File: /users/agnon/pp2021/benmaorr/Desktop/verilogEncDec-main/EncDec_D/EncDec_D_lib/hdl/DC/DC/LibraryFiles/db/slow.db)

Number of ports:                          481
Number of nets:                          2162
Number of cells:                         1770
Number of combinational cells:           1472
Number of sequential cells:               294
Number of macros/black boxes:               0
Number of buf/inv:                        534
Number of references:                     107

Combinational area:              39883.536441
Buf/Inv area:                    11456.121727
Noncombinational area:           23284.800095
Macro/Black Box area:                0.000000
Net Interconnect area:         1023171.981094

Total cell area:                 63168.336535
Total area:                    1086340.317630
```

Figure 1: Area Report 7.5ns

As we can see, The DUT stands with the assignment constraints. The area limit was $50000000\ \mu m^2$, and out DUT turned out to be $1086340\ \mu m^2$ which is $1.086\ mm^2$.

If we need a smaller design, we can make our clock slower than$7.5\ ns$, which is the minimal clock this DUT can handle, for example if we take clock with period of $10\ ns$ we get this report -

```
****************************************
Report : area
Design : ECC_ENC_DEC
Version: O-2018.06-SP4
Date   : Tue Dec 28 13:06:36 2021
****************************************

Library(s) Used:

    slow (File: /users/agnon/pp2021/benmaorr/Desktop/verilogEncDec-main/EncDec_D/EncDec_D_lib/hdl/DC/DC/LibraryFiles/db/slow.db)

Number of ports:                          481
Number of nets:                          1920
Number of cells:                         1528
Number of combinational cells:           1230
Number of sequential cells:               294
Number of macros/black boxes:               0
Number of buf/inv:                        382
Number of references:                      98

Combinational area:              29179.181012
Buf/Inv area:                     6127.228852
Noncombinational area:           21721.391998
Macro/Black Box area:                0.000000
Net Interconnect area:          972771.716095

Total cell area:                 50900.573010
Total area:                    1023672.289105
```

Figure 2: Area Report 10ns

As we can see we saved $0.063\ mm^2$ area by just changing the clock period to a slower frequency.

4.3 Timing Report

```
ECC_ENC_DEC        tsmc18_wl50           slow

Point                                                   Incr       Path
-----------------------------------------------------------------------------
clock clk (rise edge)                                   0.00       0.00
clock network delay (ideal)                             0.00       0.00
current_state_reg[2]/CK (DFFRHQX4)                      0.00       0.00 r
current_state_reg[2]/Q (DFFRHQX4)                       0.50       0.50 r
U656/Y (BUFX20)                                         0.29       0.78 r
U809/Y (OR2X4)                                          0.45       1.23 r
U579/Y (BUFX20)                                         0.33       1.56 r
U757/Y (INVX12)                                         0.30       1.86 f
U826/Y (INVX8)                                          0.24       2.10 r
U725/Y (CLKINVX4)                                       0.17       2.28 f
U990/Y (OAI222X4)                                       0.54       2.82 r
U849/Y (BUFX20)                                         0.22       3.03 r
Num_Of_Errors/DATA_IN[0] (Num_Of_Errors)                0.00       3.03 r
Num_Of_Errors/U52/Y (XOR2X1)                            0.62       3.65 r
Num_Of_Errors/U61/Y (OAI222X4)                          0.53       4.18 f
Num_Of_Errors/U43/Y (BUFX20)                            0.19       4.36 f
Num_Of_Errors/U25/Y (NAND4BBX4)                         0.27       4.63 f
Num_Of_Errors/U37/Y (AOI2BB1X4)                         0.35       4.98 f
Num_Of_Errors/NOF[1] (Num_Of_Errors)                    0.00       4.98 f
U971/Y (BUFX20)                                         0.21       5.19 f
Error_fix/NOF[1] (Error_fix_DATA_WIDTH32)               0.00       5.19 f
Error_fix/U69/Y (NAND4BBX4)                             0.30       5.49 f
Error_fix/U232/Y (BUFX20)                               0.23       5.72 f
Error_fix/U59/Y (BUFX20)                                0.15       5.87 f
Error_fix/U85/Y (OR2X4)                                 0.36       6.23 f
Error_fix/U234/Y (INVX8)                                0.17       6.40 r
Error_fix/U92/Y (NAND2BX4)                              0.25       6.65 r
Error_fix/U94/Y (NAND3X4)                               0.19       6.84 f
Error_fix/U274/Y (MX2X4)                                0.40       7.24 f
Error_fix/Dec_Out_reg[30]/D (DFFRXL)                    0.00       7.24 f
data arrival time                                                  7.24

clock clk (rise edge)                                   7.50       7.50
clock network delay (ideal)                             0.00       7.50
clock uncertainty                                      -0.10       7.40
Error_fix/Dec_Out_reg[30]/CK (DFFRXL)                   0.00       7.40 r
library setup time                                     -0.16       7.24
data required time                                                 7.24
-----------------------------------------------------------------------------
data required time                                                 7.24
data arrival time                                                 -7.24
-----------------------------------------------------------------------------
slack (MET)                                                        0.00
```

Figure 3: Timing Report 7.5ns

From this timing report, we show the lowest period of clock that we can have in our design before we are getting negative slack. With this period, we get the critical path in the image above. We can make our period faster, if we will improve this critical path.

```
---------------------------------------------------
ECC_ENC_DEC        tsmc18_wl50           slow

Point                                                 Incr       Path
-----------------------------------------------------------------------------
clock clk (rise edge)                                 0.00       0.00
clock network delay (ideal)                           0.00       0.00
Register_selctor/CODEWORD_WIDTH_reg[0]/CK (DFFRHQX2)
                                                      0.00       0.00 r
Register_selctor/CODEWORD_WIDTH_reg[0]/Q (DFFRHQX2)   0.67       0.67 r
Register_selctor/U3/Y (BUFX16)                        0.26       0.93 r
Register_selctor/CODEWORD_WIDTH[0] (Register_selctor_AMBA_WORD32)
                                                      0.00       0.93 r
U541/Y (INVX8)                                        0.10       1.04 f
U638/Y (OR2X4)                                        0.32       1.35 f
U438/Y (CLKBUFX16)                                    0.43       1.78 f
U437/Y (INVX4)                                        0.97       2.75 r
Error_fix/Medium (Error_fix_DATA_WIDTH32)             0.00       2.75 r
Error_fix/U102/Y (INVXL)                              0.61       3.36 f
Error_fix/U72/Y (NOR2X1)                              1.94       5.29 r
Error_fix/U152/Y (CLKINVX3)                           2.77       8.06 f
Error_fix/U43/Y (OAI222X1)                            1.52       9.59 r
Error_fix/Dec_Out_reg[18]/D (DFFRHQX1)                0.00       9.59 r
data arrival time                                                9.59

clock clk (rise edge)                                10.00      10.00
clock network delay (ideal)                           0.00      10.00
clock uncertainty                                    -0.10       9.90
Error_fix/Dec_Out_reg[18]/CK (DFFRHQX1)               0.00       9.90 r
library setup time                                   -0.29       9.61
data required time                                               9.61
-----------------------------------------------------------------------------
data required time                                               9.61
data arrival time                                               -9.59
-----------------------------------------------------------------------------
slack (MET)                                                      0.02
```

Figure 4: Timing Report 10ns

We did also try a period of 10 ns, for compering between two periods. As we can see, the critical path got shorter but took longer, and we also got positive slack, which says that we do not have good constrain and we can improve it.

4.4 Power Report

```
ECC_ENC_DEC            tsmc18_wl50       slow


Global Operating Voltage = 1.62
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   2.7024 mW   (84%)
  Net Switching Power  = 529.8959 uW   (16%)
                         ---------
Total Dynamic Power    =   3.2323 mW  (100%)

Cell Leakage Power     =   3.2586 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000            0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000            0.0000  (   0.00%)
register           2.6624        2.6620e-02          7.9852e+05           2.6898  (  83.13%)
sequential         0.0000           0.0000              0.0000            0.0000  (   0.00%)
combinational   3.9992e-02          0.5033          2.4601e+06           0.5457  (  16.87%)
--------------------------------------------------------------------------------------------------
Total              2.7024 mW        0.5299 mW       3.2586e+06 pW         3.2355 mW
```

Figure 5: Power Report 7.5ns

As we can see most of our power is going to the registers, what can tell us if we want better performance, we need to improve them by for example by clock gating, to prevent unnecessary toggling. For example in our design we can use clock gating on the main state machine.

4.5 Constraints Violations

```
****************************************
Report : constraint
         -all_violators
Design : ECC_ENC_DEC
Version: O-2018.06-SP4
Date   : Tue Dec 28 13:26:29 2021
****************************************

This design has no violated constraints.
```

Figure 6: Constraints Report

In our design we did not get any violations.

4.6 Check Design

```
****************************************
check_design summary:
Version:     O-2018.06-SP4
Date:        Tue Dec 28 13:26:29 2021
****************************************

                   Name                                            Total
--------------------------------------------------------------------------------
Inputs/Outputs                                                     18
    Unconnected ports (LINT-28)                                    18
--------------------------------------------------------------------------------

Warning: In design 'ECC_ENC_DEC', port 'PADDR[19]' is not connected to any nets. (LINT-28)
Warning: In design 'ECC_ENC_DEC', port 'PADDR[18]' is not connected to any nets. (LINT-28)
Warning: In design 'ECC_ENC_DEC', port 'PADDR[17]' is not connected to any nets. (LINT-28)
Warning: In design 'ECC_ENC_DEC', port 'PADDR[16]' is not connected to any nets. (LINT-28)
Warning: In design 'ECC_ENC_DEC', port 'PADDR[15]' is not connected to any nets. (LINT-28)
Warning: In design 'ECC_ENC_DEC', port 'PADDR[14]' is not connected to any nets. (LINT-28)
Warning: In design 'ECC_ENC_DEC', port 'PADDR[13]' is not connected to any nets. (LINT-28)
Warning: In design 'ECC_ENC_DEC', port 'PADDR[12]' is not connected to any nets. (LINT-28)
Warning: In design 'ECC_ENC_DEC', port 'PADDR[11]' is not connected to any nets. (LINT-28)
Warning: In design 'ECC_ENC_DEC', port 'PADDR[10]' is not connected to any nets. (LINT-28)
Warning: In design 'ECC_ENC_DEC', port 'PADDR[9]' is not connected to any nets. (LINT-28)
Warning: In design 'ECC_ENC_DEC', port 'PADDR[8]' is not connected to any nets. (LINT-28)
Warning: In design 'ECC_ENC_DEC', port 'PADDR[7]' is not connected to any nets. (LINT-28)
Warning: In design 'ECC_ENC_DEC', port 'PADDR[6]' is not connected to any nets. (LINT-28)
Warning: In design 'ECC_ENC_DEC', port 'PADDR[5]' is not connected to any nets. (LINT-28)
Warning: In design 'ECC_ENC_DEC', port 'PADDR[4]' is not connected to any nets. (LINT-28)
Warning: In design 'ECC_ENC_DEC', port 'PADDR[1]' is not connected to any nets. (LINT-28)
Warning: In design 'ECC_ENC_DEC', port 'PADDR[0]' is not connected to any nets. (LINT-28)
```

Figure 7: Check Design Report

As we can see we got only warning about the unconnected PADDR. The reason is that we use only the PADDR[3:2] bits in our design, we don’t need the rest of the bits, because they not effective for the functionality, its only for a purpose of reading/writing.

5. APPENDIX

5.1 Terminology

LSB - Least Significant Bit

TBR - To Be Reviewed

TBD - To Be Defined

IF - Inteface

DUT - Device Under Test

GM - Golden Model

tb - Test Bench