NCTU-EE IC LAB – Fall2021

Online Test

Design: Geofence

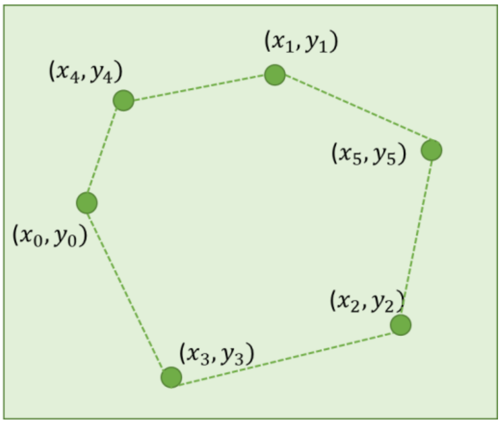
Data Preparation

1. Extract test data from TA’s directory:

   % tar -xvf ~iclabta01/OT_2021_fall.tar

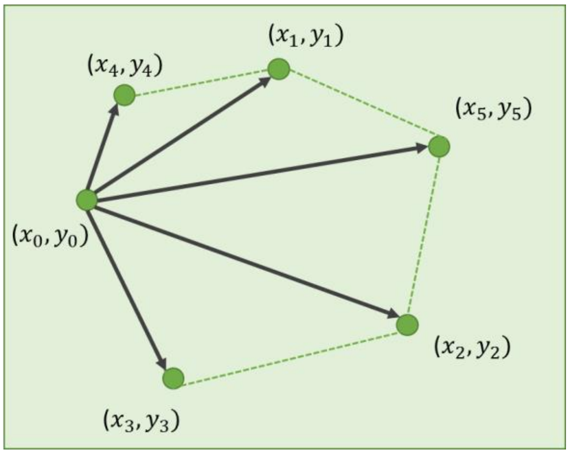
Design Description

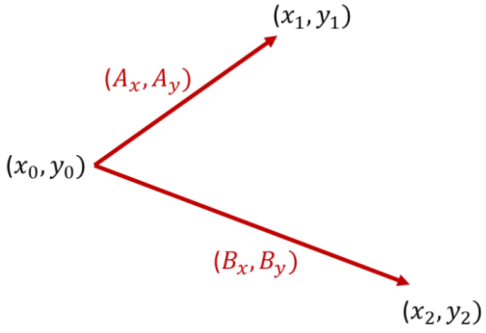
請大家完成一個**地理圍籬系統**，此系統使用**6顆接收器，**目的是在平面上建構出虛擬圍籬。



此系統**每次會輸入6個頂點的座標(x_i, y_i), $i = 0\sim5$**，且接收到的座標並不會照著圍籬順序，本次測驗目的在於**找到正確的座標順序並輸出**。

要排序座標順序，可將**一頂點作為原點**，和其他5個頂點形成五組向量，利用**計算向量外積**判斷兩組向量方向關係，進行排序讓前後向量固定維持順時針或逆時針關係，便可以求得6邊形頂點的順時針順序並輸出。





- **向量外積計算:**
  - 若有兩向量，向量A $= (A_x, A_y) = (x_1 - x_0, y_1 - y_0)$，向量B $= (B_x, B_y) = (x_2 - x_0, y_2 - y_0)$，
    則A和B的外積 $= \boldsymbol{A_x \times B_y - B_x \times A_y}$
    若外積結果< 0 ，表示B在A的順時針方向(A到B順時針夾角$< 180°$)，反之則為逆時針方向
  - **最後請以第一個輸入座標為起點，逆時針方向照順序輸出6個頂點座標**

- **六邊形面積計算:**
  - 若要計算六邊形面積，可使用相關公式：
  - 已知一多邊形，其頂點依逆時針排列座標為(x_0, y_0)、$(x_1, y_1) \ldots \ldots (x_{n-1}, y_{n-1})$，
  - 此多邊形面積 $= \frac{1}{2}\left(\begin{vmatrix} x_0 & x_1 \\ y_0 & y_1 \end{vmatrix} + \begin{vmatrix} x_1 & x_2 \\ y_1 & y_2 \end{vmatrix} + \begin{vmatrix} x_2 & x_3 \\ y_2 & y_3 \end{vmatrix} + \cdots + \begin{vmatrix} x_{n-1} & x_0 \\ y_{n-1} & y_0 \end{vmatrix}\right)$
    $= \frac{1}{2}\left((x_0y_1 - x_1y_0) + (x_1y_2 - x_2y_1) + \cdots + (x_{n-1}y_0 - x_0y_{n-1})\right)$

    EX: 以n=6，**六邊形面積** $= \frac{1}{2}\left((x_0y_1 - x_1y_0) + (x_1y_2 - x_2y_1) + (x_2y_3 - x_3y_2) + (x_3y_4 - x_4y_3) + (x_4y_5 - x_5y_4) + (x_5y_0 - x_0y_5)\right)$
    若頂點順序為順時針，則上式為負值。

- **Notice：**
  - 因為計算面積公式中有除以二，故**Area 面積輸出取floor function**
    EX: 六邊形面積 $= \lfloor \frac{1}{2}(1+1+1+2+1+1) \rfloor = \lfloor 3.5 \rfloor = 3$
  - 本次測驗的pattern皆為**凸六邊形**

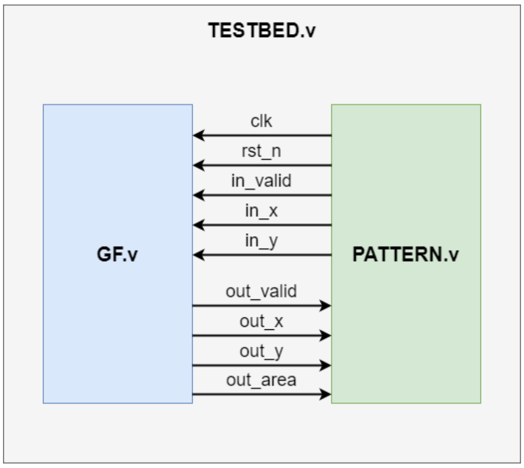
Input Signal	Bit Width	Definition
clk	1	Clock.
rst_n	1	Asynchronous active-low reset.
in_valid	1	High when input signals are valid.
in_x	10	The input x coordinate.
in_y	10	The input y coordinate.

Output Signal	Bit Width	Definition
out_valid	1	High when output is valid.
out_x	10	The output x coordinate.
out_y	10	The output y coordinate.
out_area	24	Area of hexagon *(Bonus)*

Inputs

1. The **in_x[9:0]** and **in_y[9:0]** might be valid 6 cycles when **in_valid is high.**
2. All input signals will be synchronized at **negative edge** of the clock.
3. The next input pattern will be triggered 1 ~ 5 cycles after **out_valid** falls.

Outputs



1. All outputs should be low after **rst_n** assert
2. **out_valid** should not be raised when **in_valid** is high.
3. Output signals should be synchronized at clock positive edge.
4. **out_valid** is set to high when the output value is valid and it will be high for 6 cycles continuously when triggered.
5. TA’s pattern will capture your output for checking at **negative** clock edge.

Specifications

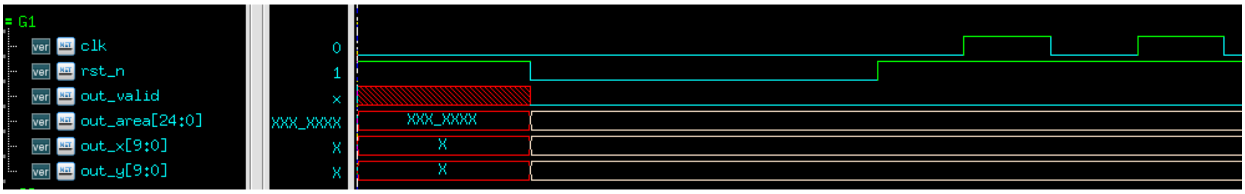
1. Top module name：GF (Filename: GF.v)
2. It is asynchronous reset and active-low architecture. If you use synchronous reset (reset after clock starting) in your design, you may fail to reset signals.
3. The clock period of the design is **10ns.**
4. The **rst_n** would be triggered only once. All output signals should be reset to low after the reset signal is asserted.
5. The out_valid and output data must be asserted successively **6** cycles.
6. The next group of inputs will come in 1~5 cycles after your out_valid pull down.
7. The synthesis result of data type cannot include any LATCH.
8. The slack in the timing report should be non-negative and the result should be MET.
9. The gate level simulation cannot include any timing violation.
10. The latency of your design in each pattern should not be larger than 10000 cycles.
11. The look-up table method is forbidden. (TA will check your design)
12. Don’t use any wire/reg/submodule/parameter name called *error*, *congratulation*, *latch* or *fail* otherwise you will fail the lab. Note: * means any char in front of or behind the word. e.g: error_note is forbidden.
13. Don’t write Chinese comments or other language comments in the file you turned in.
14. Verilog commands//synopsys dc_script_begin, //synopsys dc_script_end, //synopsys translate_off, //synopsys translate_on are only allowed during the usage of including and setting designware IPs, other design compiler optimizations are forbidden.
15. Using the above commands are allowed, however any error messages during synthesize and simulation, regardless of the result will lead to failure in this lab.
16. Any form of display or printing information in verilog design is forbidden. You may use this methodology during debugging, but the file you turn in should not contain any coding that is not synthesizable.

Grading Policy

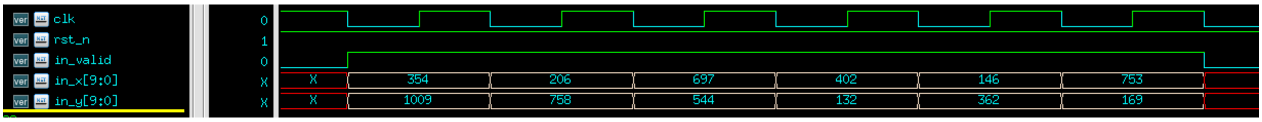
- **Functionality (85%) + Performance (15%)**
- **Performance(15%):** Latency x Area
- The smaller the performance index is, the higher score you can get.
- 繳交方式：執行 OT_2021_fall/09_SUBMIT/01_submit
- 請於考試結束前繳交檔案
  - Deadline：A組：15:45, B組：19:00
- Demo 與 繳交注意事項
  - **禁止使用 linux01，要保留作為demo使用**
  - demo機會**只有一次**，只要通過助教提供的PATTERN測資即可通過 functionality 並計算其performance
  - 09_SUBMIT/01_submit 是繳交檔案的意思，不代表demo，在Deadline內可重複繳交
  - 09_SUBMIT/02_check 是下載繳交檔案的意思，可確認目前繳交的版本與狀態
  - 助教demo時，會檢查檔案是否有繳交，以及檔案最後時間，因此若是填寫表單提前demo同學務必要先執行繳交再來填寫demo表單
  - 在考試開始至截止前30分鐘，可以來助教的電腦填寫demo表單，提早知道結果
  - 在考試截止前30分鐘內，不用填寫表單，助教會統一回去demo後公告結果
  - 使用筆電的同學，請於當天晚上8:00前上傳螢幕錄影於下方資料夾(iclabxxx.mp4): https://drive.google.com/drive/u/2/folders/1XRUA_j8s-U39zMrTv3ktTmMoB7HhrcKy
  - Demo 表單(可來前方使用助教電腦填寫，填完即用掉一次demo 機會) https://forms.gle/6vzBvgNexknrjous8
- **提醒同學，考試結束後請勿再更動帳號內的檔案，若改動使修改時間超過繳交時間，則當對demo結果有疑慮時，助教這邊將無法提供協助**

Sample Waveform

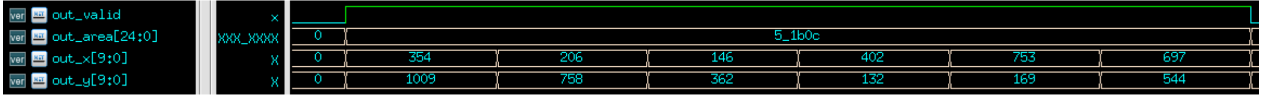
1. asynchronous reset and active-low and reset all output



2. 6 cycles for input



3. 6 cycles for output


out_valid
out_area[24:0]
out_x[9:0]
out_y[9:0]
x
XXX_XXXX
X
X
0
5_1b0c
0
354
206
146
402
753
697
0
1009
758
362
132
169
544