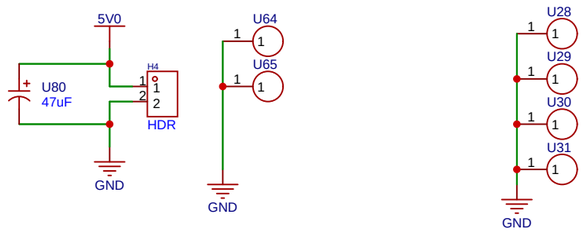
To do:
-Lots of schematic clean-up! Posting for now for those interested.
-Update board routing based on minor schematic changes since the board production.

To do:
-power off sequencing
-0.675 power indicator design (different mosfet for lower voltage?)
-Programming header HS3 should be 2.0mm instead of 2.54mm
-Move R267 from DDR to closer to SoC
-Moce C193 closer to U61
-Incorrect part # on 33MHz oscillator - installed 25MHz for now
-Additional oscillator for FPGA fabric (without Eth IC)?
-Power header for 3.3V
-Onboard LED for PL
-Onboard buttones for PS and PL
-Power rail selection jumpers don't seem to be needed. Always leave set to external DC barrel power.
-Improve Ethernet reset circuit?
-Add in HDMI controller (ADV7513?)
-Power coming in from HDMI connection - something needed to prevent this when the PCB is off?

Temporary fan header, mounting.
Replace based on actual fan selected.
To do: Fan control based on temp?



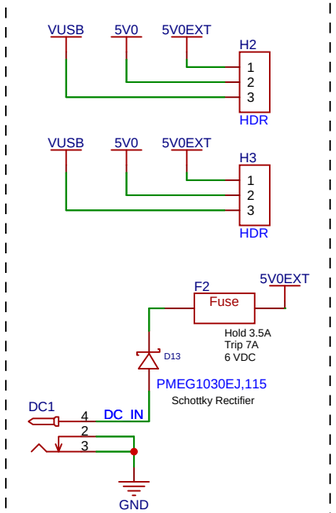
Schematic	schematic1	Update Date	2024-12-18
		Create Date	2024-11-09
Page	Misc	Part Number	
Drawn	rehsd	FPGA Dev Board - XILINX XC7Z020-1CLG484I v0.07	
Reviewed			
		VER / SIZE / PAGE 1 OF 13	
EasyEDA	V0.1	B	

SoC Bypass Capacitors

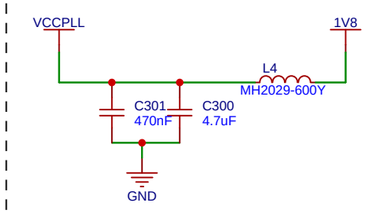
...

To do:
-Verify ferrite bead specs for analog power, PLL

DC Barrel, PWR Select

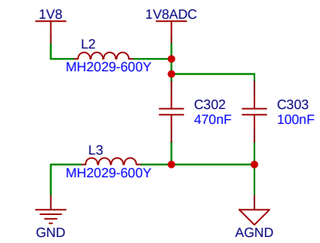


PLL

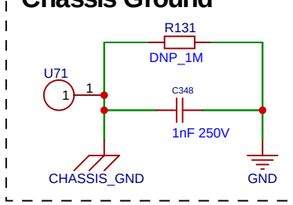


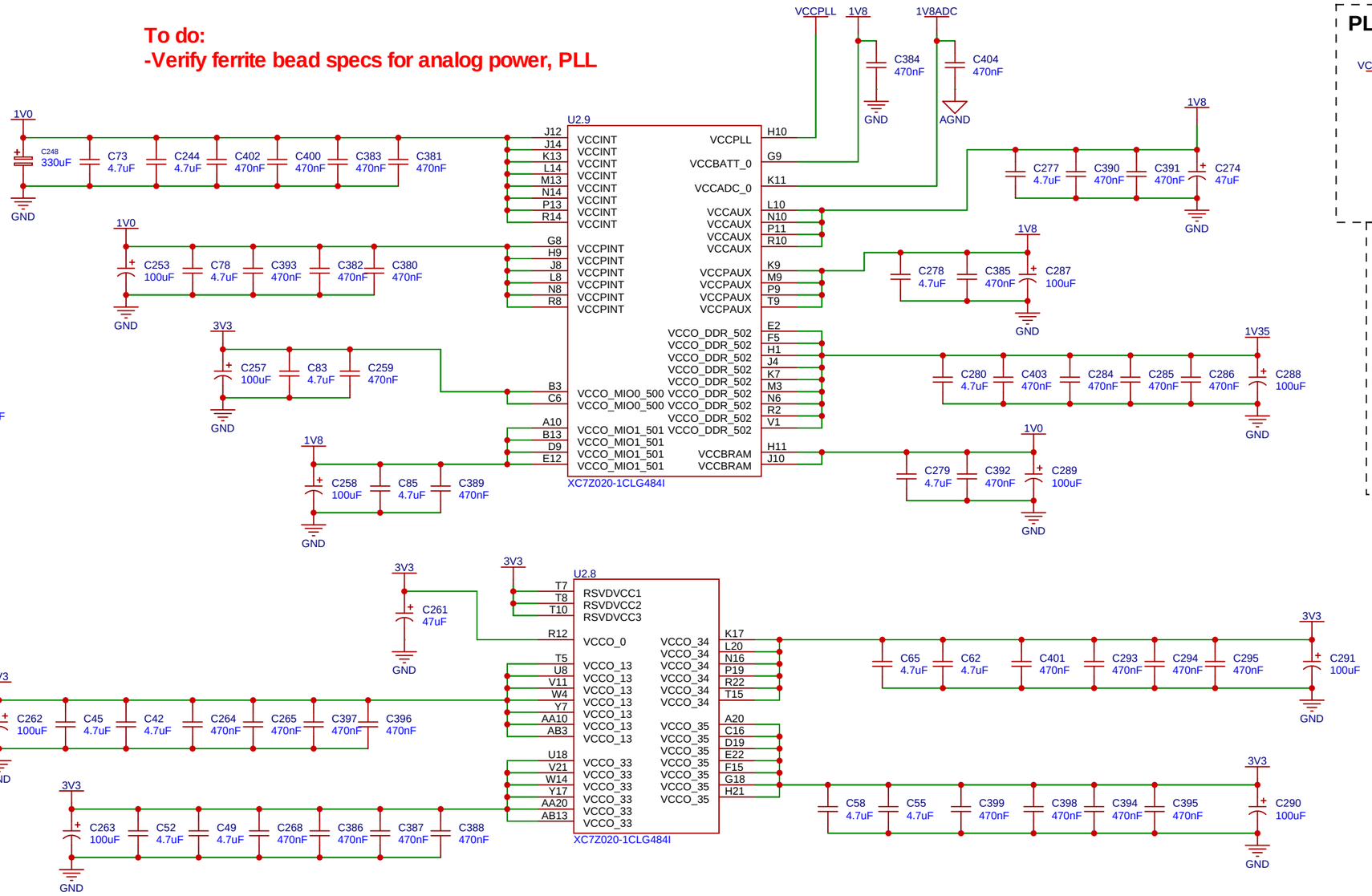
Analog

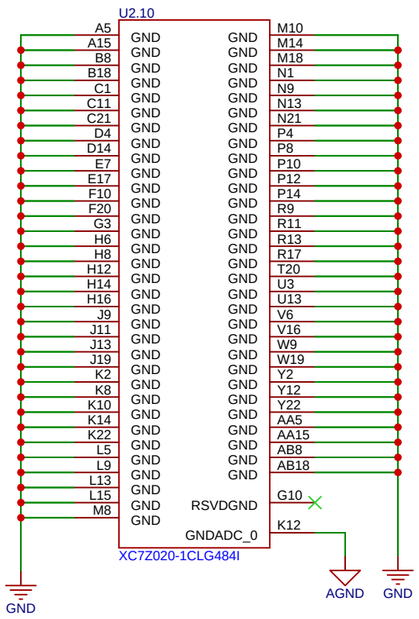
On-chip reference.
VCCAUX is using 1V8. See UG480.
*Need to select specific ferrites yet.



Chassis Ground







UG933

Table 3-1: **Required PCB Capacitor Quantities per Device (PL)**

Package	Device	V_{CCINT} 680 µF	V_{CCINT} 330 µF	V_{CCINT} 100 µF	V_{CCINT} 4.7 µF	V_{CCINT} 0.47 µF	V_{CCBRAM} 100 µF	V_{CCBRAM} 47 µF	V_{CCBRAM} 4.7 µF	V_{CCBRAM} 0.47 µF	V_{CCAUX} 47 µF	V_{CCAUX} 4.7 µF	V_{CCAUX} 0.47 µF	V_{CCAUX_IO} 47 µF	V_{CCAUX_IO} 4.7 µF	V_{CCAUX_IO} 0.47 µF	V_{CCO} per Bank[2][4] 47 µF or 100 µF	V_{CCO} per Bank[2][4] 4.7 µF	V_{CCO} per Bank[2][4] 0.47 µF	Bank 0 47 µF
CLG484	Z-7020	0	1	0	2	4	1	0	1	1	1	1	2	NA	NA	NA	1	2	4	1

Table 3-2: **Required PCB Capacitor Quantities per Device (PS) *(Cont'd)***

Package	Device	V_{CCPINT} 100 µF	V_{CCPINT} 4.7 µF	V_{CCPINT} 0.47 µF	V_{CCPAUX}[1] 100 µF	V_{CCPAUX}[1] 4.7 µF	V_{CCPAUX}[1] 0.47 µF	V_{CCO_DDR} 100 µF	V_{CCO_DDR} 4.7 µF	V_{CCO_DDR} 0.47 µF	V_{CCO_MIO0} 100 µF	V_{CCO_MIO0} 4.7 µF	V_{CCO_MIO0} 0.47 µF	V_{CCO_MIO1} 100 µF	V_{CCO_MIO1} 4.7 µF	V_{CCO_MIO1} 0.47 µF	V_{CCPLL}[2][3]	
CLG484	Z-7020	1	1	3	1	1	1	1	1	4	1	1	1	1	1	1		

Table 3-3: **PCB Capacitor Specifications**

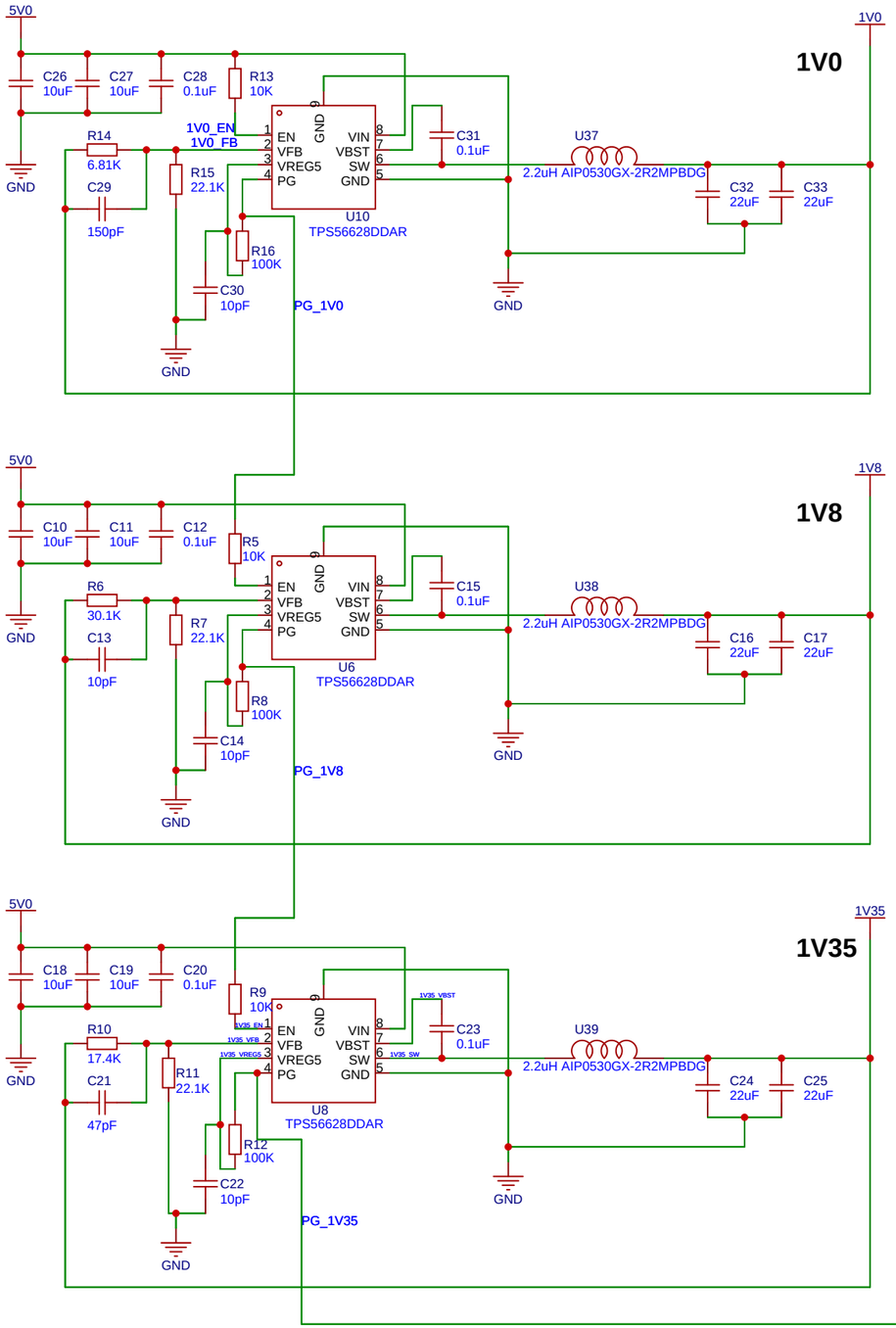
Ideal Value	Value Range[4]	Body Size[4]	Type	ESL Maximum	ESR Range[3]	Voltage Rating[4]	Suggested Part Number
680 µF	C > 680 µF	2917/D /7343	2-Terminal Tantalum	2.1 nH	5 mΩ < ESR < 40 mΩ	2.5V	T530X687M006ATE018
330 µF	C > 330 µF	2917/D /7343	2-Terminal Tantalum	2.0 nH	5 mΩ < ESR < 40 mΩ	2.5V	T525D337M006ATE025
330 µF	C > 330 µF	2917/D /7343	2-Terminal Niobium Oxide	2.0 nH	5 mΩ < ESR < 40 mΩ	2.5V	NOSD337M002#0035
100 µF	C > 100 µF	1210	2-Terminal Tantalum, Ceramic X7R, X7U, or X5R	1 nH	1 mΩ < ESR < 40 mΩ	2.5V	GRM32EE70G107ME19
47 µF	C > 47 µF	1210	2-Terminal Ceramic X7R or X5R	1 nH	1 mΩ < ESR < 40 mΩ	6.3V	GRM32ER70J476ME20L
10 µF	C = 10 µF	0603	2-Terminal Ceramic X7R or X5R	0.25 nH	5 mΩ	4.0V	GRM188R60G106ME47
4.7 µF	C > 4.7 µF	0805	2-Terminal Ceramic X7R or X5R	0.5 nH	1 mΩ < ESR < 20 mΩ	6.3V	GRM21BR71A475KA73
0.47 µF	C > 0.47 µF	0603	2-Terminal Ceramic X7R or X5R	0.5 nH	1 mΩ < ESR < 20 mΩ	6.3V	GRM188R70J474KA01

Schematic	schematic1	Update Date	2024-11-11
		Create Date	2024-11-09
Page	Power	Part Number	
Drawn	rehsd	FPGA Dev Board - XILINX XC7Z020-1CLG484I v0.07	
Reviewed			
		VER	SIZE
		V0.1	B

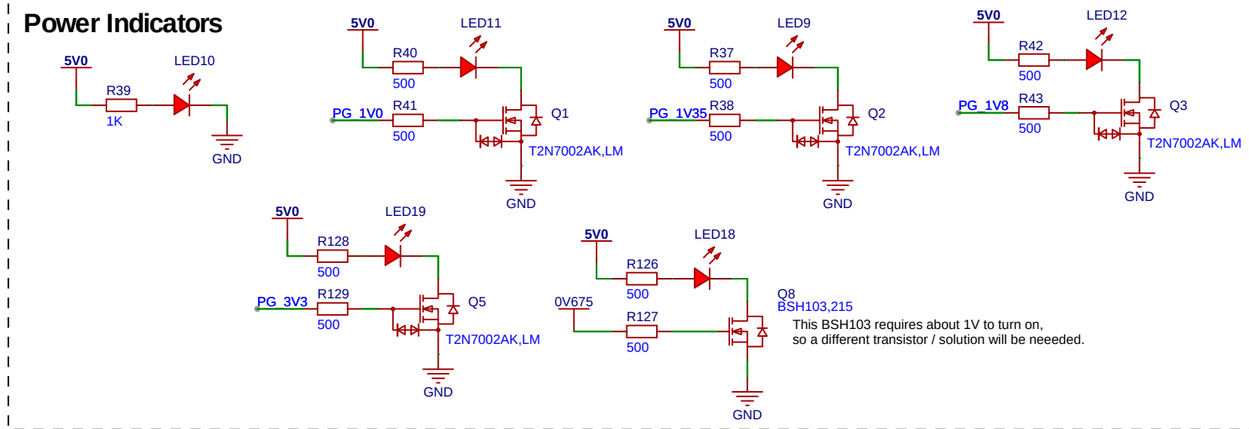
EasyEDA

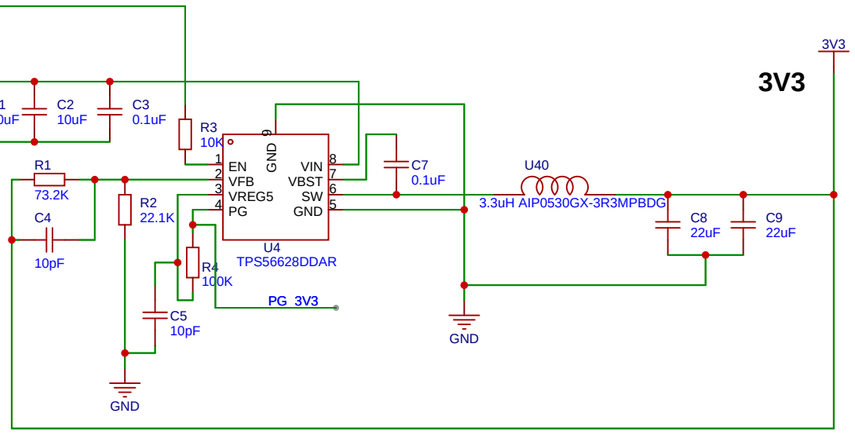
Buck Converters

Sequence: 1V0, 1V8, 1V35, 3V3

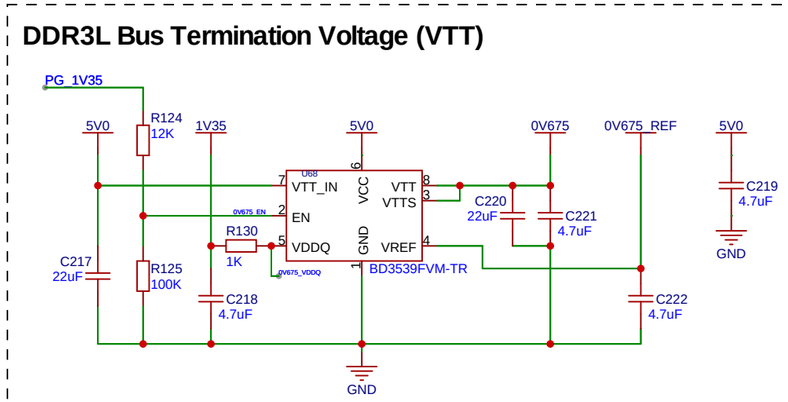


Power Indicators





DDR3L Bus Termination Voltage (VTT)



Schematic	schematic1	Update Date	2024-11-12
		Create Date	2024-11-09
Page	Regulators	Part Number	
Drawn	rehsd	FPGA Dev Board - XILINX XC7Z020-1CLG484I v0.07	
Reviewed			
		VER / SIZE / PAGE 3 OF 13	
EasyEDA	V0.1 / B	EasyEDA.com	

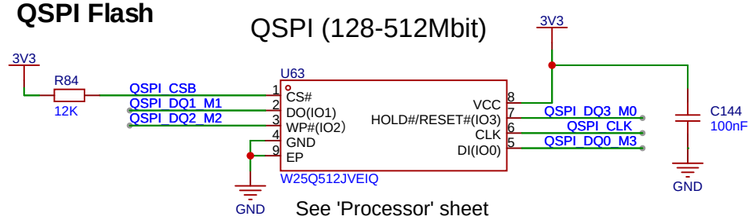
Programming

...

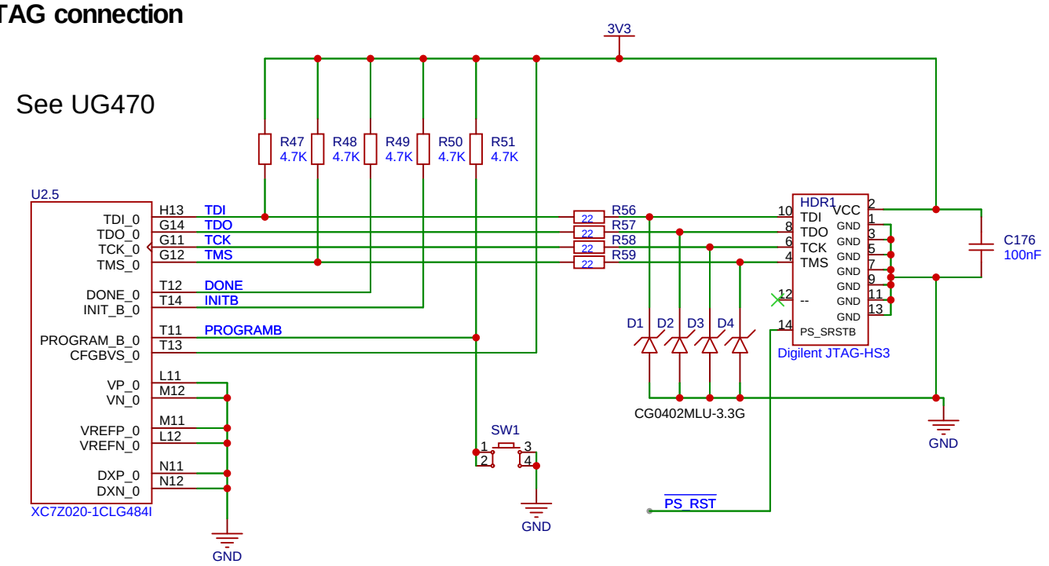
To do:

-

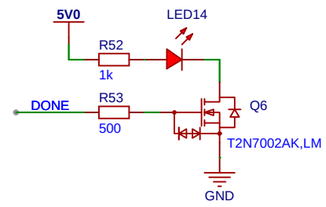
QSPI Flash



JTAG connection



Done indicator

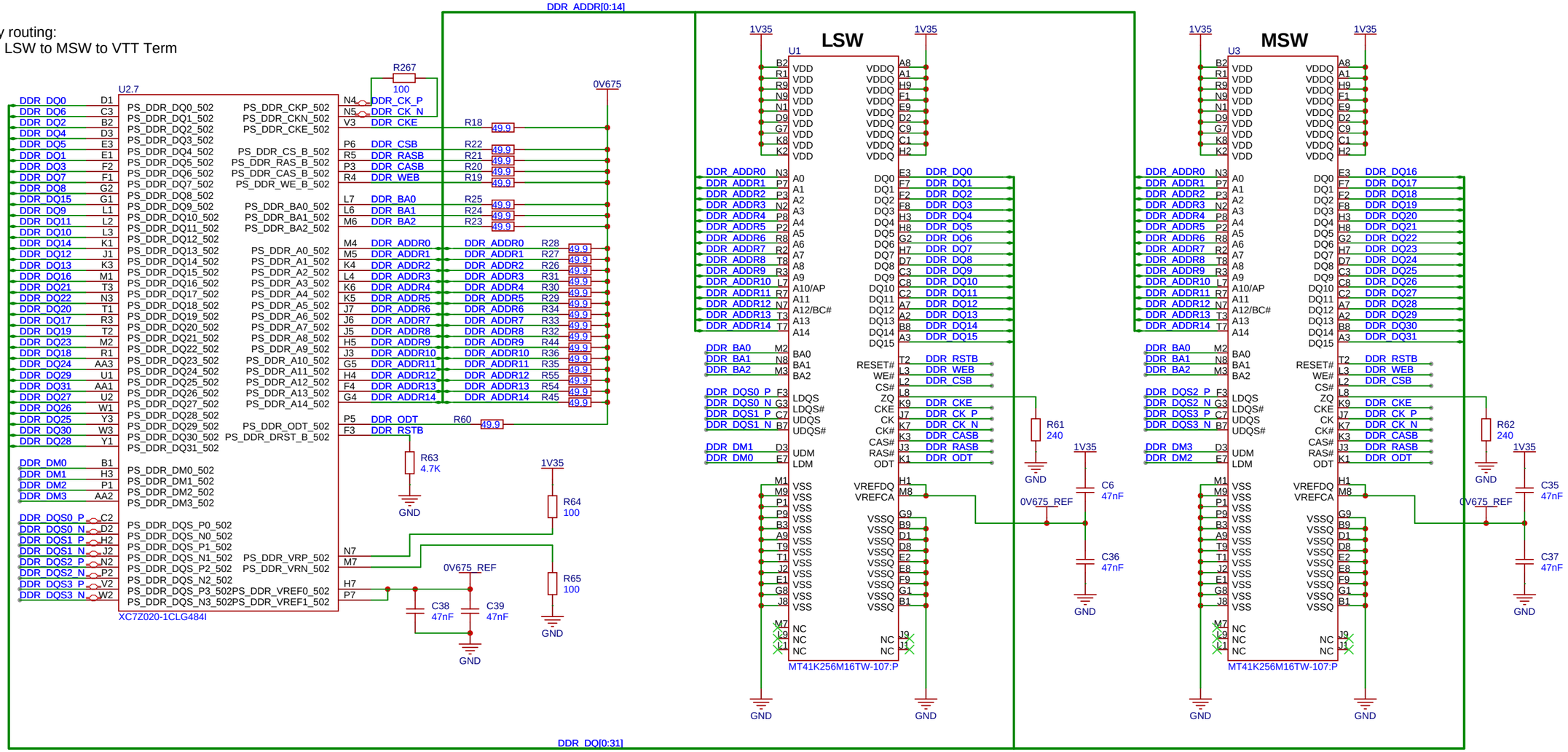


Schematic	schematic1	Update Date	2024-11-09
		Create Date	2024-11-09
Page	Program	Part Number	JLCPCB-002
Drawn	EasyEDA	FPGA Dev Board - XILINX XC7Z020-1CLG484I v0.07	
Reviewed	EasyEDA		
		VER / SIZE / PAGE 4 OF 13	
EasyEDA	V0.1 / A4	EasyEDA.com	

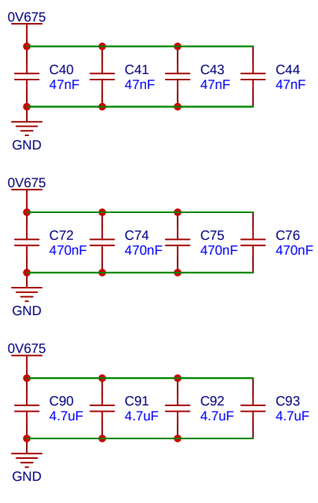
DDR3L

Fly-by routing:
PS to LSW to MSW to VTT Term

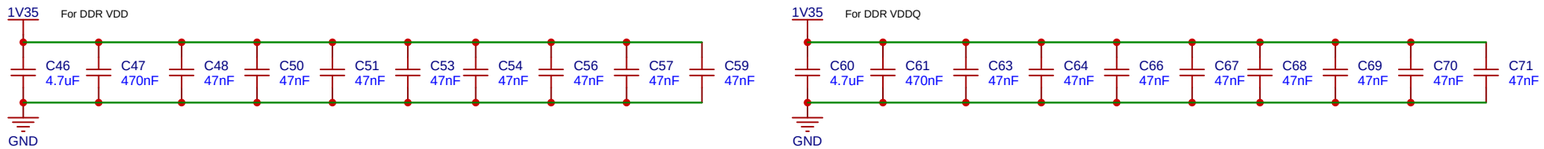
...



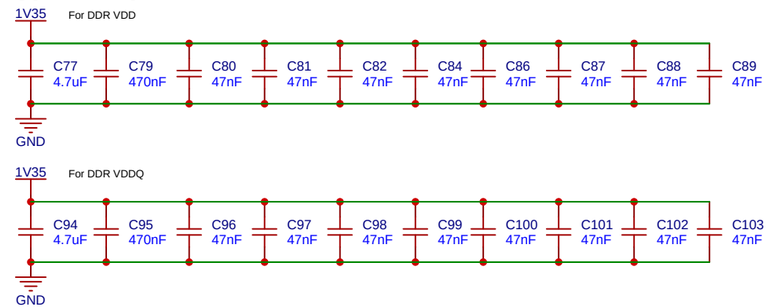
Bypass Caps DDR Term



Bypass Caps DDR MSW



Bypass Caps DDR LSW



Schematic	schematic1	Update Date	2024-11-09
Page	DDR3L	Create Date	2024-11-09
Drawn	rehsd	Part Number	
Reviewed		FPGA Dev Board - XILINX XC7Z020-1CLG484I v0.07	
		VER / SIZE / PAGE 5 OF 13	
EasyEDA	V0.1 / B	EasyEDA.com	

USB

Programming, Serial

USB-C Physical Connector
for Power, Programming

Should the two pairs of USB data lines be connected? Currently, the orientation of the data connection matters (flipping connector).

ADBUS4 pull-up to 3.3V
See https://etherealwake.com/2024/06/xilinx-ftdi-jtag/.

ADBUS7 (SRST_B) is an output that connects to the PS_SRST_B signal on Zynq parts. Like POR_B, this must be buffered with an open-collector output. See https://etherealwake.com/2024/06/xilinx-ftdi-jtag/.

From @asmi06: add a comparator (I use MCP6541T-E/OT) to pin ADBUS4 such that if your board is powered externally (and not through USB - which is how most of my boards are powered because USB just doesn't provide enough juice for devices like Artix-A100T), ADBUS4 would only go high if main power is connected

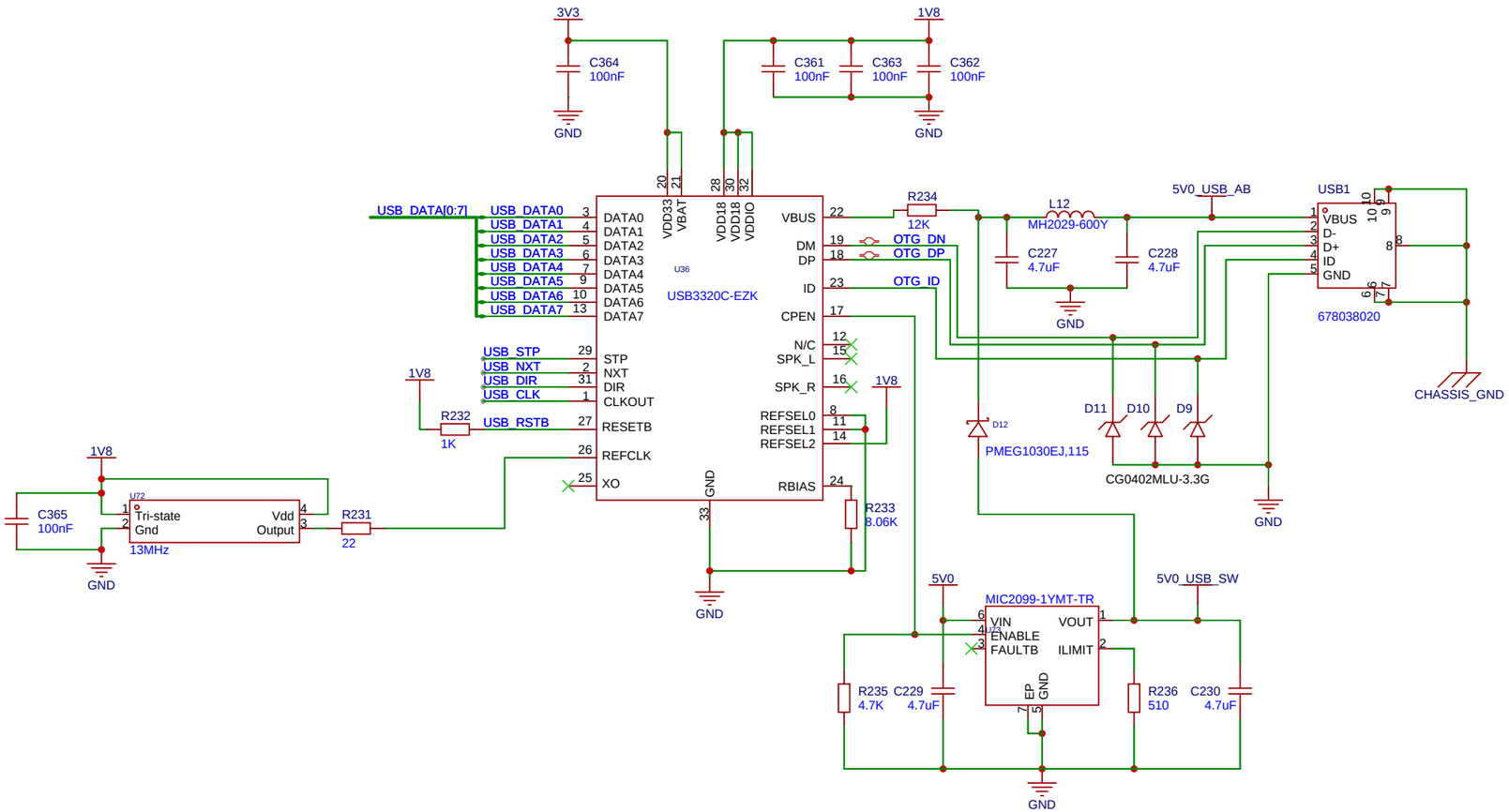
See UG908

-added 12K pullups on CLK and CS

Schematic	schematic1	Update Date	2024-12-06
		Create Date	2024-11-09
Page	USB FT2232	Part Number	JLCPCB-002
Drawn	EasyEDA	FPGA Dev Board - XILINX XC7Z020-1CLG484I v0.07	
Reviewed	EasyEDA		
		VER	SIZE	PAGE 6 OF 13
EasyEDA		V0.1	A4	EasyEDA.com

USB OTG

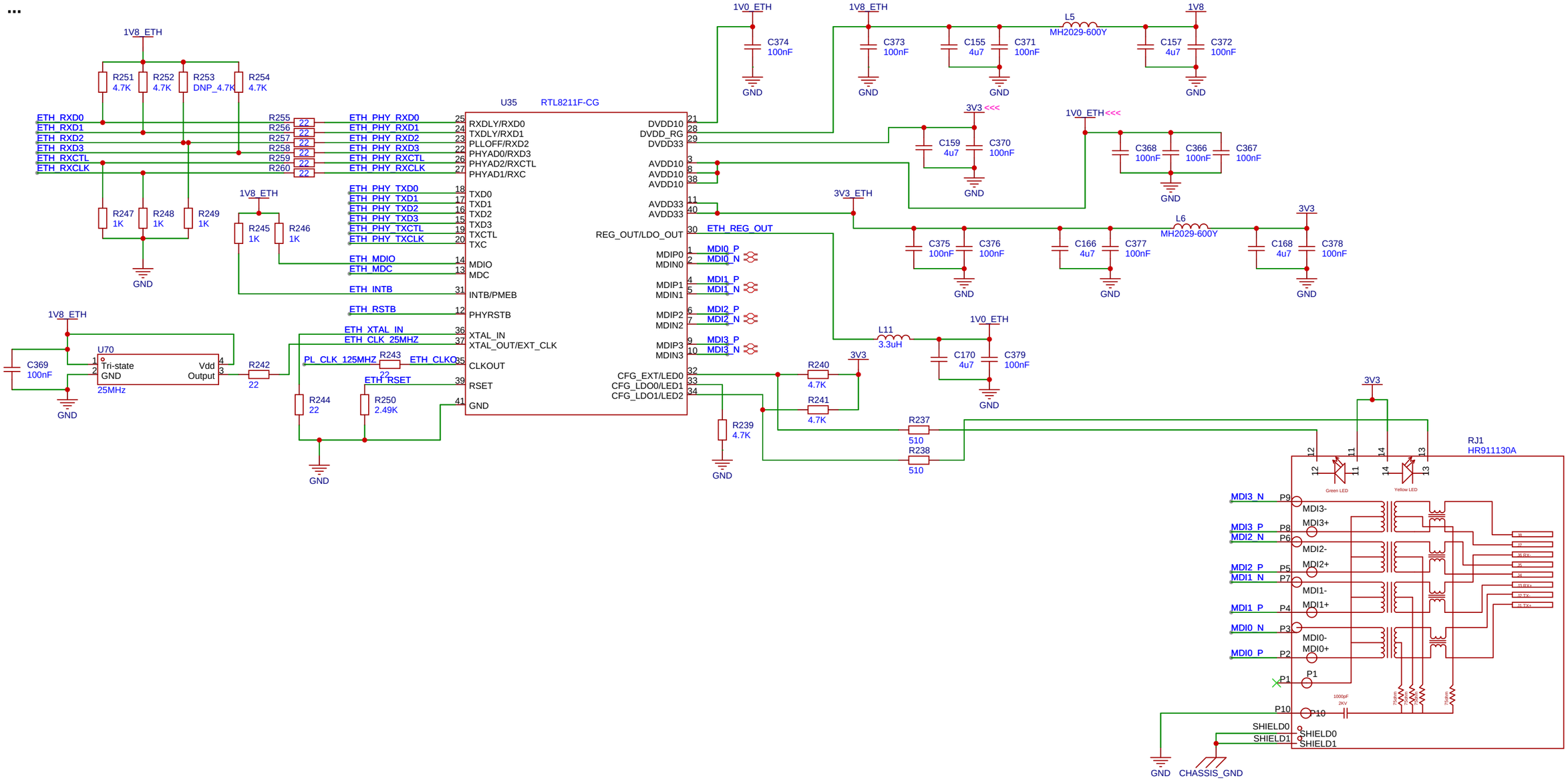
USB 2.0 ULPI PHY



Schematic	schematic1	Update Date	2024-11-09
		Create Date	2024-11-09
Page	USB USB3320	Part Number	JLCPCB-002
Drawn	EasyEDA	FPGA Dev Board - XILINX XC7Z020-1CLG484I v0.07	
Reviewed	EasyEDA		
		VER	SIZE / PAGE 7 OF 13
EasyEDA		V0.1	A4 / EasyEDA.com

Ethernet

...



Schematic	schematic1	Update Date	2024-12-01
		Create Date	2024-11-09
Page	Ethernet	Part Number	JLCPCB-002
Drawn	EasyEDA	FPGA Dev Board - XILINX XC7Z020-1CLG484I v0.07	
Reviewed	EasyEDA		
		VER	SIZE	PAGE 8 OF 13
EasyEDA		V0.1	A4	EasyEDA.com

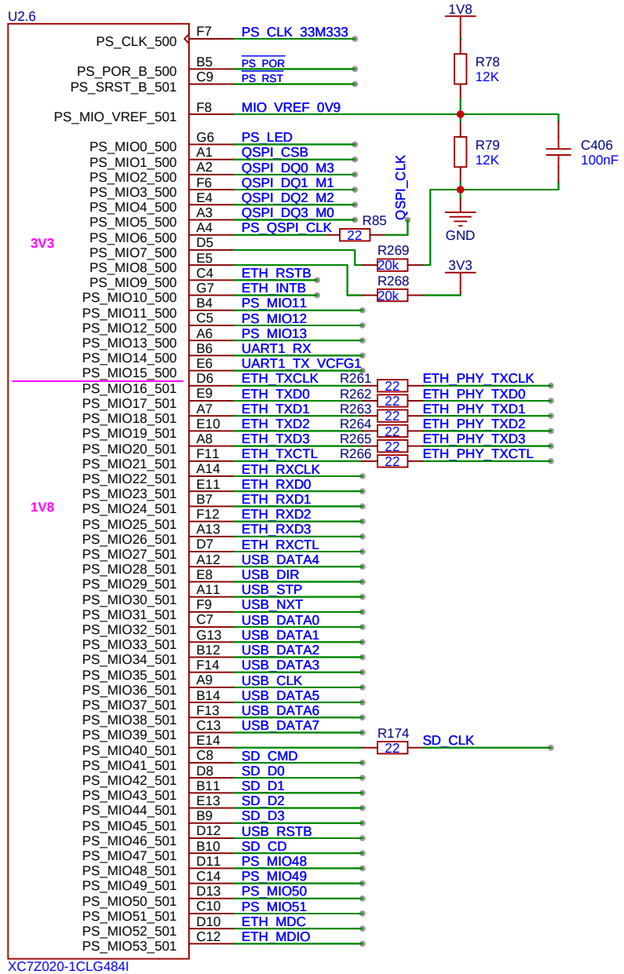
Processing System

...

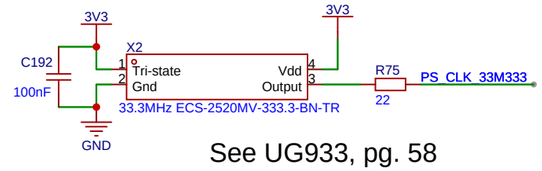
Configure PS pinouts Vivado!

MIO0 (_500) is 3V3

MIO1 (_501) is 1V8 HSTL
ETH
USB



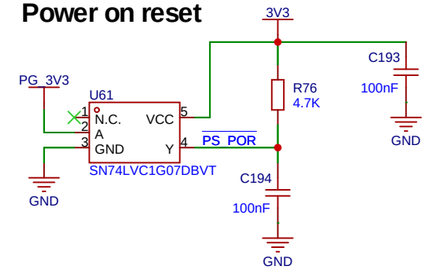
PS Clock



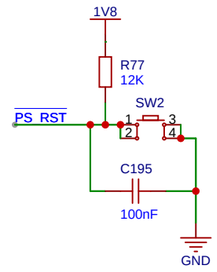
See UG933, pg. 58

30-60 MHz OK
33.333 MHz is tooling default

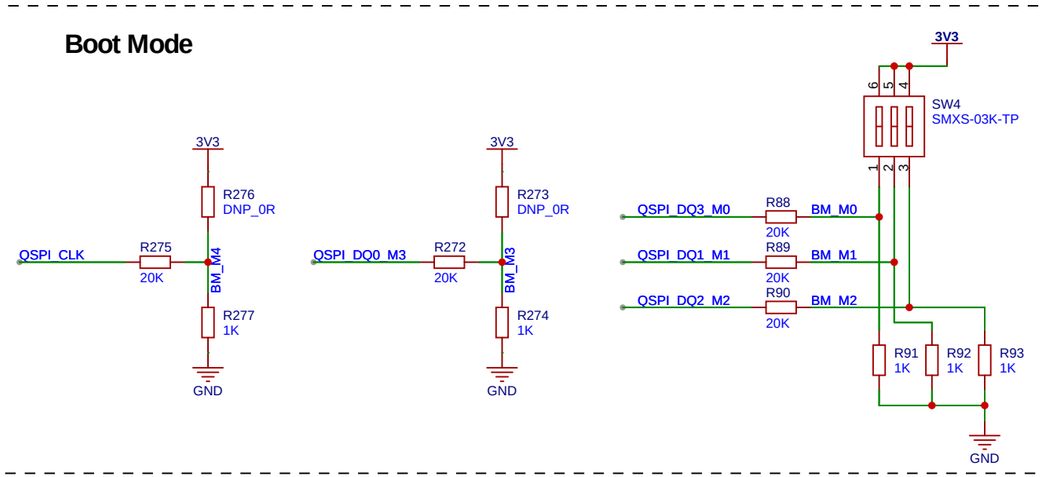
Power on reset



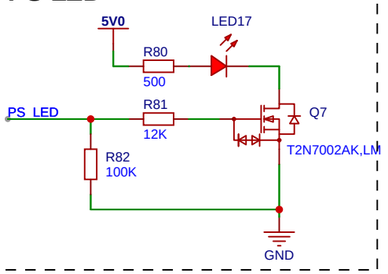
Reset



Boot Mode



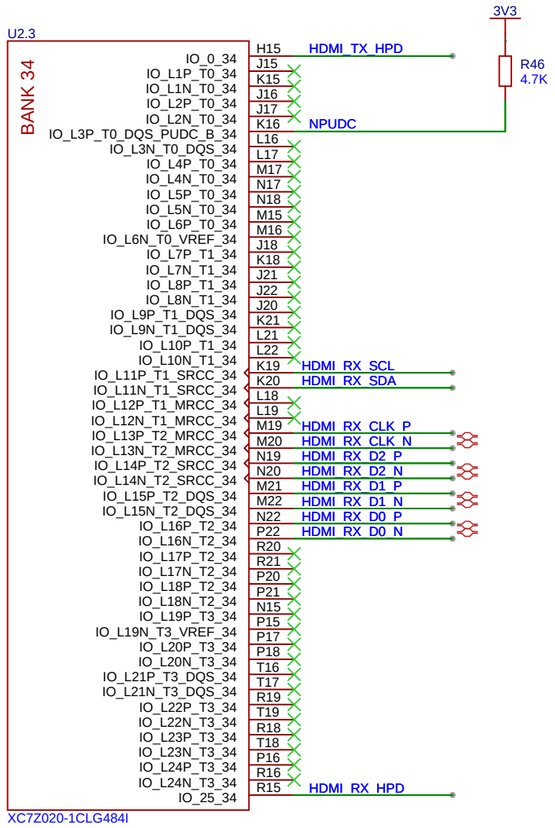
PS LED

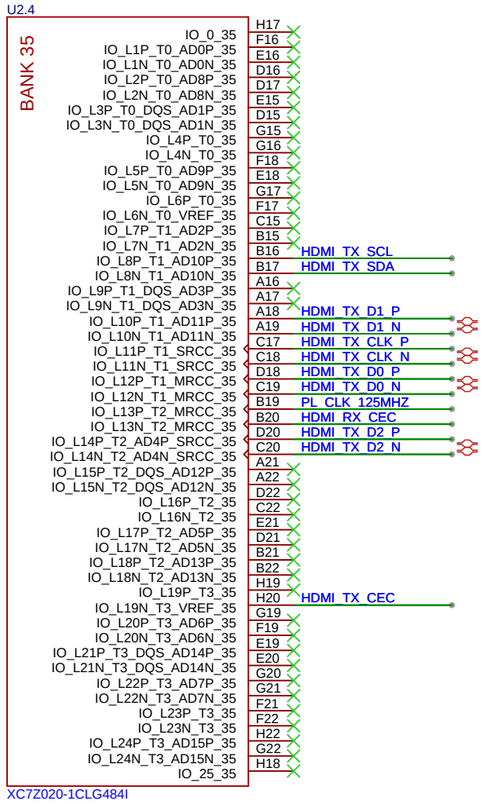


Schematic	schematic1	Update Date	2024-12-01
		Create Date	2024-11-09
Page	Processor	Part Number	JLCPCB-002
Drawn	EasyEDA	FPGA Dev Board - XILINX XC7Z020-1CLG484I v0.07	
Reviewed	EasyEDA		
		VER	SIZE	PAGE 9 OF 13
EasyEDA		V0.1	A4	EasyEDA.com

Banks 34,35 - HDMI

...



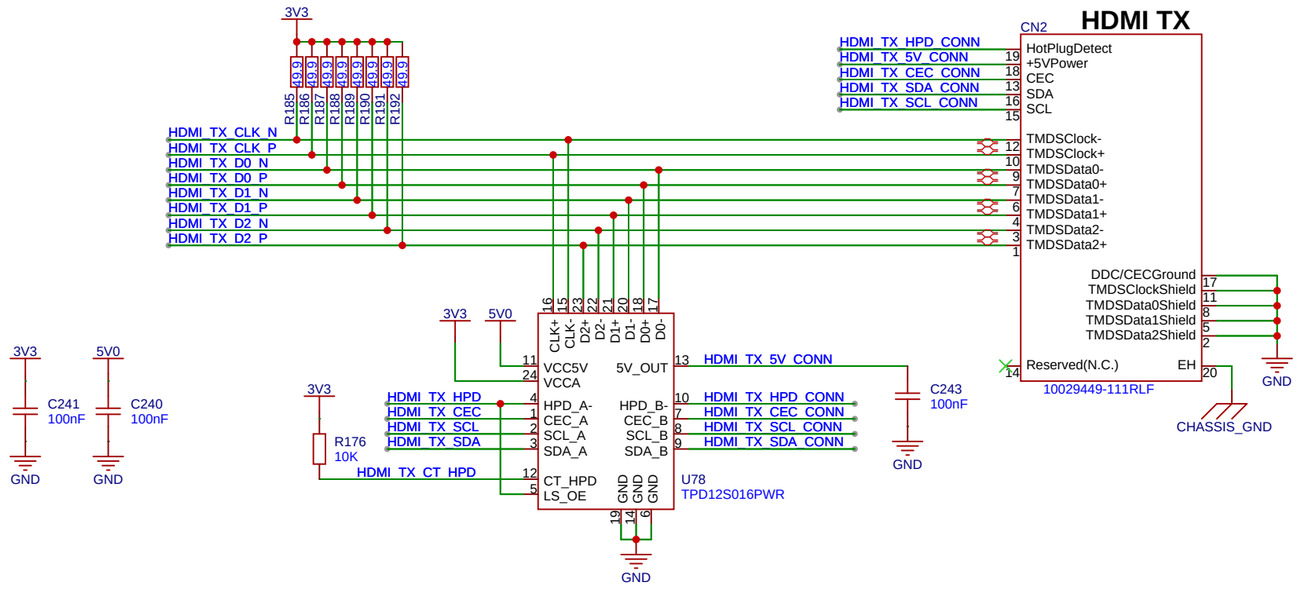


Schematic	schematic1	Update Date	2024-12-12
		Create Date	2024-11-09
Page	Banks 34,35 - HDMI, Expansion	Part Number	JLCPCB-002
Drawn	EasyEDA	FPGA Dev Board - XILINX XC7Z020-1CLG484I v0.07	
Reviewed	EasyEDA		
		VER	SIZE	PAGE 10 OF 13
EasyEDA		V0.1	A4	EasyEDA.com

HDMI

...

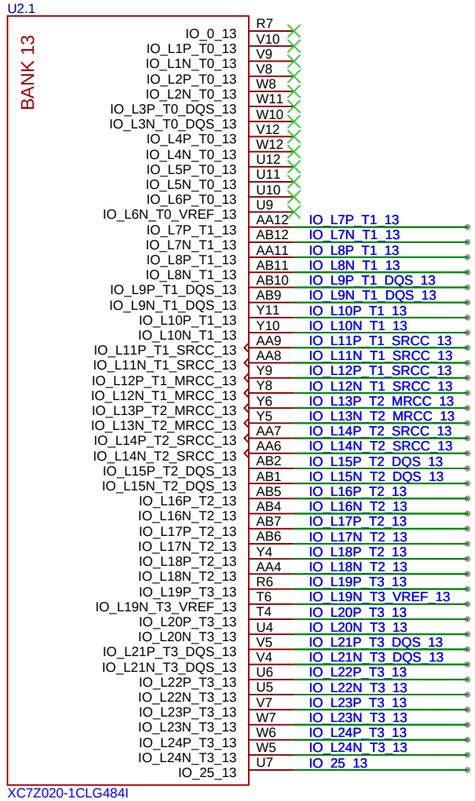
Fly-by routing

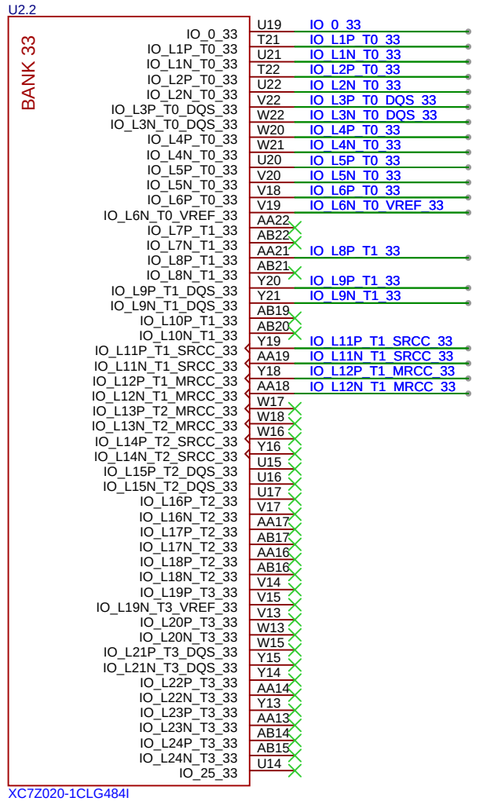


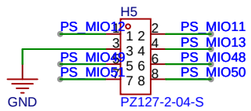
Schematic	schematic1	Update Date	2024-11-09
		Create Date	2024-11-09
Page	HDMI	Part Number	JLCPCB-002
Drawn	EasyEDA	FPGA Dev Board - XILINX XC7Z020-1CLG484I v0.07	
Reviewed	EasyEDA		
		VER / SIZE / PAGE 11 OF 13	
EasyEDA		V0.1 / A4	EasyEDA.com

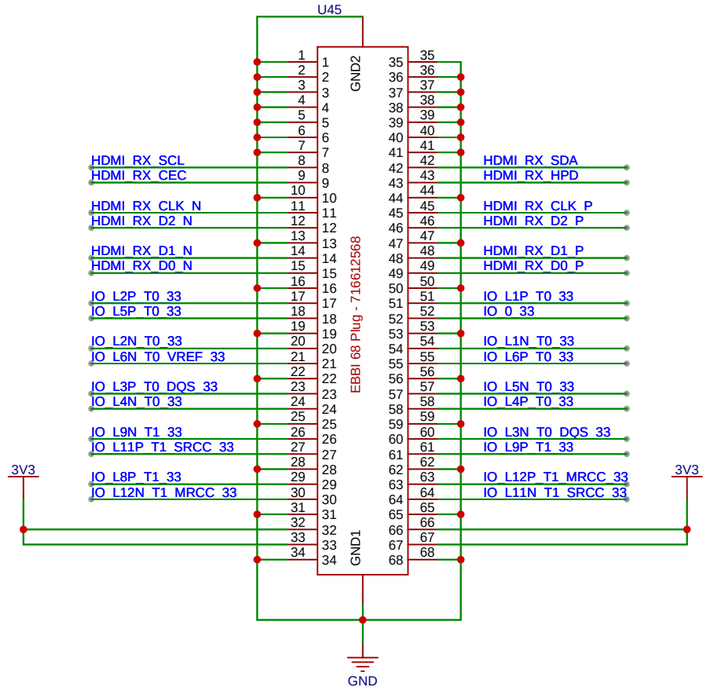
Expansion Ports

...

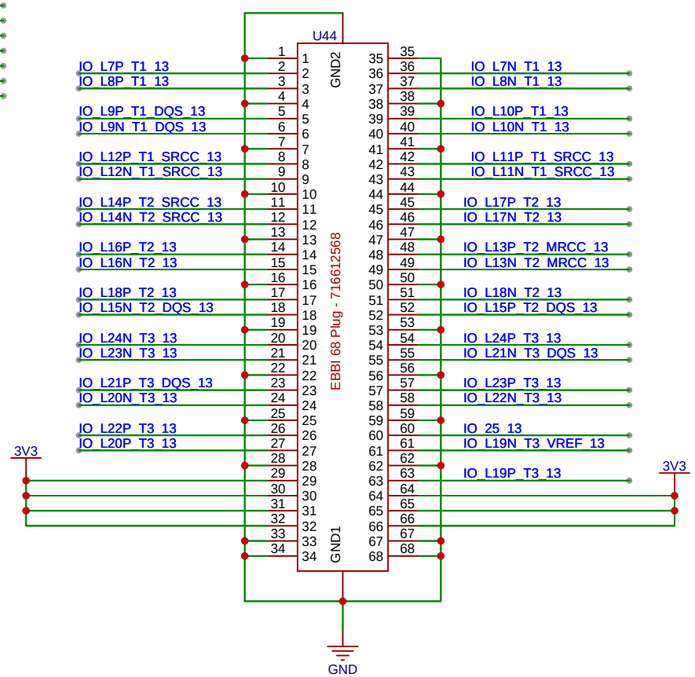








BAY > 36,2,37,3, ...



Schematic	schematic1	Update Date	2024-11-09
		Create Date	2024-11-09
Page	Banks 13,33 - Expansion	Part Number	JLCPCB-002
Drawn	EasyEDA	FPGA Dev Board - XILINX XC7Z020-1CLG484I v0.07	
Reviewed	EasyEDA		
		VER / SIZE / PAGE 12 OF 13	
EasyEDA	V0.1 / A4	EasyEDA.com	

SD Card Reader

Placeholder...

To do:

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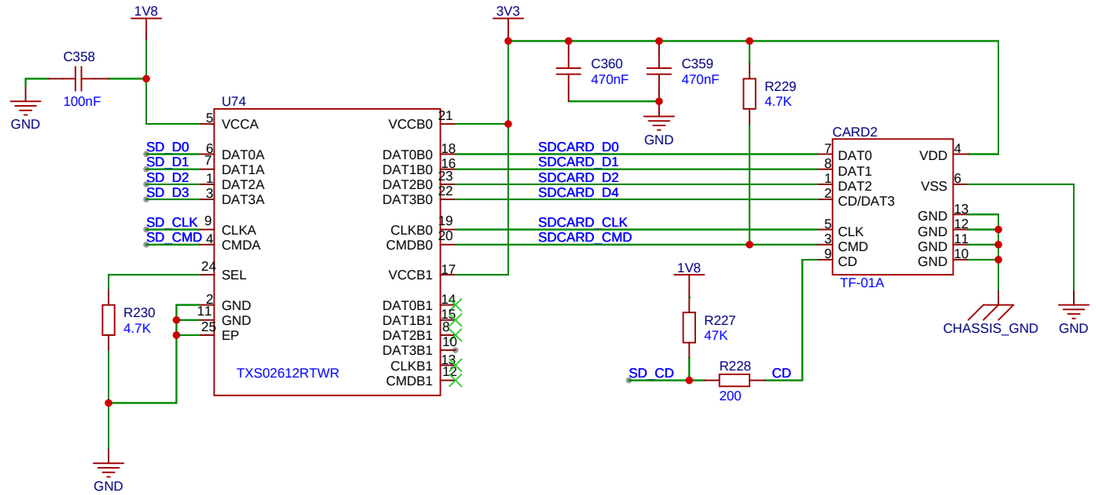

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		Create Date	2024-11-09
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