

TO DO

- To do:
- Pin1 markings on headers
 - 10pF instead of 47/27pF on crystal circuits, along with 150 instead of 1.5k
 - Cutable connections or 0 ohm resistors for questionable tracks
 - Rename both GAL's OEBs from generic to specific and verify throughout
 - Triple-check decode ranges and enables
 - Verify no components without LCSC equiv. part #
 - Print to scale, test fit (especially TFT LCD & ZIFs)
 - Review all status LEDs to confirm they are on good pins for showing status
 - Verify fill on all layers & rebuild
 - External transceivers and/or clock distribution ICs needed? (really long traces)

System Block Diagram

Conventions (e.g., naming)

- Signals for secondary (audio-visual co-processor) MCU prefaced with "AV_"
- Tracks more likely needing bodging on bottom layer
- Horizontal tracks - Top, InnerLower
- Vertical tracks - InnerUpper

Memory Map, Native Decode

W65C265SX8 Memory Map				
Start	End	Size	Chip Select	Description
(C0)	(FF)	4 MB	CS7B	USER MEMORY (FOR EXPANSION)
(40)	(BF)	8 MB	CS6B	USER MEMORY (FOR EXPANSION)
(00)	(3F)	4 MB	CS5B	MEMORY <i>See Note 2</i>
(00)E000 (00)8000	(00)FFFF (00)DEFF	8192 B 24320 B	CS4B	ROM MEMORY (<i>Note 1</i>) ROM MEMORY (<i>Note 1</i>)
(00)0200	(00)7FFF	32256	CS3B	Cache Memory <i>See Note 3</i>
(00)FF00 (00)E000 (00)DF80 (00)DF70 (00)DF50 (00)DF40 (00)DF20 (00)DF00 (00)0000	(00)FFFF (00)FEFF (00)DFBF (00)DF7F (00)DF6F (00)DF4F (00)DF27 (00)DF07 (00)01FF	256 B 7936 B 64 B 16 B 32 B 16 B 8 B 8 B 512 B	CS2B	On Chip Interrupt Vectors On-Chip ROM On-Chip RAM On-Chip Comm. Registers On-Chip Timer Registers On-Chip Control Registers On-Chip IO Registers On-Chip IO Registers On-Chip RAM
(00)DFC0	0xDFFF	64 B		External Chip Select 1 (P71)
(00)DF00	0xDF1F	32 B		External Chip Select 0 (P70) <i>See Note 4</i>

Note 1 - When on-chip 8K bytes of ROM are enabled:
a.) Addresses (00)E000-FFFF will not appear in CS4B chip select decode.
b.) On Chip addresses (00)DF00-DFFF never appear in CS4B or CS5B chip select decode.

Note 2 - When on-chip ROM, CS3B and/or CS4B are enabled:
a.) CS5B decode is reduced by the addresses used by same.
b.) CS0B and CS1B address space never appears in CS2B, CS4B or CS5B decoded space.

Note 3 - When SSCR2 is "0" (internal RAM), then CS3B is active for addresses (00)0200-7FFF. When SSCR2 is "1" (external RAM), then CS3B is active for addresses (00)0000-7FFF.

Note 4 - CS0B is inactive when 00DF00-00DF07 are used for internal I/O register select (BCR0-0). When (BCR0-1) external memory bus is enabled CS0B is active for addresses 00DF00-00DF1F.

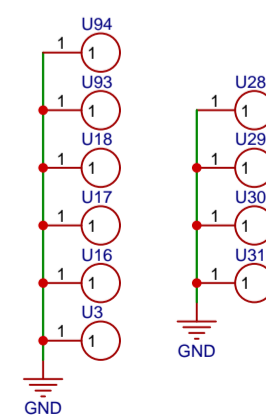
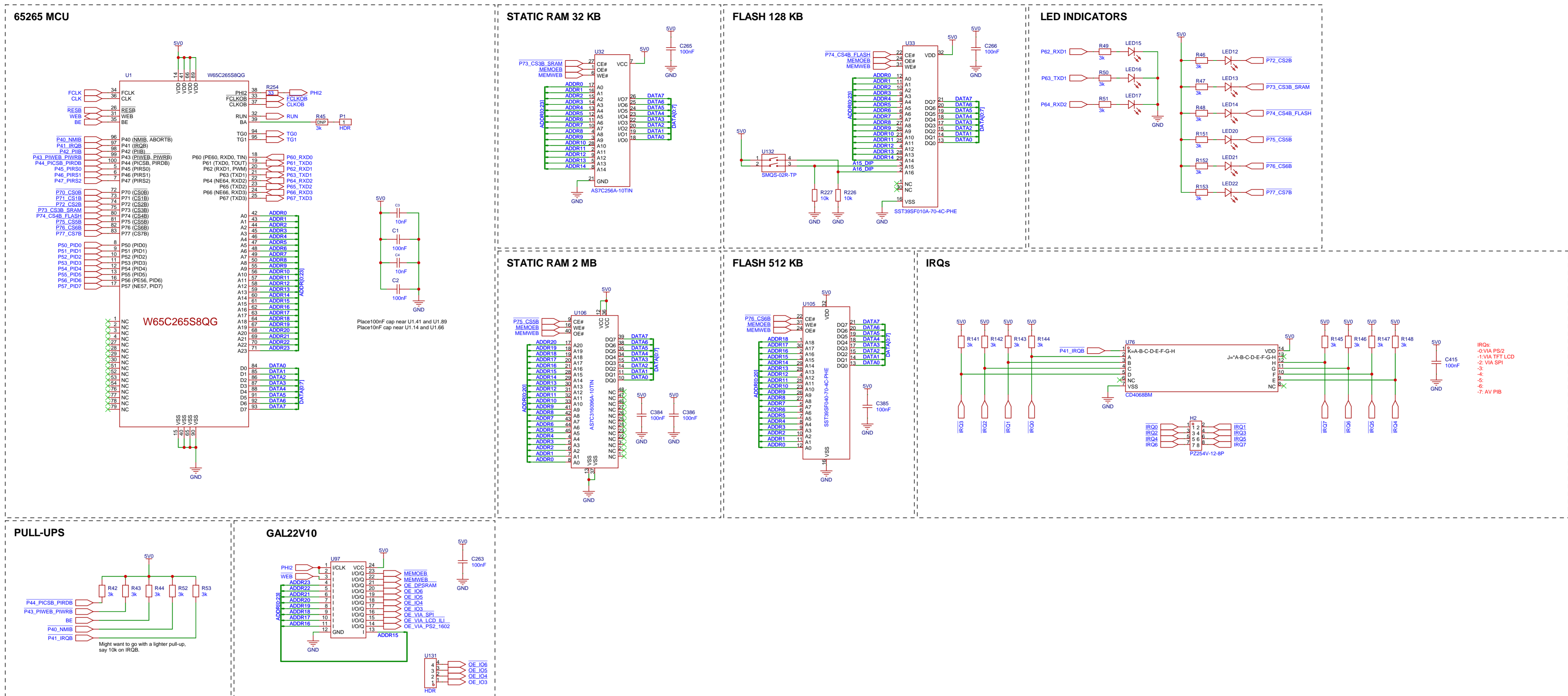
Extended Decode (GAL)


C0:0000 to FF:FFFF CS7B
1100:000000000000000000000000 to 1111:111111111111111111111111 (range: top two bits are 11)
1100: VIA0 C0:xxxx C0:0000 to C0:000F
1101: VIA1 D0:xxxx D0:0000 to D0:000F
1110: VIA2 E0:xxxx E0:0000 to E0:000F
1111: VIA3 F0:xxxx F0:0000 to F0:000F

**re-map I/O by bringing in additional address lines see Overview page for details

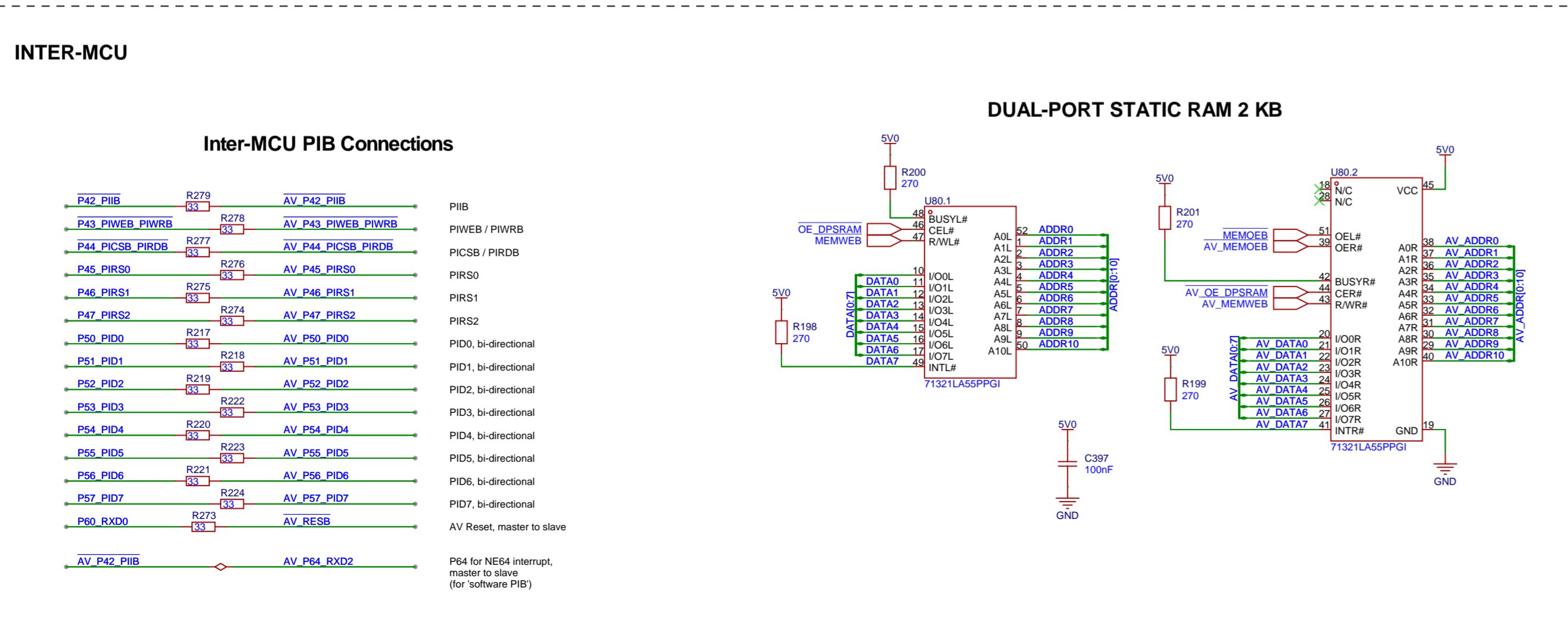
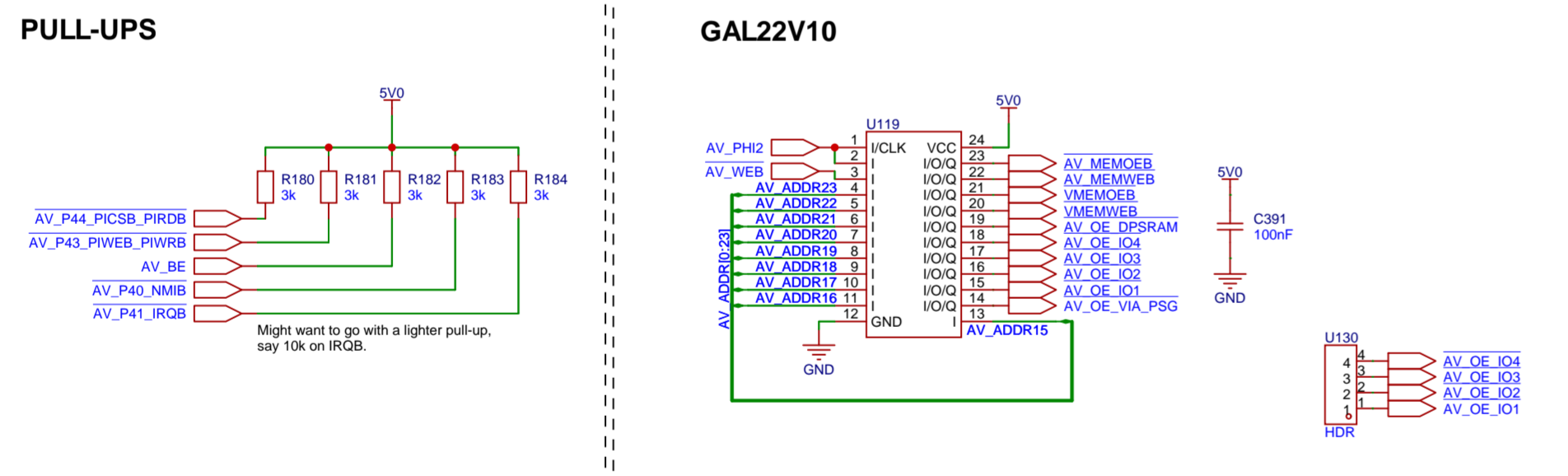
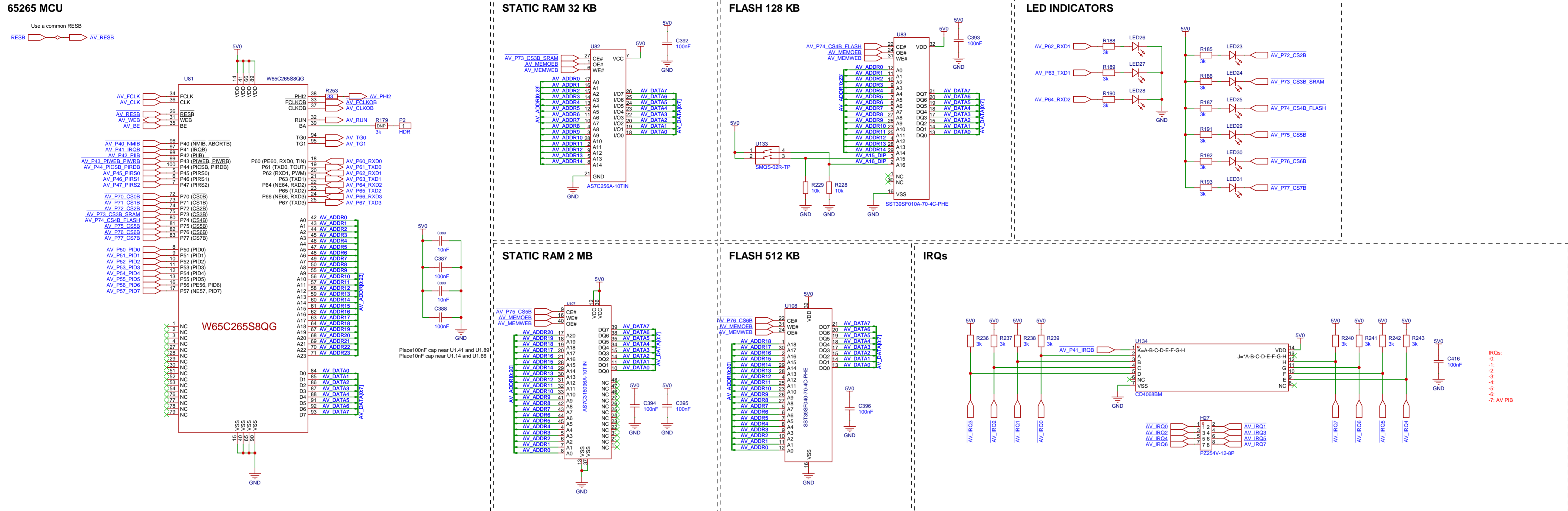
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Board	Board1			Update at	2026-01-08
Drawn	W65C265S v0.12			Page	Overview
Reviewed					
		Version	Size	Page 1 Total 12	
EasyEDA		V1.0	A4	EasyEDA.com	


MCU (Primary)



Schematic	Schematic1			Create at	2026-01-04
Board	Board1			Update at	2026-01-09
Drawn	W65C265S v0.12			Page	MCU Primary
Reviewed					
		Version	Size	Page 2 Total 12	
 EasyEDA		V1.0	A4	EasyEDA.com	

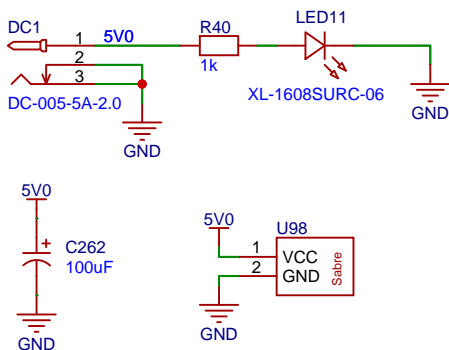
MCU (AV)



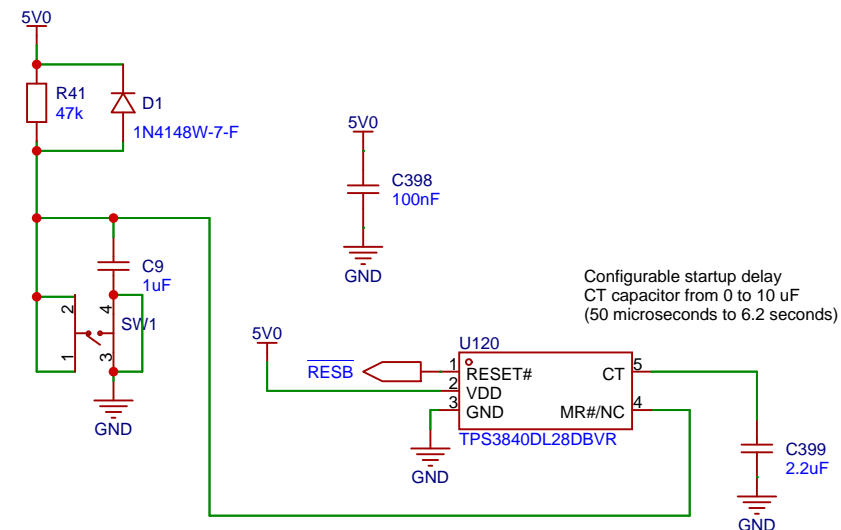
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Board	Board1		Update at	2026-01-12
Drawn	W65C265S v0.12		Page	MCU AV
Reviewed				
	Version	Size	Page 3 Total 12	
 EasyEDA	V1.0	A4	EasyEDA.com	

POWER

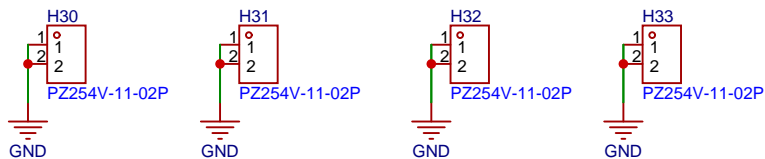
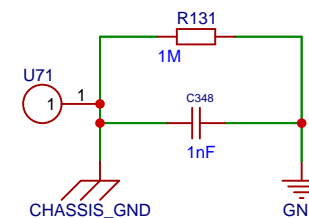
Input



Reset



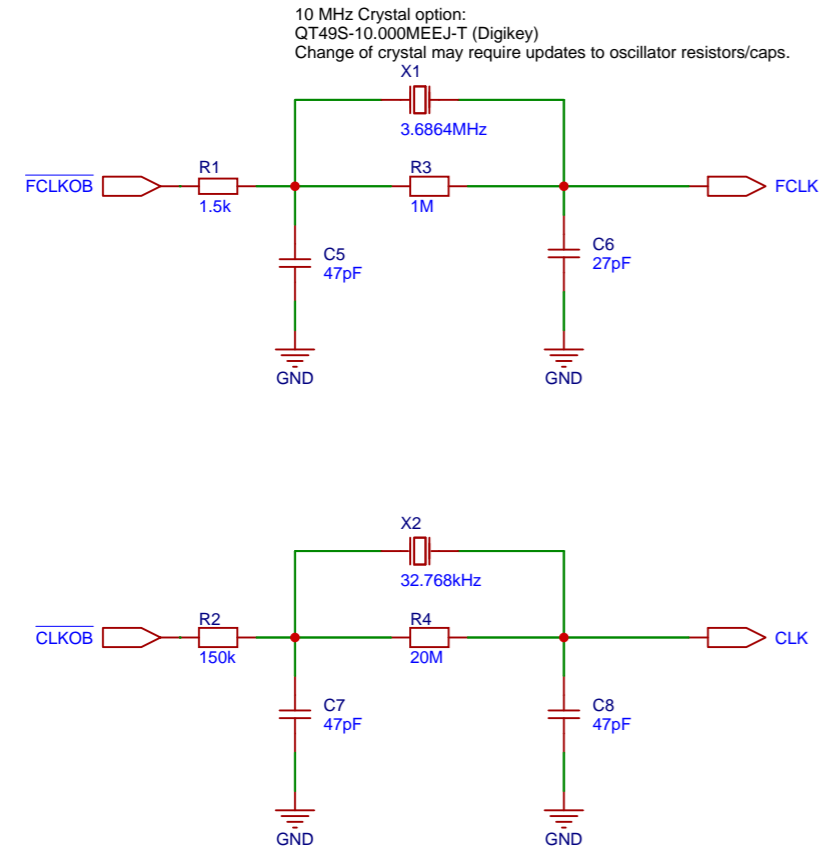
Chassis Ground



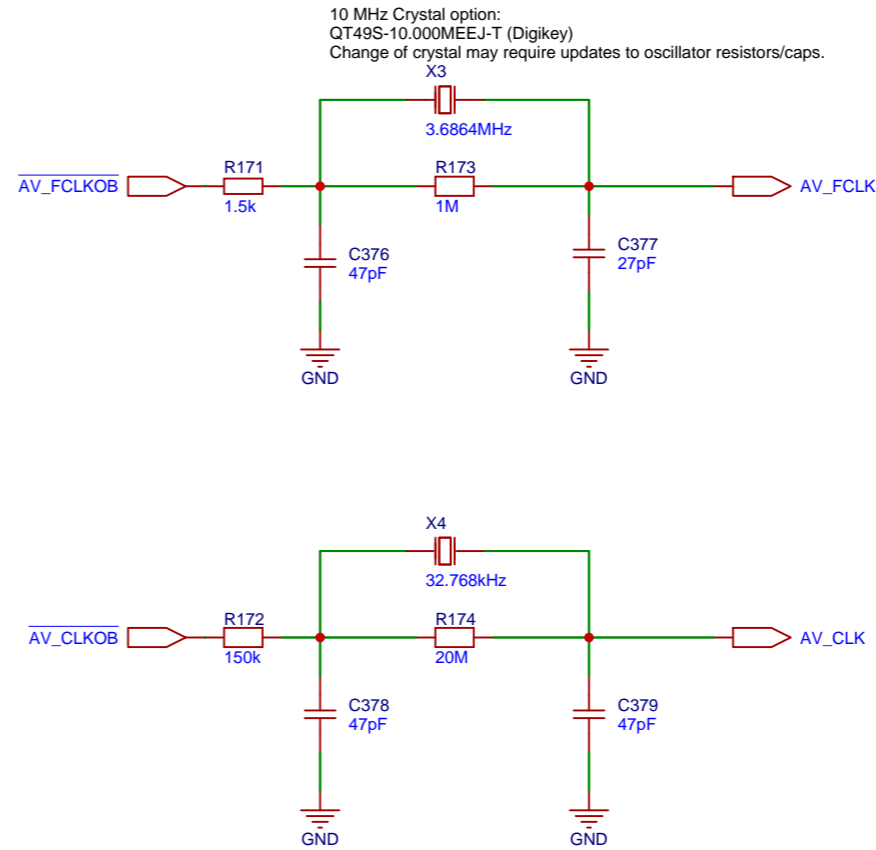
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Board	Board1			Update at	2026-01-06
Drawn		W65C265S v0.12			
Reviewed					
		Version	Size	Page 4 Total 12	
		V1.0	A4	EasyEDA.com	

CLOCKS

PRIMARY



AV



Schematic	Schematic1			Create at	2026-01-05
				Update at	2026-01-04
Board	Board1			Page	Clocks
Drawn		W65C265S v0.12			
Reviewed					
		Version	Size	Page 5 Total 12	
EasyEDA		V1.0	A4	EasyEDA.com	

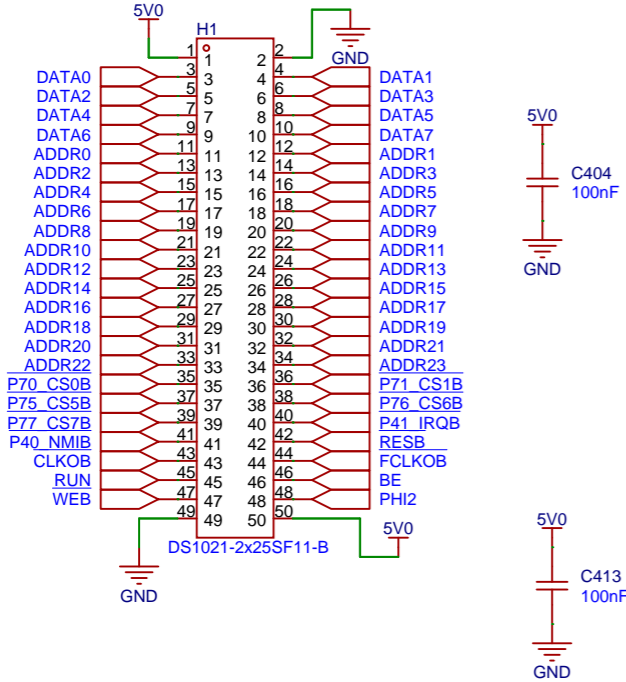
EXPANSION

Used:

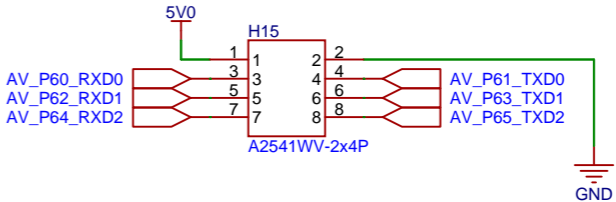
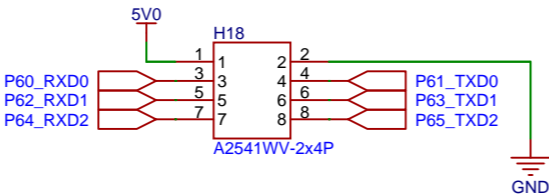
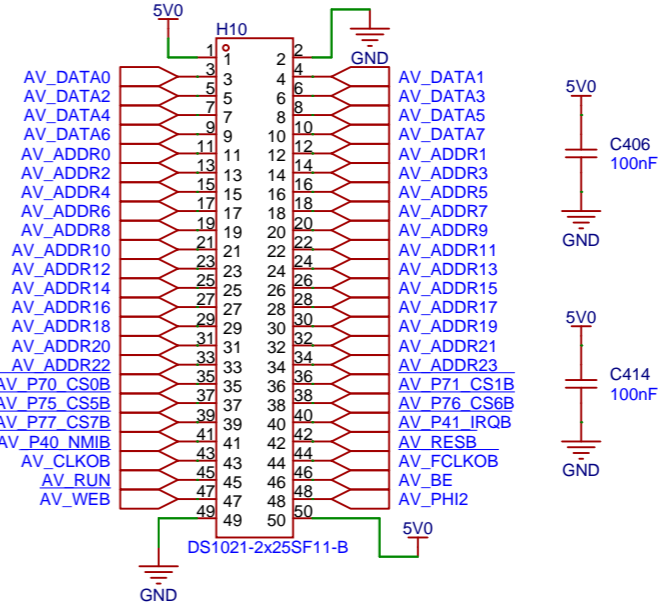
P50:56 - 1602 LCD
P51 - Available

P62 - PS2KBD DATA
P64 - PS2KBD CLK
P66 - RXD3
P67 - TXD3

Primary XBus265

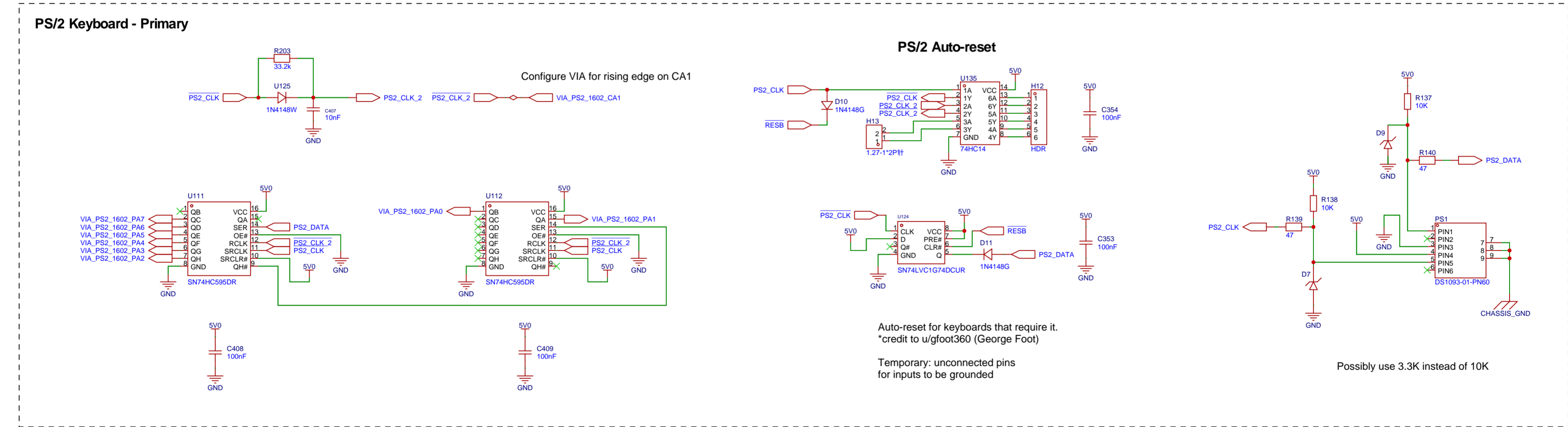
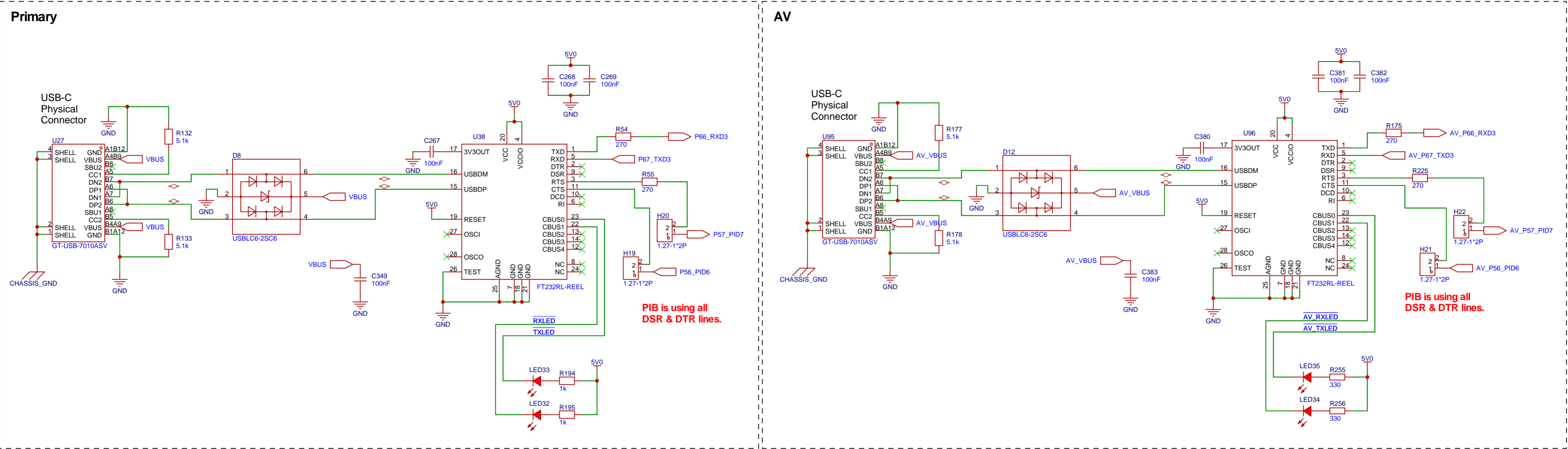


AV XBus265



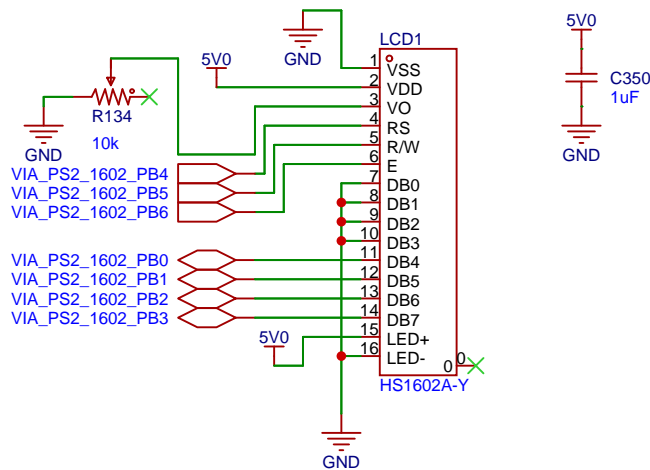
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Board	Board1		Page	Expansion
Drawn		W65C265S v0.12		
Reviewed				
		Version	Size	Page 6 Total 12
EasyEDA		V1.0	A4	EasyEDA.com

USB SERIAL, PS/2 KEYBOARD



Schematic	Schematic1			Create at	2026-01-05
Board	Board1			Update at	2026-01-08
Drawn				Page	Serial & PS2
Reviewed				W65C265S v0.12	
		Version	Size	Page 7 Total 12	
EasyEDA		V1.0	A4	EasyEDA.com	

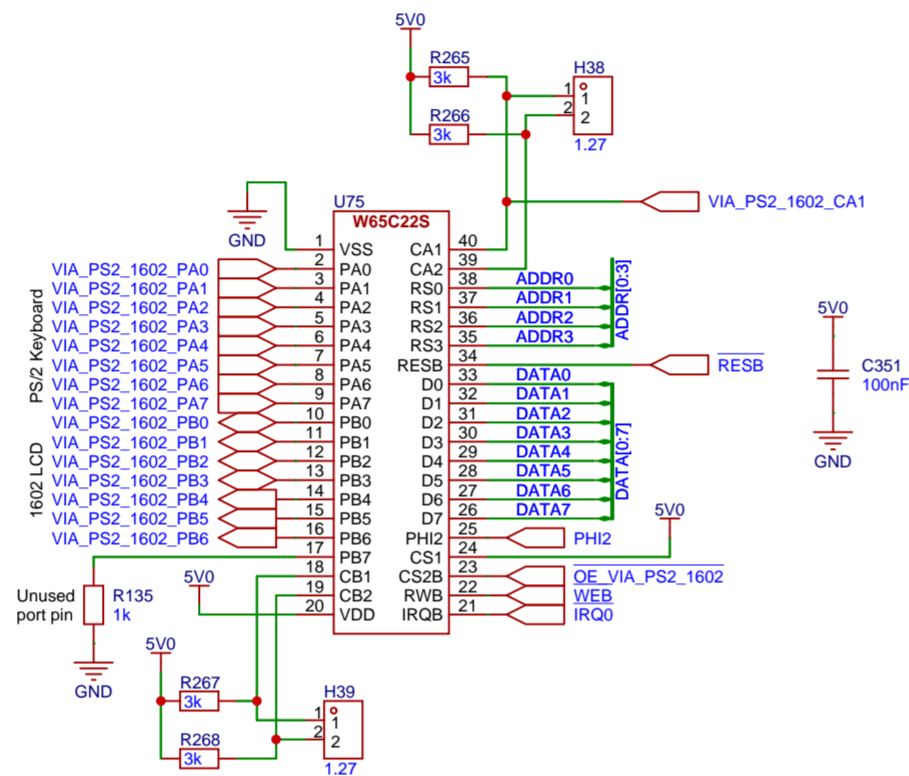
LCD 1602



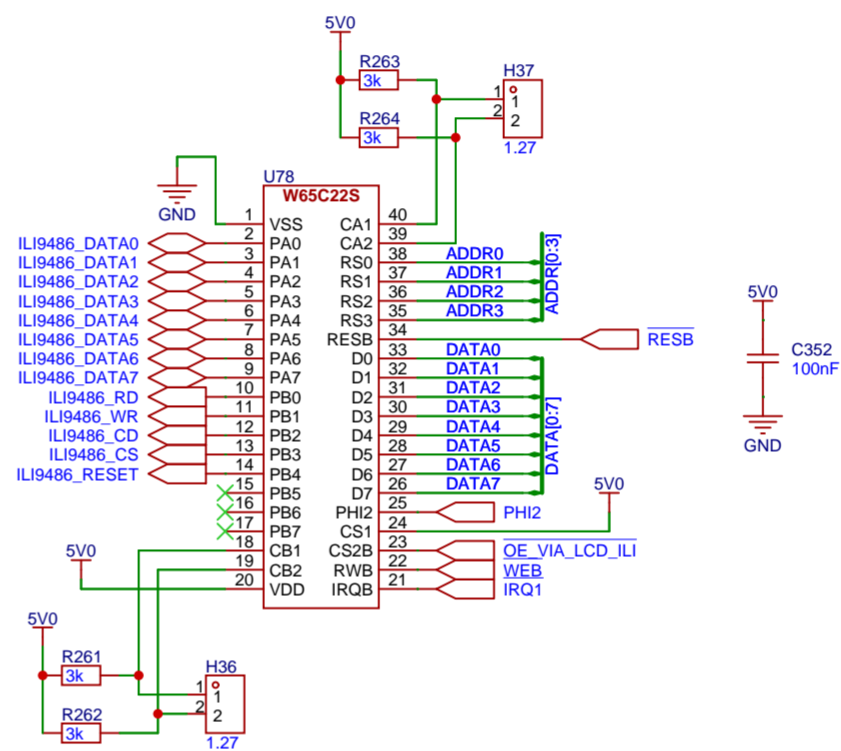
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Board	Board1		Page	LCD_1602
Drawn		W65C265S v0.12		
Reviewed				
		Version	Size	Page 8 Total 12
EasyEDA		V1.0	A4	EasyEDA.com

VIAs

PS/2 Keyboard, 1602 LCD



TFT LCD (ILI)

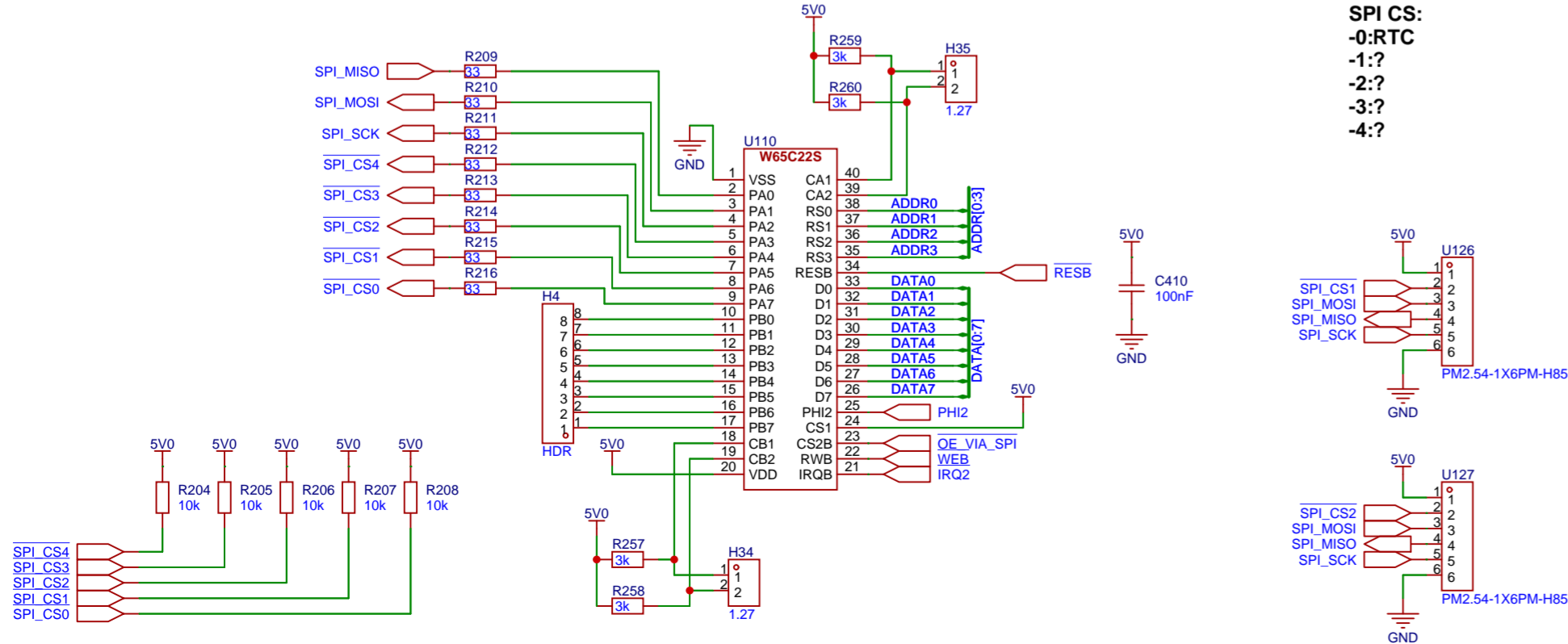


C0:0000 to FF:FFFF CS7B

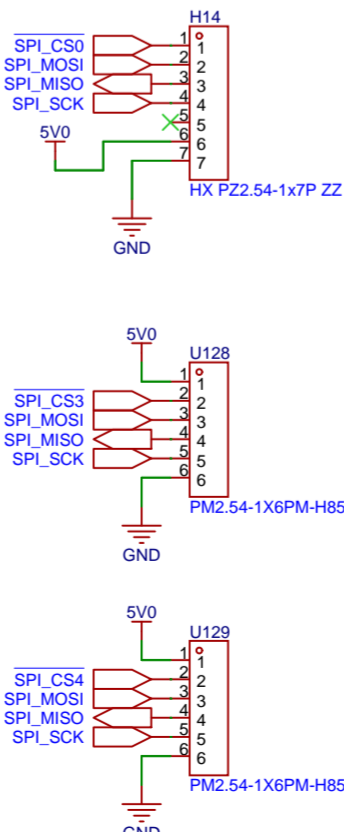
1100:00000000000000000000000000000000 to
1111:1111111111111111111111111111111111
(range: top two bits are 11)

1100: VIA0 C0:xxxx C0:0000 to C0:000F
1101: VIA1 D0:xxxx D0:0000 to D0:000F
1110: VIA2 E0:xxxx E0:0000 to E0:000F
1111: VIA3 F0:xxxx F0:0000 to F0:000F

SPI, Expansion



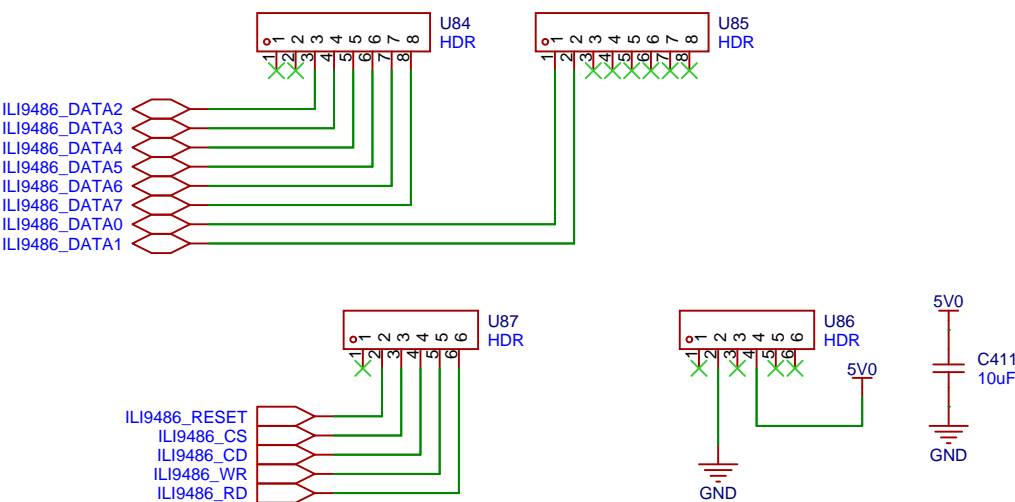
SPI CS:
-0:RTC
-1:?
-2:?
-3:?
-4:?



Schematic	Schematic1		Create at	2026-01-05
Board	Board1		Update at	2026-01-08
Drawn			Page	VIAs
Reviewed			W65C226S v0.12	
		Version	Size	Page 9 Total 12
		V1.0	A4	EasyEDA.com

LCD - ILI

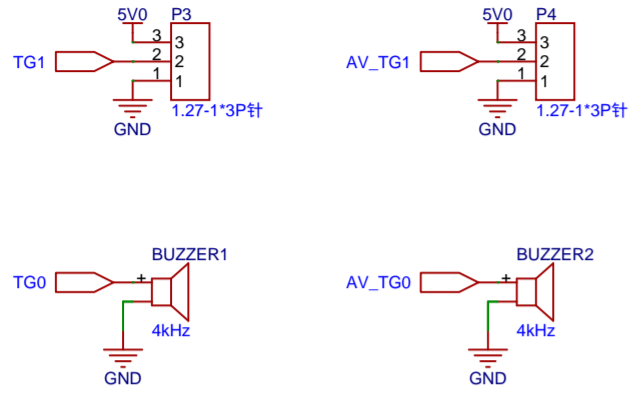
Arduino-style header for DIYables TFT LCD



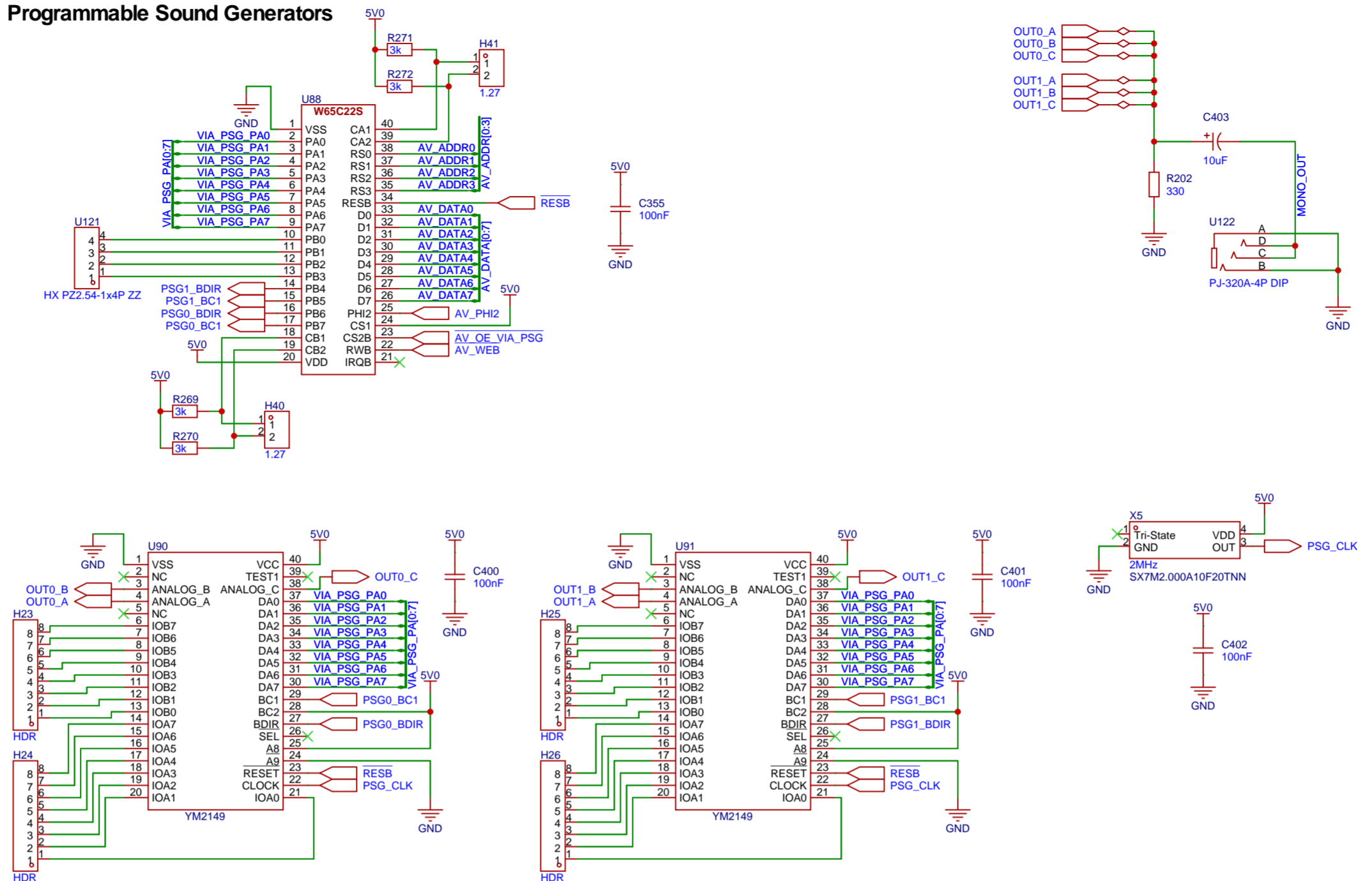
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Board	Board1			Page	LCD_ILI
Drawn		W65C265S v0.12			
Reviewed					
		Version	Size	Page 10 Total 12	
		V1.0	A4	EasyEDA.com	


Sound

Tone Generators



Programmable Sound Generators



Schematic	Schematic1				Create at	2026-01-05
					Update at	2026-01-08
Board	Board1				Page	Sound
Drawn		W65C265S v0.12				
Reviewed						
		Version	Size	Page 11 Total 12		
		V1.0	A4	EasyEDA.com		

VGA 320x240 x1Byte

RRRRGGGB

VGA Signal 320 x 240 @ 60 Hz

General timing
Screen refresh rate60 Hz
Vertical refresh31.46875 kHz
Pixel freq 12.2875 MHz

Horizontal timing (line)
Polarity of horizontal sync pulse is negative.
Scanline pairPulseTime [µs]
Visible area32012.711
Front porch60.318 320 101000000
Sync pulse481.807 320 101001000
Back porch240.953 376 101111000
Whole line4015.889 400 110010000

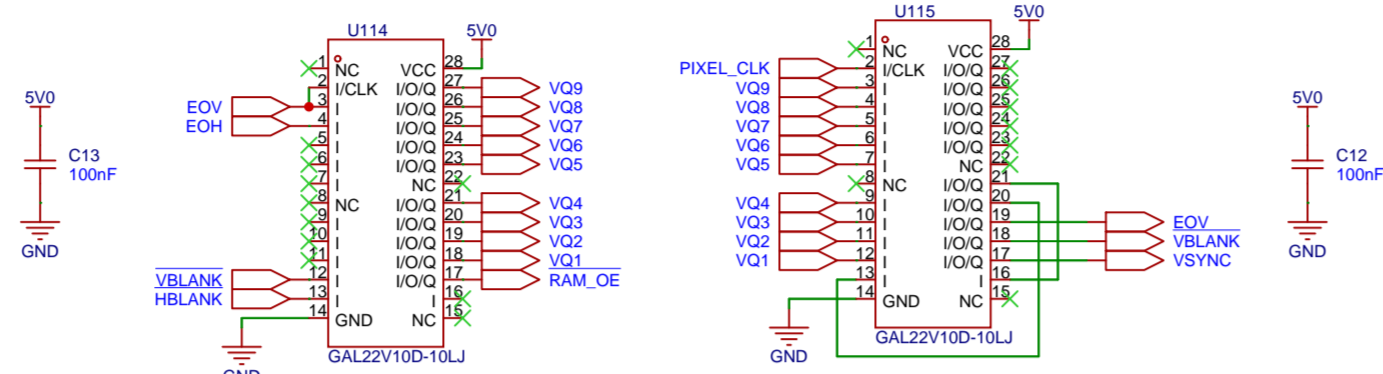
Vertical timing (frame)
Polarity of vertical sync pulse is negative.
Frame pairLinesTime [µs]
Visible area6015.253
Front porch100.318 480 0111100000
Sync pulse20.984 480 011101010
Back porch331.046 492 0111010100
Whole frame2516.883 525 1000001101

320x240 x1Byte
-3bit Red
-3bit Green
-2bit Blue

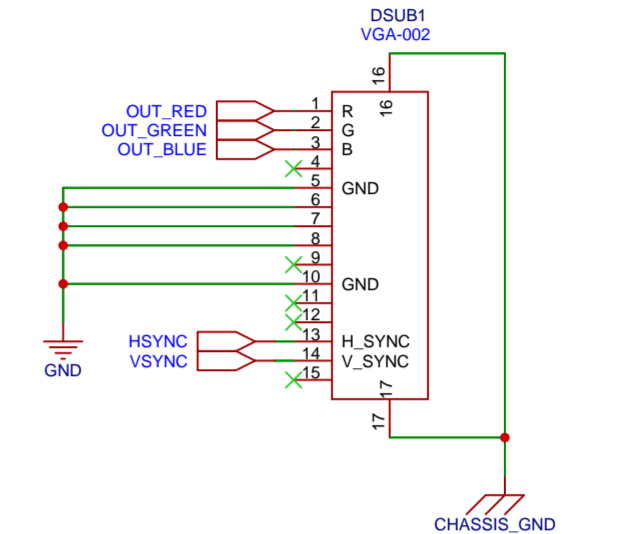
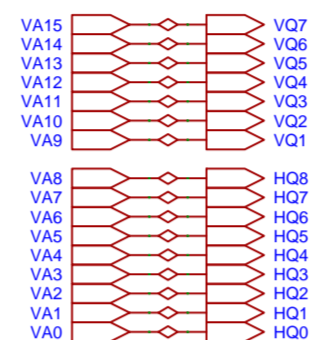
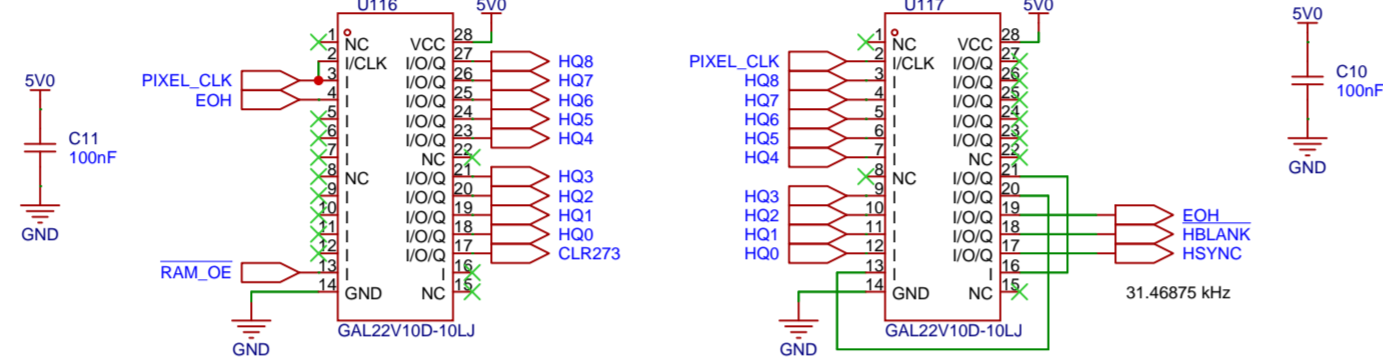
IO2_EN OR'd with MEMR/MEMW to generate VMEMOE and VMEMEWB

CS7B is C0:0000 to FF:FFFF
OE3B is E0:0000 to EF:0000
Video MRB/MWB are EA:0000 to EB:FFFF

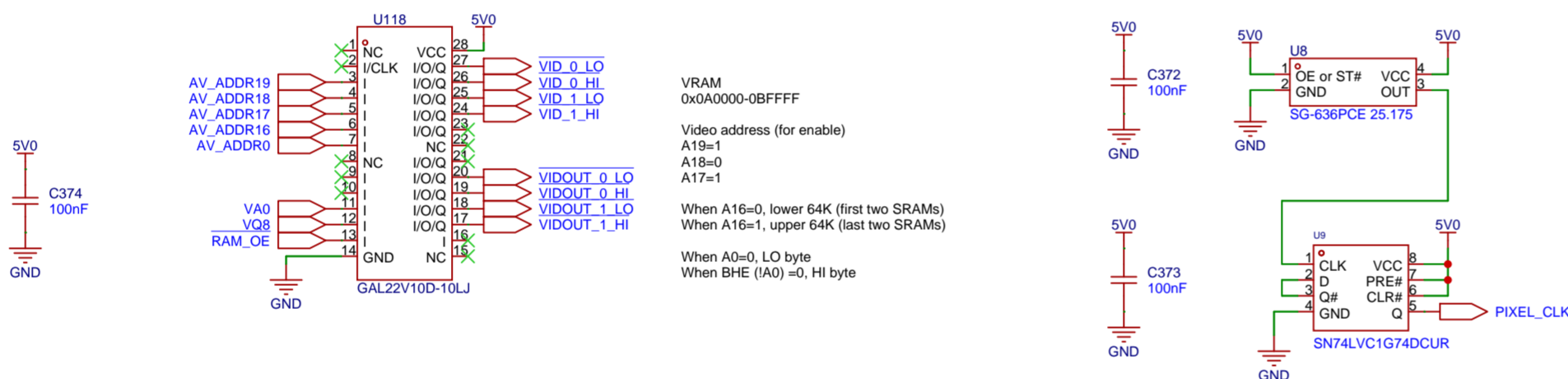
VSYNC



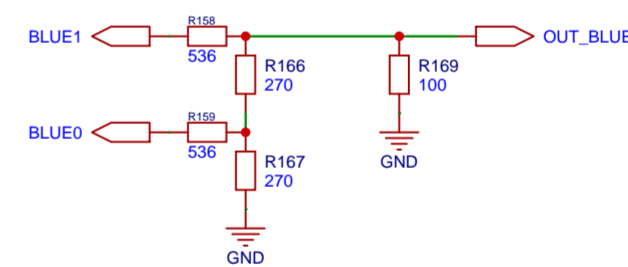
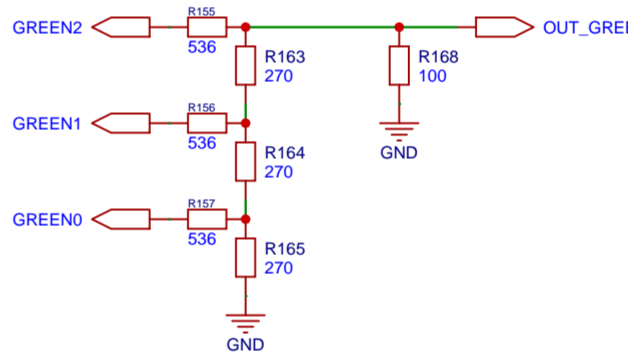
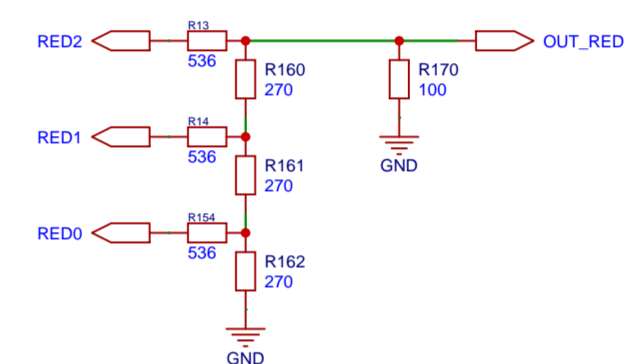
HSYNC



DECODE



To do:
-fill top / bottom layers with GND
- same with inner signal



LOWER 64K (VID_0)

UIPPER 64K (VID_1)

