

## TO DO

- Triple-check decode logic for all ICs
- Pin1 markings on headers
- 10pF instead of 47/27pF on crystal circuits, along with 150 instead of 1.5k
- Cuttable connections or 0 ohm resistors for questionable tracks
- Rename both GAL's OEBs from generic to specific and verify throughout
- Triple-check decode ranges and enables
- Verify no components without LCSC equiv. part #
- Print to scale, test fit (especially TFT LCD & ZIFs)
- Review all status LEDs to confirm they are on good pins for showing status
- Verify fill on all layers & rebuild
- External transceivers and/or clock distribution ICs needed? (really long traces)
- Swap out YM2149 with AY-3-8913?
- Swap out VIAs with PLCC versions?

## System Block Diagram

## Conventions (e.g., naming)

- Signals for secondary (audio-visual co-processor) MCU prefaced with "AV\_"
- Tracks more likely needing bodge on bottom layer
- Horizontal tracks - Top, InnerLower
- Vertical tracks - InnerUpper

## Memory Map, Native Decode

W65C265XB Memory Map				
Start	End	Size	Chip Select	Description
(C0)	(FF)	4 MB	CS7B	USER MEMORY (FOR EXPANSION)
(40)	(BF)	8 MB	CS6B	USER MEMORY (FOR EXPANSION)
(00)	(3F)	4 MB	CS5B	MEMORY See Note 2
(00)E000	(00)FFFF	8192 B	CS4B	ROM MEMORY (Note 1) ROM MEMORY (Note 1)
(00)8000	(00)DEFF	24320 B	CS4B	
(00)0200	(00)7FFF	32256	CS3B	Cache Memory See Note 3
(00)F000	(00)FFFF	256 B	CS2B	On Chip Interrupt Vectors
(00)E000	(00)FEFF	7936 B		On-Chip ROM
(00)DF80	(00)DFBF	64 B		On-Chip RAM
(00)DF70	(00)DF7F	16 B		On-Chip Comm. Registers
(00)DF50	(00)DF6F	32 B		On-Chip Timer Registers
(00)DF40	(00)DF4F	16 B		On-Chip Control Registers
(00)DF20	(00)DF27	8 B		On-Chip IO Registers
(00)DF00	(00)DF07	8 B		On-Chip IO Registers
(00)0000	(00)01FF	512 B		On-Chip RAM
(00)DFO0	0xDFFF	64 B	CS1B	External Chip Select 1 (P71)
(00)DF00	0xDF1F	32 B	CS0B	External Chip Select 0 (P70) See Note 4

## Extended Decode (GAL)



Note 1 - When on-chip 8K bytes of ROM are enabled:  
a.) Addresses (00)E000-FFFF will not appear in CS4B chip select decode.  
b.) On Chip addresses (00)DFO0-DFFF never appear in CS4B or CS5B chip select decode.

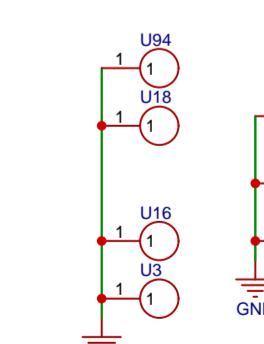
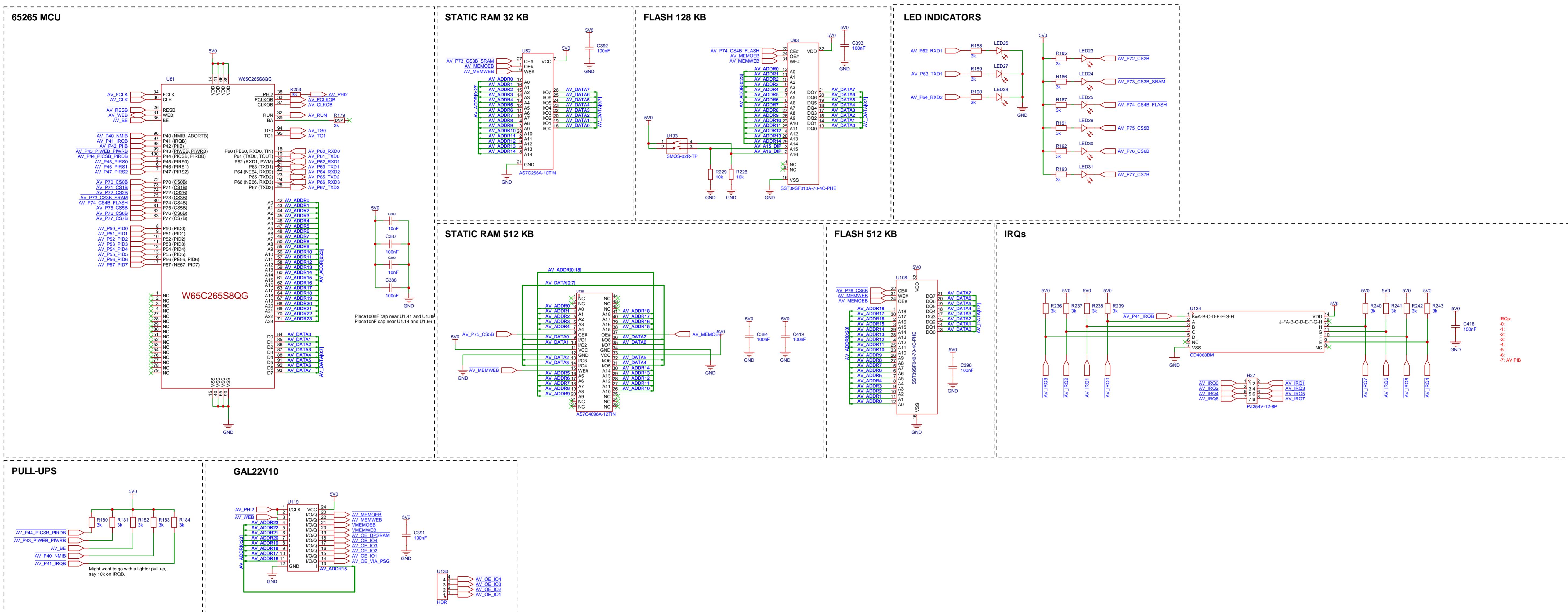
Note 2 - When on-chip ROM, CS3B and/or CS4B are enabled:  
a.) CS5B decode is reduced by the addresses used by same.  
b.) CS5B and CS1B address space never appears in CS2B, CS4B or CS5B decoded space.

Note 3 - When SSZR2 is "0" (internal RAM), then CS3B is active for addresses (00)0200-7FFF. When SSZR2 is "1" (external RAM), then CS3B is active for addresses (00)0000-7FFF.

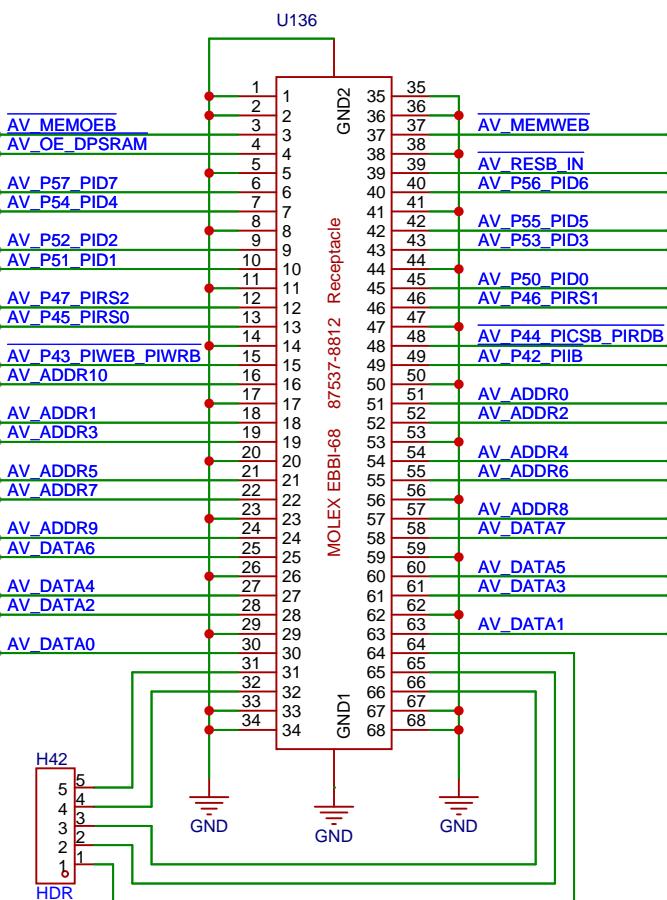
Note 4 - CS0B is inactive when 00DF00-00DF07 are used for internal IO register select (BCR0=0). When (BCR0=1) external memory bus is enabled CS0B is active for addresses 00DF00-00DF1F.

Schematic	Schematic1		Create at	2026-01-24
Board	Board1		Update at	2026-01-24
Drawn	Reviewed	Page	Overview	
			W65C265S AV v0.12	
			Version	Size
			V1.0	A4
			EasyEDA.com	

# MCU (AV)

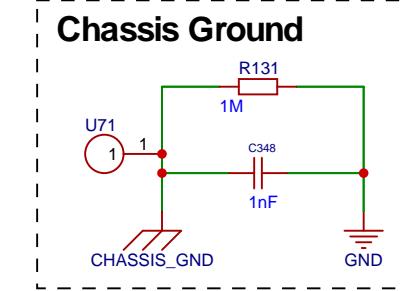
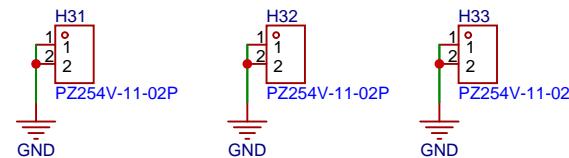
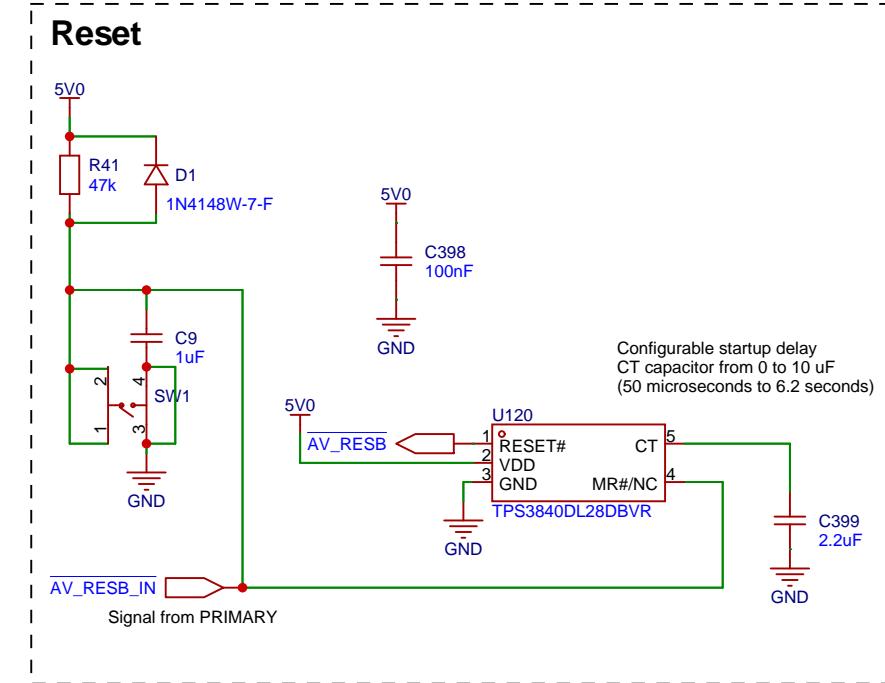
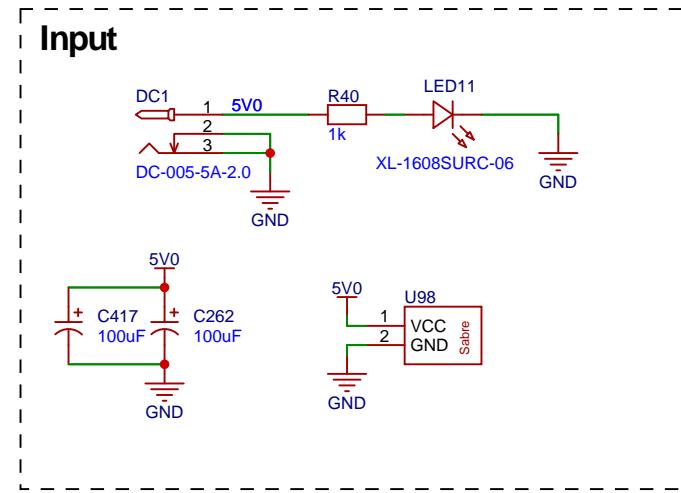


Schematic	Schematic1		Create at	2026-01-24
			Update at	2026-01-24
Board	Board1		Page	MCU AV
Drawn				
Reviewed			W65C265S AV v0.12	
			Version Size Page 2 Total 9	
 EasyEDA		V1.0	A4	EasyEDA.com



Schematic	Schematic1		Create at	2026-01-24
Board	Board1		Update at	2026-01-24
Drawn			Page	Interconnect
Reviewed				
	Version	Size	Page 3 Total 9	
		V1.0	A4	EasyEDA.com

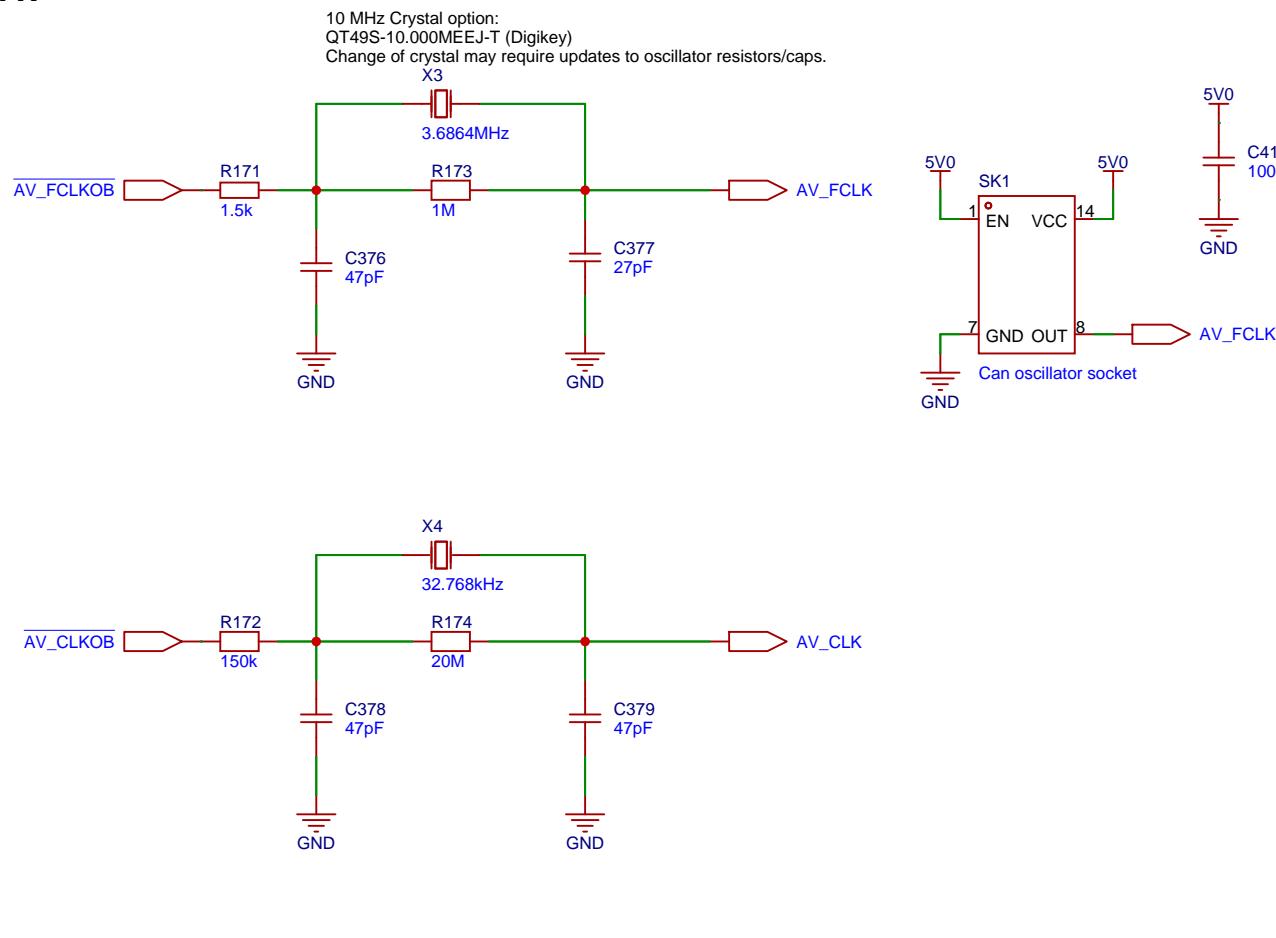
# POWER



Schematic	Schematic1			Create at	2026-01-24
Board	Board1			Update at	2026-01-24
Drawn				Page	Power
Reviewed					
	Version	Size	Page 4 Total 9		
<b>EasyEDA</b>		V1.0	A4	EasyEDA.com	

# CLOCKS

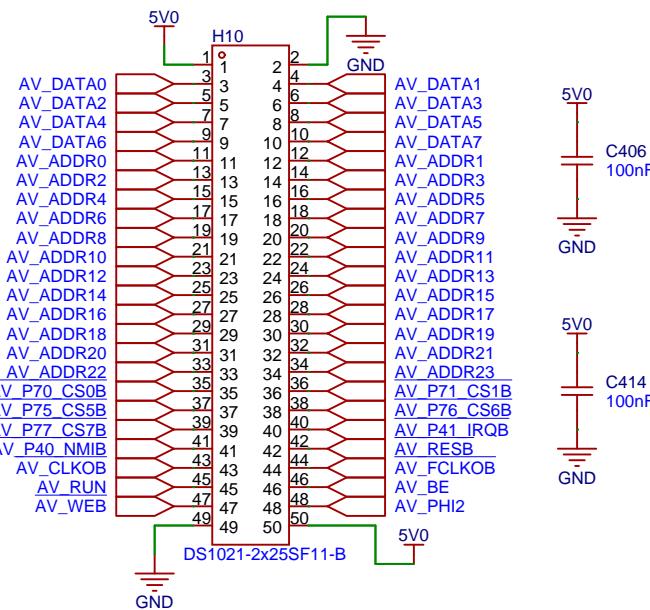
**AV**



Schematic	Schematic1			Create at	2026-01-24
Board	Board1			Update at	2026-01-24
Drawn				Page	Clocks
Reviewed				W65C265S AV v0.12	
	Version	Size	Page 5 Total 9		
		V1.0	A4	EasyEDA.com	

# EXPANSION

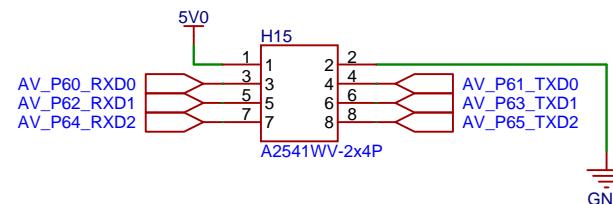
## AV XBus265



Used:

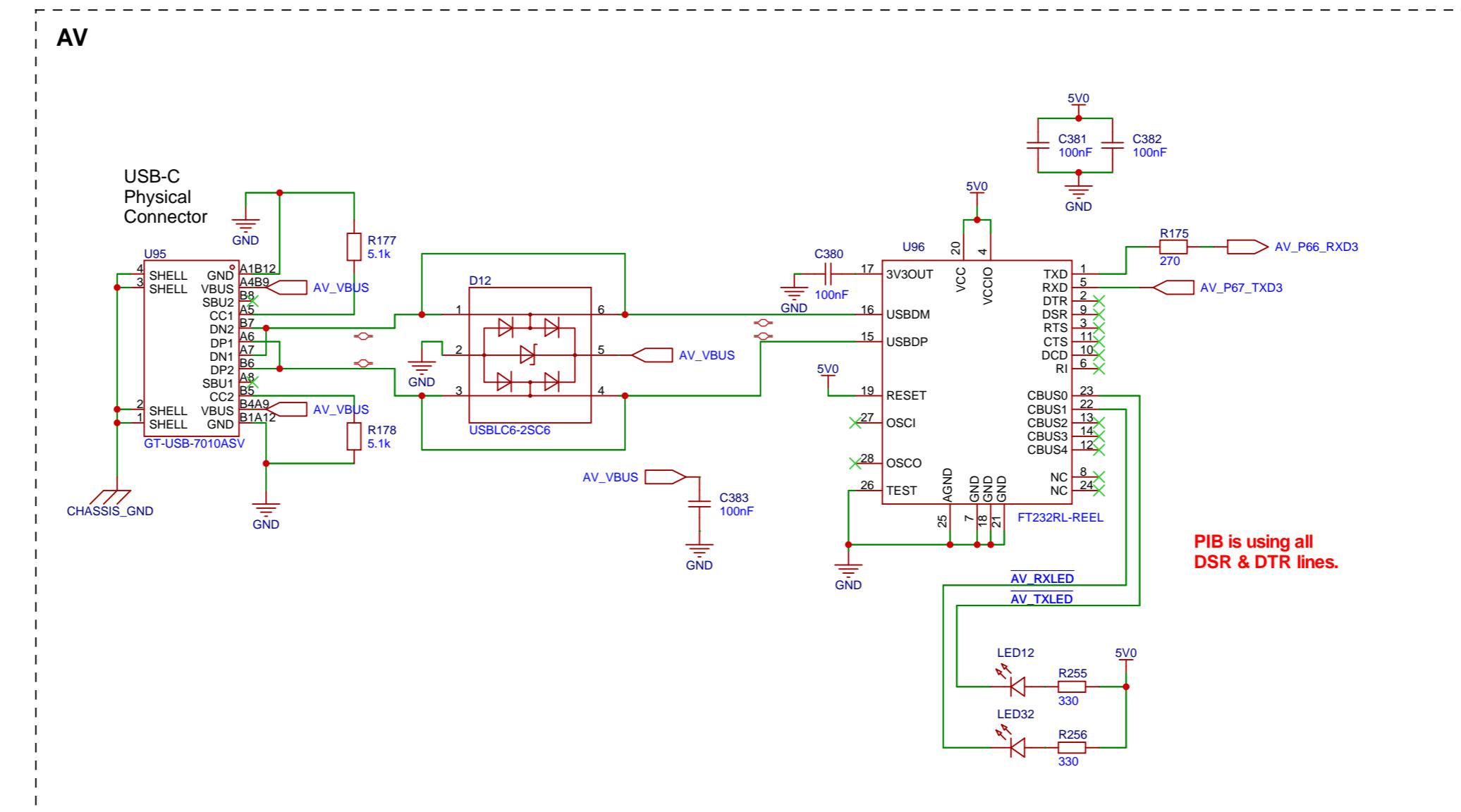
P50:56 - 1602 LCD  
P51 - Available

P62 - PS2KBD DATA  
P64 - PS2KBD CLK  
P66 - RXD3  
P67 - TXD3



Schematic	Schematic1			Create at	2026-01-24
Board	Board1			Update at	2026-01-24
Drawn				Page	Expansion
Reviewed				W65C265S AV v0.12	
	Version	Size	Page 6 Total 9		
 EasyEDA		V1.0	A4	EasyEDA.com	

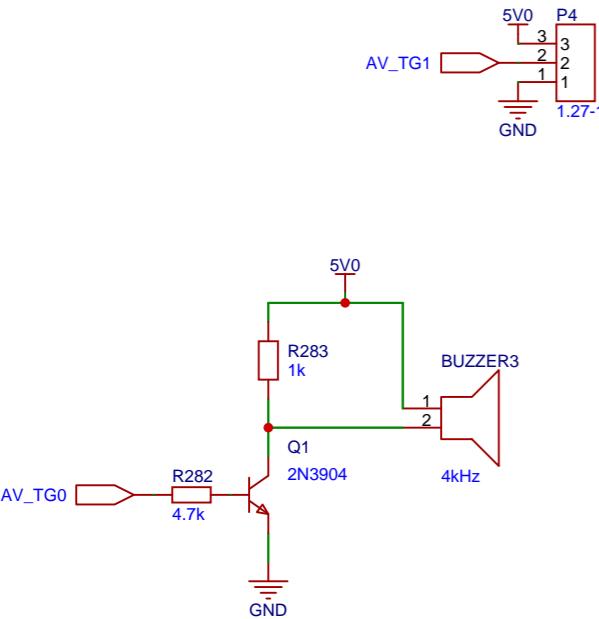
# USB SERIAL, PS/2 KEYBOARD



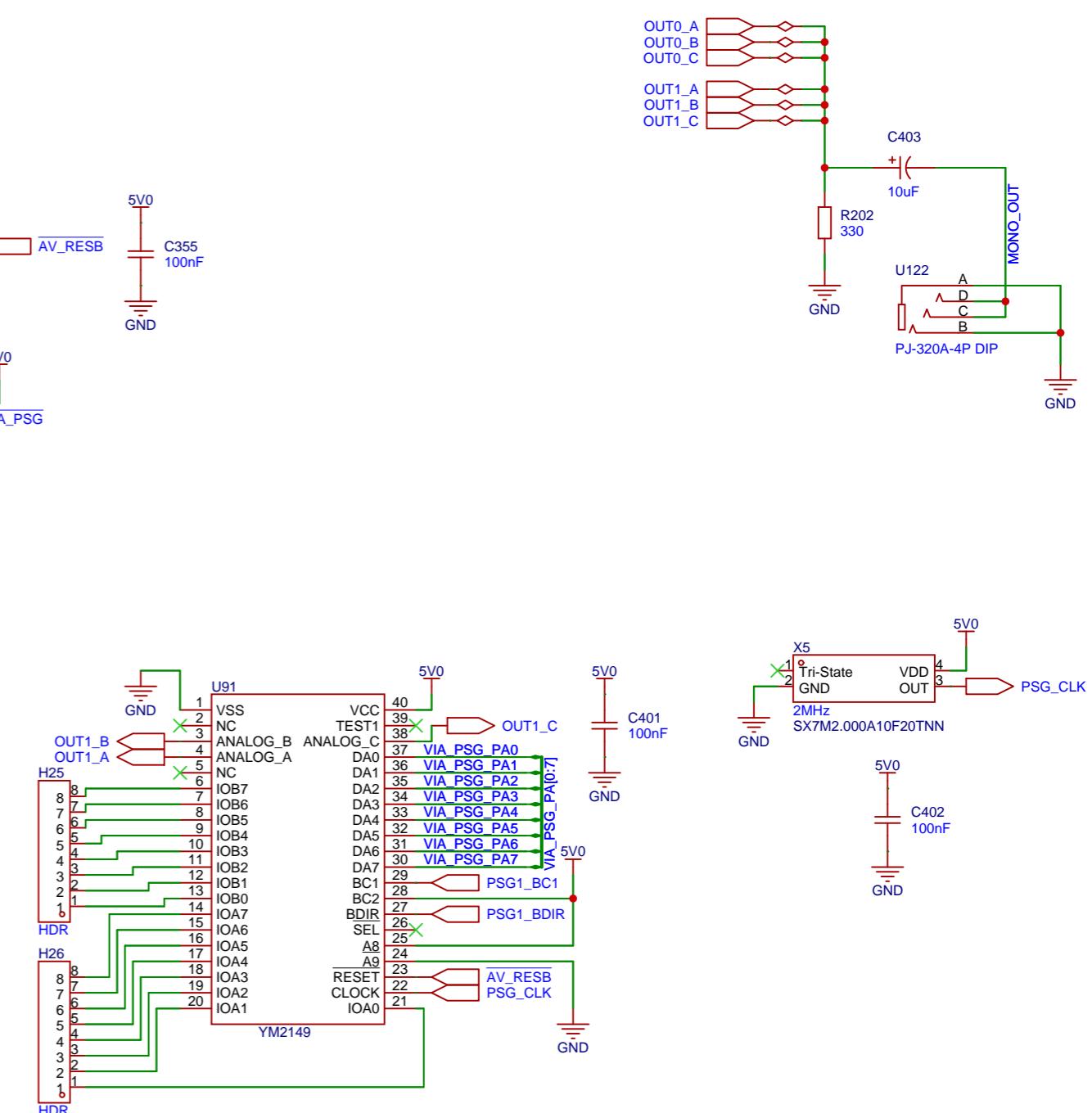
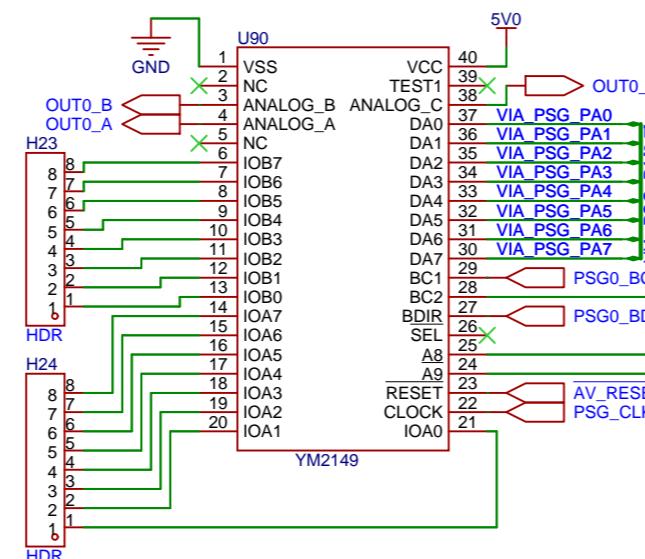
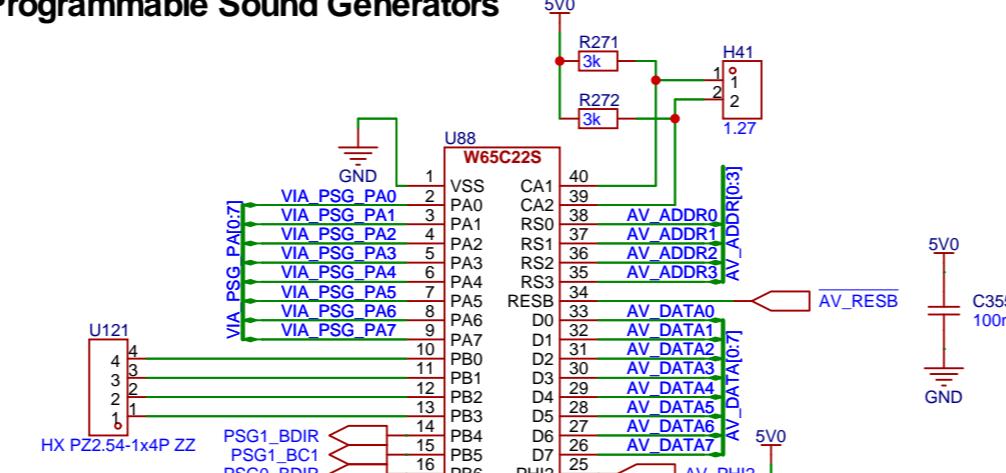
Schematic	Schematic1			Create at	2026-01-24
Board	Board1			Update at	2026-01-24
Drawn				Page	Serial
Reviewed					
				W65C265S AV v0.12	
	Version	Size	Page 7 Total 9		
		V1.0	A4	EasyEDA.com	

# Sound

## Tone Generators



## Programmable Sound Generators



Schematic	Schematic1			Create at	2026-01-24
Board	Board1			Update at	2026-01-24
Drawn				Page	Sound
Reviewed					
	Version	Size	Page 8 Total 9		
	V1.0	A4	EasyEDA.com		

# VGA 320x240 x1Byte

**RRRGGBB**

VGA Signal 320 x 240 @ 60 Hz  
General timing  
Screen refresh rate 60 Hz  
Vertical refresh 31.46875 kHz  
Pixel freq. 12.5875 MHz

```

Horizontal timing (line)
Polarity of horizontal sync pulse is negative.
Scanline partPixelsTime [μs]
Visible area320212.711
Front porch80.318   320 101000000
Sync pulse481.907   328 101001000
Back porch240.953   376 101111000
Whole line40015.889   400 110010000

```

```
Vertical timing (frame)
Polarity of vertical sync pulse is negative.
Frame partLinesTime [ms]
Visible area48015.253
Front porch100.318    480 0111100000
Sync pulse20.064      490 0111101010
Back porch331.049     492 0111101100
Whole frame52516.683   525 1000001101
```

320x240 x1Byte  
-3bit Red  
-3bit Green  
-2bit Blue

IO2\_EN OR'd with MEMR#/MEMW# to generate VMEMOE# and VMEMEW#  
CS7B is C0:0000 to FF:FFFF  
OE3B is E0:0000 to EF:0000  
Video MRB/MWB are EA:0000 to EB:FFFF

## DECODE

The diagram illustrates the connection of the GAL22V10D-10LJ chip to external memory. The chip has 26 pins, with pins 1 through 14 connected to RAM and pins 15 through 26 connected to VRAM.

- RAM Side:**
  - Pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, and 14 are connected to RAM. Pin 14 is labeled **RAM\_OE**.
  - Pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, and 14 are also connected to the **GND** rail.
- VRAM Side:**
  - Pins 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, and 26 are connected to VRAM.
  - Pins 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, and 26 are also connected to the **GND** rail.

On the left, a 5V0 source is connected to pin 14 (RAM\_OE) via a 100nF capacitor C374. A ground connection is also shown.

On the right, the VRAM connection is detailed as follows:

- Pin 26: VID\_0\_LQ
- Pin 25: VID\_0\_HI
- Pin 24: VID\_1\_LQ
- Pin 23: VID\_1\_HI
- Pin 22: NC
- Pin 21: VIDOUT\_0\_LQ
- Pin 20: VIDOUT\_0\_HI
- Pin 19: VIDOUT\_1\_LQ
- Pin 18: VIDOUT\_1\_HI
- Pin 17: NC
- Pin 16: NC
- Pin 15: NC

Annotations on the right side provide additional context:

- Video address (for enable)
- A19=1
- A18=0
- A17=1
- When A16=0, lower 64K (f)
- When A16=1, upper 64K (l)
- When A0=0, LO byte
- When BHE (!A0) = 0, HI by

## LOWER 64K (VID\_0)

The diagram illustrates the connection of the AV\_ADDR1 pin (shifted AV\_ADDR1[1:15]) to the VA1 pin. The AV\_ADDR1 pin is connected to the U6 chip via a red wire. The U6 chip has pins 55 (A0L), 56 (A1L), 57 (A2L), 58 (A3L), 59 (A4L), 60 (A5L), 61 (A6L), 62 (A7L), 63 (A8L), 64 (A9L), 65 (A10L), 66 (A11L), 67 (A12L), and 68 (VCC). The U6 chip is connected to the IDT7007 chip via a green wire. The IDT7007 chip has pins 48 (A0R), 49 (A1R), 50 (A2R), 51 (A3R), 52 (A4R), 53 (A5R), 54 (A6R), 55 (A7R), 56 (A8R), 57 (A9R), 58 (A10R), 59 (A11R), and 60 (A12R). The IDT7007 chip is connected to the VA1 pin via a blue wire. The VA1 pin is labeled "VA[1:15]". A GND connection is shown at pin 22 of U6 and pin 68 of IDT7007. A 5V0 connection is shown at pin 17 of U6.

such as a

5V0

C367  
100nF

C368  
100nF

C369  
100nF

GND

5V0

U7

AV\_ADDR1 55 A0L VCC 17 48 VA1  
AV\_ADDR2 56 A1L VCC 22 47 VA2  
AV\_ADDR3 57 A2L VCC 69 46 VA3  
AV\_ADDR4 58 A3L VCC 45 VA4  
AV\_ADDR5 59 A4L VCC 44 VA5  
AV\_ADDR6 60 A5L VCC 43 VA6  
AV\_ADDR7 61 A6L VCC 42 VA7  
AV\_ADDR8 62 A7L VCC 41 VA8  
AV\_ADDR9 63 A8L VCC 40 VA9  
AV\_ADDR10 64 A9L VCC 39 VA10  
AV\_ADDR11 65 A10L VCC 38 VA11  
AV\_ADDR12 66 A11L VCC 37 VA12  
AV\_ADDR13 67 A12L VCC 36 VA13  
VA1.5

IDT7007

The diagram illustrates two sets of 16-bit parallel-to-serial converters. Each converter consists of a red input bus (VA15 to VA0 or HQ8 to HQ0) and a red output bus. A green diamond symbol is positioned at the center of each converter.

Input Bus	Output Bus
VA15	VQ7
VA14	VQ6
VA13	VQ5
VA12	VQ4
VA11	VQ3
VA10	VQ2
VA9	VQ1
VA8	HQ8
VA7	HQ7
VA6	HQ6
VA5	HQ5
VA4	HQ4
VA3	HQ3
VA2	HQ2
VA1	HQ1
VA0	HQ0

chematic	Schematic1		Create at	2026-01-24
			Update at	2026-01-24
oard	Board1		Page	VGA
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		Version	Size	Page 9 Total 9
 EasyEDA	V1.0	A4	EasyEDA.com	

**VSYNC**

The diagram shows the pinout of the GAL22V10D-10LJ chip. Pins 1 through 14 are connected to various logic functions and ground. Pin 14 is connected to GND. Pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, and 14 are each connected to a green NC (No Connection) terminal. Pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, and 14 are also connected to a green NC terminal. Pin 15 is connected to GND. Pin 16 is connected to the VSYNC output. Pin 17 is connected to the VBLANK output. Pin 18 is connected to the I/O/Q17 output. Pin 19 is connected to the I/O/Q18 output. Pin 20 is connected to the I/O/Q20 output. Pin 21 is connected to the I/O/Q21 output. Pin 22 is connected to the I/O/Q22 output. Pin 23 is connected to the I/O/Q23 output. Pin 24 is connected to the I/O/Q24 output. Pin 25 is connected to the I/O/Q25 output. Pin 26 is connected to the I/O/Q26 output. Pin 27 is connected to the I/O/Q27 output. Pin 28 is connected to the VCC supply. Pin 29 is connected to the 5V0 supply. Pin 30 is connected to the C10 capacitor.

The diagram shows the connections of the U1117 chip. Pin 28 is connected to VCC (Pin 1). Pin 27 is connected to I/O/Q (Pin 26). Pin 26 is connected to I/O/Q (Pin 25). Pin 25 is connected to I/O/Q (Pin 24). Pin 24 is connected to I/O/Q (Pin 23). Pin 23 is connected to I/O/Q (Pin 22). Pin 22 is connected to NC. Pin 21 is connected to I/O/Q (Pin 20). Pin 20 is connected to I/O/Q (Pin 19). Pin 19 is connected to I/O/Q (Pin 18). Pin 18 is connected to I/O/Q (Pin 17). Pin 17 is connected to I/O/Q (Pin 16). Pin 16 is connected to EOH (Pin 15). Pin 15 is connected to HBLANK (Pin 14). Pin 14 is connected to HSYNC (Pin 13). Pin 13 is connected to GND. Pin 12 is connected to I/O/Q (Pin 11). Pin 11 is connected to I/O/Q (Pin 10). Pin 10 is connected to I/O/Q (Pin 9). Pin 9 is connected to NC. Pin 1 is connected to NC. Pin 2 is connected to I/CLK (Pin 3). Pin 3 is connected to HQ8 (Pin 4). Pin 4 is connected to HQ7 (Pin 5). Pin 5 is connected to HQ6 (Pin 6). Pin 6 is connected to HQ5 (Pin 7). Pin 7 is connected to HQ4 (Pin 8). Pin 8 is connected to NC. Pin 14 is connected to GND. Pin 15 is connected to NC. Pin 16 is connected to 31.46875 kHz. Pin 17 is connected to HSYNC. Pin 18 is connected to I/O/Q. Pin 19 is connected to I/O/Q. Pin 20 is connected to I/O/Q. Pin 21 is connected to I/O/Q. Pin 22 is connected to NC. Pin 23 is connected to I/O/Q. Pin 24 is connected to I/O/Q. Pin 25 is connected to I/O/Q. Pin 26 is connected to I/O/Q. Pin 27 is connected to I/O/Q. Pin 28 is connected to VCC. A 5V0 source is connected to Pin 1 and Pin 28. A 5V0 source is connected to Pin 1 and GND. A capacitor C1 is connected between Pin 1 and GND.

This diagram shows the pinout for the VGA-002 component. The pins are numbered 1 through 17. The connections are as follows:

- Pins 1, 2, and 3 are connected to OUT\_RED, OUT\_GREEN, and OUT\_BLUE respectively.
- Pins 4, 5, and 6 are connected to GND.
- Pins 7, 8, and 9 are connected to GND.
- Pins 10, 11, and 12 are connected to GND.
- Pins 13 and 14 are connected to H\_SYNC and V\_SYNC respectively.
- Pins 15 and 16 are connected to R, G, and B respectively.
- Pins 17 and 18 are connected to CHASSIS\_GND.

The diagram illustrates three parallel signal processing paths, each consisting of an input signal, a resistor, a 536 ohm resistor, a 270 ohm resistor, and an output signal. The paths are as follows:

- RED Path:** Input **RED2** passes through a resistor **R13** (536 ohm) to a junction point. From this junction, the signal splits into two parallel branches. The top branch contains a 270 ohm resistor **R160** and a ground connection. The bottom branch contains a 270 ohm resistor **R161**. Both branches converge at another junction point, which then passes through a 100 ohm resistor **R170** and a ground connection to produce the output **OUT\_RED**.
- GREEN Path:** Input **GREEN2** passes through a resistor **R155** (536 ohm) to a junction point. From this junction, the signal splits into two parallel branches. The top branch contains a 270 ohm resistor **R163** and a ground connection. The bottom branch contains a 270 ohm resistor **R164**. Both branches converge at another junction point, which then passes through a 100 ohm resistor **R168** and a ground connection to produce the output **OUT\_GREEN**.
- BLUE Path:** Input **BLUE1** passes through a resistor **R158** (536 ohm) to a junction point. From this junction, the signal splits into two parallel branches. The top branch contains a 270 ohm resistor **R166** and a ground connection. The bottom branch contains a 100 ohm resistor **R169**. Both branches converge at another junction point to produce the output **OUT\_BLUE**.

SN74HC273PWR

U14

5V0

RED2  
VD7  
VD6  
RED1  
RED0  
VD5  
VD4  
GREEN2  
PIXEL\_CLK

C371  
100nF

GND