# TO DO

To do:
-Pin1 markings on headers
-10pF instead of 47/27pF on crystal circuits, along with 150 instead of 1.5k
-Cuttable connections or 0 ohm resistors for questionable tracks
-Verify no VCC nets (should be 5V0)
-Rename both GAL's OEBs from generic to specific and verify throughout
-Triple-check decode ranges and enables
-Verify no components without LCSC equiv. part #
-Print to scale, test fit (especially TFT LCD & ZIFs)
-Review all status LEDs to confirm they are on good pins for showing status
-Verify fill on all layers & rebuild
-External transceivers and/or clock distribution ICs needed? (really long traces)

# System Block Diagram

# Conventions (e.g., naming)

-Signals for secondary (audio-visual co-processor) MCU prefaced with "AV_"
-Tracks more likely needing bodging on bottom layer
-Horizontal tracks - Top, InnerLower
-Vertical tracks - InnerUpper

# Memory Map, Native Decode

| *W65C265SXB Memory Map* | | | | |
|---|---|---|---|---|
| ***Start*** | ***End*** | ***Size*** | ***Chip Select*** | ***Description*** |
| (C0) | (FF) | 4 MB | CS7B | USER MEMORY (FOR EXPANSION) |
| (40) | (BF) | 8 MB | CS6B | USER MEMORY (FOR EXPANSION) |
| (00) | (3F) | 4 MB | CS5B | MEMORY *See Note 2* |
| (00)E000<br>(00)8000 | (00)FFFF<br>(00)DEFF | 8192 B<br>24320 B | CS4B | ROM MEMORY (*Note 1*)<br>ROM MEMORY (*Note 1*) |
| (00)0200 | (00)7FFF | 32256 | CS3B | Cache Memory *See Note 3* |
| (00)FF00<br>(00)E000<br>(00)DF80<br>(00)DF70<br>(00)DF50<br>(00)DF40<br>(00)DF20<br>(00)DF00<br>(00)0000 | (00)FFFF<br>(00)FEFF<br>(00)DFBF<br>(00)DF7F<br>(00)DF6F<br>(00)DF4F<br>(00)DF27<br>(00)DF07<br>(00)01FF | 256 B<br>7936 B<br>64 B<br>16 B<br>32 B<br>16 B<br>8 B<br>8 B<br>512 B | CS2B | On Chip Interrupt Vectors<br>On-Chip ROM<br>On-Chip RAM<br>On-Chip Comm. Registers<br>On-Chip Timer Registers<br>On-Chip Control Registers<br>On-Chip IO Registers<br>On-Chip IO Registers<br>On-Chip RAM |
| (00)DFC0 | 0xDFFF | 64 B | CS1B | External Chip Select 1 (P71) |
| (00)DF00 | 0xDF1F | 32 B | CS0B | External Chip Select 0 (P70) *See Note 4* |

I/O Devices: See GAL Decode

Extended Flash 512 KB

Extended SRAM 2 MB (01):(02)
Dual-port SRAM (03)

Primary Flash 128 KB (four 32 KB sections)

SRAM 32 KB

Note 1 - When on-chip 8K bytes of ROM are enabled:
a.) Addresses (00)E000-FFFF will not appear in CS4B chip select decode.
b.) On Chip addresses (00)DF00-DFFF never appear in CS4B or CS5B chip select decode.

Note 2 - When on-chip ROM, CS3B and/or CS4B are enabled:
a.) CS5B decode is reduced by the addresses used by same.
b.) CS0B and CS1B address space never appears in CS2B, CS4B or CS5B decoded space.

Note 3 - When SSCR2 is "0" (internal RAM), then CS3B is active for addresses (00)0200-7FFF. When SSCR2 is "1" (external RAM), then CS3B is active for addresses (00)0000-7FFF.

Note 4 - CS0B is inactive when 00DF00-00DF07 are used for internal I/O register select (BCR0=0). When (BCR0=1) external memory bus is enabled CS0B is active for addresses 00DF00-00DF1F.

# Extended Decode (GAL)

C0:0000 to FF:FFFF CS7B

1100:0000000000000000000 to
1111:1111111111111111111
(range: top two bits are 11)

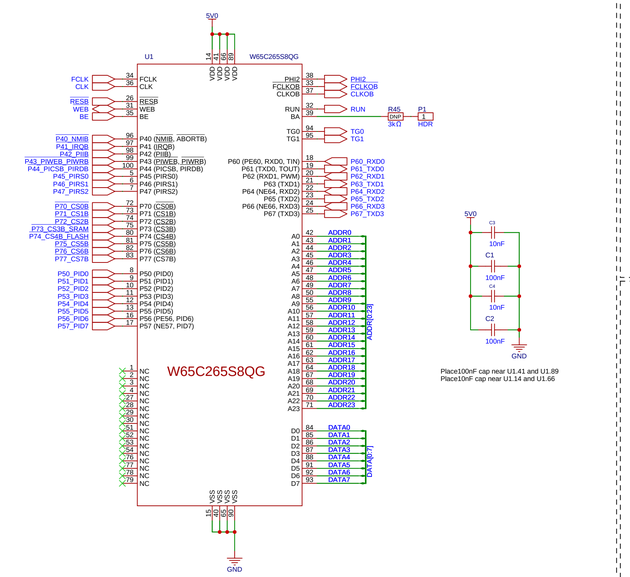
1100: VIA0 C0:xxxx C0:0000 to C0:000F
1101: VIA1 D0:xxxx D0:0000 to D0:000F
1110: VIA2 E0:xxxx E0:0000 to E0:000F
1111: VIA3 F0:xxxx F0:0000 to F0:000F

**re-map I/O by bringing in additional address lines
see Overview page for details

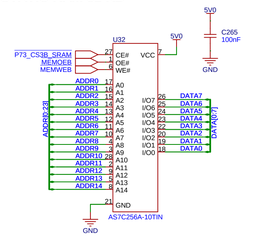
| | | | |
|---|---|---|---|
| Schematic | Schematic1 | Create at | 2026-01-05 |
| | | Update at | 2026-01-05 |
| Board | Board1 | Page | Overview |
| Drawn | | W65C265S v0.12 | |
| Reviewed | | | |
| | | Version | Size | Page 1 Total 12 |
| EasyEDA | | V1.0 | A4 | EasyEDA.com |

# MCU (Primary)

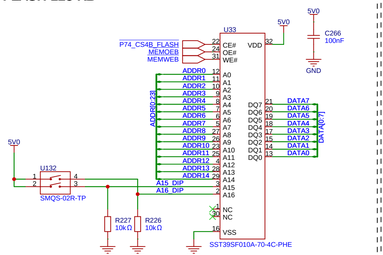
## 65265 MCU



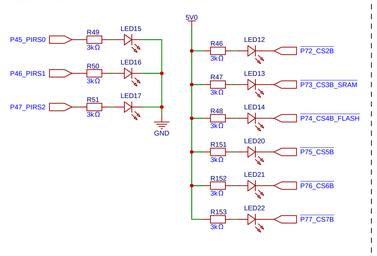

## STATIC RAM 32 KB



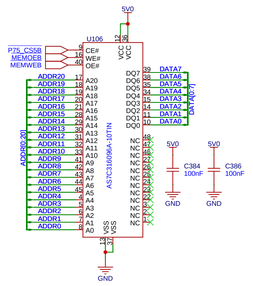

## FLASH 128 KB



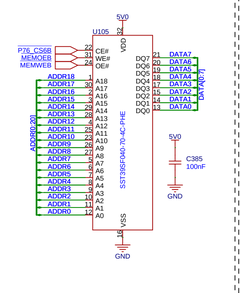

## LED INDICATORS



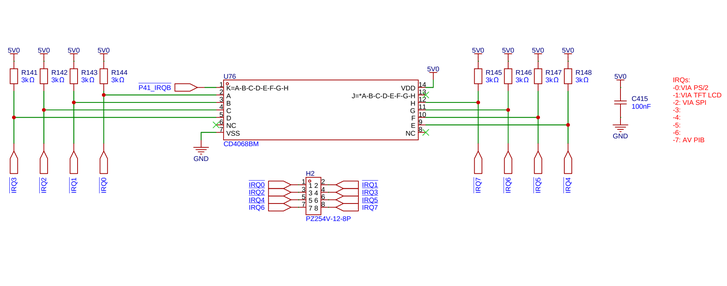

## STATIC RAM 2 MB



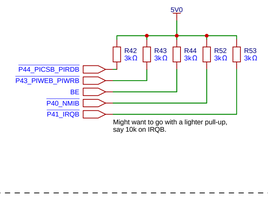

## FLASH 512 KB



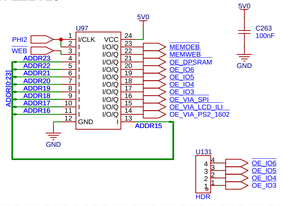

## IRQs

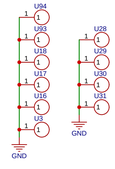



## PULL-UPS




## GAL22V10

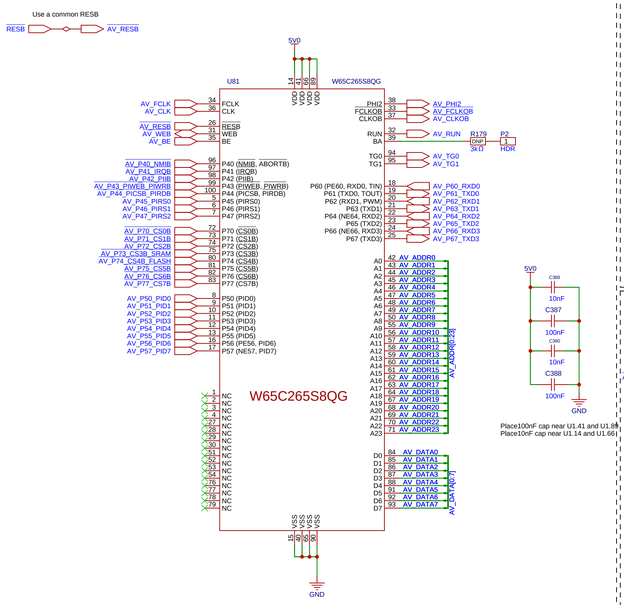


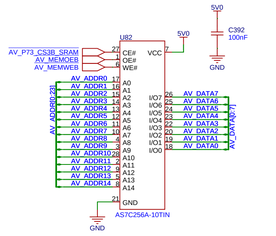

| | | | |
|---|---|---|---|
| Schematic | Schematic1 | Create at | 2026-01-05 |
| | | Update at | 2026-01-04 |
| Board | Board1 | Page | MCU Primary |
| Drawn | | W65C265S v0.12 | |
| Reviewed | | | |
| | | Version | Size | Page 2 Total 12 |
| EasyEDA | | V1.0 | A4 | EasyEDA.com |

# MCU (AV)

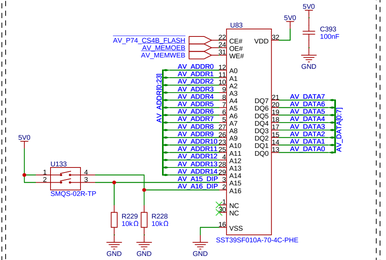
## 65265 MCU



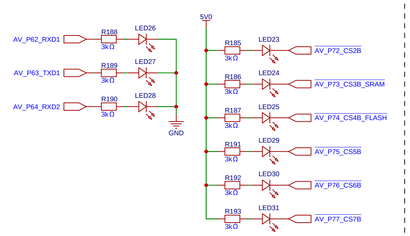

## STATIC RAM 32 KB



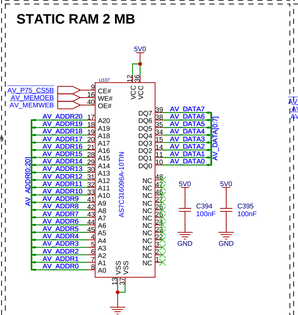

## FLASH 128 KB



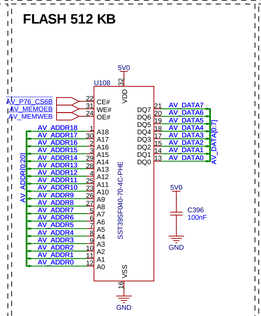

## LED INDICATORS



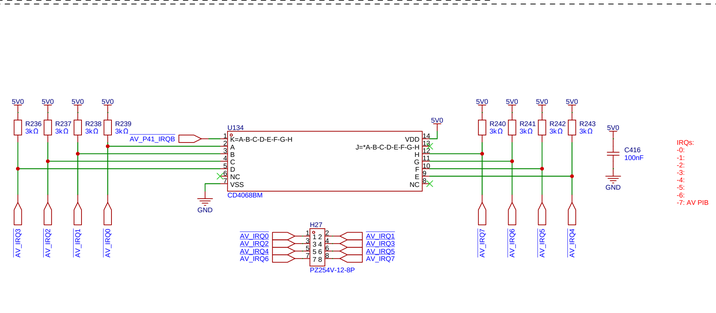

## STATIC RAM 2 MB




## FLASH 512 KB

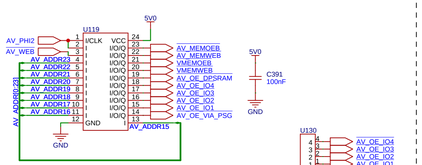



## IRQs



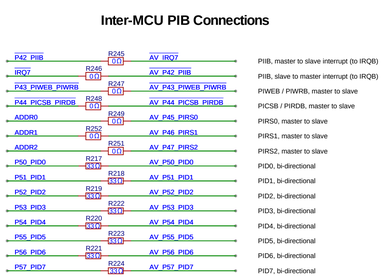

## PULL-UPS


## GAL22V10

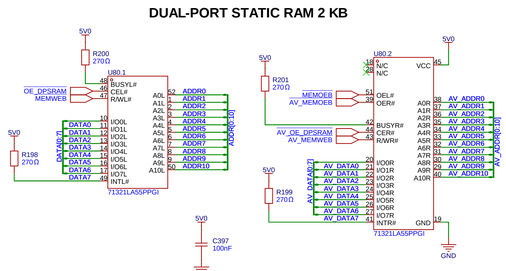



## INTER-MCU

### Inter-MCU PIB Connections



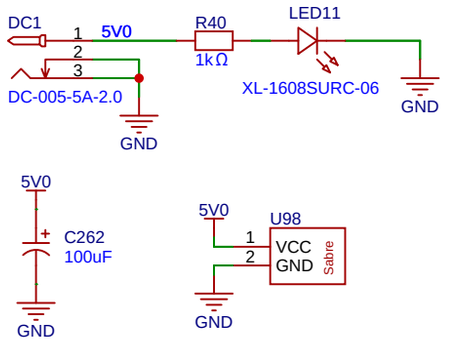

### DUAL-PORT STATIC RAM 2 KB



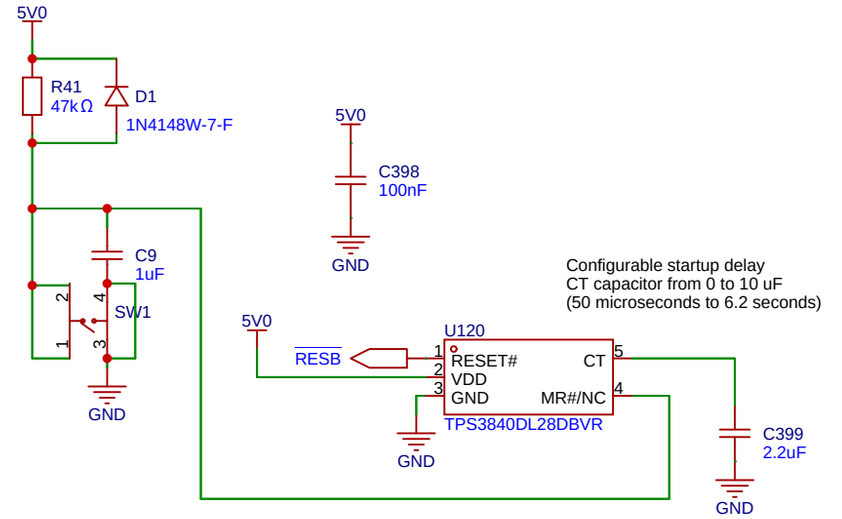

| | | | |
|---|---|---|---|
| Schematic | Schematic1 | Create at | 2026-01-05 |
| | | Update at | 2026-01-04 |
| Board | Board1 | Page | MCU AV |
| Drawn | | W65C265S v0.12 | |
| Reviewed | | | |
| | | Version | Size |
| EasyEDA | | V1.0 | A4 |
| | | Page 3 Total 12 | |
| | | EasyEDA.com | |

# POWER

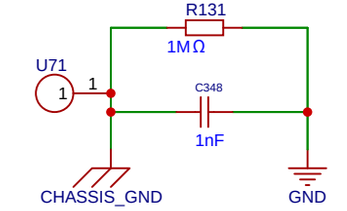
## Input




## Reset




## Chassis Ground

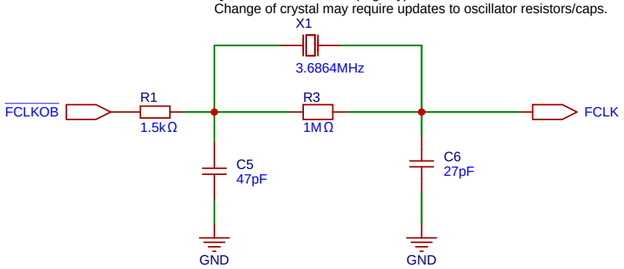


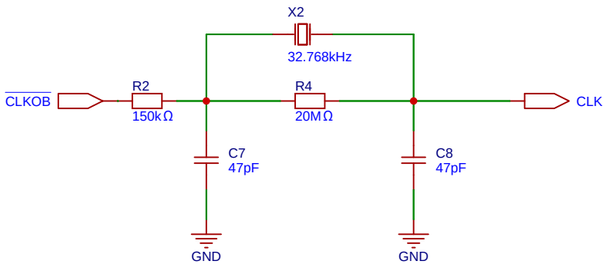

| | | | |
|---|---|---|---|
| Schematic | Schematic1 | Create at | 2026-01-05 |
| | | Update at | 2026-01-04 |
| Board | Board1 | Page | Power |
| Drawn | | W65C265S v0.12 | |
| Reviewed | | | |
| | | | |
| | | Version | Size | Page 4 Total 12 |
| EasyEDA | | V1.0 | A4 | EasyEDA.com |

# CLOCKS

## PRIMARY

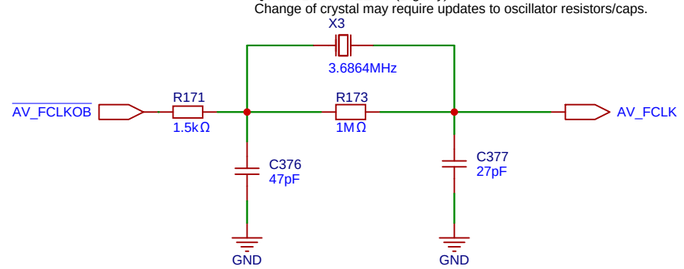
10 MHz Crystal option:
QT49S-10.000MEEJ-T (Digikey)
Change of crystal may require updates to oscillator resistors/caps.

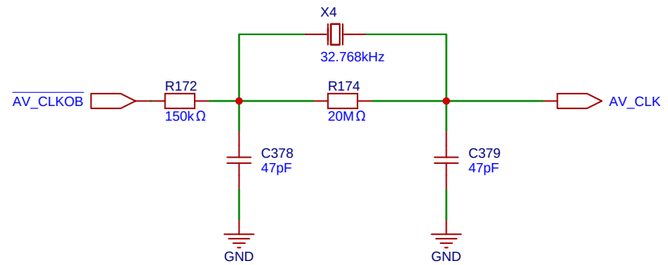



## AV

10 MHz Crystal option:
QT49S-10.000MEEJ-T (Digikey)
Change of crystal may require updates to oscillator resistors/caps.




| | | | |
|---|---|---|---|
| Schematic | Schematic1 | Create at | 2026-01-05 |
| | | Update at | 2026-01-04 |
| Board | Board1 | Page | Clocks |
| Drawn | | W65C265S v0.12 | |
| Reviewed | | | |
| | | Version | Size | Page 5 Total 12 |
| EasyEDA | | V1.0 | A4 | EasyEDA.com |

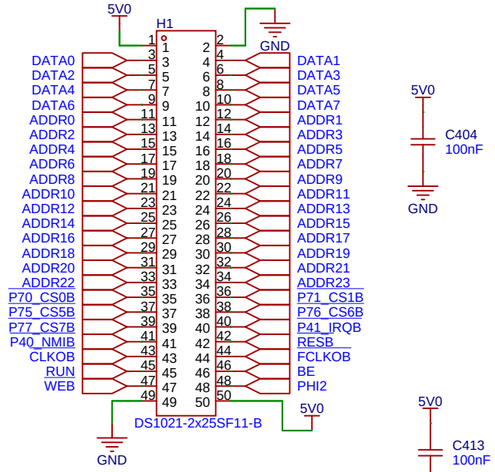
# EXPANSION

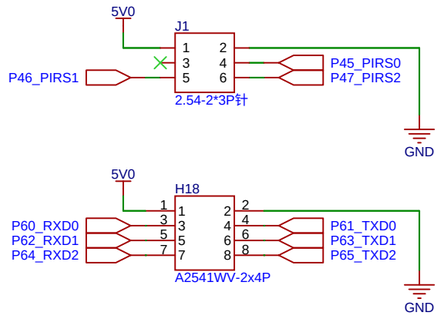
Used:

P50:56 - 1602 LCD
P51 - Available

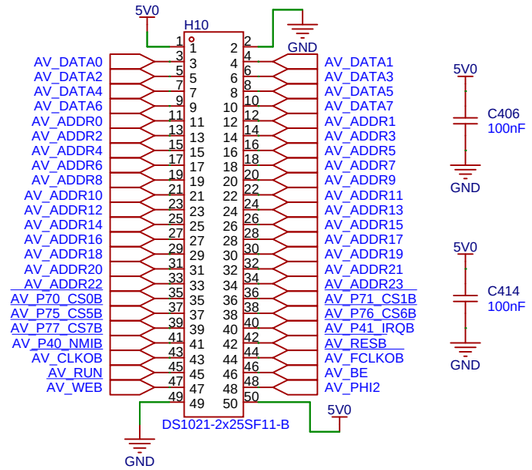
P62 - PS2KBD DATA
P64 - PS2KBD CLK
P66 - RXD3
P67 - TXD3

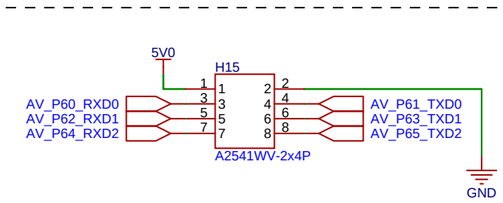
## Primary XBus265




## AV XBus265

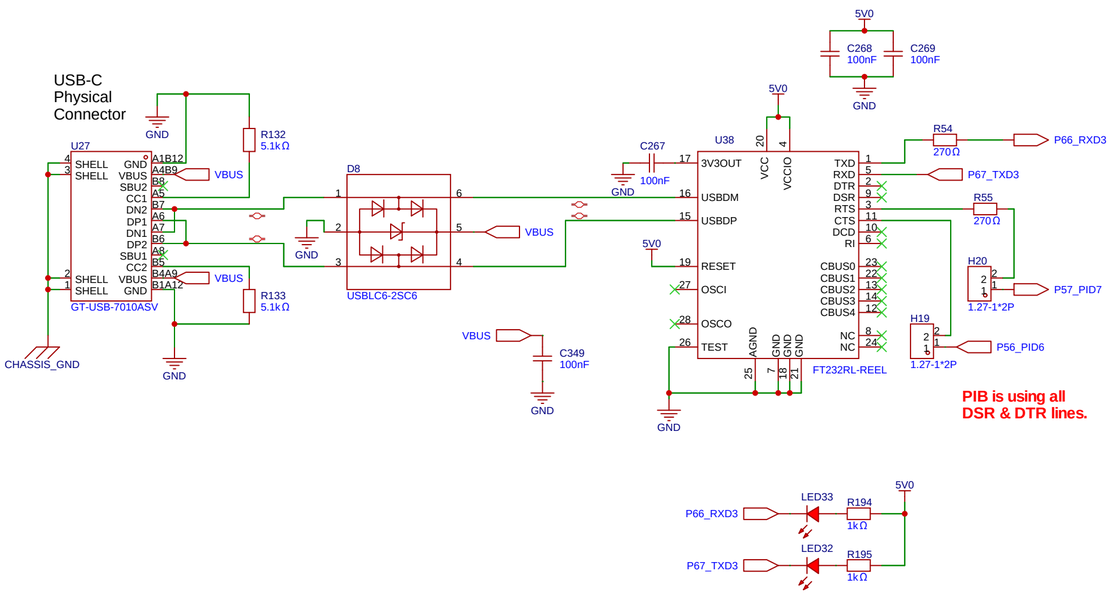


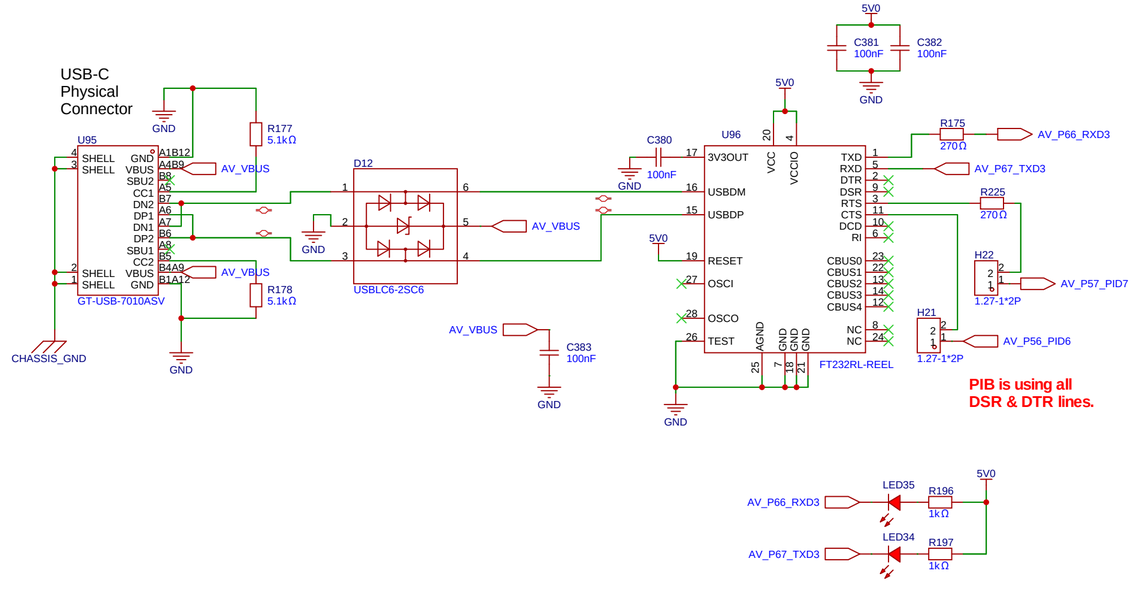

| | | | |
|---|---|---|---|
| Schematic | Schematic1 | Create at | 2026-01-05 |
| | | Update at | 2026-01-04 |
| Board | Board1 | Page | Expansion |
| Drawn | | W65C265S v0.12 | |
| Reviewed | | | |
| | | Version | Size | Page 6 Total 12 |
| EasyEDA | | V1.0 | A4 | EasyEDA.com |

# USB SERIAL, PS/2 KEYBOARD

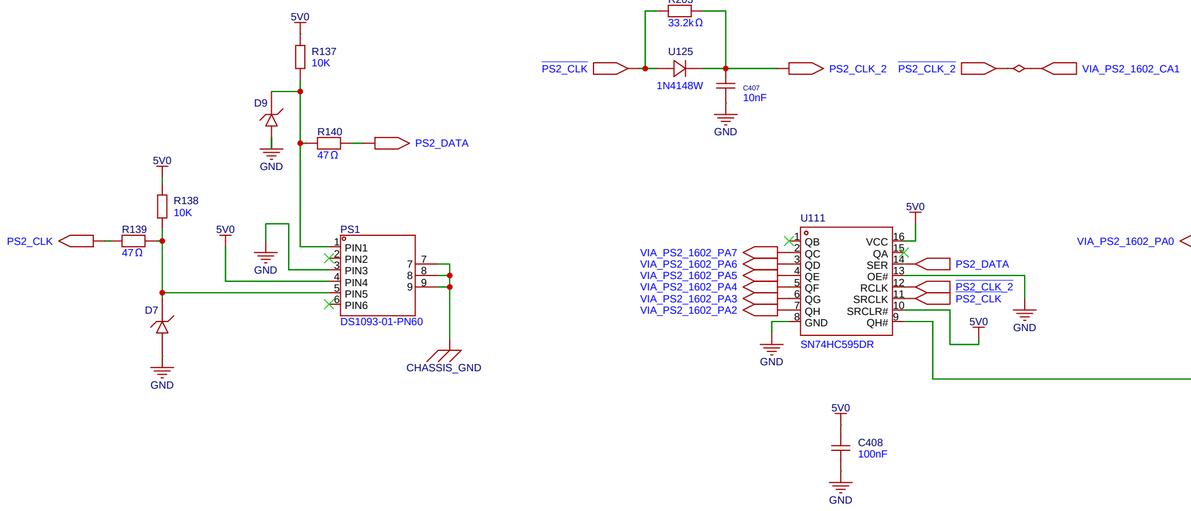
## Primary



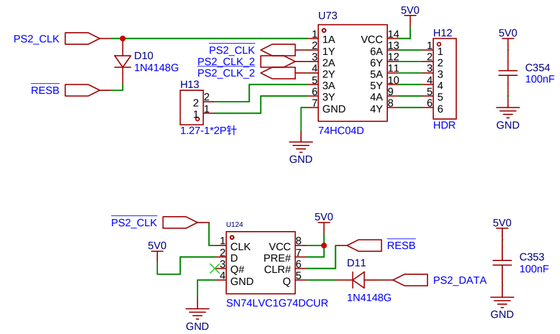

## AV




## PS/2 Keyboard - Primary




## PS/2 Auto-reset

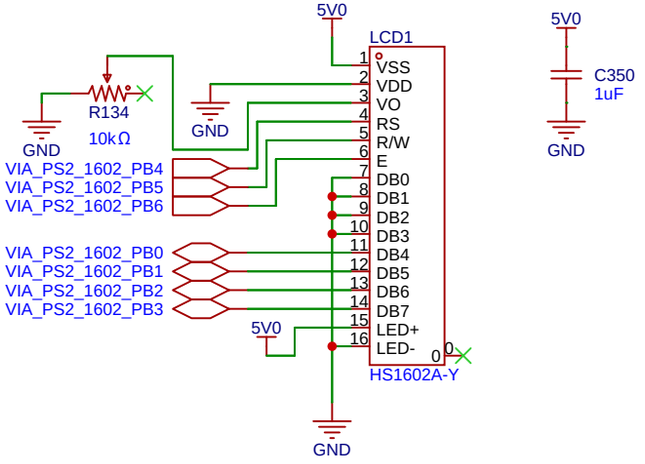



Auto-reset for keyboards that require it.
*credit to u/gfoot360 (George Foot)

Temporary: unconnected pins
for inputs to be grounded

| | | | |
|---|---|---|---|
| Schematic | Schematic1 | Create at | 2026-01-05 |
| | | Update at | 2026-01-05 |
| Board | Board1 | Page | Serial & PS2 |
| Drawn | | W65C265S v0.12 | |
| Reviewed | | | |
| | | Version | Size | Page 7 Total 12 |
| EasyEDA | | V1.0 | A4 | EasyEDA.com |

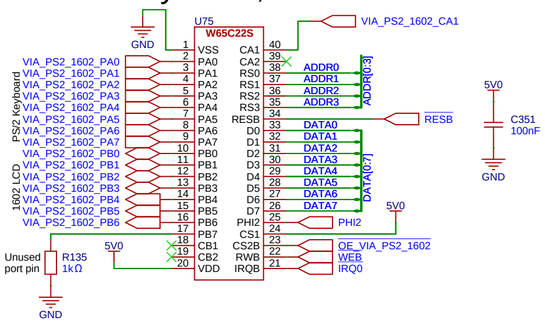
# LCD 1602



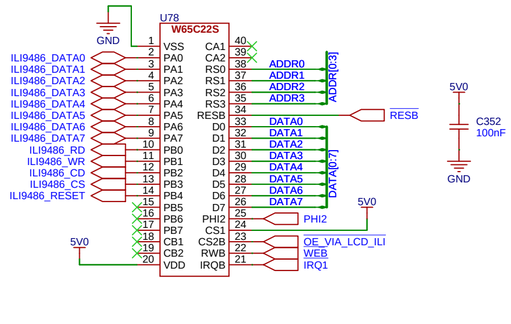

| | | | |
|---|---|---|---|
| Schematic | Schematic1 | Create at | 2026-01-05 |
| | | Update at | 2026-01-04 |
| Board | Board1 | Page | LCD_1602 |
| Drawn | | W65C265S v0.12 | |
| Reviewed | | | |
| | | Version | Size | Page 8 Total 12 |
| EasyEDA | | V1.0 | A4 | EasyEDA.com |

# VIAs

## PS/2 Keyboard, 1602 LCD




## TFT LCD (ILI)

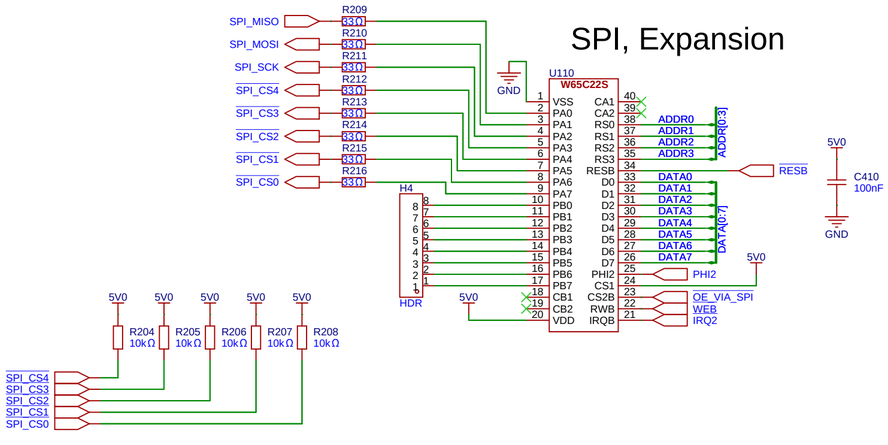



C0:0000 to FF:FFFF CS7B

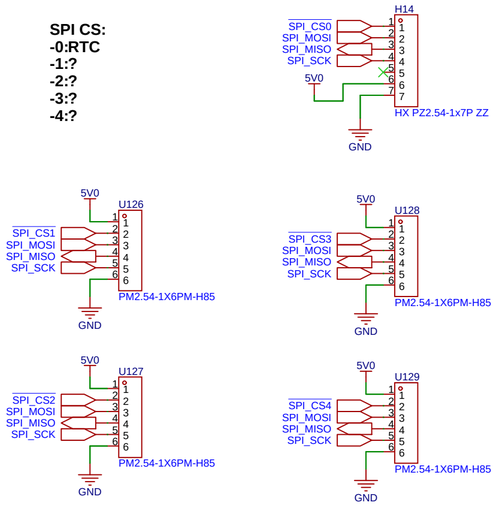
1100:0000000000000000000 to
1111:1111111111111111111
(range: top two bits are 11)

1100: VIA0 C0:xxxx C0:0000 to C0:000F
1101: VIA1 D0:xxxx D0:0000 to D0:000F
1110: VIA2 E0:xxxx E0:0000 to E0:000F
1111: VIA3 F0:xxxx F0:0000 to F0:000F

## SPI, Expansion



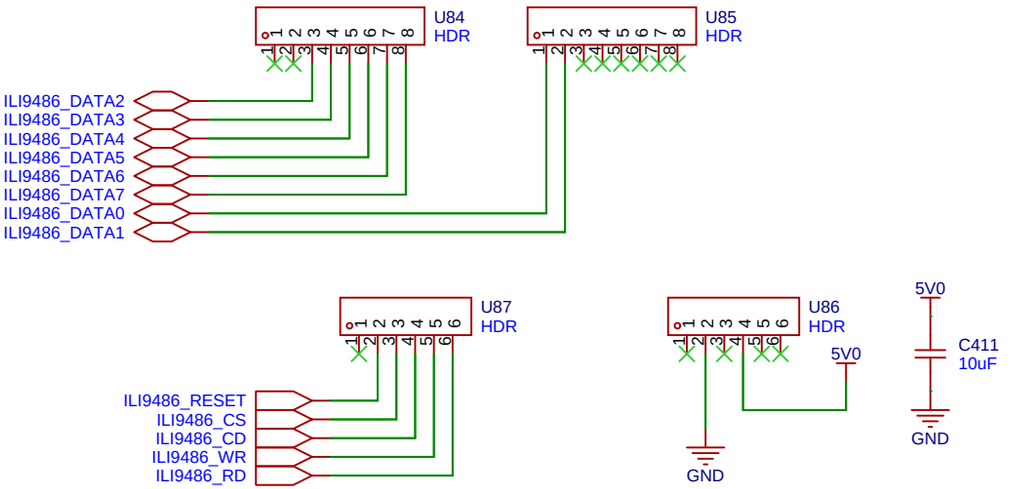

**SPI CS:**
**-0:RTC**
**-1:?**
**-2:?**
**-3:?**
**-4:?**




| | | | |
|---|---|---|---|
| Schematic | Schematic1 | Create at | 2026-01-05 |
| | | Update at | 2026-01-04 |
| Board | Board1 | Page | VIAs |
| Drawn | | W65C265S v0.12 | |
| Reviewed | | | |
| | | Version | Size / Page 9 Total 12 |
| EasyEDA | | V1.0 | A4 / EasyEDA.com |

# LCD - ILI

## Arduino-style header for DIYables TFT LCD

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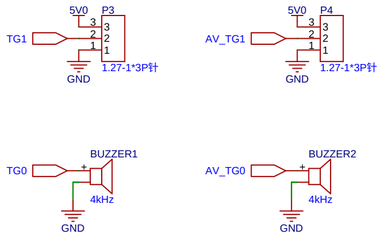
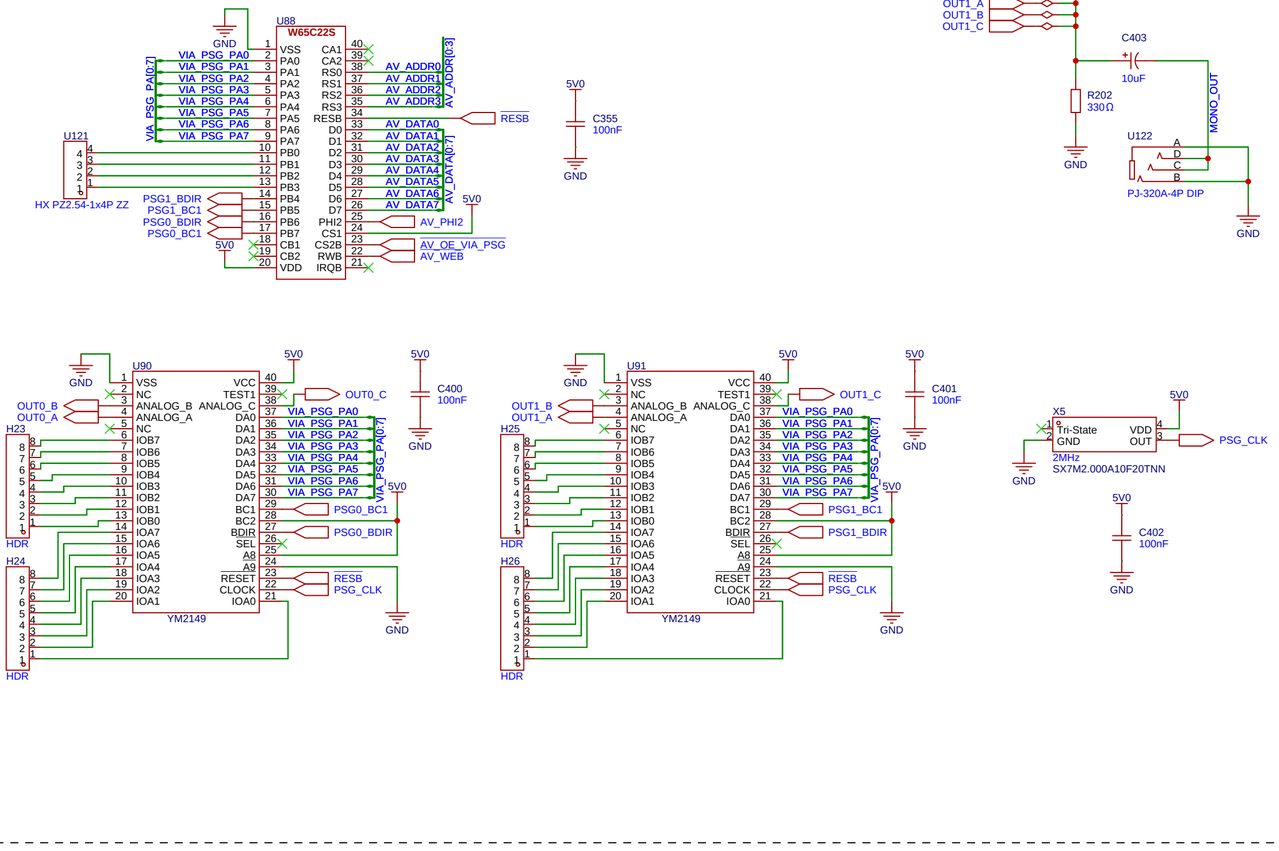
|---|---|---|---|
| Schematic | Schematic1 | Create at | 2026-01-05 |
| | | Update at | 2026-01-04 |
| Board | Board1 | Page | LCD_ILI |
| Drawn | | W65C265S v0.12 | |
| Reviewed | | | |
| | | | |
| | Version | Size | Page 10 Total 12 |
| EasyEDA | V1.0 | A4 | EasyEDA.com |

# Sound

## Tone Generators




## Programmable Sound Generators




| | | | |
|---|---|---|---|
| Schematic | Schematic1 | Create at | 2026-01-04 |
| | | Update at | 2026-01-05 |
| Board | Board1 | Page | Sound |
| Drawn | | W65C265S v0.12 | |
| Reviewed | | | |
| | | Version | Size | Page 11 Total 12 |
| EasyEDA | | V1.0 | A4 | EasyEDA.com |

# VGA 320x240 x1Byte

## RRRGGGBB

VGA Signal 320 x 240 @ 60 Hz

General timing
Screen refresh rate60 Hz
Vertical refresh31.46875 kHz
Pixel freq.12.5875 MHz

Horizontal timing (line)
Polarity of horizontal sync pulse is negative.
Scanline partPixelsTime [µs]
Visible area32012.711
Front porch80.318 320 101000000
Sync pulse481.907 328 101001000
Back porch240.953 376 101111000
Whole line40015.889 400 110010000

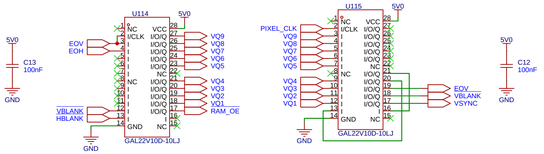
Vertical timing (frame)
Polarity of vertical sync pulse is negative.
Frame partLinesTime [ms]
Visible area48015.253
Front porch100.318 480 0111100000
Sync pulse20.064 490 0111101010
Back porch331.049 492 0111101100
Whole frame52516.683 525 1000001101

320x240 x1Byte
-3bit Red
-3bit Green
-2bit Blue

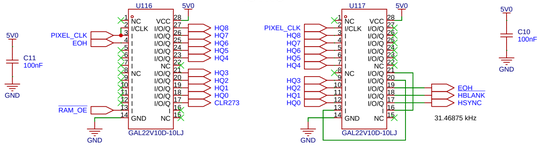
IO2_EN OR'd with MEMR#/MEMW# to generate VMEMOEB and VMEMEWB

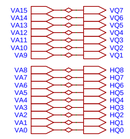
CS7B is C0.0000 to FF.FFFF
OE3B is E0.0000 to EF.0000
Video MRB/MWB are EA.0000 to EB.FFFF

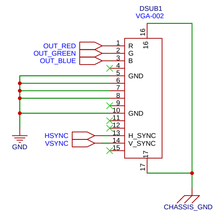
### VSYNC



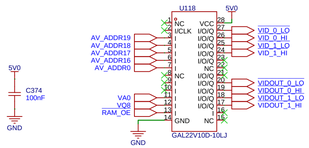

### HSYNC




### DECODE

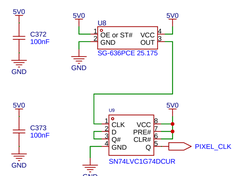



VRAM
0x0A0000-0BFFFF

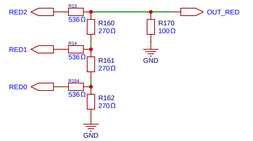
Video address (for enable)
A19=1
A18=0
A17=1

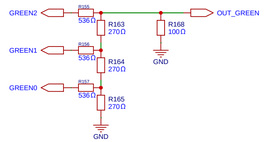
When A16=0, lower 64K (first two SRAMs)
When A16=1, upper 64K (last two SRAMs)

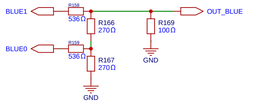
When A0=0, LO byte
When BHE (/A0) =0, HI byte



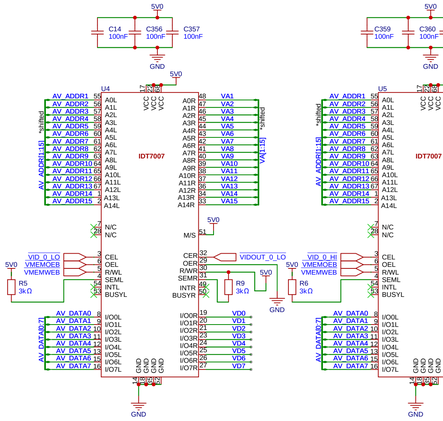

To do:
-fill top / bottom layers with GND
- same with inner signal



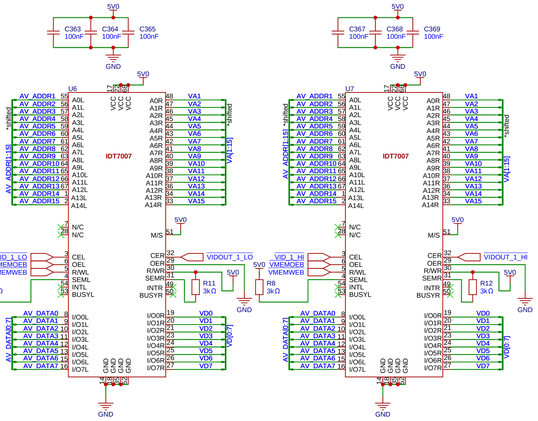



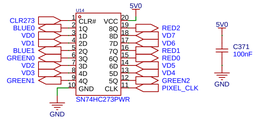




### LOWER 64K (VID_0)




### UIPPER 64K (VID_1)




| | | | |
|---|---|---|---|
| Schematic | Schematic1 | Create at | 2026-01-05 |
| | | Update at | 2026-01-04 |
| Board | Board1 | Page | VGA |
| Drawn | | W65C265S v0.12 | |
| Reviewed | | | |
| | | Version | Size | Page 12 Total 12 |
| EasyEDA | | V1.0 | A4 | EasyEDA.com |