TO DO

To do:
-Triple-check decode logic for all ICs
-Pin1 markings on headers
-10pF instead of 47/27pF on crystal circuits, along with 150 instead of 1.5k
-Cuttable connections or 0 ohm resistors for questionable tracks
-Rename both GAL's OEBs from generic to specific and verify throughout
-Triple-check decode ranges and enables
-Verify no components without LCSC equiv. part #
-Print to scale, test fit (especially TFT LCD & ZIFs)
-Review all status LEDs to confirm they are on good pins for showing status
-Verify fill on all layers & rebuild
-External transceivers and/or clock distribution ICs needed? (really long traces)
-Swap out YM2149 with AY-3-8913?
-Swap out VIAs with PLCC versions?

ISSUES!

-supevisor requires a pull-up on line to '265
-a more appropriate part # (low voltage value) for the monitor should be used

System Block Diagram

Conventions (e.g., naming)

-Signals for secondary (audio-visual co-processor) MCU prefaced with "AV_"
-Tracks more likely needing bodging on bottom layer
-Horizontal tracks - Top, InnerLower
-Vertical tracks - InnerUpper

Memory Map, Native Decode

W65C265SXB Memory Map				
Start	***End***	***Size***	***Chip Select***	***Description***
(C0)	(FF)	4 MB	CS7B	USER MEMORY (FOR EXPANSION)
(40)	(BF)	8 MB	CS6B	USER MEMORY (FOR EXPANSION)
(00)	(3F)	4 MB	CS5B	MEMORY *See Note 2*
(00)E000	(00)FFFF	8192 B	CS4B	ROM MEMORY (*Note 1*)
(00)8000	(00)DEFF	24320 B		ROM MEMORY (*Note 1*)
(00)0200	(00)7FFF	32256	CS3B	Cache Memory *See Note 3*
(00)FF00	(00)FFFF	256 B	CS2B	On Chip Interrupt Vectors
(00)E000	(00)FEFF	7936 B		On-Chip ROM
(00)DF80	(00)DFBF	64 B		On-Chip RAM
(00)DF70	(00)DF7F	16 B		On-Chip Comm. Registers
(00)DF50	(00)DF6F	32 B		On-Chip Timer Registers
(00)DF40	(00)DF4F	16 B		On-Chip Control Registers
(00)DF20	(00)DF27	8 B		On-Chip IO Registers
(00)DF00	(00)DF07	8 B		On-Chip IO Registers
(00)0000	(00)01FF	512 B		On-Chip RAM
(00)DFC0	0xDFFF	64 B	CS1B	External Chip Select 1 (P71)
(00)DF00	0xDF1F	32 B	CS0B	External Chip Select 0 (P70) *See Note 4*

Note 1 - When on-chip 8K bytes of ROM are enabled:
a.) Addresses (00)E000-FFFF will not appear in CS4B chip select decode.
b.) On Chip addresses (00)DF00-DFFF never appear in CS4B or CS5B chip select decode.

Note 2 - When on-chip ROM, CS3B and/or CS4B are enabled:
a.) CS5B decode is reduced by the addresses used by same.
b.) CS0B and CS1B address space never appears in CS2B, CS4B or CS5B decoded space.

Note 3 - When SSCR2 is "0" (internal RAM), then CS3B is active for addresses (00)0200-7FFF. When SSCR2 is "1" (external RAM), then CS3B is active for addresses (00)0000-7FFF.

Note 4 - CS0B is inactive when 00DF00-00DF07 are used for internal I/O register select (BCR0=0). When (BCR0=1) external memory bus is enabled CS0B is active for addresses 00DF00-00DF1F.

(Fx) Interconnect Dual SRAM 2K
(Ex) VGA
(Dx) UNUSED
(Cx) VIA PS/2s

(4x) Extended Flash 512 KB

(00) Extended SRAM 512 KB
First 32K not accessible - see Note 2

(00) Primary Flash 128 KB (four 32 KB sections)

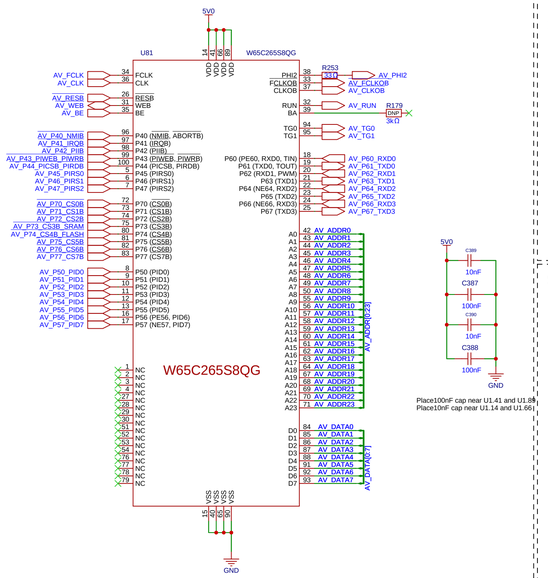
(00) SRAM 32 KB

Extended Decode (GAL)

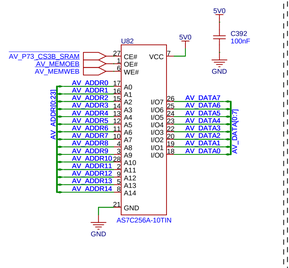
Schematic	Schematic1	Create at	2026-01-24
		Update at	2026-02-21
Board	Board1	Page	Overview
Drawn		W65C265S AV v0.12	
Reviewed			
		Version	Size	Page 1 Total 9
EasyEDA		V1.0	A4	EasyEDA.com

MCU (AV)

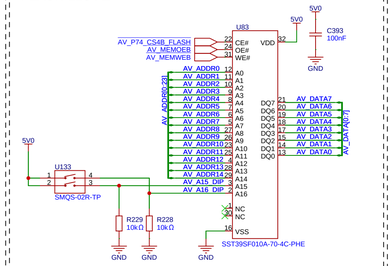
65265 MCU



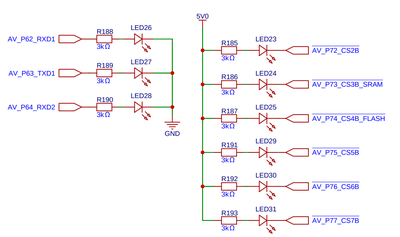
STATIC RAM 32 KB



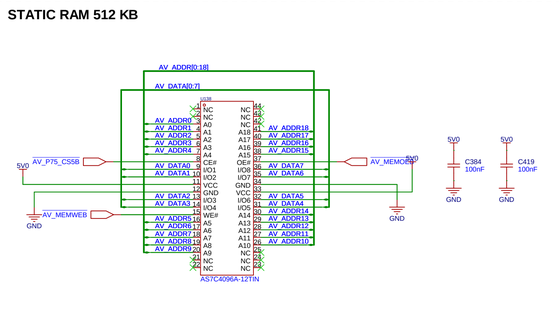
FLASH 128 KB



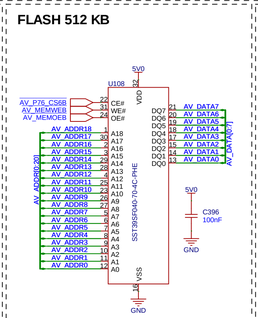
LED INDICATORS



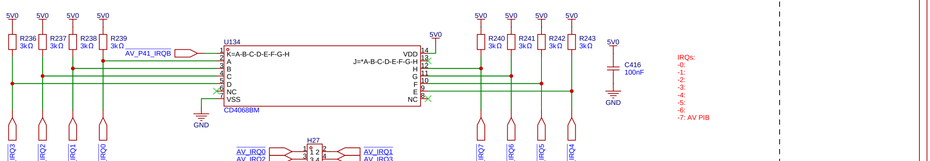
STATIC RAM 512 KB



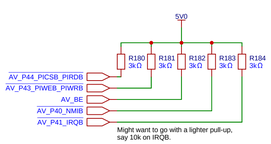
FLASH 512 KB



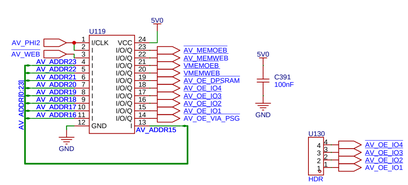
IRQs

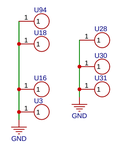


PULL-UPS

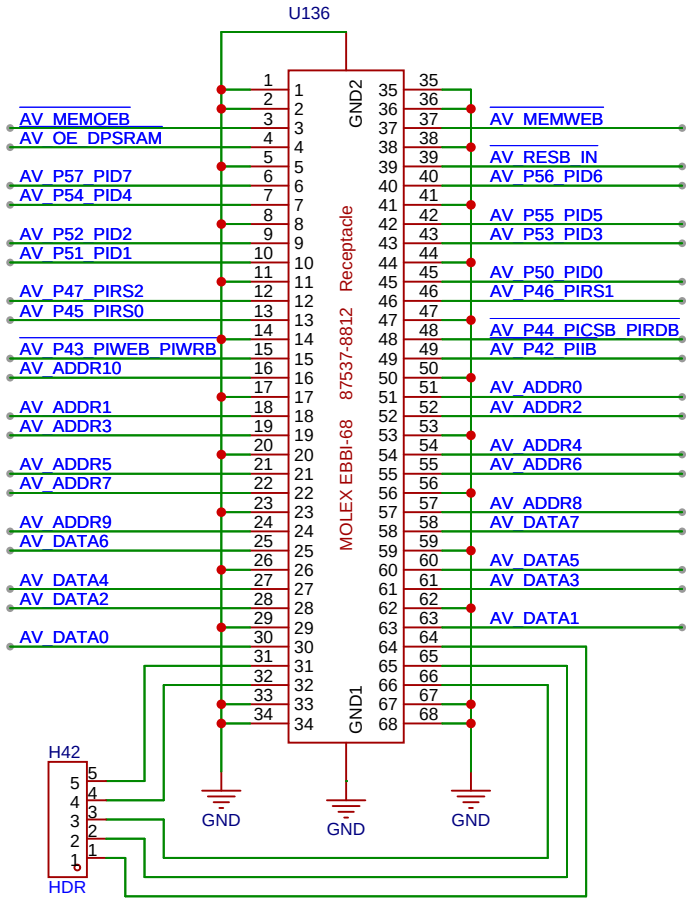


GAL22V10





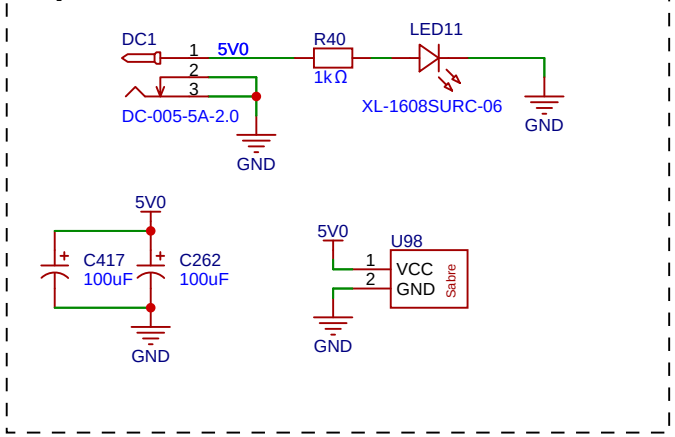
Schematic	Schematic1	Create at	2026-01-24
		Update at	2026-01-24
Board	Board1	Page	MCU AV
Drawn		W65C265S AV v0.12	
Reviewed			
		Version	Size	Page 2 Total 9
EasyEDA		V1.0	A4	EasyEDA.com



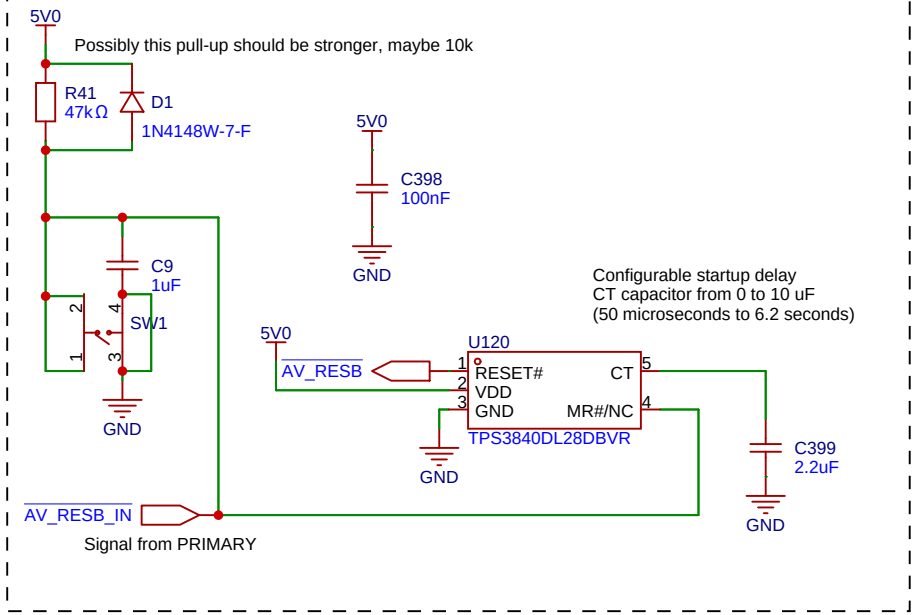
Schematic	Schematic1	Create at	2026-01-24
		Update at	2026-01-24
Board	Board1	Page	Interconnect
Drawn		W65C265S AV v0.12	
Reviewed			
		Version	Size	Page 3 Total 9
EasyEDA		V1.0	A4	EasyEDA.com

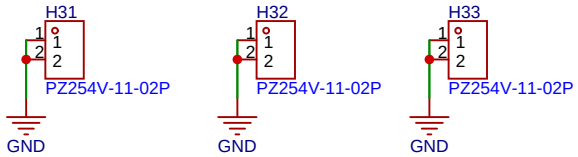
POWER

Input

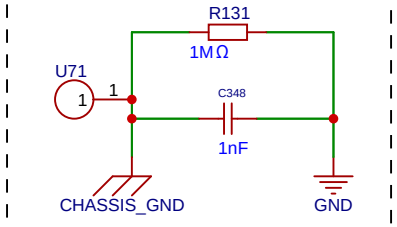


Reset



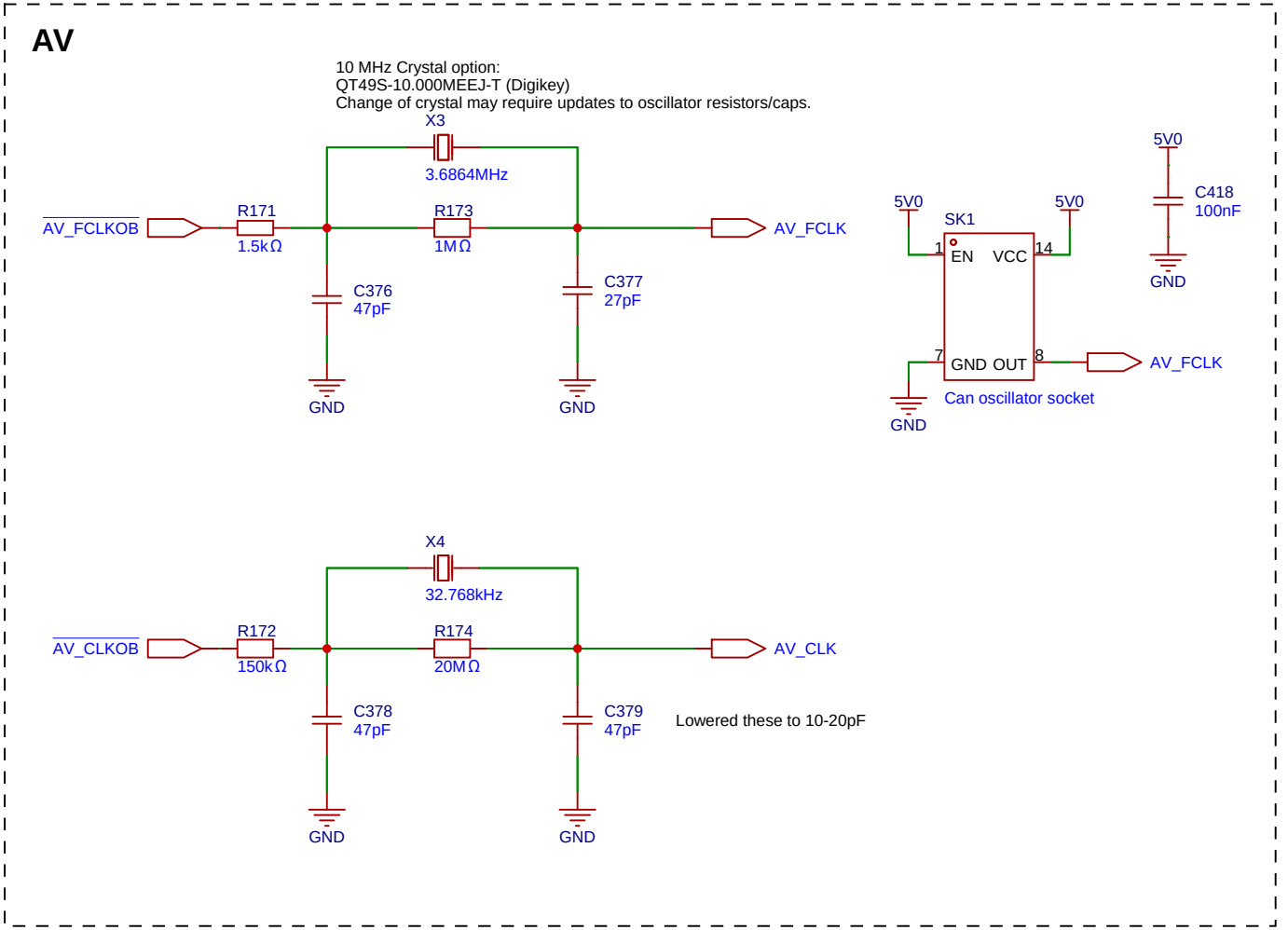


Chassis Ground



Schematic	Schematic1	Create at	2026-01-24
		Update at	2026-02-20
Board	Board1	Page	Power
Drawn		W65C265S AV v0.12	
Reviewed			
		Version	Size	Page 4 Total 9
EasyEDA		V1.0	A4	EasyEDA.com

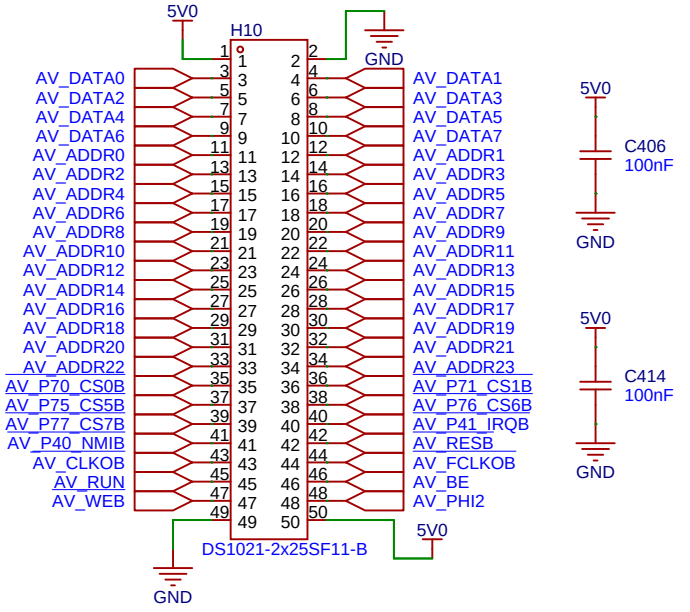
CLOCKS



Schematic	Schematic1	Create at	2026-01-24
		Update at	2026-02-19
Board	Board1	Page	Clocks
Drawn		W65C265S AV v0.12	
Reviewed			
		Version	Size	Page 5 Total 9
EasyEDA		V1.0	A4	EasyEDA.com

EXPANSION

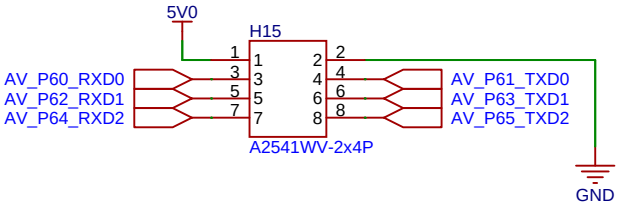
AV XBus265



Used:

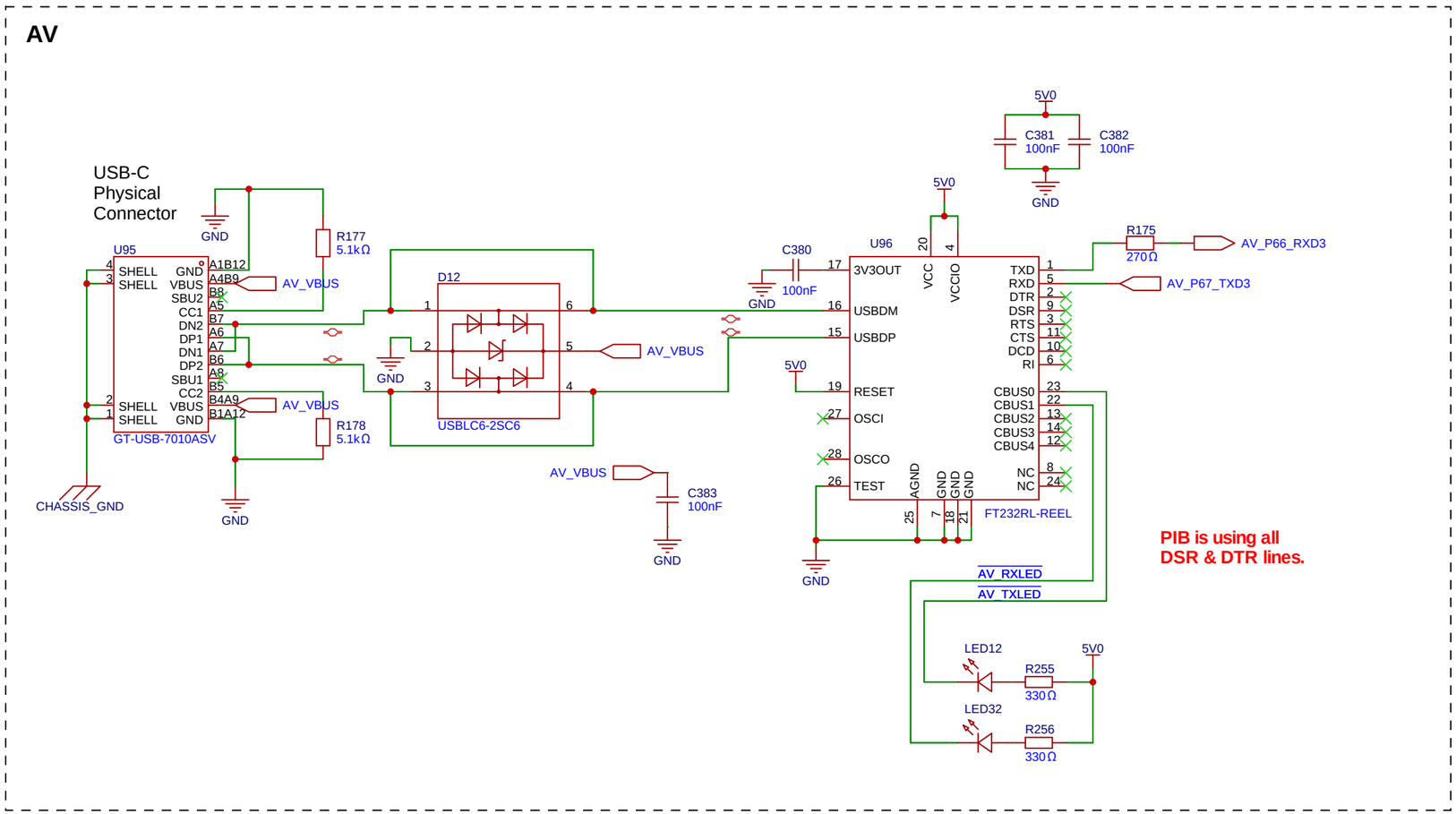
P50:56 - 1602 LCD
P51 - Available

P62 - PS2KBD DATA
P64 - PS2KBD CLK
P66 - RXD3
P67 - TXD3



Schematic	Schematic1	Create at	2026-01-24
		Update at	2026-01-24
Board	Board1	Page	Expansion
Drawn		W65C265S AV v0.12	
Reviewed			
	Version	Size	Page 6 Total 9
EasyEDA	V1.0	A4	EasyEDA.com

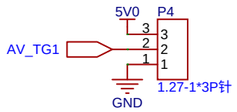
USB SERIAL, PS/2 KEYBOARD

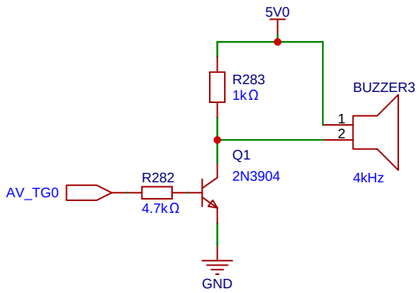


Schematic	Schematic1	Create at	2026-01-24
		Update at	2026-01-24
Board	Board1	Page	Serial
Drawn		W65C265S AV v0.12	
Reviewed			
		Version	Size	Page 7 Total 9
EasyEDA		V1.0	A4	EasyEDA.com

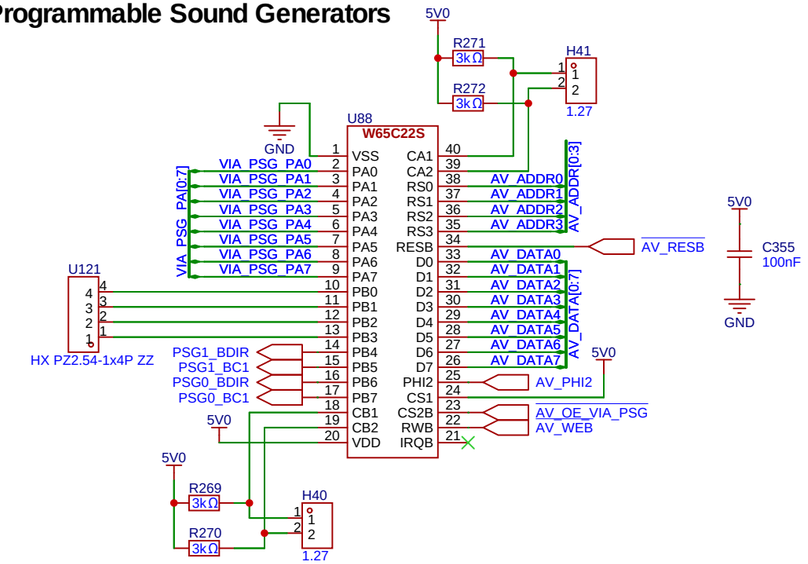
Sound

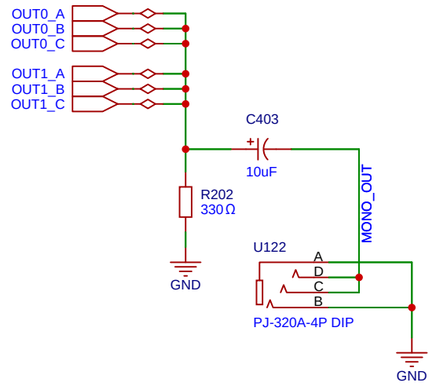
Tone Generators

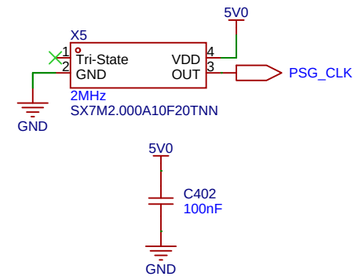




Programmable Sound Generators







Schematic	Schematic1	Create at	2026-01-24
		Update at	2026-01-24
Board	Board1	Page	Sound
Drawn		W65C265S AV v0.12	
Reviewed			
		Version	Size	Page 8 Total 9
EasyEDA		V1.0	A4	EasyEDA.com

VGA 320x240 x1Byte

RRRGGGBB

VGA Signal 320 x 240 @ 60 Hz

General timing
Screen refresh rate60 Hz
Vertical refresh31.46875 kHz
Pixel freq.12.5875 MHz

Horizontal timing (line)
Polarity of horizontal sync pulse is negative.
Scanline partPixelsTime [µs]
Visible area32012.711
Front porch80.318 320 101000000
Sync pulse481.907 328 101001000
Back porch240.953 376 101111000
Whole line40015.889 400 110010000

Vertical timing (frame)
Polarity of vertical sync pulse is negative.
Frame partLinesTime [ms]
Visible area48015.253
Front porch100.318 480 0111100000
Sync pulse20.064 490 0111101010
Back porch331.049 492 0111101100
Whole frame52516.683 525 1000001101

320x240 x1Byte
-3bit Red
-3bit Green
-2bit Blue

IO2_EN OR'd with MEMR#/MEMW# to generate VMEMOEB and VMEMEWB

CS7B is C0:0000 to FF:FFFF
OE3B is E0:0000 to EF:0000
Video MRB/MWB are EA:0000 to EB:FFFF

DECODE

VRAM
0x0A0000-0BFFFF

Video address (for enable)
A19=1
A18=0
A17=1

When A16=0, lower 64K (first two SRAMs)
When A16=1, upper 64K (last two SRAMs)

When A0=0, LO byte
When BHE (!A0) =0, HI byte

LOWER 64K (VID_0)

UIPPER 64K (VID_1)

VSYNC

HSYNC

GAL22V10D PLCC to DIP mapping
(for Digital, using DIP pin numbers)

PLCC	DIP	Name		Name	DIP	PLCC
2	1	I/CLK		VCC	24	28
3	2	I		I/O/Q	23	27
4	3	I		I/O/Q	22	26
5	4	I		I/O/Q	21	25
6	5	I		I/O/Q	20	24
7	6	I		I/O/Q	19	23
9	7	I		I/O/Q	18	21
10	8	I		I/O/Q	17	20
11	9	I		I/O/Q	16	19
12	10	I		I/O/Q	15	18
13	11	I		I/O/Q	14	17
14	12	GND		I	13	16

To connect to MCU edge-interruptible pin.
Interrupt during non-visible time for other processing, such as audio playback.

Schematic	Schematic1	Create at	2026-01-24
		Update at	2026-02-21
Board	Board1	Page	VGA
Drawn		W65C265S AV v0.12	
Reviewed			
		Version	Size	Page 9 Total 9
EasyEDA		V1.0	A4	EasyEDA.com