TO DO

To do:
-Triple-check decode logic for all ICs
-Power jumper to second board
-Pin1 markings on headers
-10pF instead of 47/27pF on crystal circuits, along with 150 instead of 1.5k
-Cuttable connections or 0 ohm resistors for questionable tracks
-Rename both GAL's OEBs from generic to specific and verify throughout
-Triple-check decode ranges and enables
-Verify no components without LCSC equiv. part #
-Print to scale, test fit (especially TFT LCD & ZIFs)
-Review all status LEDs to confirm they are on good pins for showing status
-Verify fill on all layers & rebuild
-External transceivers and/or clock distribution ICs needed? (really long traces)

System Block Diagram

Conventions (e.g., naming)

-Signals for secondary (audio-visual co-processor) MCU prefaced with "AV_"
-Tracks more likely needing bodging on bottom layer
-Horizontal tracks - Top, InnerLower
-Vertical tracks - InnerUpper

Memory Map, Native Decode

W65C265SXB Memory Map				
Start	***End***	***Size***	***Chip Select***	***Description***
(C0)	(FF)	4 MB	CS7B	USER MEMORY (FOR EXPANSION)
(40)	(BF)	8 MB	CS6B	USER MEMORY (FOR EXPANSION)
(00)	(3F)	4 MB	CS5B	MEMORY *See Note 2*
(00)E000 (00)8000	(00)FFFF (00)DEFF	8192 B 24320 B	CS4B	ROM MEMORY (*Note 1*) ROM MEMORY (*Note 1*)
(00)0200	(00)7FFF	32256	CS3B	Cache Memory *See Note 3*
(00)FF00 (00)E000 (00)DF80 (00)DF70 (00)DF50 (00)DF40 (00)DF20 (00)DF00 (00)0000	(00)FFFF (00)FEFF (00)DFBF (00)DF7F (00)DF6F (00)DF4F (00)DF27 (00)DF07 (00)01FF	256 B 7936 B 64 B 16 B 32 B 16 B 8 B 8 B 512 B	CS2B	On Chip Interrupt Vectors On-Chip ROM On-Chip RAM On-Chip Comm. Registers On-Chip Timer Registers On-Chip Control Registers On-Chip IO Registers On-Chip IO Registers On-Chip RAM
(00)DFC0	0xDFFF	64 B	CS1B	External Chip Select 1 (P71)
(00)DF00	0xDF1F	32 B	CS0B	External Chip Select 0 (P70) *See Note 4*

I/O Devices: See GAL Decode

Extended Flash 512 KB

Extended SRAM 2 MB (01) (02)
Dual-port SRAM (03)

Primary Flash 128 KB (four 32 KB sections)

SRAM 32 KB

Note 1 - When on-chip 8K bytes of ROM are enabled:
a.) Addresses (00)E000-FFFF will not appear in CS4B chip select decode.
b.) On Chip addresses (00)DF00-DFFF never appear in CS4B or CS5B chip select decode.

Note 2 - When on-chip ROM, CS3B and/or CS4B are enabled:
a.) CS5B decode is reduced by the addresses used by same.
b.) CS0B and CS1B address space never appears in CS2B, CS4B or CS5B decoded space.

Note 3 - When SSCR2 is "0" (internal RAM), then CS3B is active for addresses (00)0200-7FFF. When SSCR2 is "1" (external RAM), then CS3B is active for addresses (00)0000-7FFF.

Note 4 - CS0B is inactive when 00DF00-00DF07 are used for internal I/O register select (BCR0=0). When (BCR0=1) external memory bus is enabled CS0B is active for addresses 00DF00-00DF1F.

Extended Decode (GAL)

C0:0000 to FF:FFFF CS7B

1100:0000000000000000000 to
1111:1111111111111111111
(range: top two bits are 11)

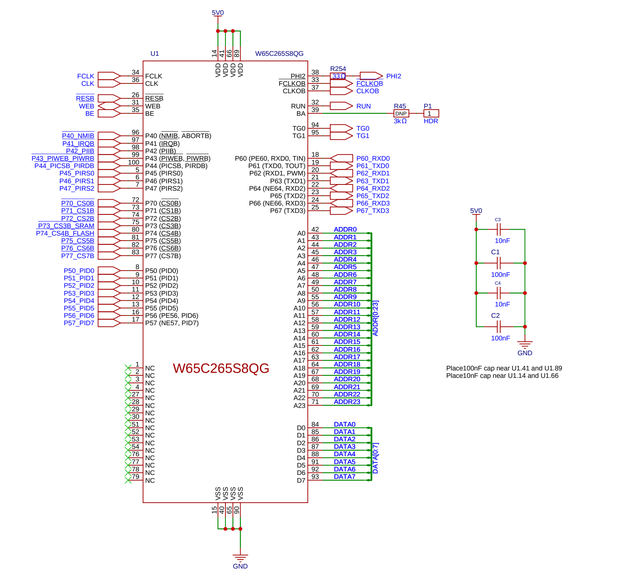
1100: VIA0 C0:xxxx C0:0000 to C0:000F
1101: VIA1 D0:xxxx D0:0000 to D0:000F
1110: VIA2 E0:xxxx E0:0000 to E0:000F
1111: VIA3 F0:xxxx F0:0000 to F0:000F

**re-map I/O by bringing in additional address lines
see Overview page for details

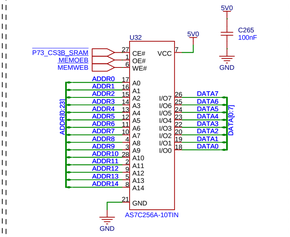
Schematic	Schematic1	Create at	2026-01-15
		Update at	2026-01-16
Board	Board1	Page	Overview
Drawn		W65C265S Primary v0.10	
Reviewed			
		Version	Size	Page 1 Total 10
EasyEDA		V1.0	A4	EasyEDA.com

MCU (Primary)

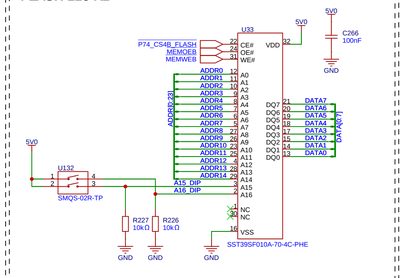
65265 MCU



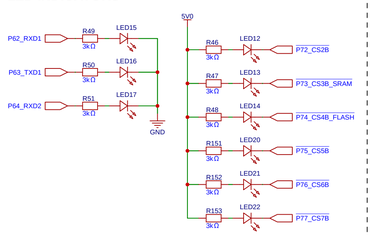
STATIC RAM 32 KB



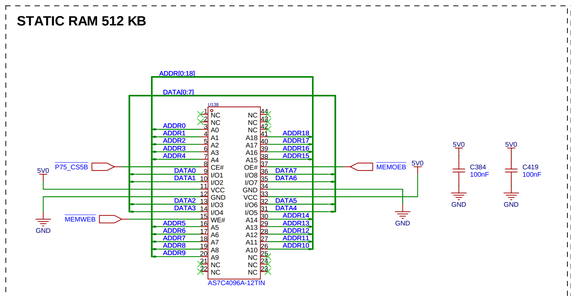
FLASH 128 KB



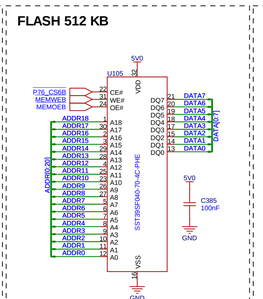
LED INDICATORS



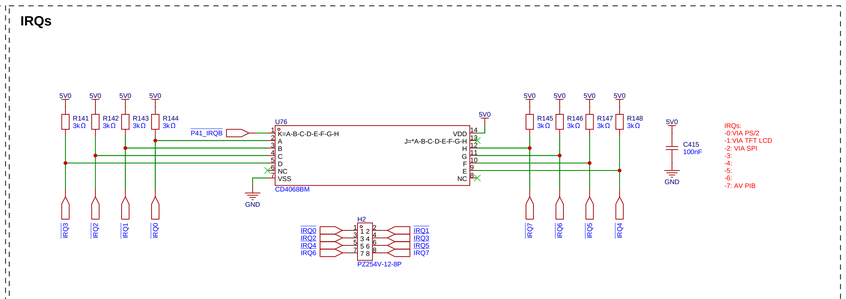
STATIC RAM 512 KB



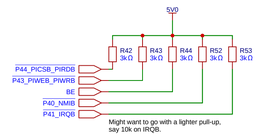
FLASH 512 KB



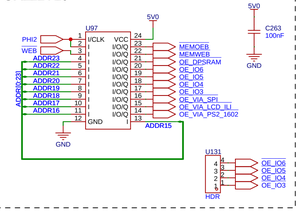
IRQs

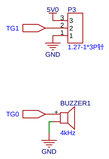


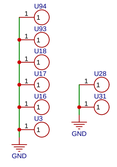
PULL-UPS



GAL22V10





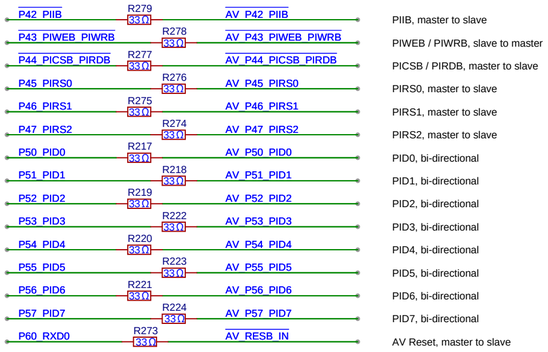


Schematic	Schematic1	Create at	2026-01-15
		Update at	2026-01-19
Board	Board1	Page	MCU Primary
Drawn		W65C265S Primary v0.10	
Reviewed			
		Version	Size / Page 2 Total 10
EasyEDA		V1.0	A4 / EasyEDA.com

MCU (AV)

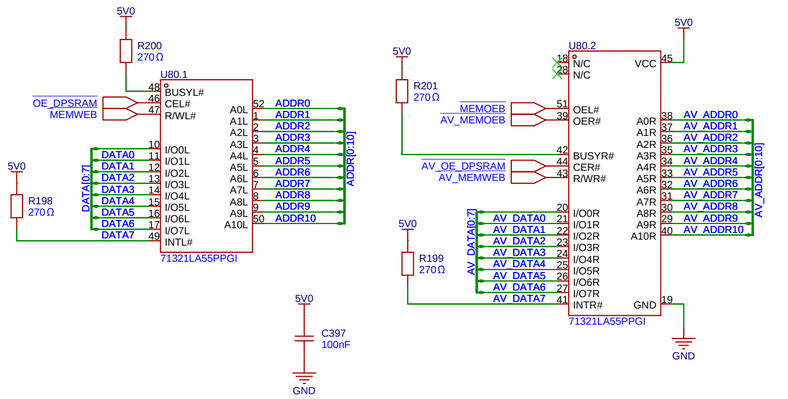
INTER-MCU

Inter-MCU PIB Connections

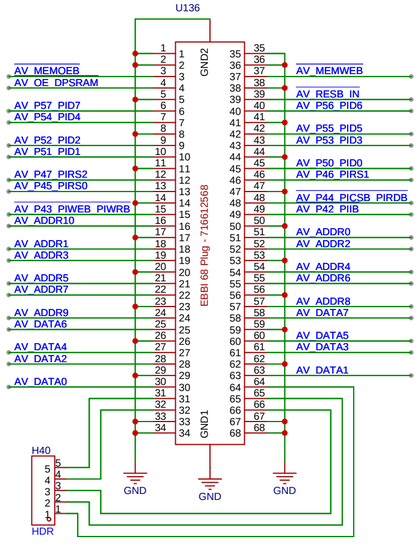


PIIB, master to slave
PIWEB / PIWRB, slave to master
PICSB / PIRDB, master to slave
PIRS0, master to slave
PIRS1, master to slave
PIRS2, master to slave
PID0, bi-directional
PID1, bi-directional
PID2, bi-directional
PID3, bi-directional
PID4, bi-directional
PID5, bi-directional
PID6, bi-directional
PID7, bi-directional
AV Reset, master to slave

DUAL-PORT STATIC RAM 2 KB

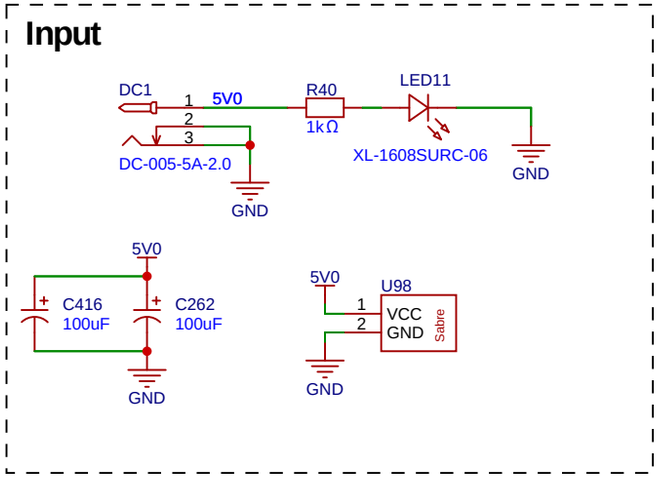


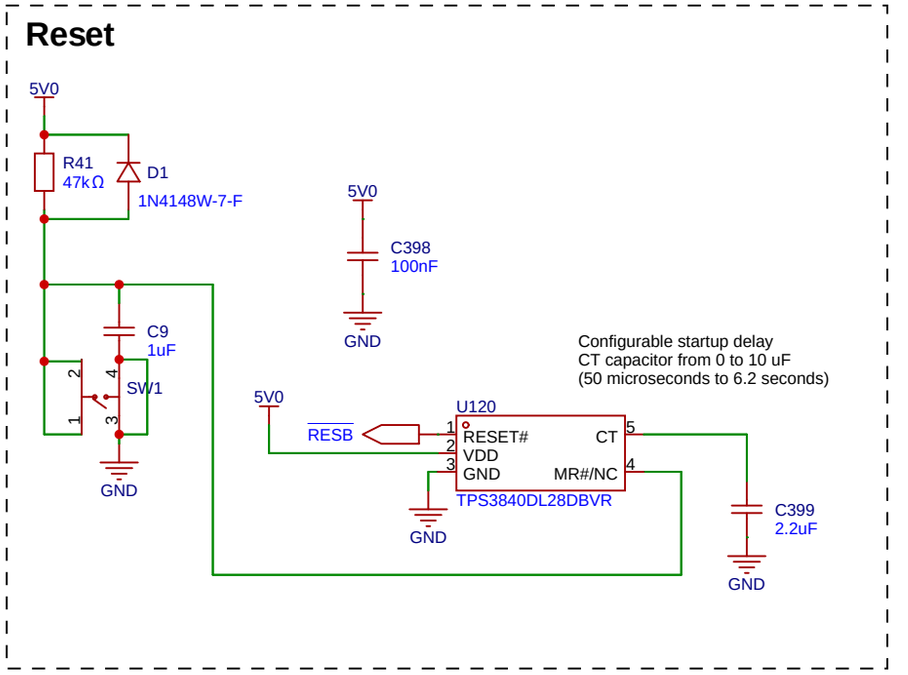
U136

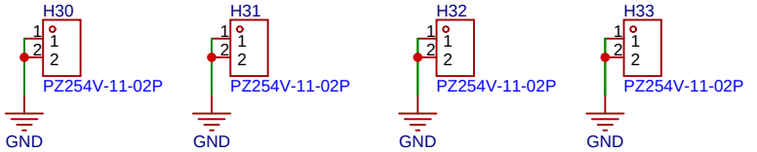


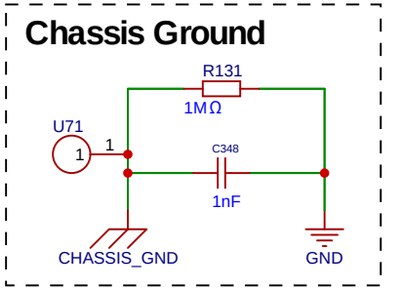
Schematic	Schematic1	Create at	2026-01-15
		Update at	2026-01-19
Board	Board1	Page	Interconnect
Drawn		W65C265S Primary v0.10	
Reviewed			
		Version	Size / Page 3 Total 10
EasyEDA	V1.0	A4	EasyEDA.com

POWER







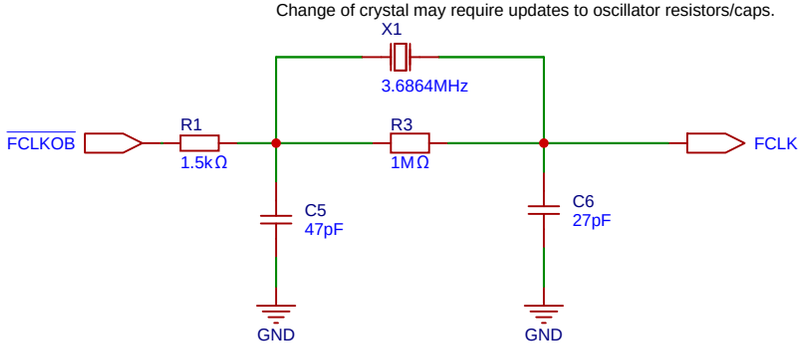


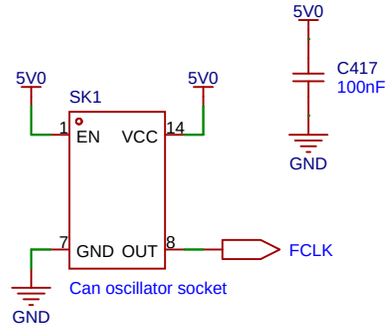
Schematic	Schematic1	Create at	2026-01-15
		Update at	2026-01-15
Board	Board1	Page	Power
Drawn		W65C265S Primary v0.10	
Reviewed			
		Version	Size	Page 4 Total 10
EasyEDA		V1.0	A4	EasyEDA.com

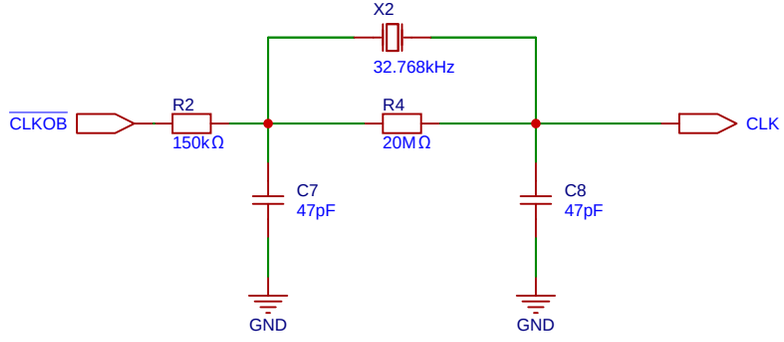
CLOCKS

PRIMARY

10 MHz Crystal option:
QT49S-10.000MEEJ-T (Digikey)
Change of crystal may require updates to oscillator resistors/caps.







Schematic	Schematic1	Create at	2026-01-15
		Update at	2026-01-19
Board	Board1	Page	Clocks
Drawn		W65C265S Primary v0.10	
Reviewed			
		Version	Size	Page 5 Total 10
EasyEDA		V1.0	A4	EasyEDA.com

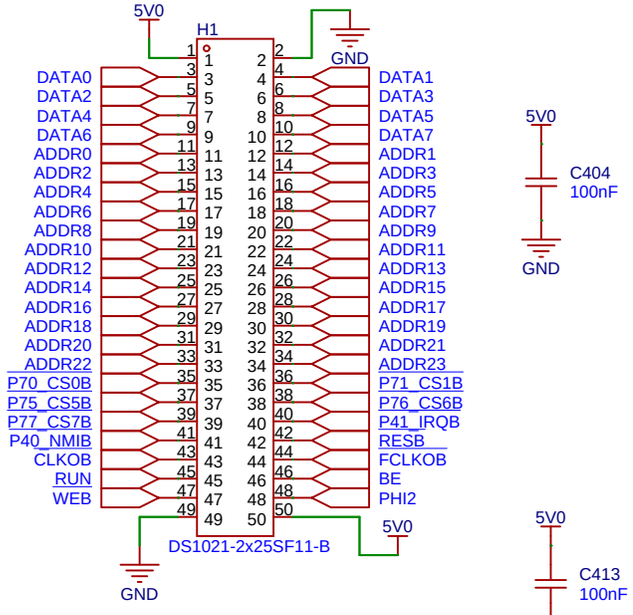
EXPANSION

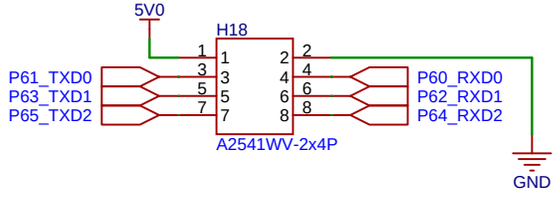
Used:

P50:56 - 1602 LCD
P51 - Available

P62 - PS2KBD DATA
P64 - PS2KBD CLK
P66 - RXD3
P67 - TXD3

Primary XBus265

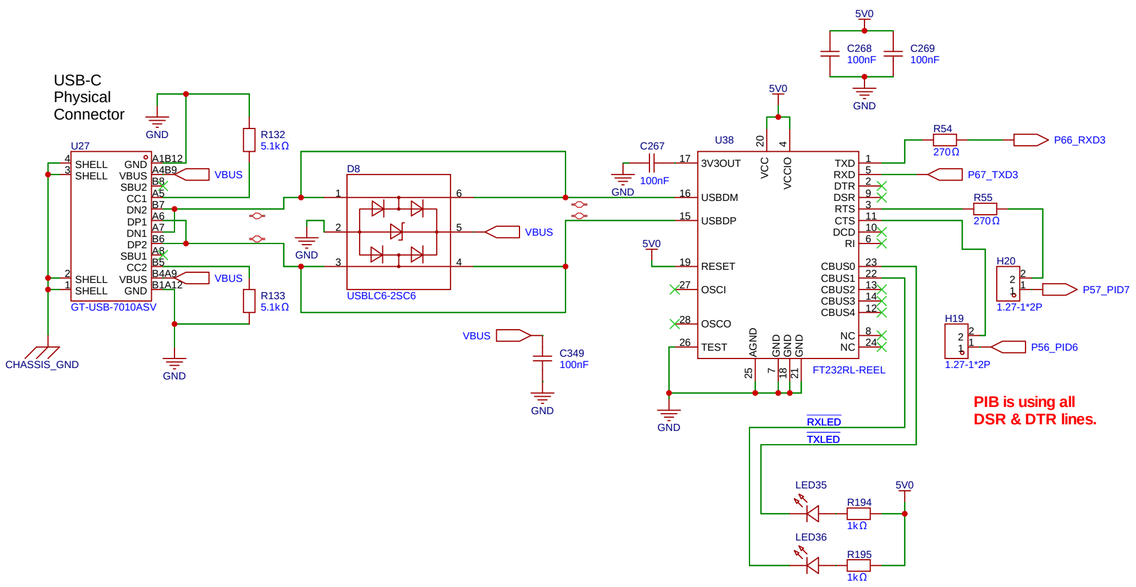




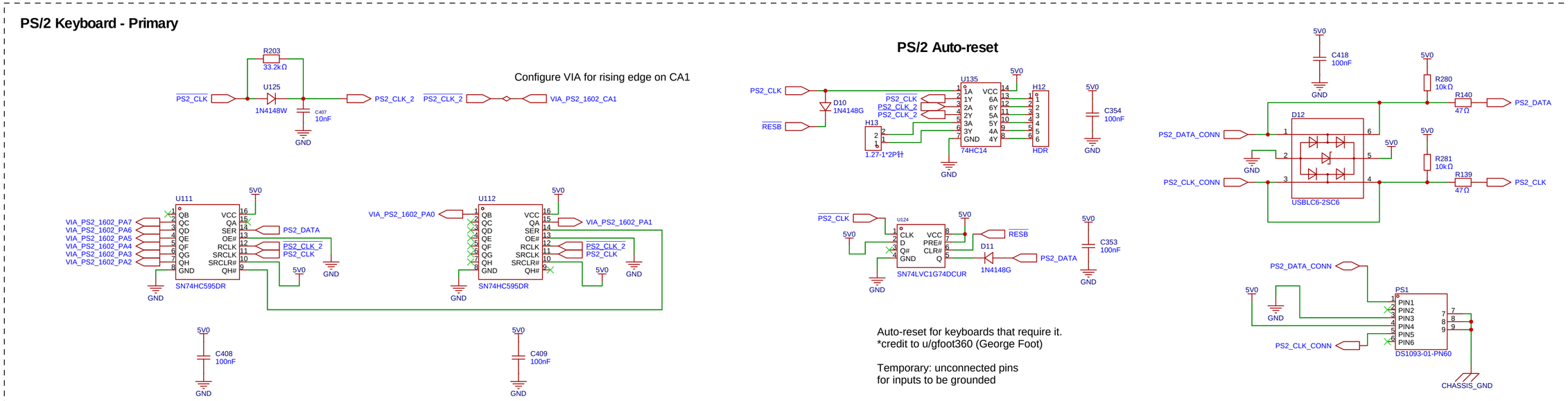
Schematic	Schematic1	Create at	2026-01-15
		Update at	2026-01-19
Board	Board1	Page	Expansion
Drawn		W65C265S Primary v0.10	
Reviewed			
		Version	Size	Page 6 Total 10
EasyEDA		V1.0	A4	EasyEDA.com

USB SERIAL, PS/2 KEYBOARD

Primary

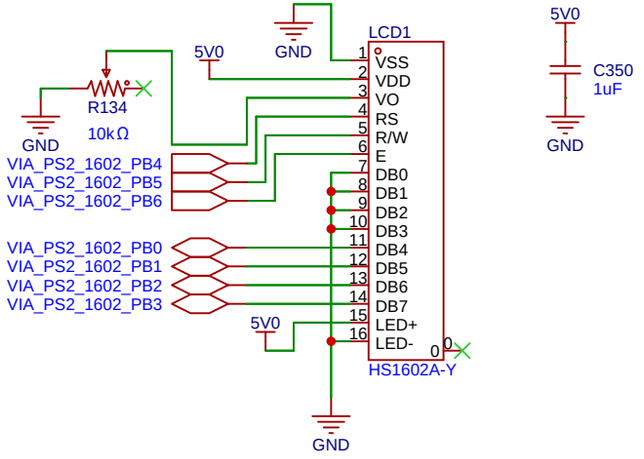


PS/2 Keyboard - Primary



Schematic	Schematic1	Create at	2026-01-15
		Update at	2026-01-19
Board	Board1	Page	Serial & PS2
Drawn		W65C265S Primary v0.10	
Reviewed			
		Version	Size	Page 7 Total 10
EasyEDA		V1.0	A4	EasyEDA.com

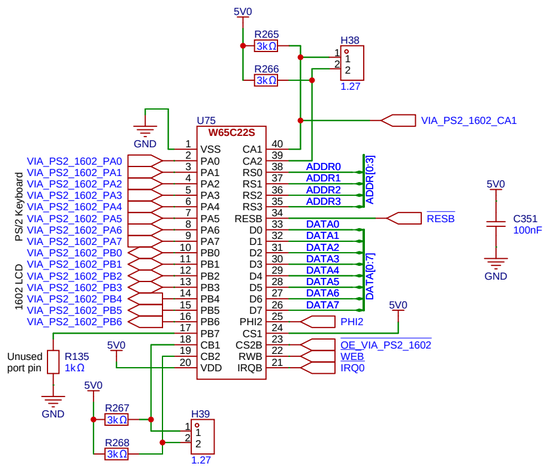
LCD 1602



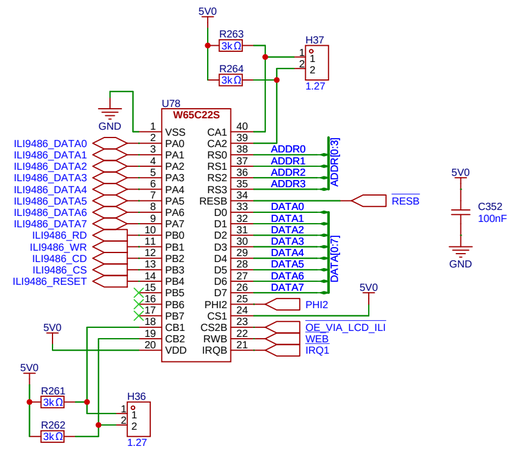
Schematic	Schematic1	Create at	2026-01-15
		Update at	2026-01-15
Board	Board1	Page	LCD_1602
Drawn		W65C265S Primary v0.10	
Reviewed			
	Version	Size	Page 8 Total 10
EasyEDA	V1.0	A4	EasyEDA.com

VIAs

PS/2 Keyboard, 1602 LCD



TFT LCD (ILI)

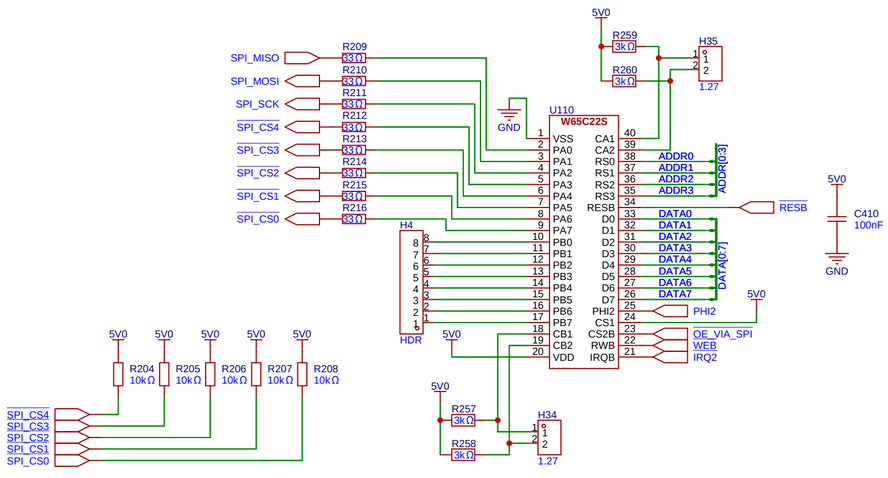


C0:0000 to FF:FFFF CS7B

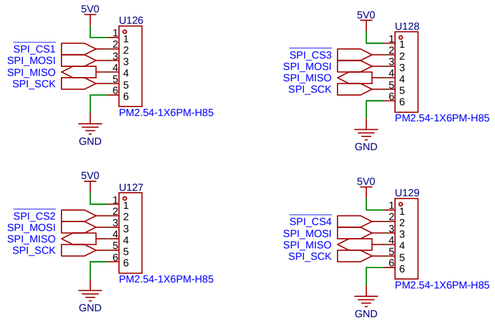
1100:0000000000000000000 to
1111:1111111111111111111
(range: top two bits are 11)

1100: VIA0 C0:xxxx C0:0000 to C0:000F
1101: VIA1 D0:xxxx D0:0000 to D0:000F
1110: VIA2 E0:xxxx E0:0000 to E0:000F
1111: VIA3 F0:xxxx F0:0000 to F0:000F

SPI, Expansion



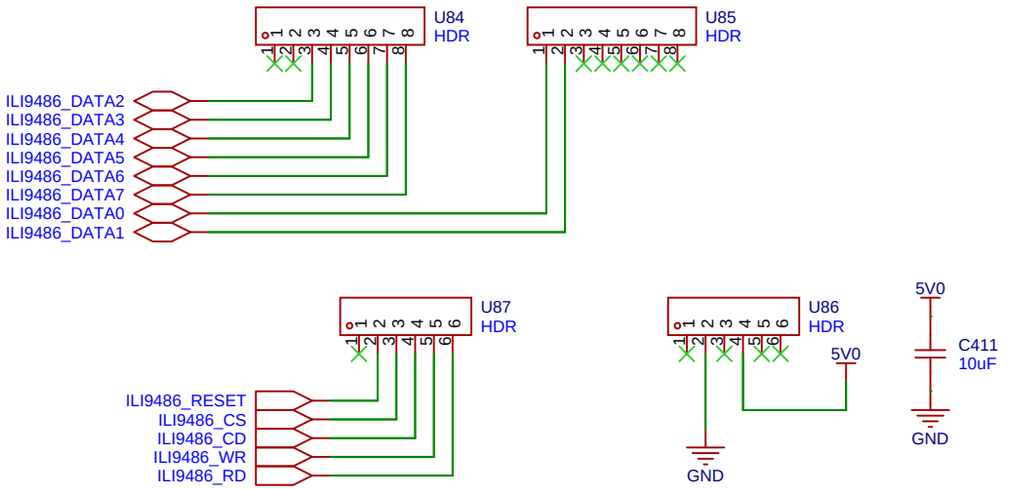
SPI CS:
-0:RTC
-1:?
-2:?
-3:?
-4:?



Schematic	Schematic1	Create at	2026-01-15
		Update at	2026-01-19
Board	Board1	Page	VIAs
Drawn		W65C265S Primary v0.10	
Reviewed			
		Version	Size	Page 9 Total 10
EasyEDA		V1.0	A4	EasyEDA.com

LCD - ILI

Arduino-style header for DIYables TFT LCD



Schematic	Schematic1	Create at	2026-01-15
		Update at	2026-01-15
Board	Board1	Page	LCD_ILI
Drawn		W65C265S Primary v0.10	
Reviewed			
		Version	Size	Page 10 Total 10
EasyEDA		V1.0	A4	EasyEDA.com