Understanding Energy Performance of Containers Deployment on SoC-Based post-Moore Platforms

Pablo Josue Rojas Yepes
Carlos Jaime Barrios Hernandez
Luiz Angelo Steffenel

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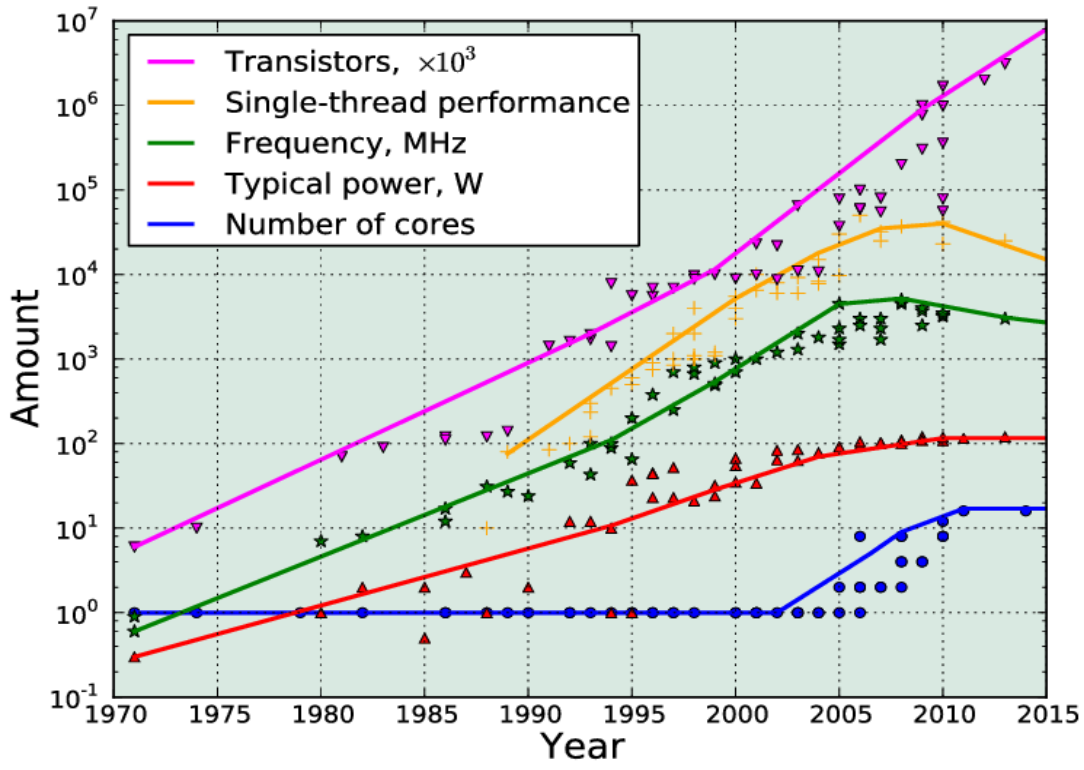
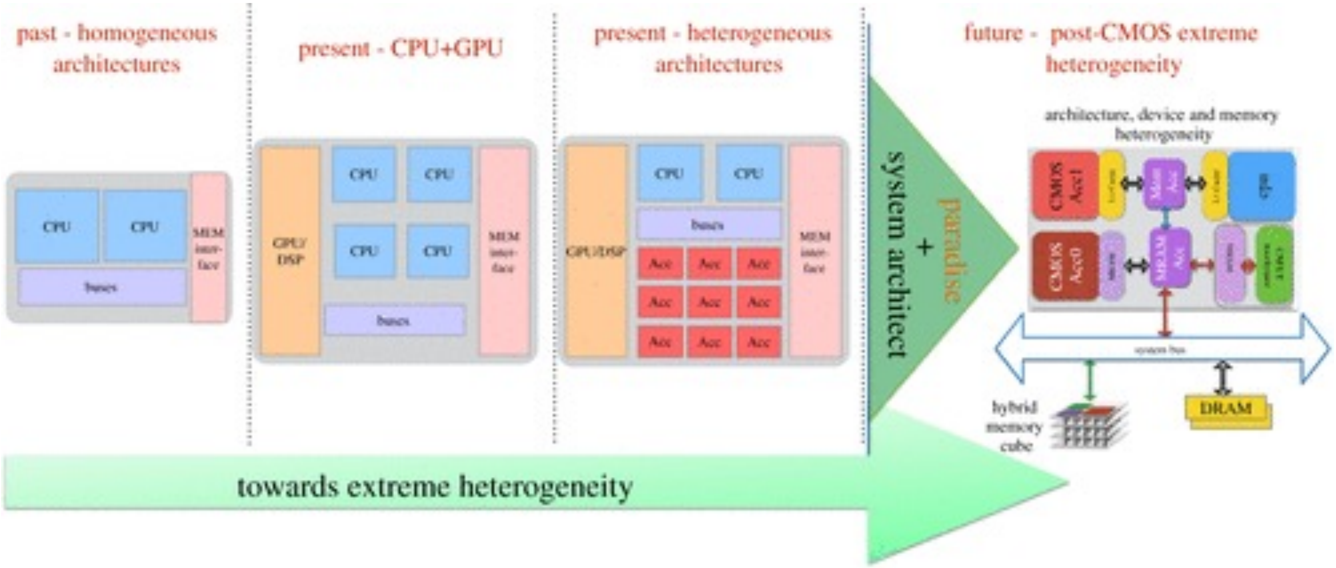
Power Consumption and Computational Capabilities



Evolution of Computational Capabilities . Vitaly Petrov, Dmitri Moltchanov, Maria Komar, Alexander Antonov, Pavel Kustarev, Shaloo Rakheja, and Yevgeni Koucheryavy. 2017. Terahertz Band Intra-Chip Communications: Can Wireless Links Scale Modern x86 CPUs? IEEE Access 5 (2017), 6095–6109. https://doi.org/10.1109/ACCESS.2017.2689077

- Expectation
  - Increase the frequency by core without affecting power consumption.
  - Die size reduction
  - Growth of the computational performance follows Moore's Law.
- Reality
  - To meet expectations, it has been necessary new computational paradigms, including architecture, organization, and program modeling (Post Moore Architectures)

The Post Moore Architecture Concept

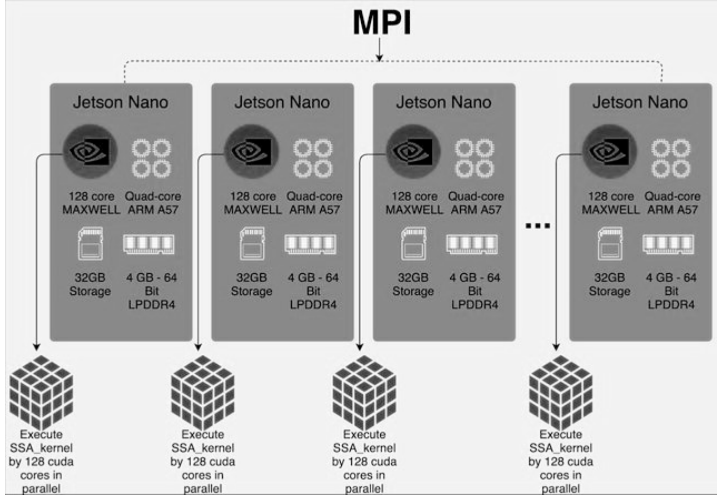


Architectural specialization and extreme heterogeneity are anticipated to be the near-term response to the end of classical technology scaling. Figure courtesy of D. Vasudevan from LBNL. (https://royalsocietypublishing.org/doi/10.1098/rsta.2019.0061)

- Accepted Features
  - Heterogenous Architectures
  - Parallelism
- Discussion Features
  - New Program Models
  - Specialized and Different Scale Systems (Hardware/Software)
  - Energy Efficient (or New Concept of Computer Efficiency as Watt per Instruction).

Milliclusters: A post-Moore implementation

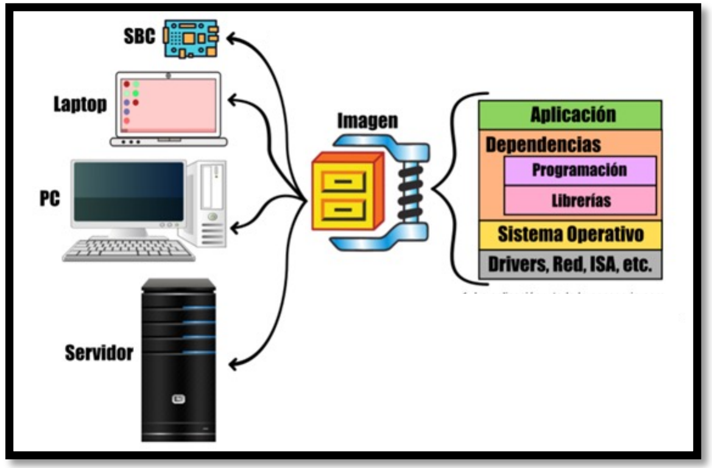
A SC3UIS HPC@Pocket Milliclusters (www.sc3.uis.edu.co)



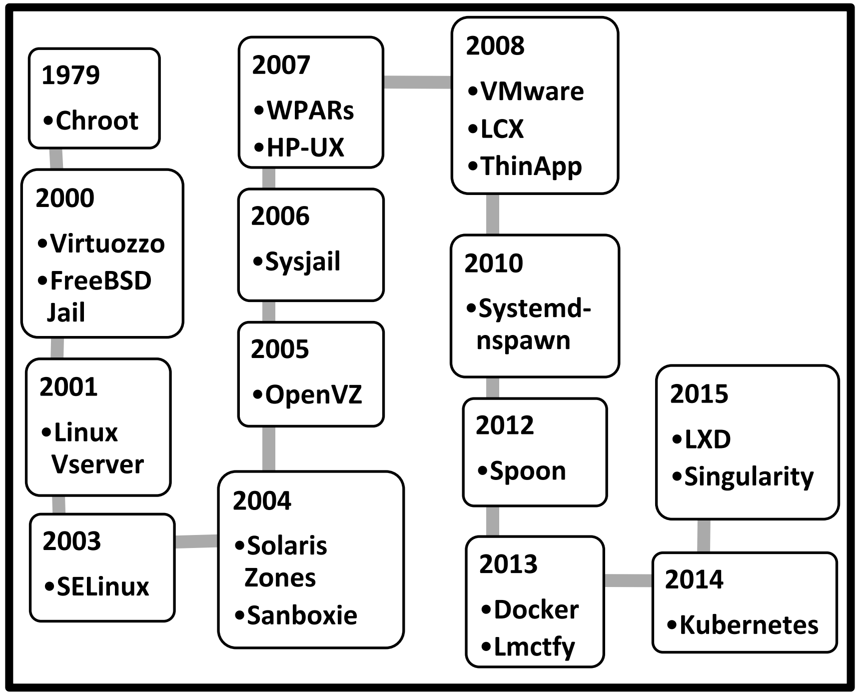
Pilsung Kang and Sungmin Lim. 2020. A Taste of Scientific Computing on the GPU-Accelerated Edge Device. IEEE Access 8 (01 2020), 208337–208347. https://doi.org/10.1109/ACCESS.2020.3038714

- Low-power computational infrastructures to improve energy efficiency and to support HPC needs.
  - IoT or Distributed Systems
  - Testbed platforms
  - Low-Cost HPC@Pocket Platforms
- Replication of classical HPC clusters (in scale):
  - Support hybrid model of execution (i.e. MPI/CUDA or MPI/OpenMP)
  - Support many deployment contexts
    - Virtualization or Containerization
    - Package Management (i.e. nix)
  - Support typical data transfers and protocols
  - Support diversity in applications
- Commercially accessible components
  - NVIDIA Jetson Nano Kits
  - Raspberry Pi
  - Many SoC (Parallela, FPGAs, etc.)

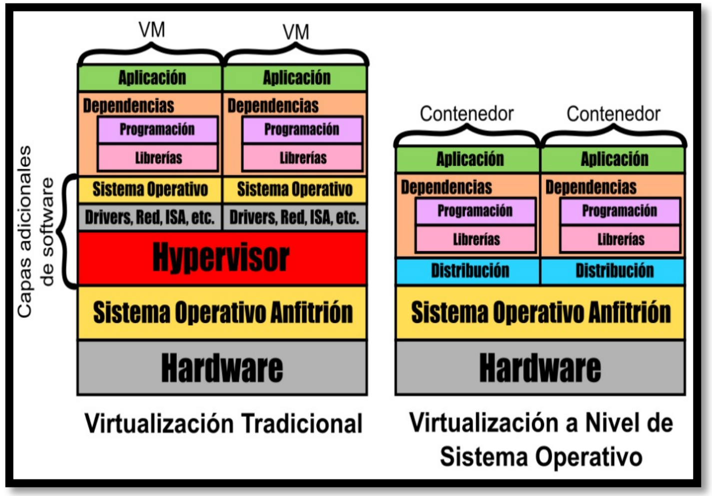
Containers and Virtualisation Deployment



Virtualization



Virtualization Evolution



Containers and Virtualization

***Figures in Spanish are on purpose because no matter what you want to implant (and where).**

ACDC Methodology: Rojas Yepes, P.J., Barrios Hernandez, C.J., Steffenel, L.A. (2022). A Methodology for Evaluating the Energy Efficiency of Post-Moore Architectures. In: Gitler, I., Barrios Hernández, C.J., Meneses, E. (eds) High Performance Computing. CARLA 2021. Communications in Computer and Information Science, vol 1540. Springer, Cham. https://doi.org/10.1007/978-3-031-04209-6_4

Test Considerations

1. Deployment Mechanisms
   - Native
   - Containers
     - Docker
     - Singularity
2. Evaluation Mechanisms
     - Energy Efficiency
       - ***Cfloat, Correlate, Prime,* Matrixprod**
3. Test Workflow

Features	Docker	Singularity
Lite Installation	Yes	Yes
HPC Support	Yes	Yes
Type of Software	Tool	Program
Using Cgroups	Yes	No
Licence	Open Source	Open Source
Security	Root daemon	SUID/UserNS
MPI support	Yes	Yes
GPU support	Yes	Yes
Primary Focus	Traditional App	Scient Workloads
Portability	Good	Excellent
Scalability	Adequate	Adequate

Docker vs. Singularity Features

Measurement of Energy Consumed

Energy Consumption and Efficiency

$$\frac{W}{s}$$

$$\frac{Ops/_{s}}{W/_{s}} = \frac{Ops}{W}$$

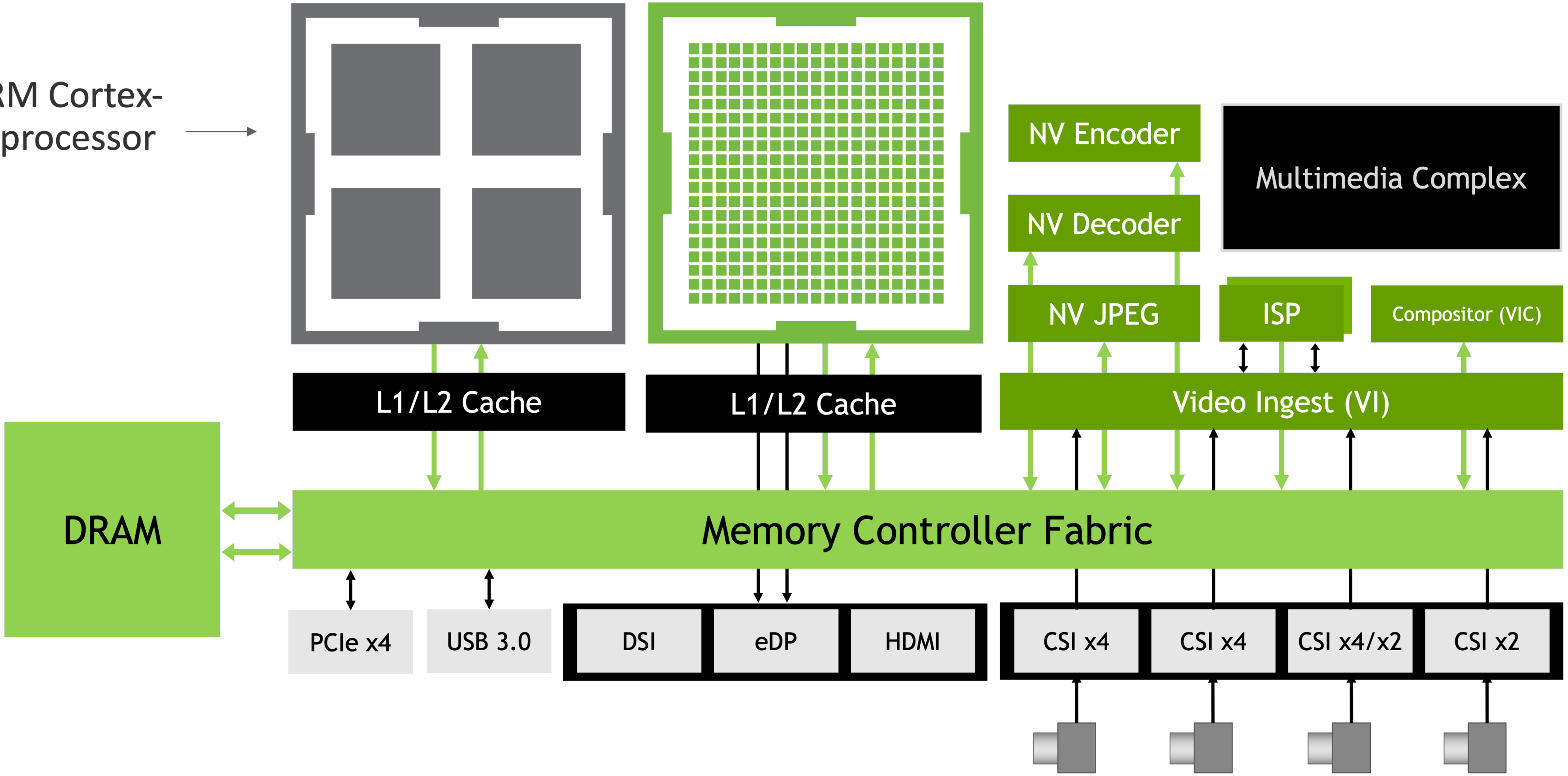
W= watts
Ops = operations
S = seconds

Workloads

- **Cfloat** is 1000 iterations of a mix of floating-point complex operations.
- **Correlate** performs 16384 × 1024 correlation of random doubles.
- **Union** performs integer arithmetic on a mix of bit fields in a C union.
- **Hyperbolic** compute sinh(θ) × cosh(θ) + sinh(2θ) + cosh(3θ) for float, double and long double hyperbolic sine and cosine functions where θ = 0 to 2π in 1500 steps.
- **Prime** finds all the primes in the range 1 to 1'000,000 using a slightly optimized brute force naïve trial division search.
- **Matrixprod** is a matrix product of two 128 × 128 matrices of double floats.

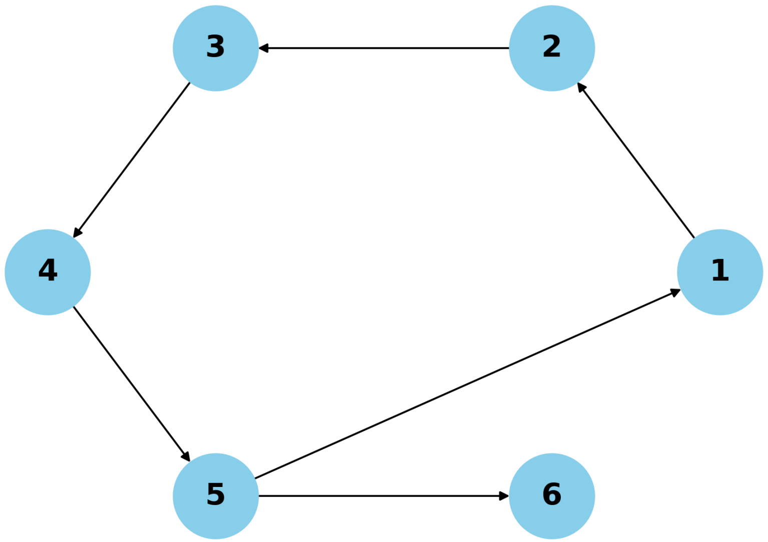
Testbed Device: NVIDIA® Jetson Nano

Quad-core ARM Cortex-A57 MPCore processor



Cortesy of NVIDIA

Tests Workflow



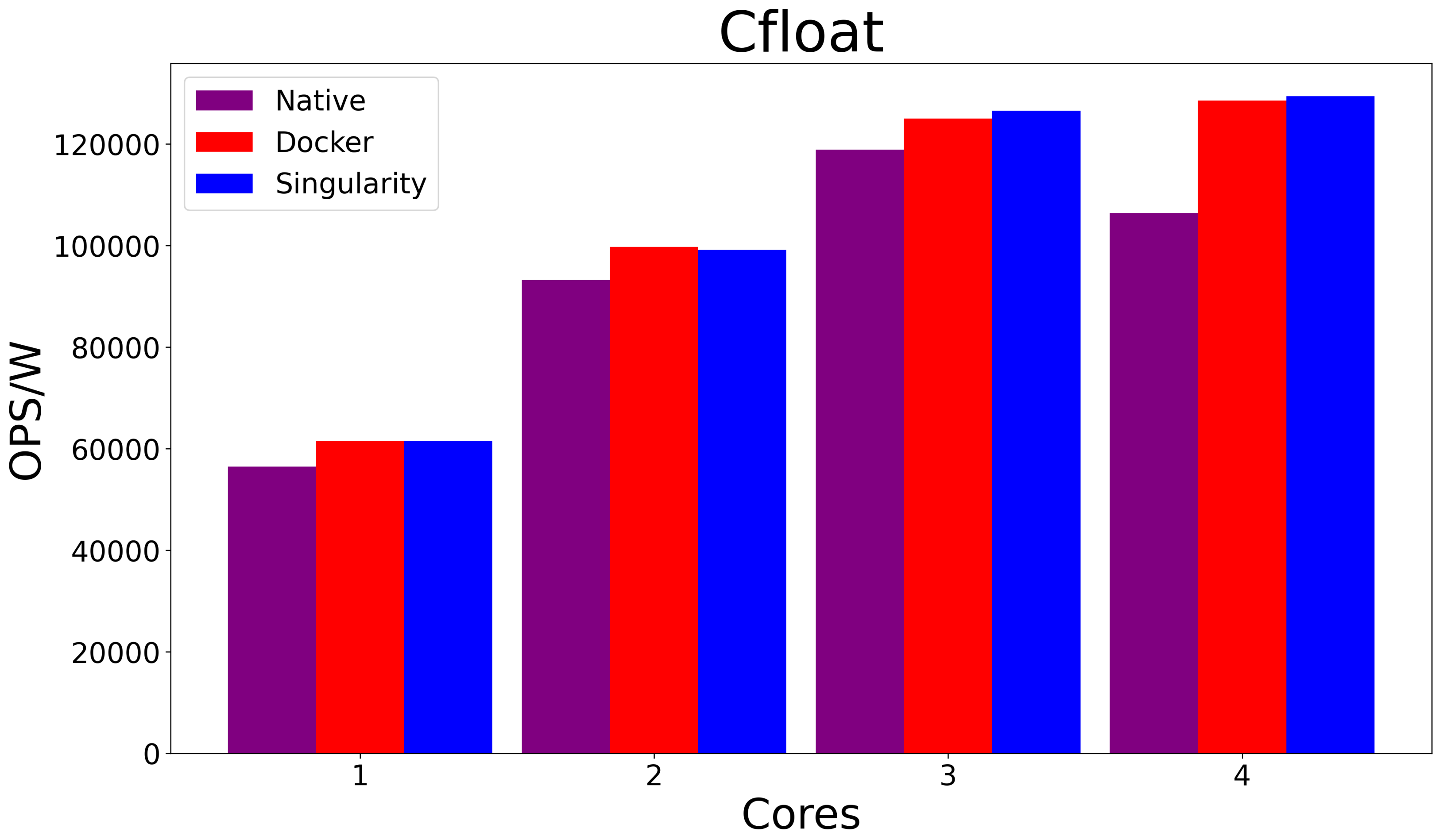
Following *ACDC Methodology: Rojas Yepes, P.J., Barrios Hernandez, C.J., Steffenel, L.A. (2022). A Methodology for Evaluating the Energy Efficiency of Post-Moore Architectures. In: Gitler, I., Barrios Hernández, C.J., Meneses, E. (eds) High Performance Computing. CARLA 2021. Communications in Computer and Information Science, vol 1540. Springer, Cham. https://doi.org/10.1007/978-3-031-04209-6_4*

1. Configure the different test requirements: modify values such as the duration time, the percentage of test load, increase the MHz or consumption patterns, etc.
2. Configure the energy consumption monitor: find a way to capture the consumption data.
3. Start the energy consumption monitoring and launch the test.
4. Store and label test results: the label should bear the device's name, the test carried out, the resources used, etc.
5. Repeat the test or start a new trial: This step is a fork. Therefore, it is good to repeat the test several times to identify patterns in the devices or to make modifications to expose problems such as bottlenecks, memory saturation, etc.
6. Group the results and generate the graphs of the tests: based on the labels, the data is processed to create the charts.

Results

Deployment Methods

Cfloat Tests



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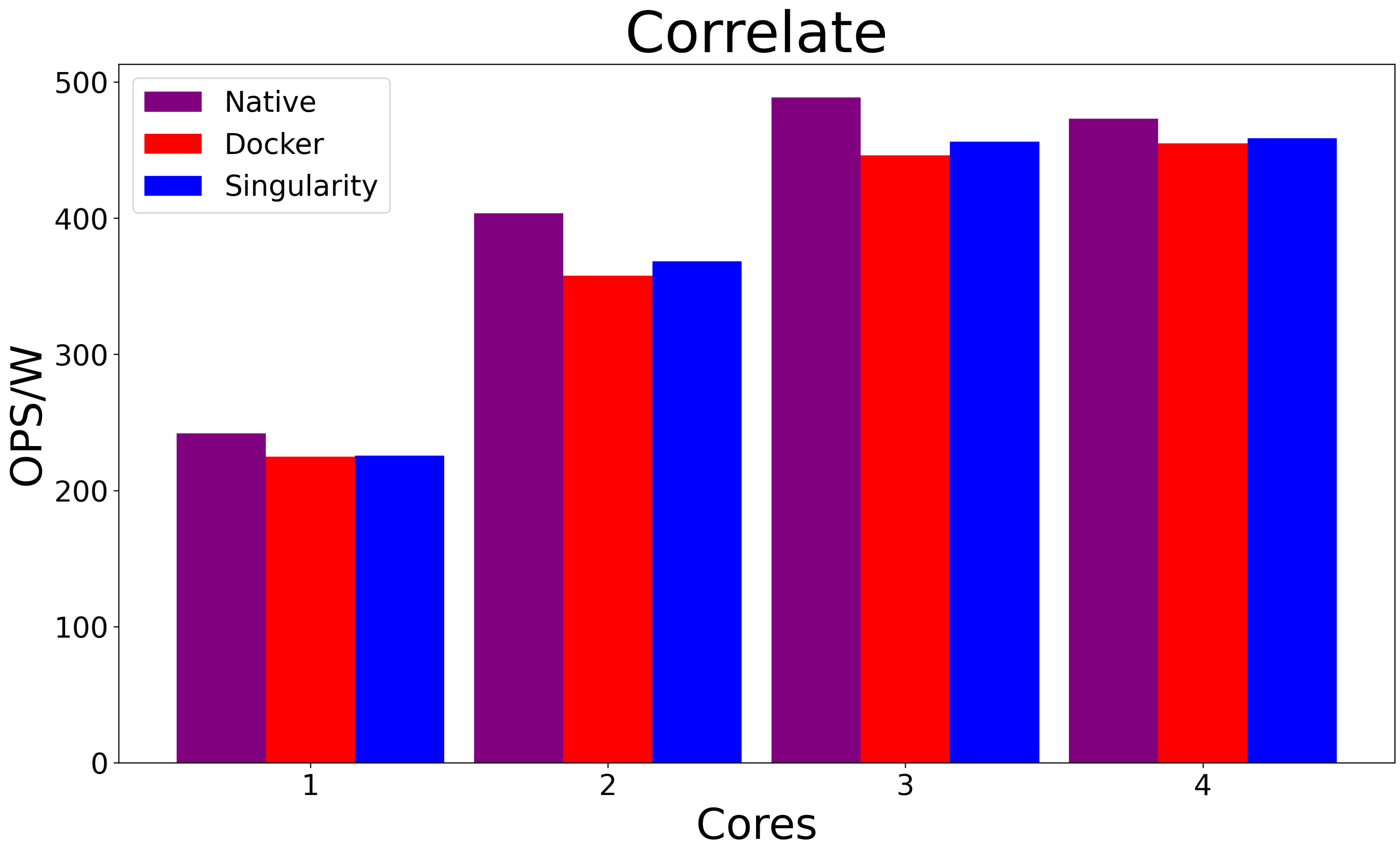
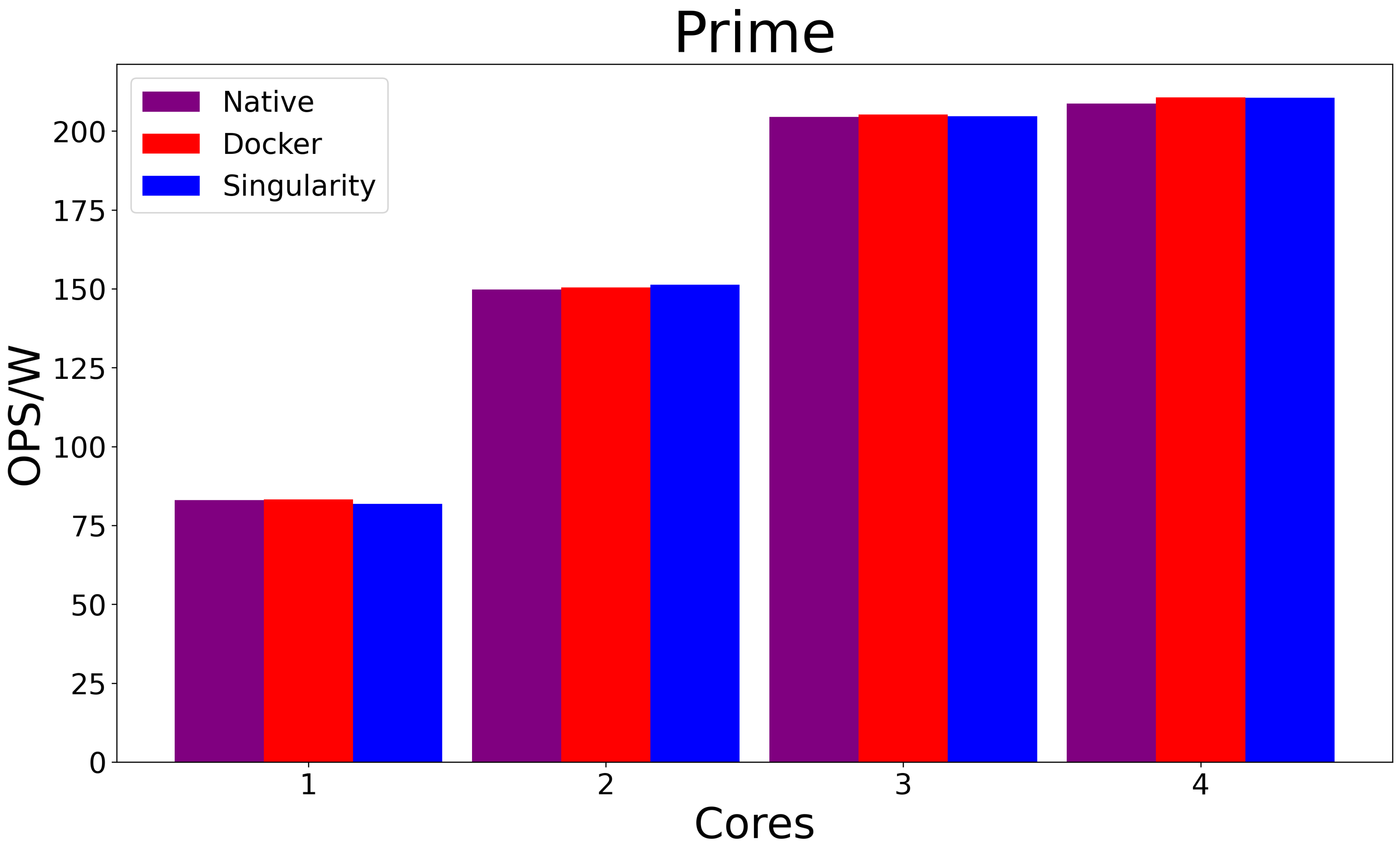
Correlate Tests



Prime Tests



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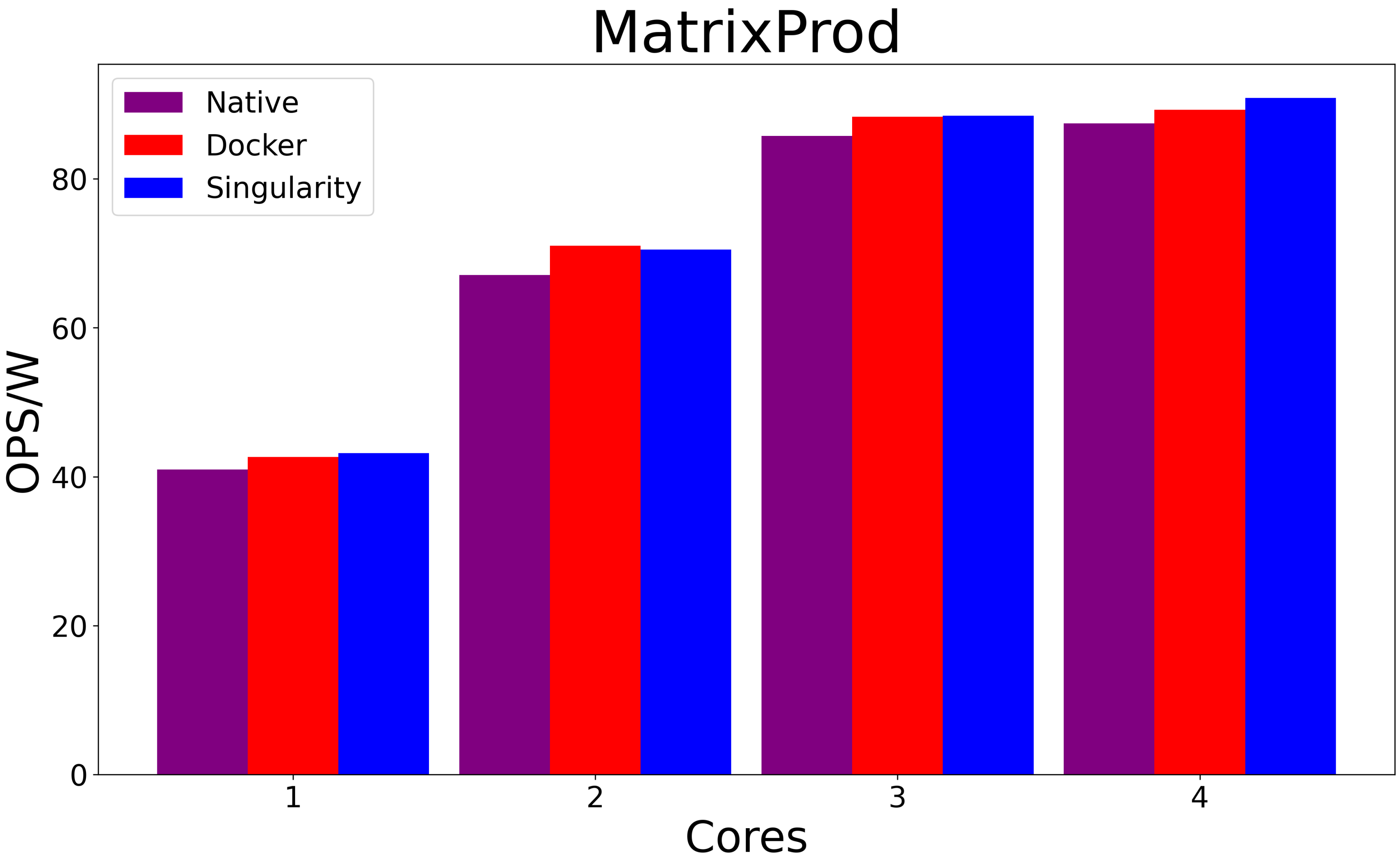
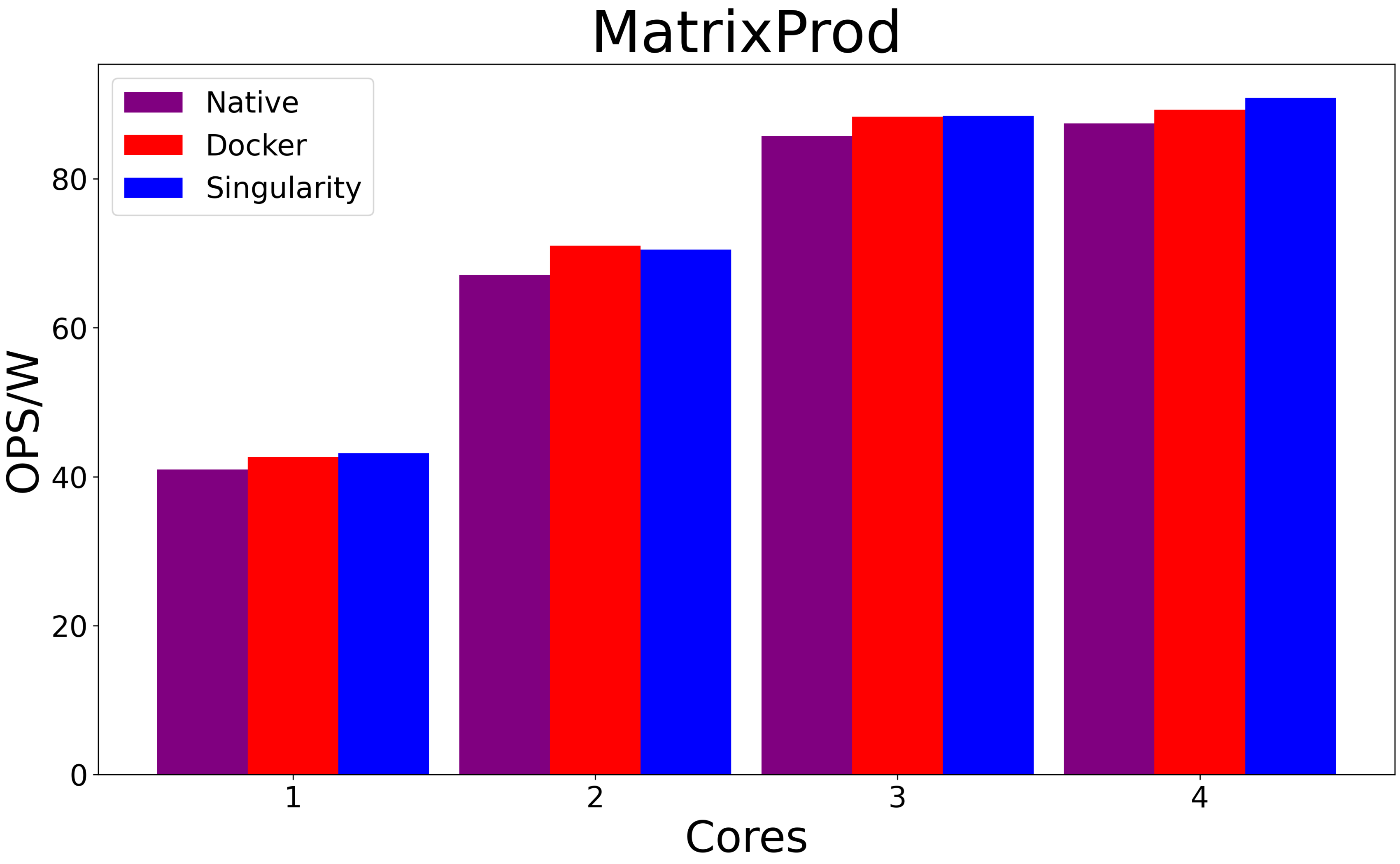
MatrixProd Tests

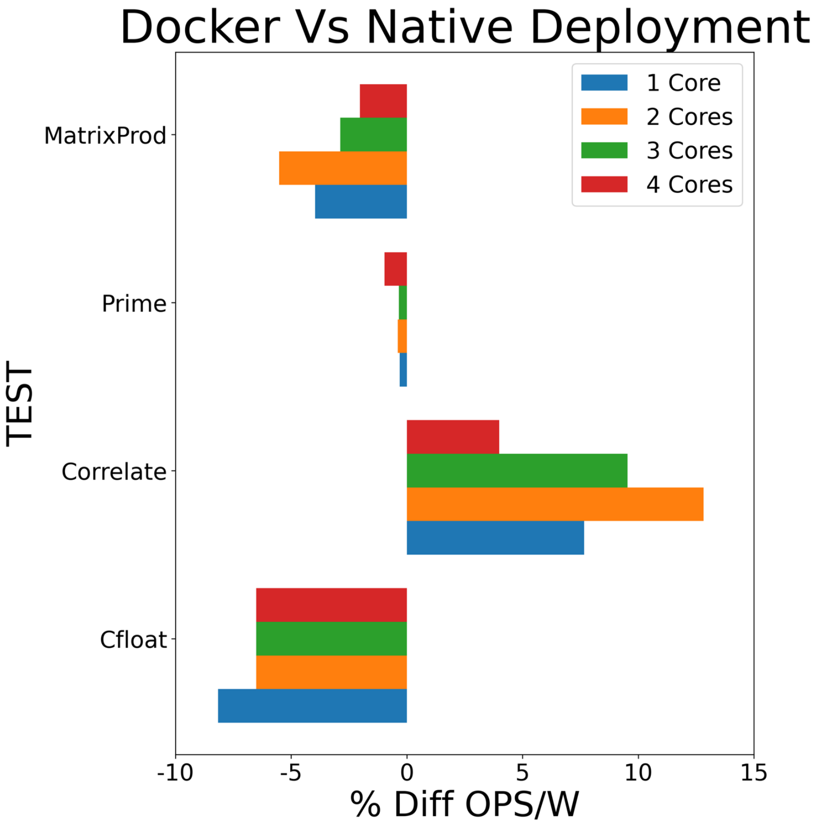


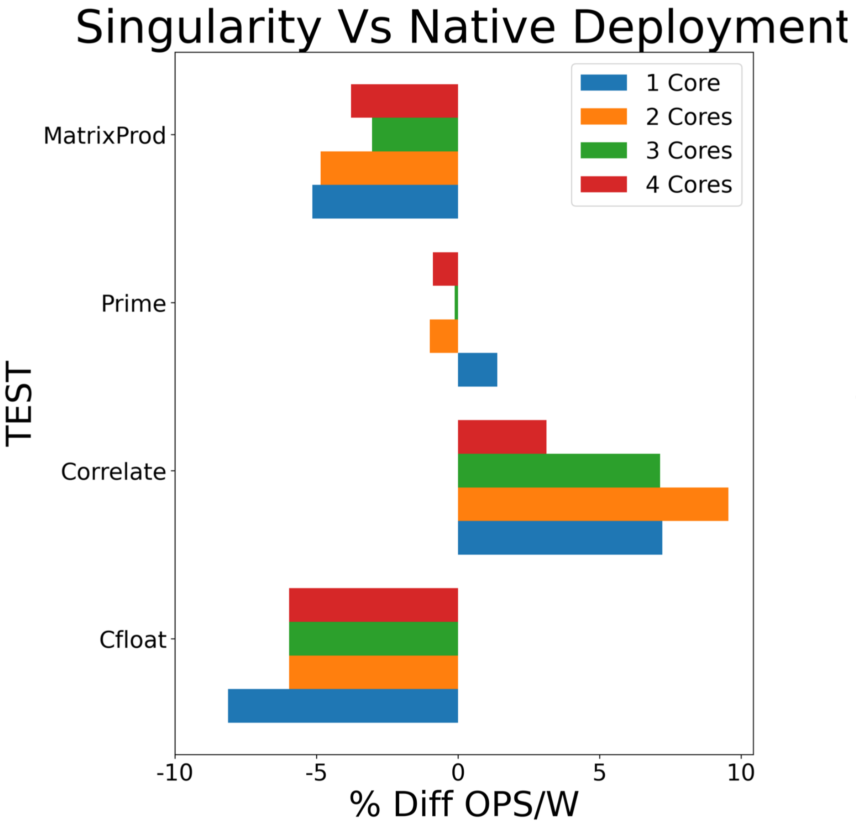
MatrixProd Tests

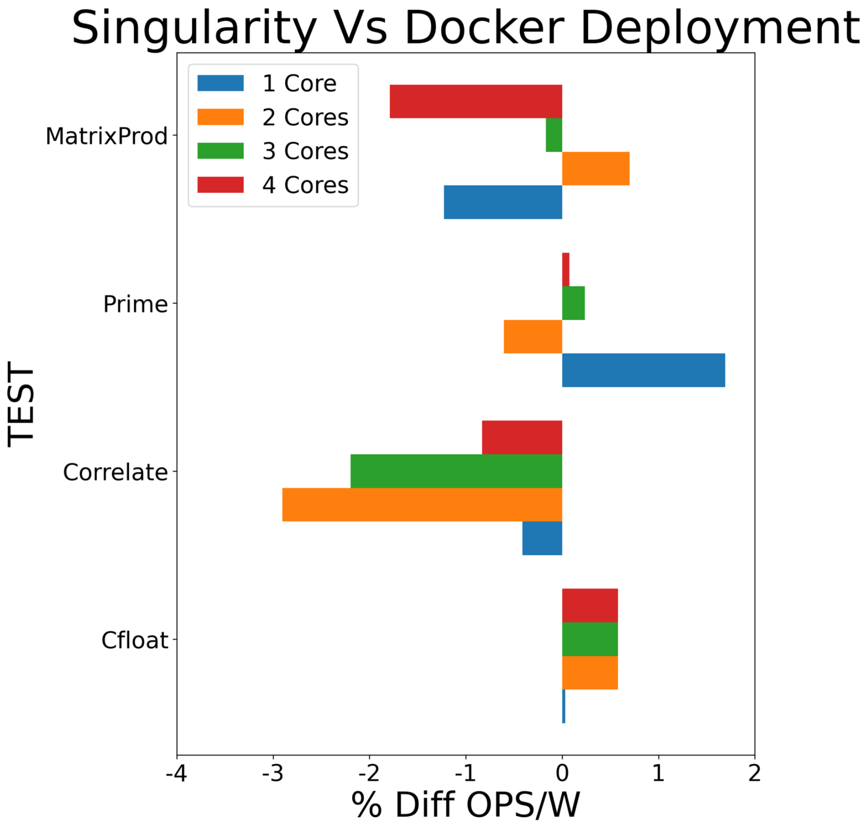


Performance Impact Based on Deployment Approach

MatrixProd Tests







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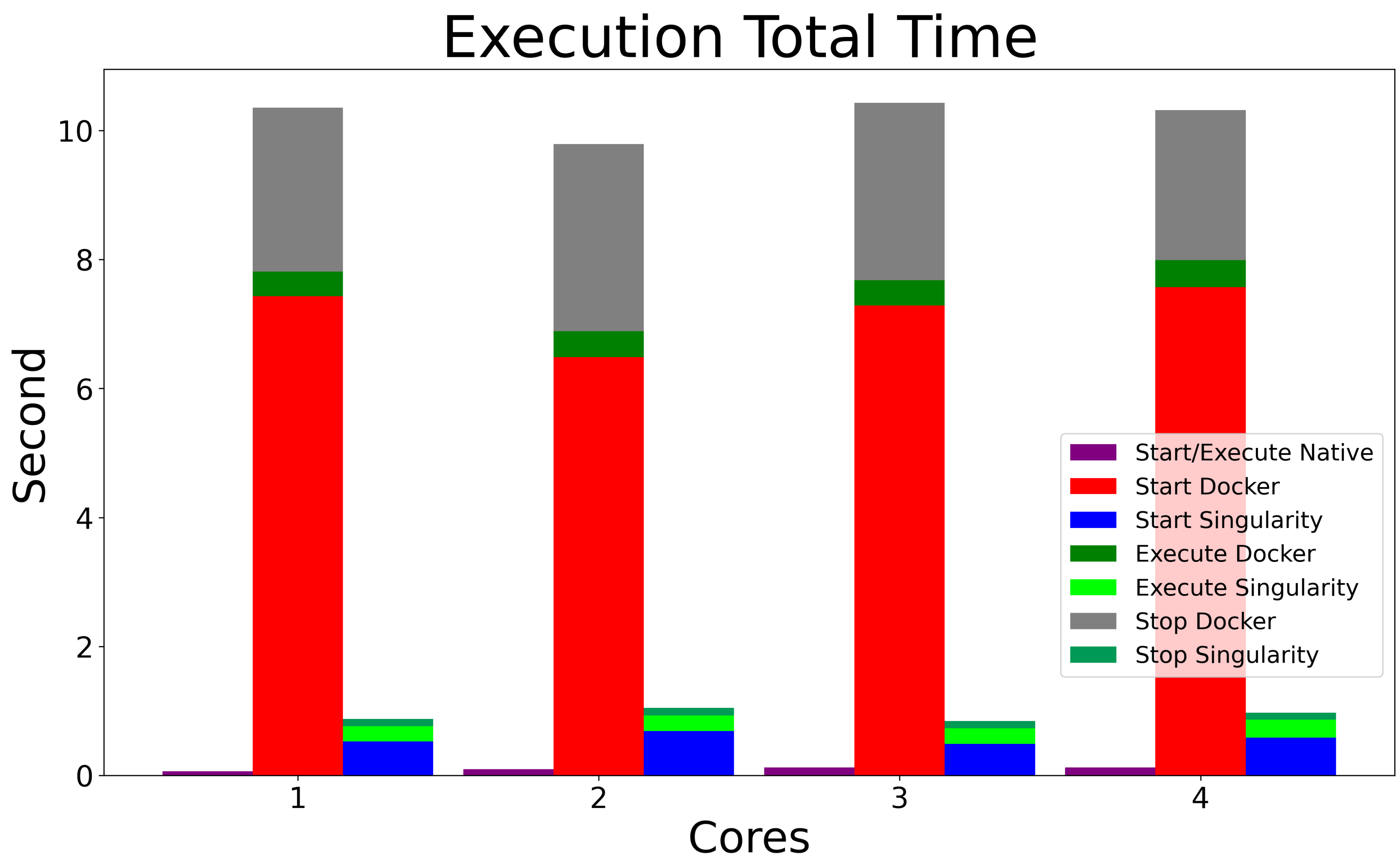
Effect of Deployment on Execution Times



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Findings, Discussion and Conclusions

- Containerized deployments on Post-Moore architecture embedded devices are more efficient in most tests.
  - Singularity minimizes the impact on total execution times and overall power consumption.
- New devices offer various hardware options catering to specific application needs. Their low cost, simplicity in manufacturing, scalability, and high energy efficiency make them excellent candidates for experimenting with solutions to industry and academic problems.
- It is necessary to add elements to define post-Moore architectures and to debate sustainability and reproducibility per peak performance in these architectures.
- it is important to know factors that affect computational (energy) efficiency during the deployment of applications and more thinking about HPC platforms that use post-Moore architectures focused on milliclusters.

Gracias, Merci, Thanks
Questions, Comments?

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