CPU and CLK

File: Sheet1.kicad_sch

ZTURN and 3.3V

File: Sheet5.kicad_sch

Bus Adapter CPLD

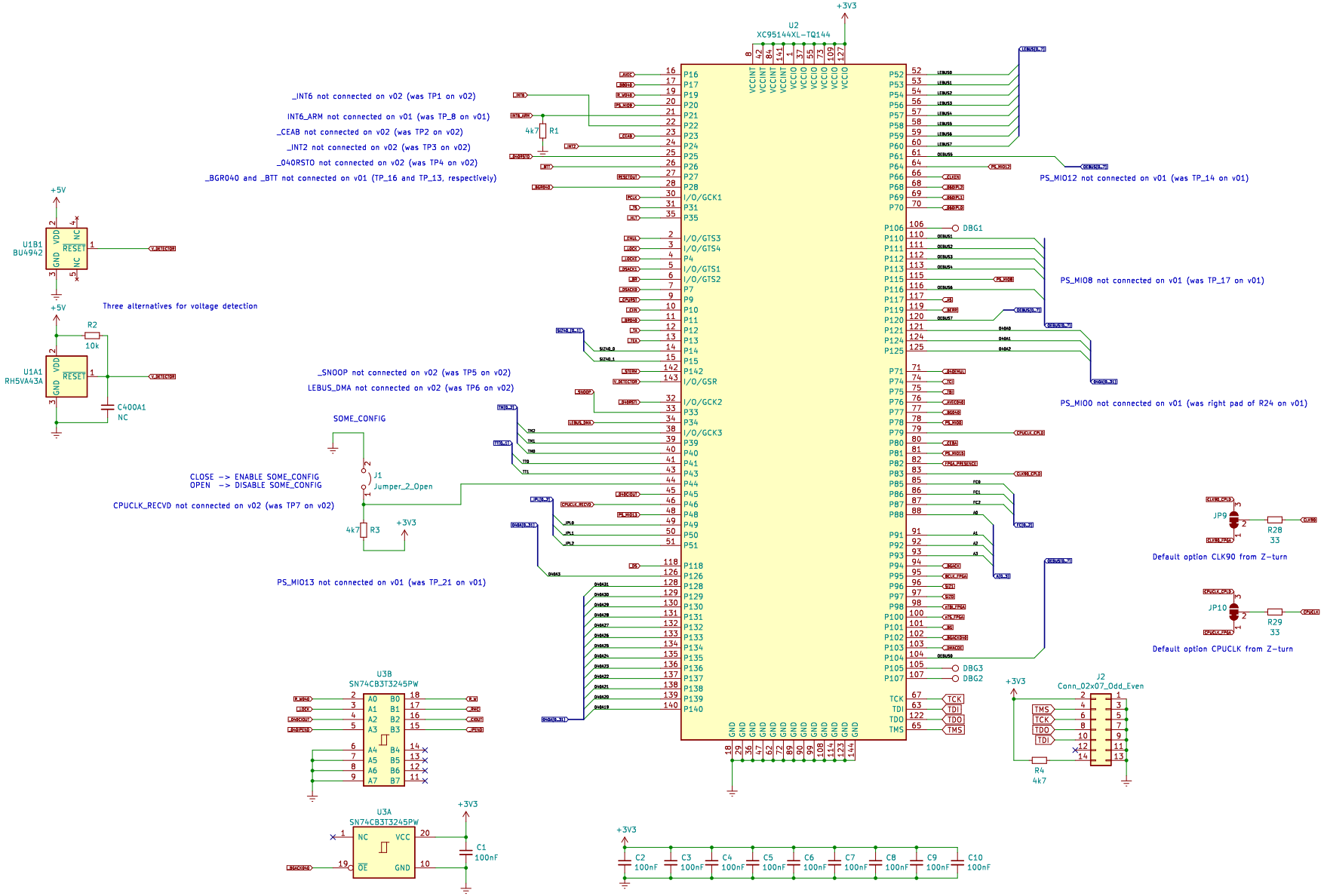
File: Sheet3.kicad_sch

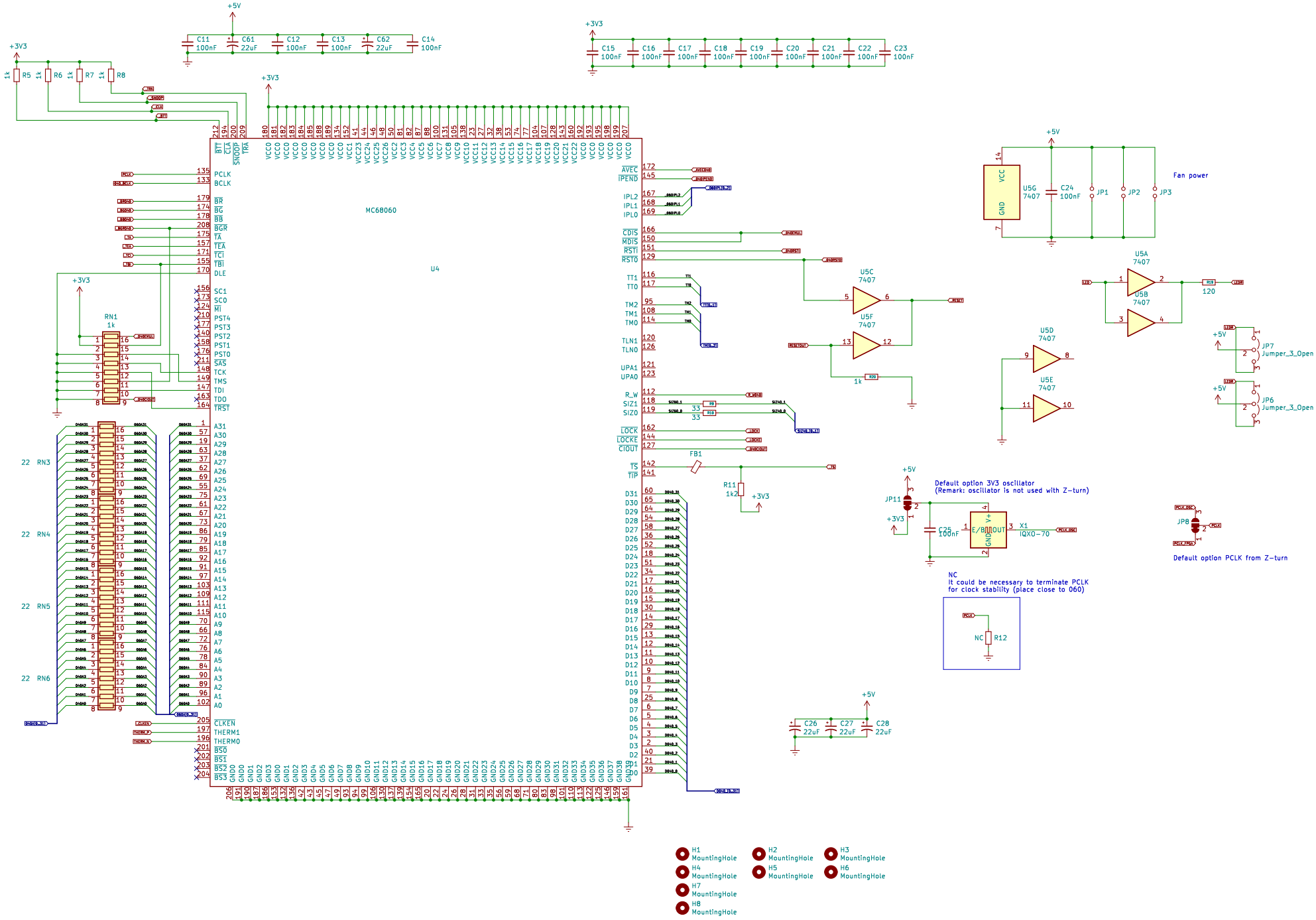
Data Bus Buffer

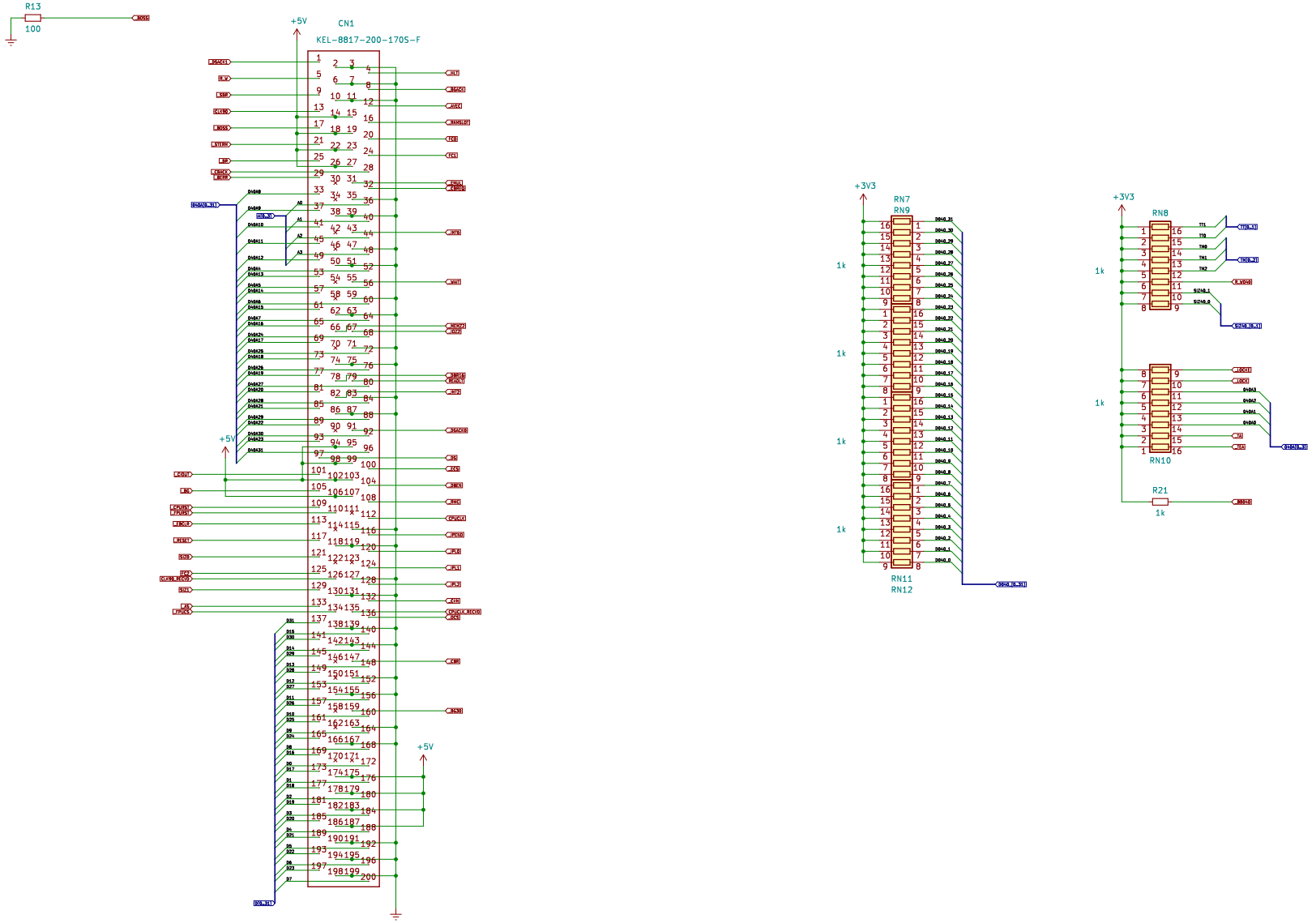
File: Sheet2.kicad_sch

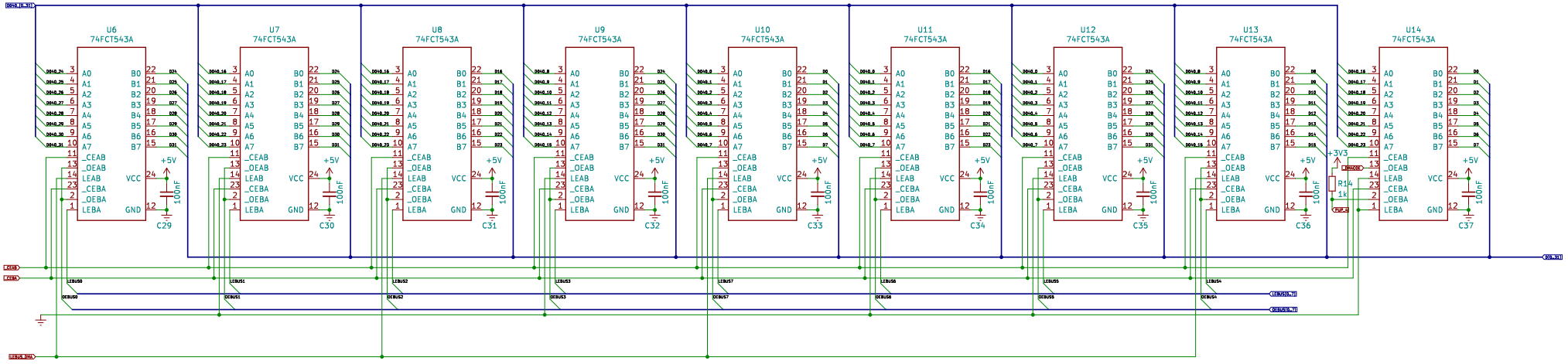
CPU Connector

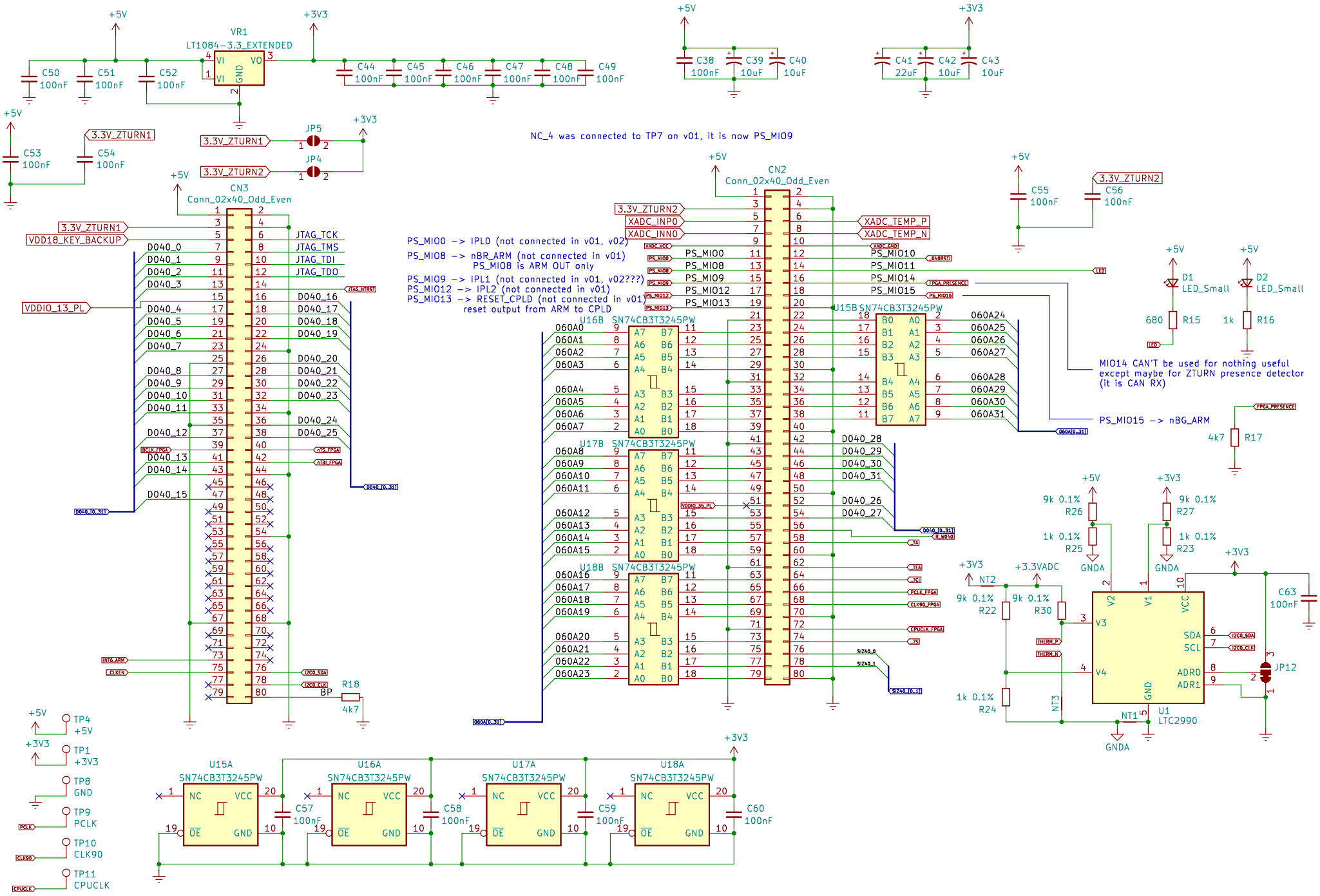
File: Sheet4.kicad_sch


U2
XC95144XL-TQ144
+3V3
_INT6 not connected on v02 (was TP1 on v02)
INT6_ARM not connected on v01 (was TP_8 on v01)
_CEAB not connected on v02 (was TP2 on v02)
_INT2 not connected on v02 (was TP3 on v02)
_040RSTO not connected on v02 (was TP4 on v02)
_BGR040 and _BTT not connected on v01 (TP_16 and TP_13, respectively)
4k7
R1
PS_MIO12 not connected on v01 (was TP_14 on v01)
PS_MIO8 not connected on v01 (was TP_17 on v01)
PS_MIO0 not connected on v01 (was right pad of R24 on v01)
DBG1
DBG3
DBG2
+5V
U1B1
BU4942
Three alternatives for voltage detection
U1A1
RH5VA43A
R2
10k
C400A1
NC
_SNOOP not connected on v02 (was TP5 on v02)
LEBUS_DMA not connected on v02 (was TP6 on v02)
SOME_CONFIG
J1
Jumper_2_Open
CLOSE -> ENABLE SOME_CONFIG
OPEN -> DISABLE SOME_CONFIG
CPUCLK_RECVD not connected on v02 (was TP7 on v02)
4k7
R3
+3V3
PS_MIO13 not connected on v01 (was TP_21 on v01)
JP9
R28
33
Default option CLK90 from Z-turn
JP10
R29
33
Default option CPUCLK from Z-turn
J2
Conn_02x07_Odd_Even
TMS
TCK
TDO
TDI
R4
4k7
U3B
SN74CB3T3245PW
U3A
SN74CB3T3245PW
C1
100nF
C2
100nF
C3
100nF
C4
100nF
C5
100nF
C6
100nF
C7
100nF
C8
100nF
C9
100nF
C10
100nF


MC68060
U4
+5V
+3V3
C11 100nF
C61 22uF
C12 100nF
C13 100nF
C62 22uF
C14 100nF
C15 100nF
C16 100nF
C17 100nF
C18 100nF
C19 100nF
C20 100nF
C21 100nF
C22 100nF
C23 100nF
R5 1k
R6 1k
R7 1k
R8 1k
RN1 1k
22 RN3
22 RN4
22 RN5
22 RN6
U5C 7407
U5F 7407
U5G 7407
U5A 7407
U5B 7407
U5D 7407
U5E 7407
Fan power
JP1
JP2
JP3
JP7 Jumper_3_Open
JP6 Jumper_3_Open
R19 120
R20 1k
FB1
R11 1k2
JP11
C25 100nF
X1 IQXO-70
Default option 3V3 oscillator
(Remark: oscillator is not used with Z-turn)
JP8
Default option PCLK from Z-turn
NC
It could be necessary to terminate PCLK
for clock stability (place close to 060)
NC R12
C26 22uF
C27 22uF
C28 22uF
H1 MountingHole
H2 MountingHole
H3 MountingHole
H4 MountingHole
H5 MountingHole
H6 MountingHole
H7 MountingHole
H8 MountingHole


R13
100
+5V
CN1
KEL-8817-200-170S-F
+5V
+5V
+3V3
RN7
RN9
RN11
RN12
1k
1k
1k
1k
+3V3
RN8
1k
RN10
R21
1k


U6
74FCT543A
U7
74FCT543A
U8
74FCT543A
U9
74FCT543A
U10
74FCT543A
U11
74FCT543A
U12
74FCT543A
U13
74FCT543A
U14
74FCT543A
A0
A1
A2
A3
A4
A5
A6
A7
B0
B1
B2
B3
B4
B5
B6
B7
_CEAB
_OEAB
LEAB
_CEBA
_OEBA
LEBA
VCC
GND
+5V
100nF
C29
C30
C31
C32
C33
C34
C35
C36
C37
+3V3
R14
1k
LEBUS0
LEBUS1
LEBUS2
LEBUS3
LEBUS7
LEBUS6
LEBUS5
LEBUS4
DEBUS0
DEBUS1
DEBUS2
DEBUS3
DEBUS7
DEBUS6
DEBUS5
DEBUS4


VR1
LT1084-3.3_EXTENDED
C50 100nF
C51 100nF
C52 100nF
C44 100nF
C45 100nF
C46 100nF
C47 100nF
C48 100nF
C49 100nF
C38 100nF
C39 10uF
C40 10uF
C41 22uF
C42 10uF
C43 10uF
C53 100nF
C54 100nF
C55 100nF
C56 100nF
C57 100nF
C58 100nF
C59 100nF
C60 100nF
C63 100nF
JP5
JP4
3.3V_ZTURN1
3.3V_ZTURN2
NC_4 was connected to TP7 on v01, it is now PS_MIO9
CN3
Conn_02x40_Odd_Even
CN2
Conn_02x40_Odd_Even
VDD18_KEY_BACKUP
VDDIO_13_PL
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_NTRST
D040_0
D040_1
D040_2
D040_3
D040_4
D040_5
D040_6
D040_7
D040_8
D040_9
D040_10
D040_11
D040_12
D040_13
D040_14
D040_15
D040_16
D040_17
D040_18
D040_19
D040_20
D040_21
D040_22
D040_23
D040_24
D040_25
D040_26
D040_27
D040_28
D040_29
D040_30
D040_31
PCLK_FPGA
nTS_FPGA
nTBI_FPGA
INT6_ARM
CLKEN
I2C0_SDA
I2C0_CLK
BP
R18
4k7
XADC_INP0
XADC_INN0
XADC_TEMP_P
XADC_TEMP_N
PS_MIO0 -> IPL0 (not connected in v01, v02)
PS_MIO8 -> nBR_ARM (not connected in v01)
PS_MIO8 is ARM OUT only
PS_MIO9 -> IPL1 (not connected in v01, v02???)
PS_MIO12 -> IPL2 (not connected in v01)
PS_MIO13 -> RESET_CPLD (not connected in v01)
reset output from ARM to CPLD
PS_MIO0
PS_MIO8
PS_MIO9
PS_MIO10
PS_MIO11
PS_MIO12
PS_MIO13
PS_MIO14
PS_MIO15
040RSTI
LED
FPGA_PRESENCE
MIO14 CAN'T be used for nothing useful
except maybe for ZTURN presence detector
(it is CAN RX)
PS_MIO15 -> nBG_ARM
D1 LED_Small
D2 LED_Small
680 R15
1k R16
4k7 R17
U15B SN74CB3T3245PW
U16B SN74CB3T3245PW
U17B SN74CB3T3245PW
U18B SN74CB3T3245PW
060A0
060A1
060A2
060A3
060A4
060A5
060A6
060A7
060A8
060A9
060A10
060A11
060A12
060A13
060A14
060A15
060A16
060A17
060A18
060A19
060A20
060A21
060A22
060A23
060A24
060A25
060A26
060A27
060A28
060A29
060A30
060A31
VDDIO_35_PL
R_W040
TA
TEA
TCI
PCLK_FPGA
CLK90_FPGA
CPUCLK_FPGA
TS
SIZ40_0
SIZ40_1
SIZ40_[0..1]
9k 0.1% R26
1k 0.1% R25
9k 0.1% R27
1k 0.1% R23
9k 0.1% R22
9k 0.1% R30
1k 0.1% R24
+3.3VADC
GNDA
NT1
NT2
NT3
THERM_P
THERM_N
U1 LTC2990
SDA
SCL
ADR0
ADR1
JP12
TP4 +5V
TP1 +3V3
TP8 GND
TP9 PCLK
TP10 CLK90
TP11 CPUCLK
U15A SN74CB3T3245PW
U16A SN74CB3T3245PW
U17A SN74CB3T3245PW
U18A SN74CB3T3245PW