CPU and CLK

File: Sheet1.kicad_sch

IPL and 3.3V

File: Sheet5.kicad_sch

Bus Adapter

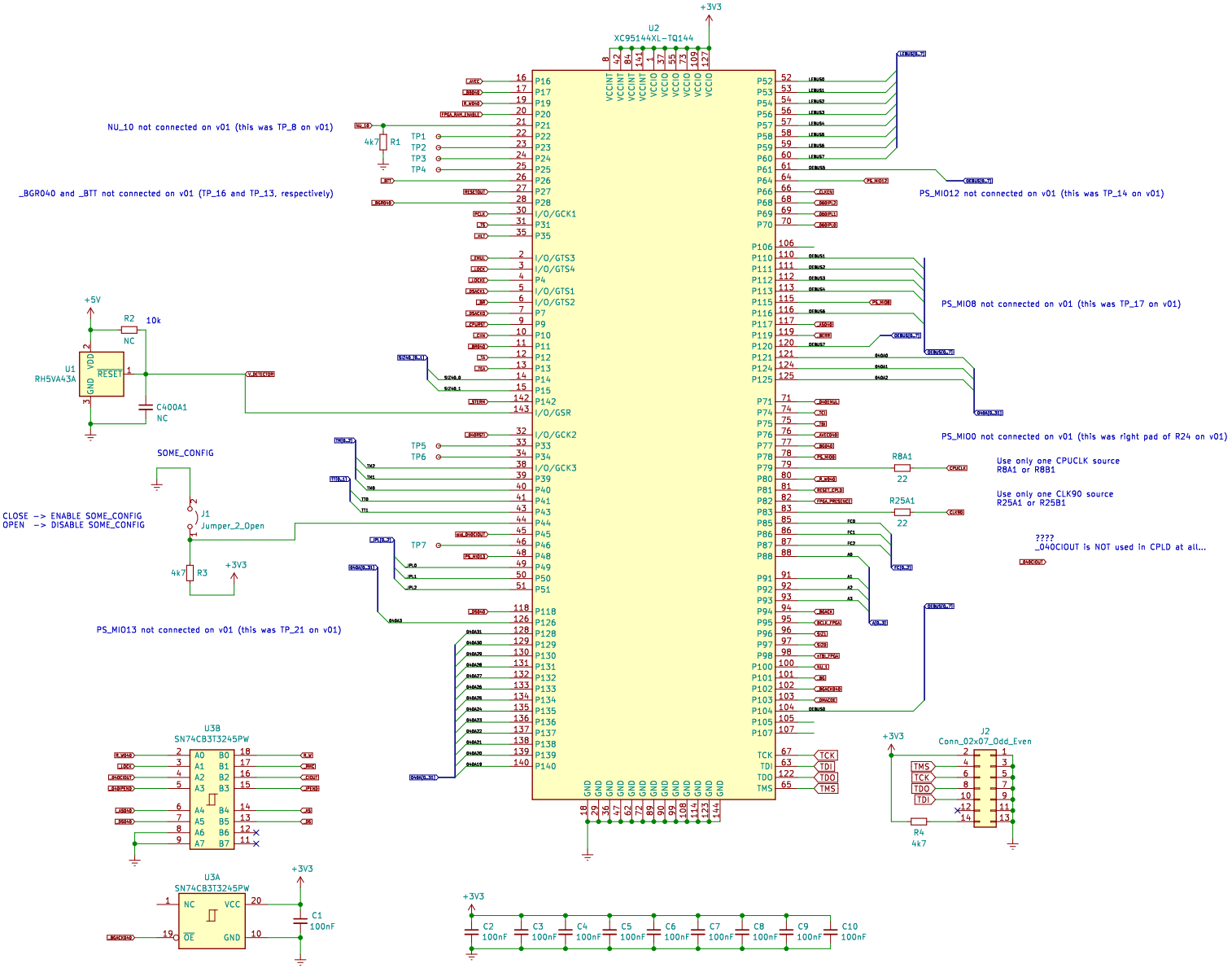
File: Sheet3.kicad_sch

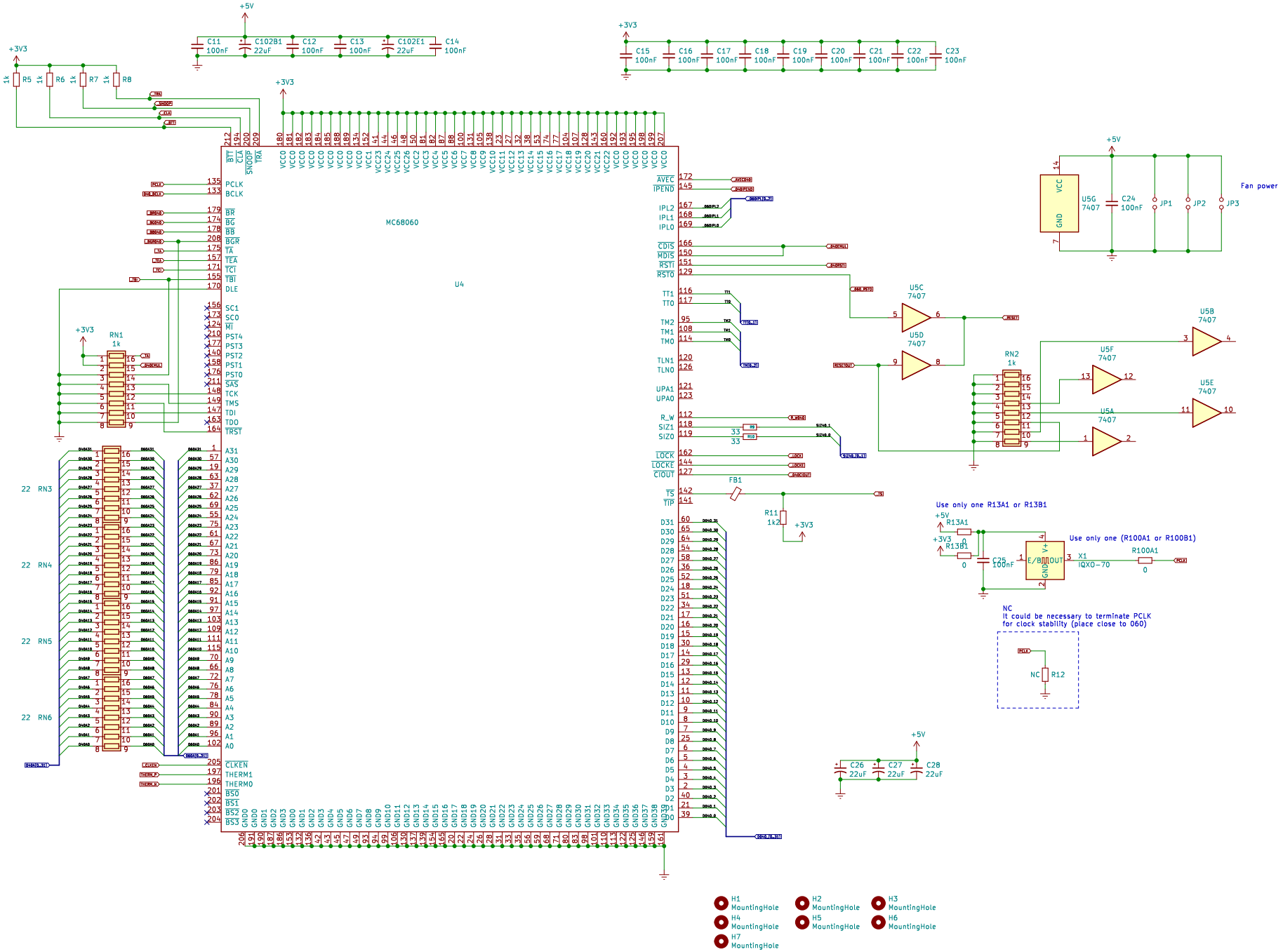
Data Bus Buffer

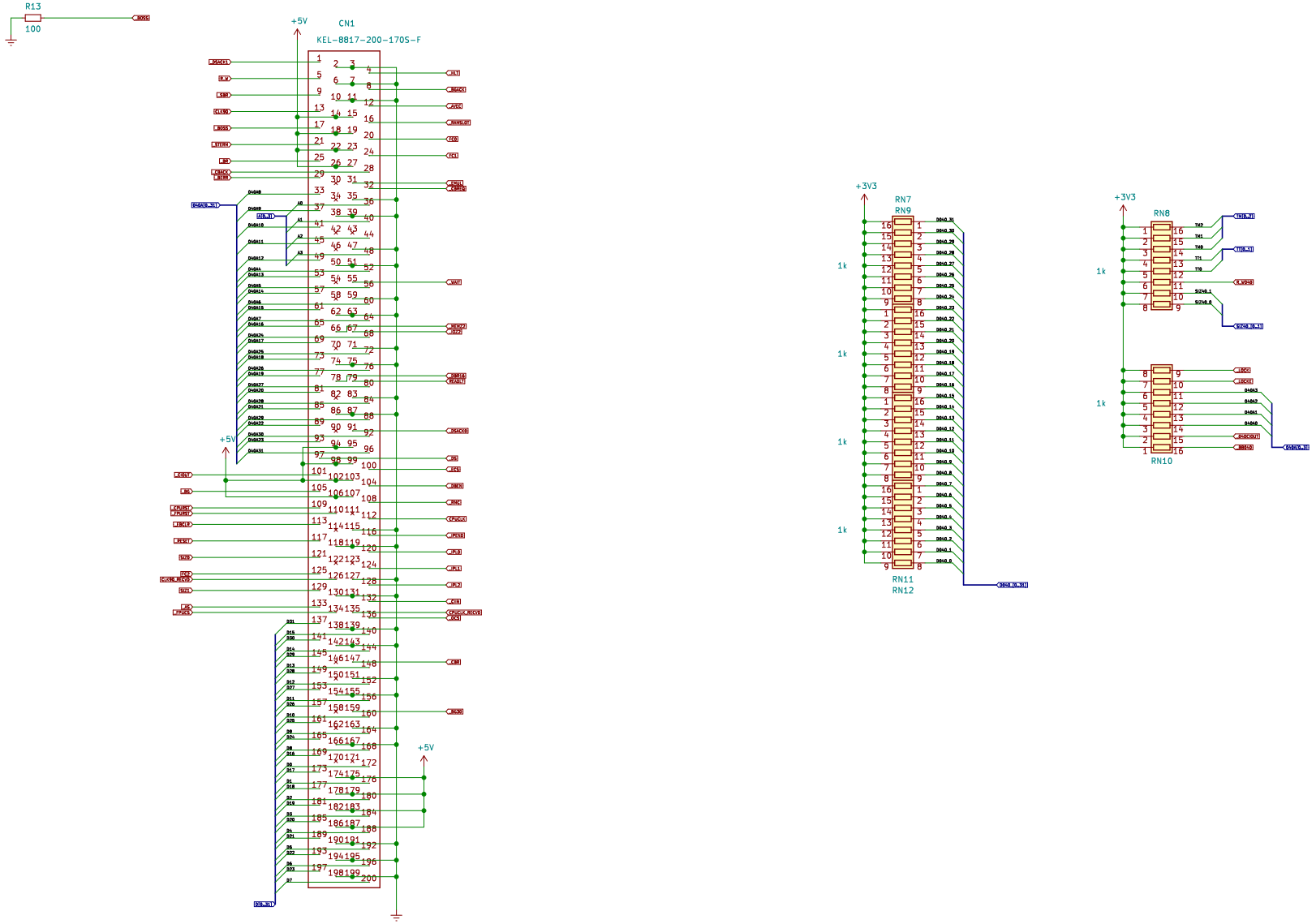
File: Sheet2.kicad_sch

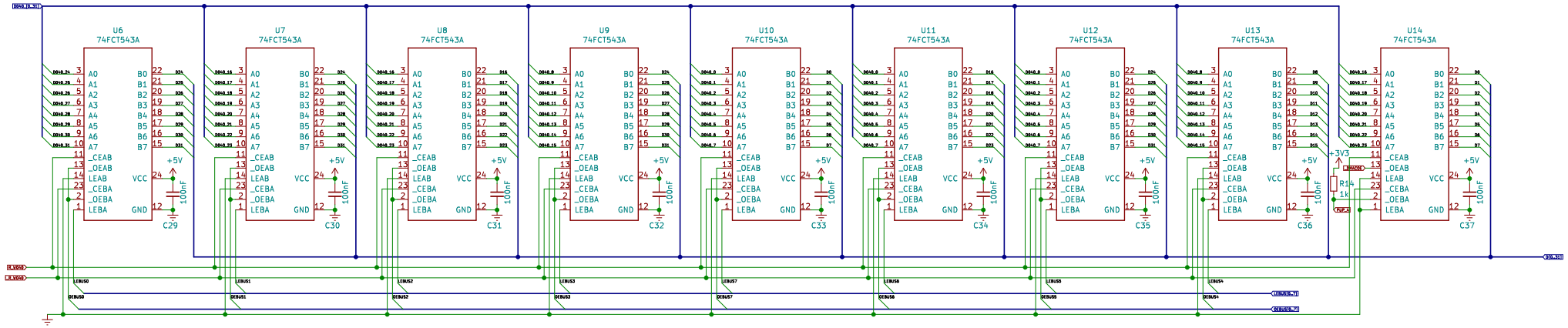
CPU Connector

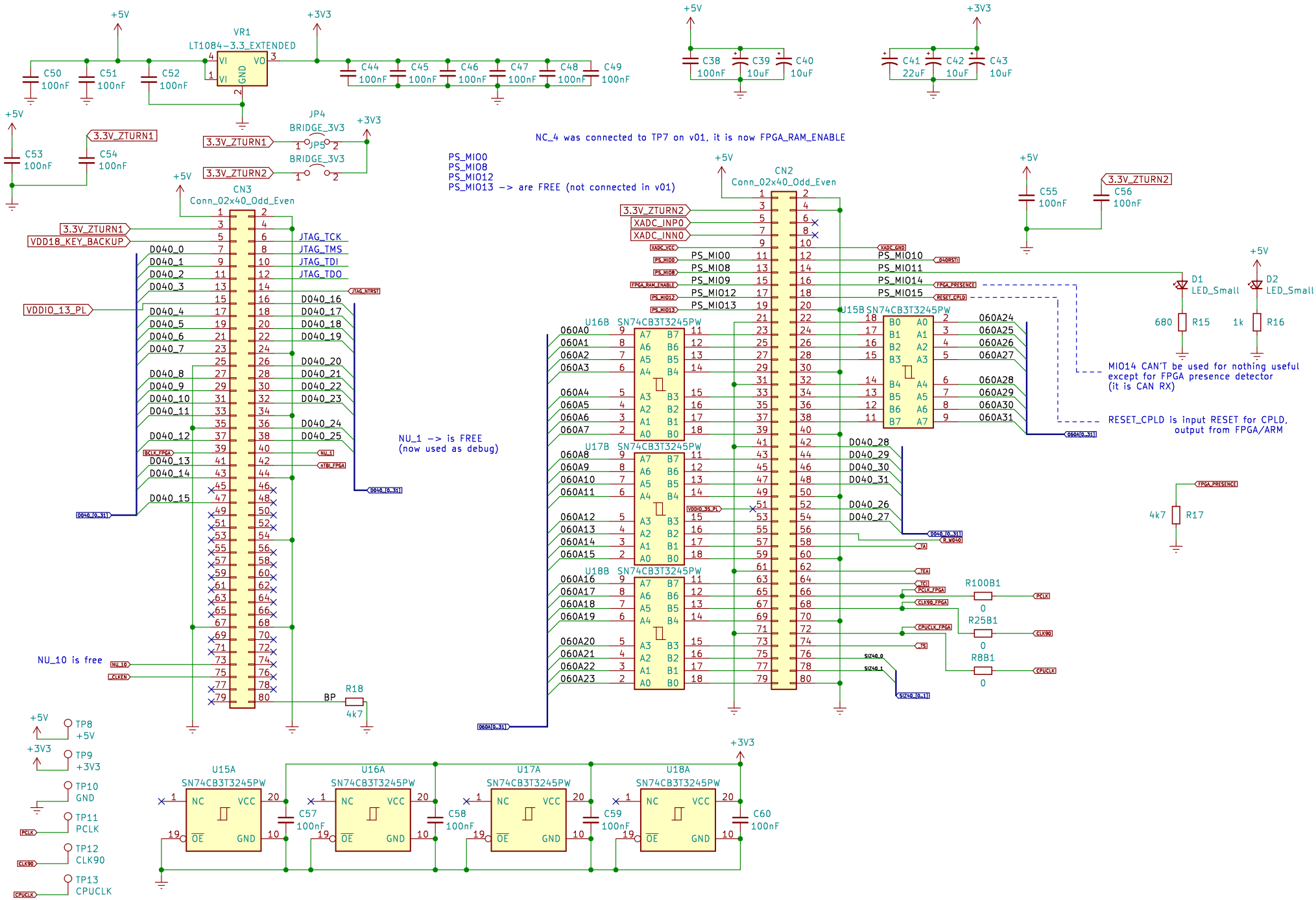
File: Sheet4.kicad_sch


U2
XC95144XL-TQ144
+3V3
NU_10 not connected on v01 (this was TP_8 on v01)
4k7
R1
TP1
TP2
TP3
TP4
_BGR040 and _BTT not connected on v01 (TP_16 and TP_13, respectively)
PS_MIO12 not connected on v01 (this was TP_14 on v01)
PS_MIO8 not connected on v01 (this was TP_17 on v01)
PS_MIO0 not connected on v01 (this was right pad of R24 on v01)
+5V
R2
10k
NC
U1
RH5VA43A
VDD
GND
RESET
C400A1
NC
SOME_CONFIG
J1
Jumper_2_Open
CLOSE -> ENABLE SOME_CONFIG
OPEN -> DISABLE SOME_CONFIG
4k7
R3
TP5
TP6
TP7
PS_MIO13 not connected on v01 (this was TP_21 on v01)
R8A1
22
Use only one CPUCLK source
R8A1 or R8B1
R25A1
22
Use only one CLK90 source
R25A1 or R25B1
????
_040CIOUT is NOT used in CPLD at all...
U3B
SN74CB3T3245PW
U3A
SN74CB3T3245PW
NC
VCC
OE
GND
C1
100nF
C2
100nF
C3
100nF
C4
100nF
C5
100nF
C6
100nF
C7
100nF
C8
100nF
C9
100nF
C10
100nF
J2
Conn_02x07_Odd_Even
TMS
TCK
TDO
TDI
R4
4k7


MC68060
U4
+5V
+3V3
C11 100nF
C102B1 22uF
C12 100nF
C13 100nF
C102E1 22uF
C14 100nF
C15 100nF
C16 100nF
C17 100nF
C18 100nF
C19 100nF
C20 100nF
C21 100nF
C22 100nF
C23 100nF
R5 1k
R6 1k
R7 1k
R8 1k
RN1 1k
RN2 1k
22 RN3
22 RN4
22 RN5
22 RN6
U5C 7407
U5D 7407
U5F 7407
U5B 7407
U5E 7407
U5A 7407
U5G 7407
C24 100nF
JP1
JP2
JP3
Fan power
FB1
R11 1k2
C25 100nF
C26 22uF
C27 22uF
C28 22uF
X1 IQXO-70
R100A1 0
R13A1 0
R13B1 0
Use only one R13A1 or R13B1
Use only one (R100A1 or R100B1)
NC
It could be necessary to terminate PCLK for clock stability (place close to 060)
R12
H1 MountingHole
H2 MountingHole
H3 MountingHole
H4 MountingHole
H5 MountingHole
H6 MountingHole
H7 MountingHole


R13
100
+5V
CN1
KEL-8817-200-170S-F
+3V3
RN7
RN9
RN11
RN12
RN8
RN10
1k


U6
74FCT543A
U7
74FCT543A
U8
74FCT543A
U9
74FCT543A
U10
74FCT543A
U11
74FCT543A
U12
74FCT543A
U13
74FCT543A
U14
74FCT543A
A0
A1
A2
A3
A4
A5
A6
A7
_CEAB
_OEAB
LEAB
_CEBA
_OEBA
LEBA
B0
B1
B2
B3
B4
B5
B6
B7
VCC
GND
+5V
100nF
C29
C30
C31
C32
C33
C34
C35
C36
C37
+3V3
R14
1k


VR1
LT1084-3.3_EXTENDED
C50 100nF
C51 100nF
C52 100nF
C44 100nF
C45 100nF
C46 100nF
C47 100nF
C48 100nF
C49 100nF
C38 100nF
C39 10uF
C40 10uF
C41 22uF
C42 10uF
C43 10uF
C53 100nF
C54 100nF
JP4
BRIDGE_3V3
JP5
3.3V_ZTURN1
3.3V_ZTURN2
NC_4 was connected to TP7 on v01, it is now FPGA_RAM_ENABLE
PS_MIO0
PS_MIO8
PS_MIO12
PS_MIO13 -> are FREE (not connected in v01)
CN3
Conn_02x40_Odd_Even
CN2
Conn_02x40_Odd_Even
VDD18_KEY_BACKUP
VDDIO_13_PL
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_NTRST
D040_0
D040_1
D040_2
D040_3
D040_4
D040_5
D040_6
D040_7
D040_8
D040_9
D040_10
D040_11
D040_12
D040_13
D040_14
D040_15
D040_16
D040_17
D040_18
D040_19
D040_20
D040_21
D040_22
D040_23
D040_24
D040_25
D040_26
D040_27
D040_28
D040_29
D040_30
D040_31
D040[0..31]
BCLK_FPGA
nTBI_FPGA
NU_1
NU_1 -> is FREE
(now used as debug)
NU_10
NU_10 is free
CLKEN
BP
R18
4k7
XADC_INP0
XADC_INN0
XADC_VCC
XADC_GND
FPGA_RAM_ENABLE
FPGA_PRESENCE
RESET_CPLD
040RSTI
U16B SN74CB3T3245PW
U17B SN74CB3T3245PW
U18B SN74CB3T3245PW
U15B SN74CB3T3245PW
060A0
060A1
060A2
060A3
060A4
060A5
060A6
060A7
060A8
060A9
060A10
060A11
060A12
060A13
060A14
060A15
060A16
060A17
060A18
060A19
060A20
060A21
060A22
060A23
060A[0..31]
VDDIO_3S_PL
R_W040
TA
TEA
TC
PCLK_FPGA
CLK90_FPGA
CPUCLK_FPGA
TS
SIZ40_0
SIZ40_1
SIZ40_[0..1]
R100B1
R25B1
R8B1
0
PCLK
CLK90
CPUCLK
C55 100nF
C56 100nF
D1
LED_Small
D2
LED_Small
680
R15
1k
R16
MIO14 CAN'T be used for nothing useful
except for FPGA presence detector
(it is CAN RX)
RESET_CPLD is input RESET for CPLD,
output from FPGA/ARM
4k7
R17
U15A SN74CB3T3245PW
U16A SN74CB3T3245PW
U17A SN74CB3T3245PW
U18A SN74CB3T3245PW
C57 100nF
C58 100nF
C59 100nF
C60 100nF
TP8 +5V
TP9 +3V3
TP10 GND
TP11 PCLK
TP12 CLK90
TP13 CPUCLK