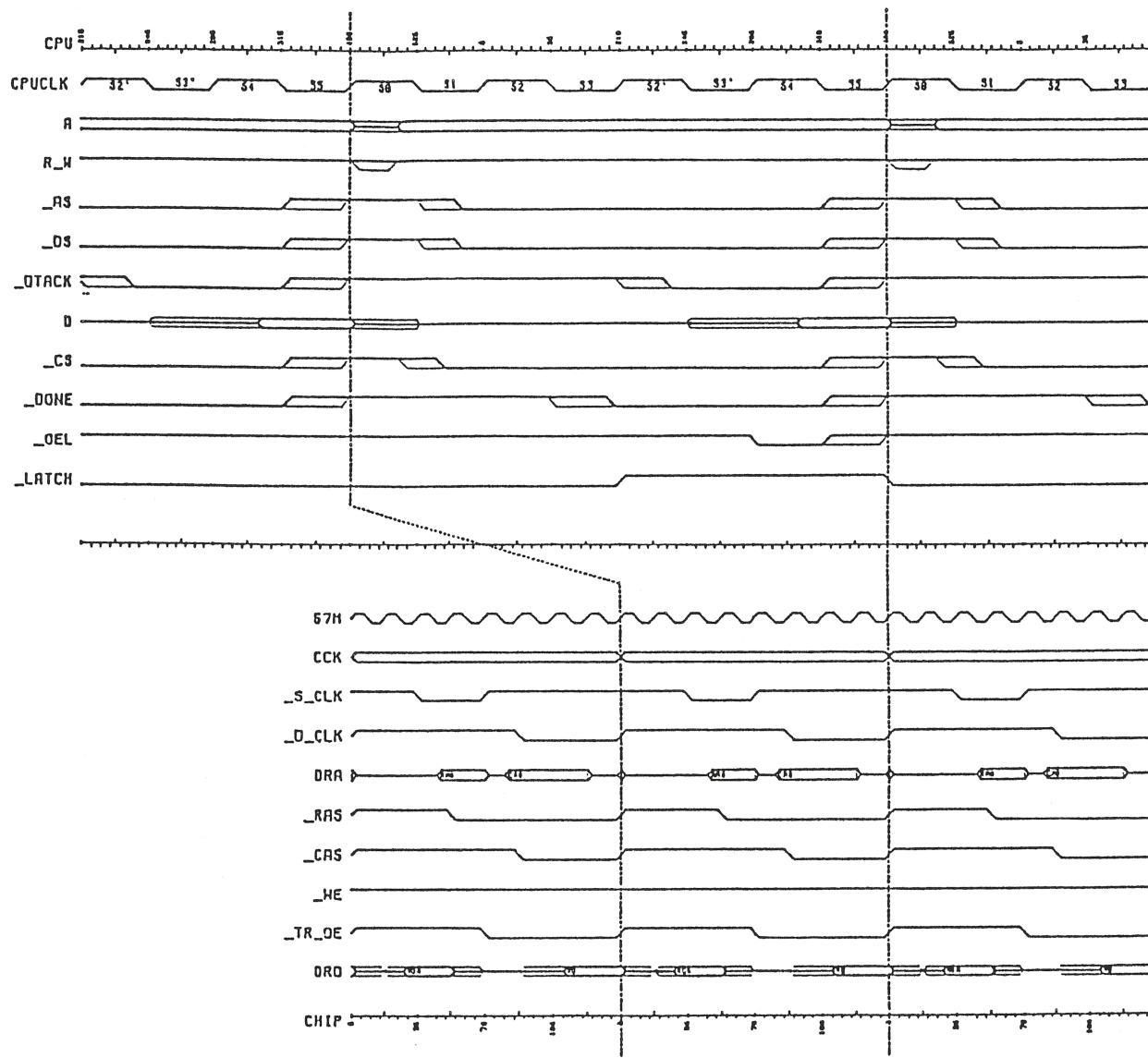


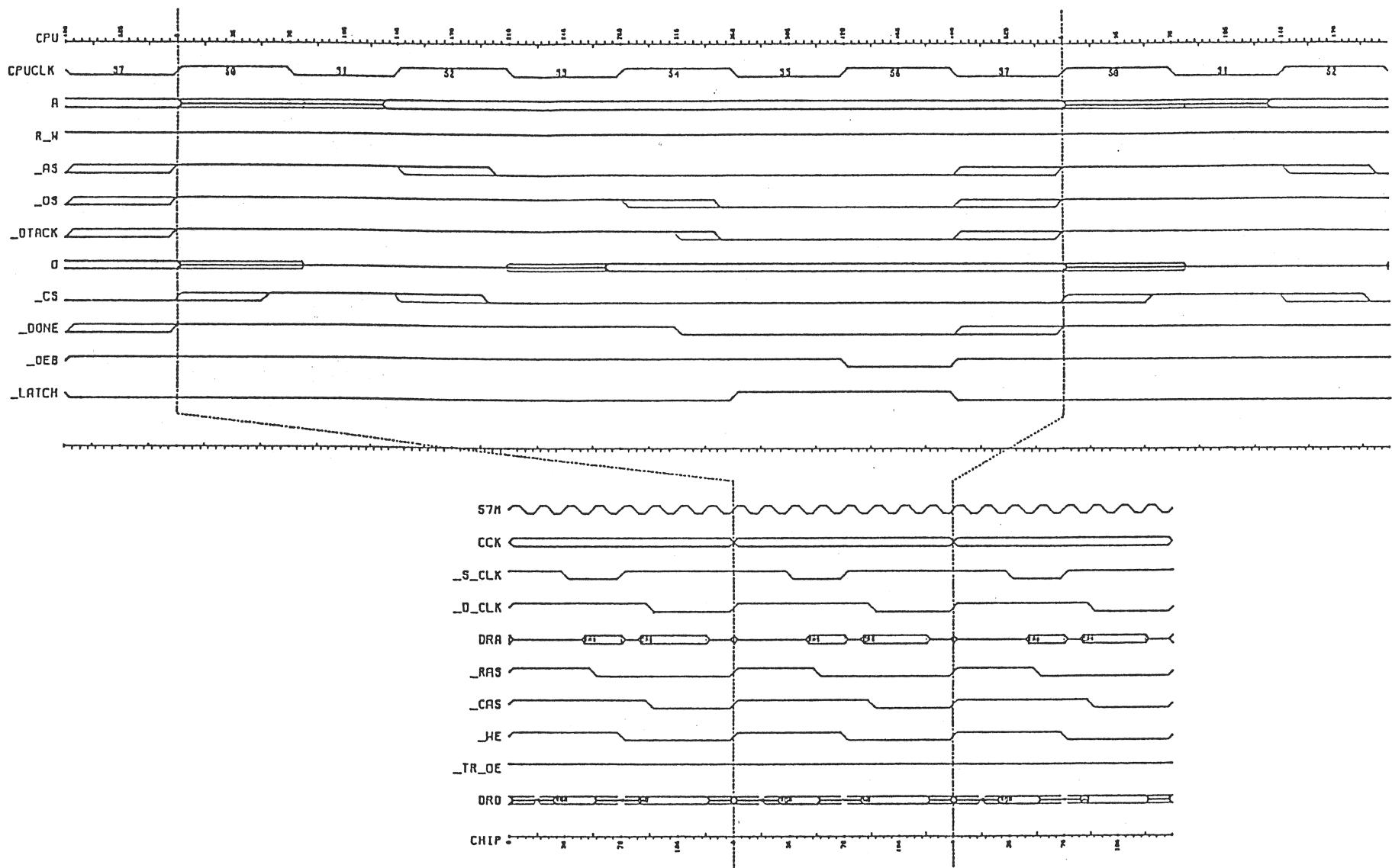
PROCESSOR WRITE CYCLE (14 MHz 68020/030)

A+ Processor/Chip Bus Timing Relations 04/01/92



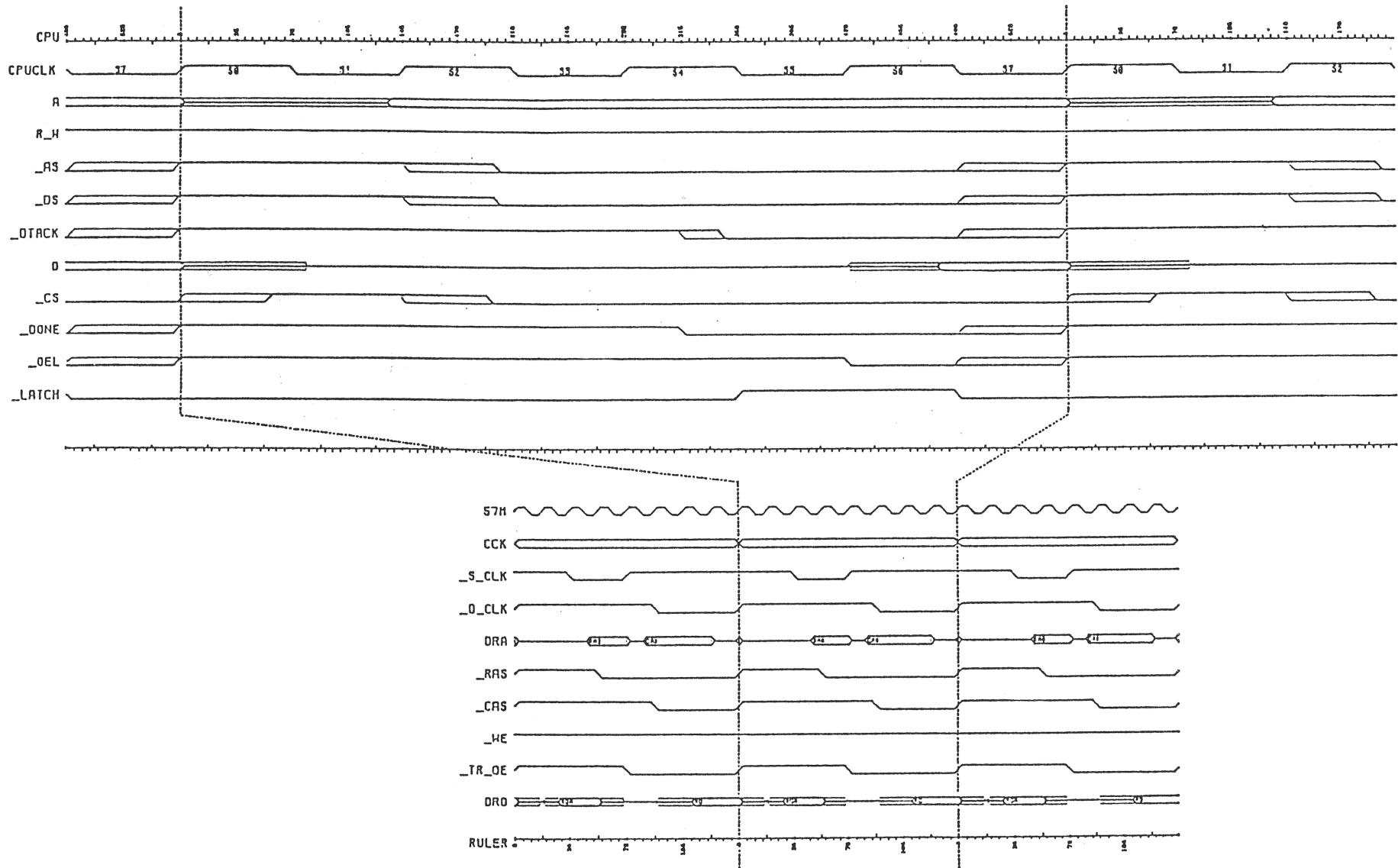
PROCESSOR READ CYCLE (14 MHZ 68020/030)

A+ Processor/Chip Bus Timing Relations 04/01/32



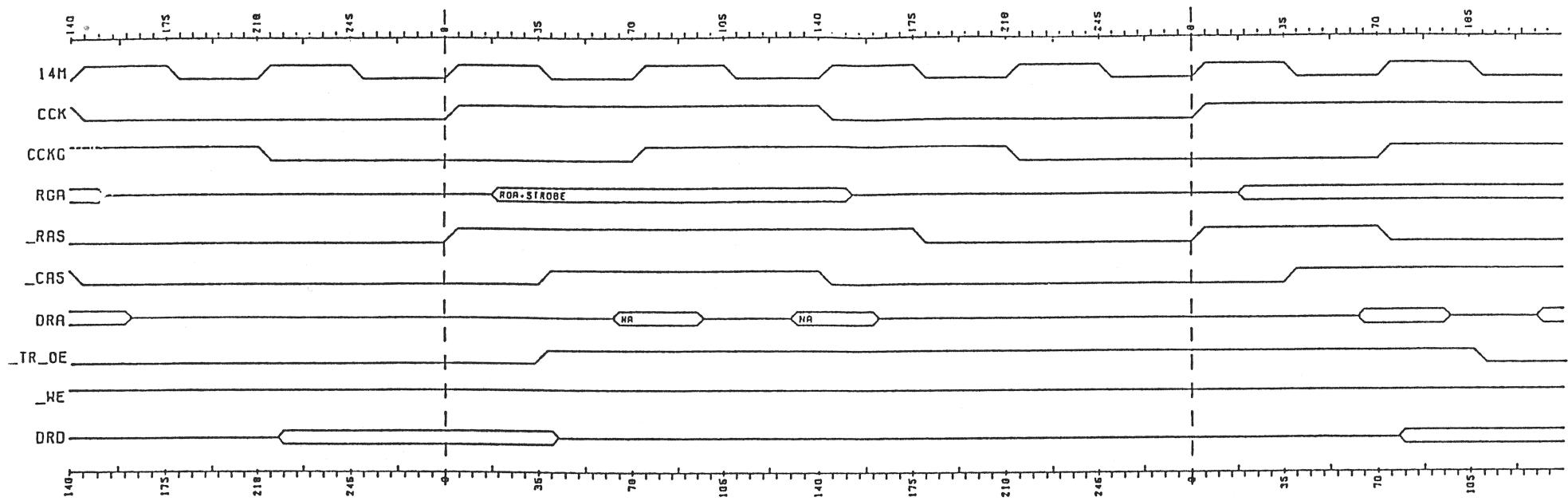
PROCESSOR WRITE CYCLE (7MHz 68000)

A+ Processor/Chip Bus Timing Relations 04/01/92

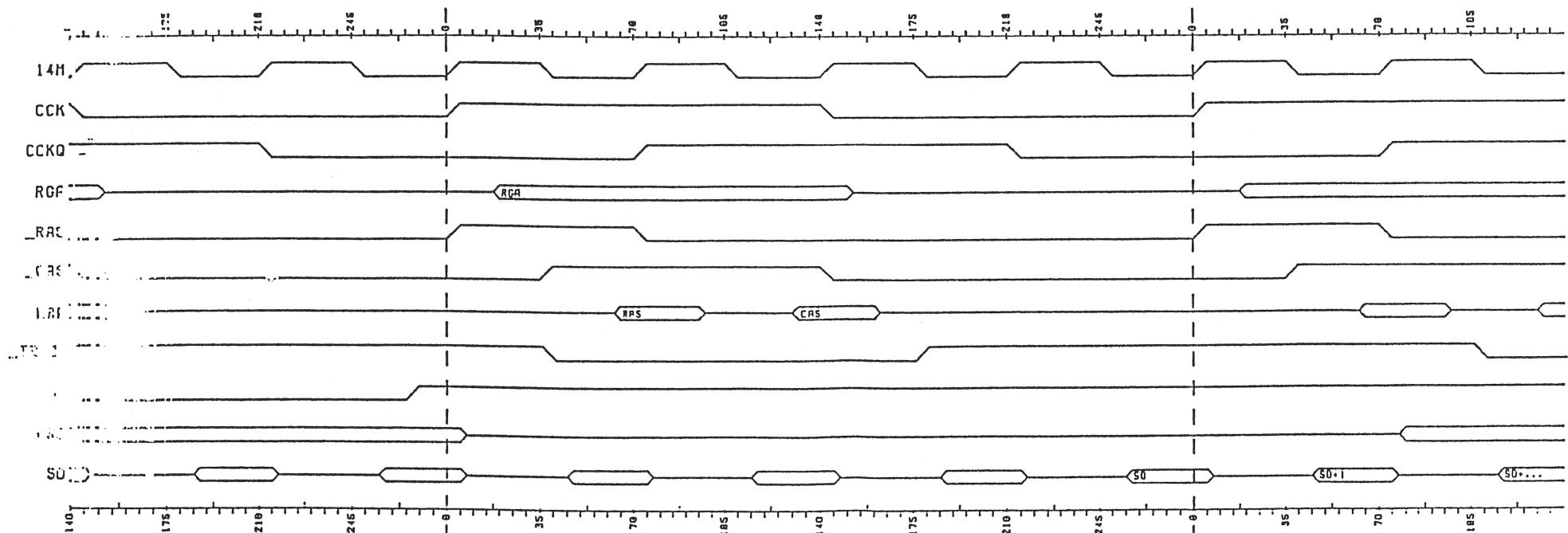


PROCESSOR READ CYCLE (7MHz 68000)

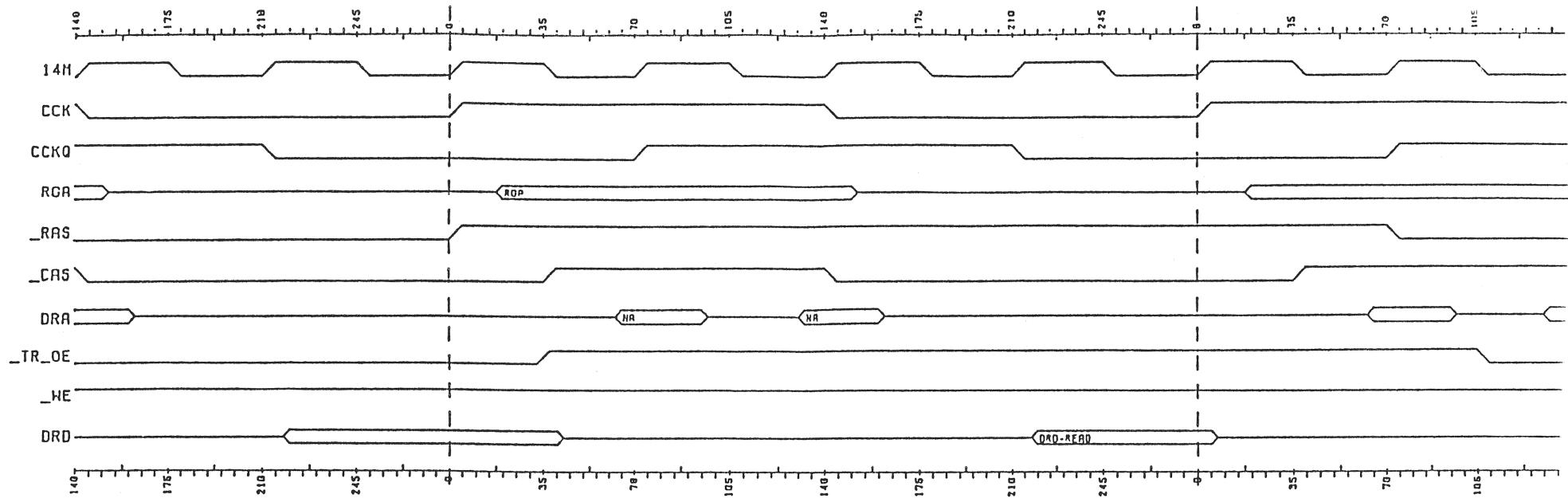
A+ Processor/Chip Bus Timing Relations 04/01/92



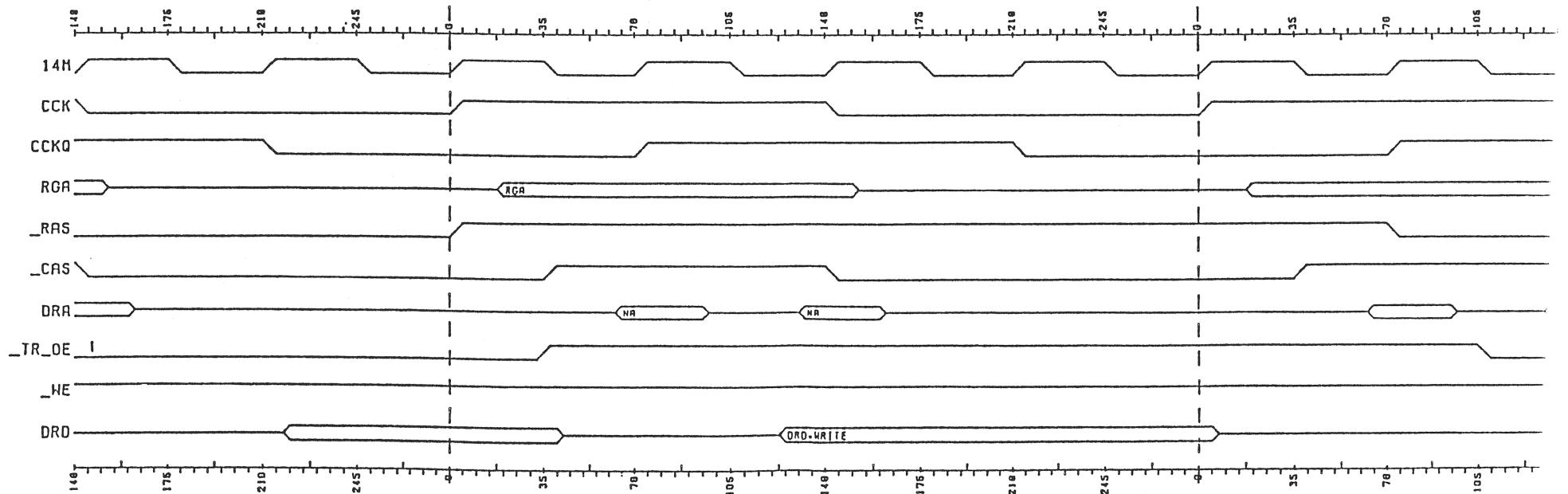
NEW CAS BEFORE RAS REFRESH



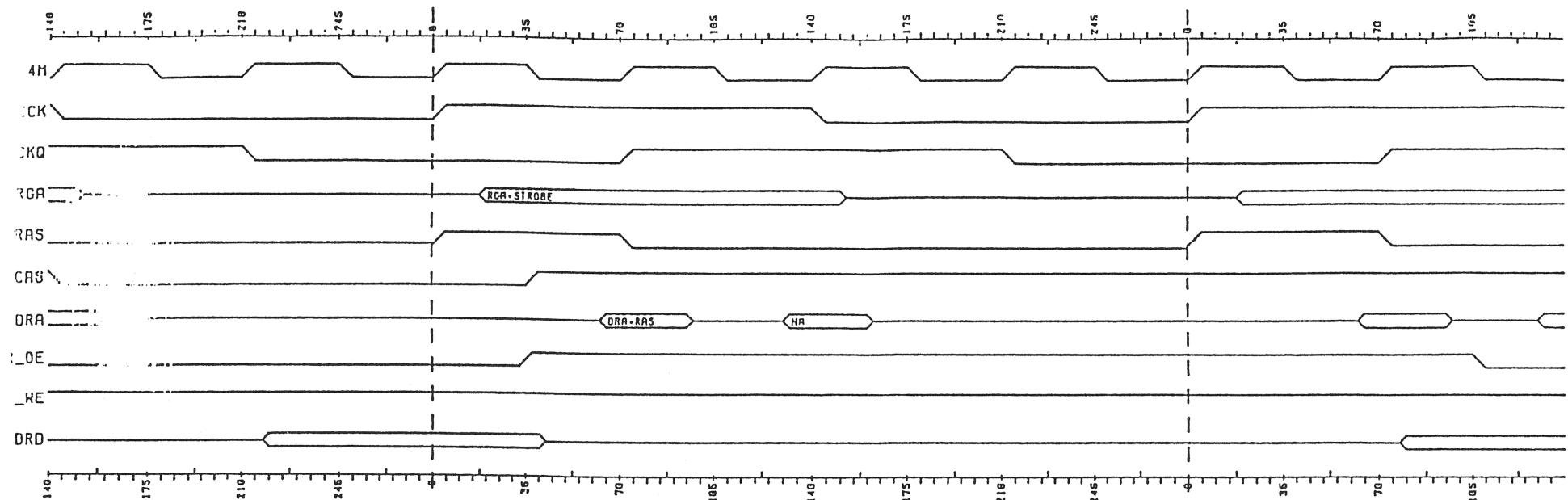
NEW SHIFT REGISTER LOAD CYCLE



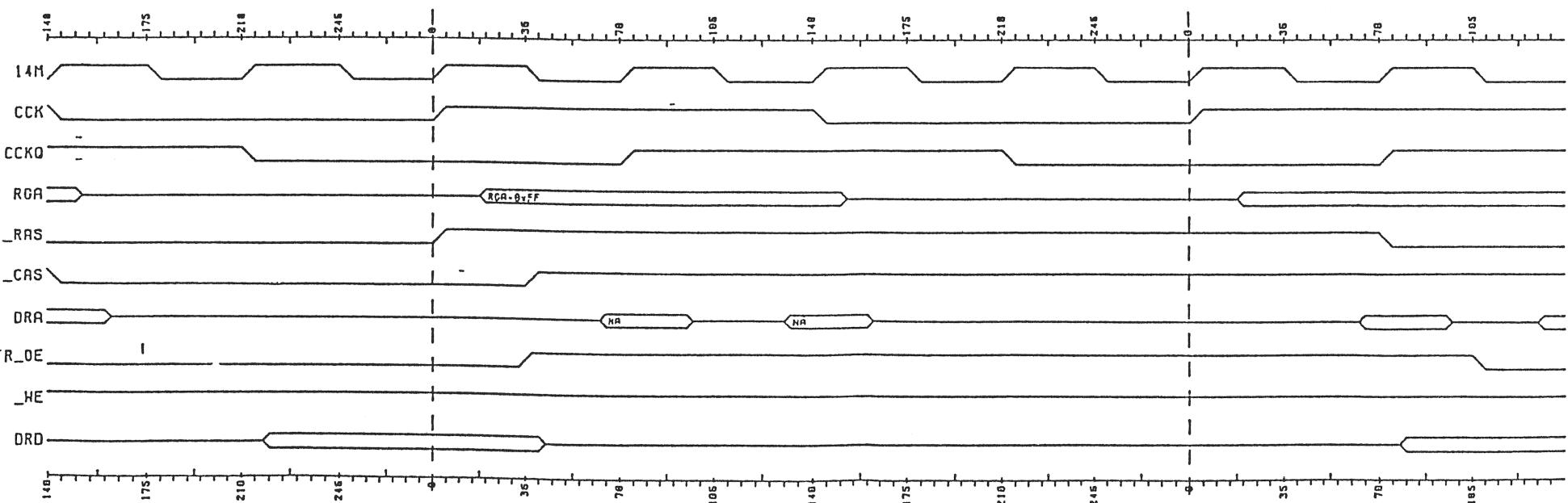
REVISED REGISTER READ CYCLE



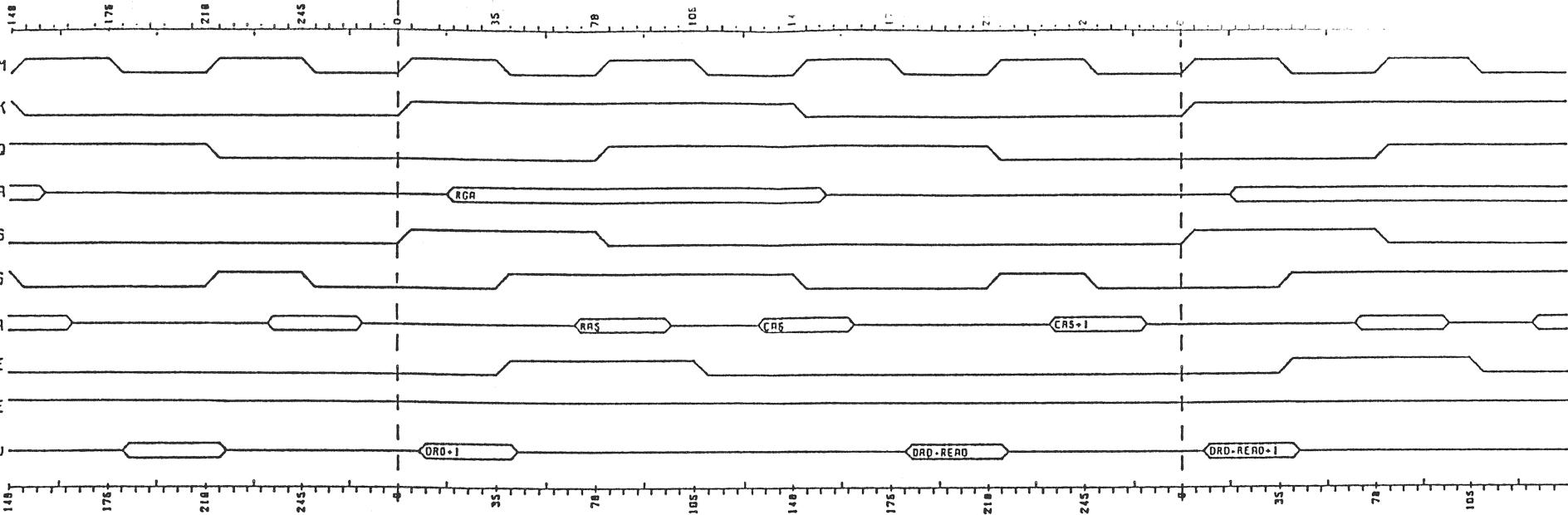
REVISED REGISTER WRITE CYCLE



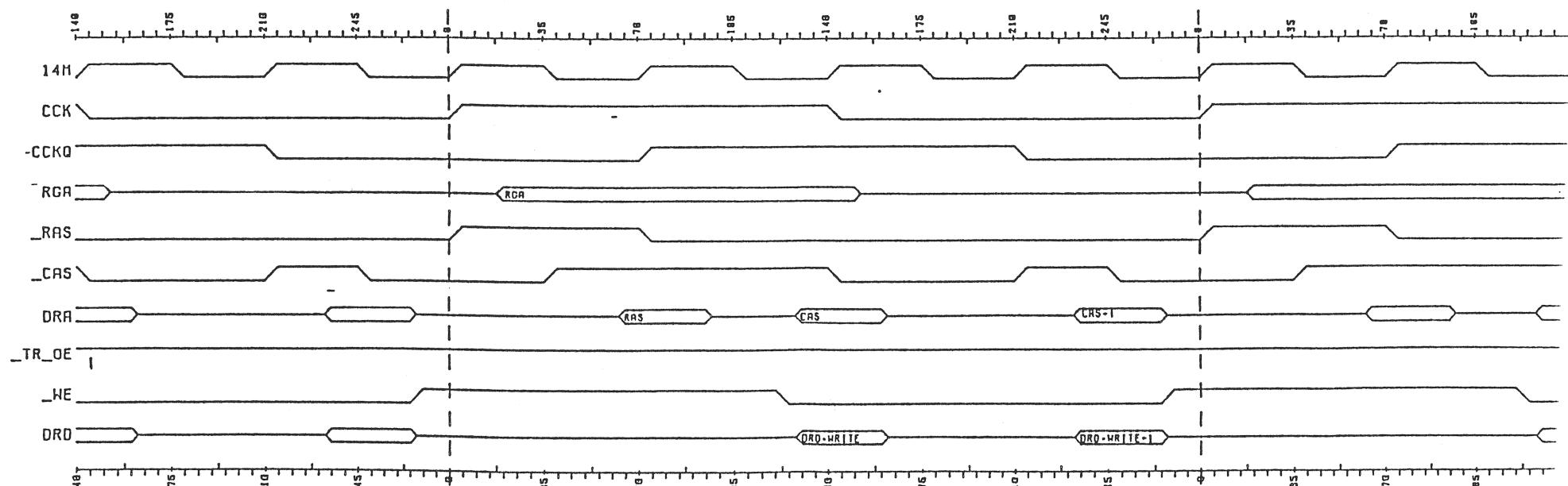
REVISED RAS ONLY REFRESH



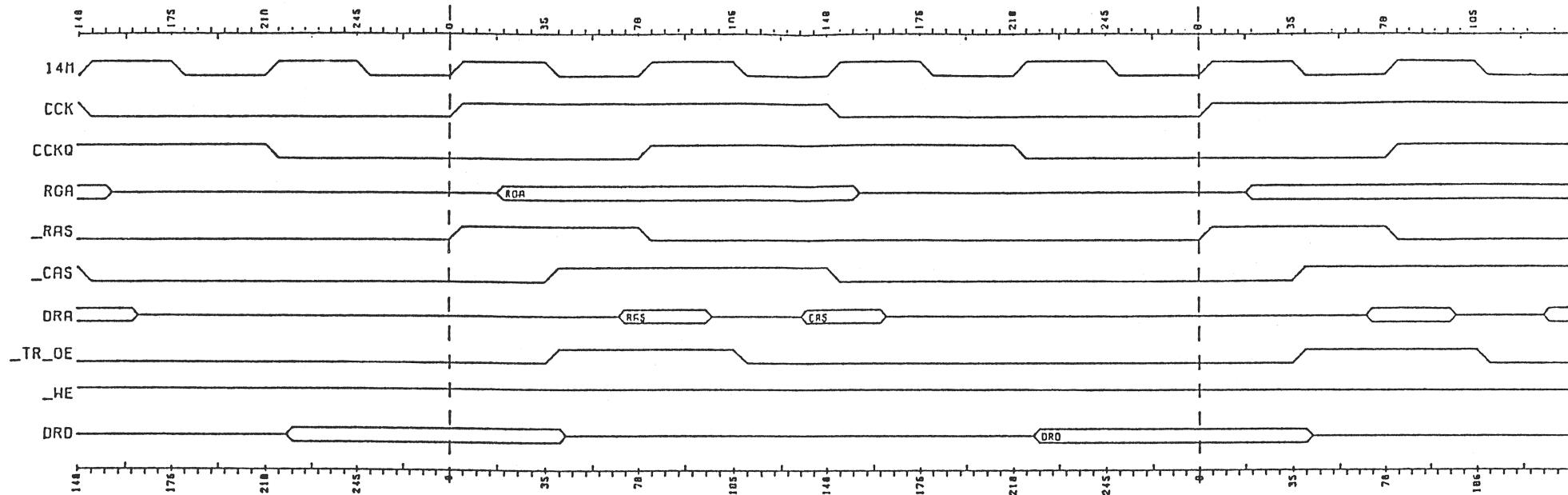
REVISED NULL CYCLE



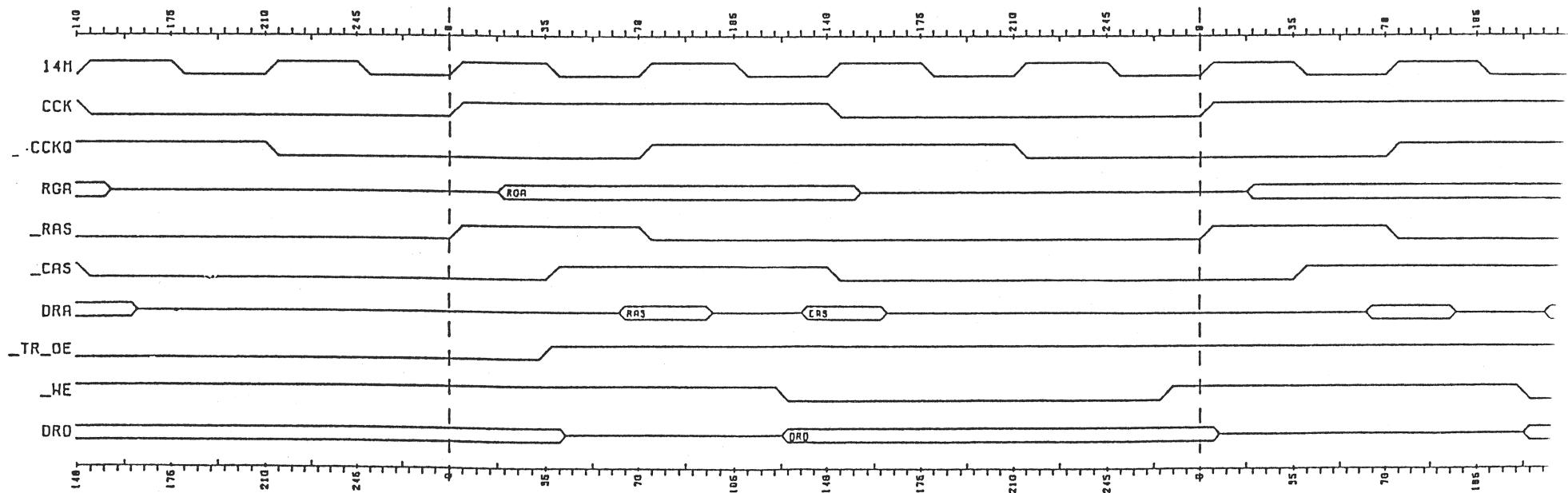
PAGE MODE DRAM READ CYCLE



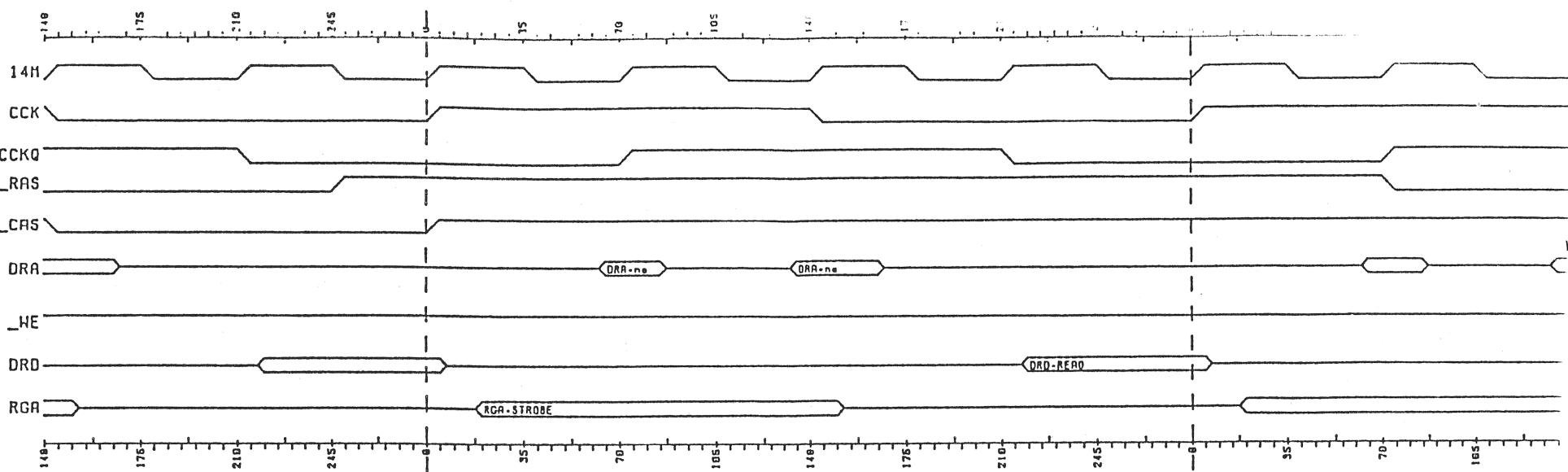
PAGE MODE DRAM WRITE CYCLE



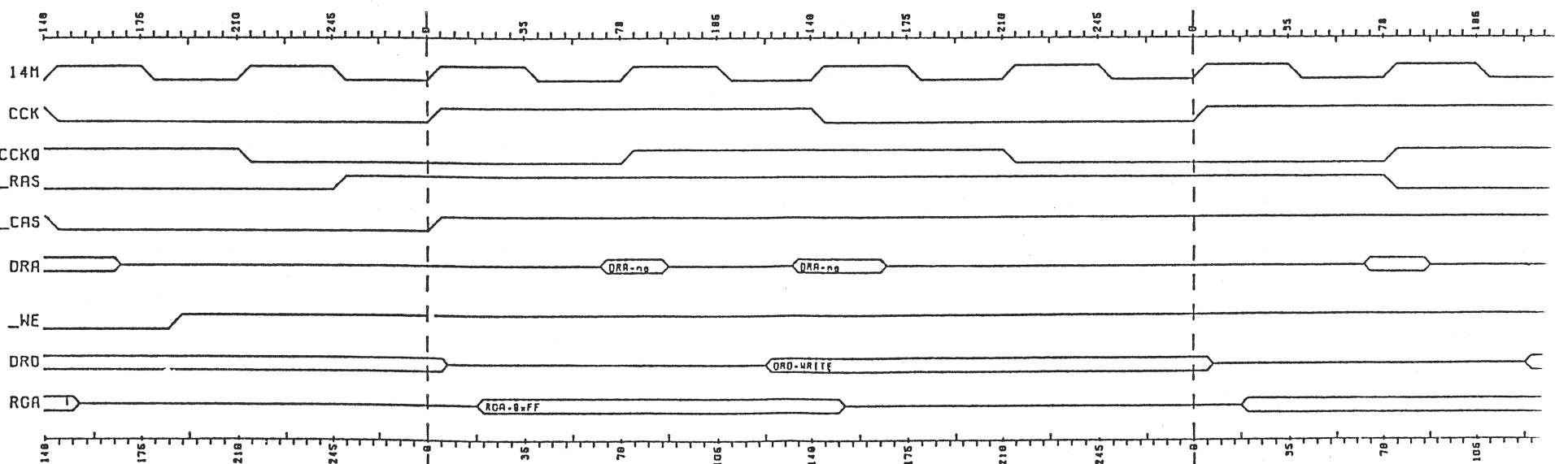
REVISED DRAM READ CYCLE



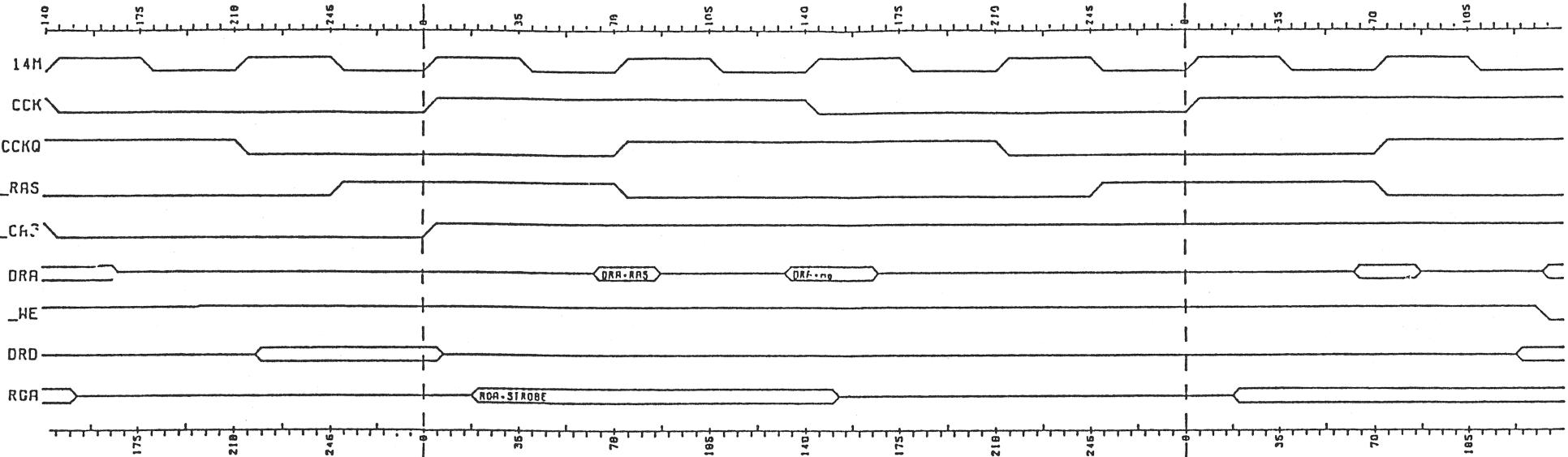
REVISED DRAM WRITE CYCLE



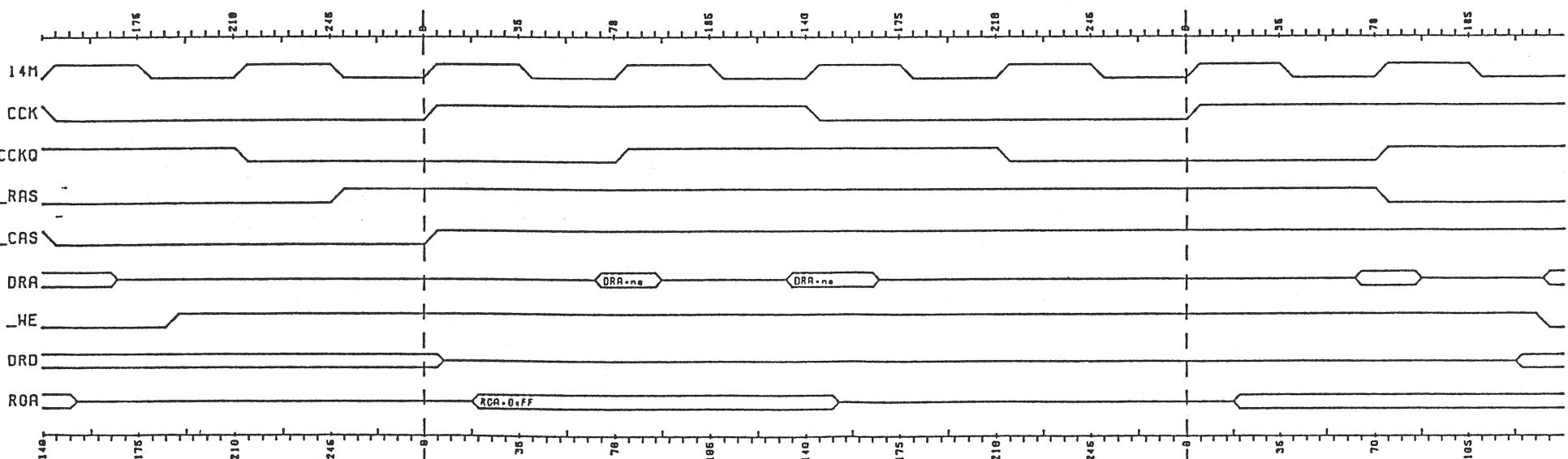
TRADITIONAL REGISTER READ CYCLE



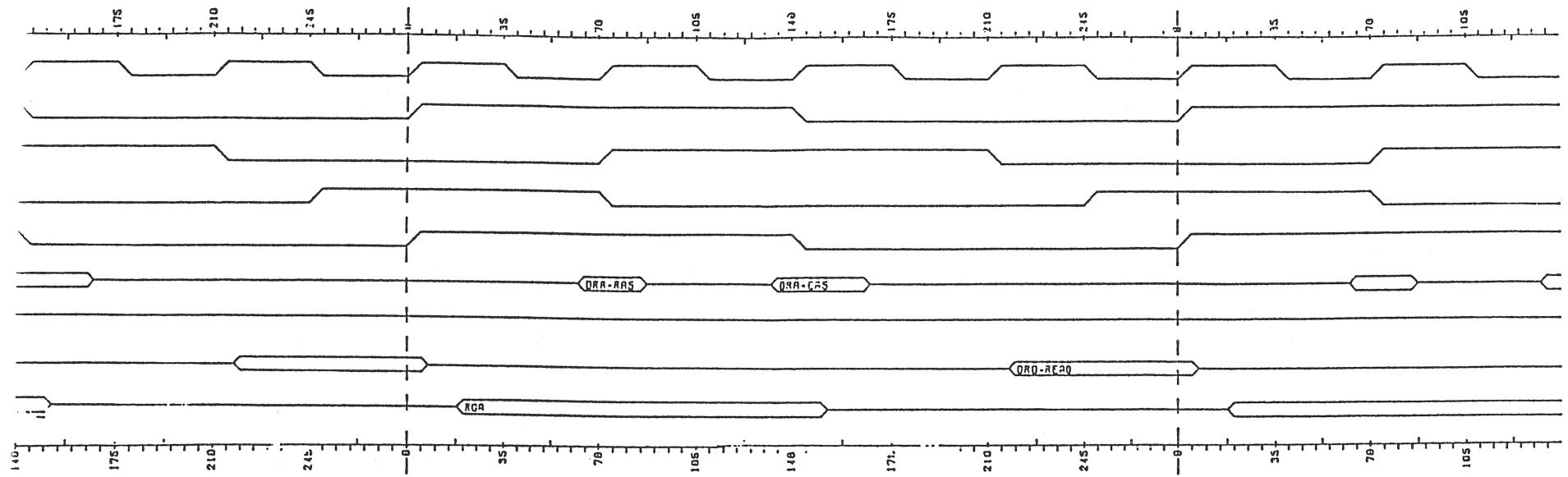
TRADITIONAL REGISTER WRITE CYCLE



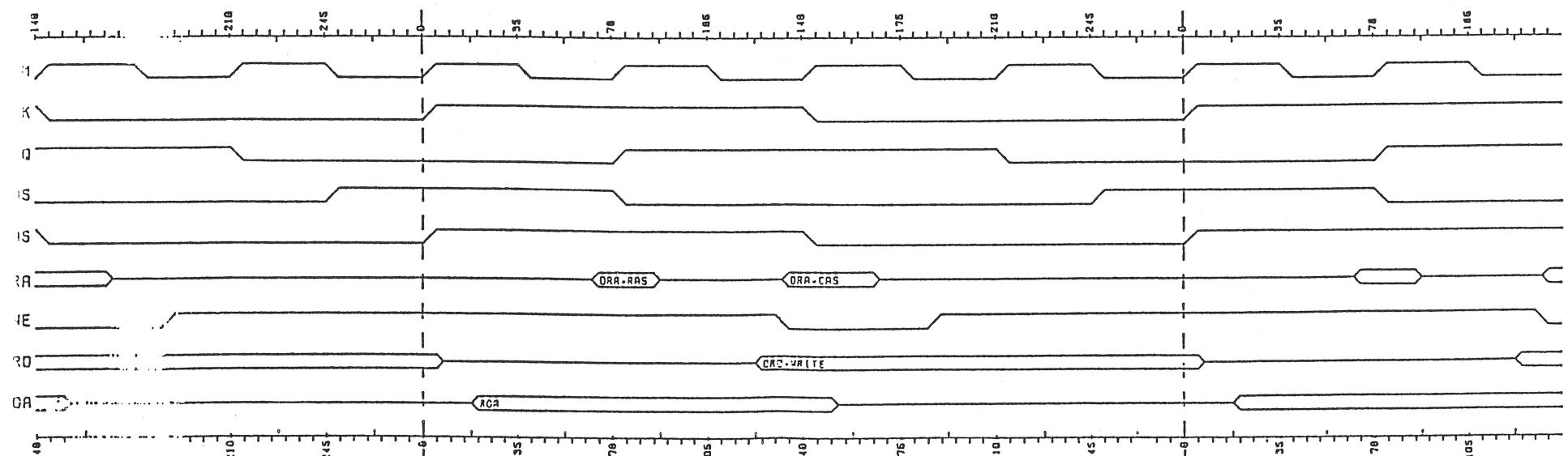
TRADITIONAL RAS-ONLY REFRESH



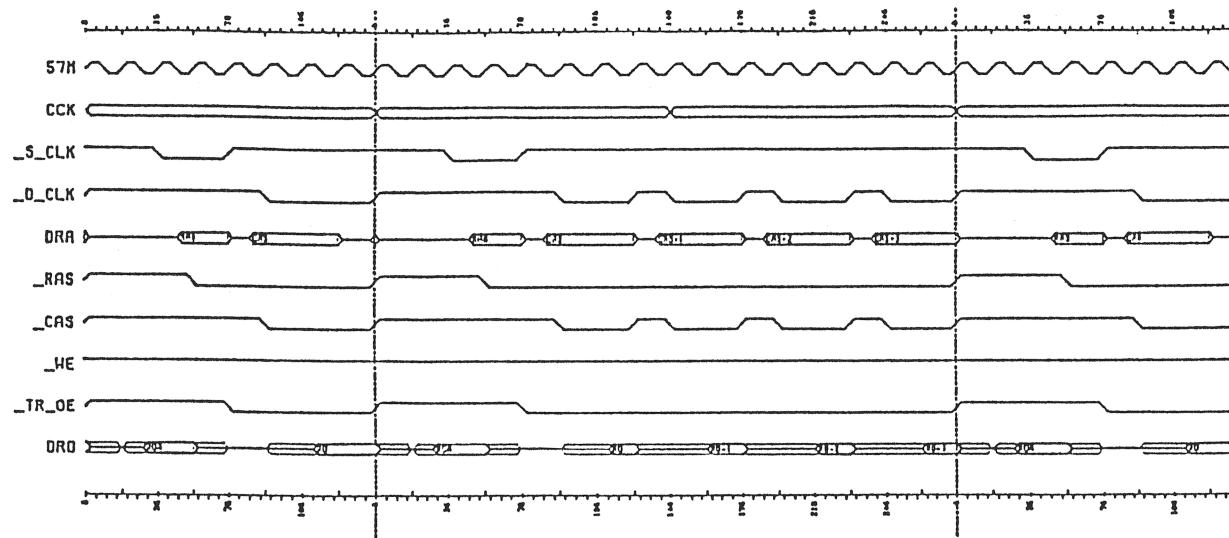
TRADITIONAL NULL CYCLE



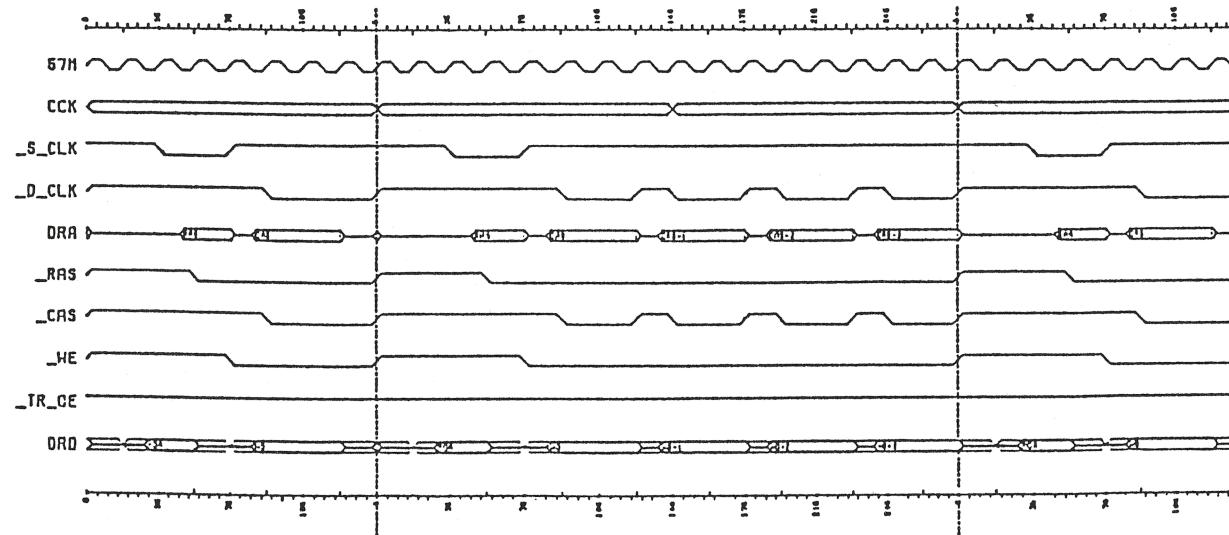
TRADITIONAL DRAM READ CYCLE



TRADITIONAL DRAM WRITE CYCLE

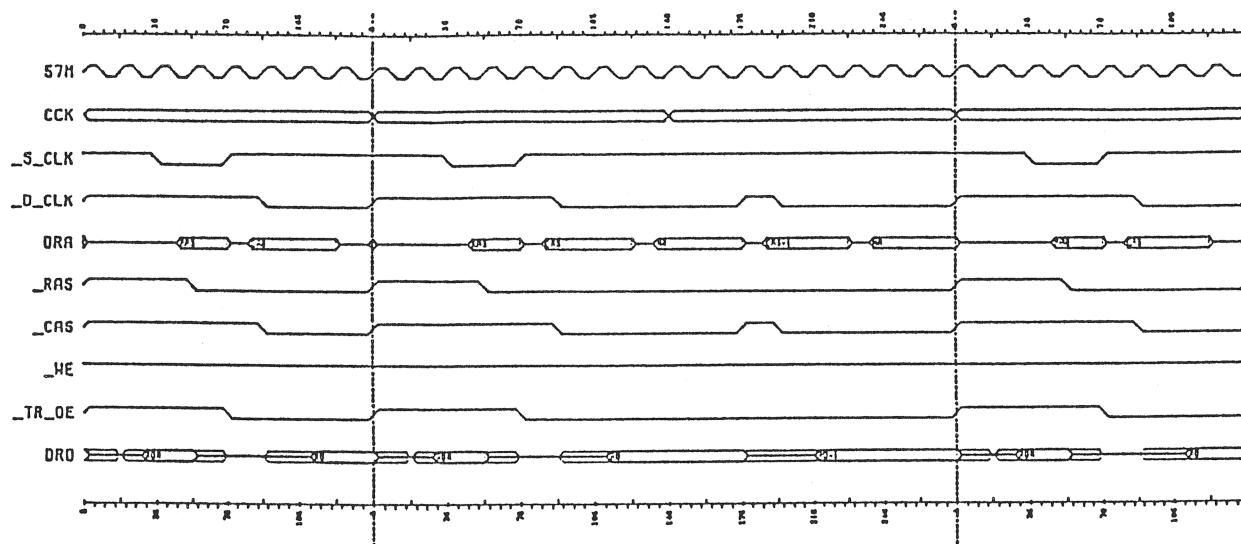


READ CYCLE (QUAD CAS)

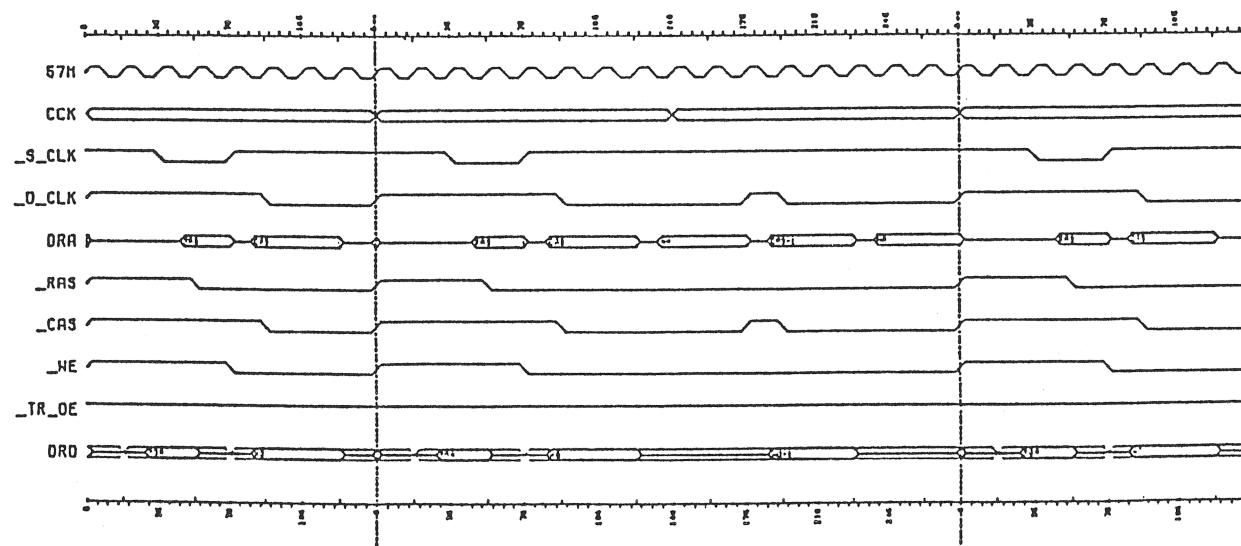


WRITE CYCLE (QUAD CAS)

A+ Chip Bus Timing (Double Speed) 03/31/92

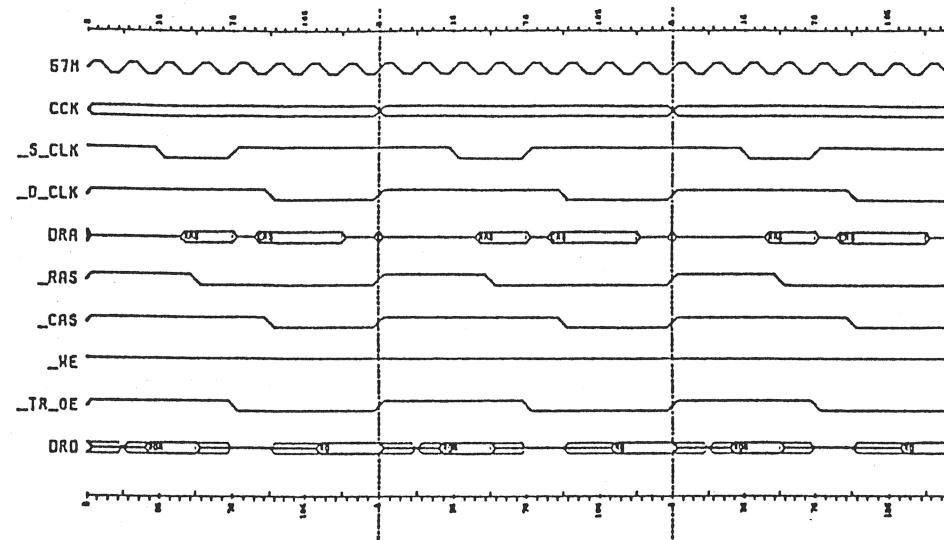


READ CYCLE (DOUBLE CAS)

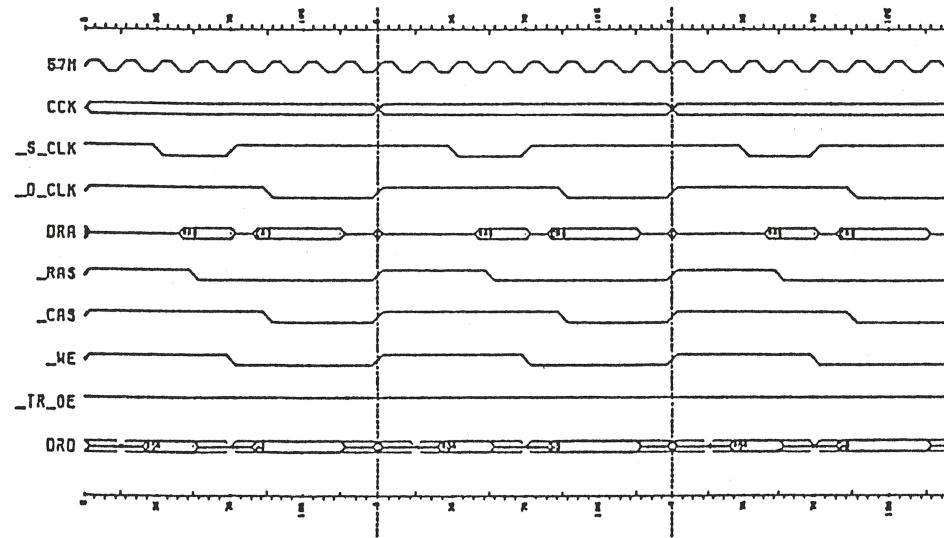


WRITE CYCLE (DOUBLE CAS)

A+ Chip Bus Timing (Double Speed) 03/31/92

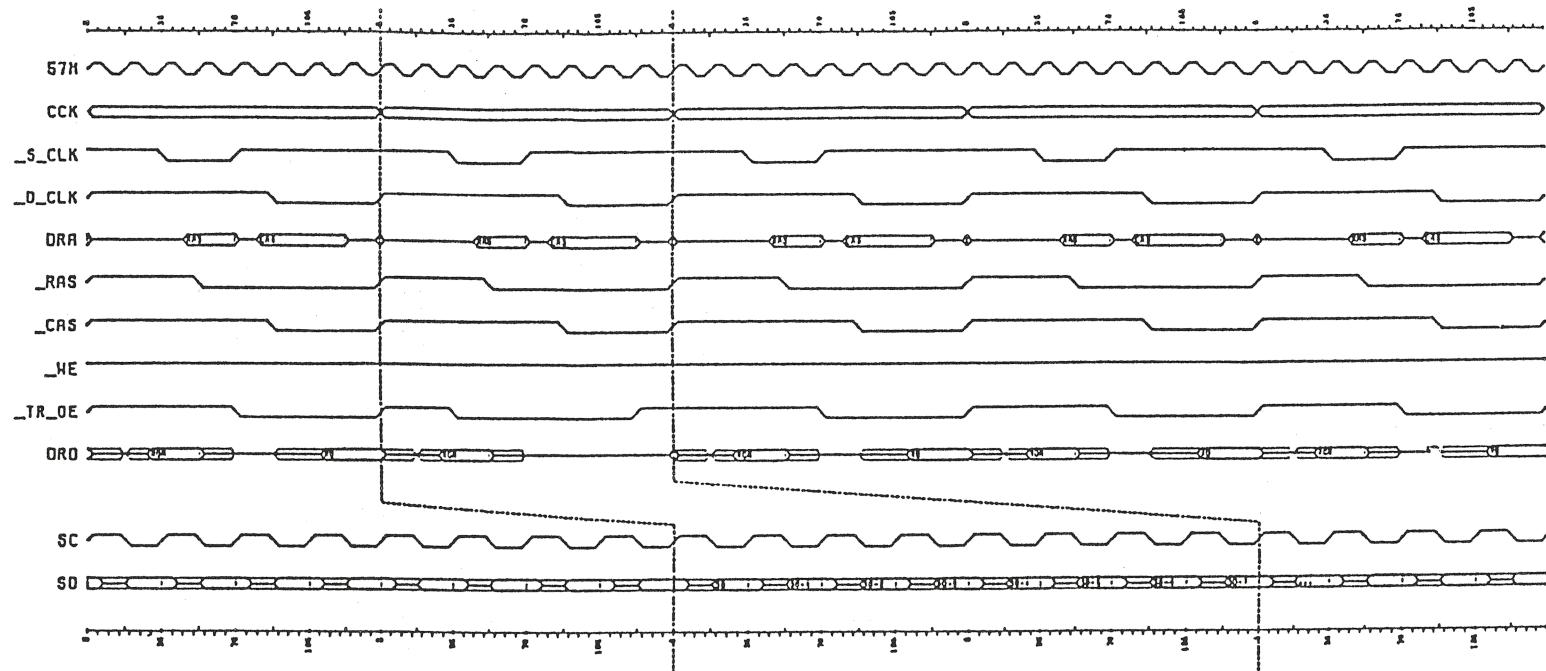


READ CYCLE (SINGLE CAS)

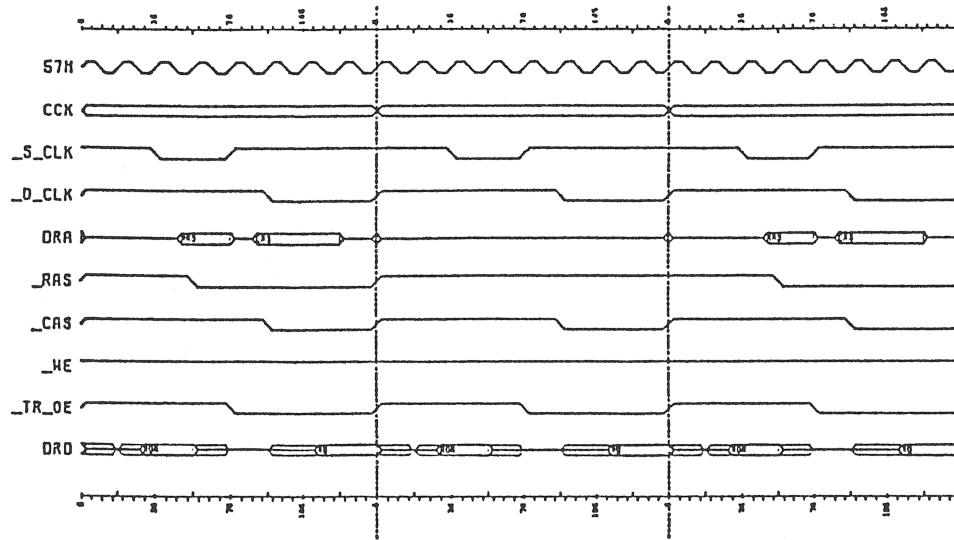


WRITE CYCLE (SINGLE CAS)

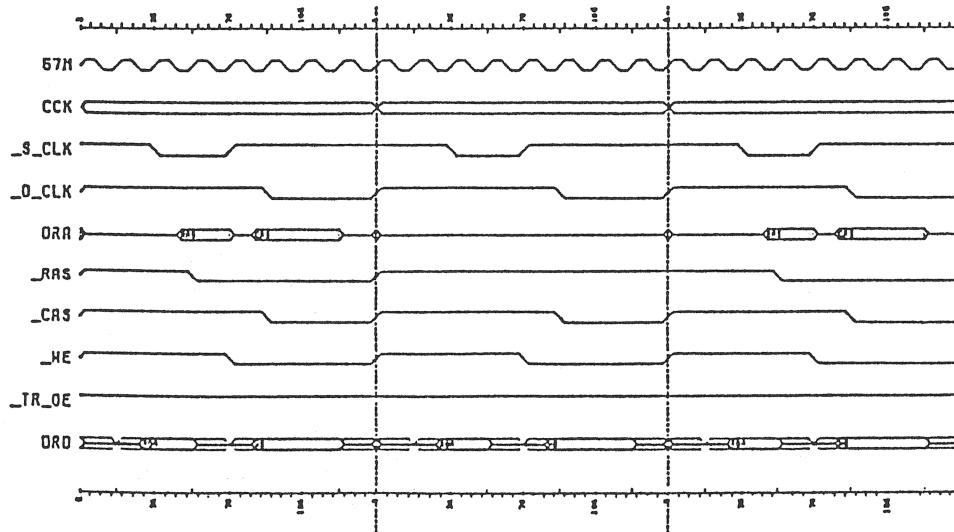
A+ Chip Bus Timing (Double Speed) 03/31/92



SHIFFT REGISTER LOAD CYCLE

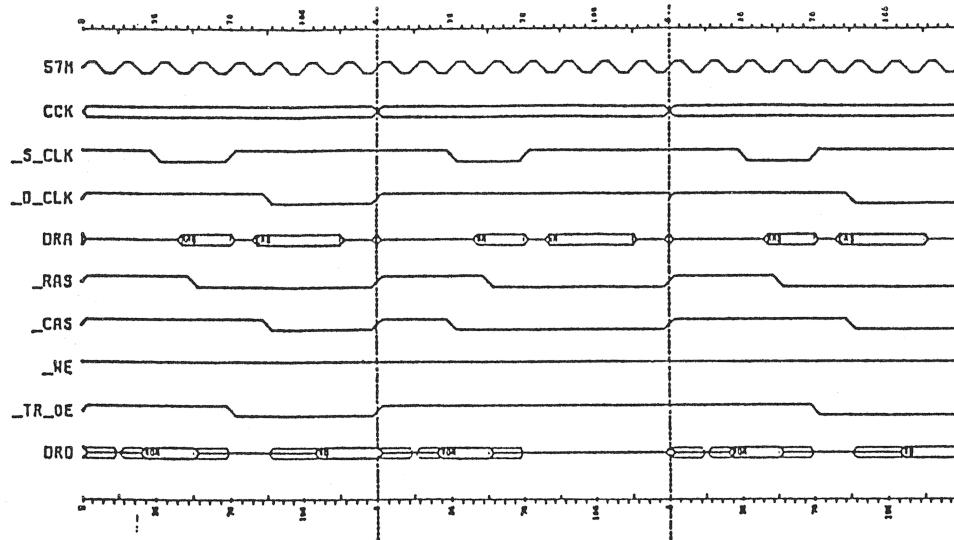


SLOW REGISTER READ

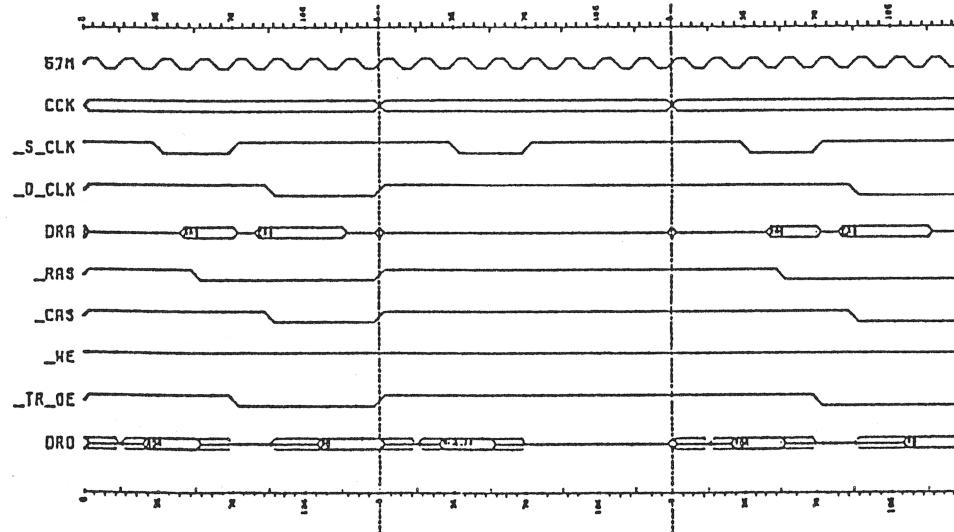


SLOW REGISTER WRITE

□+ Chip Bus Timing (Double Speed) 03/31/92

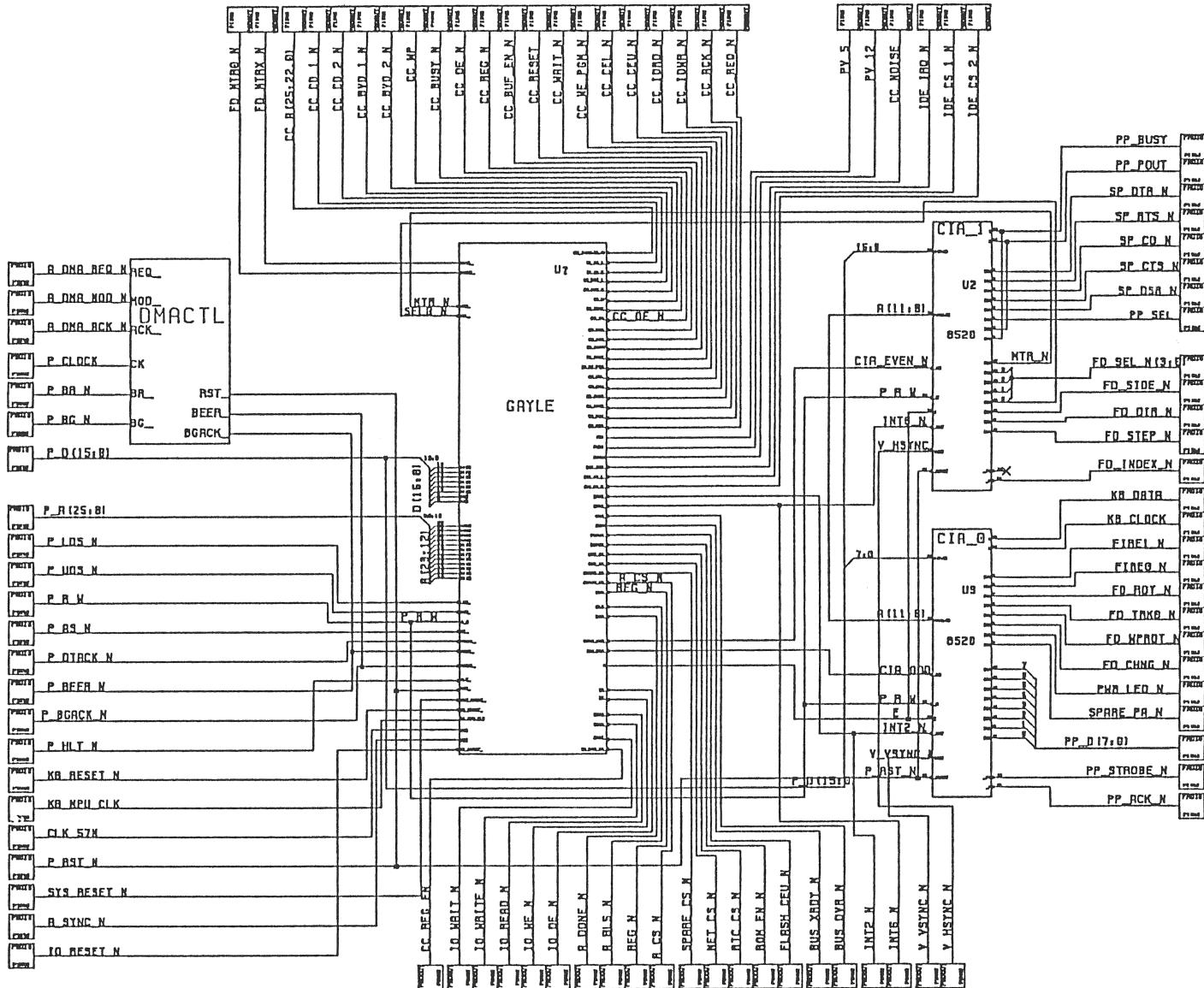


CAS BEFORE RAS REFRESH

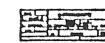
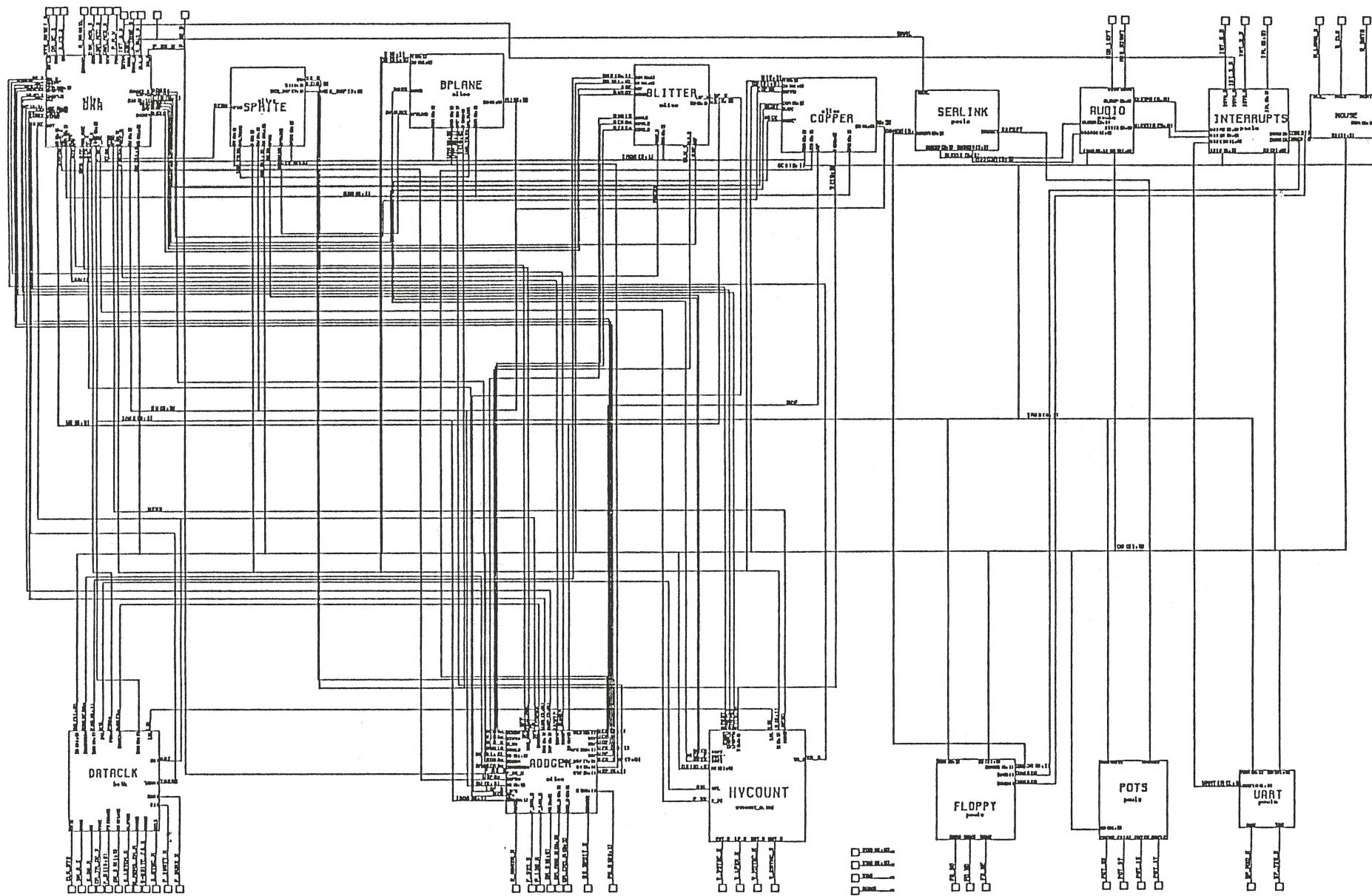


NULL CYCLE

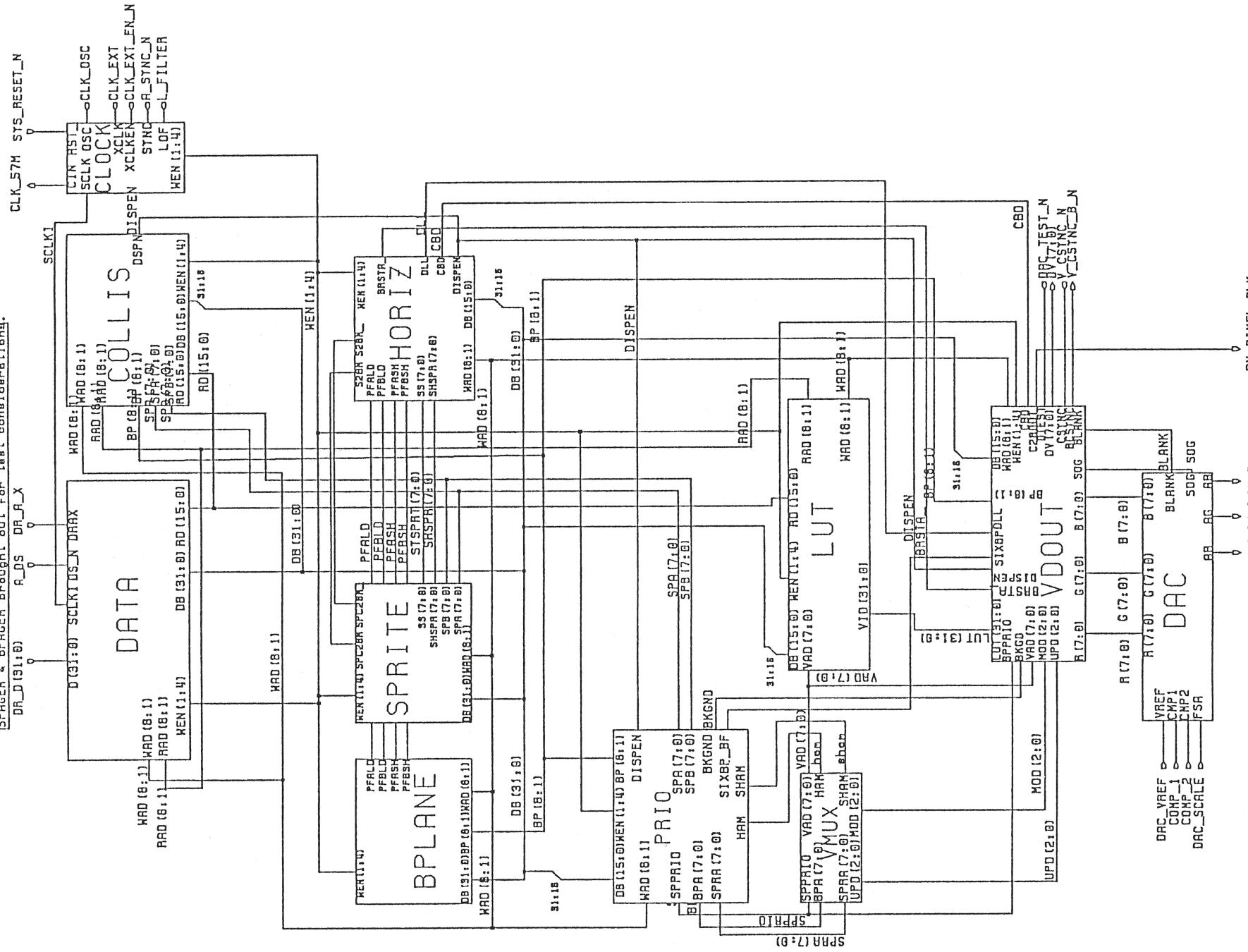
A+ Chip Bus Timing (Double Speed) 03/31/92



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