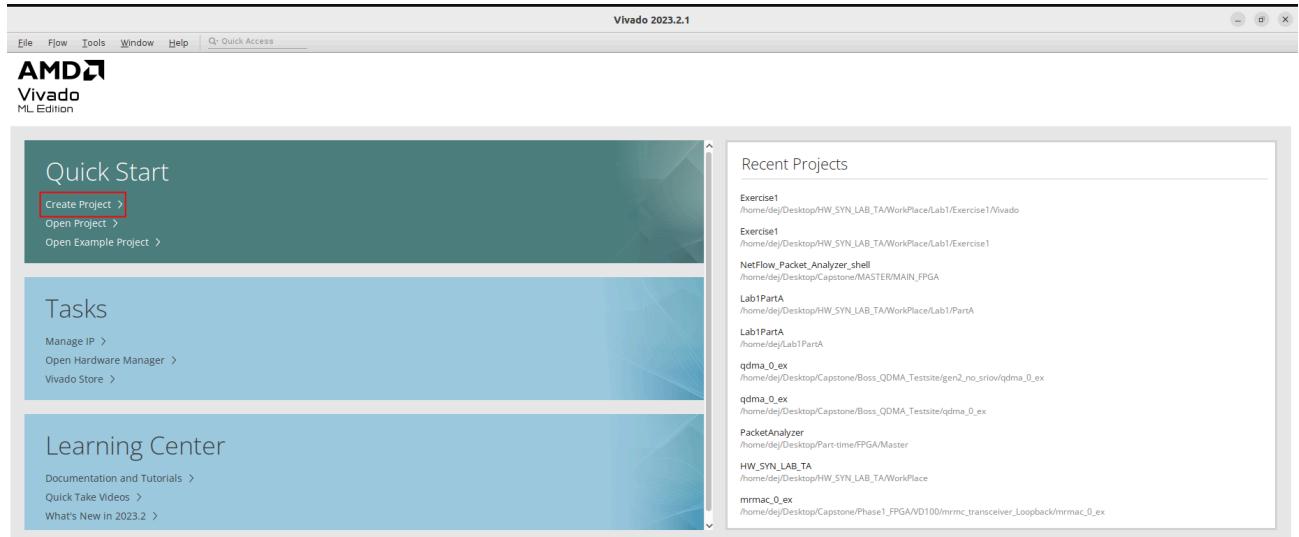
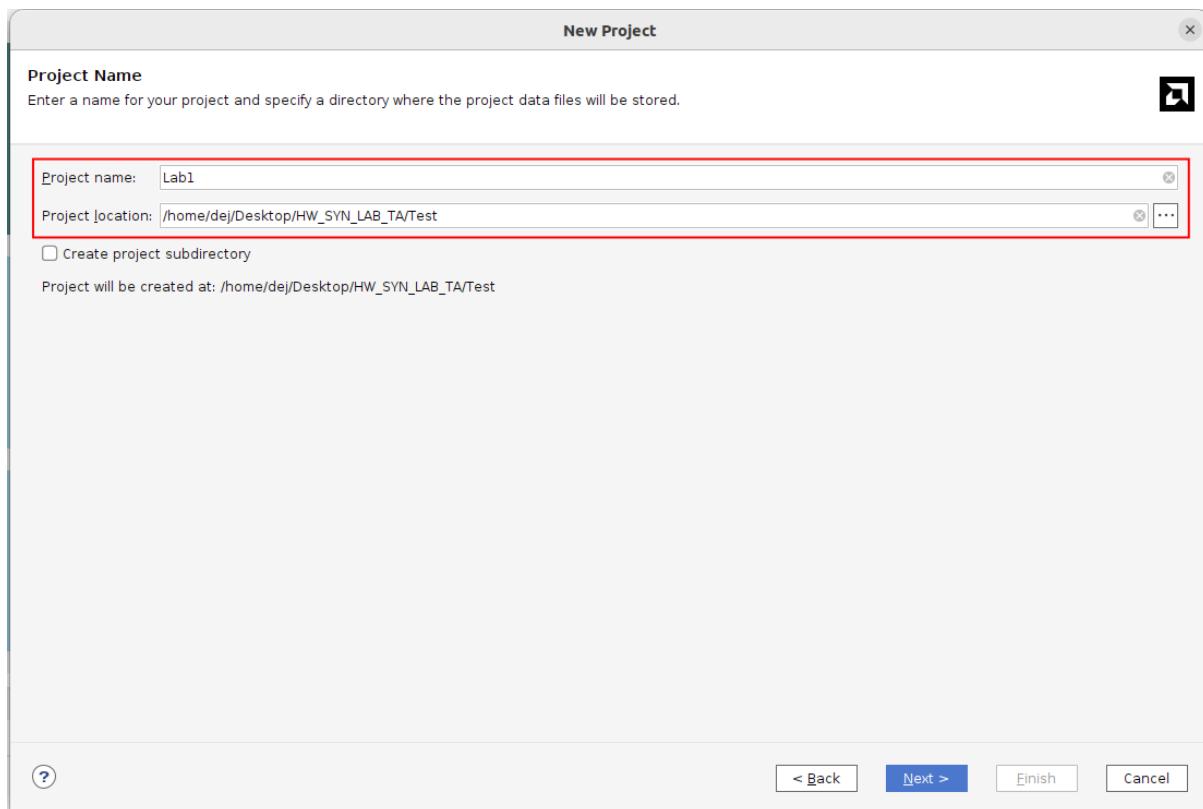


# Project Setup

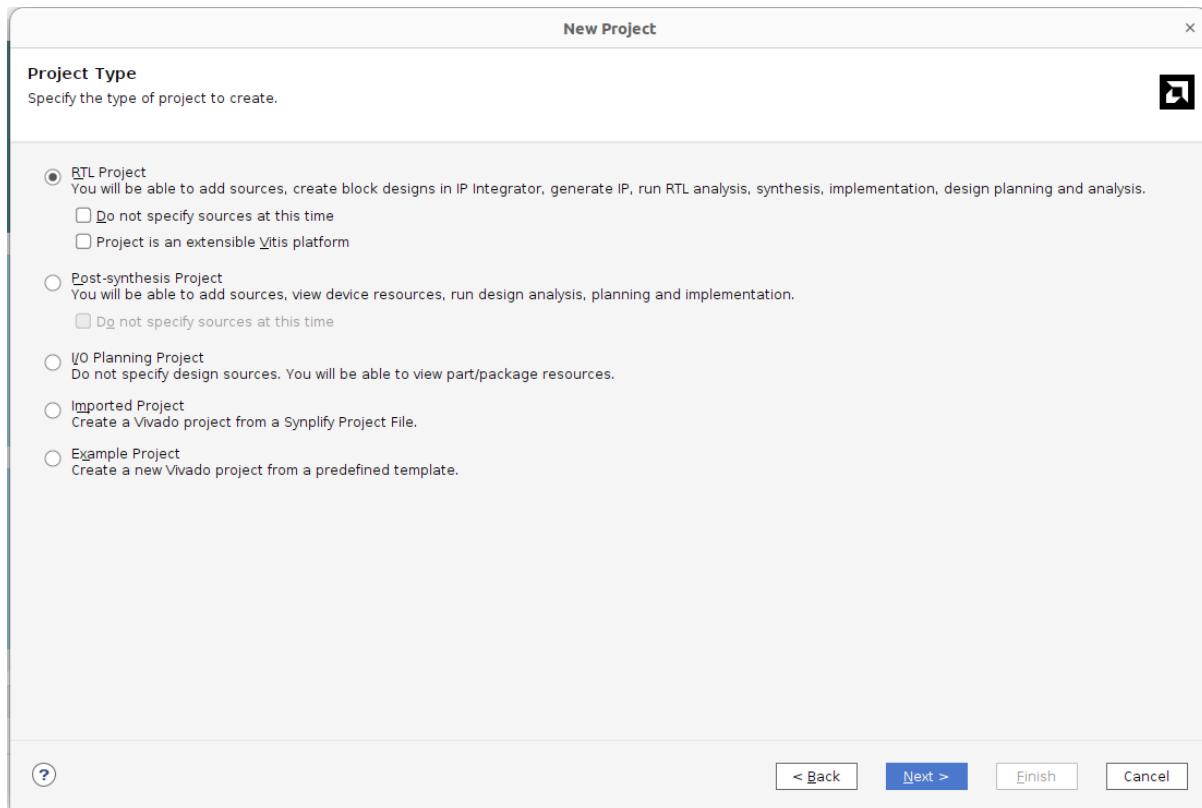
1. Download and extract the lab zip file from MCV or clone from the github  
<https://github.com/2110363-HW-SYN-LAB/lab>
2. Open Vivado and create a new project.



3. Enter the project name and project path.

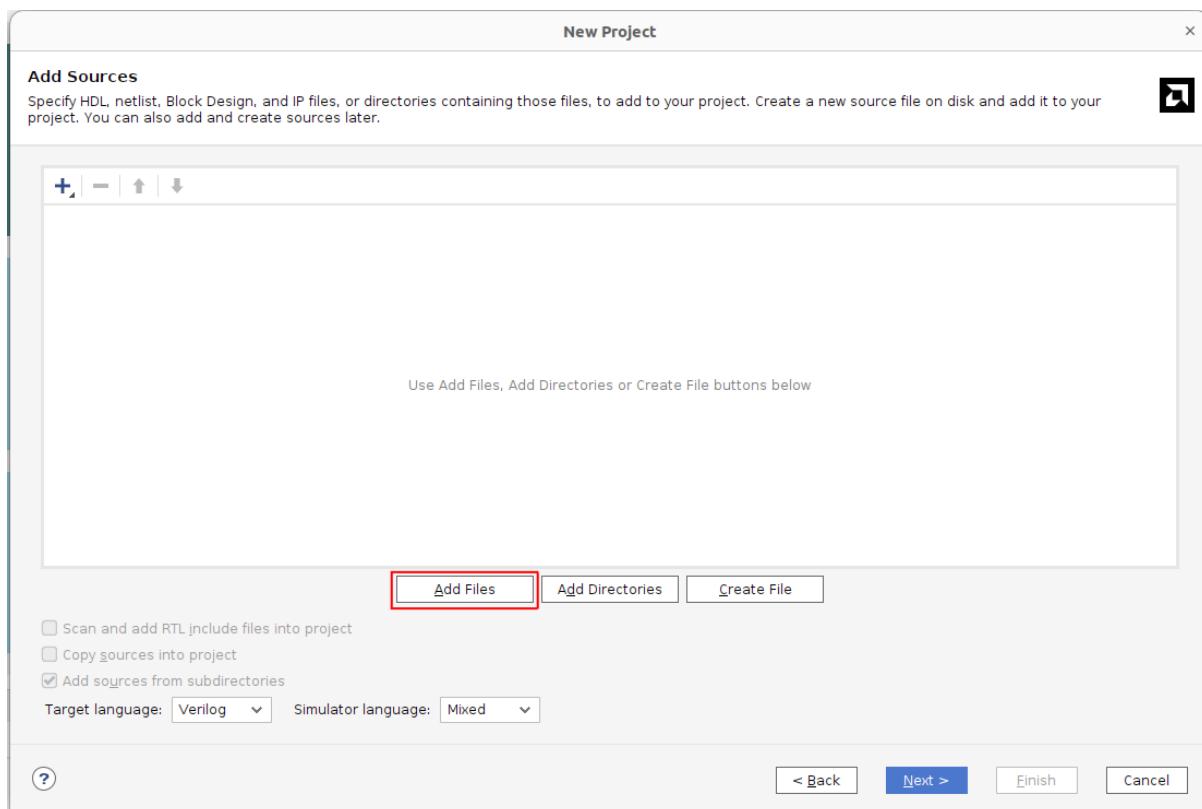


#### 4. Select Project type “RTL Project” then click next.

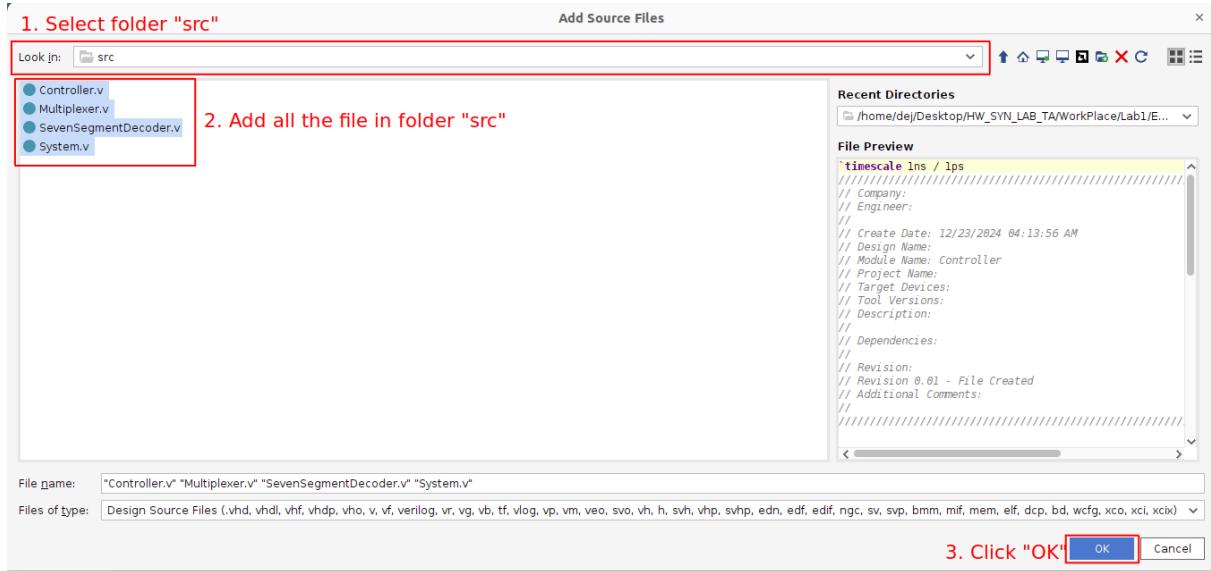


#### 5. On the Add Sources.

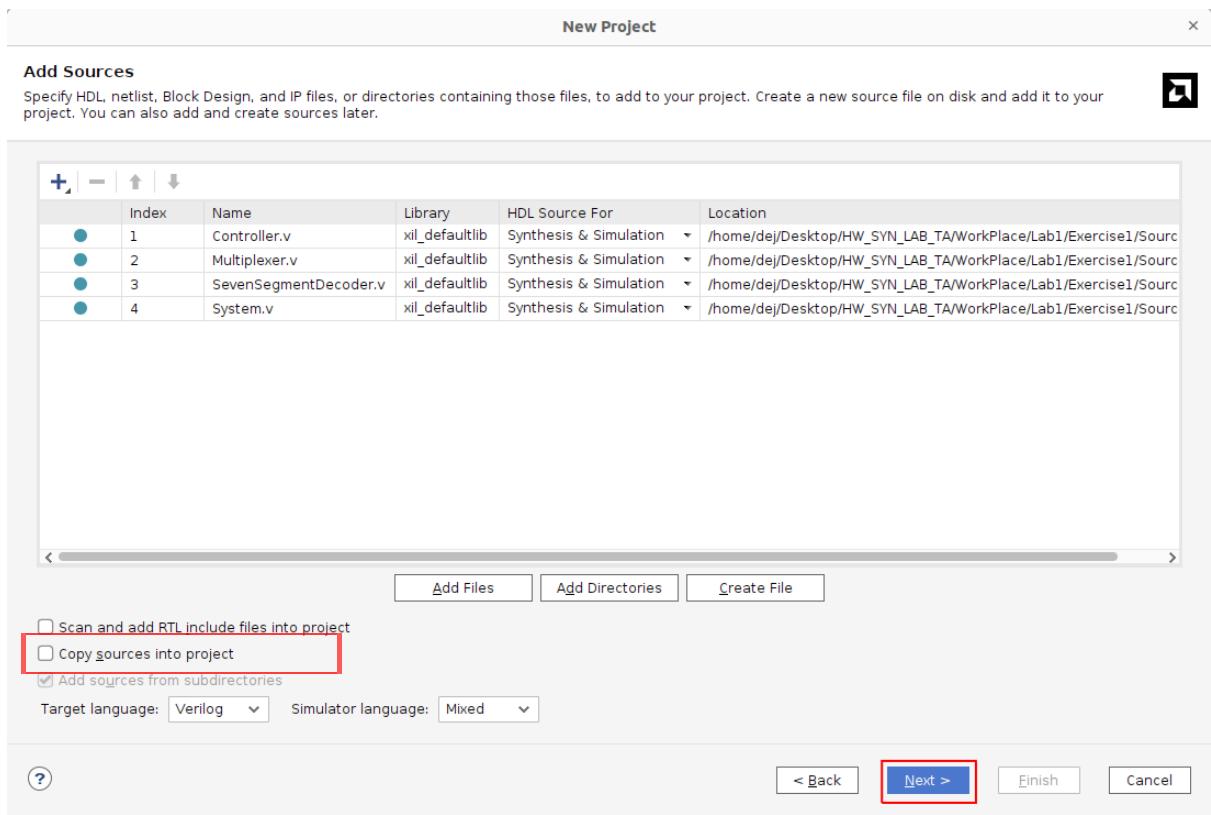
##### a. Click “Add Files”



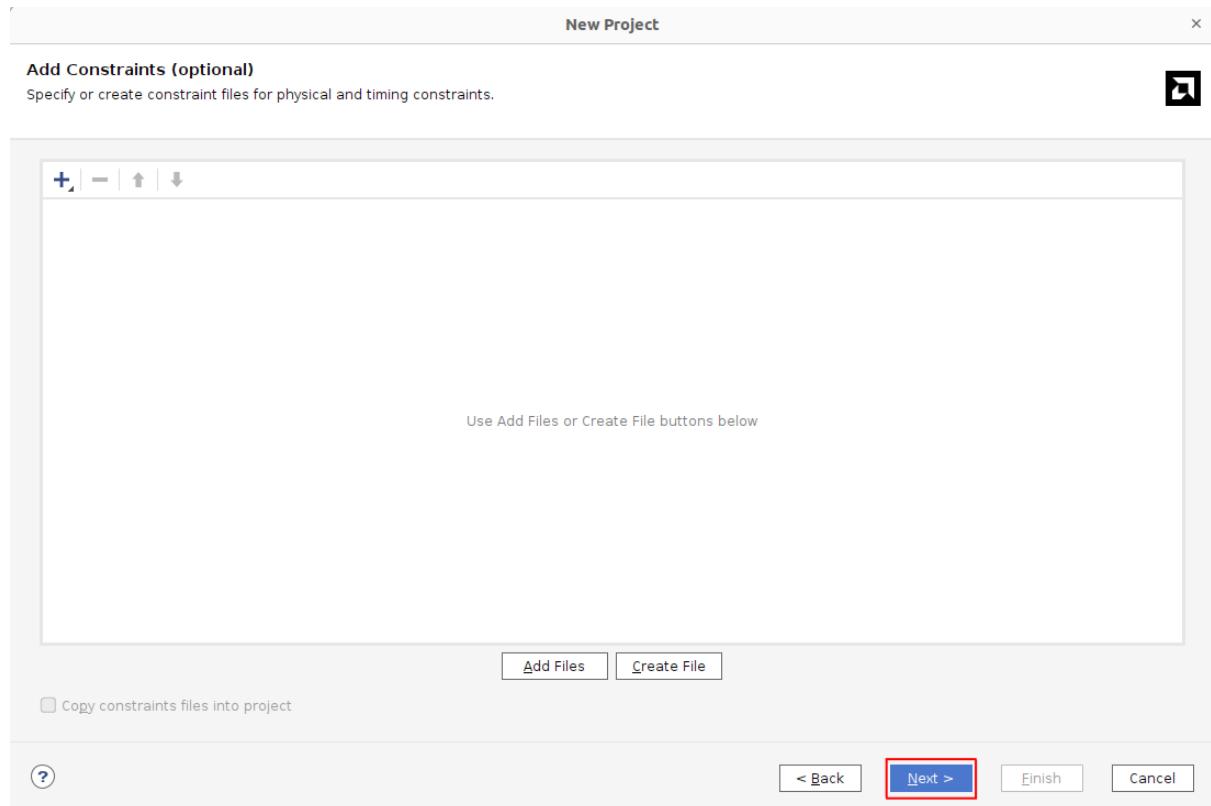
b. Add all the files from the folder src.



c. Please make sure that the “Copy sources into project” checkbox is off, then click “next”.



## 6. On the Add Constraints, click next.



## 7. On the Default Part.

### a. Click “Boards”.

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	BUFGs	Gb Transceivers	Temperature:	Static power:
xc7vx415tffv1157-1	1157	600	257600	515200	880	0	2160	32	20	All	All
xc7vx415tffv1158-3	1158	350	257600	515200	880	0	2160	32	48	C	C
xc7vx415tffv1158-2	1158	350	257600	515200	880	0	2160	32	48	C	C
xc7vx415tffv1158-2L	1158	350	257600	515200	880	0	2160	32	48	C	C
xc7vx415tffv1158-1	1158	350	257600	515200	880	0	2160	32	48	C	C
xc7vx415tffv1927-3	1927	600	257600	515200	880	0	2160	32	48	C	C
xc7vx415tffv1927-2	1927	600	257600	515200	880	0	2160	32	48	C	C
xc7vx415tffv1927-2L	1927	600	257600	515200	880	0	2160	32	48	C	C
xc7vx415tffv1927-1	1927	600	257600	515200	880	0	2160	32	48	C	C
xc7vx485tffg1157-3	1157	600	303600	607200	1030	0	2800	32	20	C	C
xc7vx485tffg1157-2	1157	600	303600	607200	1030	0	2800	32	20	C	C
xc7vx485tffg1157-2L	1157	600	303600	607200	1030	0	2800	32	20	C	C
xc7vx485tffg1157-1	1157	600	303600	607200	1030	0	2800	32	20	C	C
xc7vx485tffg1158-3	1158	350	303600	607200	1030	0	2800	32	48	C	C

- b. Search for “Basys3” then select it. After that click “Next”.

The screenshot shows the 'New Project' dialog with the 'Default Part' tab selected. The search bar at the top contains 'Search: Basys3 (2 matches)'. Below the search bar, a table lists two entries: 'Basys3' and 'Basys3'. The entry 'Basys3' is highlighted with a red box. The table columns are: Display Name, Preview, Status, Vendor, File Version, and Part. The 'Basys3' row shows 'Installed' status, vendor 'digilentinc.com', file version '1.2', and part 'xc7a35tcpg236-1'. At the bottom right of the dialog, the 'Next >' button is highlighted with a red box.

1. Search for "Basys3"

2. Select "Basys3" Board

3. Click "Next"

8. Click “Finish”

The screenshot shows the 'New Project Summary' dialog. It displays the following information:

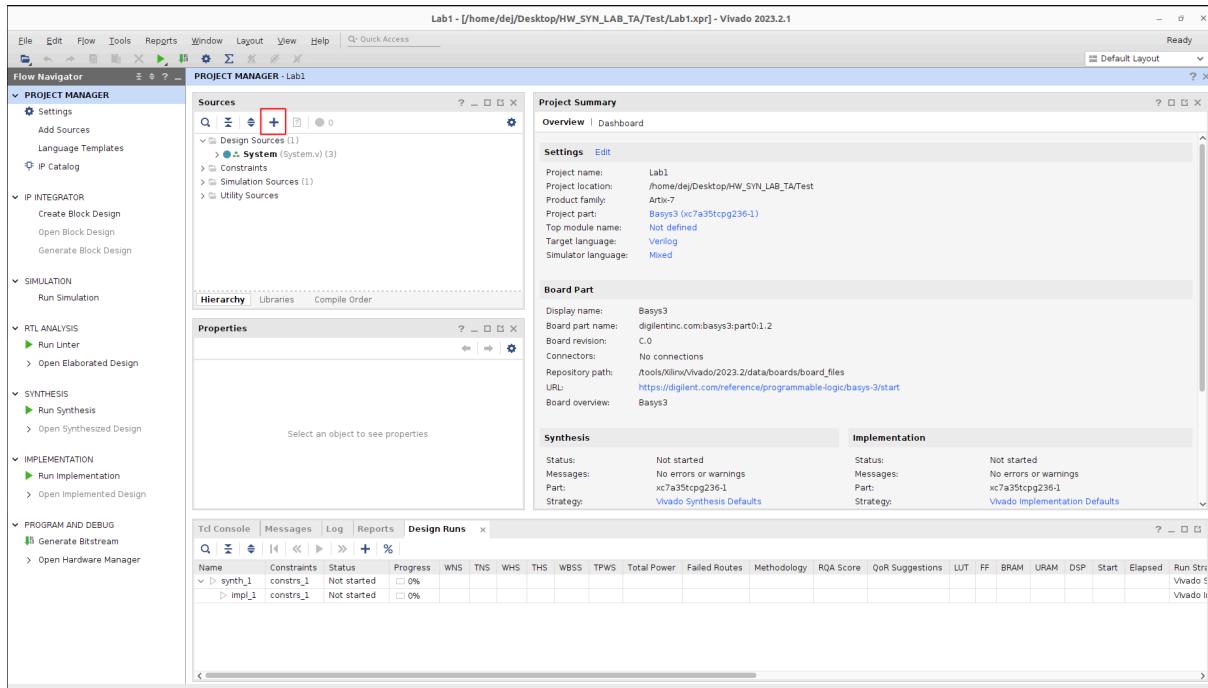
- AMD Vivado ML Edition**
- A new RTL project named 'Lab1' will be created.
- 4 source files will be added.
- No constraints files will be added. Use Add Sources to add them later.
- The default part and product family for the new project:
  - Default Board: Basys3
  - Default Part: xc7a35tcpg236-1
  - Family: Artix-7
  - Package: cpg236
  - Speed Grade: -1

To create the project, click Finish

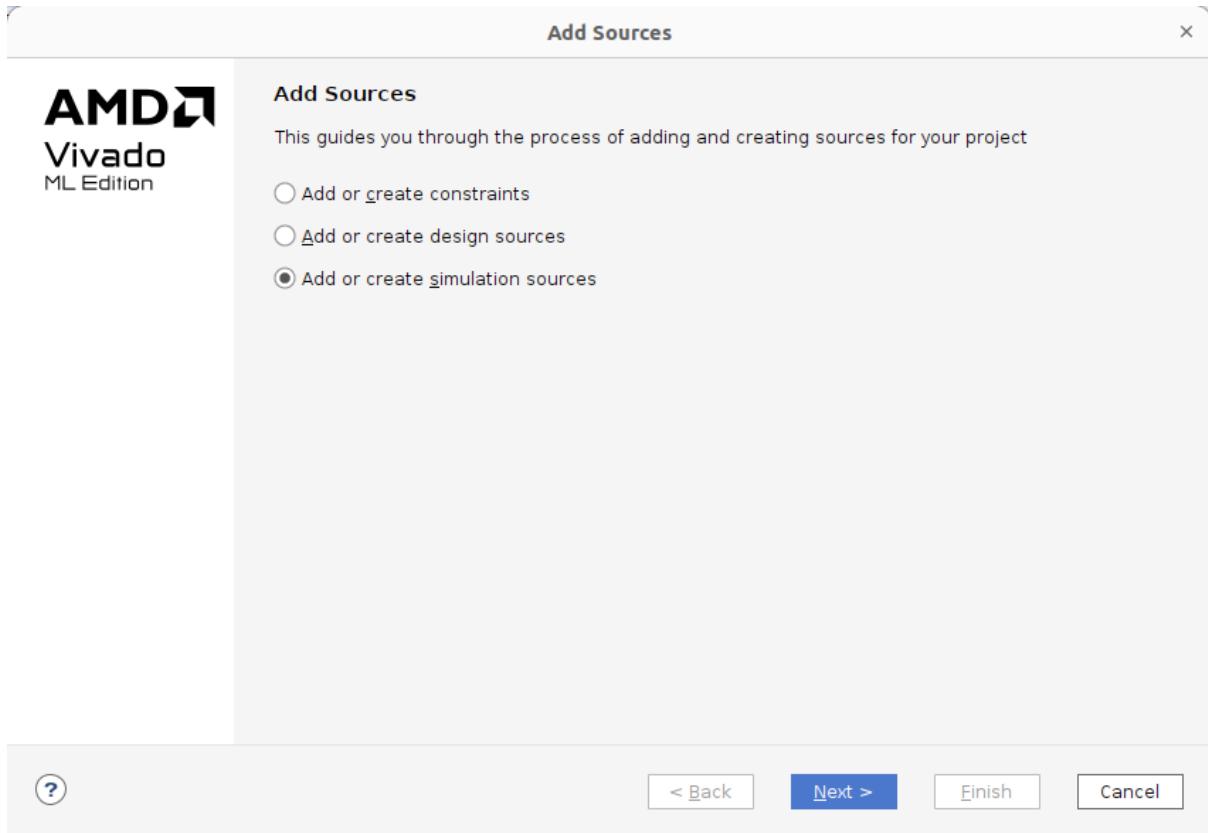
At the bottom right, the 'Finish' button is highlighted with a red box.

## 9. Add a Xilinx Testbench file.

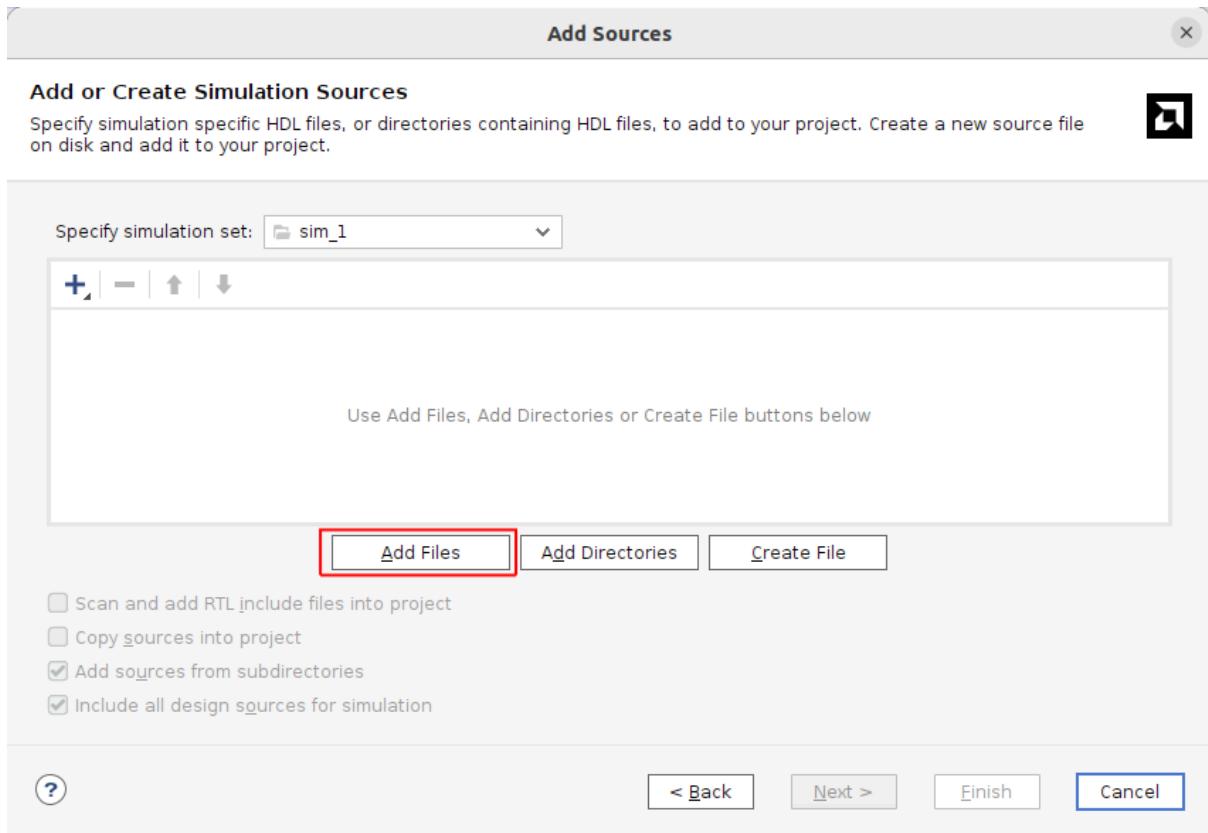
- Click the plus sign.



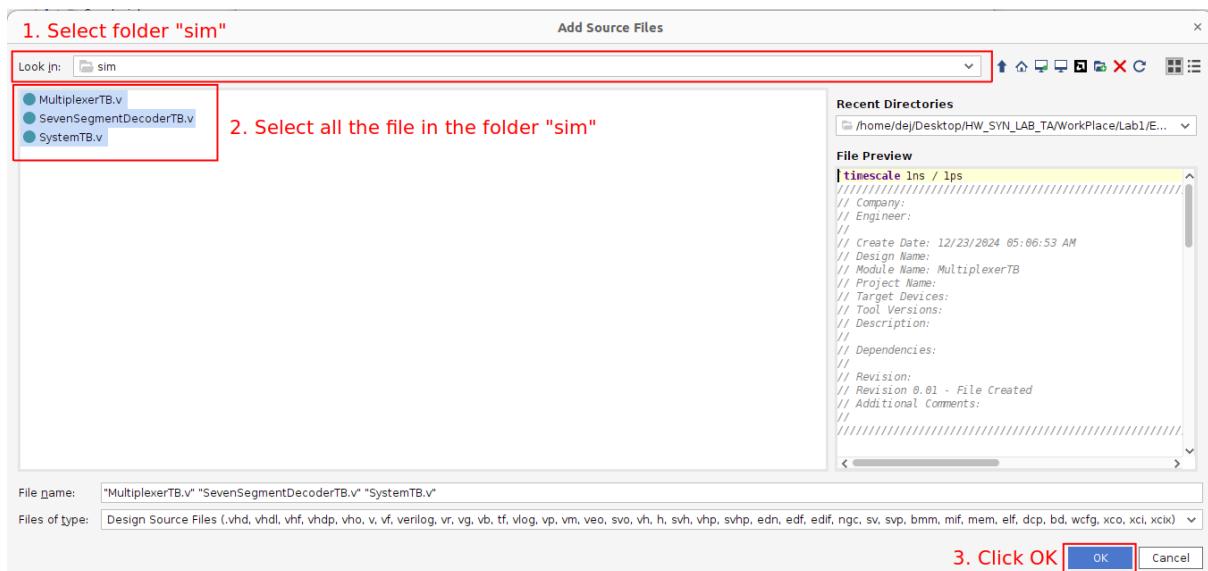
- Select Add or create simulation sources.



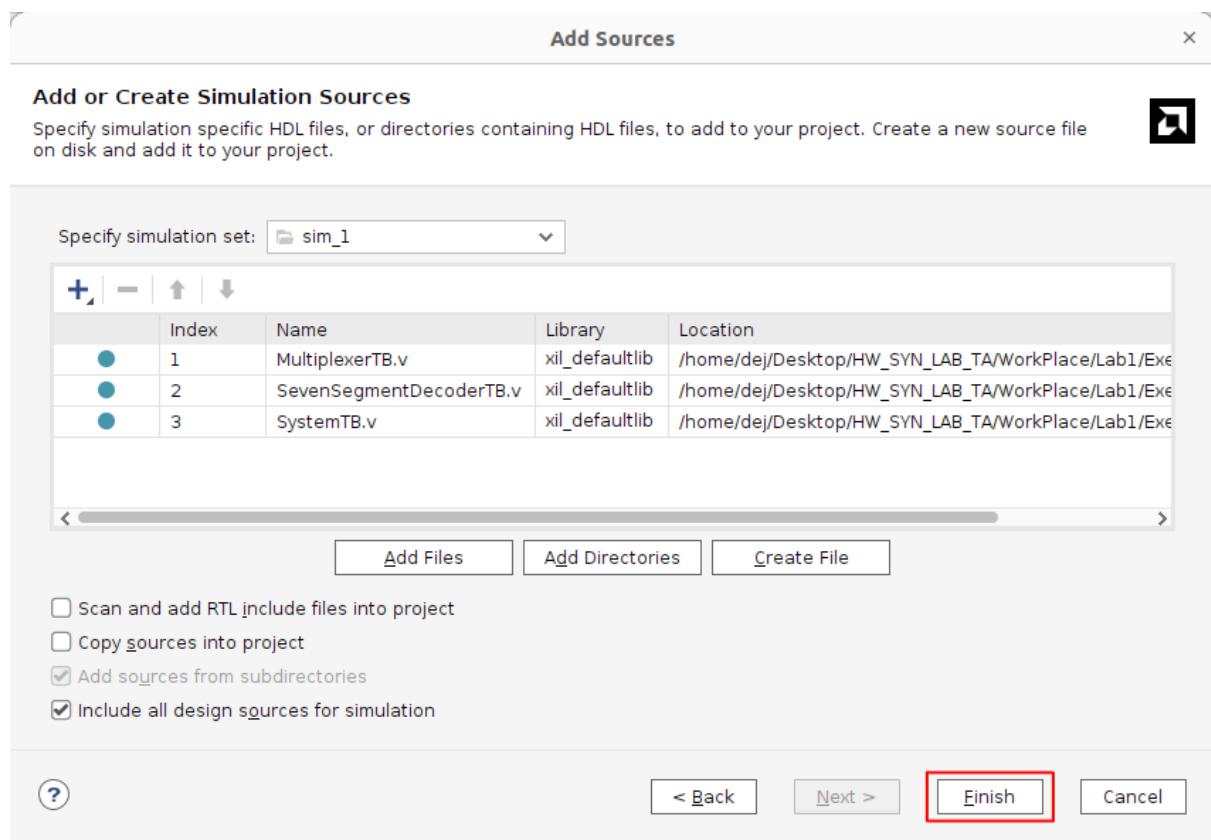
c. Click “Add files”.



d. Add all the files from the folder sim.

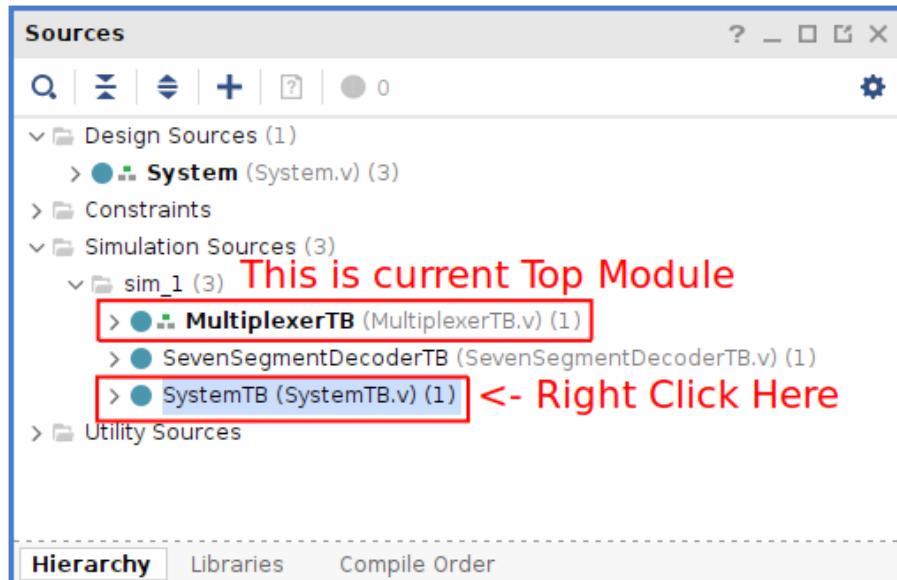


e. Click “Finish”.

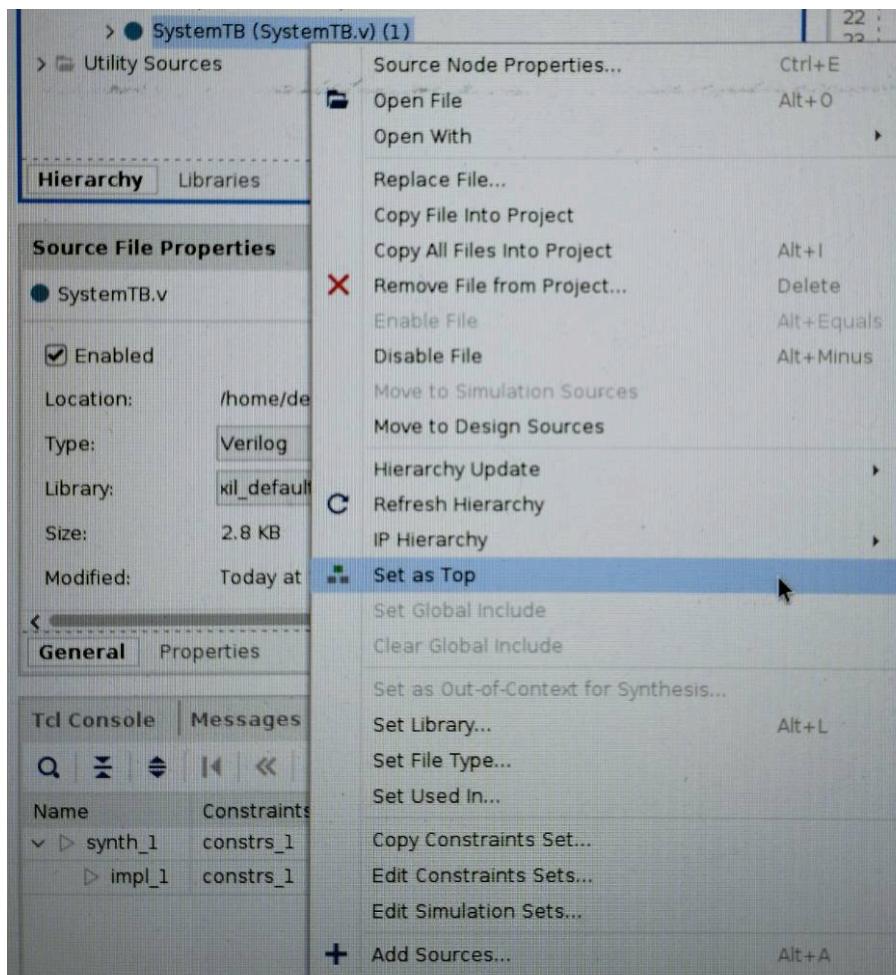


# Running Xilinx Testbench

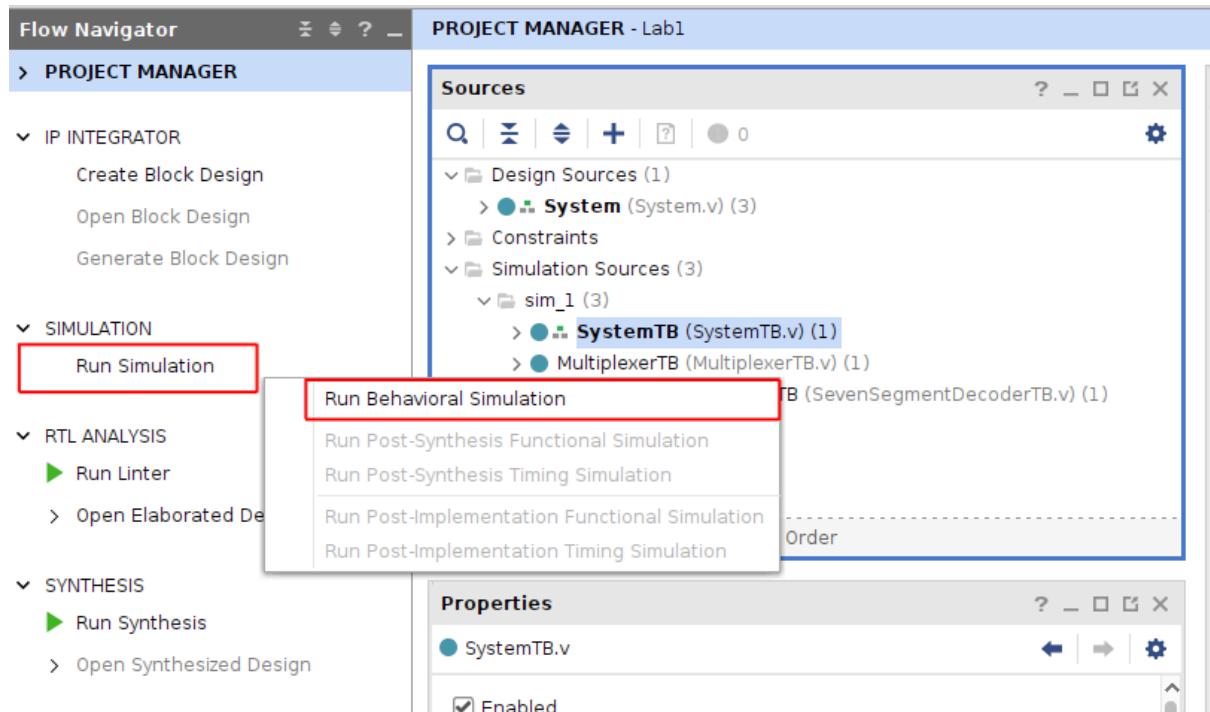
1. Select the Testbench file you want to test.
  - a. right click on that file.



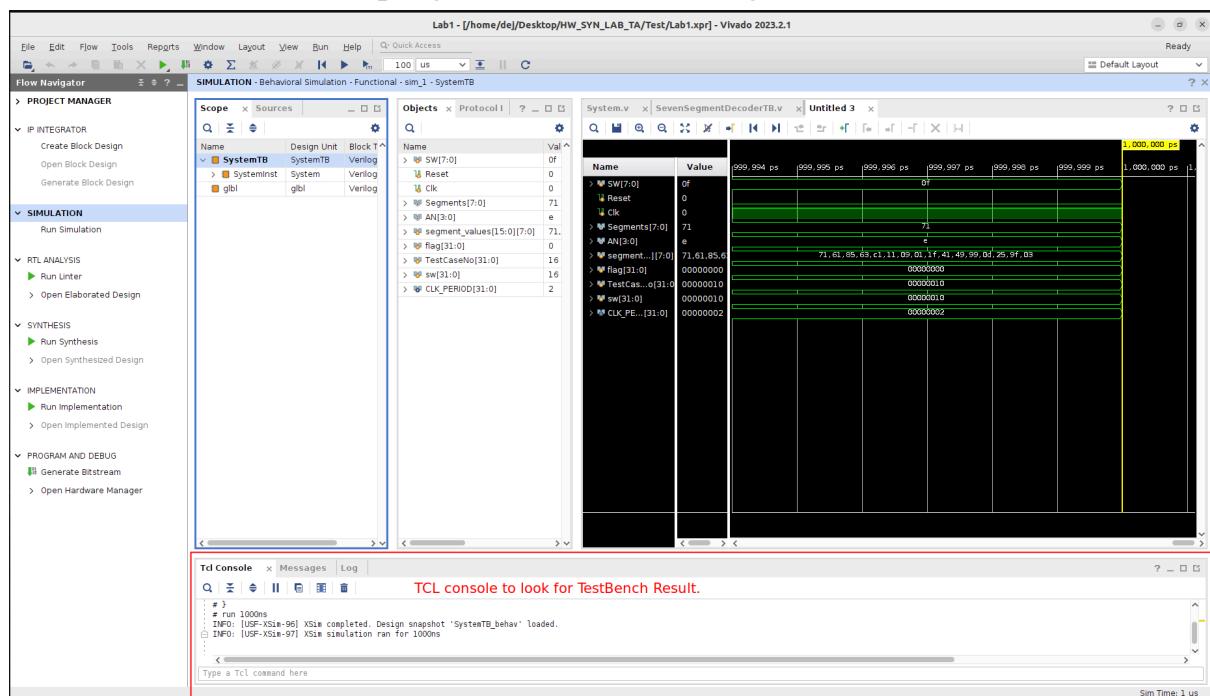
- b. select “Set as Top”.



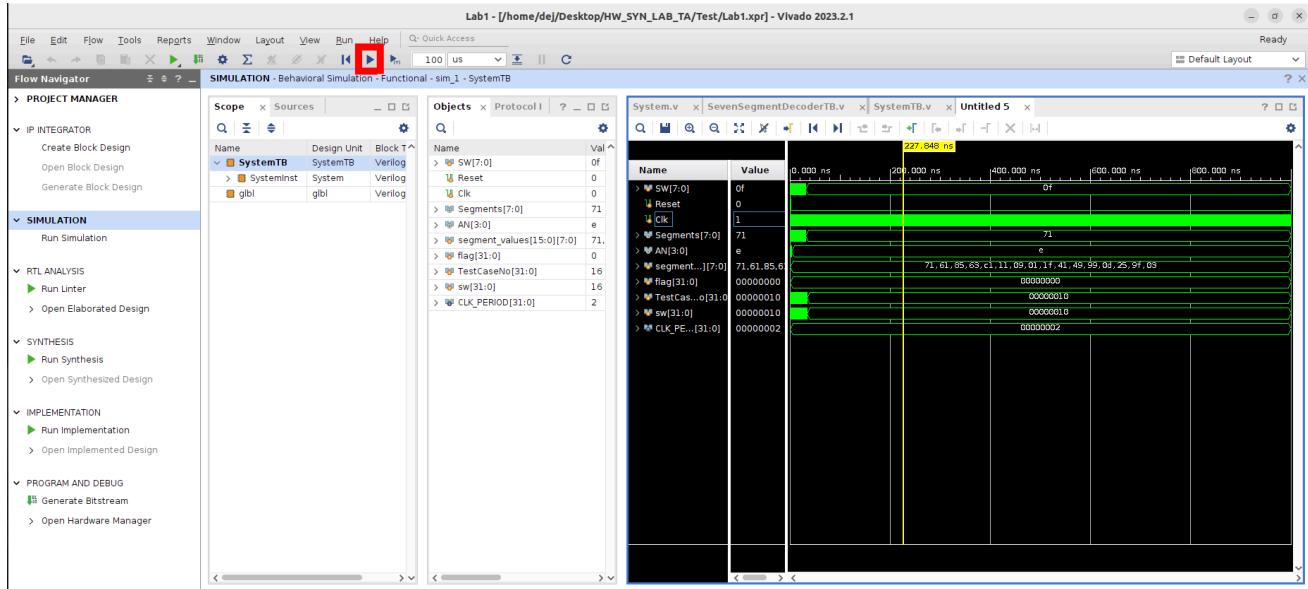
2. Click on the “Run Simulation”.
- a. Click “Run Behavioral Simulation”



- b. wait for the program to finish running the simulation.



- c. In the case Simulation is too long, the program won't execute the entire Simulation. click the "Run All" to complete the simulation.



### 3. Look at the TCL panel for testbench results.

#### a. Testbench Pass.

```

source SystemTB.tcl
# set curr_wave [current_wave_config]
# if { [string length $curr_wave] == 0 } {
#   if { [llength [get_objects]] > 0} {
#     add_wave /
#     set_property needs_save false [current_wave_config]
#   } else {
#     send_msg_id Add_Wave-1 WARNING "No top level signals found. Simulator will start without a wave window. If you want to open a wave window, run 'add_wave /' in the TCL panel"
#   }
# }
# run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'SystemTB_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
run all
All test cases pass
$finish called at time : 300066 ns : File "/home/dej/Desktop/HW_SYN_LAB_TA/WorkPlace/Lab1/Exercisel/Source/sim/SystemTB.v" Line 104

```

Type a Tcl command here

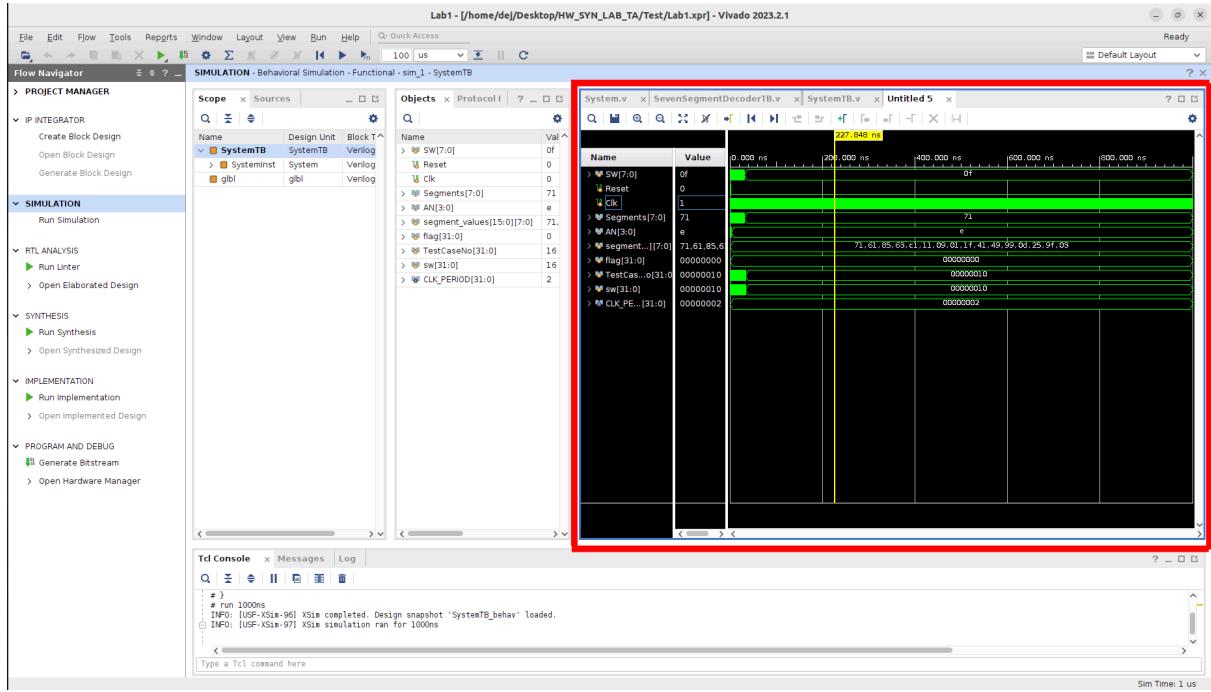
#### b. Testbench Fail + Error

```

Error: ERROR: TestCaseNo 29 | Time = 300062000 | SW = 11010000, Reset = 0 | Segments = zzzzzzzz (Expected: 10000101) | AN = 1101 (Ex
Time: 300062 ns Iteration: 0 Process: /SystemTB/check_output Scope: SystemTB.check_output File: /home/dej/Desktop/HW_SYN_LAB_TA/
Error: ERROR: TestCaseNo 30 | Time = 300064000 | SW = 11000000, Reset = 0 | Segments = zzzzzzzz (Expected: 01100001) | AN = 1101 (Ex
Time: 300064 ns Iteration: 0 Process: /SystemTB/check_output Scope: SystemTB.check_output File: /home/dej/Desktop/HW_SYN_LAB_TA/
Error: ERROR: TestCaseNo 31 | Time = 300066000 | SW = 11110000, Reset = 0 | Segments = zzzzzzzz (Expected: 01110001) | AN = 1101 (Ex
Time: 300066 ns Iteration: 0 Process: /SystemTB/check_output Scope: SystemTB.check_output File: /home/dej/Desktop/HW_SYN_LAB_TA/
Some test cases fail
$finish called at time : 300066 ns : File "/home/dej/Desktop/HW_SYN_LAB_TA/WorkPlace/Lab1/Exercisel/Source/sim/SystemTB.v" Line 104

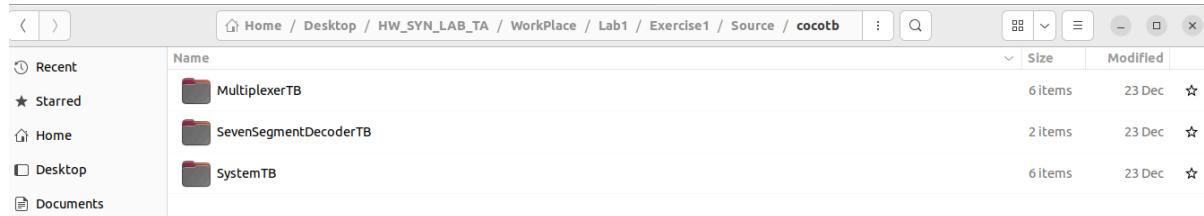
```

#### 4. The simulation waveform is shown here.



## Running CocoTB Testbench

1. go to the folder “cocotb”. This folder contains all of the CocoTB testbench.



2. go to the TB folder you want to run.
3. open the terminal window and type in make.

```
(base) dej@dej-IdeaPad-Gaming-3-15ACH6:~/Desktop/HW_SYN_LA...$ make
```

#### 4. wait for the program to return the testbench result.

##### a. Testbench Pass

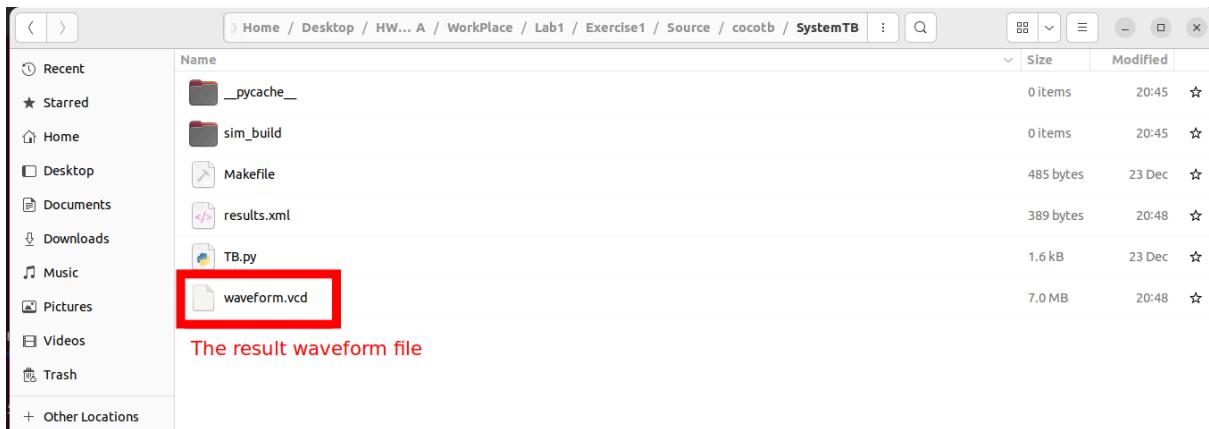
```
[cocotb] WARNING: Ignoring designs not previously learned. Scope: sys.combEvalSegmentedDecoder
150033.00ns INFO    cocotb.System          Test Complete
150033.00ns INFO    cocotb.regression      MultiplexerTB passed
150033.00ns INFO    cocotb.regression
*****
** TEST           STATUS SIM TIME (ns)  REAL TIME (s) RATIO (ns/s) **
*****
** TB.MultiplexerTB      PASS   150033.00       8.63   17381.87 ** 
*****
** TESTS=1 PASS=1 FAIL=0 SKIP=0      150033.00       8.87   16905.37 ** 
*****
make[1]: Leaving directory '/home/dej/Desktop/HW_SYN_LAB_TA/WorkPlace/Lab1/Exercise1/Source/cocotb/SystemTB'
(base) dej@dej-IdeaPad-Gaming-3-15ACH6:~/Desktop/HW_SYN_LAB_TA/WorkPlace/Lab1/Exercise1/Source/cocotb/SystemTB$
```

##### b. Testbench Fail + Error

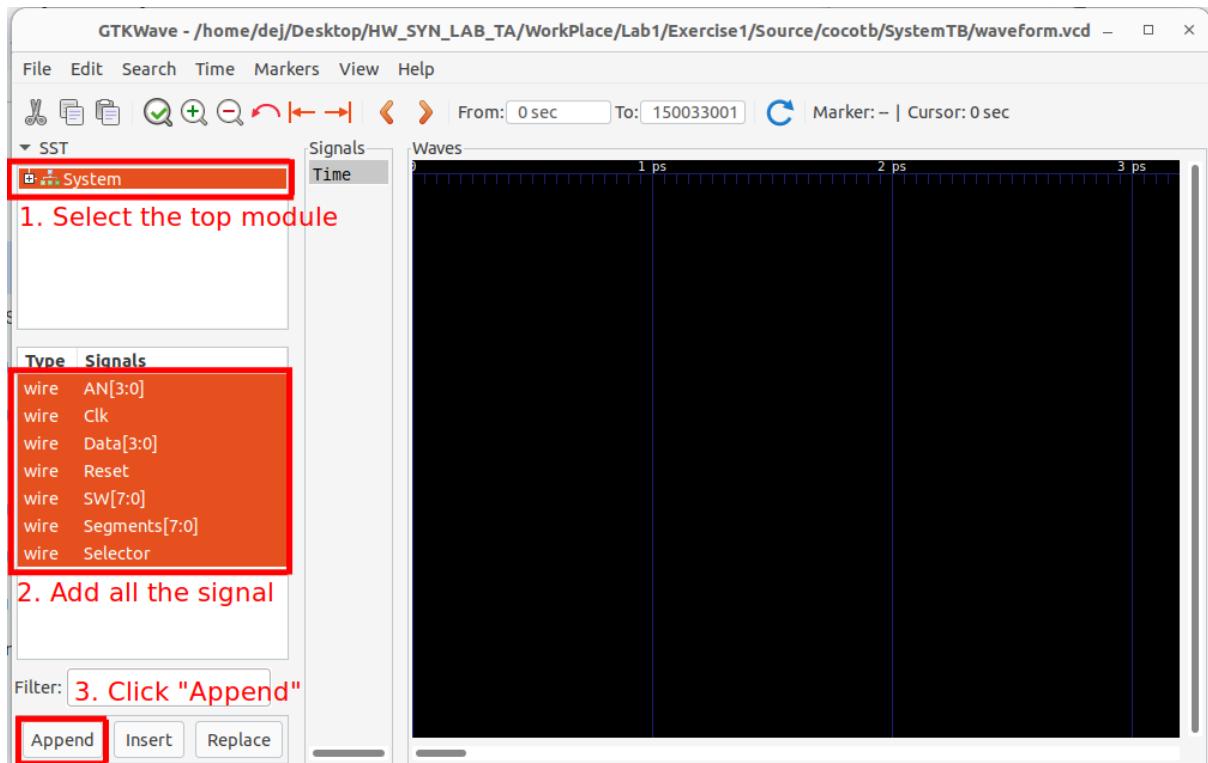
```
2.00ns INFO    cocotb.regression      ValueError: Unresolvable bit in binary string: 'z'
*****
** TEST           STATUS SIM TIME (ns)  REAL TIME (s) RATIO (ns/s) **
*****
** TB.MultiplexerTB      FAIL    2.00       0.00   1044.14 ** 
*****
** TESTS=1 PASS=0 FAIL=1 SKIP=0      2.00       0.05   43.29 ** 
*****
make[1]: Leaving directory '/home/dej/Desktop/HW_SYN_LAB_TA/WorkPlace/Lab1/Exercise1/Source/cocotb/SystemTB'
(base) dej@dej-IdeaPad-Gaming-3-15ACH6:~/Desktop/HW_SYN_LAB_TA/WorkPlace/Lab1/Exercise1/Source/cocotb/SystemTB$
```

#### 5. use the GTKWave to inspect the waveform result.

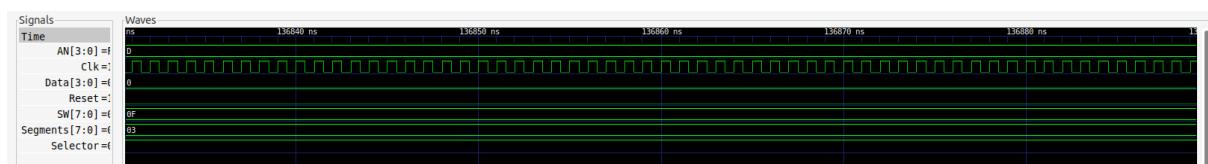
- open GTKWave.
- drag and drop the waveform.vcd from the folder you are in to GTKWave.



c. Add all the signal.



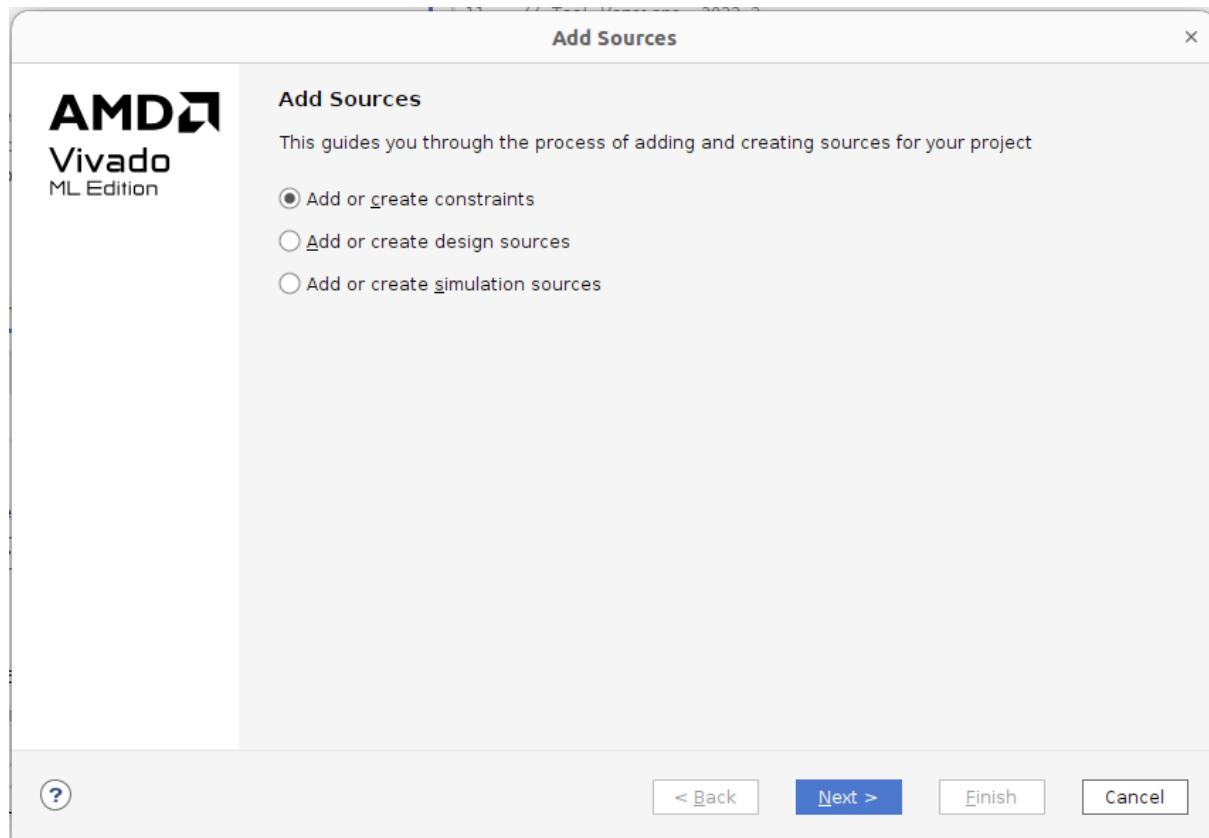
d. The waveform is here.



# Constraint File

## Path 1 : Create your own Constraint File.

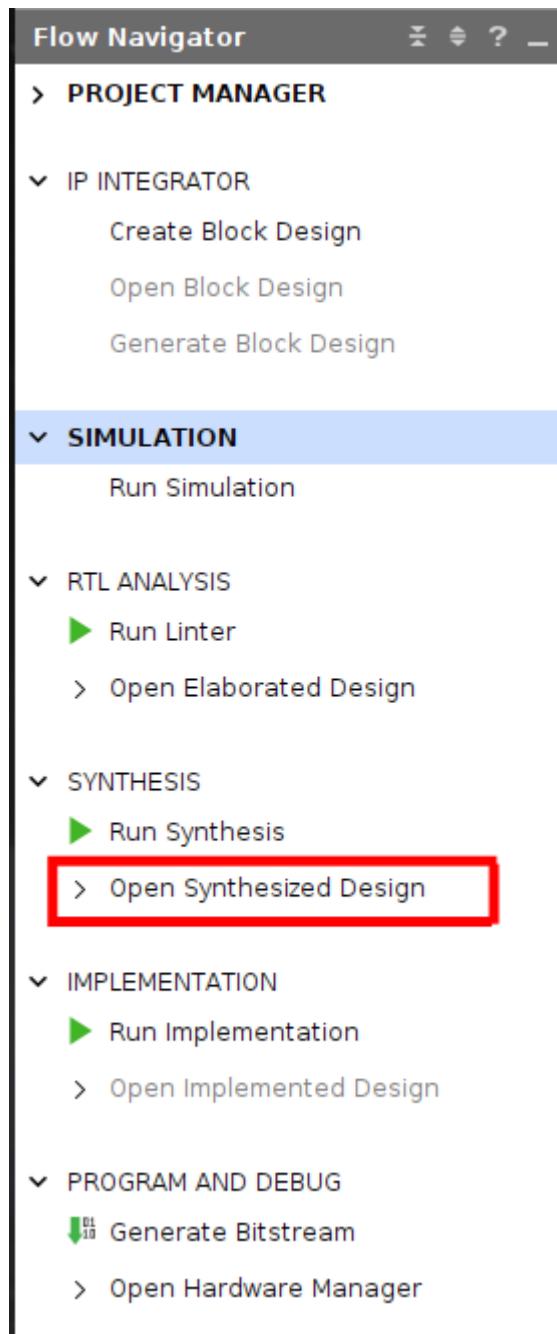
1. Add or Create your Constraint file.



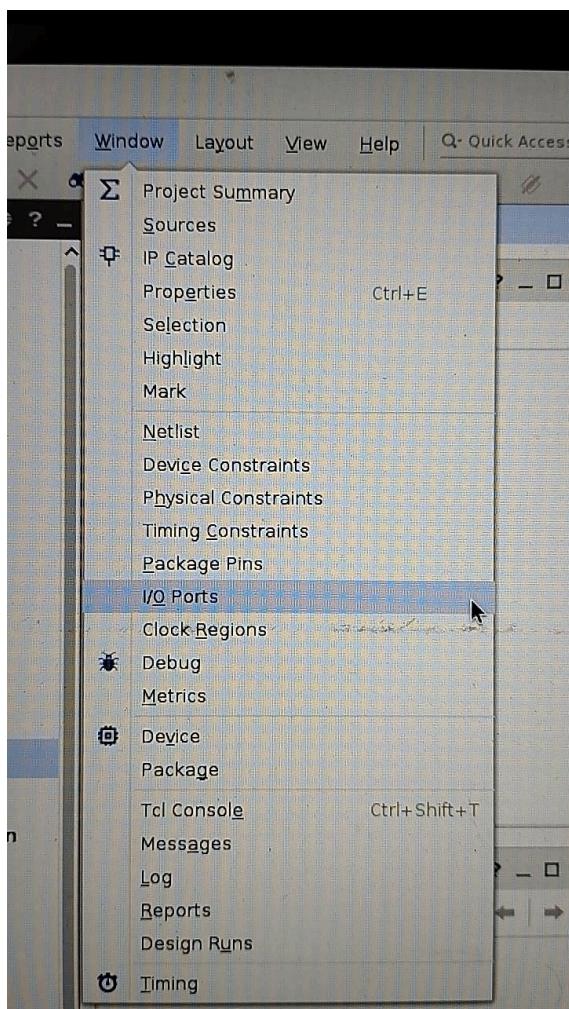
2. Code your own constraint file.

## Path 2 : Using build-in tools.

1. Run the Synthesys.
2. Open Synthesys Design.



3. select “Window” then I/O “Ports”.

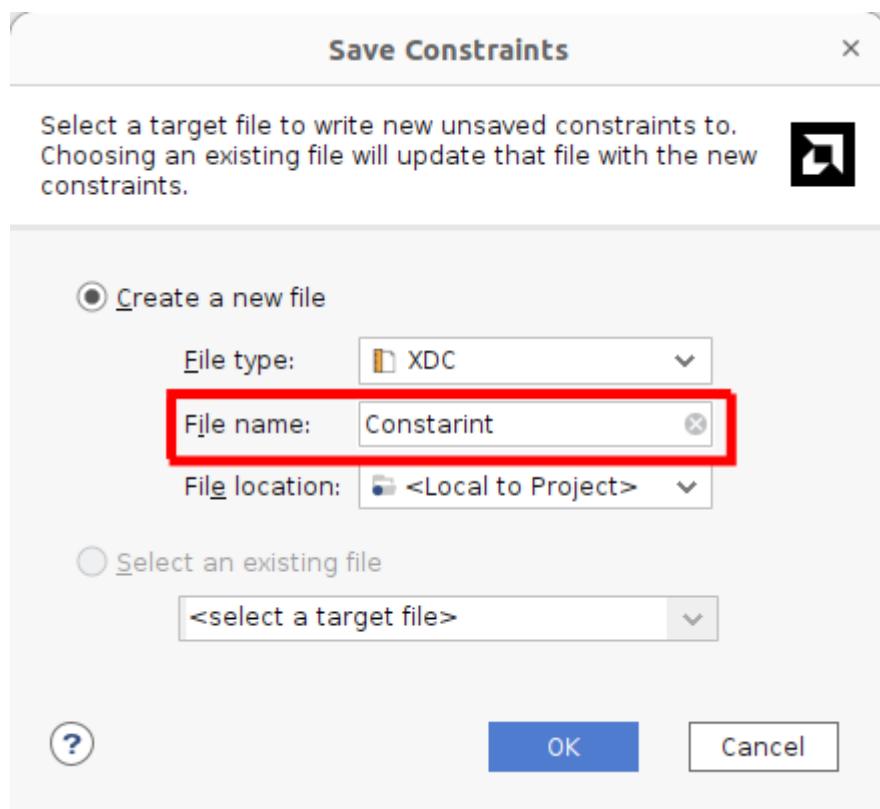


4. Fill in the Package Pin and I/O standard. The I/O standard should be LVCMOS33. You can look up the Package Pin in the Basys3 Board Reference Manual Page 15.

The screenshot shows the 'I/O Ports' configuration window. The table lists pins under the 'All ports (22)' section. The 'AN[3]' pin is selected, showing its details in the right-hand table. The table has columns for Name, Direction, Board Part Pin, Board Part Interface, Neg Diff Pair, Package Pin, Fixed, Bank, I/O Std, and Vcco. The 'Package Pin' column shows 'W4'. The 'I/O Std' column for pin 34 is set to 'LVCMOS33\*', which is highlighted with a red box. The 'Vcco' column shows '3.300'. Other pins listed in the table include AN[2], AN[1], AN[0], Segments[7], Segments[6], and Segments[5].

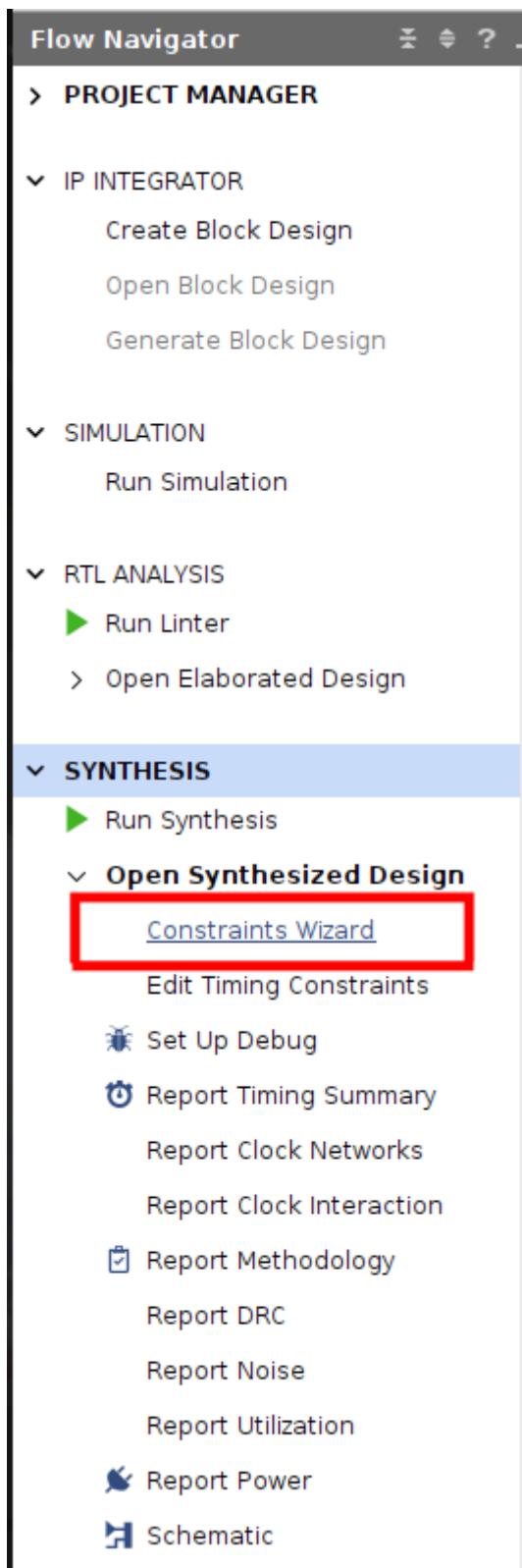
Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco
All ports (22)									
AN (4)	OUT							(Multiple)*	
AN[3]	OUT				W4	✓	34	LVCMOS33*	3.300
AN[2]	OUT					✓		default (LVCMOS18)	1.800
AN[1]	OUT					✓		default (LVCMOS18)	1.800
AN[0]	OUT					✓		default (LVCMOS18)	1.800
Segments (8)	OUT					✓		default (LVCMOS18)	1.800
Segments[7]	OUT					✓		default (LVCMOS18)	1.800
Segments[6]	OUT					✓		default (LVCMOS18)	1.800
Segments[5]	OUT					✓		default (LVCMOS18)	1.800

5. press Ctrl + s to save the constraint file.
  - a. Fill in the Constraint file name. Then Click “OK”.

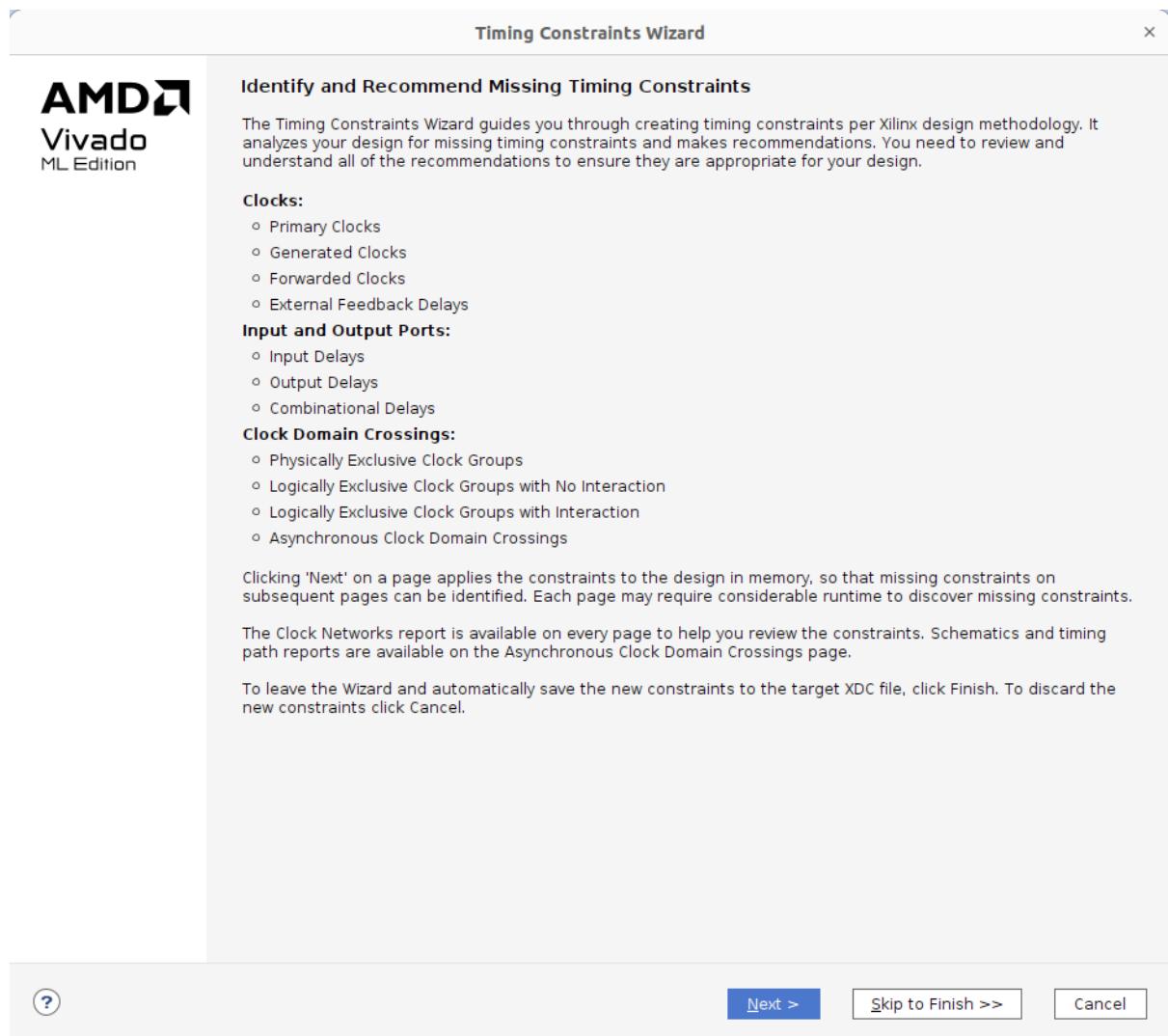


6. If your Design uses a clock, do the following.

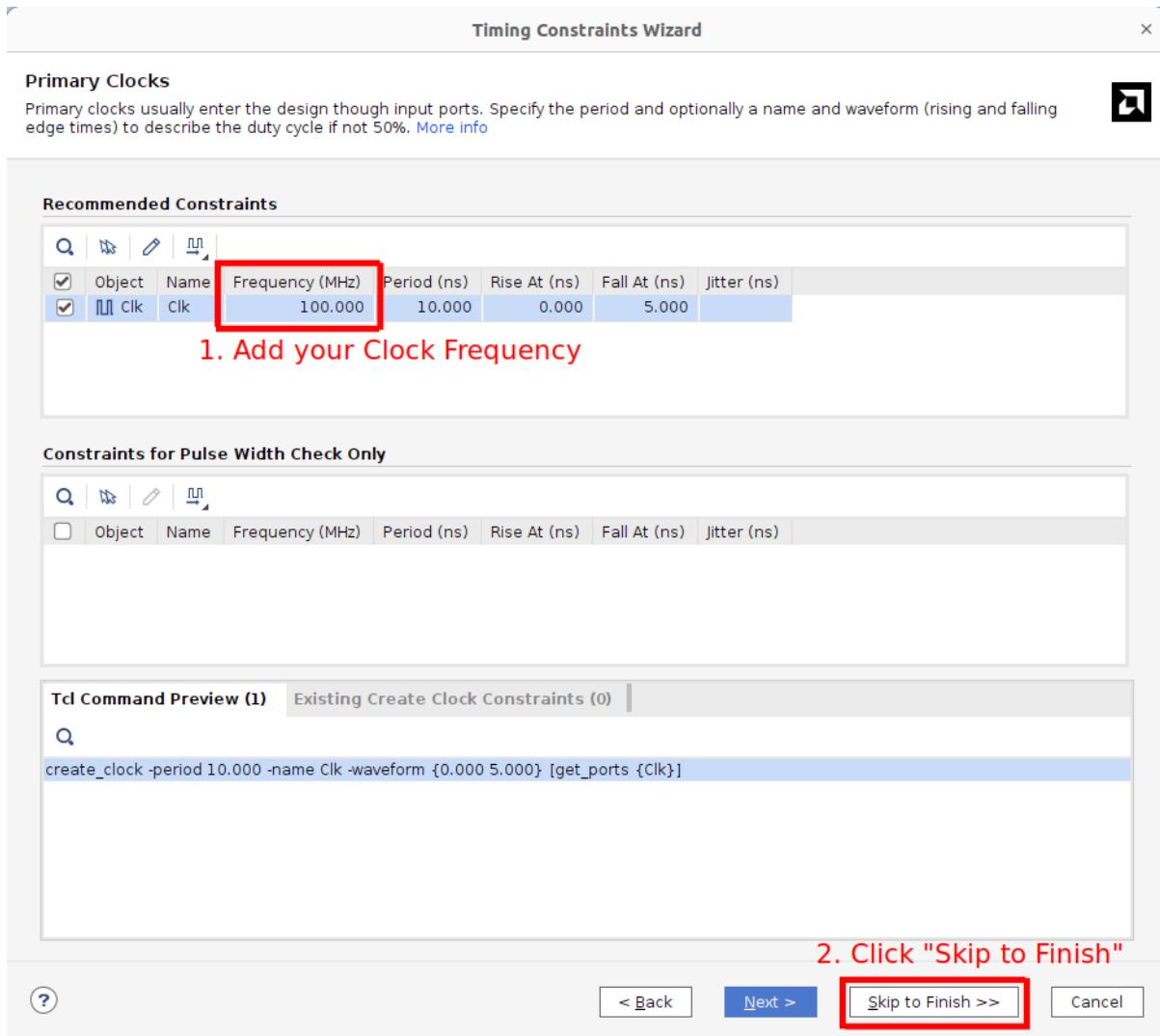
- Click on the Constraint wizard.



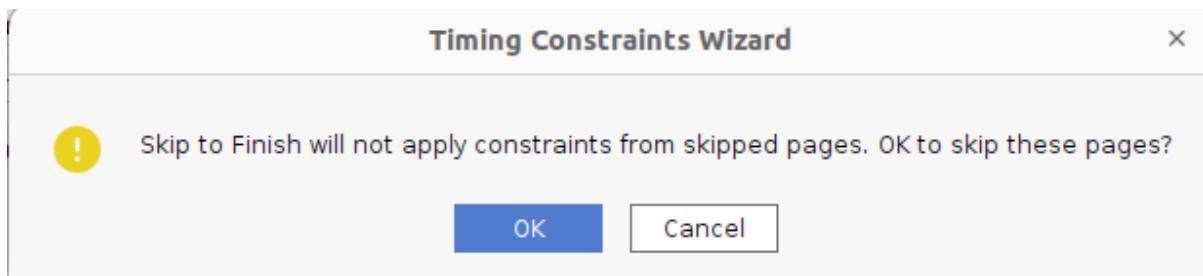
b. Click “Next”



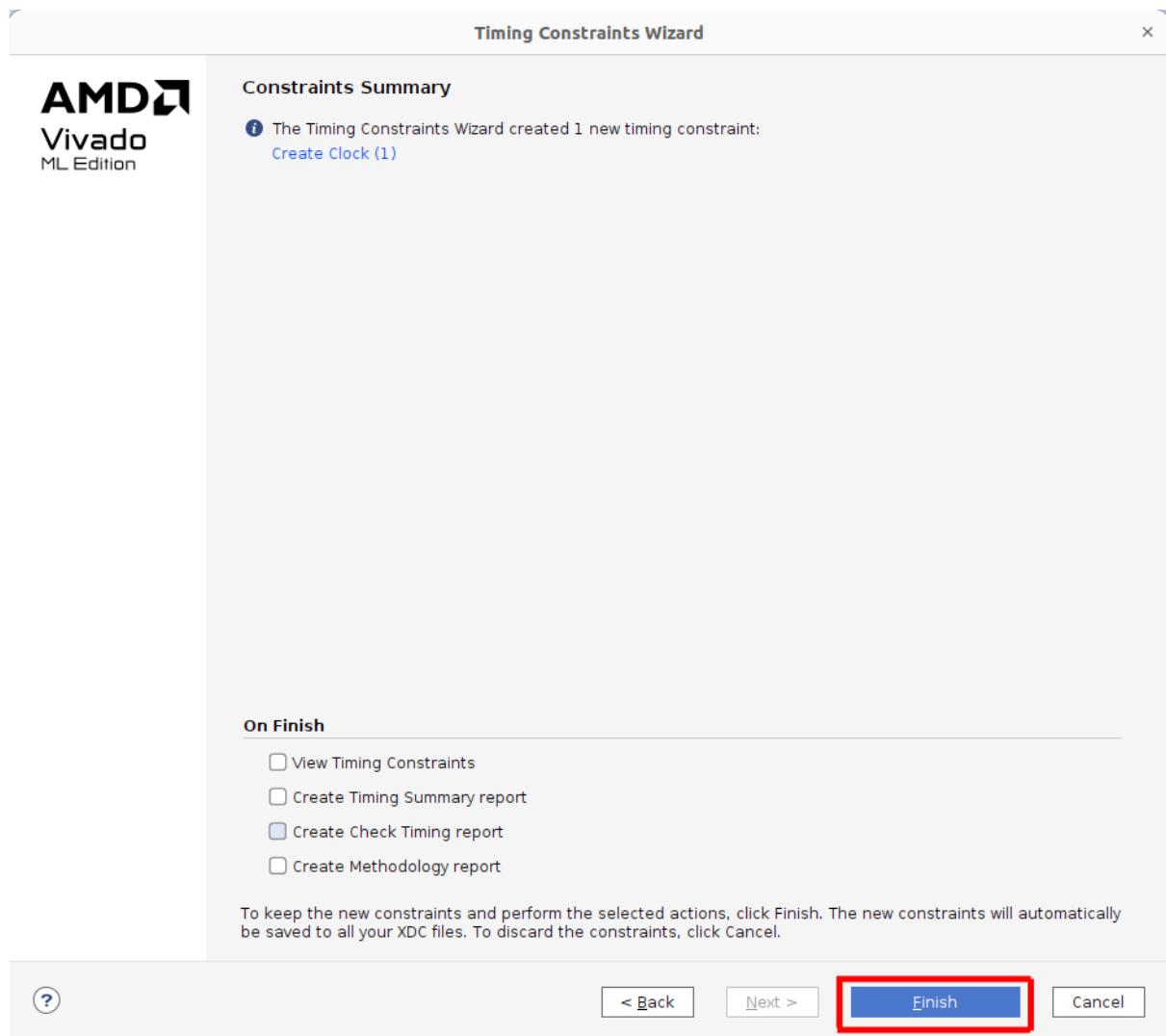
- c. Add your clock Frequency. (read Basys3 reference manual on Page 5). Then skip to Finish.



- d. Click "OK".

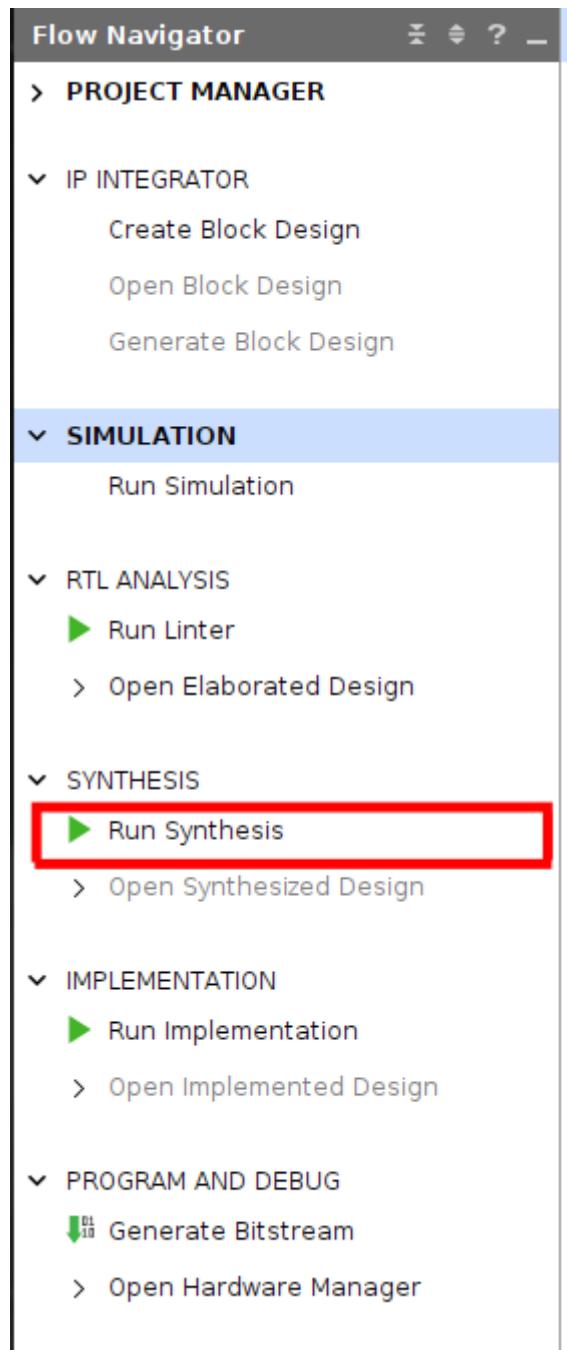


e. Click Finish.

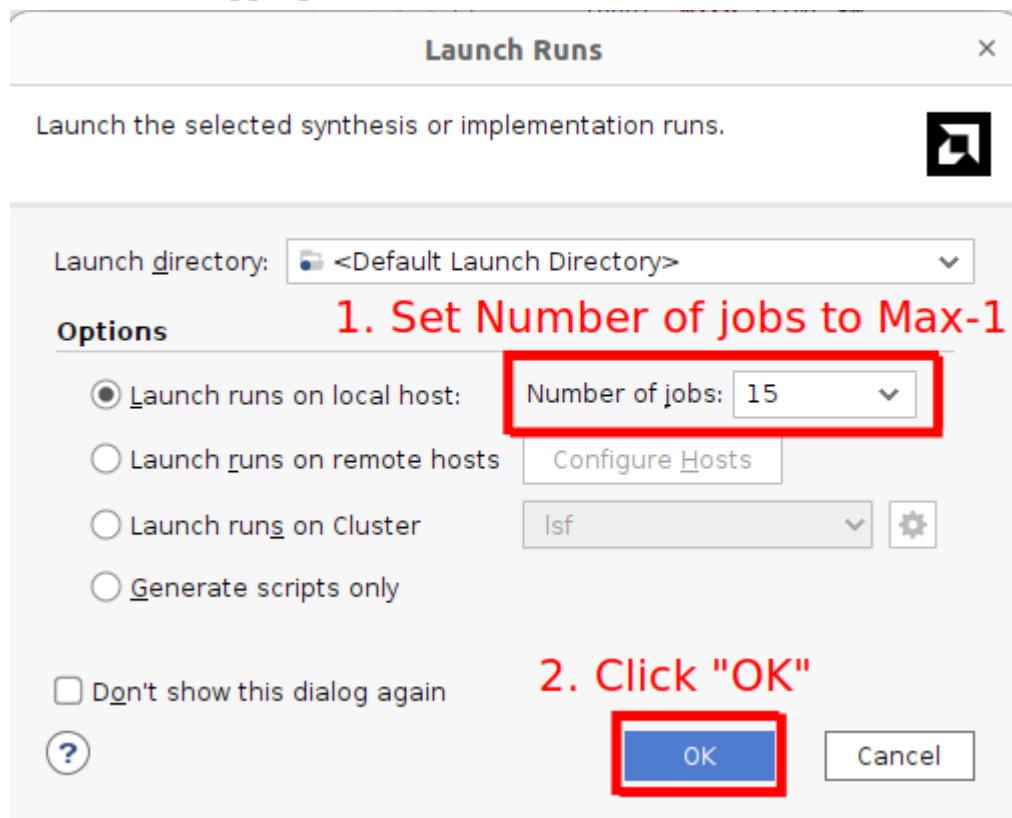


# Running Synthesis

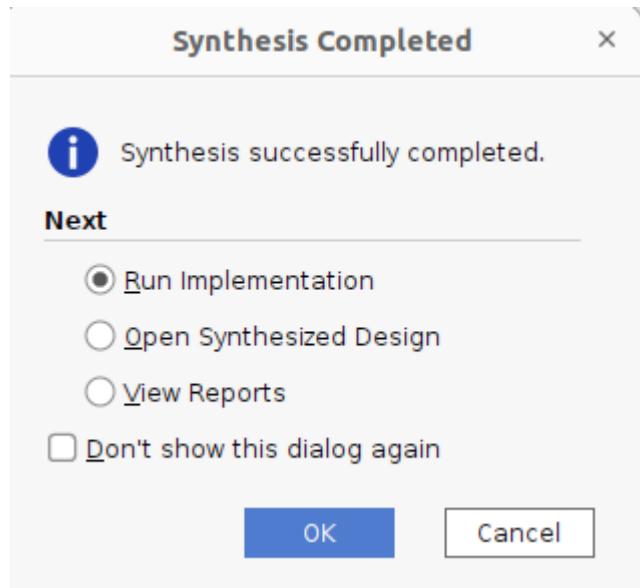
1. Click the run Synthesis



2. Set the appropriate Number of Jobs and click “OK”.

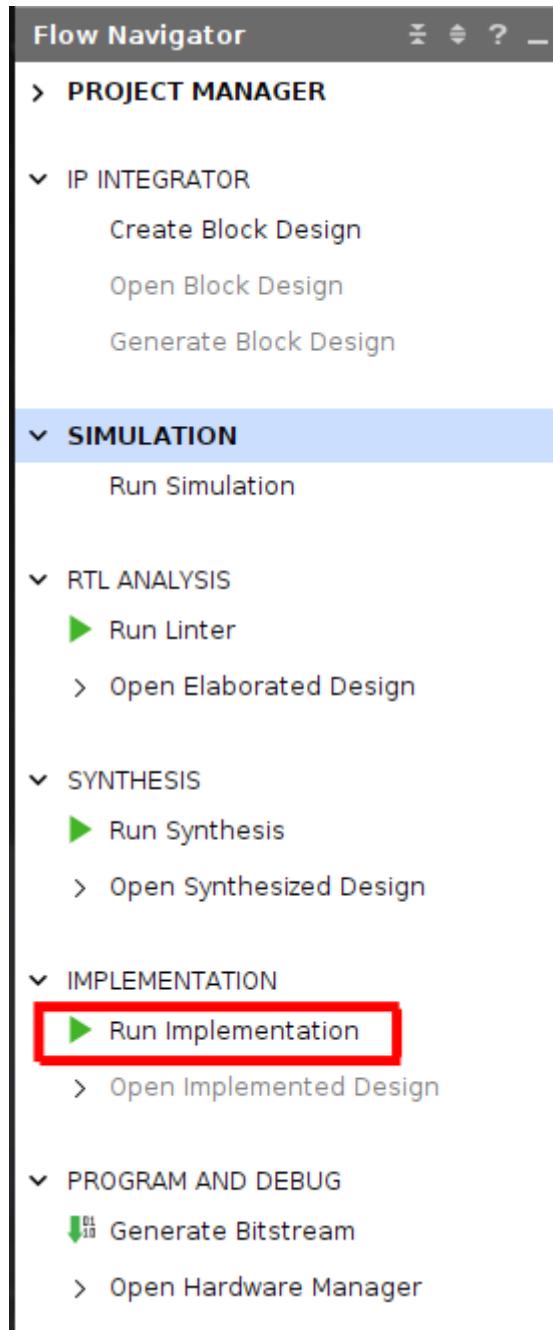


3. Wait for the program to finish running.

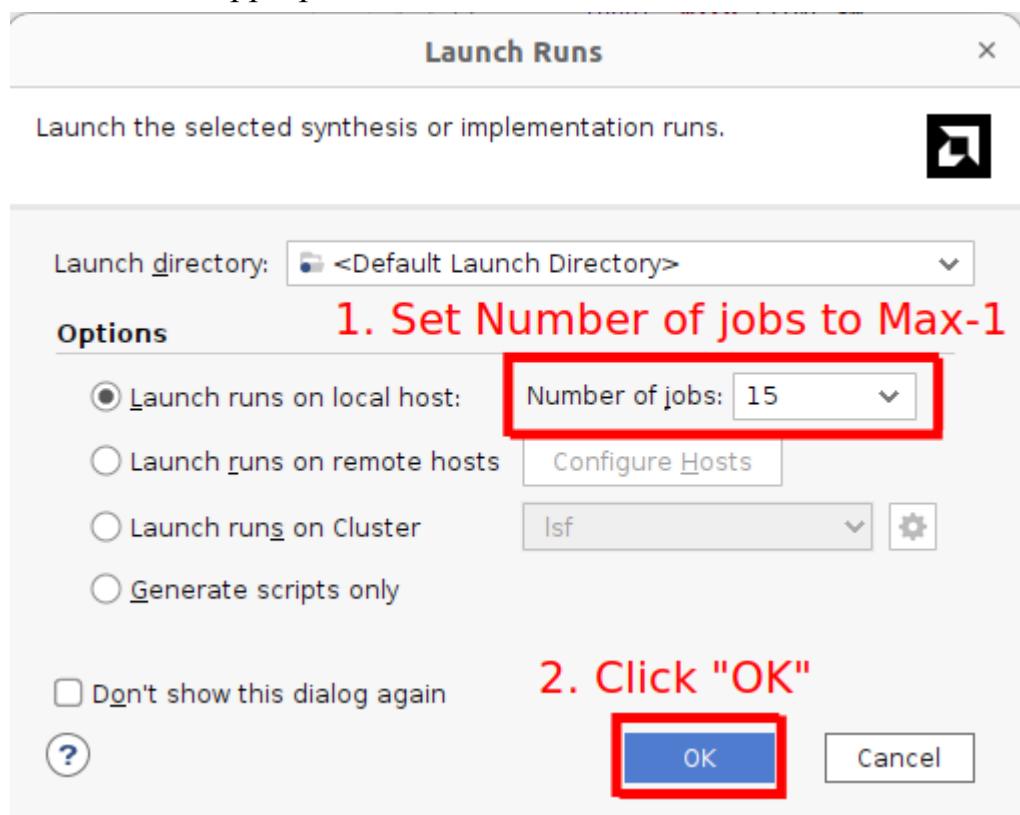


# Running Implementation

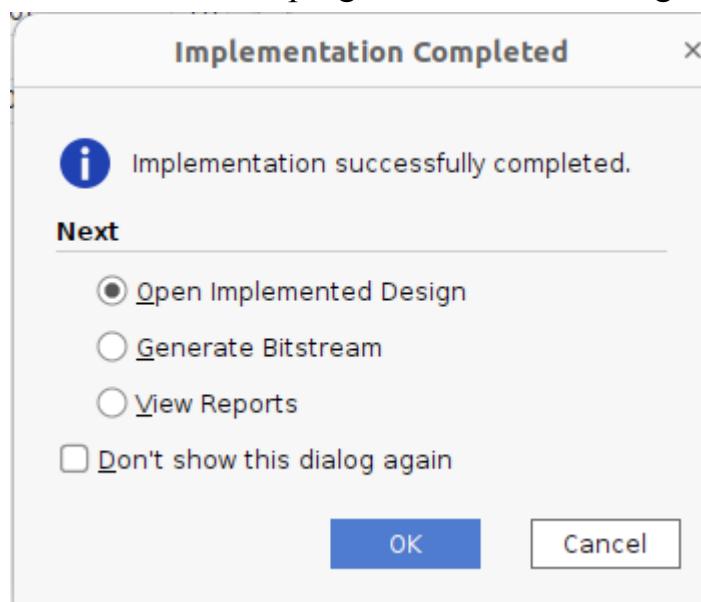
1. Click the run Implementation.



2. Set the appropriate Number of Jobs and click “OK”.

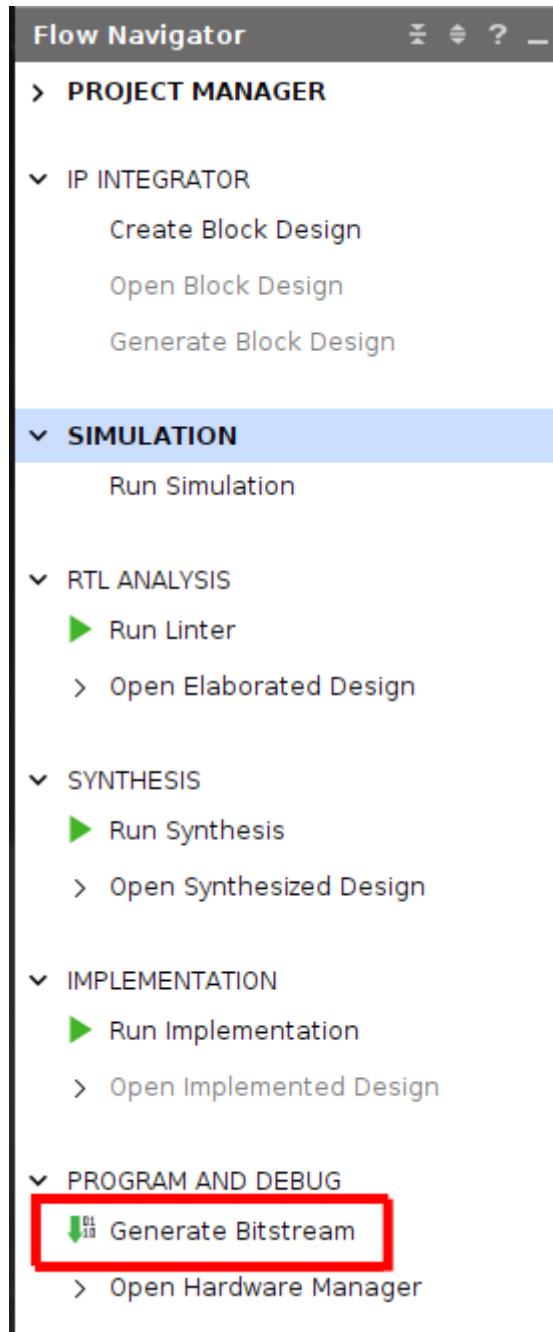


3. Wait for the program to finish running.

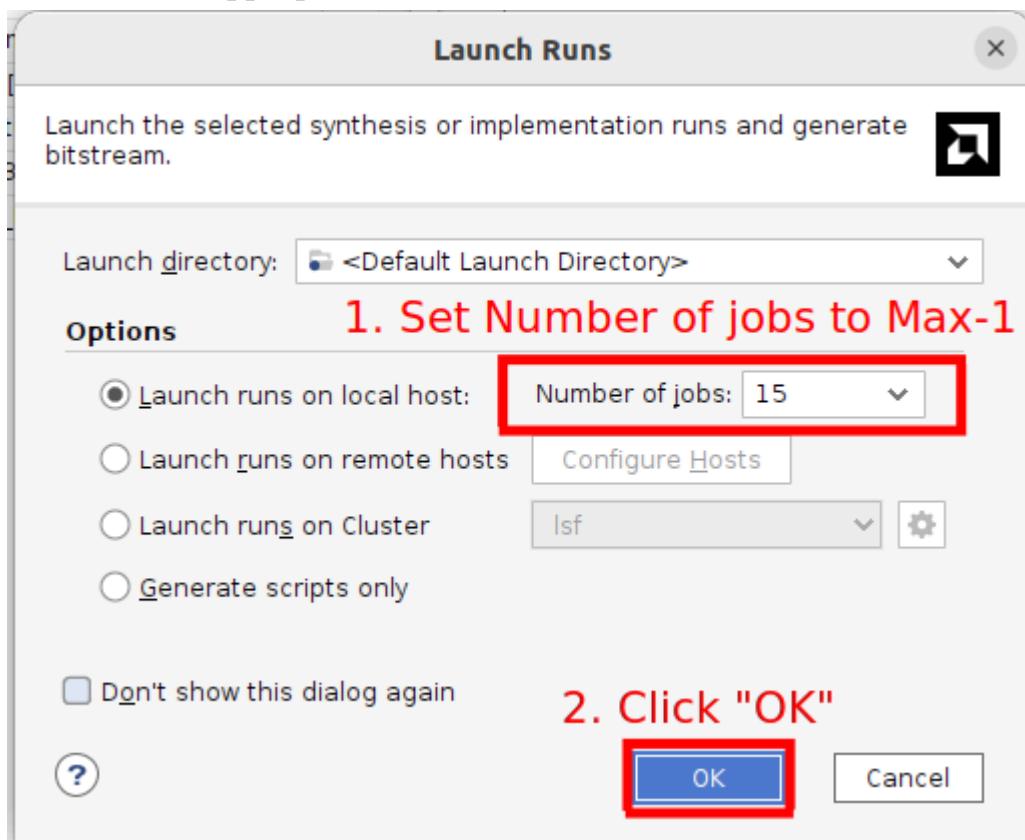


# Running Generate Bitstream

1. Run the Generate Bitstream.



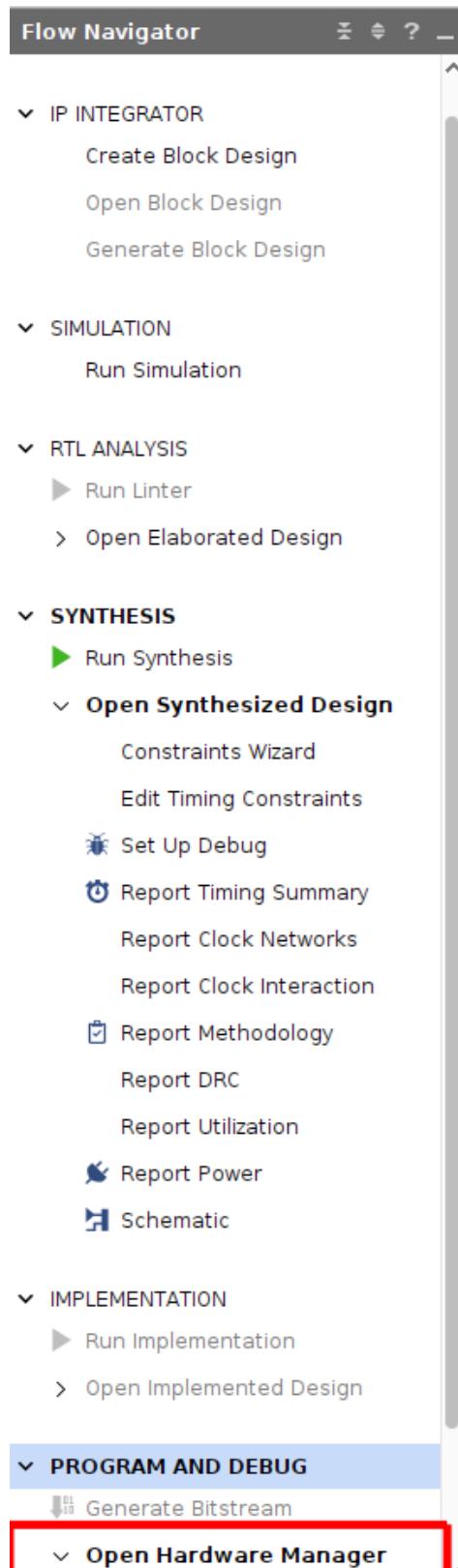
2. Set the appropriate Number of Jobs and click “OK”.



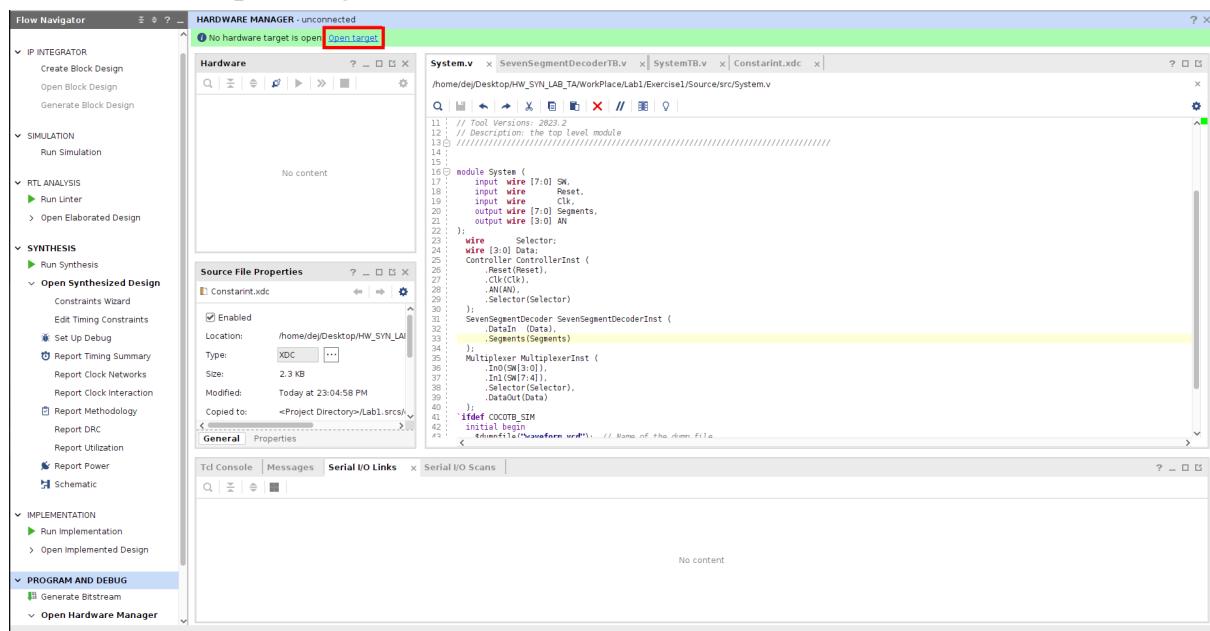
3. Wait for the program to finish running.

# Uploading Bitstream onto Basys3 Board

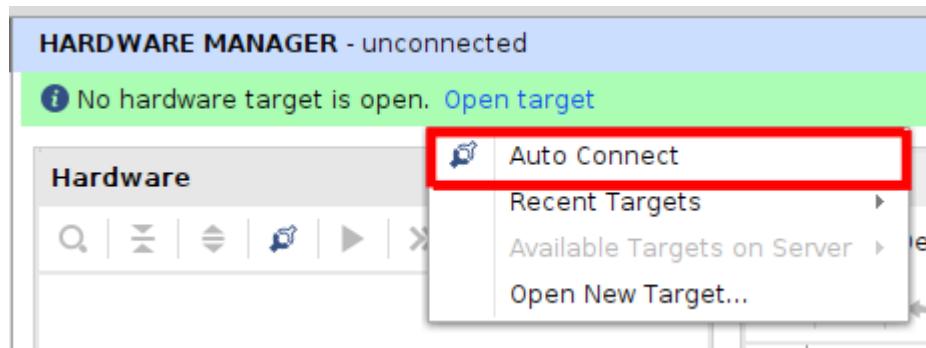
1. Connect your Basys3 board to the computer.
2. Open the Hardware Manager.



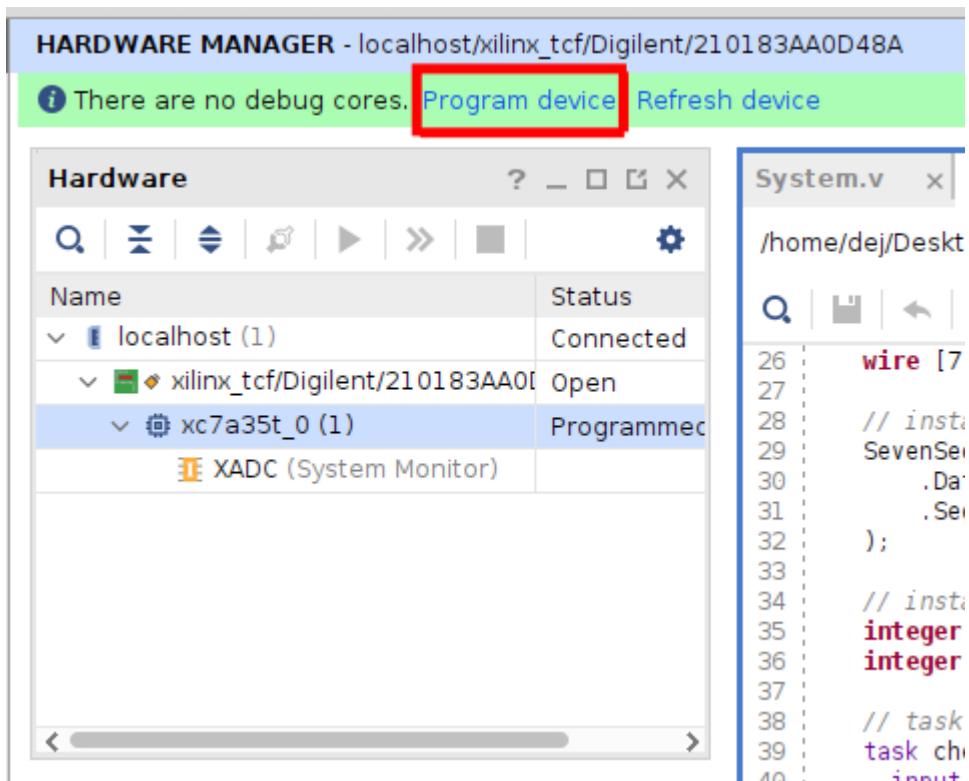
### 3. Click “Open target”



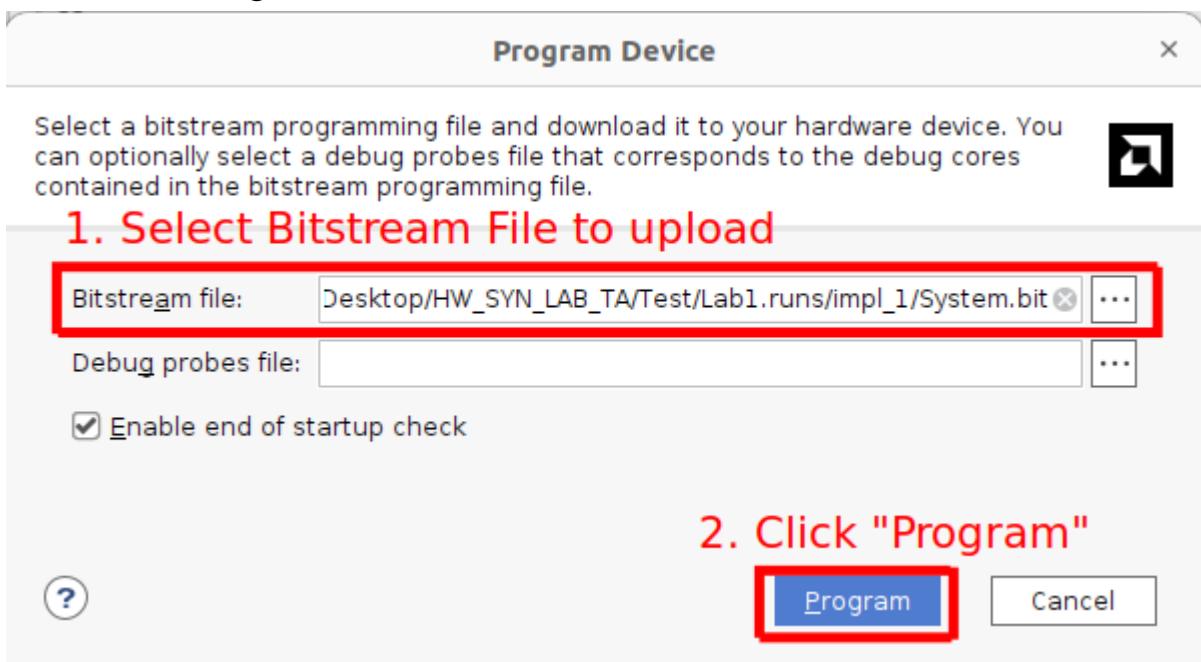
### 4. Click “Auto Connect”



5. Click “Program device”



6. select Bitstream file to upload (it should have auto select for u. If not you can find it at <YourProjectName>.runs/impl\_1/<YourTopModuleName>.bit). Then click “Program”.



7. Wait for the program to finish programming.  
8. Your Bitstream is now uploaded to the Basys3 Board.