DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT93

4-bit binary ripple counter

Product specification

File under Integrated Circuits, IC06

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Philips Semiconductors

PHILIPS

4-bit binary ripple counter   74HC/HCT93

FEATURES

- Various counting modes
- Asynchronous master reset
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT93 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT93 are 4-bit binary ripple counters. The devices consist of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate clock input ($\overline{CP}_0$ and $\overline{CP}_1$) to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q_n outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous master reset (MR_1 and MR_2) is provided which overrides both clocks and resets (clears) all flip-flops.

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a 4-bit ripple counter the output Q_0 must be connected externally to input $\overline{CP}_1$. The input count pulses are applied to clock input $\overline{CP}_0$. Simultaneous frequency divisions of 2, 4, 8 and 16 are performed at the Q_0, Q_1, Q_2 and Q_3 outputs as shown in the function table. As a 3-bit ripple counter the input count pulses are applied to input $\overline{CP}_1$.
Simultaneous frequency divisions of 2, 4 and 8 are available at the Q_1, Q_2 and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay $\overline{CP}_0$ to Q_0	C_L = 15 pF; V_{CC} = 5 V	12	15	ns
f_{max}	maximum clock frequency		100	77	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	22	22	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

    $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\ (C_L \times V_{CC}^2 \times f_o)$ where:

    f_i = input frequency in MHz; f_o = output frequency in MHz

    $\Sigma\ (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

    C_L = output load capacitance in pF; V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}; for HCT the condition is V_I = GND to $V_{CC} - 1.5$ V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

4-bit binary ripple counter

74HC/HCT93

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{CP}_1$	clock input 2nd, 3rd and 4th section (HIGH-to-LOW, edge-triggered)
2, 3	MR_1, MR_2	asynchronous master reset (active HIGH)
4, 6, 7, 13	n.c.	not connected
5	V_{CC}	positive supply voltage
10	GND	ground (0 V)
12, 9, 8, 11	Q_0 to Q_3	flip-flop outputs
14	$\overline{CP}_0$	clock input 1st section (HIGH-to-LOW, edge-triggered)

Fig.1 Pin configuration.

Fig.2 Logic symbol.

Fig.3 IEC logic symbol.
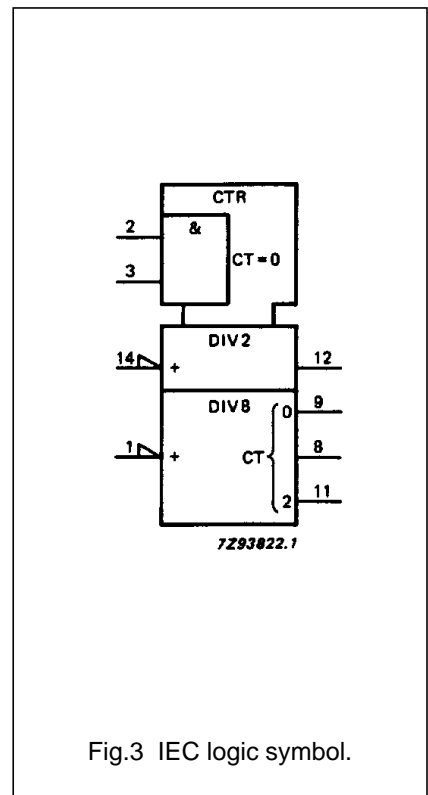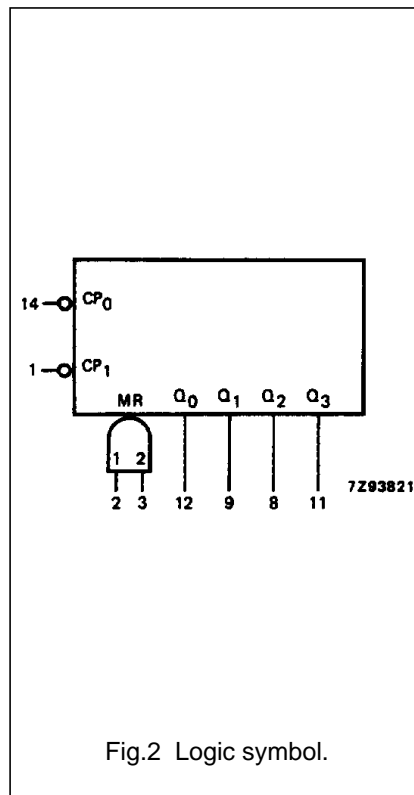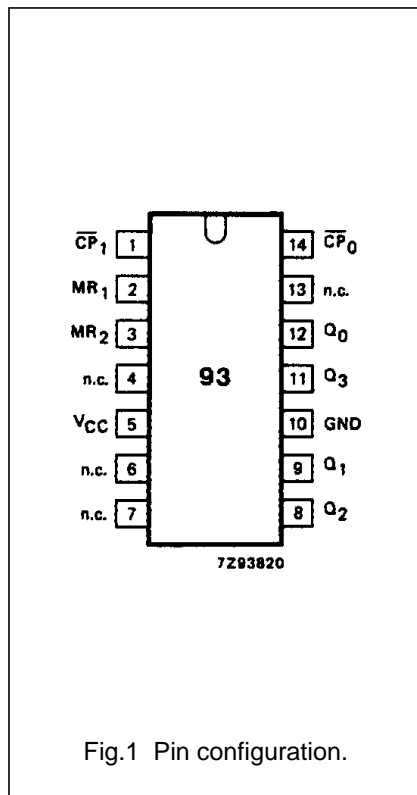
4-bit binary ripple counter

74HC/HCT93
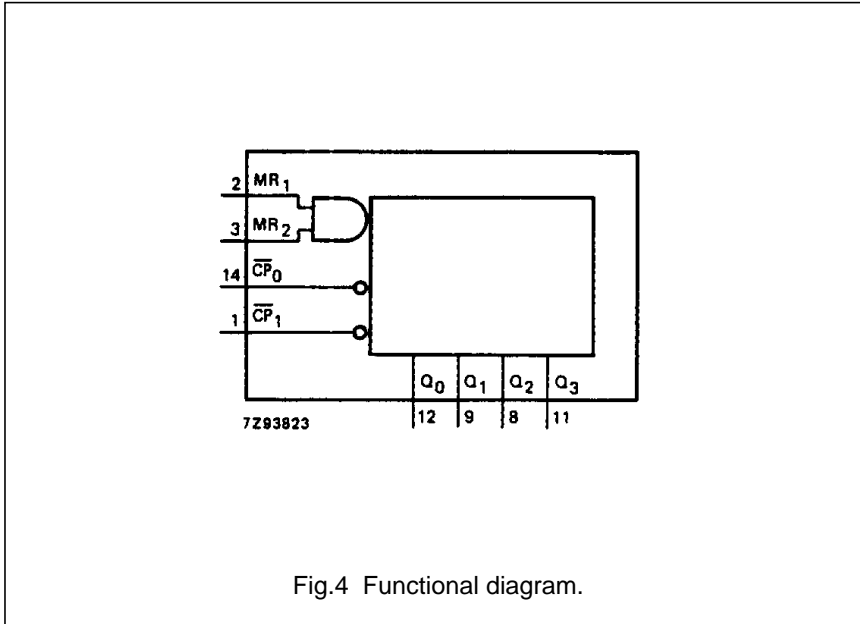
Fig.4 Functional diagram.

FUNCTION TABLE

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Notes

1. Output Q_0 connected to $\overline{CP}_1$.
    H = HIGH voltage level
    L = LOW voltage level

MODE SELECTION

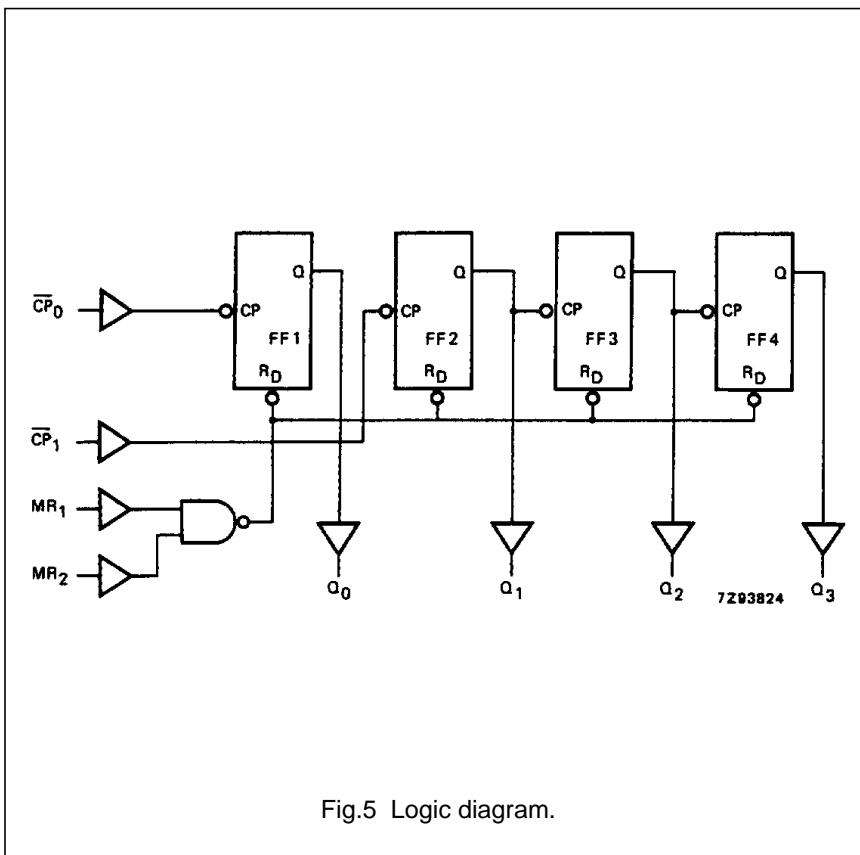| RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	count			
H	L	count			
L	L	count			

Fig.5 Logic diagram.

4-bit binary ripple counter

74HC/HCT93

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	Tamb (°C) 74HC +25 min.	+25 typ.	+25 max.	−40 to +85 min.	−40 to +85 max.	−40 to +125 min.	−40 to +125 max.	UNIT	V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_0$ to Q_0		41	125		155		190	ns	2.0	Fig.6
			15	25		31		38		4.5	
			12	21		26		32		6.0	
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_1$ to Q_1		49	135		170		205	ns	2.0	Fig.6
			16	27		34		41		4.5	
			13	23		29		35		6.0	
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_1$ to Q_2		61	185		230		280	ns	2.0	Fig.6
			22	37		46		56		4.5	
			18	31		39		48		6.0	
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_1$ to Q_3		80	245		305		370	ns	2.0	Fig.6
			29	49		61		71		4.5	
			23	42		52		63		6.0	
t_{PHL}	propagation delay MR_n to Q_n		50	155		195		235	ns	2.0	Fig.7
			18	31		39		47		4.5	
			14	26		33		40		6.0	
t_{THL}/t_{TLH}	output transition time		19	75		95		110	ns	2.0	Fig.6
			7	15		19		22		4.5	
			6	13		16		19		6.0	
t_{rem}	removal time MR_n to $\overline{CP}_0$, $\overline{CP}_1$	50	8		65		75		ns	2.0	Fig.7
		10	3		13		15			4.5	
		9	2		11		13			6.0	
t_W	pulse width $\overline{CP}_0$, $\overline{CP}_1$	80	14		100		120		ns	2.0	Fig.6
		16	5		20		24			4.5	
		14	4		17		20			6.0	
t_W	master reset pulse width MR_n	80	14		100		120		ns	2.0	Fig.7
		16	5		20		24			4.5	
		14	4		17		20			6.0	
f_{max}	maximum clock pulse frequency $\overline{CP}_0$, $\overline{CP}_1$	6.0	30		4.8		4.0		MHz	2.0	Fig.6
		30	91		24		20			4.5	
		35	108		28		24			6.0	

4-bit binary ripple counter

74HC/HCT93

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}_0$, $\overline{CP}_1$	0.60
MR_n	0.40

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_0$ to Q_0		18	34		43		51	ns	4.5	Fig.6
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_1$ to Q_1		18	34		43		51	ns	4.5	Fig.6
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_1$ to Q_2		24	46		58		69	ns	4.5	Fig.6
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_1$ to Q_3		30	58		73		87	ns	4.5	Fig.6
t_{PHL}	propagation delay MR_n to Q_n		17	33		41		50	ns	4.5	Fig.7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.6
t_{rem}	removal time MR_n to $\overline{CP}_0$, $\overline{CP}_1$	10	3		13		15		ns	4.5	Fig.7
t_W	pulse width $\overline{CP}_0$, $\overline{CP}_1$	16	7		20		24		ns	4.5	Fig.6
t_W	master reset pulse width MR_n	16	5		20		24		ns	4.5	Fig.7
f_{max}	maximum clock pulse frequency $\overline{CP}_0$, $\overline{CP}_1$	30	70		24		20		MHz	4.5	Fig.6

4-bit binary ripple counter
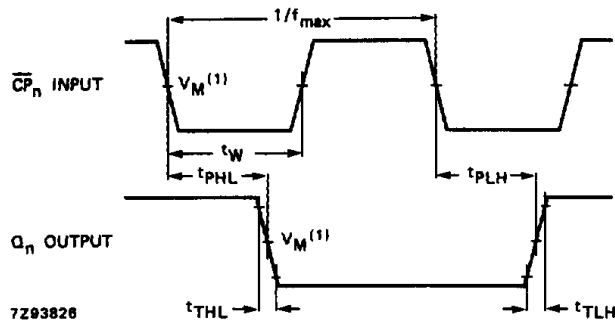
AC WAVEFORMS

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
    HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6   Waveforms showing the clock ($\overline{CP}_n$) to output (Q_n) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.
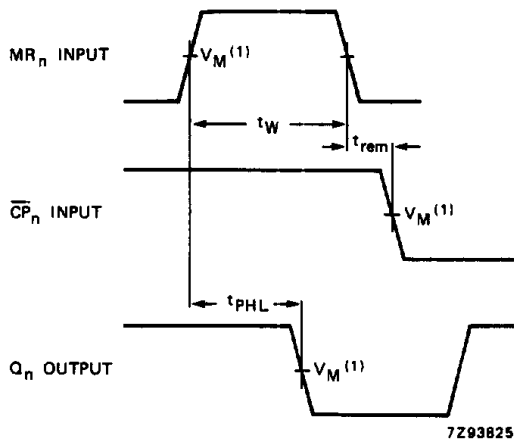
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
    HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7   Waveforms showing the master reset (MR_n) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock ($\overline{CP}_n$) removal time.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.