

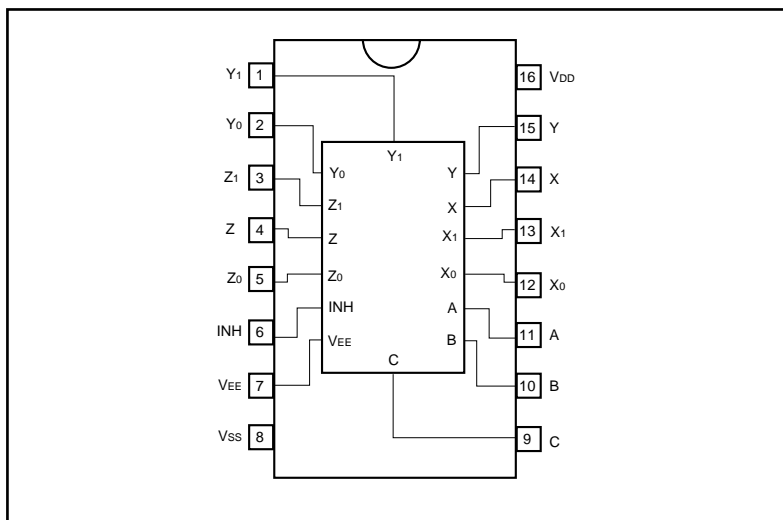
Triple 2-channel analog multiplexer / demultiplexer

BU4053BC / BU4053BCF / BU4053BCFV

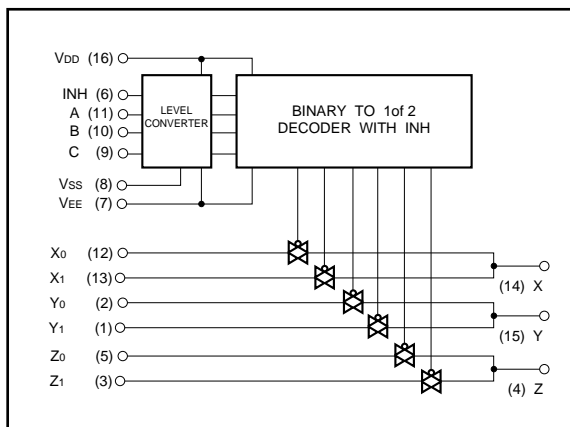
The BU4053BC, BU4053BCF, and BU4053BCFV are multiplexers / demultiplexers capable of selecting and combining analog signals and digital signals in a $2\text{ ch} \times 3$ configuration. Inhibit signals and control signals are used to turn on the switch corresponding to each of the channels. In addition, even if the logical amplitude ($V_{DD}-V_{SS}$) of the control signal is low, signals with a large amplitude ($V_{DD}-V_{EE}$) can be switched.

Also, as each switch has a low ON resistance, it can be connected to a low impedance circuit.

●Block diagram



●Logic circuit diagram



●Truth table

INH	A	B	C	ON SWITCH
L	L	L	L	X ₀ Y ₀ Z ₀
L	H	L	L	X ₁ Y ₀ Z ₀
L	L	H	L	X ₀ Y ₁ Z ₀
L	H	H	L	X ₁ Y ₁ Z ₀
L	L	L	H	X ₀ Y ₀ Z ₁
L	H	L	H	X ₁ Y ₀ Z ₁
L	L	H	H	X ₀ Y ₁ Z ₁
L	H	H	H	X ₁ Y ₁ Z ₁
H	X	X	X	NONE

X: Irrelevant

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage1	V _{DD}	− 0.5 ~ + 20	V
Power supply voltage2	V _{DD} - V _{EE}	− 0.5 ~ + 20	V
Power dissipation	P _d	1000 (DIP), 500 (SOP), 400 (SSOP)	mW
Operating temperature	Topr	− 40 ~ + 85	°C
Storage temperature	Tstg	− 55 ~ + 150	°C
Input voltage	V _{IN}	− 0.5 ~ V _{DD} + 0.5	V

●Electrical characteristics

DC characteristics (unless otherwise noted, Ta = 25°C, V_{EE} = V_{SS} = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	V _{DD} (V)	Conditions	Measurement circuit
Input high-level voltage	V _{IH}	3.5	—	—	V	5	—	Fig.1
		7.0	—	—		10		
		11.0	—	—		15		
Input low-level voltage	V _{IL}	—	—	1.5	V	5	—	Fig.1
		—	—	3.0		10		
		—	—	4.0		15		
Input high-level current	I _{IH}	—	—	0.3	μA	15	V _{IH} = 15V	Fig.1
Input low-level current	I _{IL}	—	—	− 0.3	μA	15	V _{IL} = 0V	Fig.1
R _{ON} resistance	R _{ON}	—	—	950	Ω	5	V _{IN} = V _{DD} / 2	Fig.2
		—	—	250		10		
		—	—	160		15		
R _{ON} resistance deflexion	ΔR _{ON}	—	10	—	Ω	5	—	Fig.2
		—	6	—		10		
		—	4	—		15		
OFF-channel leakage current	I _{OFF}	—	—	0.3	μA	15	—	Fig.3
		—	—	− 0.3		15		
Static current dissipation	I _{DD}	—	—	5	μA	5	V _I = V _{DD} or GND	—
		—	—	10		10		
		—	—	15		15		

Switching characteristics (unless otherwise noted, $T_a = 25^\circ\text{C}$, $V_{EE} = V_{SS} = 0\text{V}$, $R_L = 1\text{k}\Omega$, $C_L = 50\text{pF}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	V _{DD} (V)	Conditions	Measurement circuit
Propagation delay time Switch IN→OUT	t_{PLH}, t_{PHL}	—	15	45	ns	5	—	Fig.4
		—	8	20		10		
		—	6	15		15		
Propagation delay time CONT→OUT	t_{PHZ}, t_{PLZ} t_{PZH}, t_{PZL}	—	170	550	ns	5	—	Fig.5, 6
		—	90	240		10		
		—	70	160		15		
Propagation delay time INH→OUT	t_{PHZ}, t_{PLZ} t_{PZH}, t_{PZL}	—	150	380	ns	5	—	Fig.5, 6
		—	70	200		10		
		—	50	160		15		
Max. propagation frequency	f_{Max}	—	20	—	MHz	5	$V_{EE} = -5\text{V}^{*1}$	Fig.7
Feedthrough attenuation	FT	—	0.5	—	MHz	5	$V_{EE} = -5\text{V}^{*2}$	Fig.7
Sine wave distortion	D	—	0.02	—	%	5	$V_{EE} = -5\text{V}^{*3}$	Fig.7
Input capacitance (control)	C_C	—	5	—	pF	—	—	—
Input capacitance (switch)	C_S	—	10	—	pF	—	—	—

*1 $V_{IN} = 5\text{V}_{\text{p-p}}$ sine wave, frequency that enables $20 \log_{10} \frac{V_{\text{OUT}}}{V_{IN}} = -3\text{dB}$.

*2 $V_{IN} = 5\text{V}_{\text{p-p}}$ sine wave, frequency that enables $20 \log_{10} \frac{V_{\text{OUT}}}{V_{IN}} = -50\text{dB}$ at channel off.

*3 $V_{IN} = 5\text{V}_{\text{p-p}}$ sine wave.

●Measurement circuits

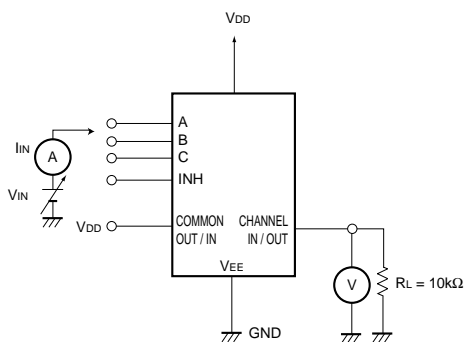


Fig. 1 Input voltage, current

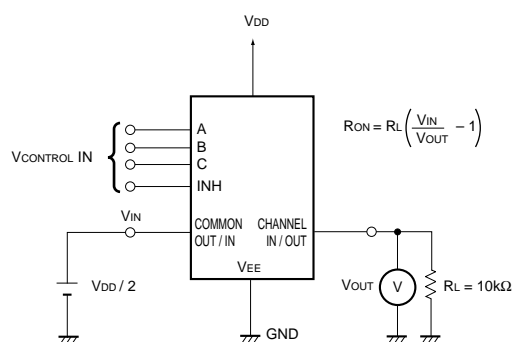


Fig. 2 ON resistance

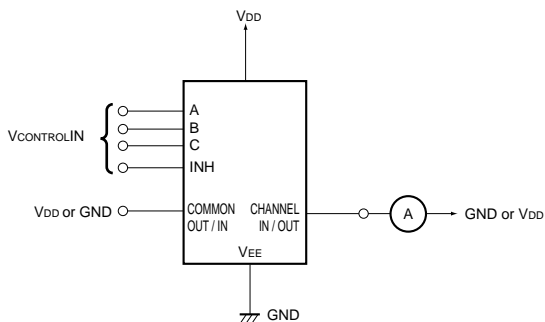


Fig. 3 Channel-OFF leakage current

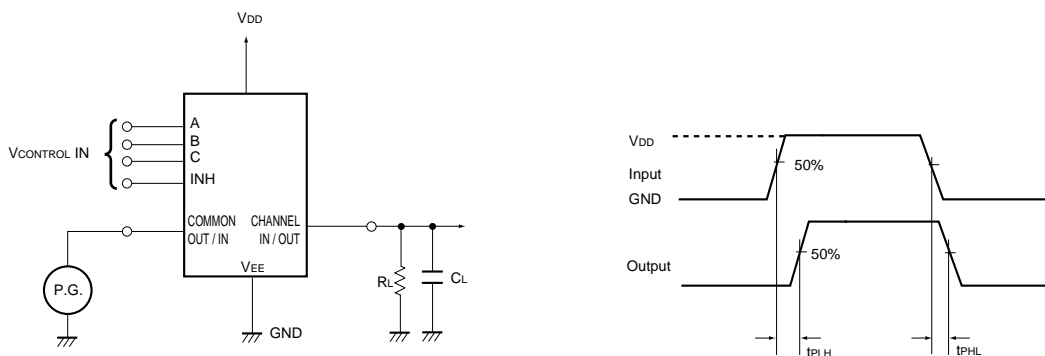


Fig. 4 Propagation delay time (Switch IN to OUT)

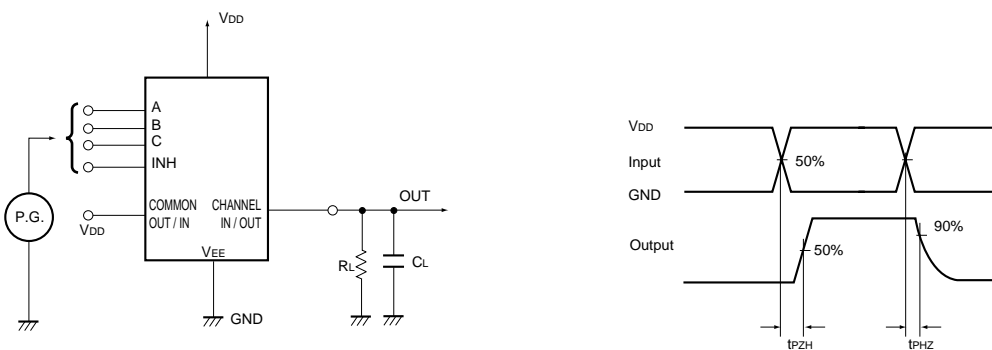


Fig. 5 Propagation delay time (CONT, INH to OUT)

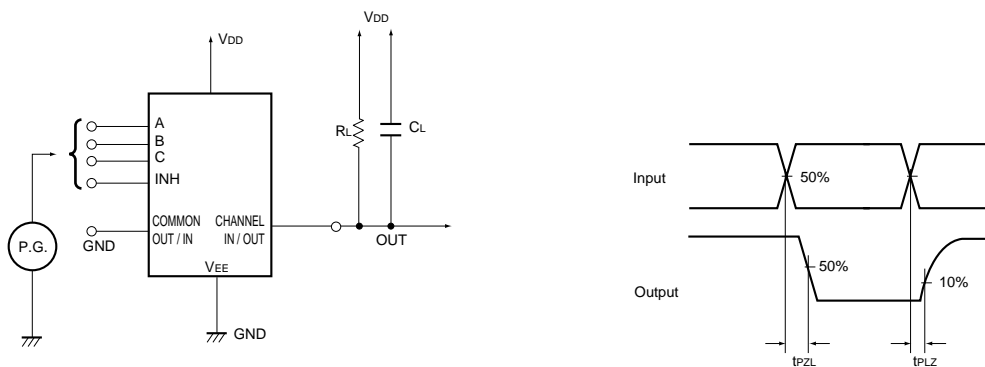


Fig. 6 Propagation delay time (CONT, INH to OUT)

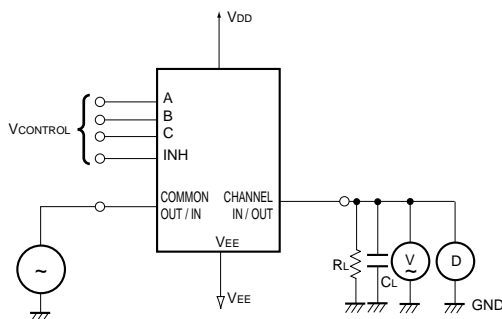
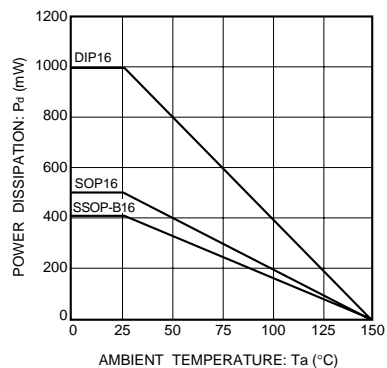


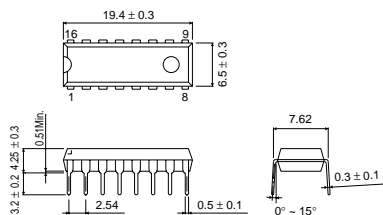
Fig. 7 Maximum propagation frequency, feedthrough, sine wave distortion

●Electrical characteristic curve

Fig. 8 Power dissipation vs. T_a

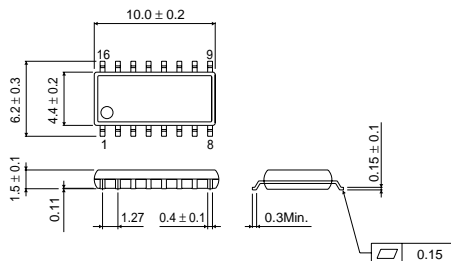
● External dimensions (Units: mm)

BU4053BC



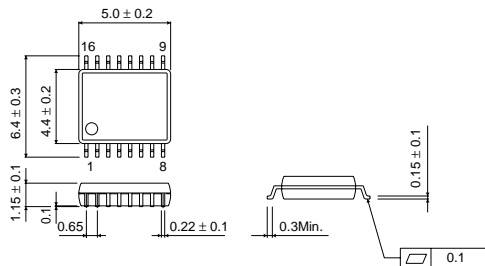
DIP16

BU4053BCF



SOP16

BU4053BCFV



SSOP-B16

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