Serial DAC design using Microwind

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***Abstract*—This paper presents our attempt at building a 6-bits 50Msps serial charge redistribution Digital-to-Analog Converter (DAC) from scratch using the Microwind software. The main architecture of the design and some critical components are discussed. Test reports and simulations are shown and areas of improvement are considered.**

***Index Terms*—digital to analog converter, CMOS cell design, charge redistribution DAC, Microwind**

I. Introduction

As part of the "Study and Modeling of Active Components" course, we were asked to design a basic electronic system using the Microwind software, by E. Sicard. We chose to work on a serial charge redistribution DAC, as it combines both digital and analog building blocs. The goal was to estimate the effective number of bits obtained by the design. We will discuss some key aspects of the design, and highlight the results and flaws of our system.

II. System Design

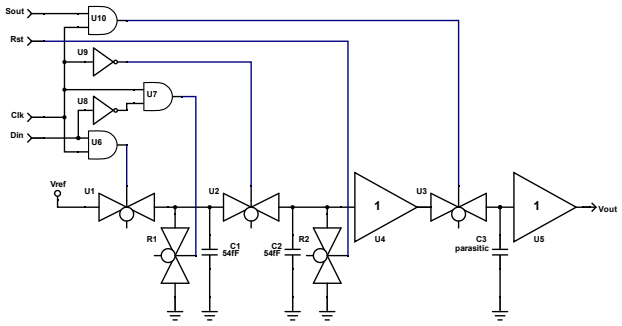

Fig. 1. Basic architecture of the charge redistribution DAC. Control signals are shown in blue. Adapted from J-Y Fourniols' course.

Fig. 1 presents the basic architecture of the system. This architecture was adapted from a theoretical model in J-Y Fourniols' data acquisition course[1]. The control part uses logic gates to derive the control signals from the inputs ports. The analog section consists of two capacitors (C1 & C2) and two buffer amplifiers. Both sections interact via transmission gates, which redirect charge onto the capacitors and the output.

A. Layout choices

In order to use a single Vdd and Vss, we designed the individual gates with two metal3 strips for the power supply, which could span the entire logic section. Inputs of the chip are routed the same way, making a bus under the the supply rails. Control signals are extracted above the supply rails, following the same principle. Although this design make for a long string of interconnected gates, which isn't optimal in terms of silicon area (therefore cost), it makes it very easy to add or modify any gate in the design by stretching the rails. The total layout area is $4.2 * 16.54 = 69.468 \mu m^2$, mainly due to the size of the capacitors.It could have been compacted by bending the main busses.

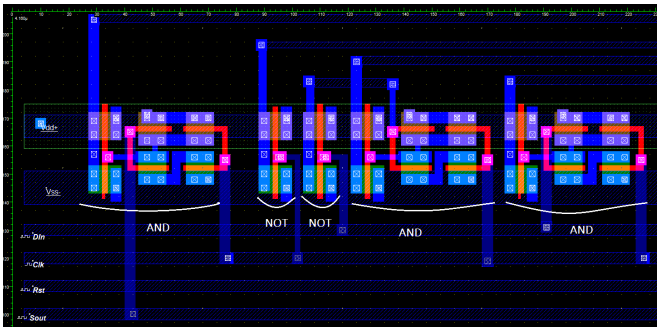

Fig. 2. Layout of the control section : notice the modular approach

B. Control section

The control section was designed from basic CMOS gates, such as AND and NOT gates. We designed modular gates in order to be able to chain them during the placement process. You can find in detail the layout of an AND gate (built with NOT and NAND gates) in Fig. 3.

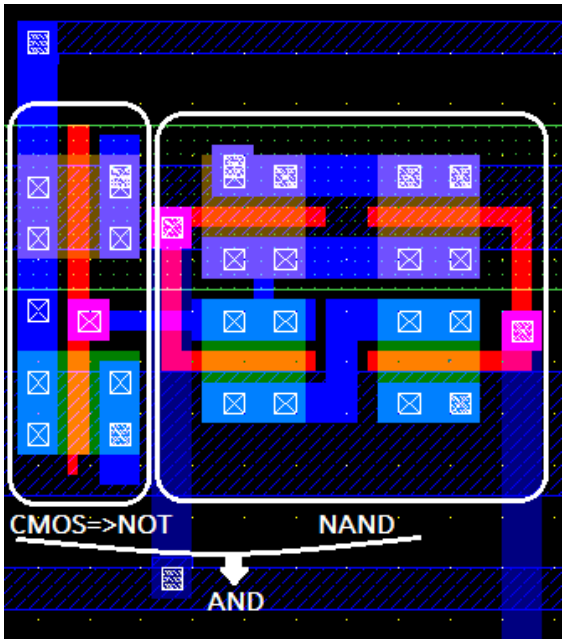

Fig. 3. The layout of an AND gate designed with Microwind

We settled on using the following inputs and outputs for the DAC :

- Clk ; input.
- Din : Data input, latched serially on a high clock level.
- Rst : system reset, active high input.
- Sout : Output latch, active high input.
- Vout : Analog output.

From these specifications we derived the control laws for each gate :

$$\begin{cases} I1 = Din \wedge Clk \\ R1 = \sim Din \wedge Clk \\ I2 = \sim Clk \\ R2 = Rst \\ I3 = Sout \wedge Clk \end{cases} \quad (1)$$

Fig. 2 shows the whole logic layout.

C. Analog section

The analog path of the DAC contains a voltage reference of $1V$, which is internal. Through a series of transmission gates, the voltages are divided between two capacitors of equal value. This is critical to guarantee the linearity and monotonicity of the system. Special care as been taken to minimize the ON-resistance of the switches in comparison to the size of the capacitors. Indeed, the losses during the charge transfer could cause an imbalance and therefore error. The layout of the switches and capacitors is shown in Fig. 4. There is a

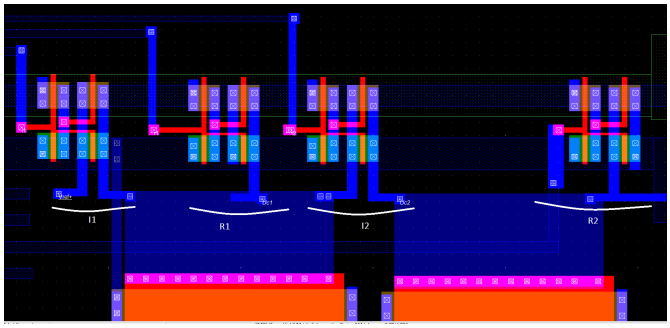

Fig. 4. The layout for the switches I1, R1, I2, R2 designed with Microwind

trade-off regarding the capacitors' size. They require a non-negligible area of silicon to get a high enough value, and they are the main speed limitation of the system, as its bandwidth is constrained by the charging/transfer time. We settled for a pair of 54fF MOS capacitors, made with polysilicon and TiN gate materials[2]. Fig. 5 shows the capacitors' layout.

The amplifiers used in this design are double differential amplifiers. We chose this topology because of its reduced error and almost rail to rail operation. The design was copied from Microwind's included component library. Fig. 6 shows the amplifiers' layout. At a later stage in the design process, we replaced the Vdd of the amplfiers with a Vdd_{HV}, around $1.5V$, which significantly reduced the offset error in our amplifier and allowed us to push the specification from 4-bits to 6-bits. Finally, Fig. 7 shows the whole layout of our 6-bit DAC.

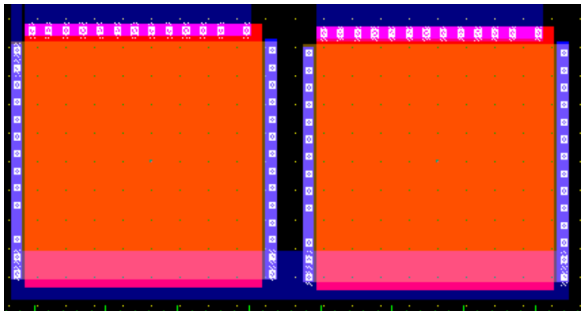

Fig. 5. Charge transfer capacitors

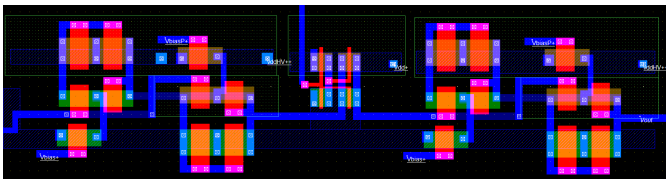

Fig. 6. The layout of the two double amplifiers

III. Test results

We simulated the converter, firstly simulating each element separately and then the system in its entirety.
However, due to the limitations in our knowledge of the software, we weren't able to automate the process of simulation for each possible input value (2^6 !), and therefore we have little results regarding Integral and Differential Non-Linearity[3]. We chose to sample the output for some input values, but we are well aware that it does not constitute a proper characterization.

A. Speed of the converter

As mentioned earlier, the main limitation for the speed of the converter is the charging time of the capacitors. For the worst case scenario of charging from 0V to near Vref (with an acceptable error less than 1/2 LSB), the charge transfer period must be at least $\approx 1.25ns$. Knowing the value of the capacitors, we can estimate the switches' ON-resistance (and layout resistance) using the following equation :

$$R_{on} = -\log(\frac{1}{2 \times 2^{bits}}) \times \frac{\tau_{min}}{C} = 4.85 \times \frac{1.25n}{54f} \approx 100\Omega \quad (2)$$

Due to the serial nature of our architecture, each bit must be held sequentially for the minimum hold time, and each bit must be followed by a discharge period for the C1 capacitor. Therefore, for a 6-bit converter, we need $(2 \times 6 + 2) \times 1.25ns = 20ns$ to output the data (accounting for Sout and Rst bits), resulting in a maximum throughput of 50Msps.

B. Resolution and sources of error

Through testing of the DAC, we discovered that the charge transfer process yielded very good results in terms of accuracy, that is, very little charge was lost during transfers.
The main issue was the amplifiers offsets and non-linearity, especially near the supply rails. Although we used double

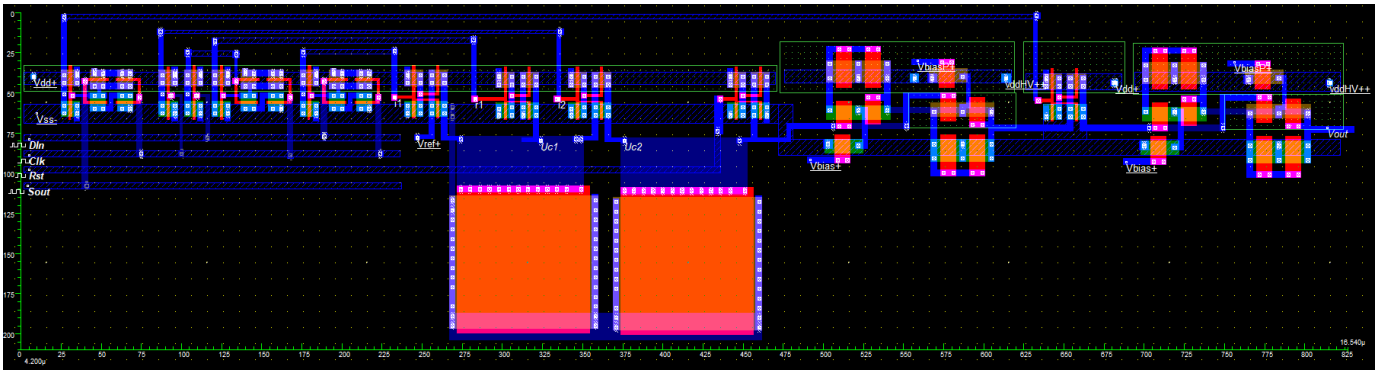

Fig. 7. The complete layout of our 6-bits DAC, designed in Microwind

differential amplifiers, there was still a significant offset, which limited us to using 4-bits.
Otherwise, with a voltage supply of 1V for the amplifiers, we obtained an error rather close to the 1 LSB of 6-bits. In order to decrease this error, we decided to use 1.5V for V_{DD} which allow us to reduce by half the error (see the next section for more details).

C. Simulations of the DAC

We will go through the analysis of performance with a sample test. The chosen binary value is 0b100101. This value matches to 0.640625 after calculating by the following method :

$$\begin{cases} '1' \Longrightarrow \frac{1+0}{2} = 0.5 \\ '10' \Longrightarrow \frac{0.5+0}{2} = 0.25 \\ '100' \Longrightarrow \frac{0.25+0}{2} = 0.125 \\ '1001' \Longrightarrow \frac{0.125+1}{2} = 0.5625 \\ '10010' \Longrightarrow \frac{0.5625+0}{2} = 0.28125 \\ '100101' \Longrightarrow \frac{0.28125+1}{2} = 0.640625 \end{cases} \quad (3)$$

Din is a PWL signal with a time-period of $2.5ns$ for each binary value of the data sent. Then the signal Clk is a pulse with a time-period of $2.5ns$ (1.25ns for both high level '1' and low level '0'). The RST and SOUT signals are also PWL types.
We tested in 3 conditions using the "process variable" option during the simulations :

- normal conditions (temperature of 25°C, typical voltage supply)
- minimal conditions (slow, high temperature (until 125°C), low voltage)
- maximal conditions (fast, low temperature (until −50°C), high voltage)

You will find the results for these simulations below.

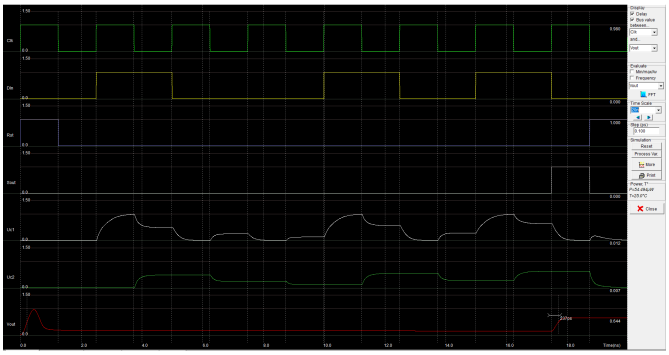

Fig. 8. Results of the DAC simulation with typical conditions

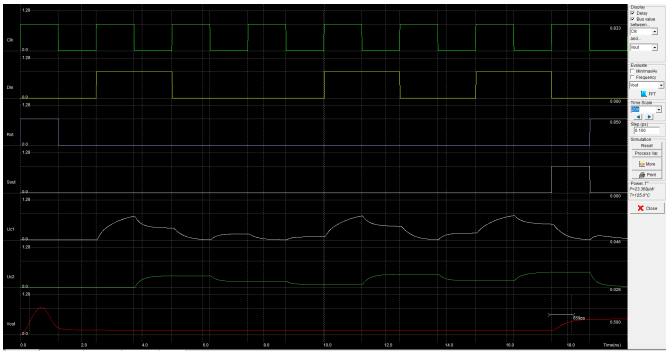

Fig. 9. Results of the DAC simulation with minimal conditions

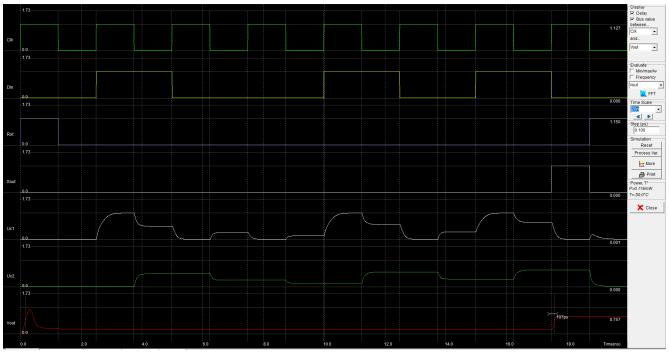

Fig. 10. Results of the DAC simulation with maximal conditions

D. Analysis of the output value

The threshold error before losing a bit is :

$$error = \frac{1}{2^6} = \frac{1}{64} = 1.56\% \tag{4}$$

We can notice in Fig. 8 that the obtained output value is 0.644. If we calculate the error of conversion, we obtained :

$$\begin{aligned} error &= \frac{|RealValue - TrueValue|}{TrueValue} \\ &= \frac{0.644 - 0.640625}{0.640625} = 0.58\% \end{aligned} \tag{5}$$

We can deduce that the specification of the loss of one bit is respected. Our 6-bit DAC provides fairly precise output values during typical conditions, that is a correct supply voltage supply and standard temperature.

However, we do not have the same results with critical conditions. Indeed, for a minimal simulation showed in Fig. 9, the final value is 0.500 which generates the following error :

$$error = \frac{|0.500 - 0.640625|}{0.640625} = 21.95\% \tag{6}$$

We can make the same observation during a maximal simulation showed in Fig. 10:

$$error = \frac{|0.757 - 0.640625|}{0.640625} = 18.16\% \tag{7}$$

We deduce that for both minimal and maximal cases we lose several bits. So our DAC presents a serious lack of robustness towards extreme conditions. This can be due to the amplifiers design : analog components are tricky to calibrate precisely and sensitive to polarization values. Furthermore, it also depends on the values of the bias voltages that we put for the differential pairs. Error propagation may occur when connecting different logical gates with the analog components. This is a real issue that would have required us to carefully investigate the sources of drift and error, and suggest solutions to counter-balance the temperature drifts. This is an area of improvement for future work. However, our time in this project was limited, and we could not investigate further.

E. Analysis of the power consumption

For a typical simulation, we obtain a power consumption of 54.494μW which seems normal for a DAC. Howewer, with the maximal conditions, the power consumption reach $0.119mW$ which is rather high for a 6-bit DAC. Finally with minimal conditions, we obtain 23.369μW.

IV. Conclusion

To put it in a nutshell, this lab allowed us to experiment the design of active components in order to built typical structures that take part of every kind of embedded circuits, microprocessors, FPGA...
Moreover, it raised awareness of the different rules of design which are essential for a strong optimization and in order to obtain the highest possible performance (operation with high/low temperatures, power consumption...), particularly by respecting the recommended width for the strips of materials (TiN gate...) depending on the function to realize, or properly arrange the blocks to optimize the occupied area. In addition, taking care of having one V_{DD} and one V_{SS} is important because there is often only one pin for each of them. Through this project, we acquired the basics of mixed-signals CMOS design, and discovered the challenges asociated with that. This project helped us to put into practice the knowledge acquired during P.Tounsi EMCA course. We appreciated working on it. The sessions were very interesting and instructive.

References

[1] S. Sahin and L. Val, *Serial DAC Design*. http://srv-wwwperso.insa-toulouse.fr/s̃icard/microwind/, 2014.
[2] E. Sicard and S. Delmas Bendhia, *Basics of CMOS Cell Design*. Toulouse, FR: Mc GrawHill Education, 2007.
[3] ——, *Advanced CMOS Cell Design*. Toulouse, FR: Mc Graw Hill Education, 2007.