

Vout: (R253)2x 39k in //

Sync block: Removed C77 -> to be replaced with 10nF

F dividers: C70 C71 -> 470n+1u+1u (1u seem LV type, 470n has more effect)

Hours/Minutes button: D301/D323 add 39k pulldown from 100n cap diode side to GND

RST CLK generators: replaced R90,R118,R52,R18 by 4700hms, added 10k to Q45,Q59,Q26,Q9 B-E

R168 (24hr clk) to 1.96k?

PSU: added 12V 47u electrolytic cap in // to C74

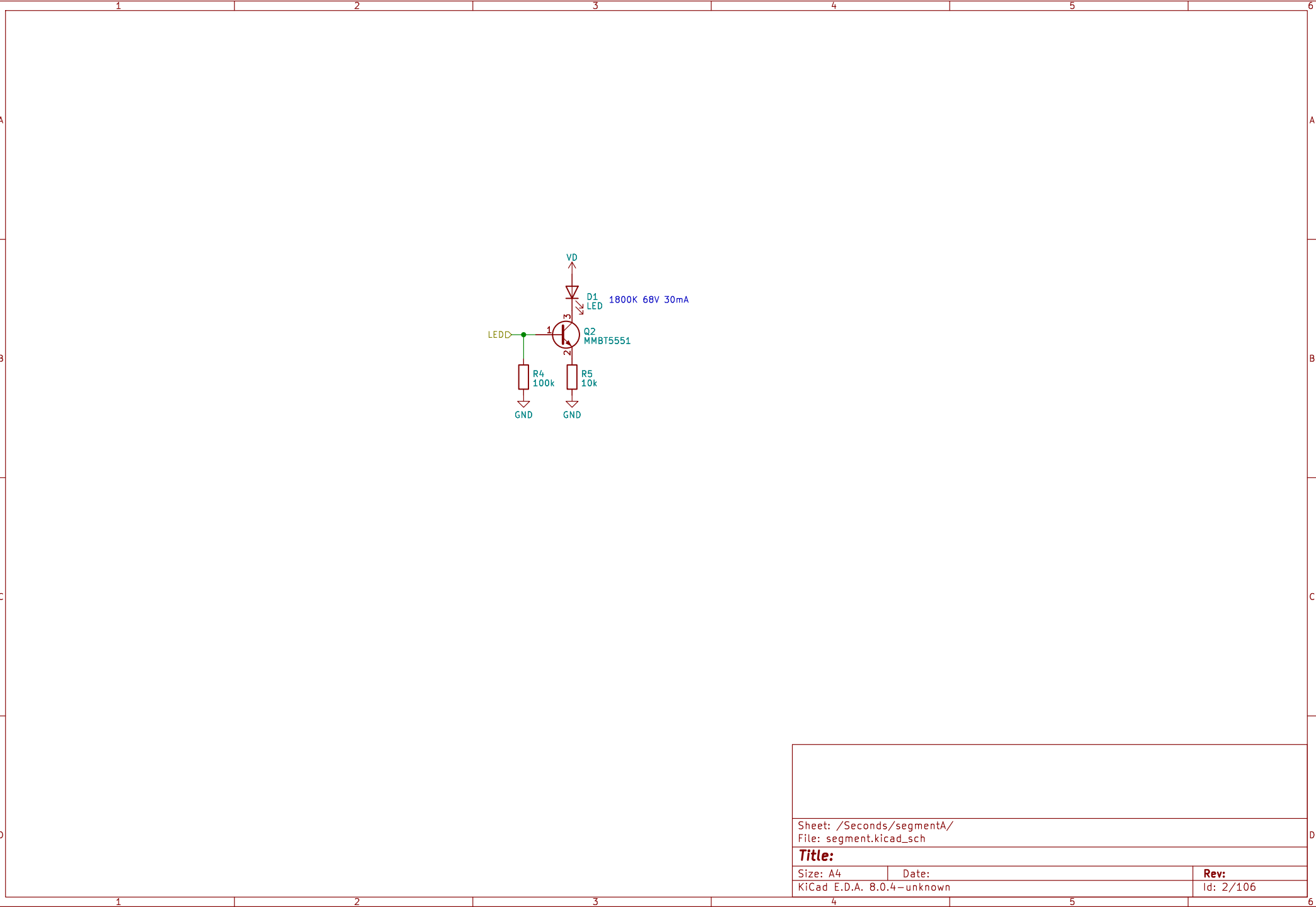
Not necessary: R252 replace BAT54, R253=39k//33k

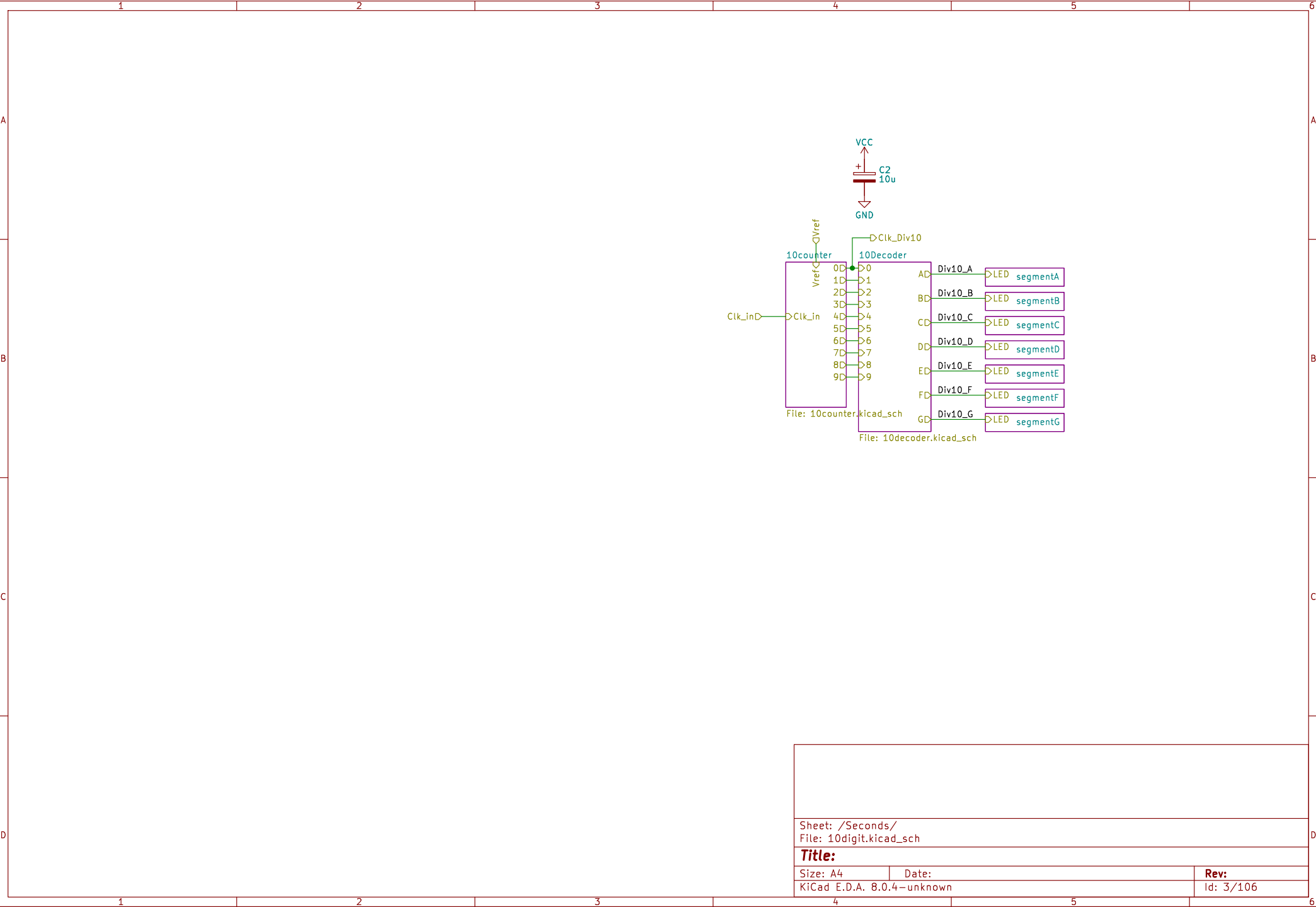
PSU\_ R254=12k

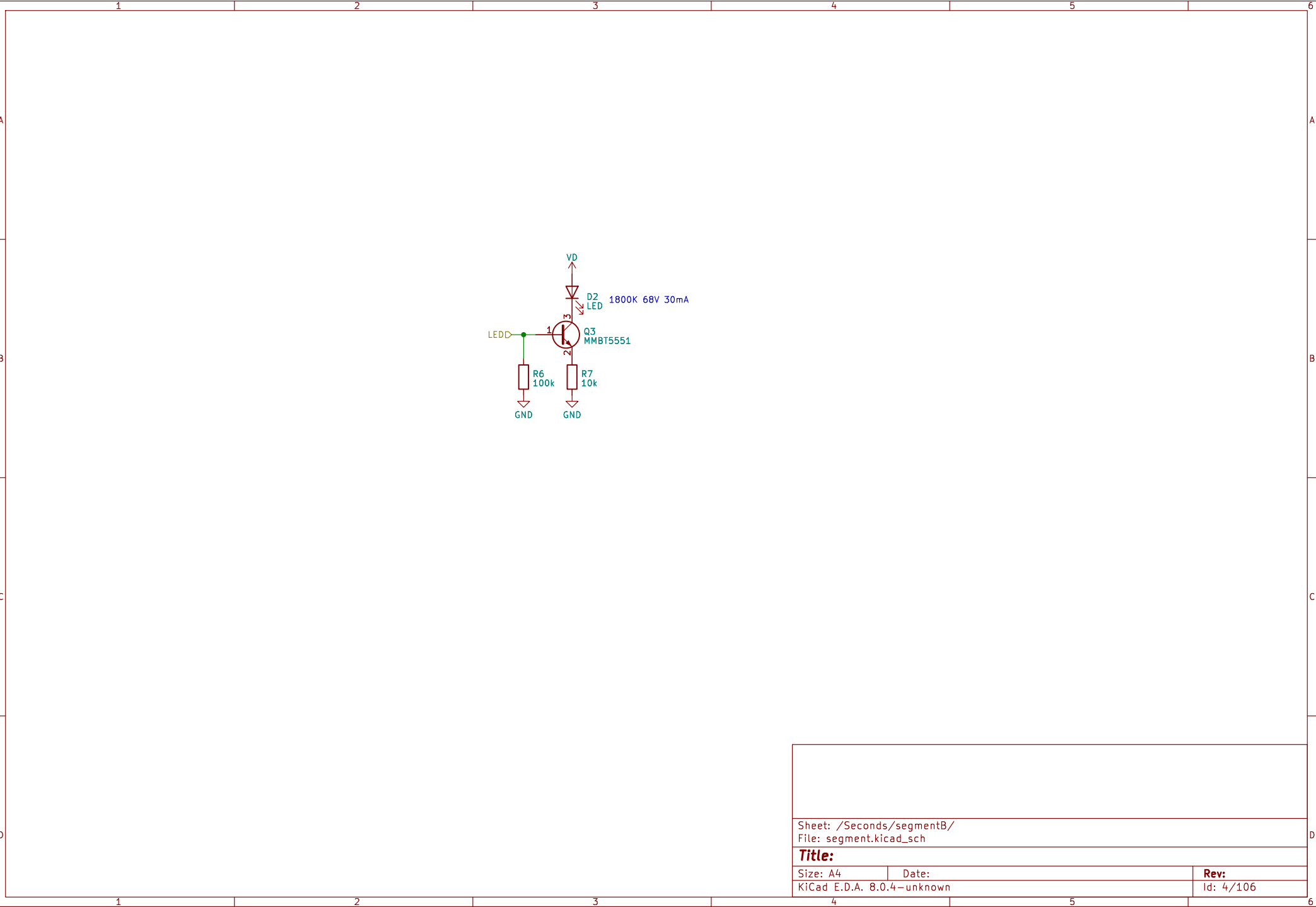
Vref R2=33k//39k, R1=3.3k

TODO check voltage + add LDR?

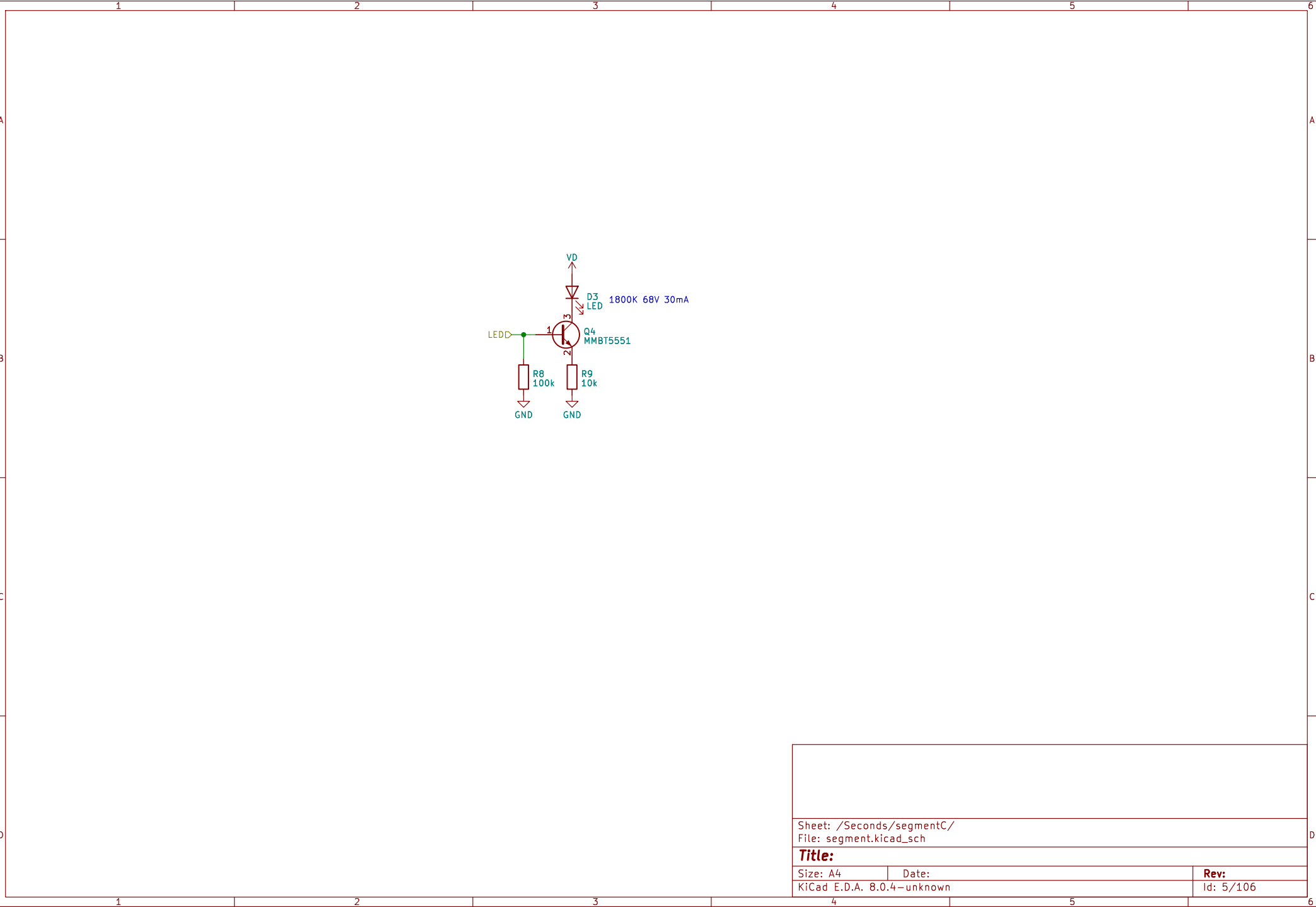
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KiCad E.D.A. 8.0.4-unknown		Id: 1/106

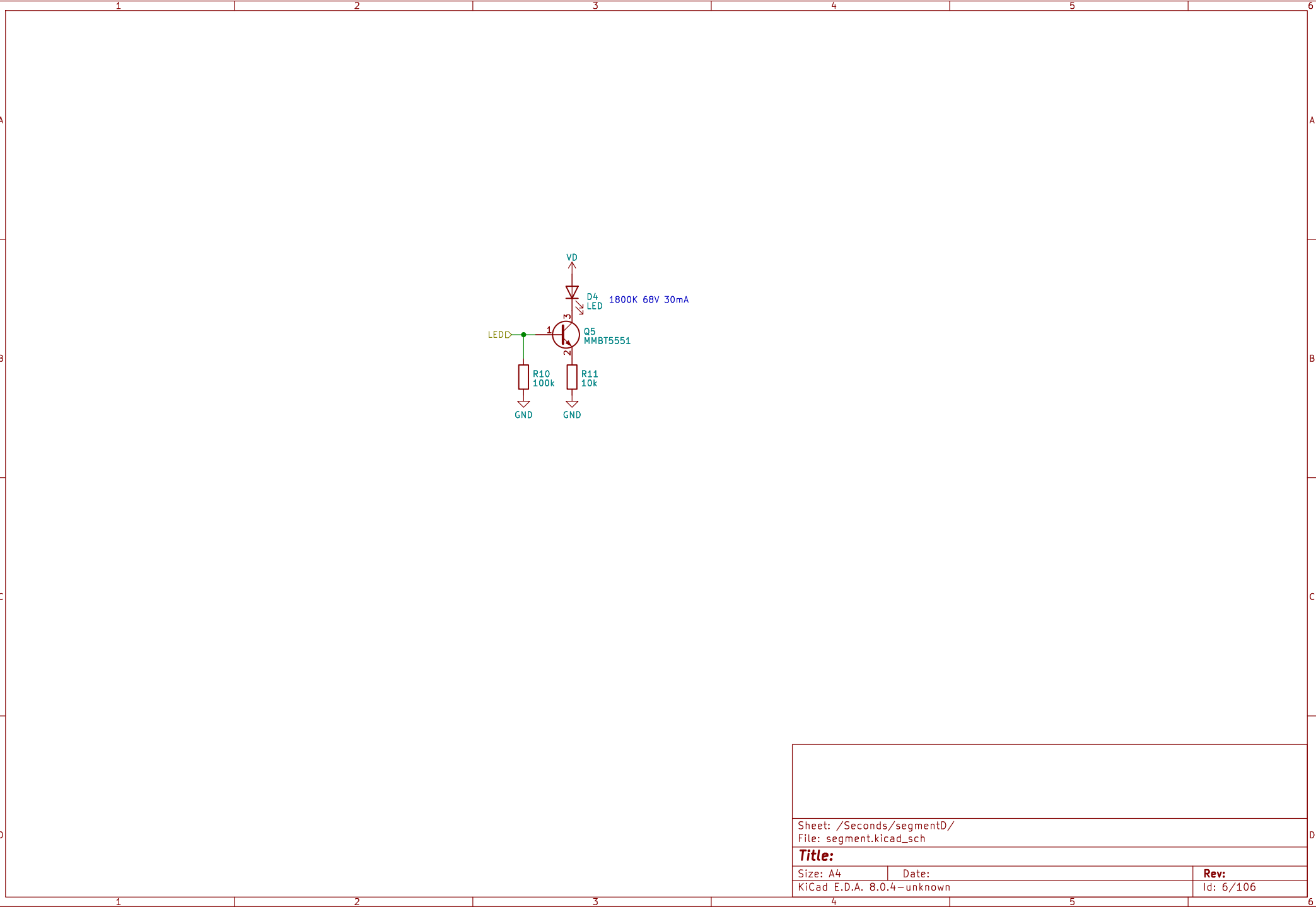


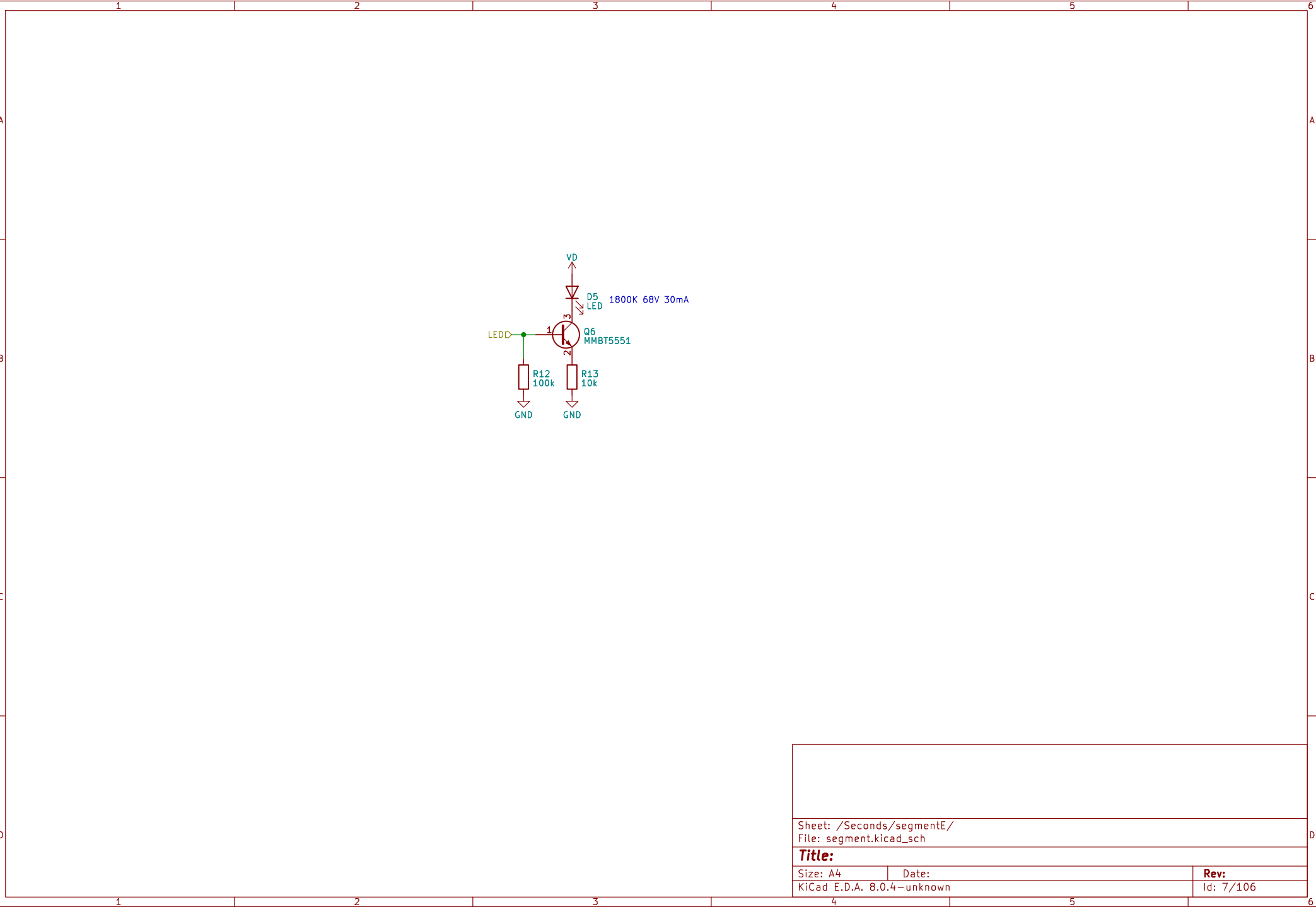


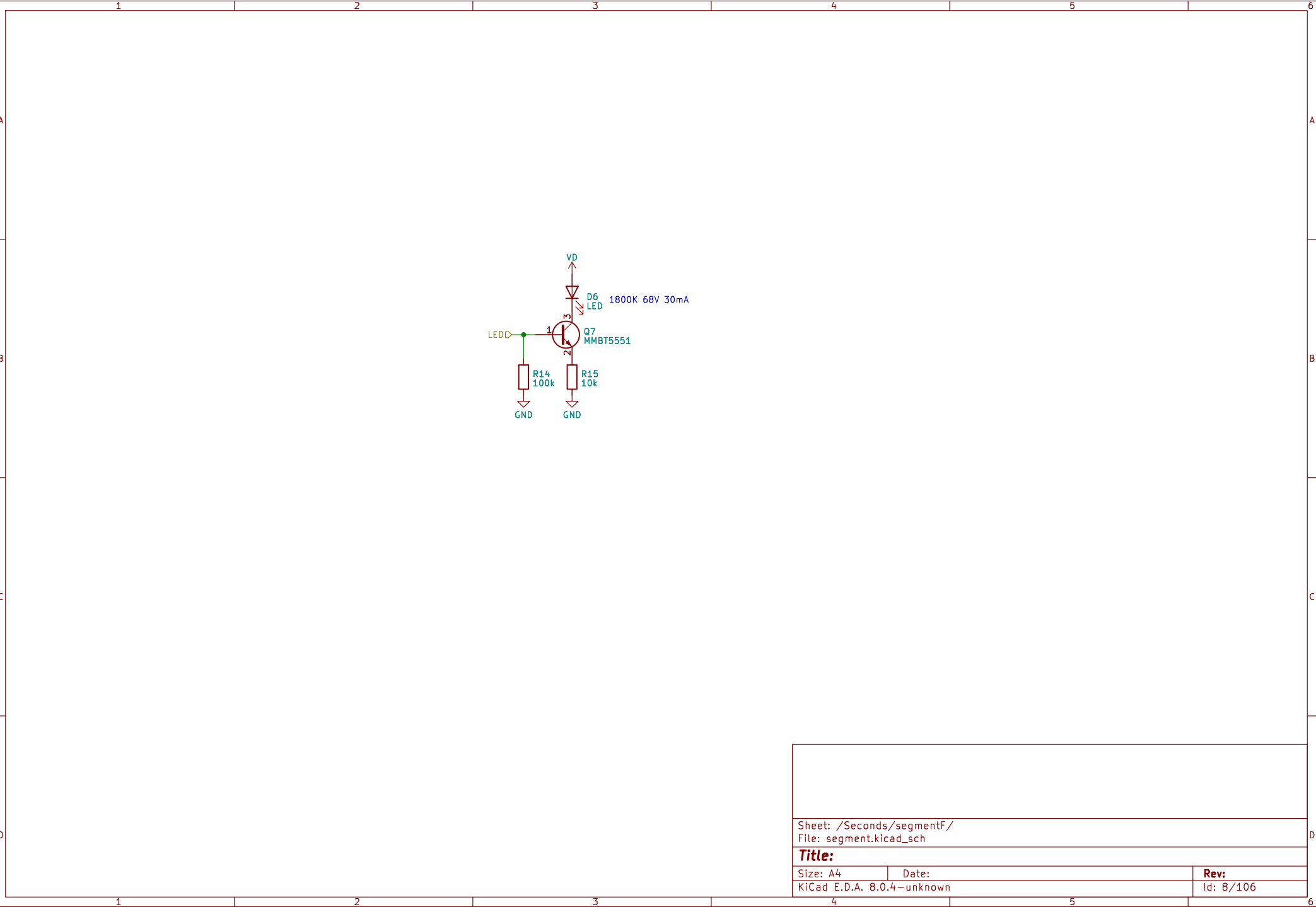


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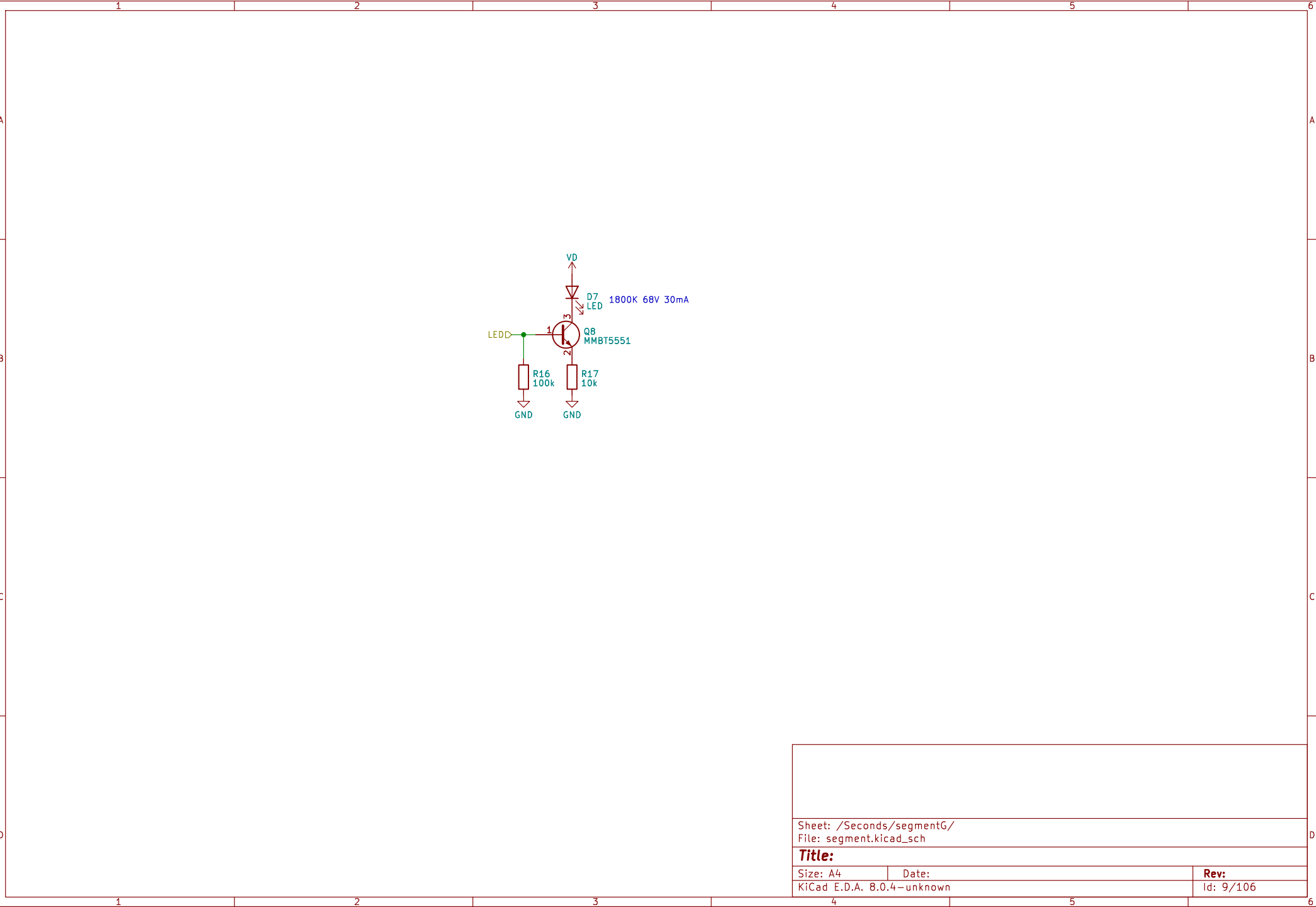


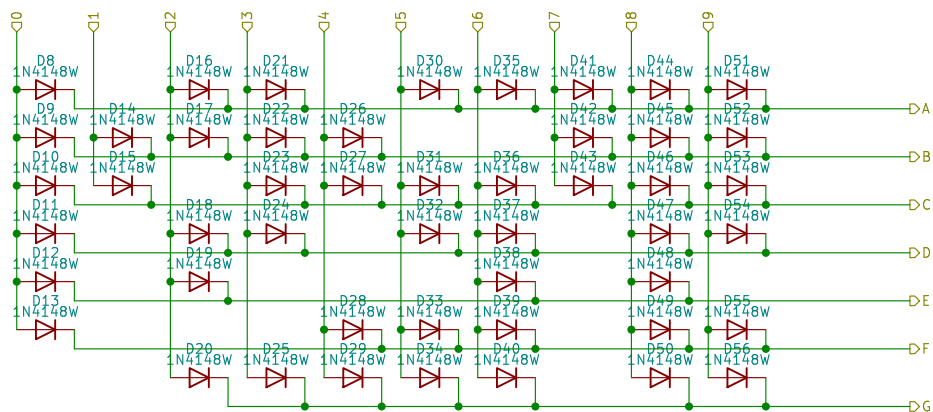












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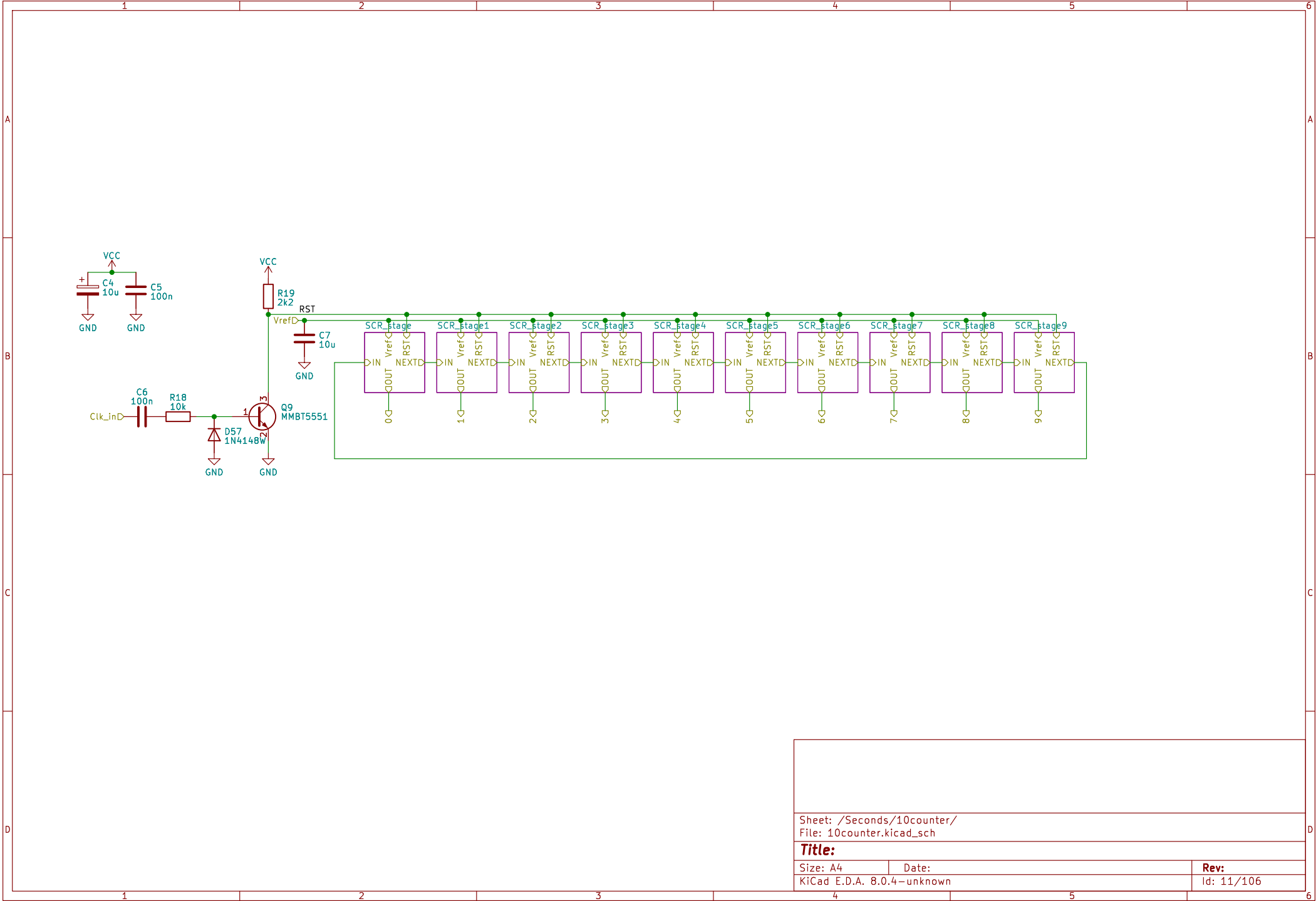
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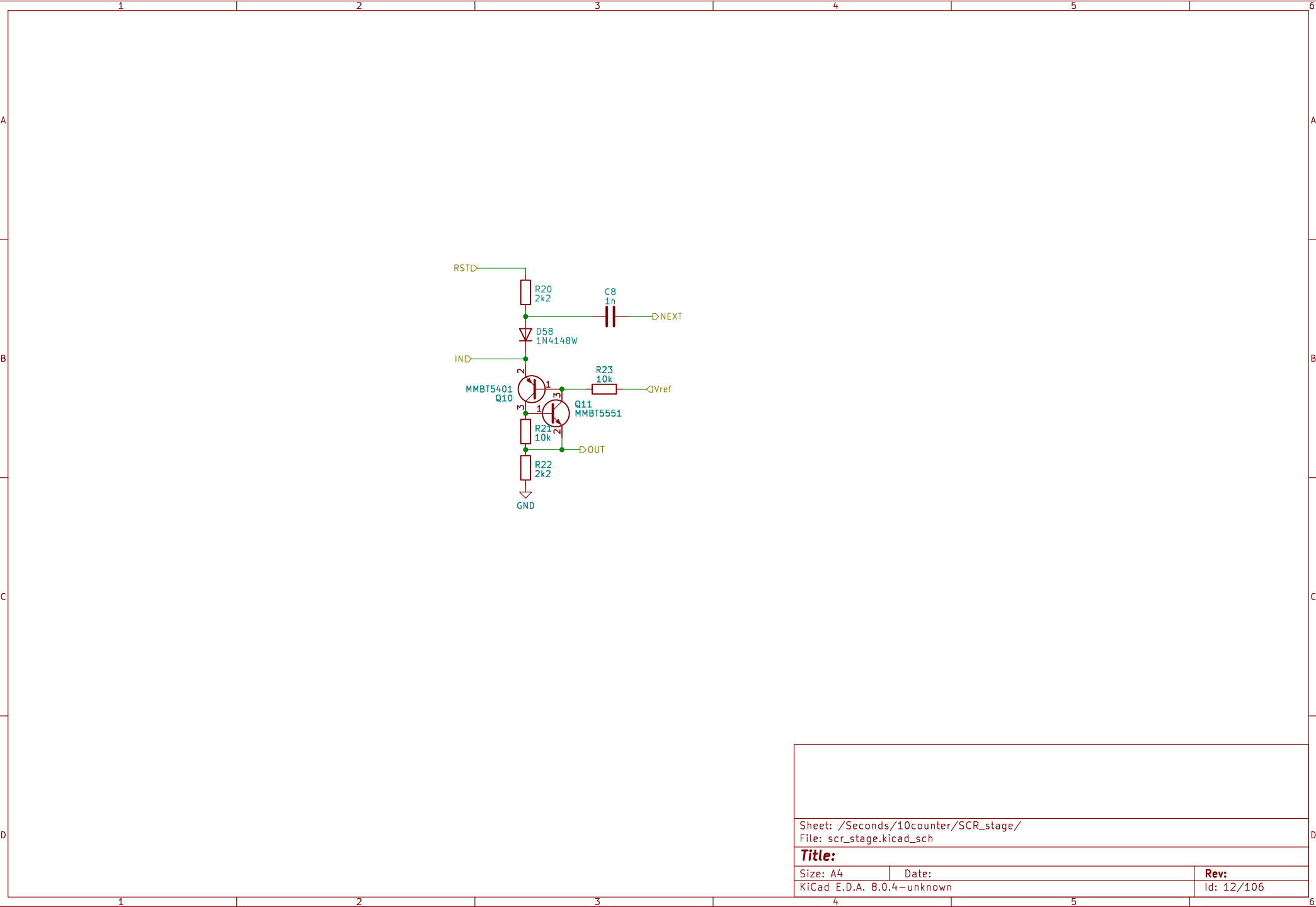
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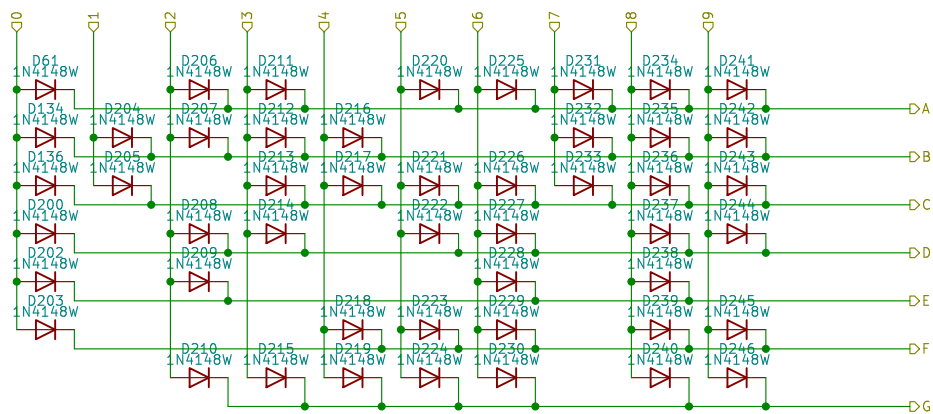
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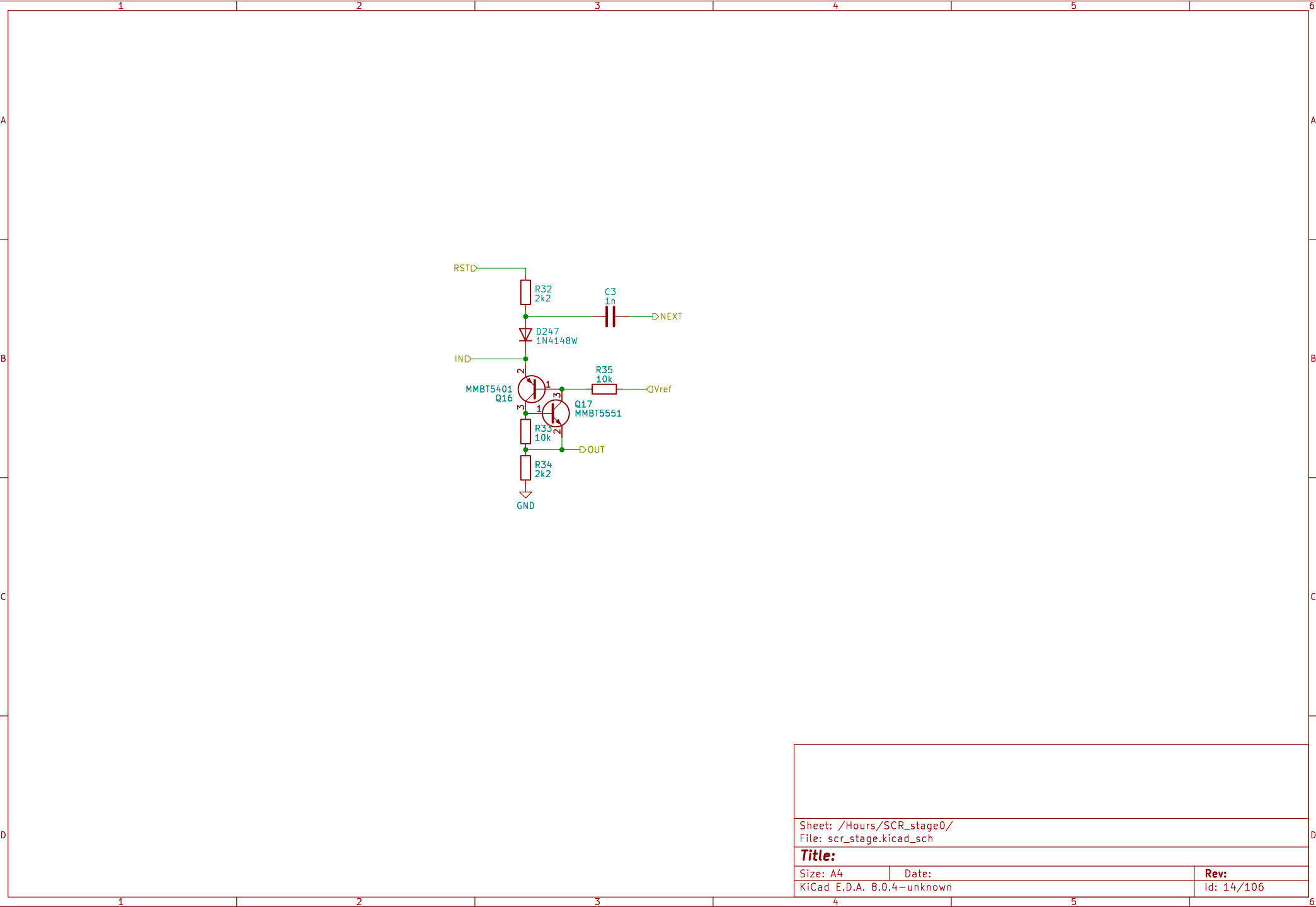
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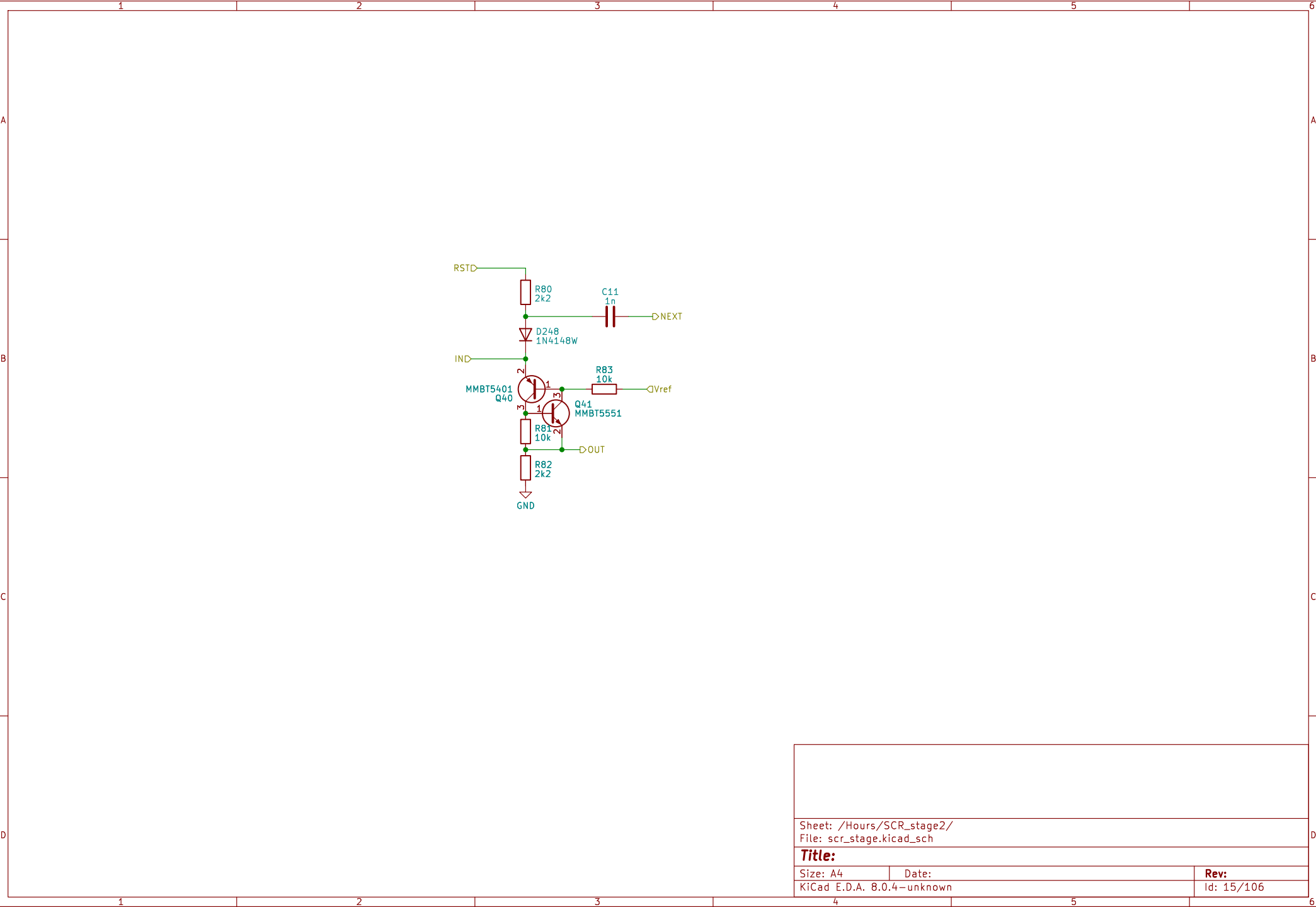
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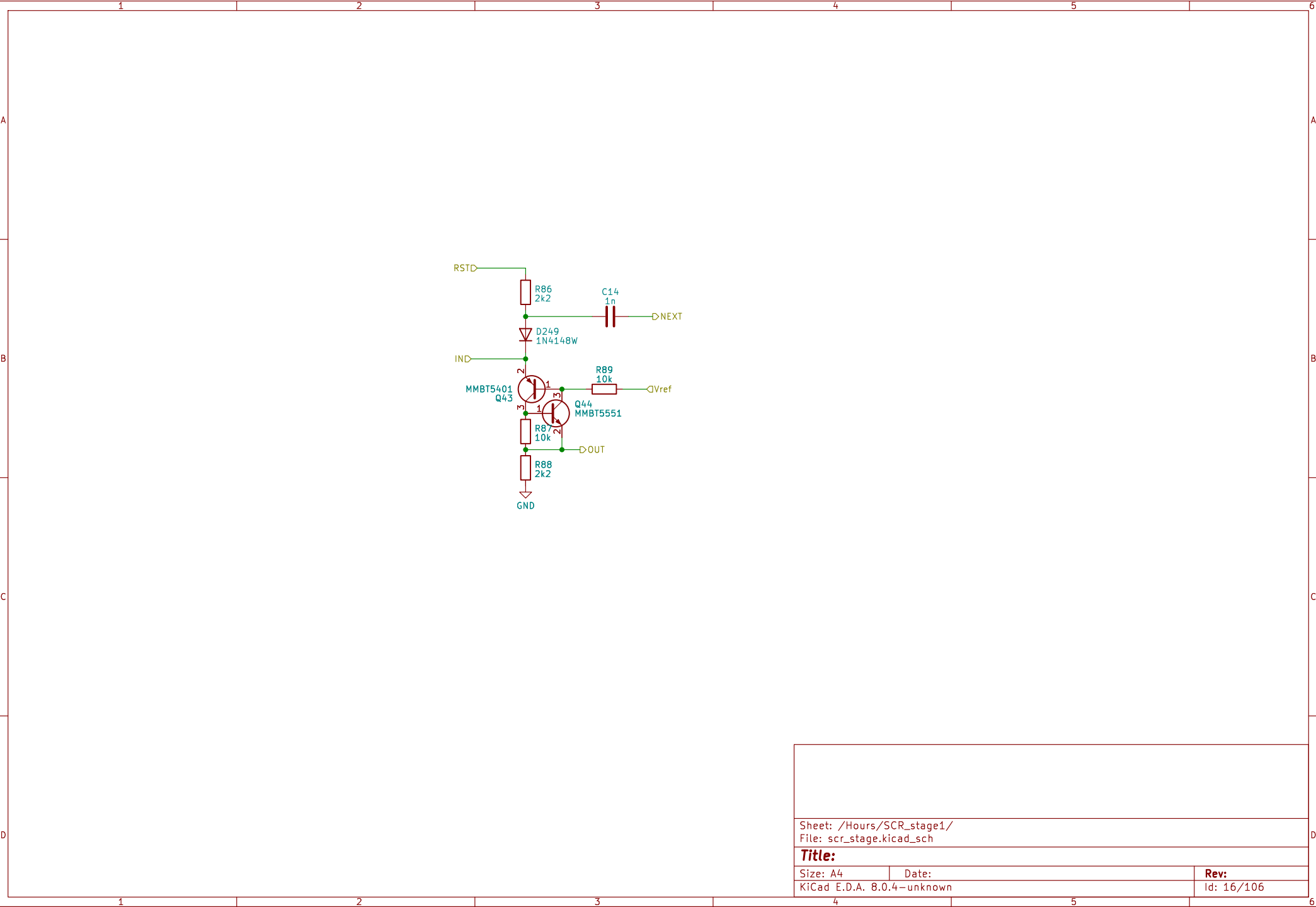
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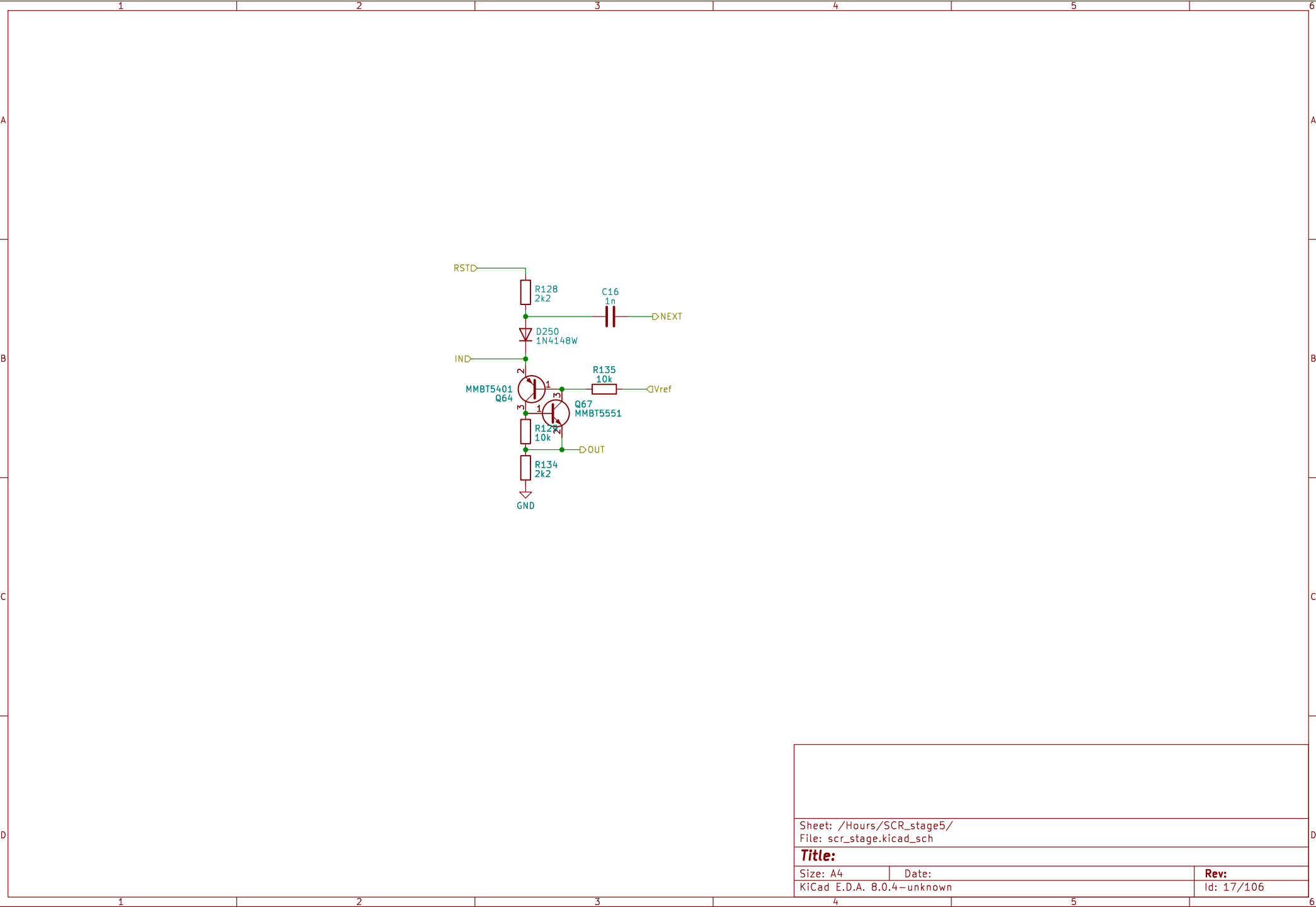
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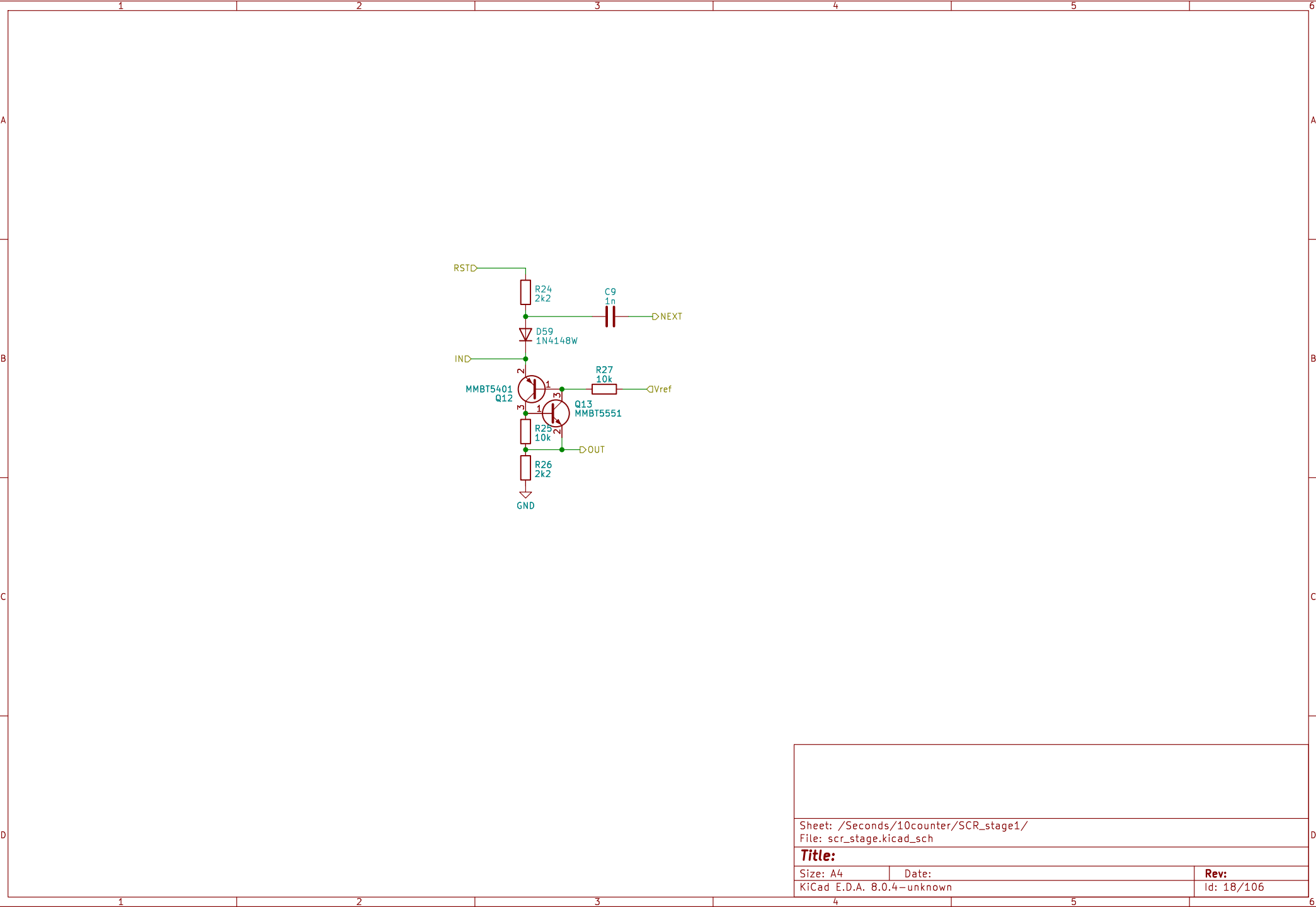


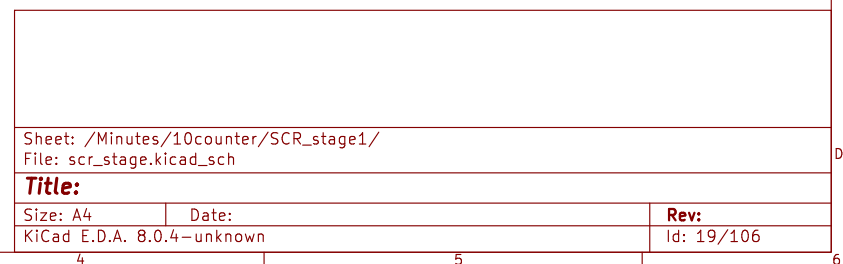


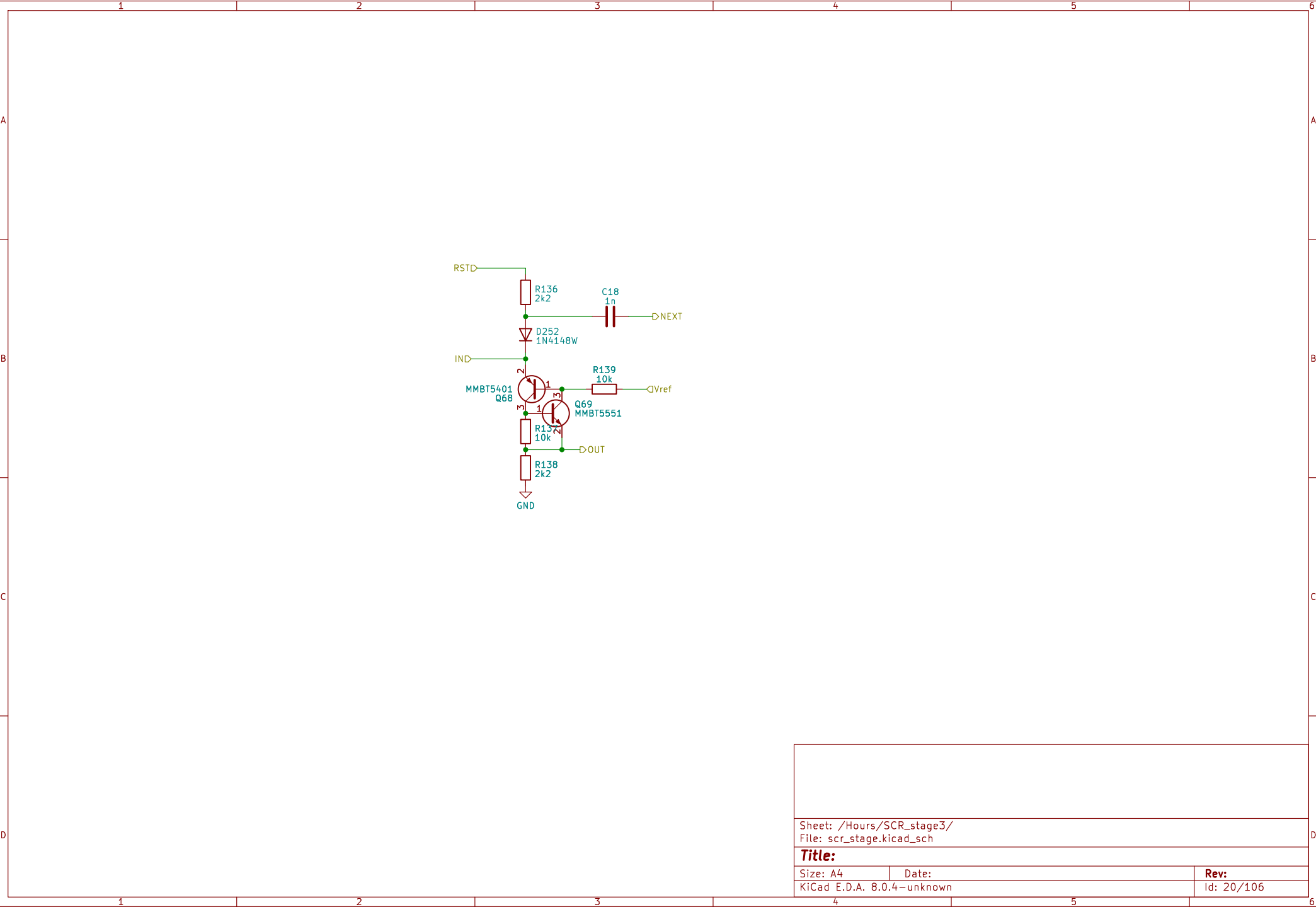


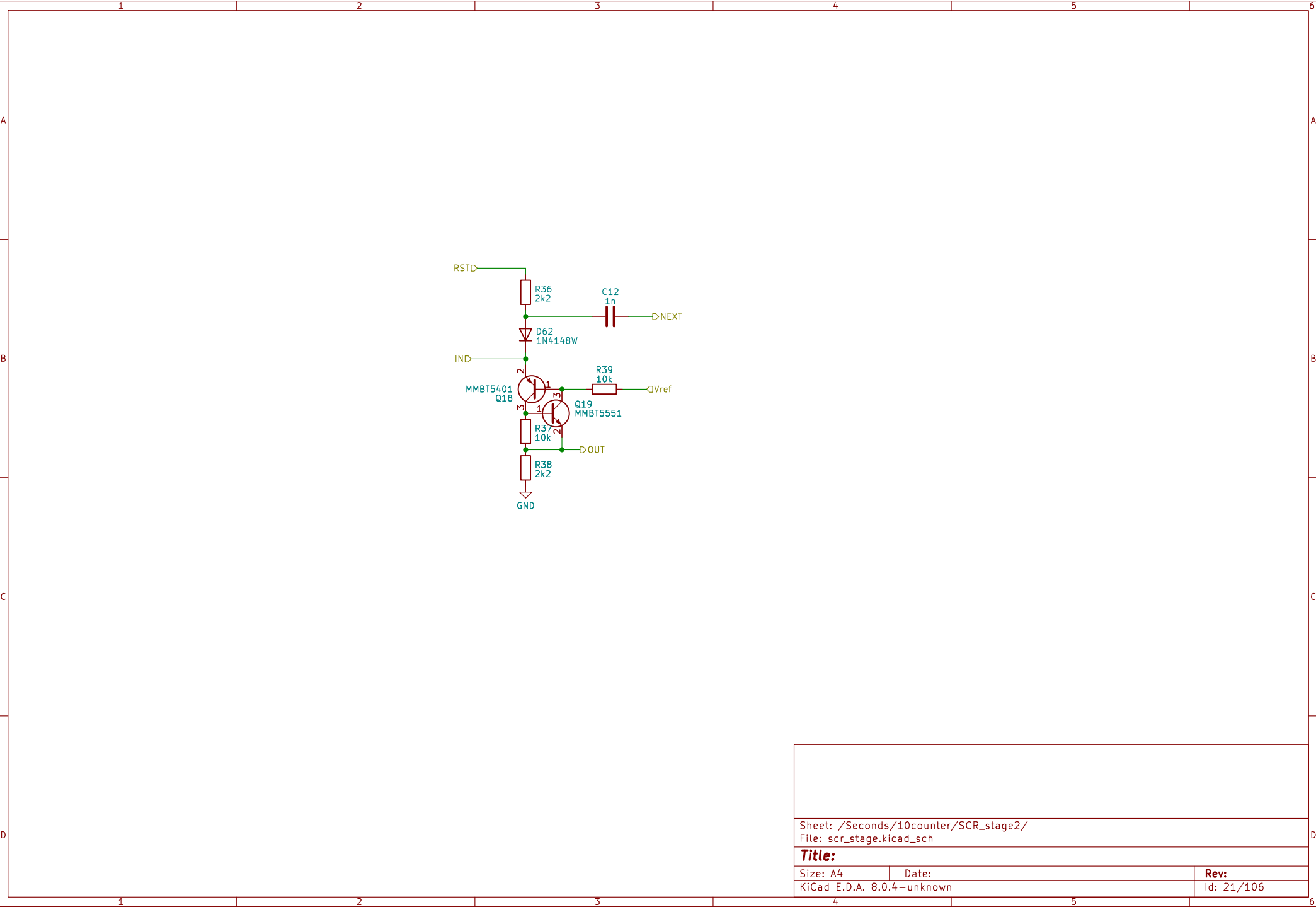


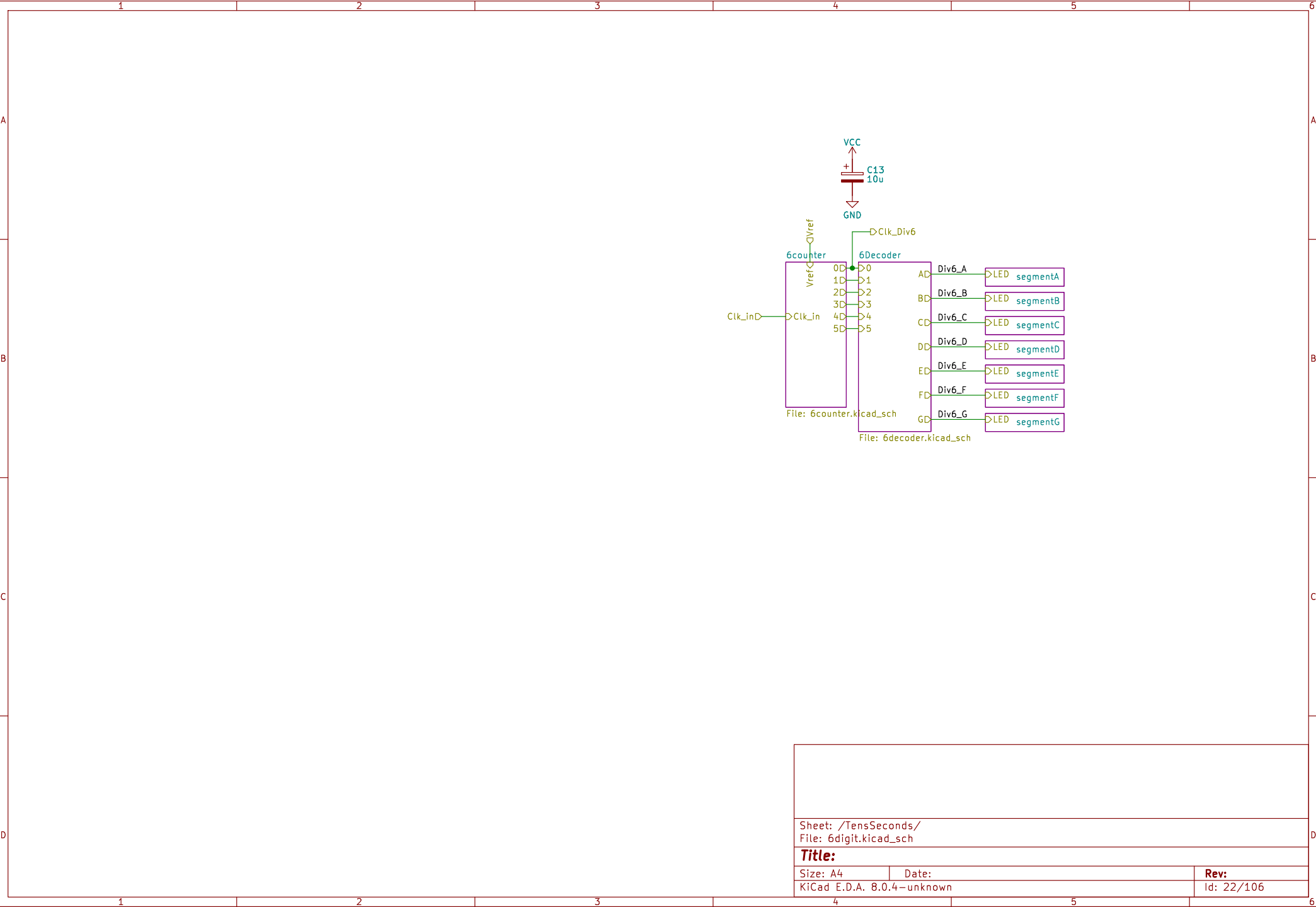




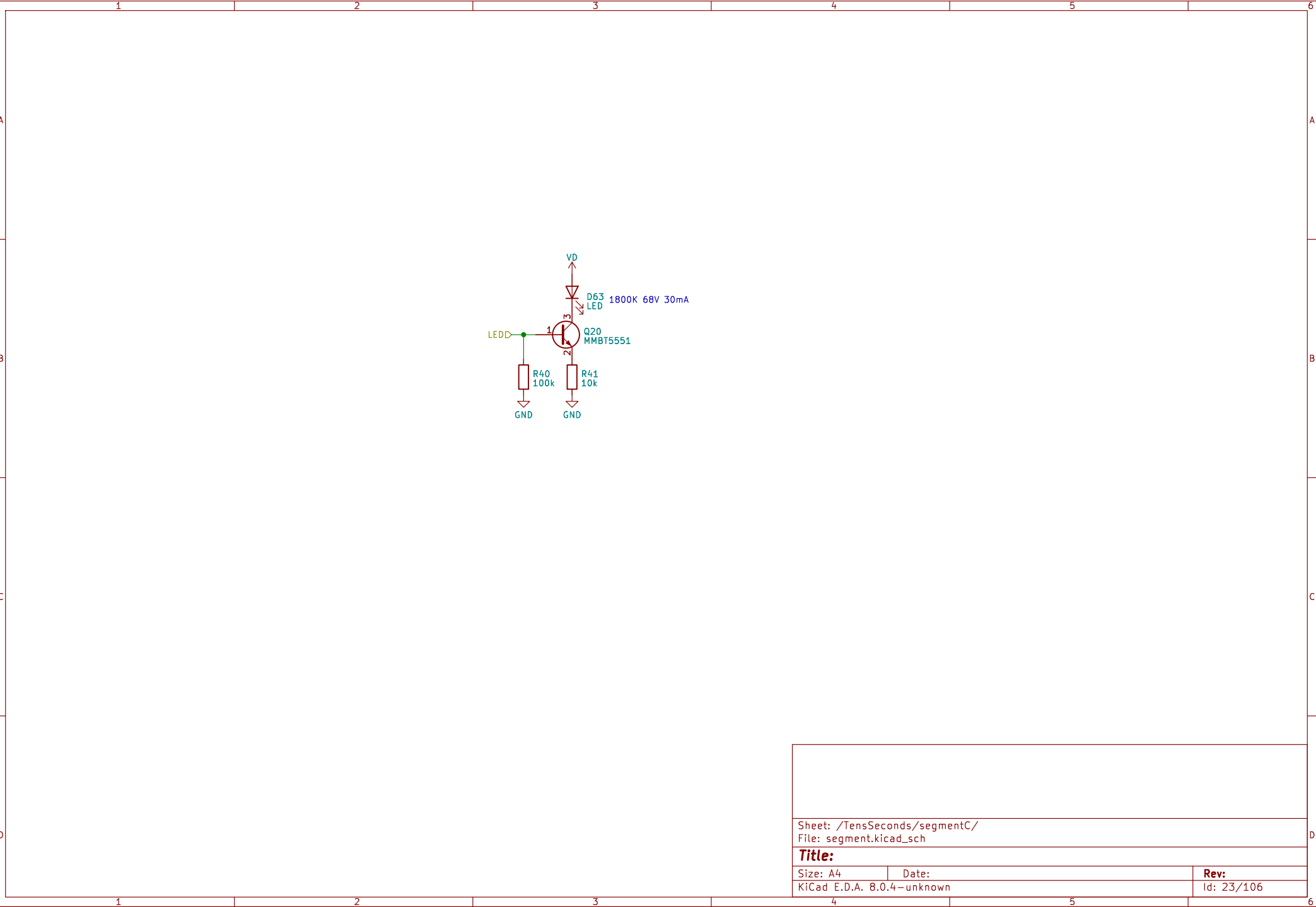


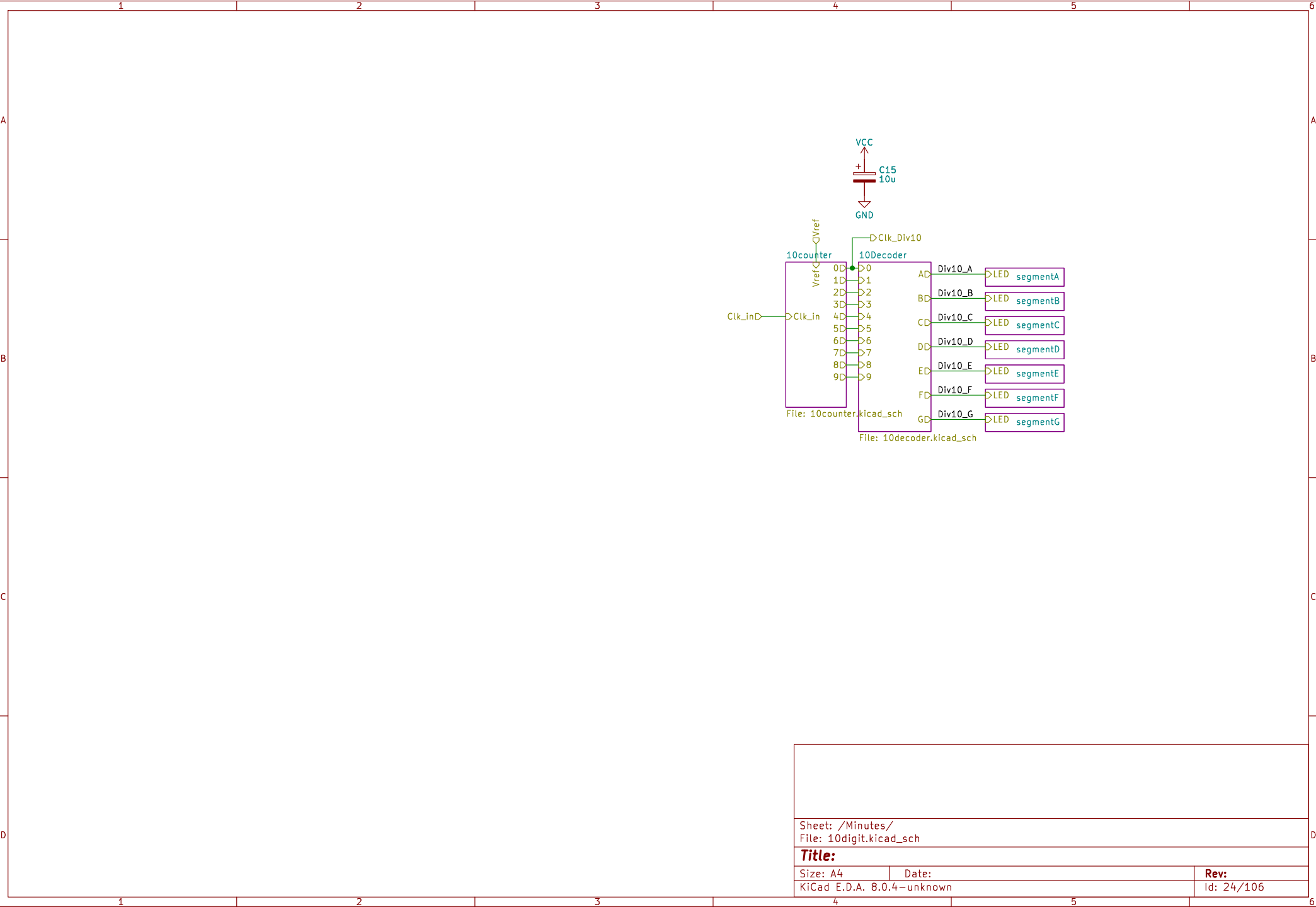




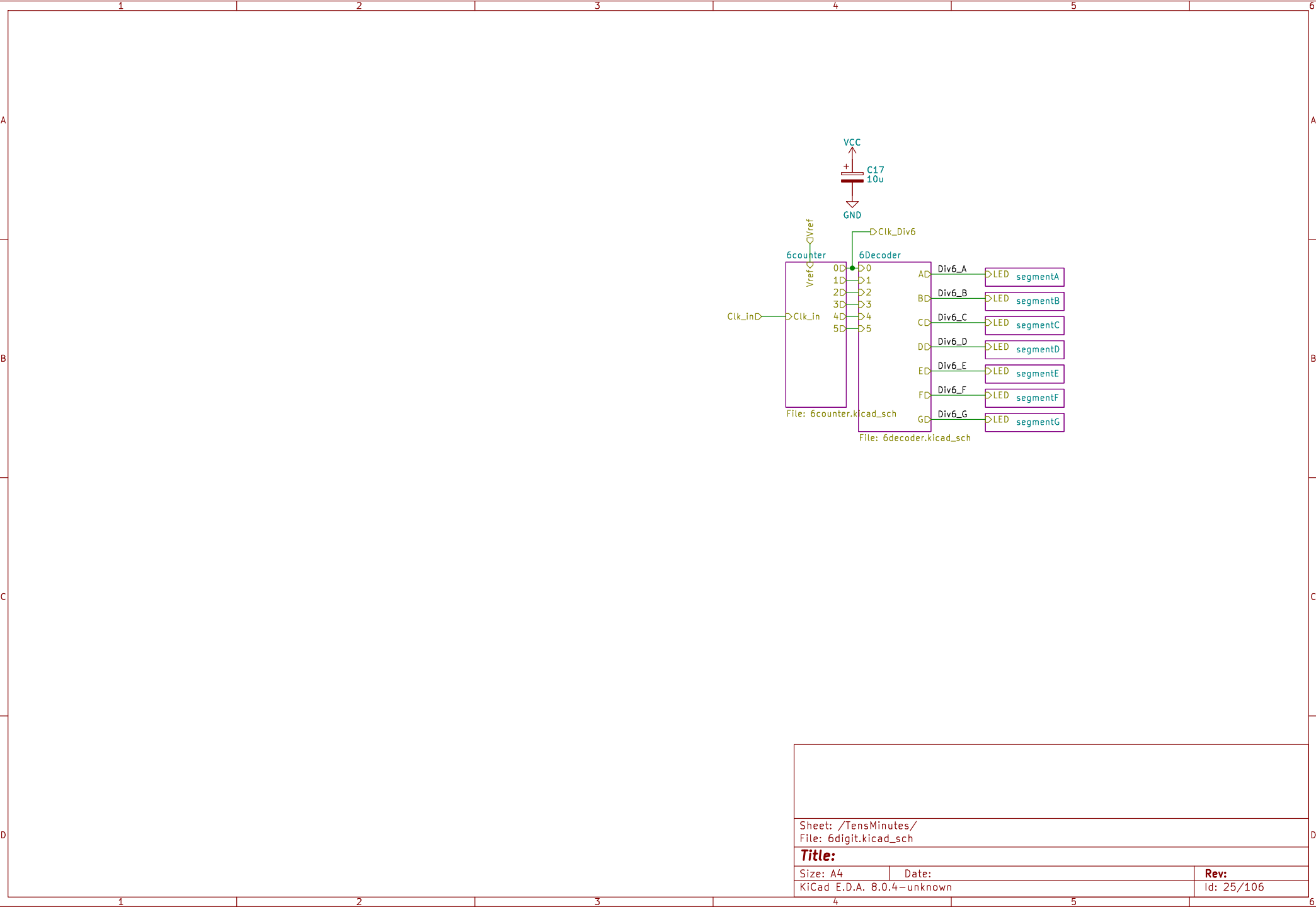


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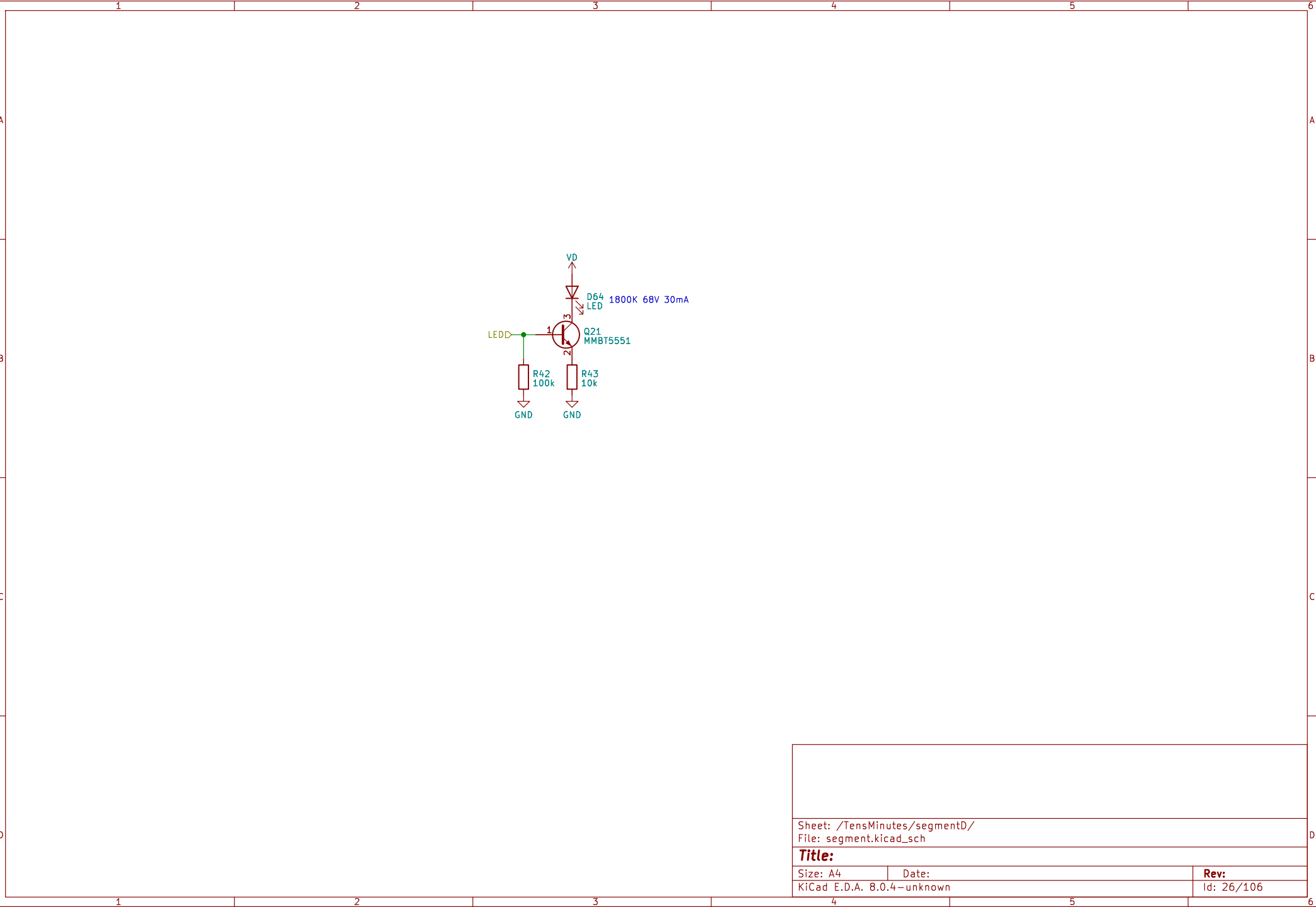


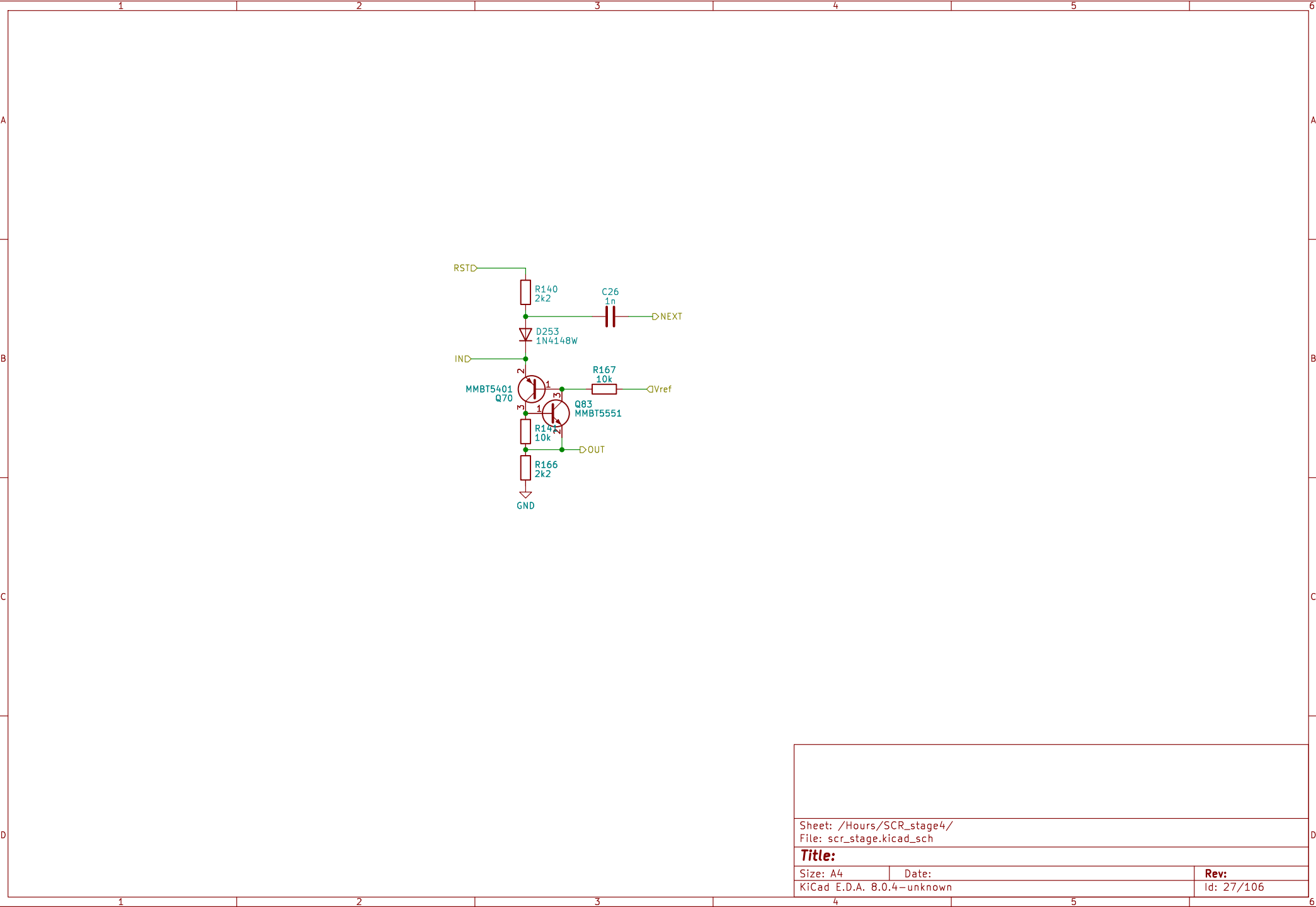


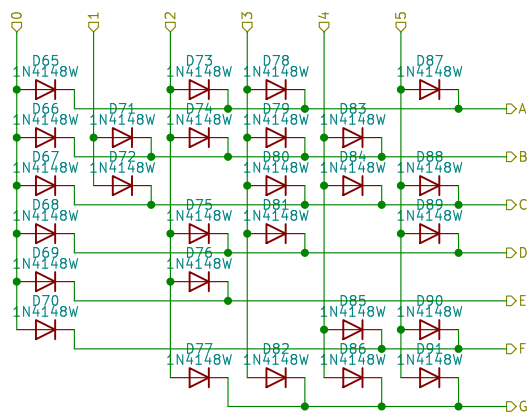




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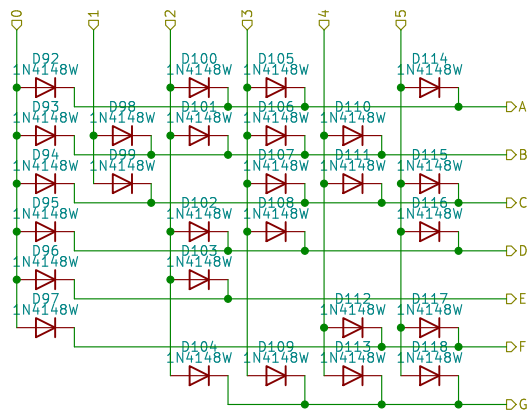
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**Rev:**

Id: 28/106



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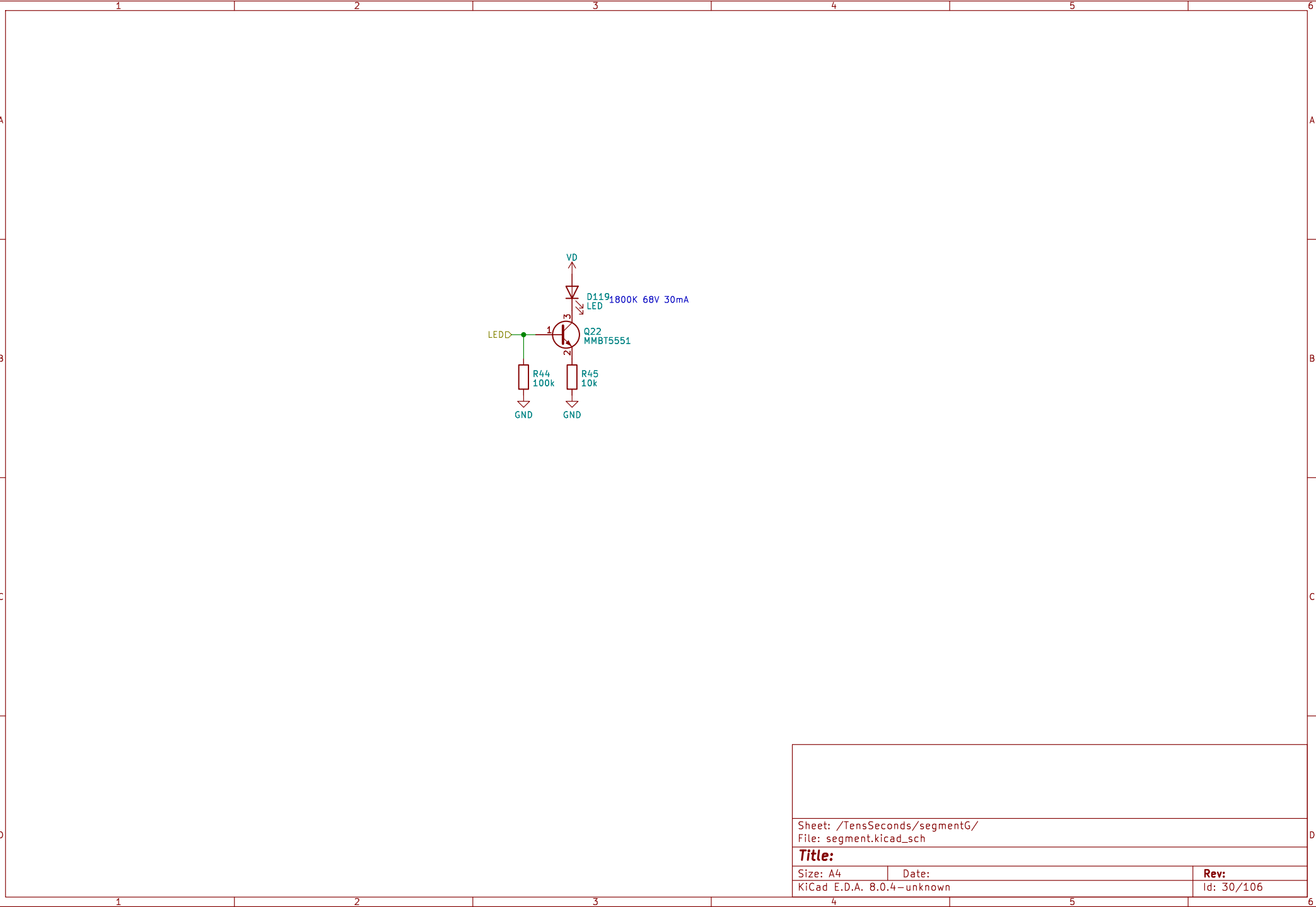
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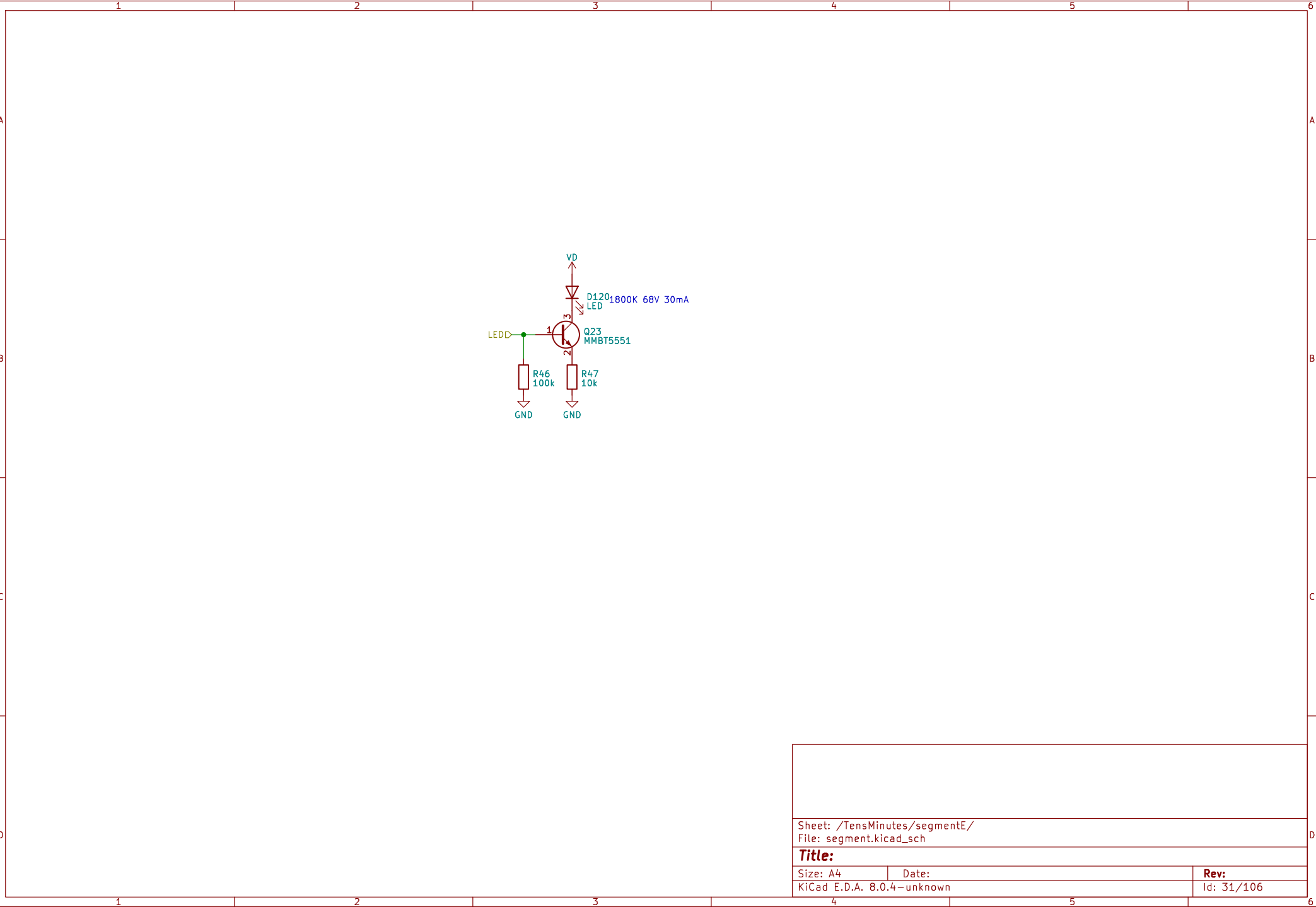
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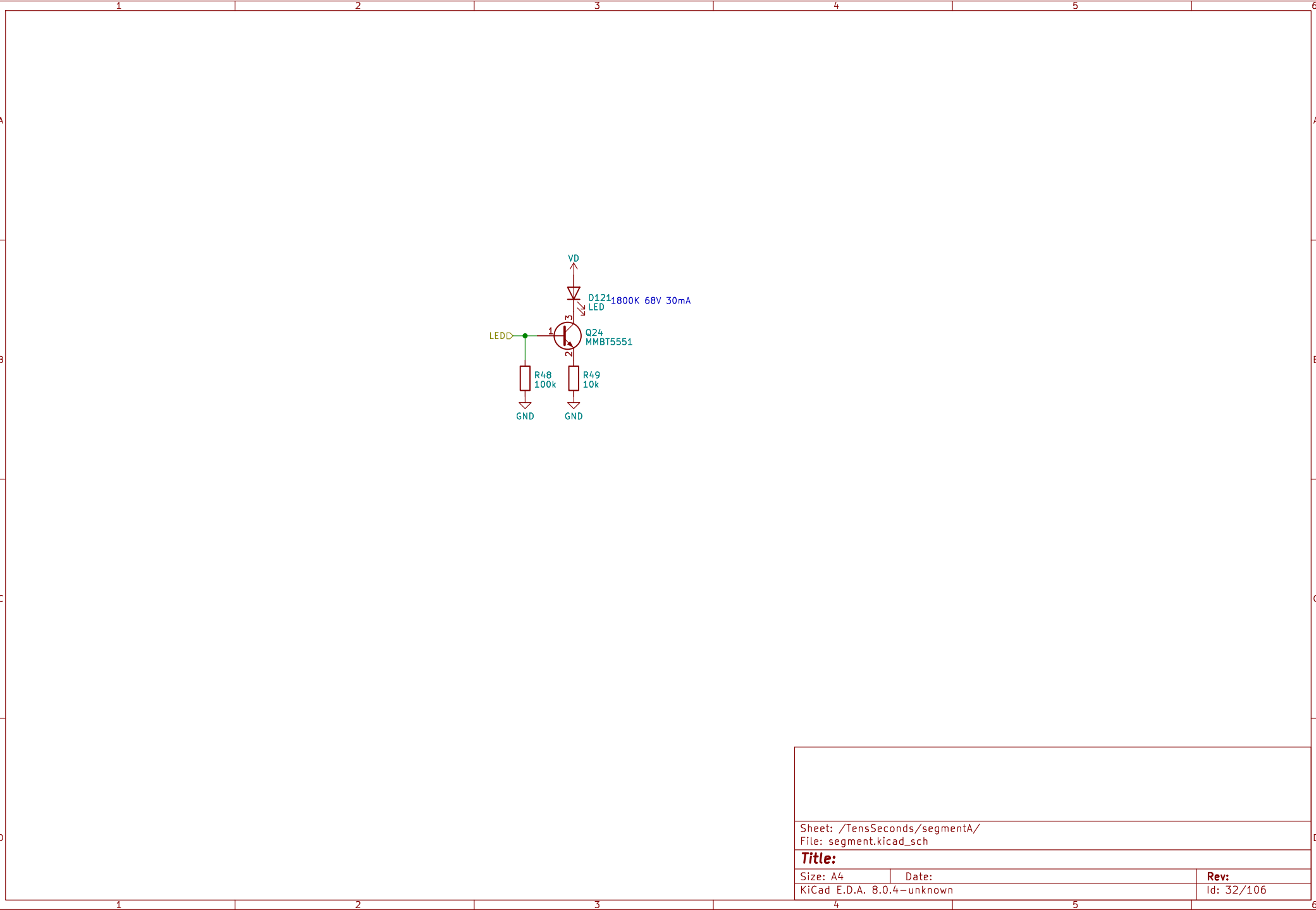
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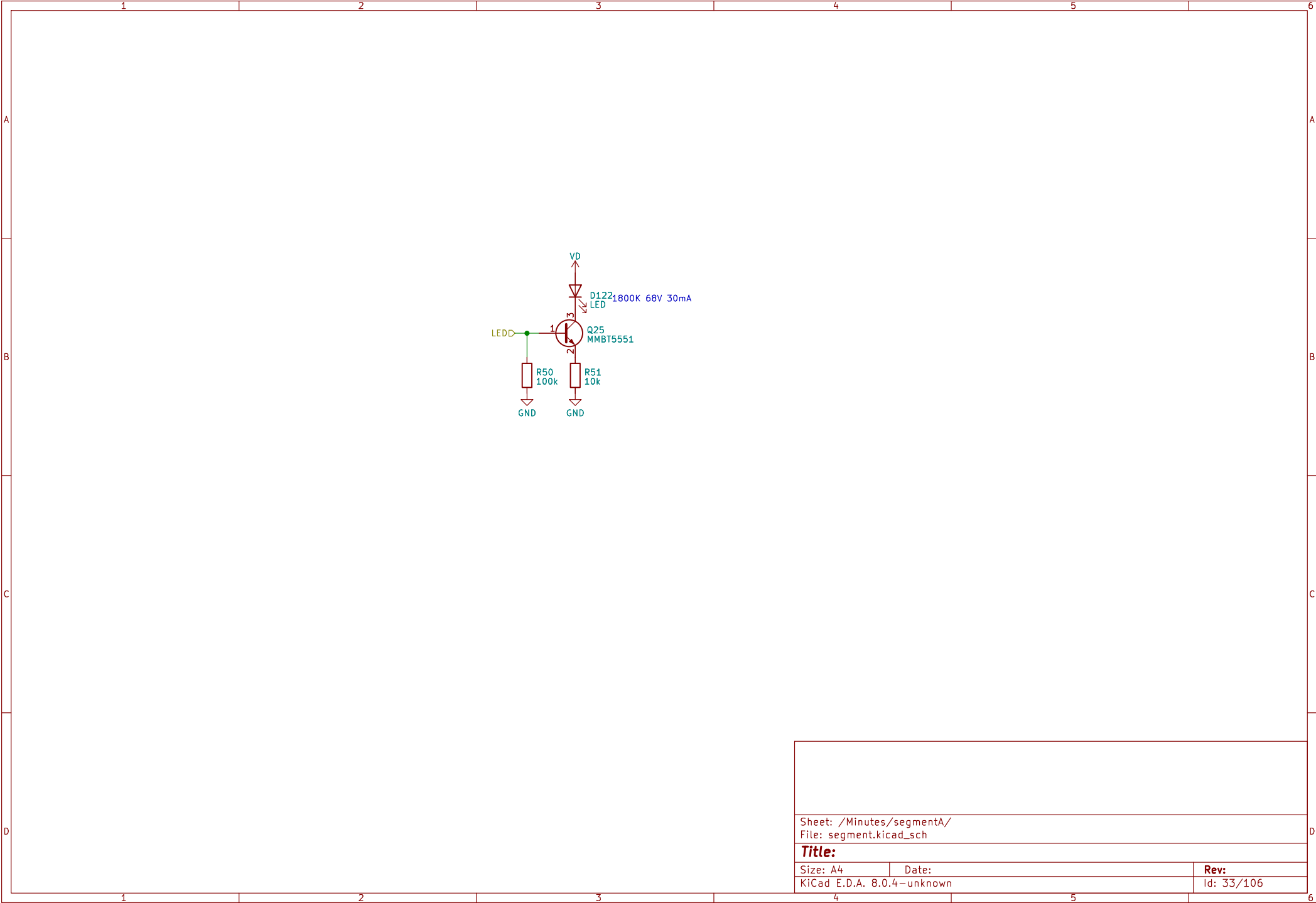
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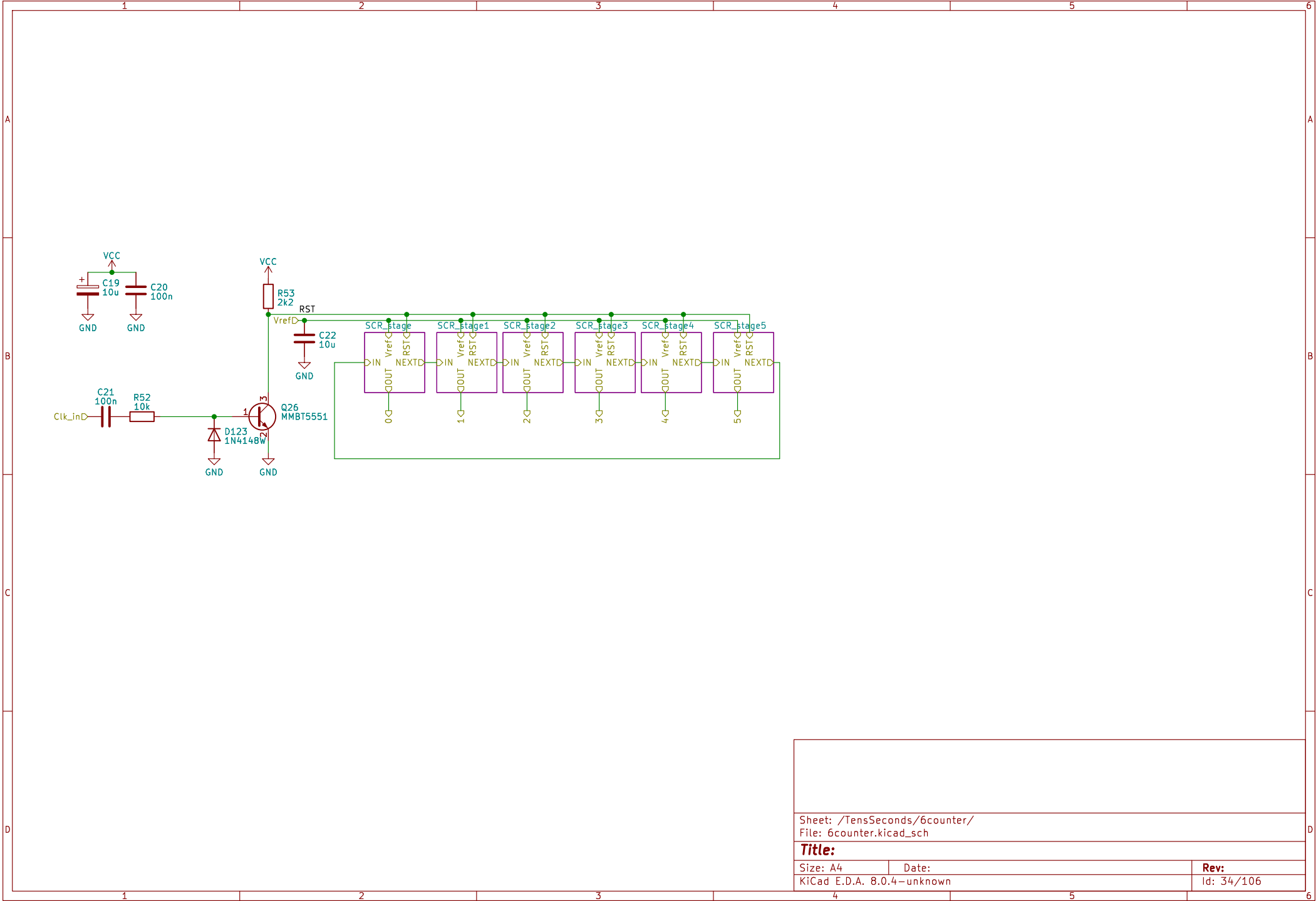


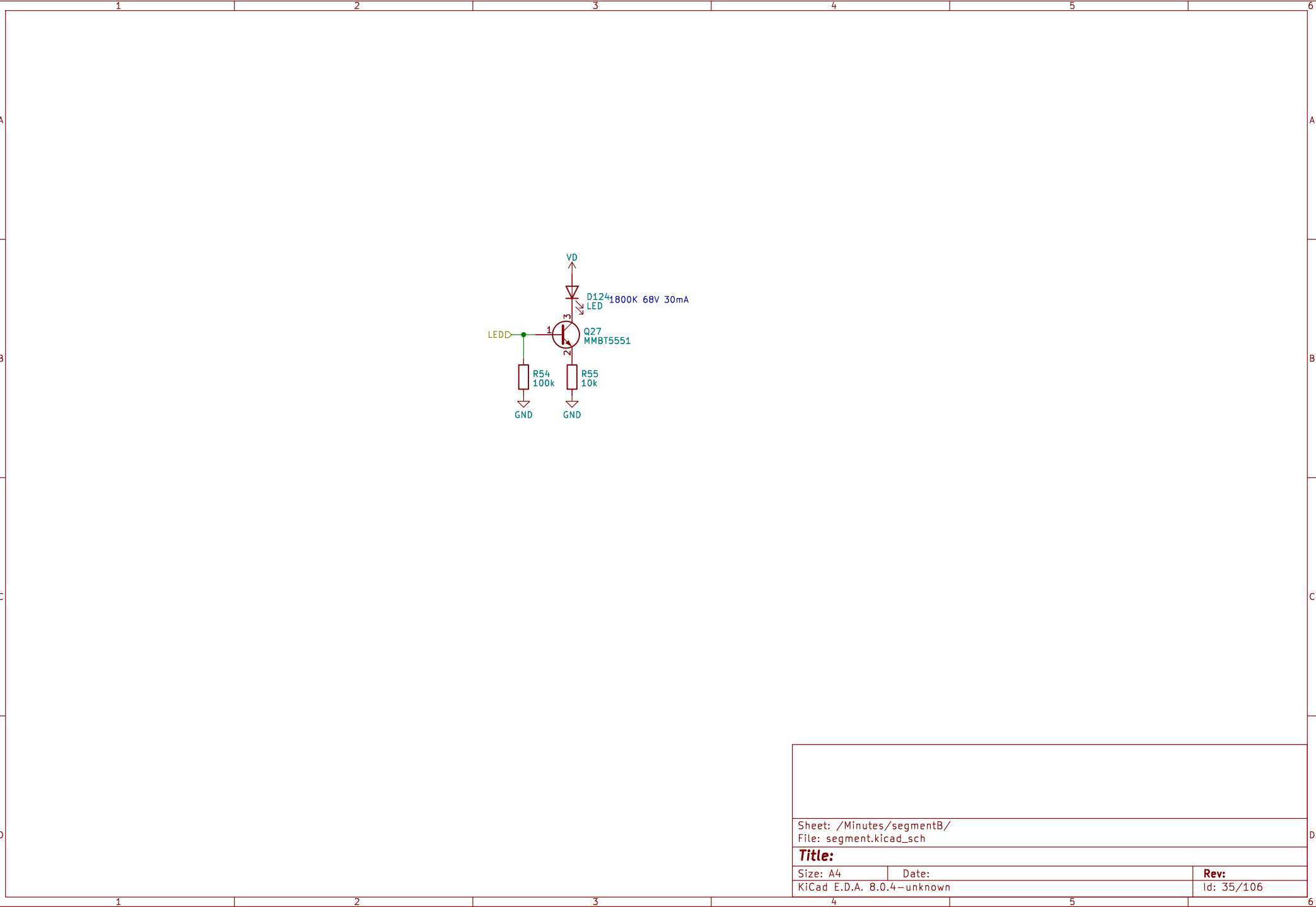


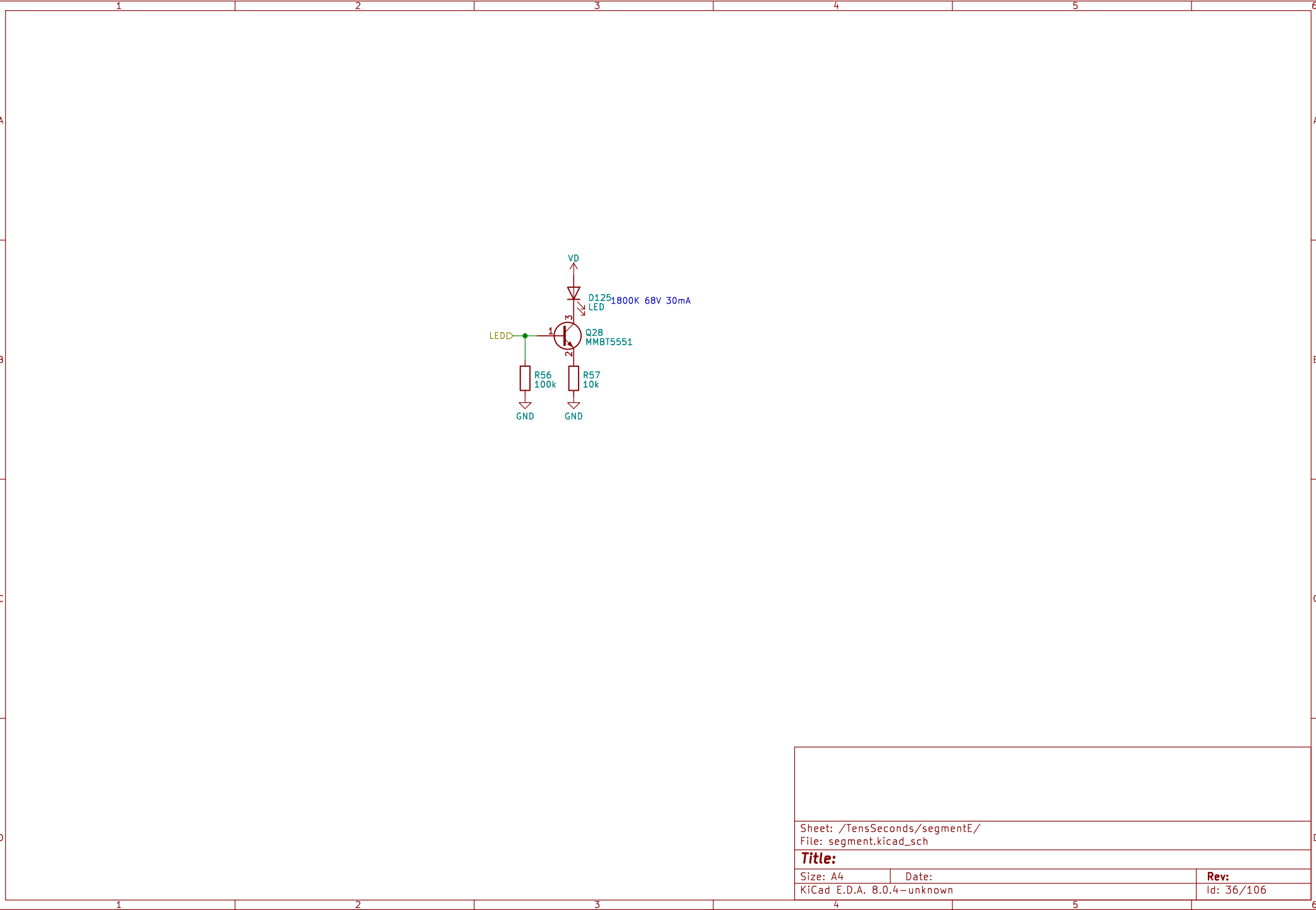


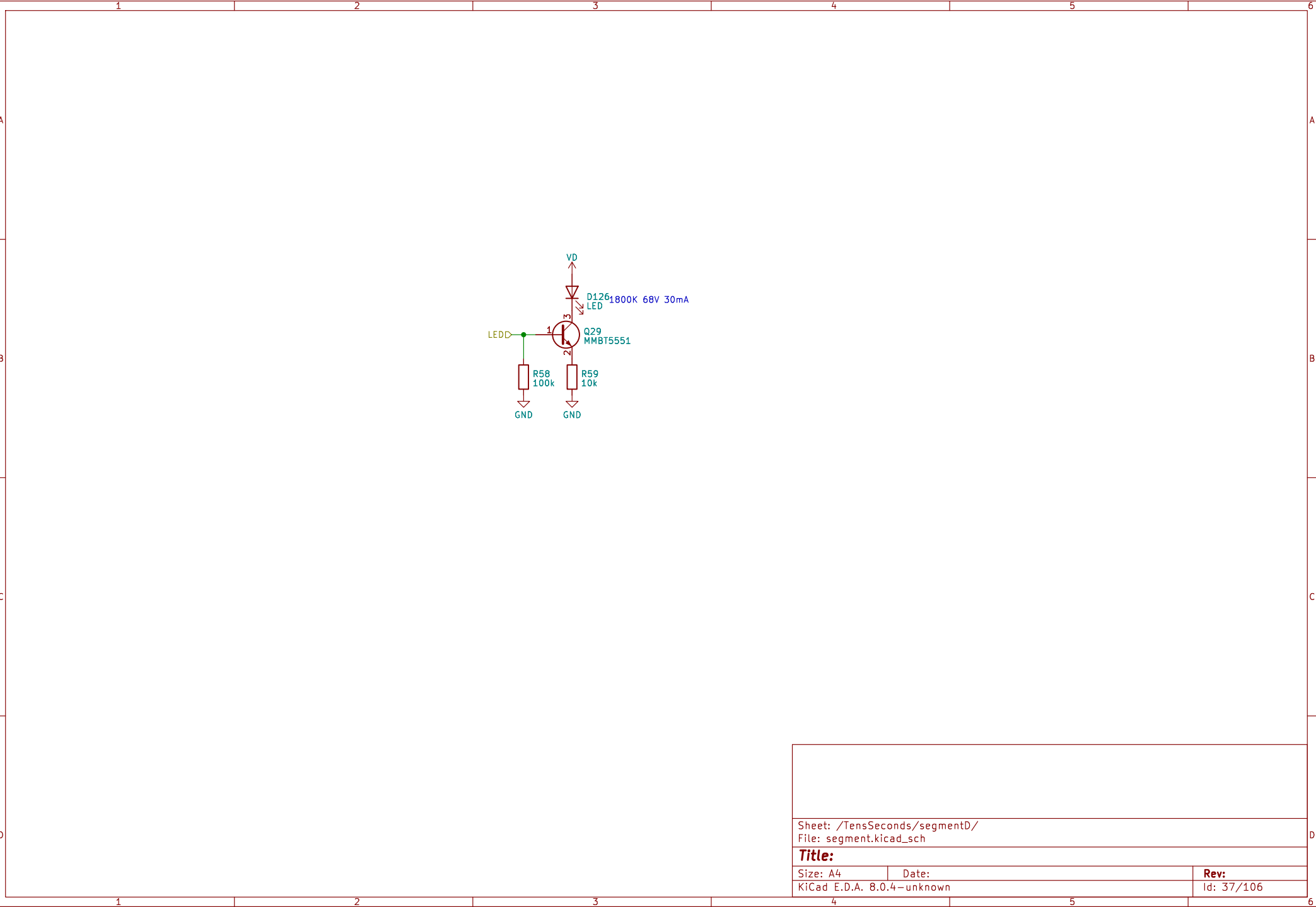


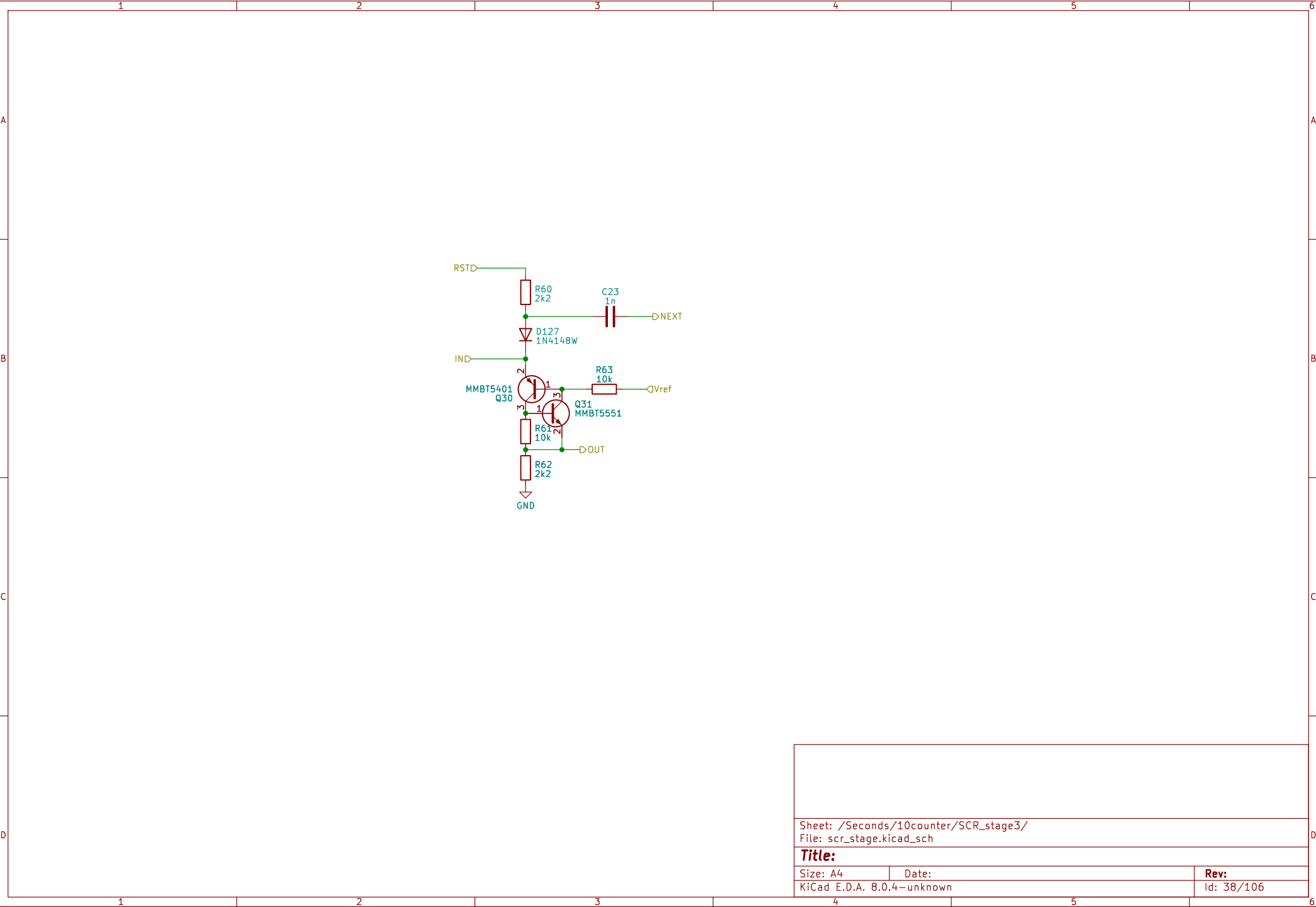


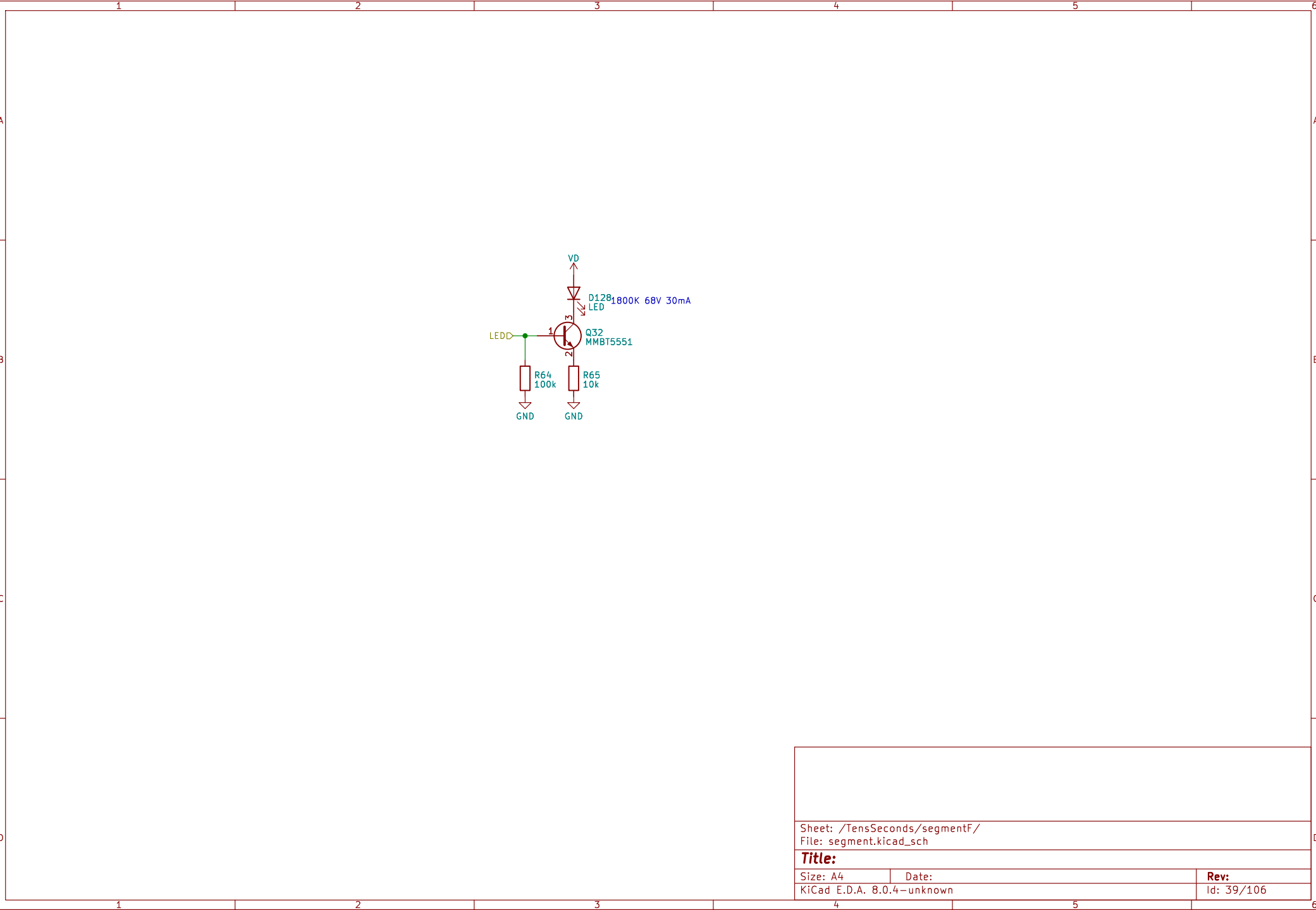


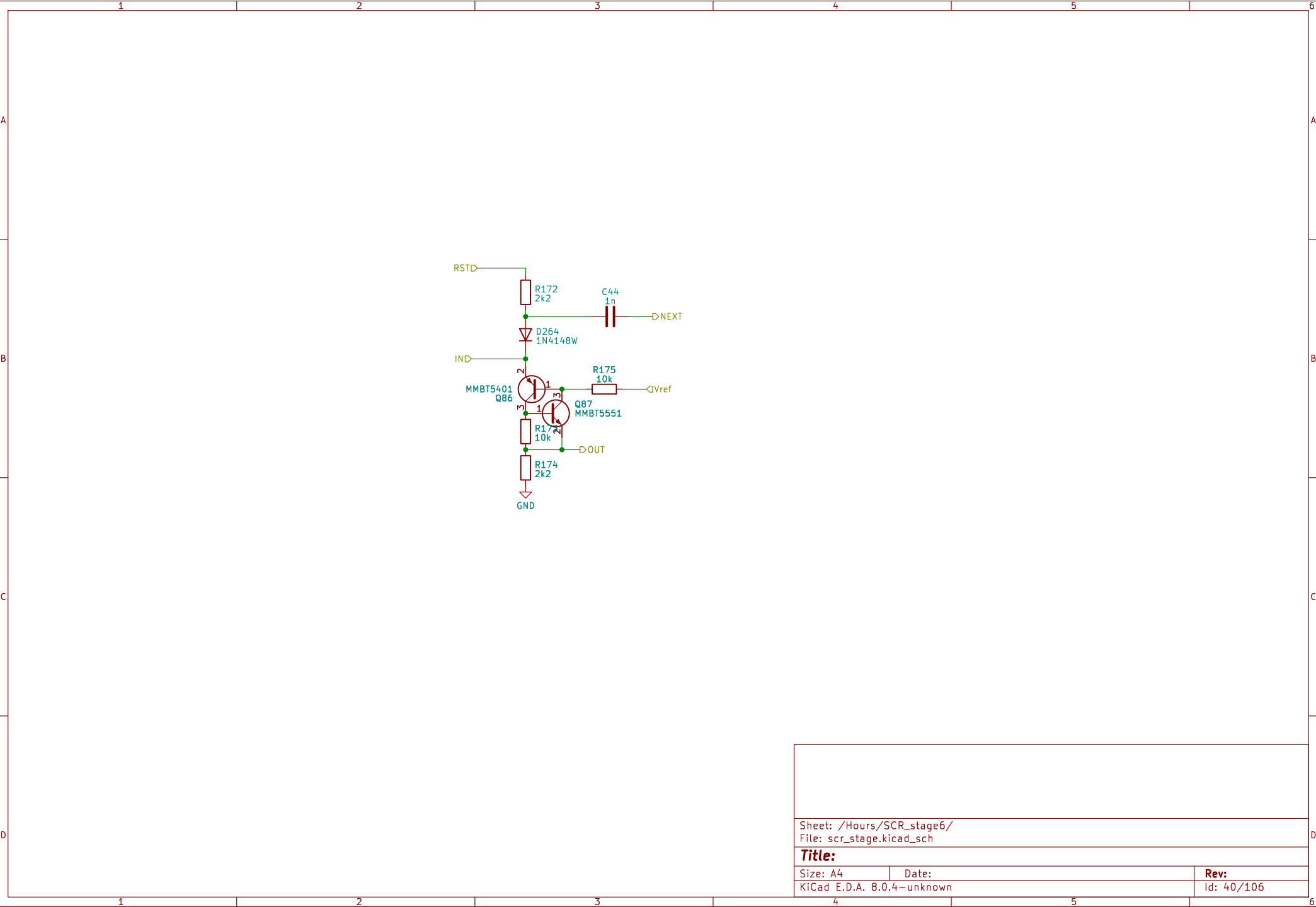




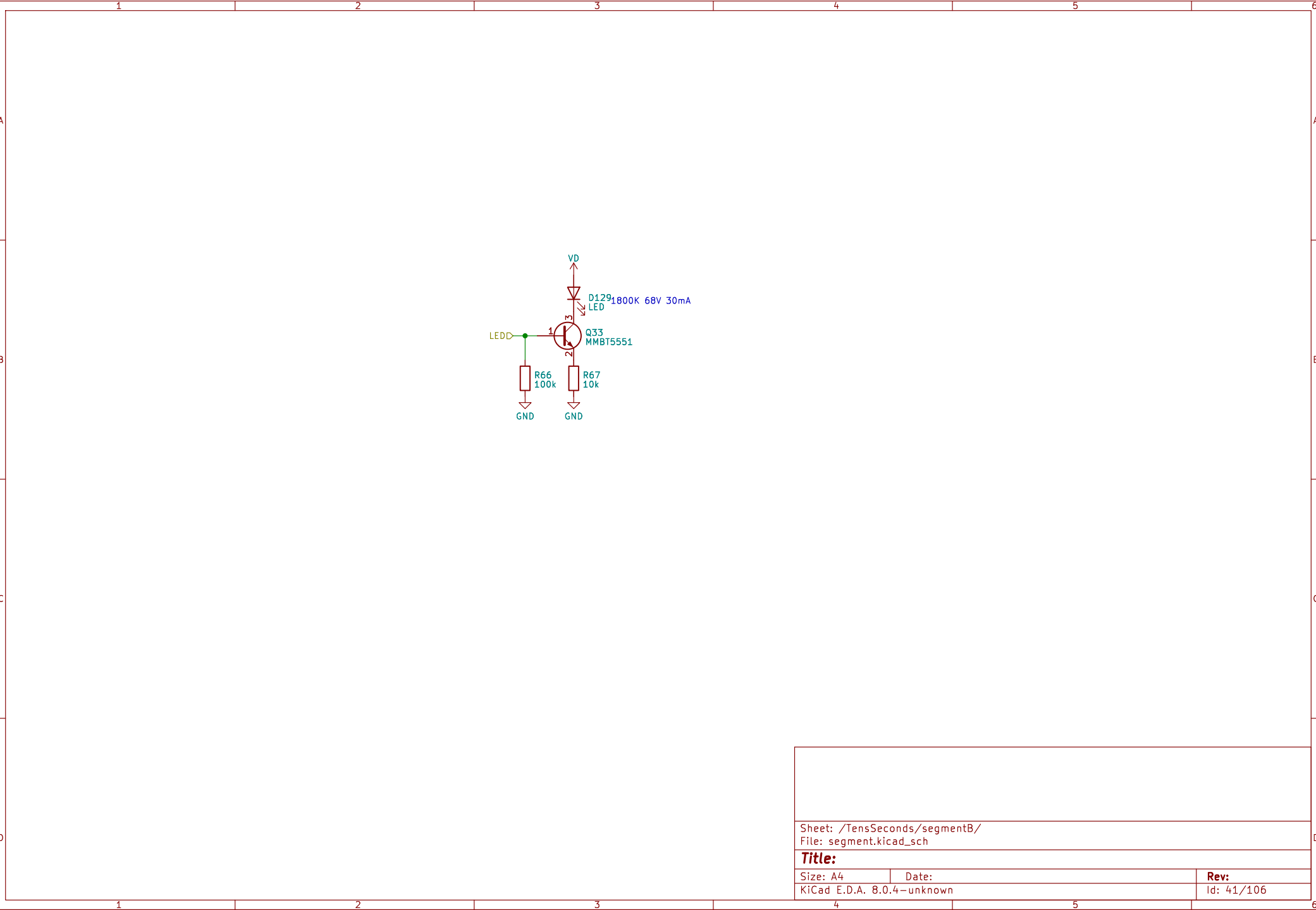


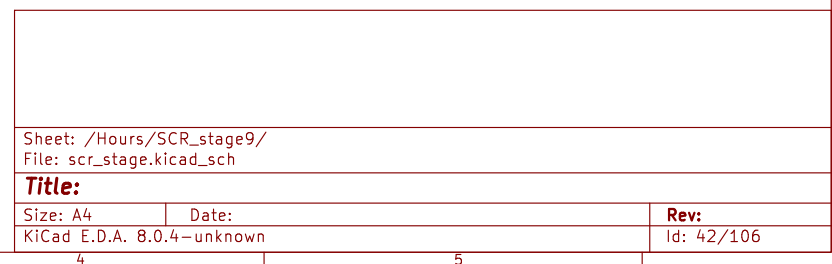


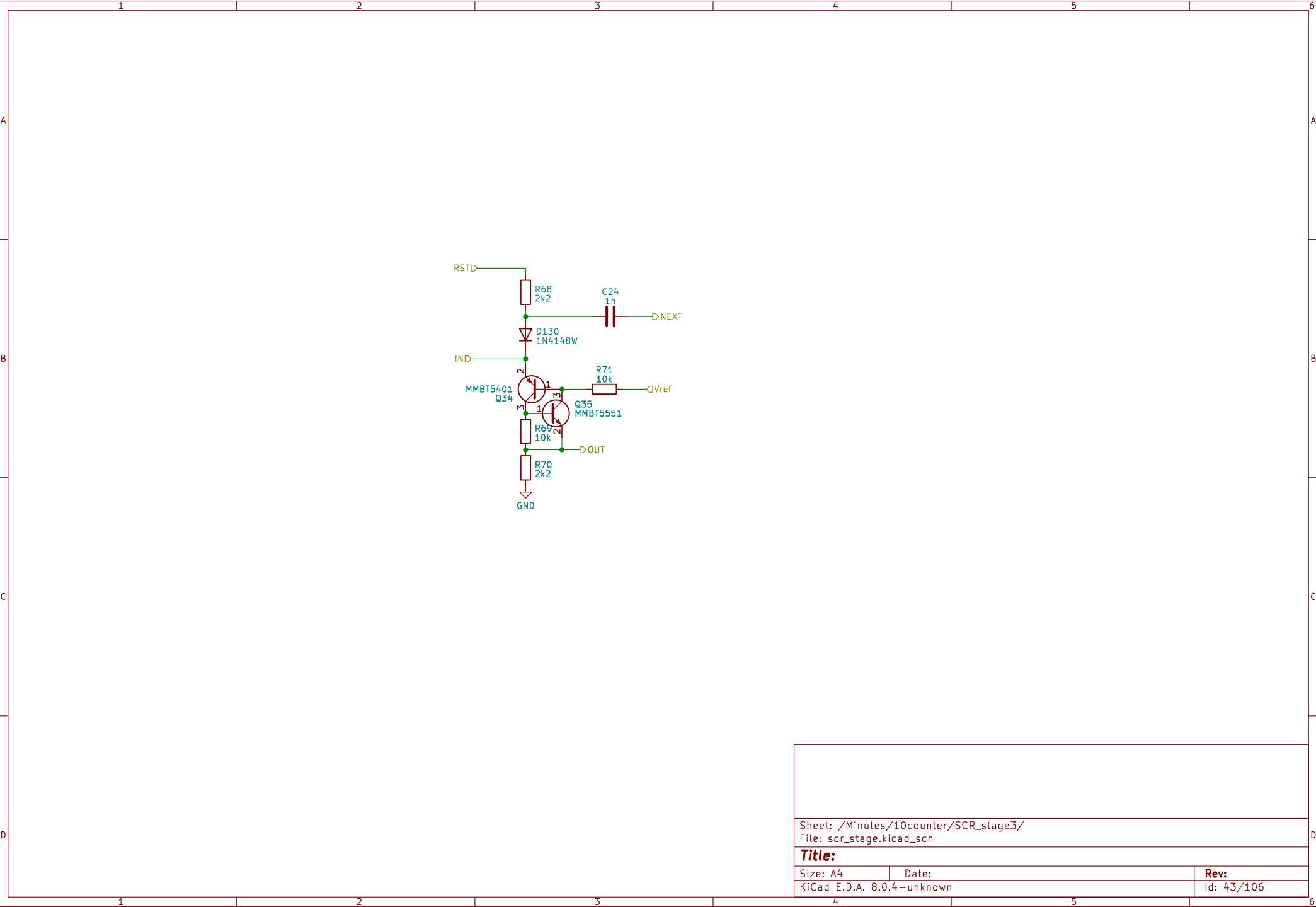


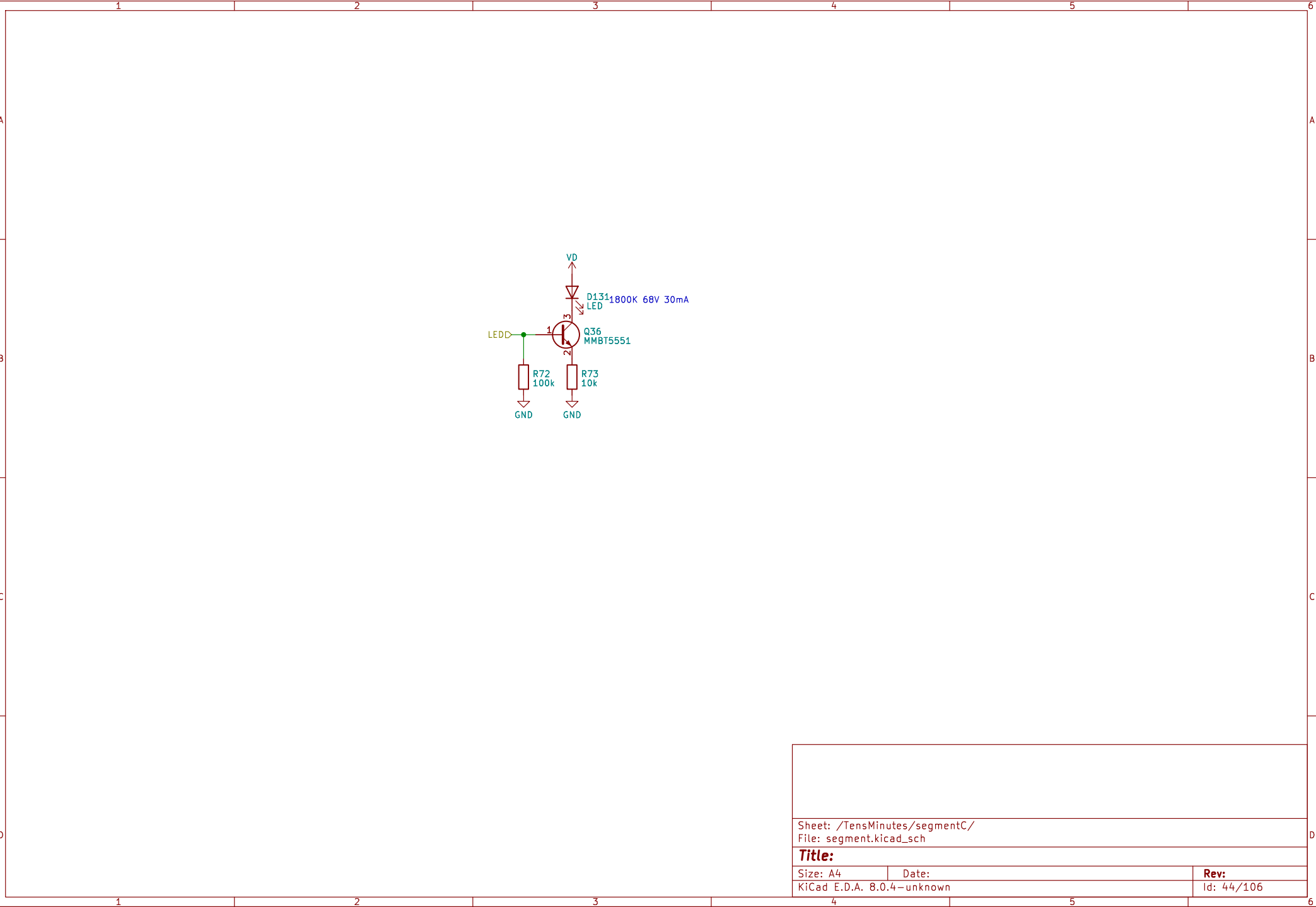


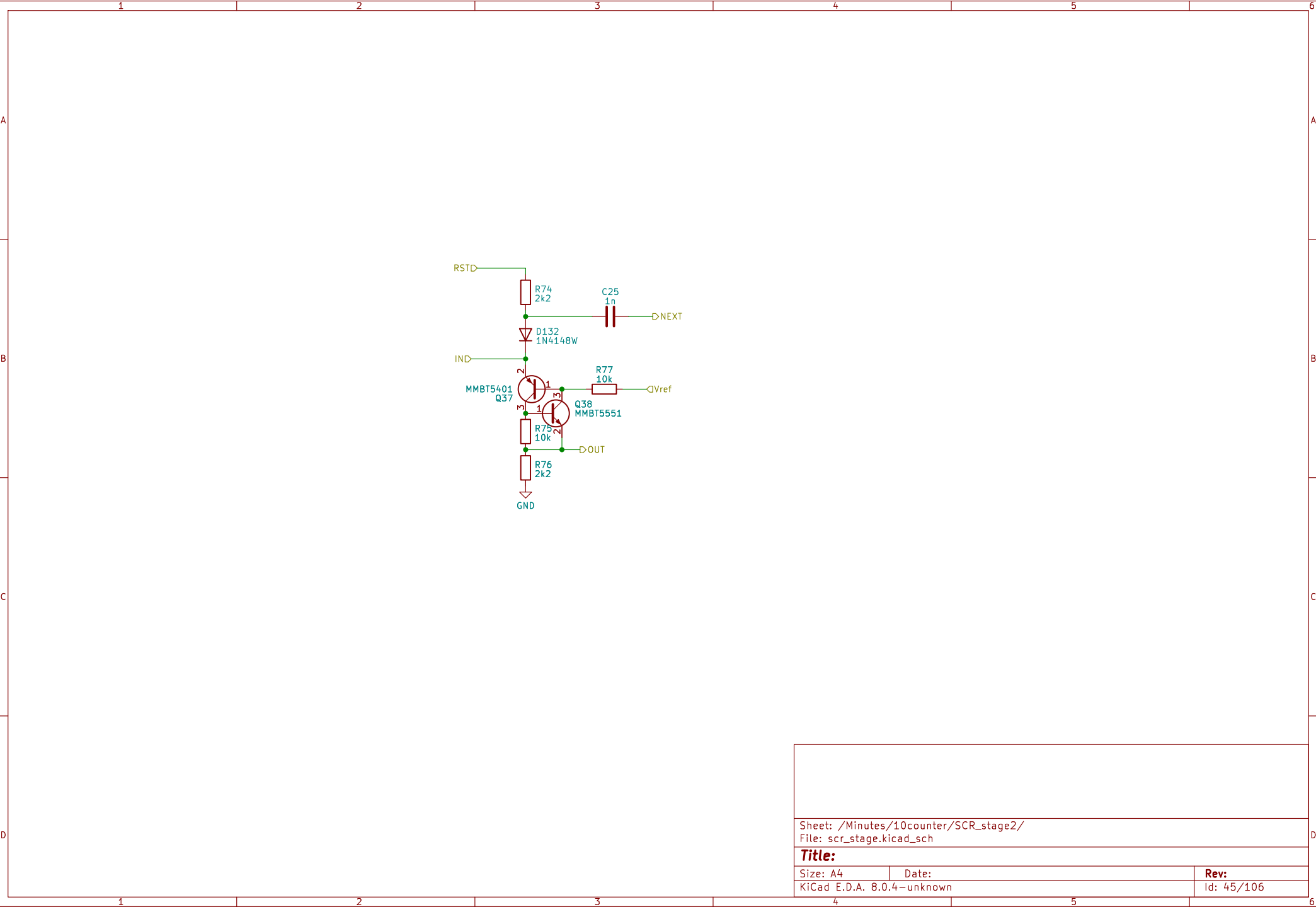


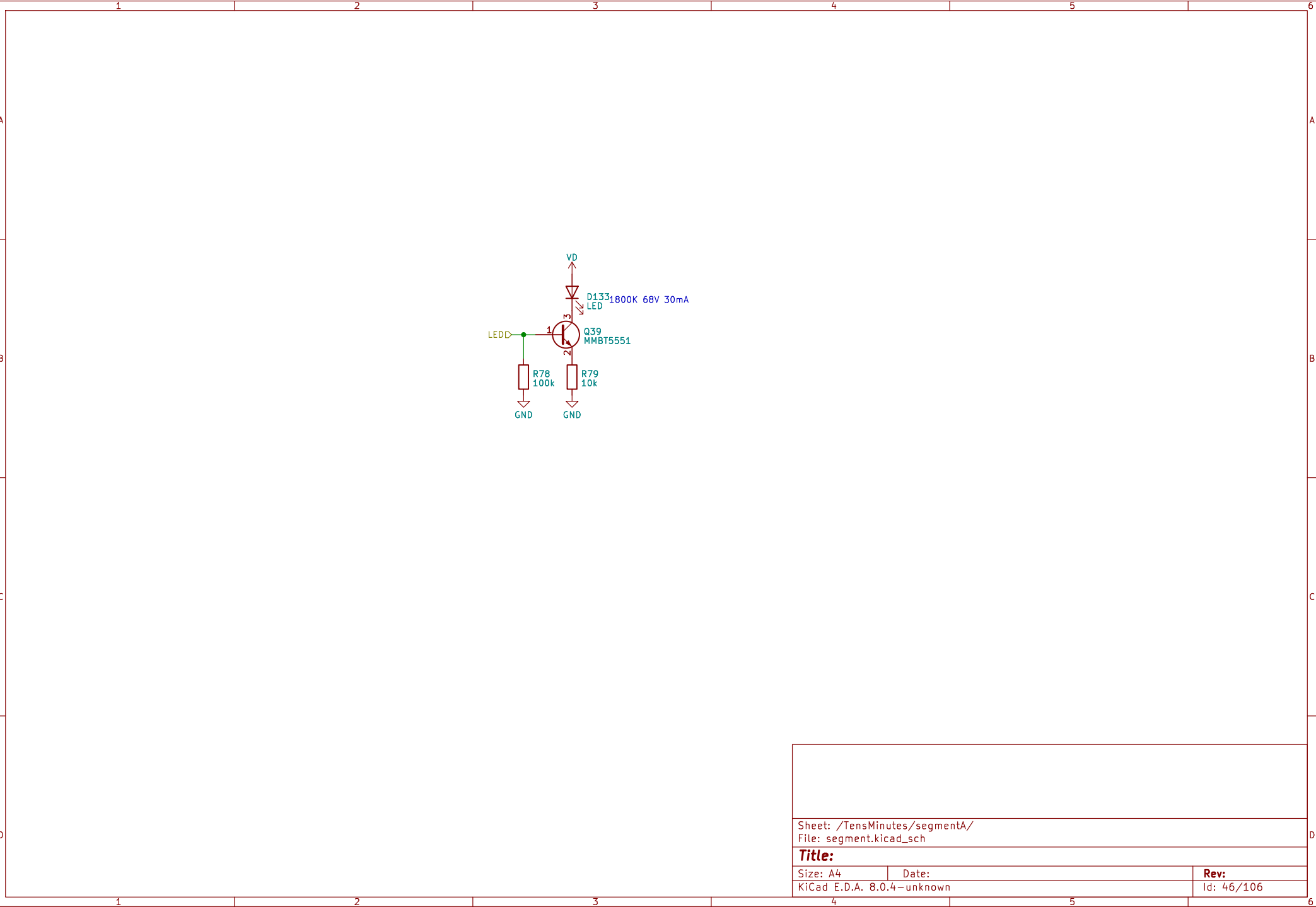


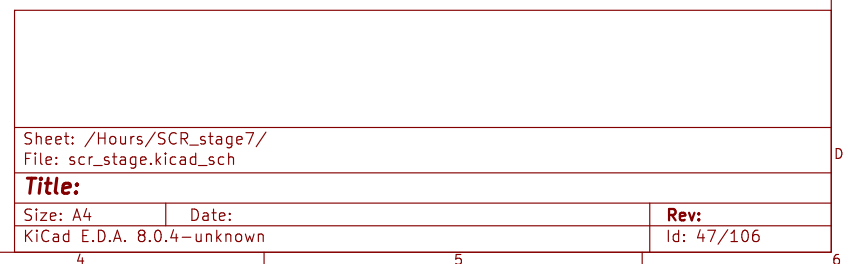


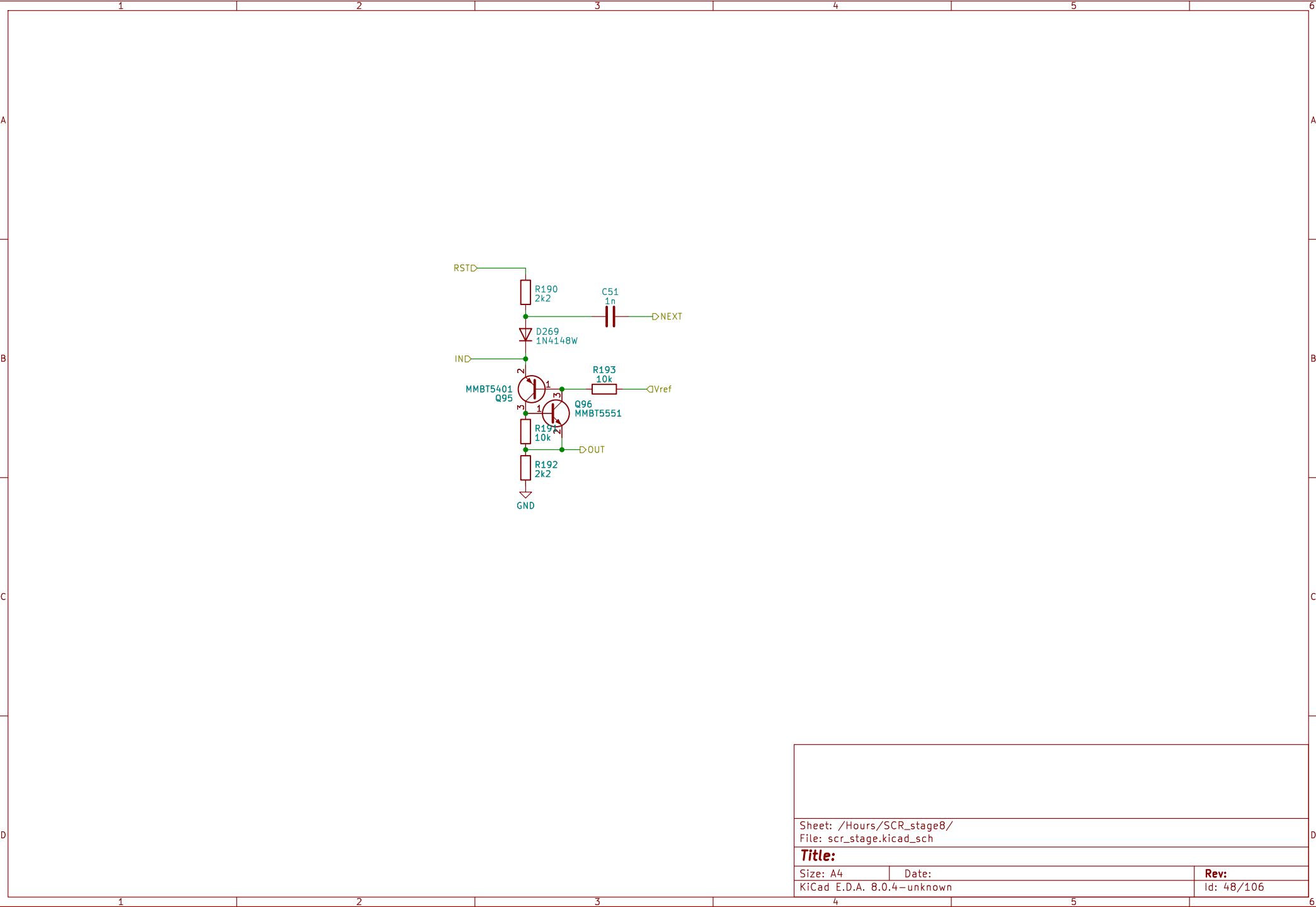












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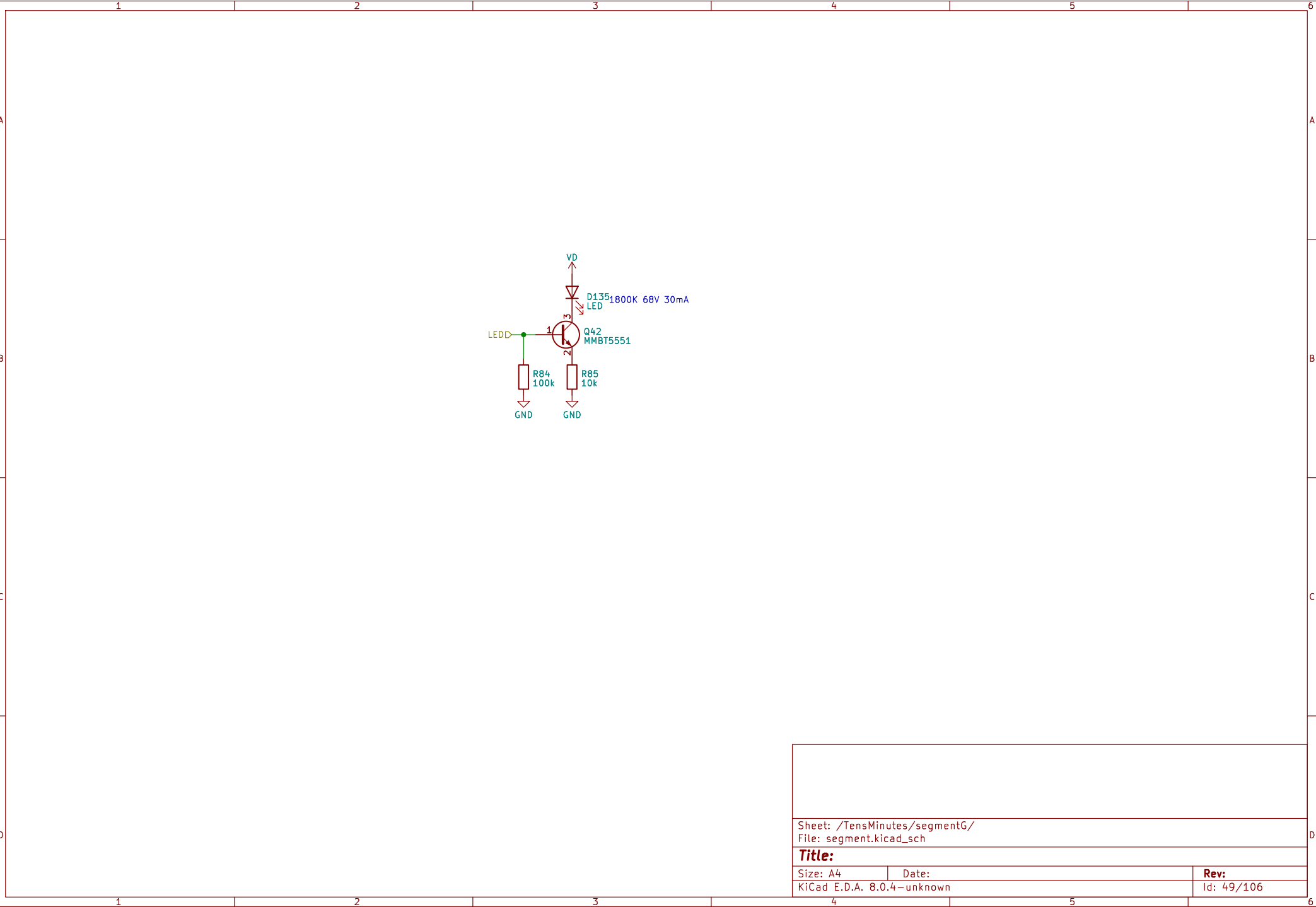
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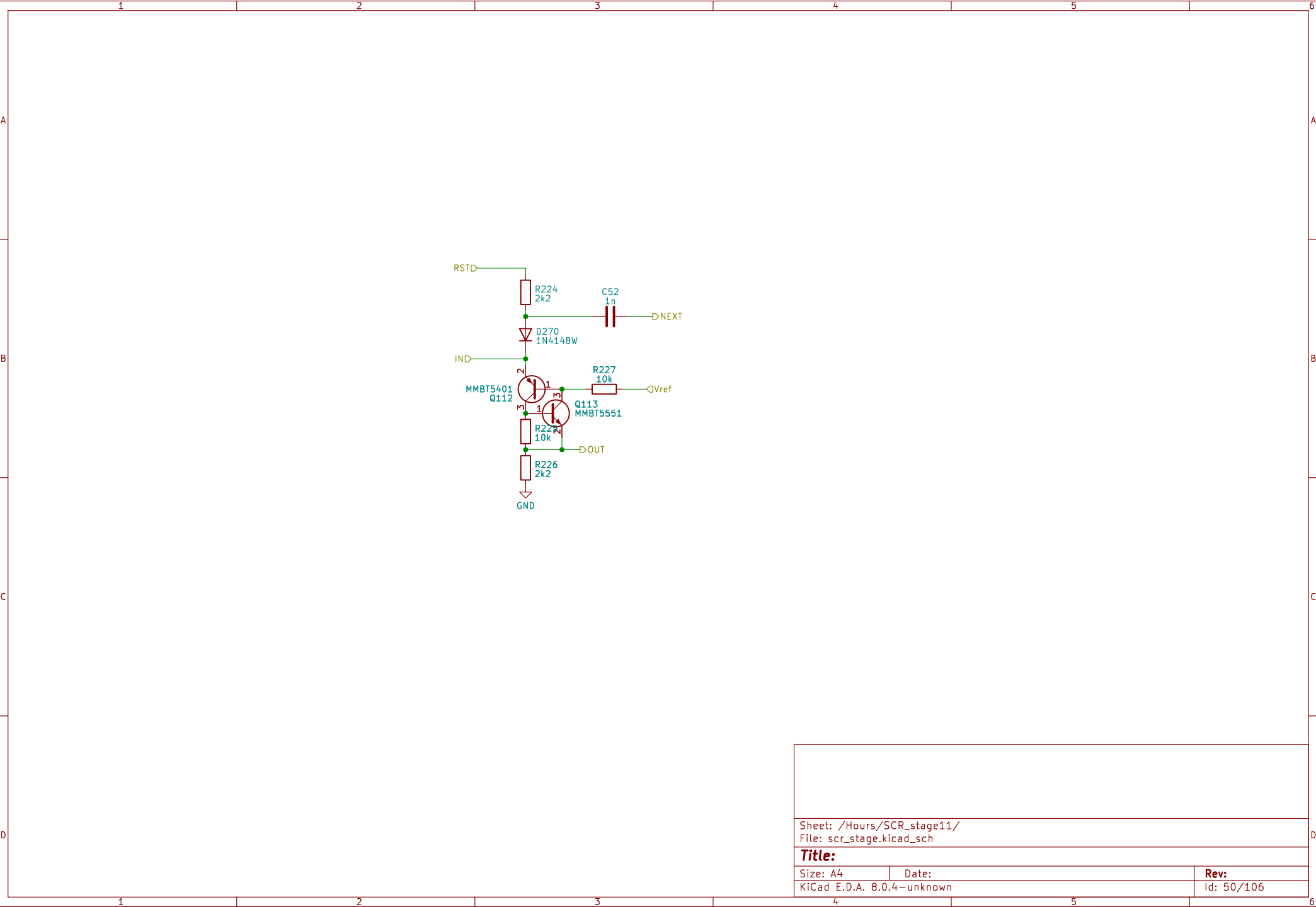
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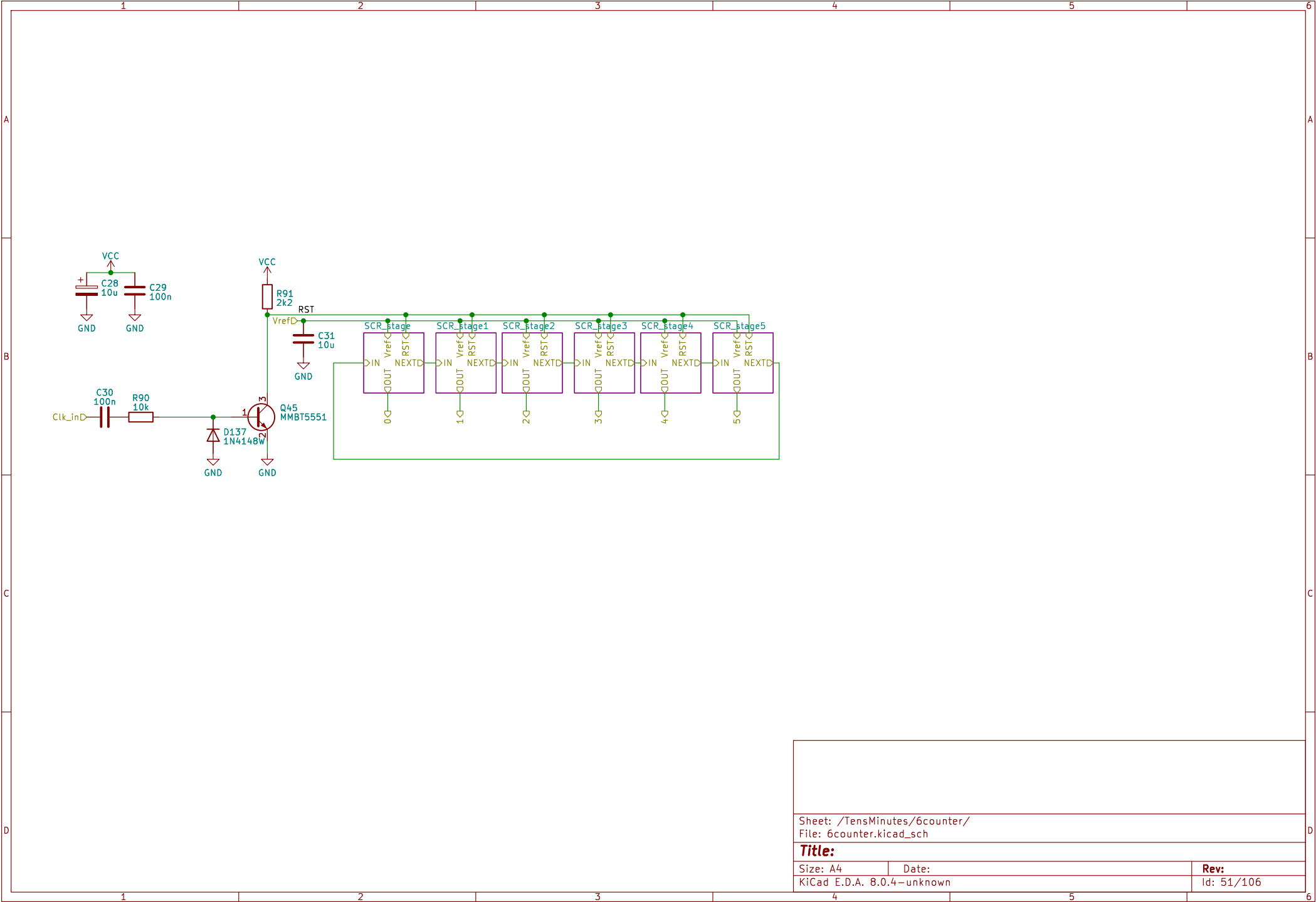
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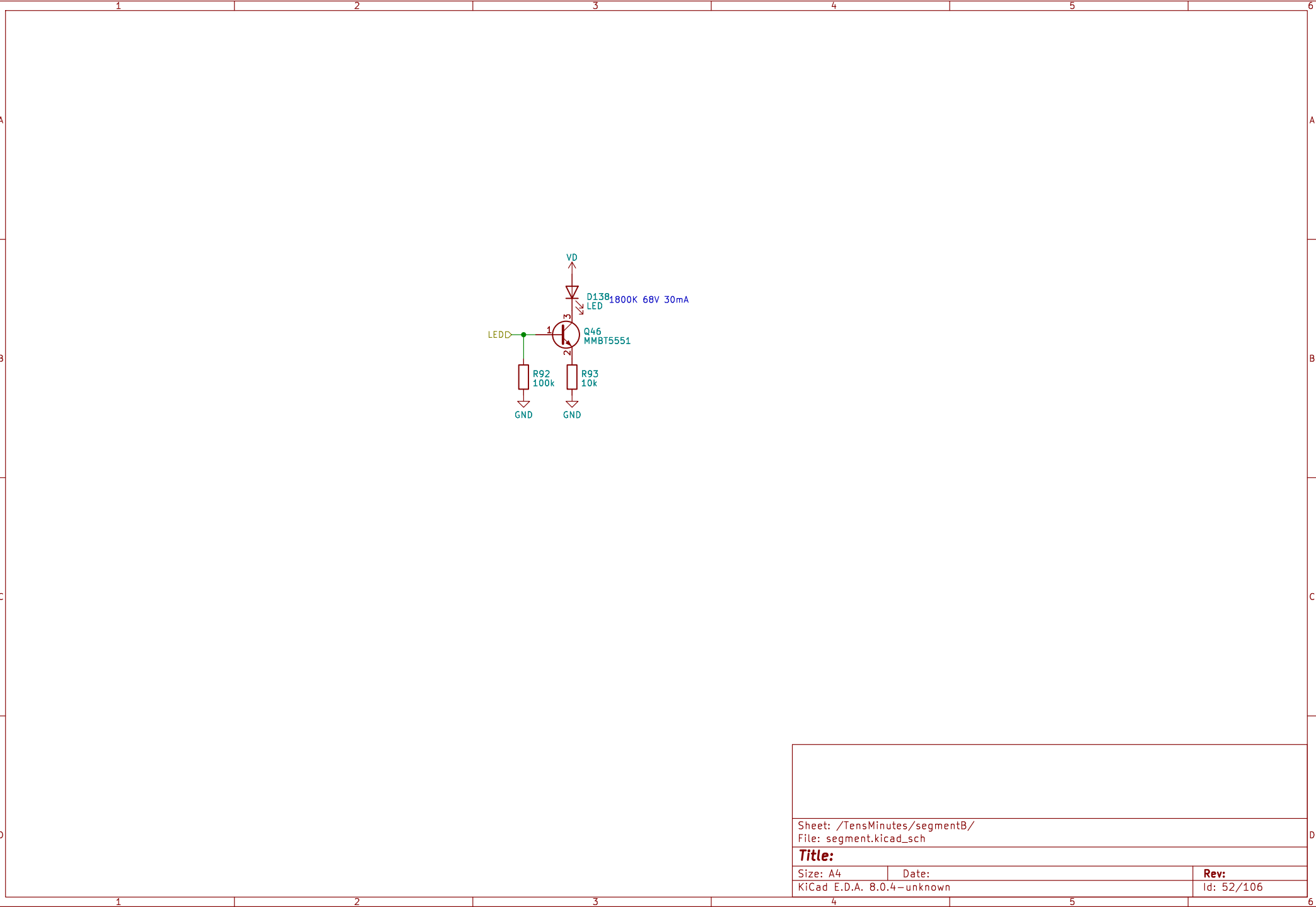
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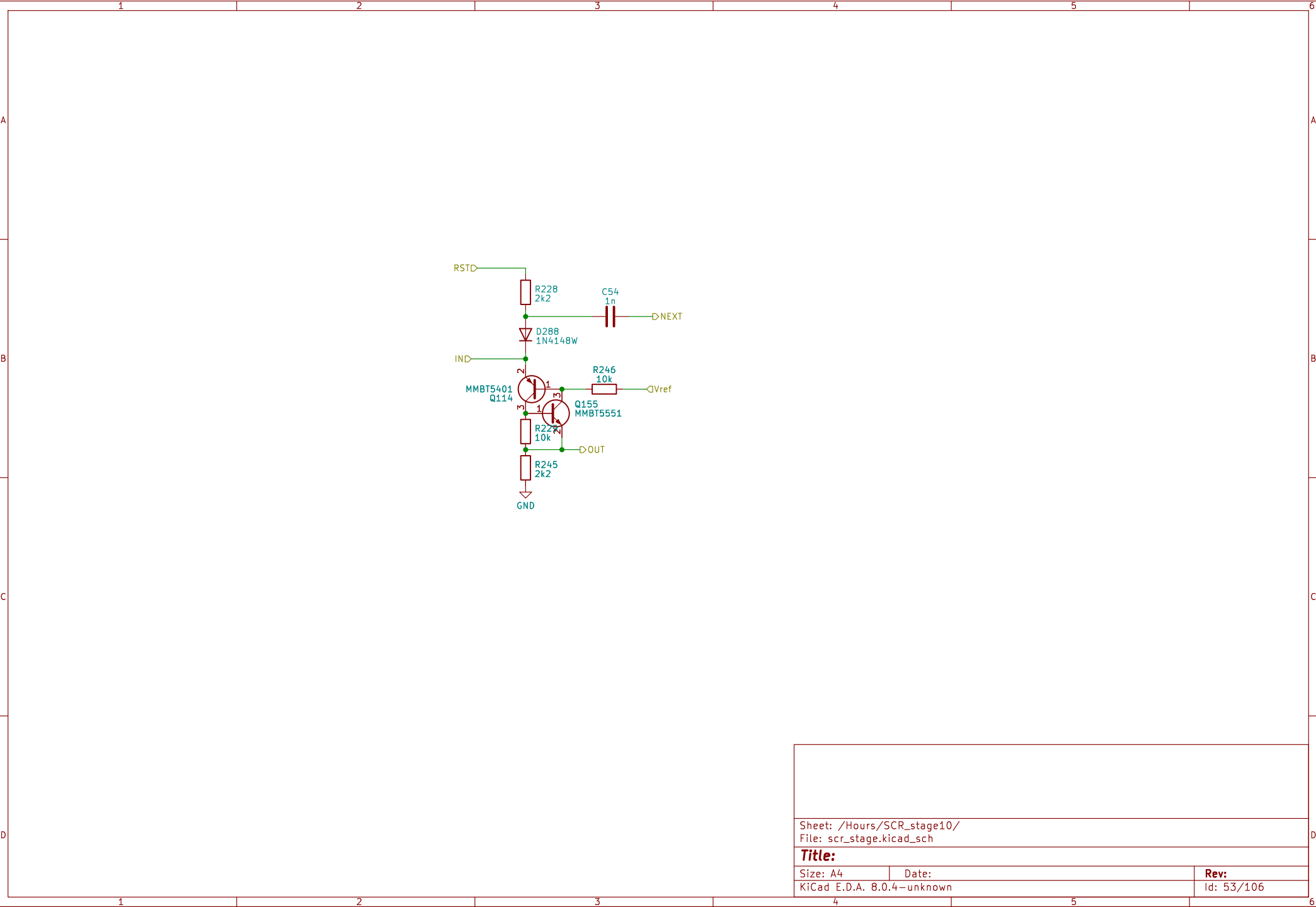
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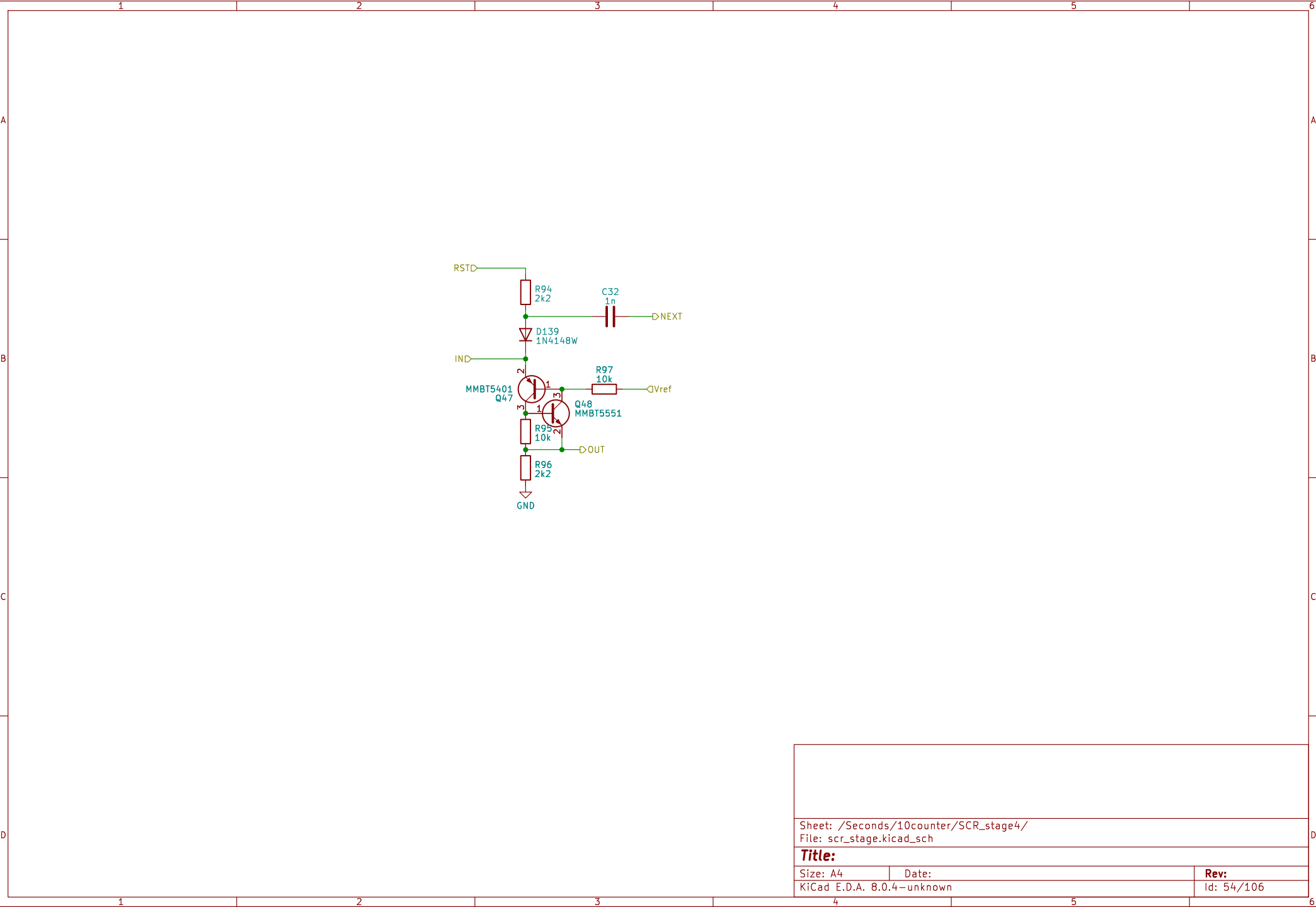
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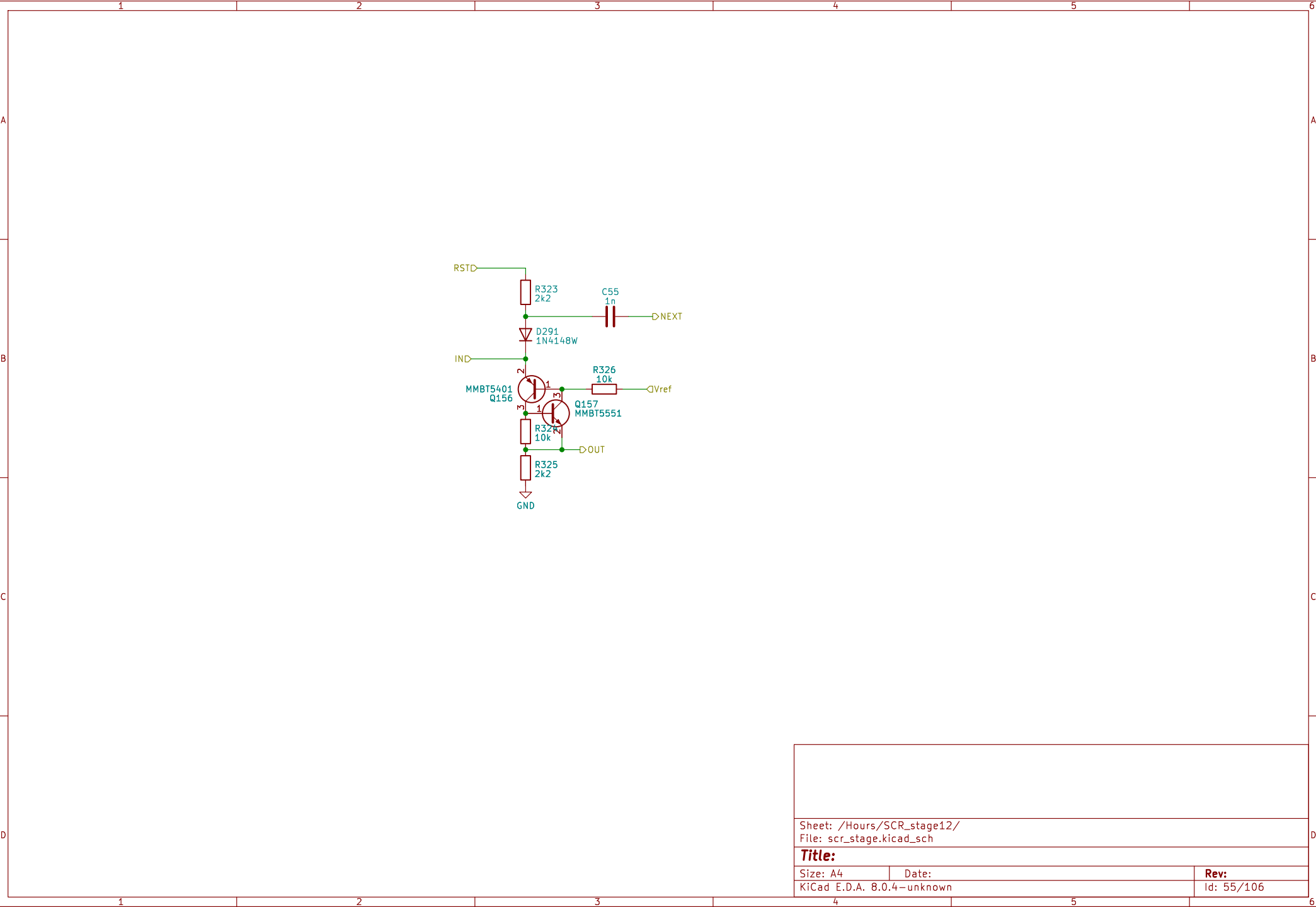
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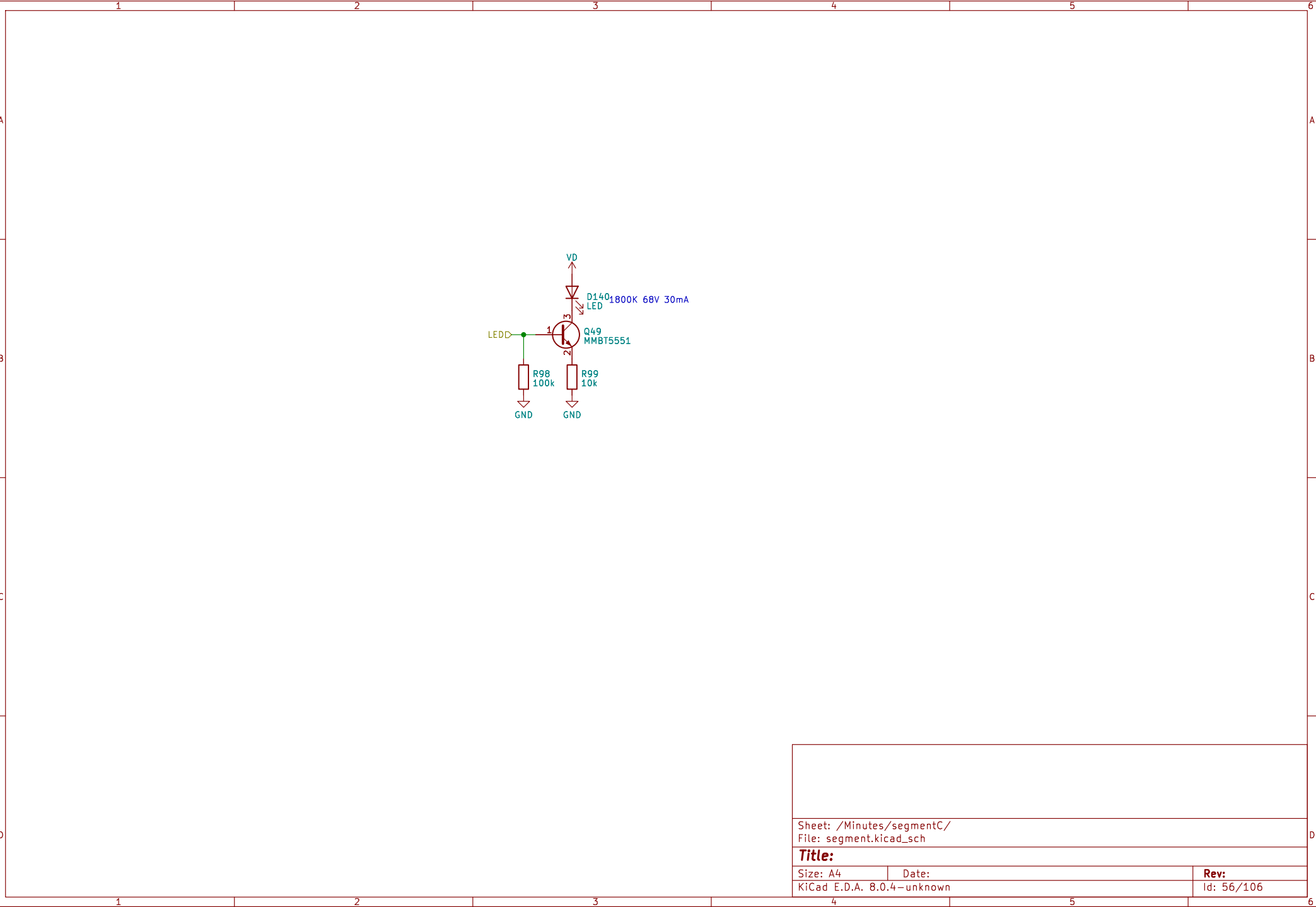
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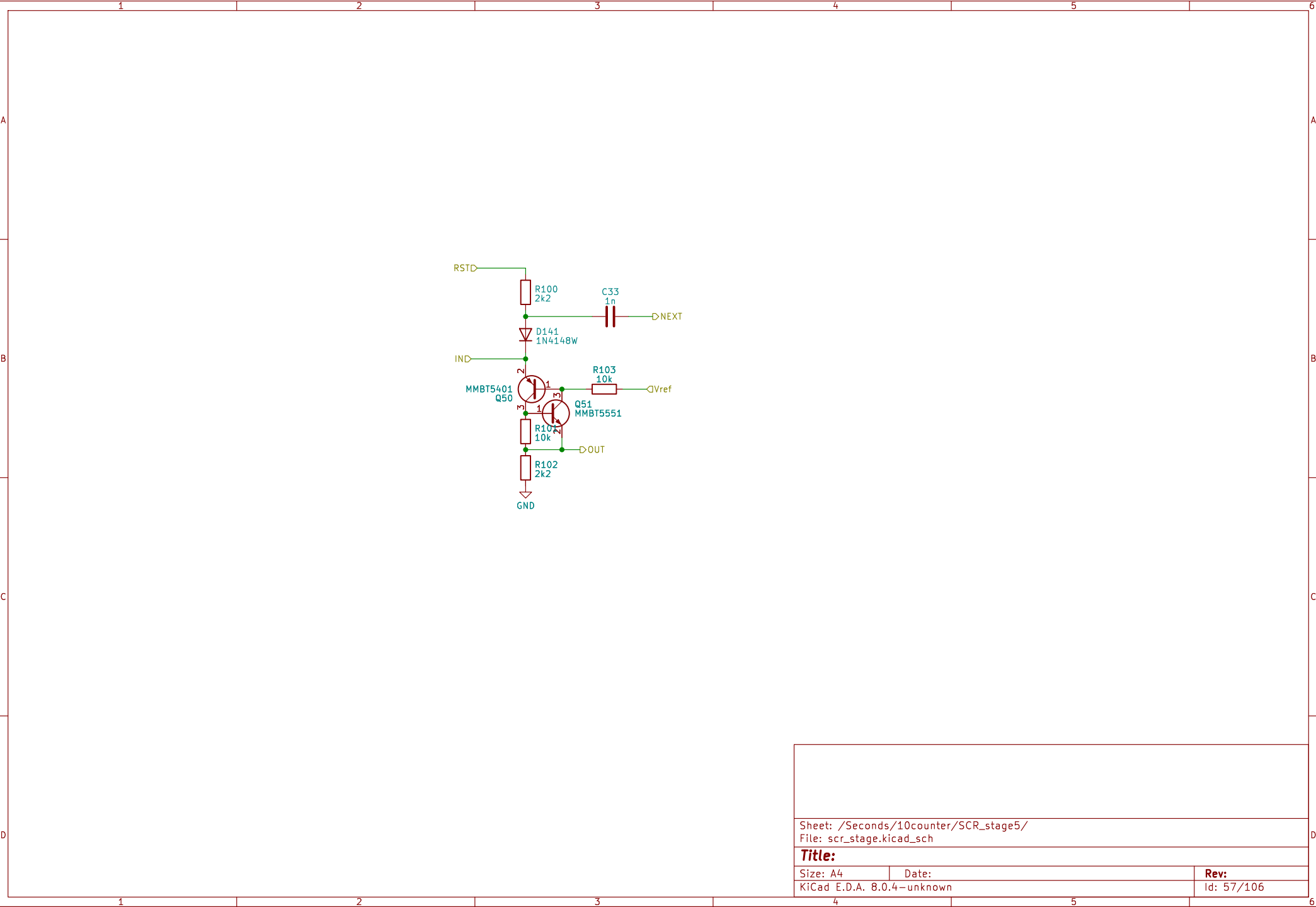


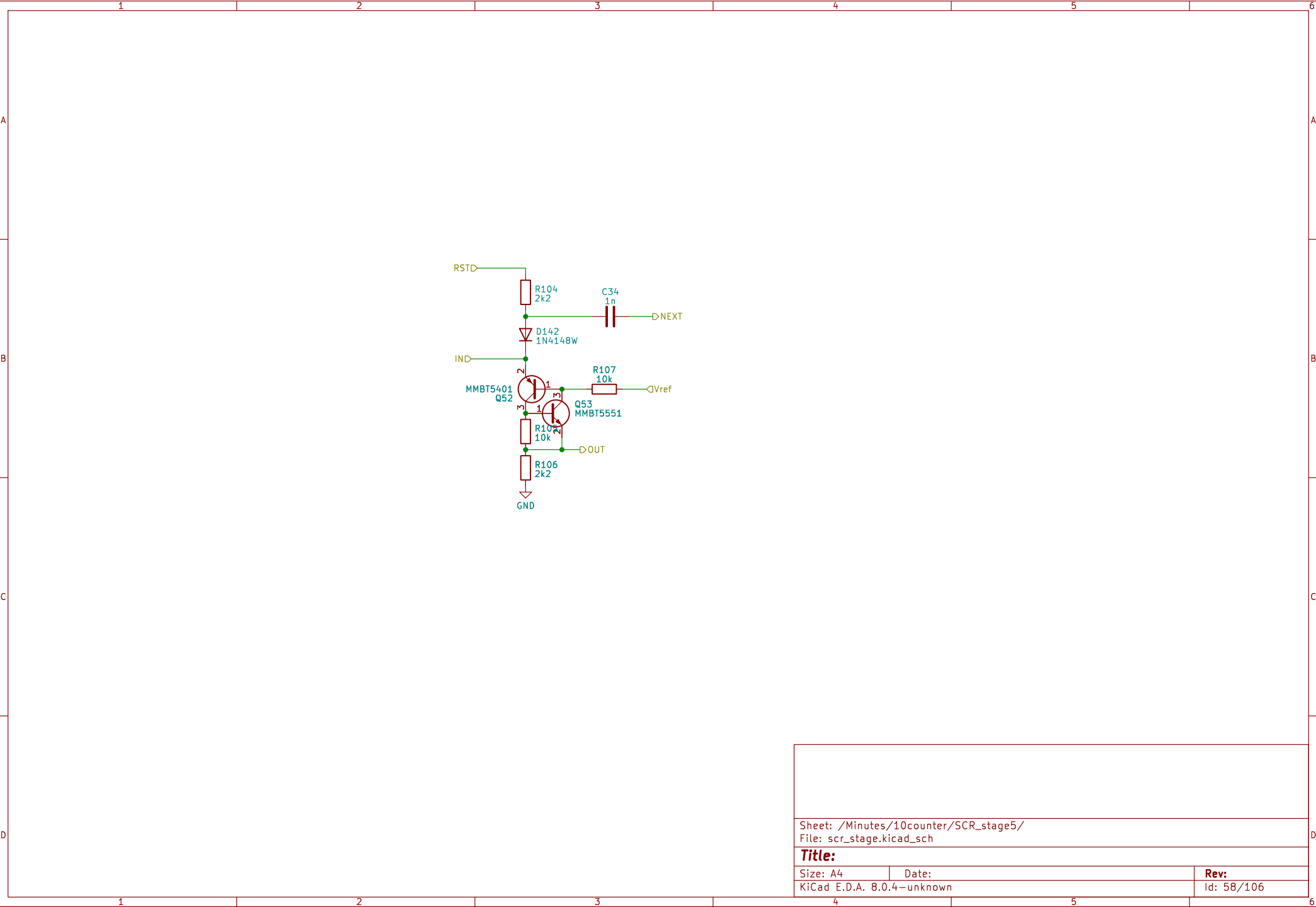


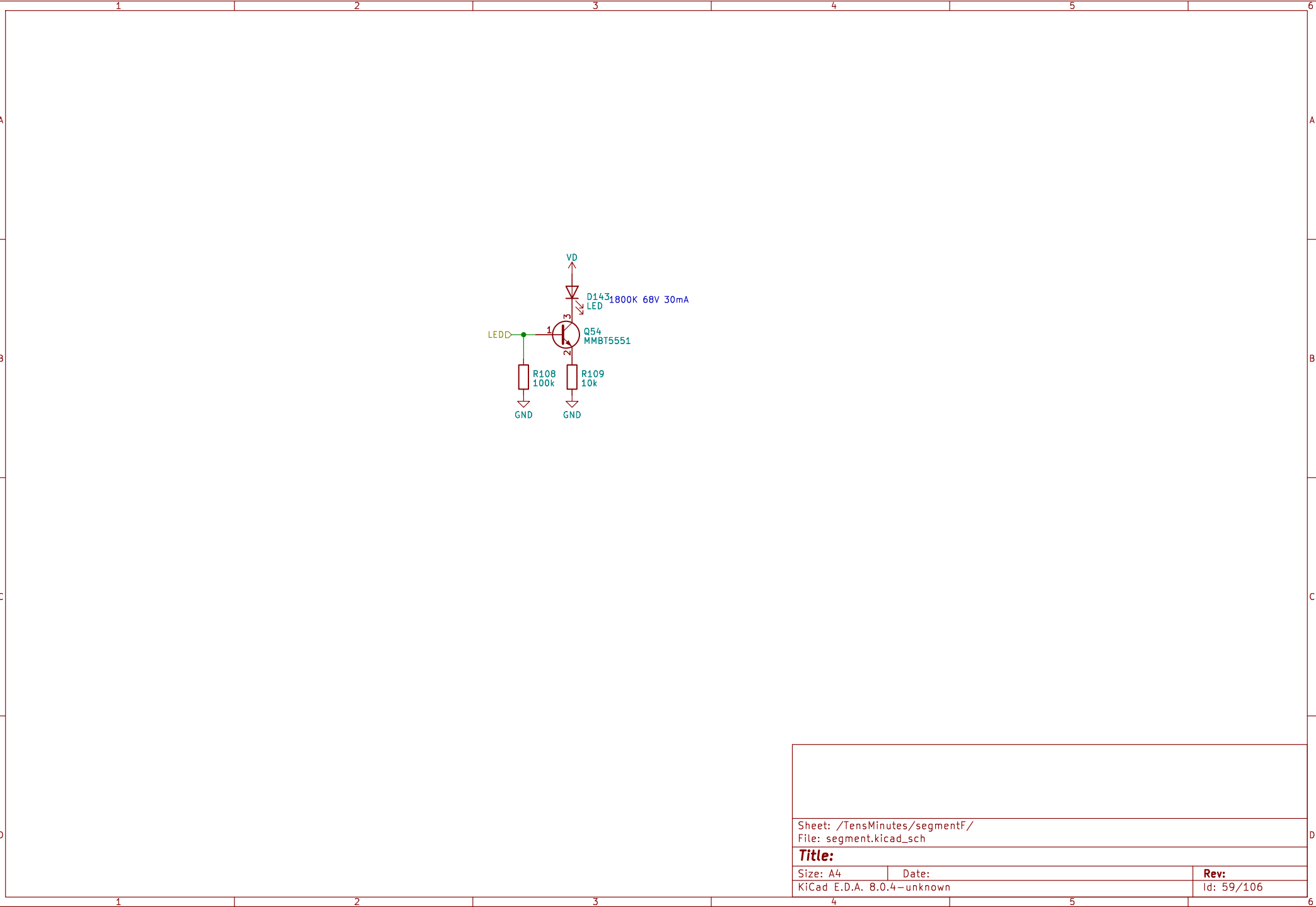


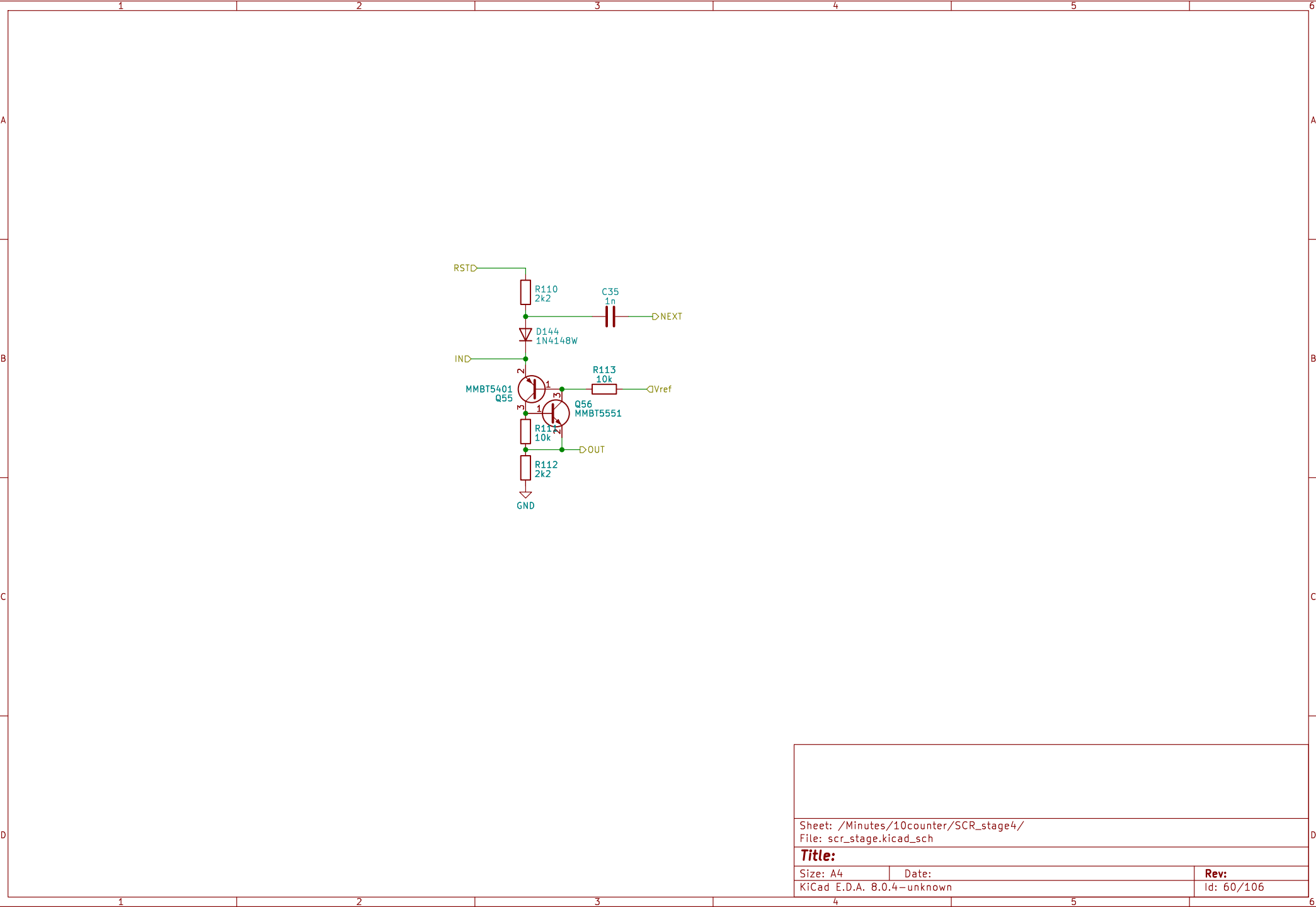


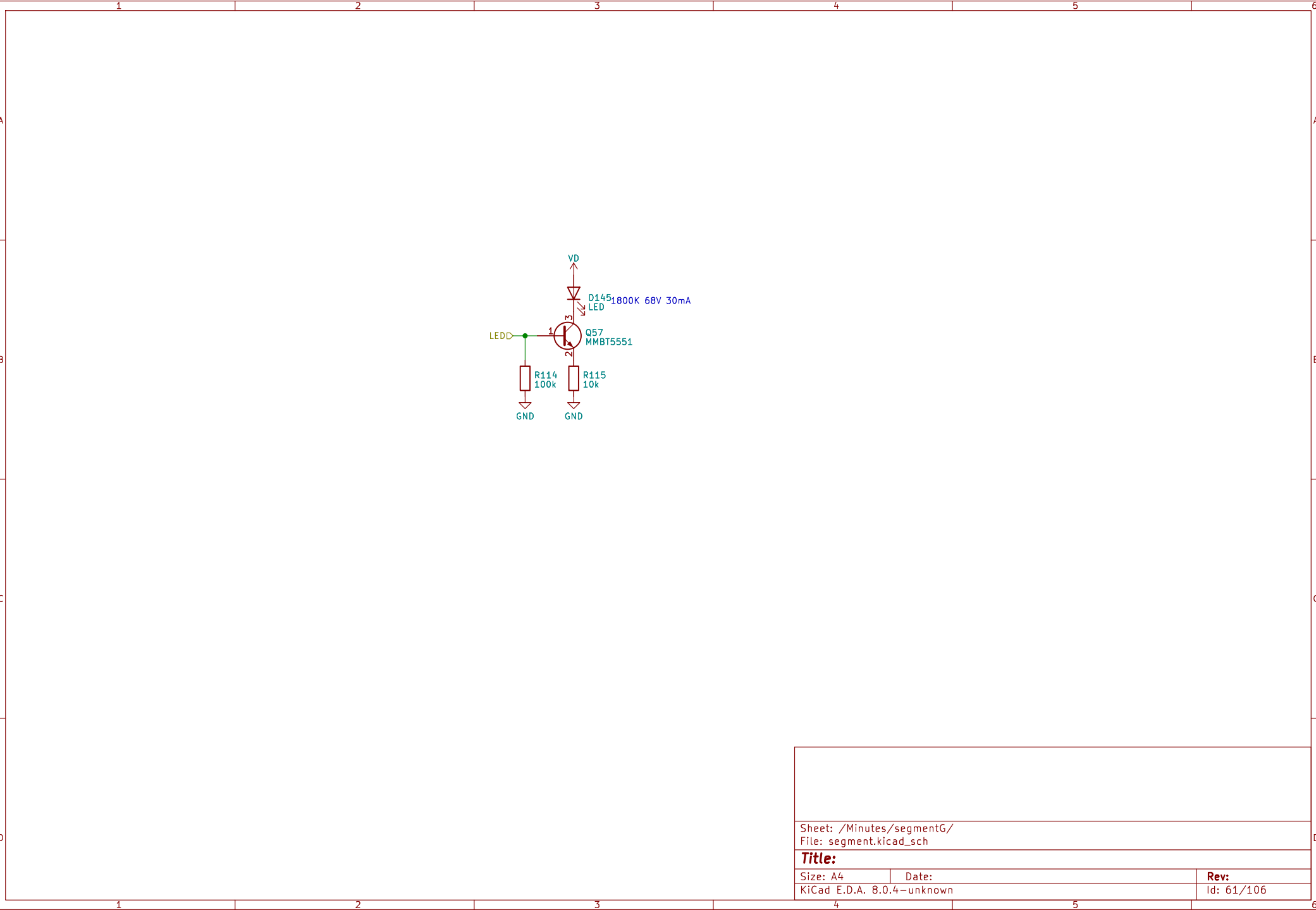


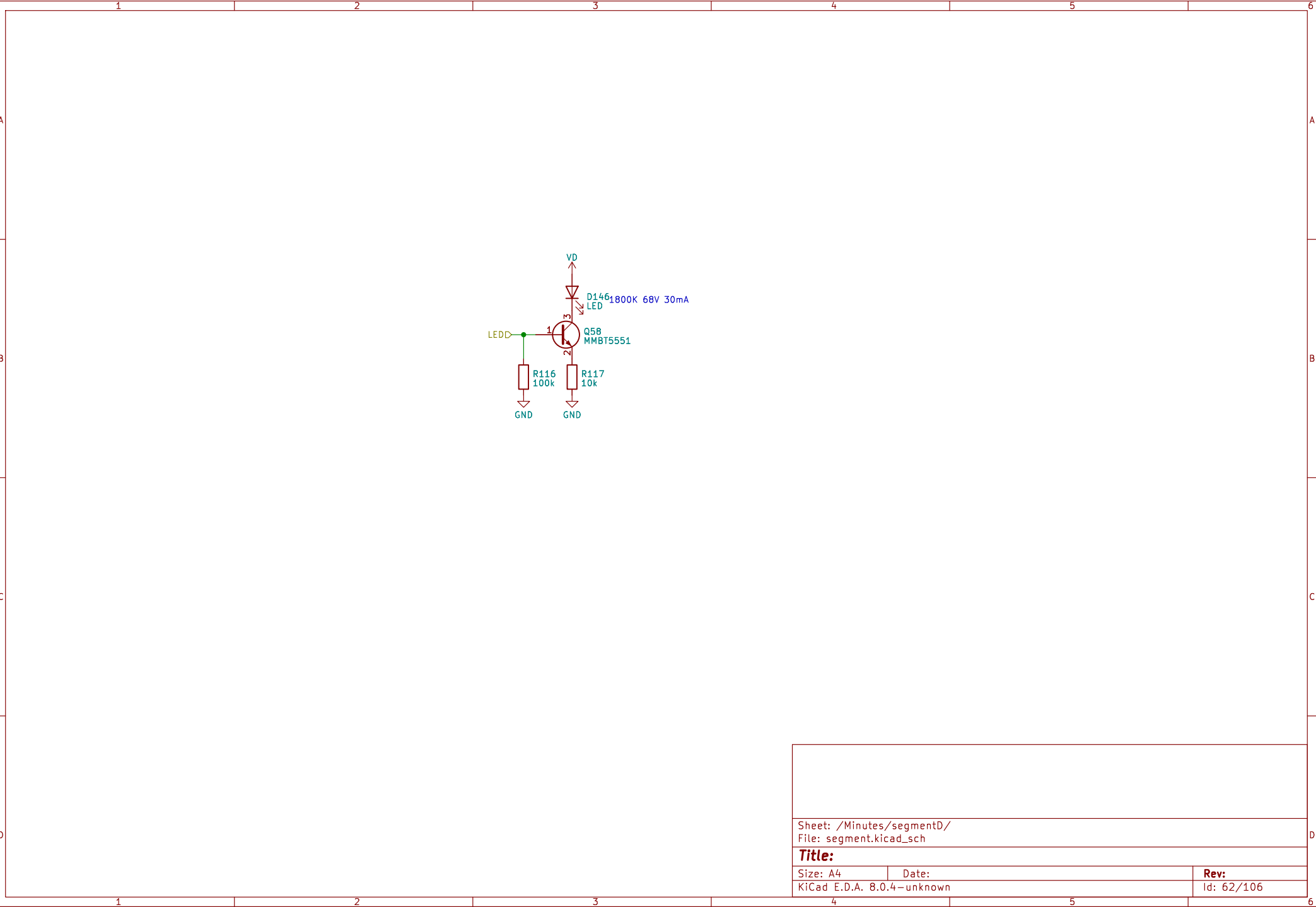


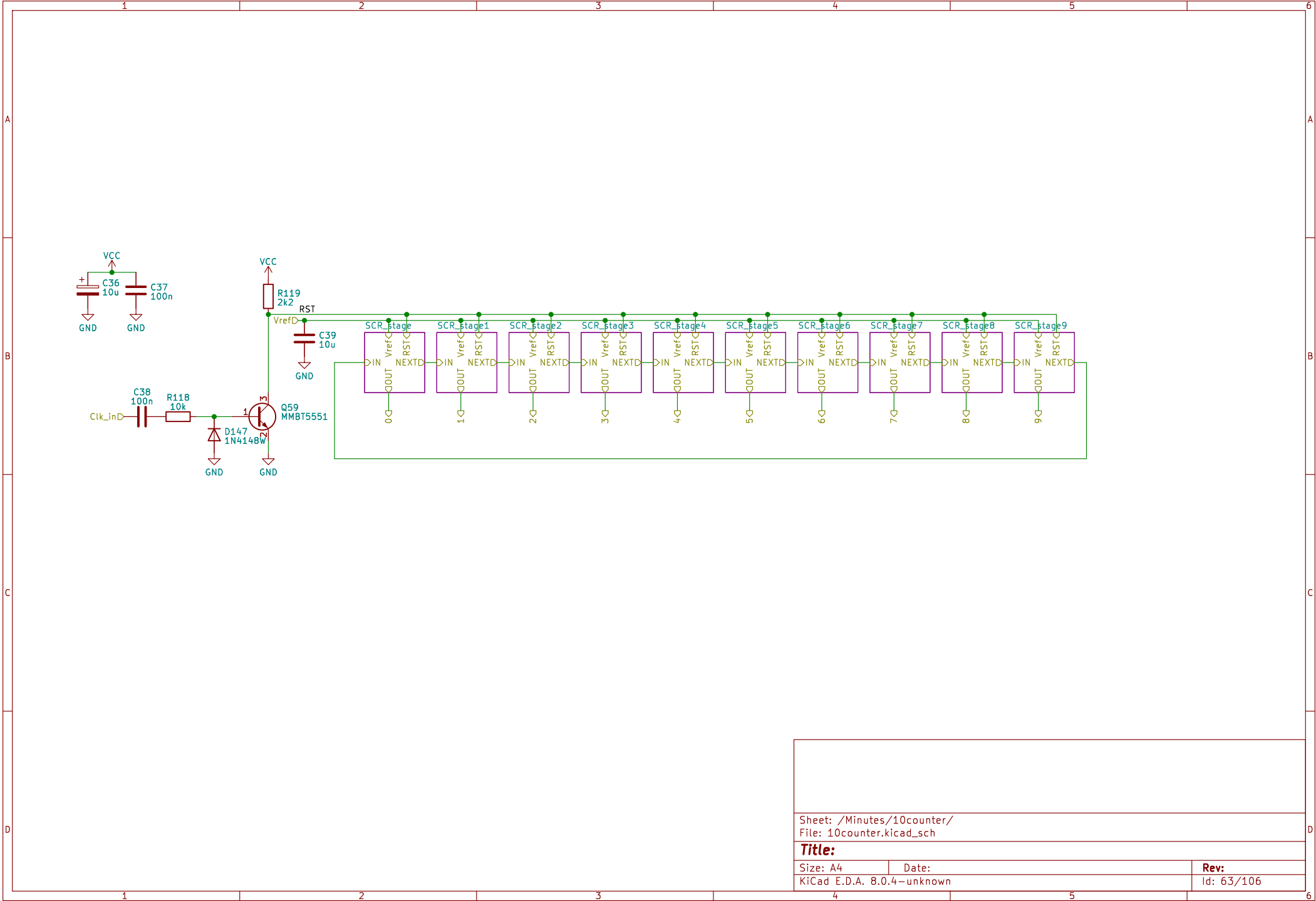












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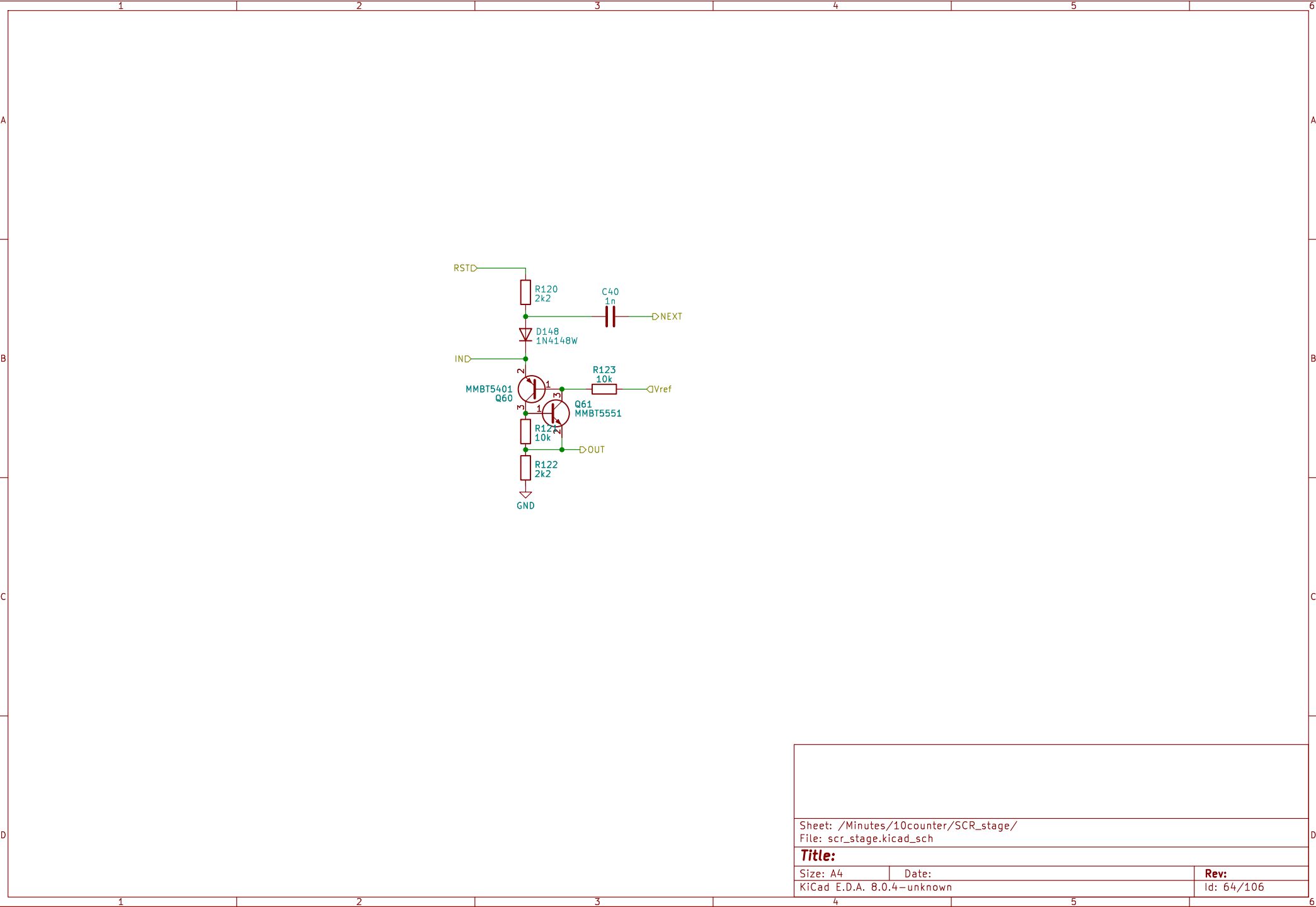
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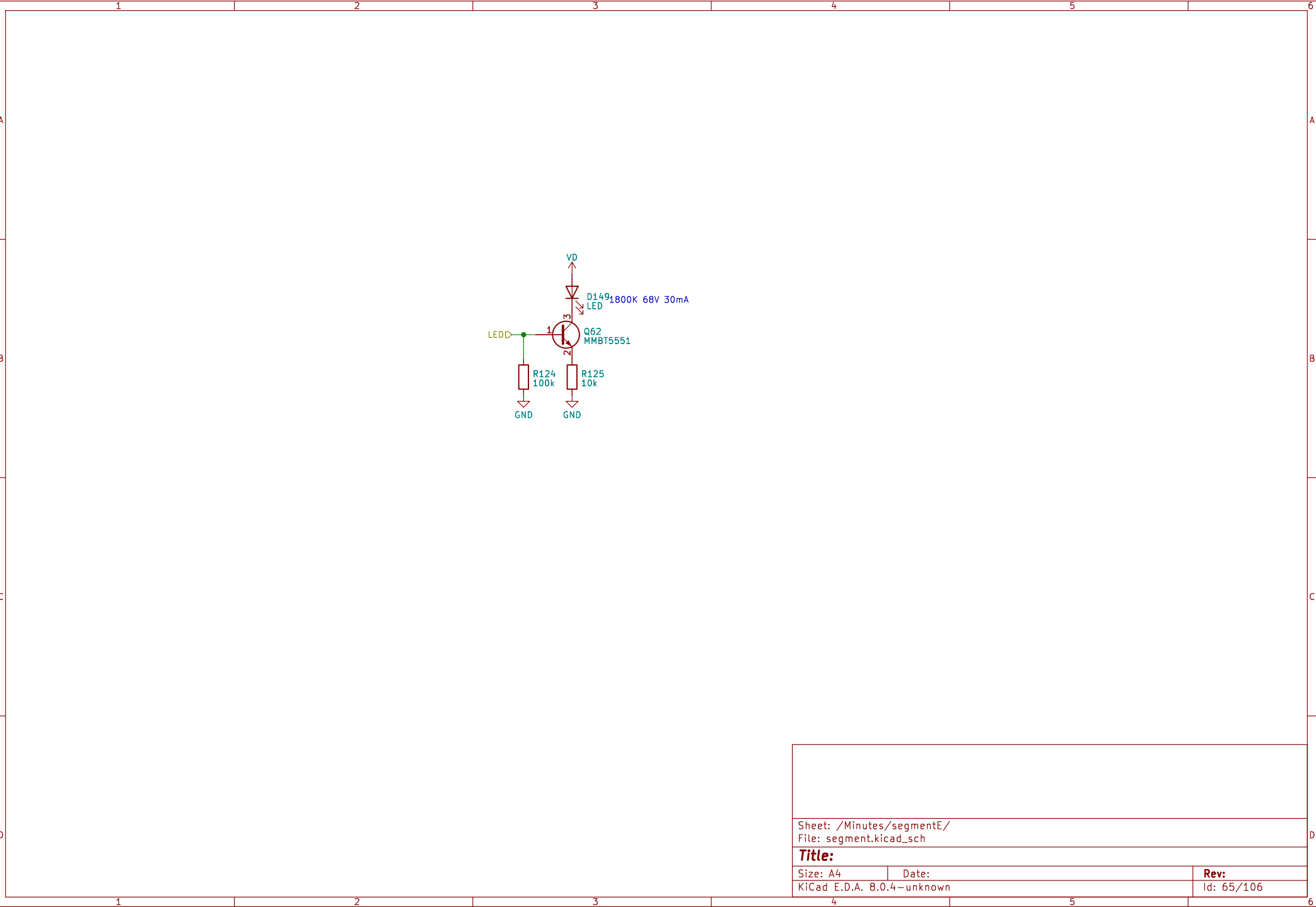
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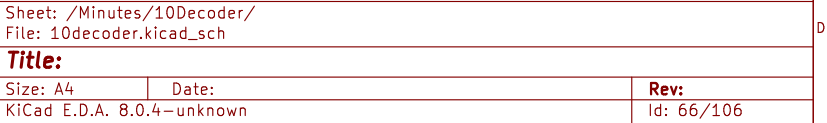
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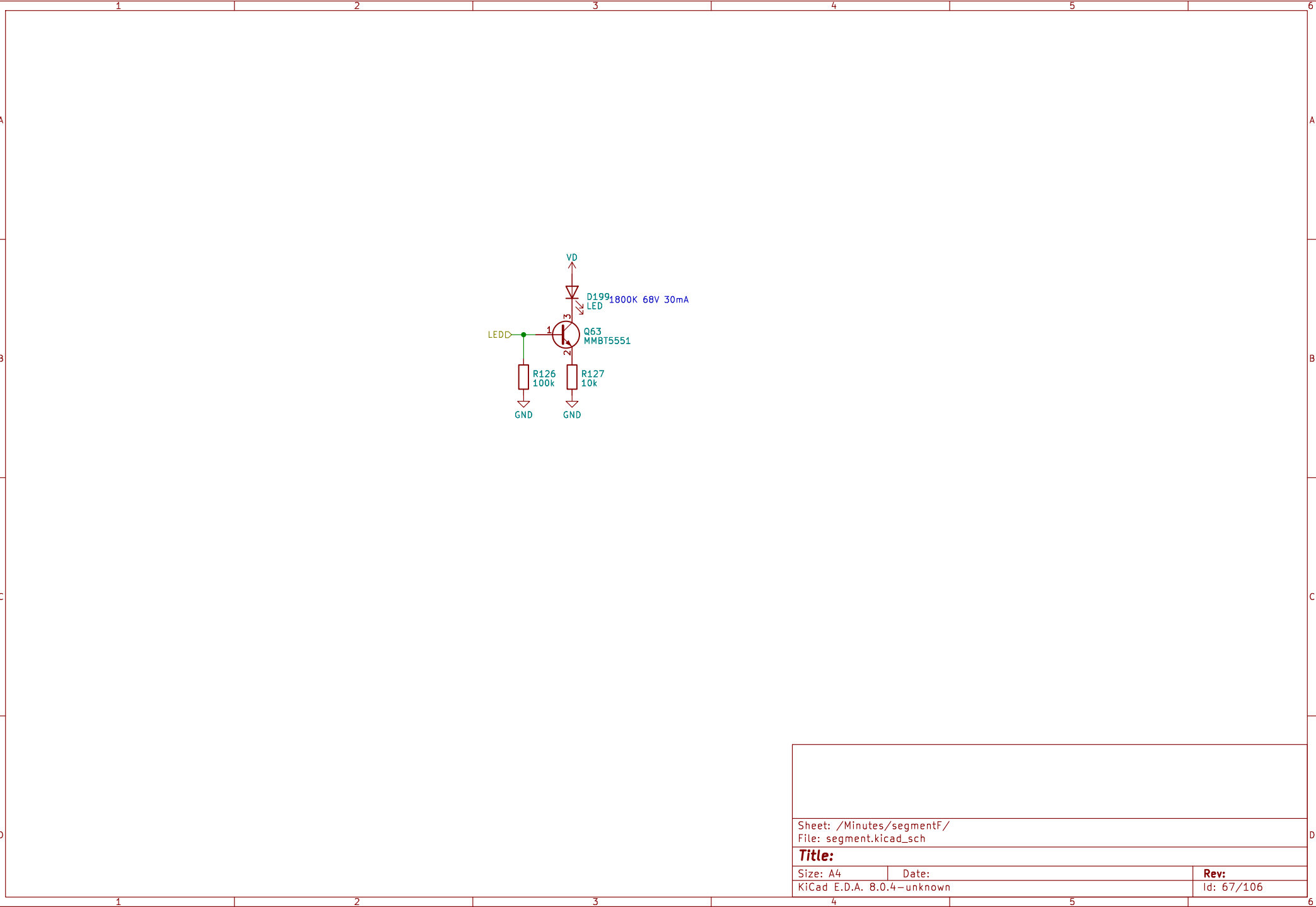


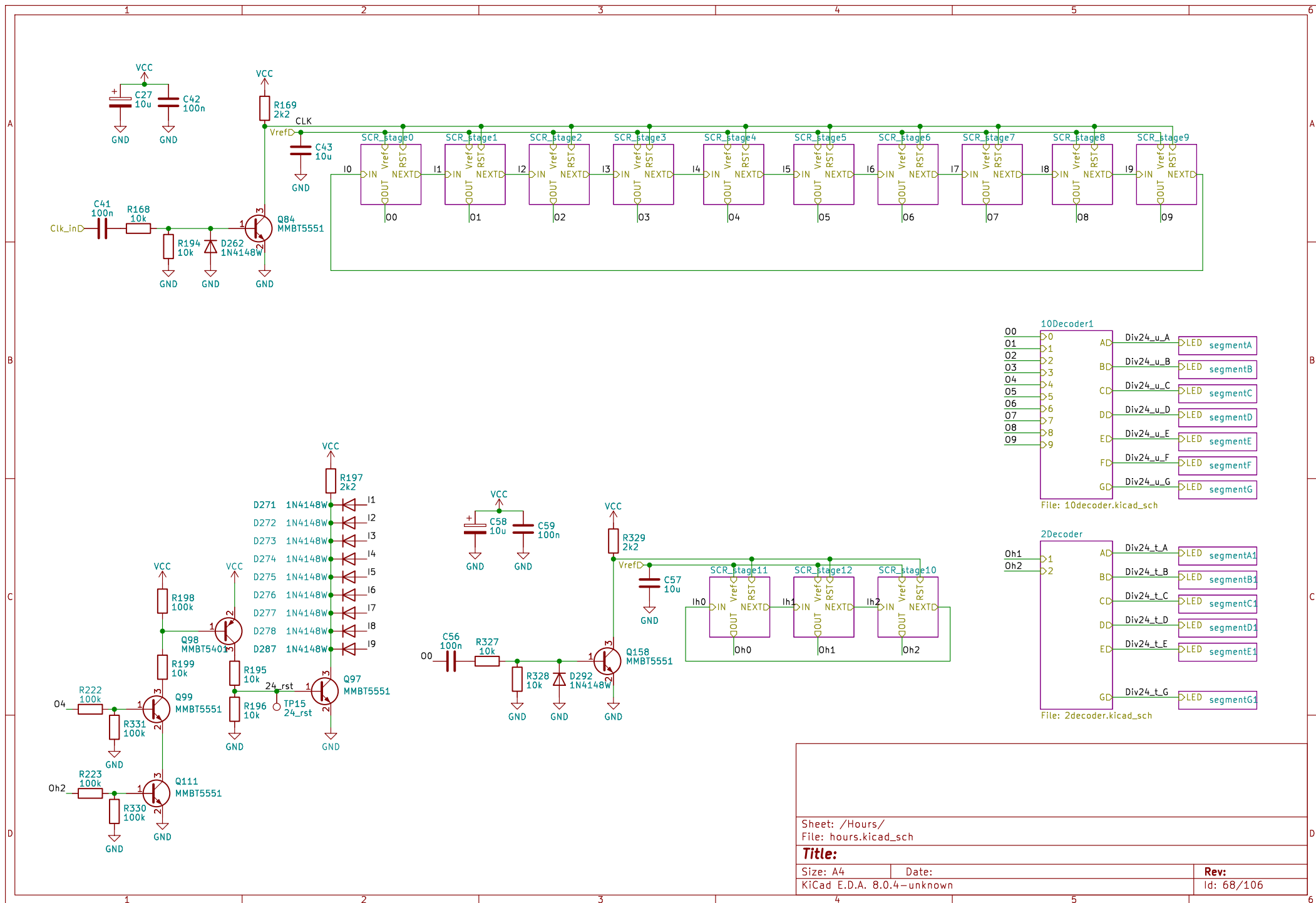
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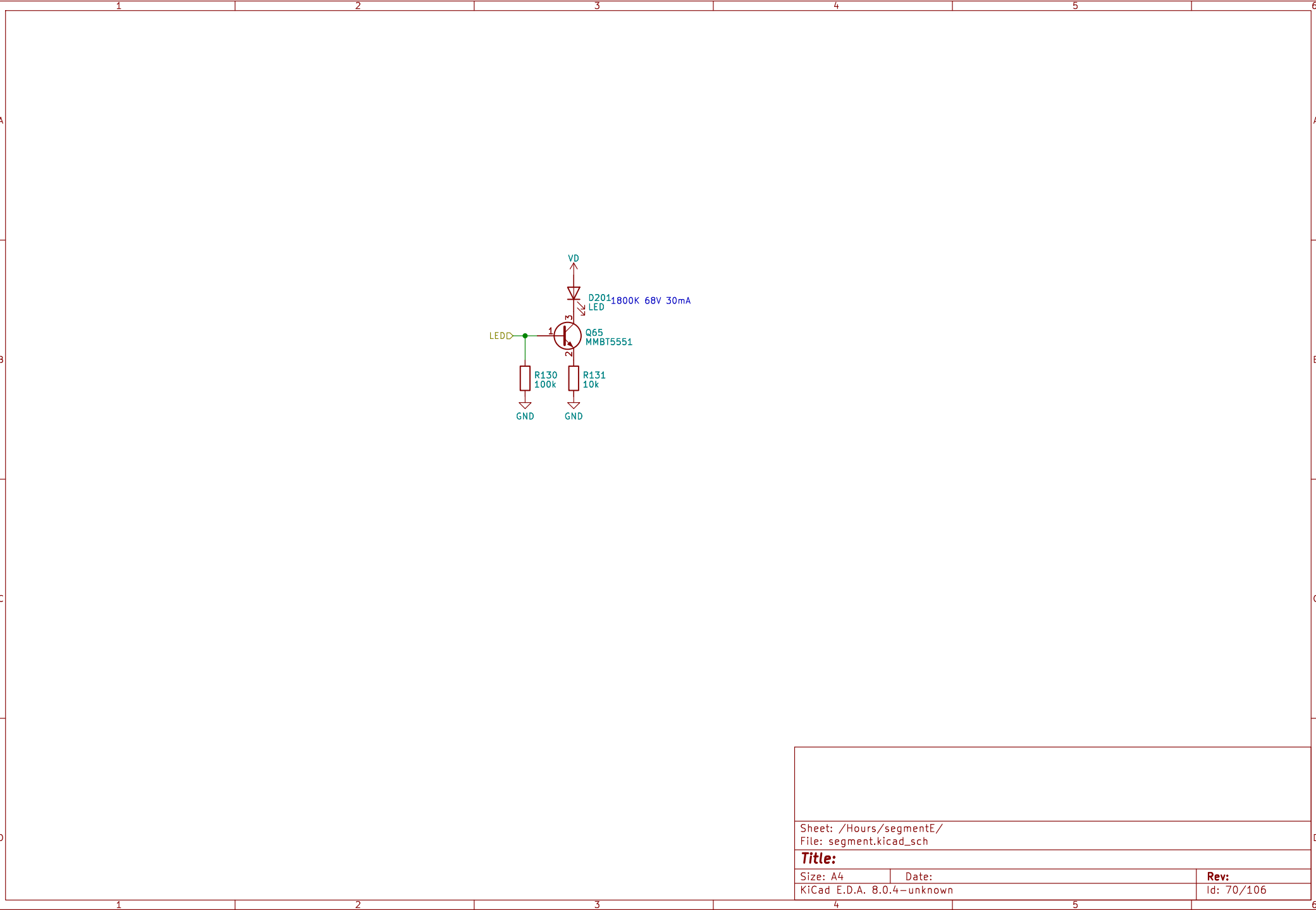


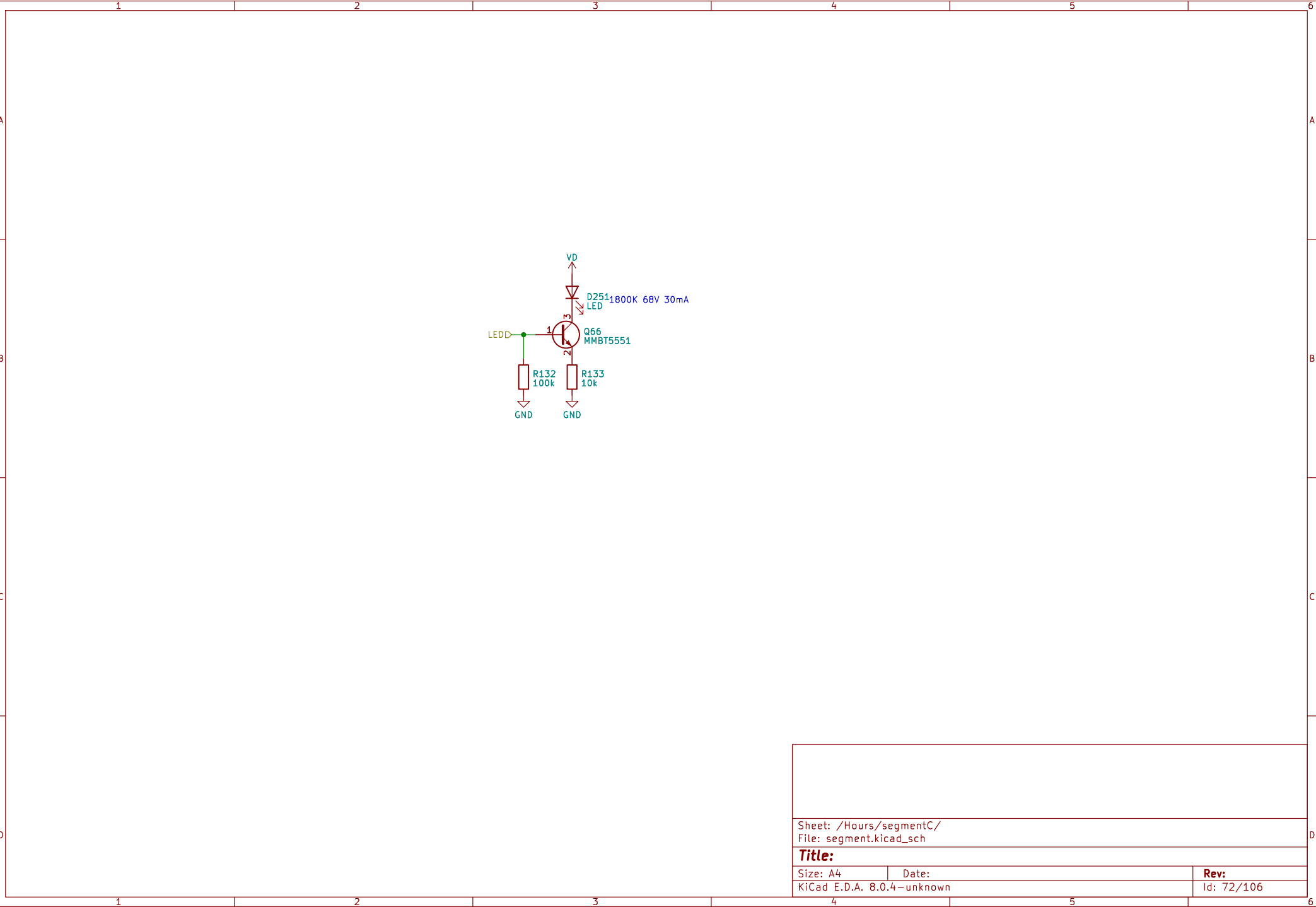


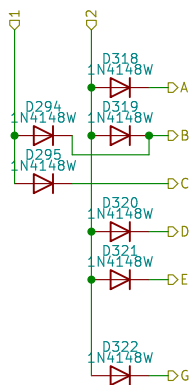












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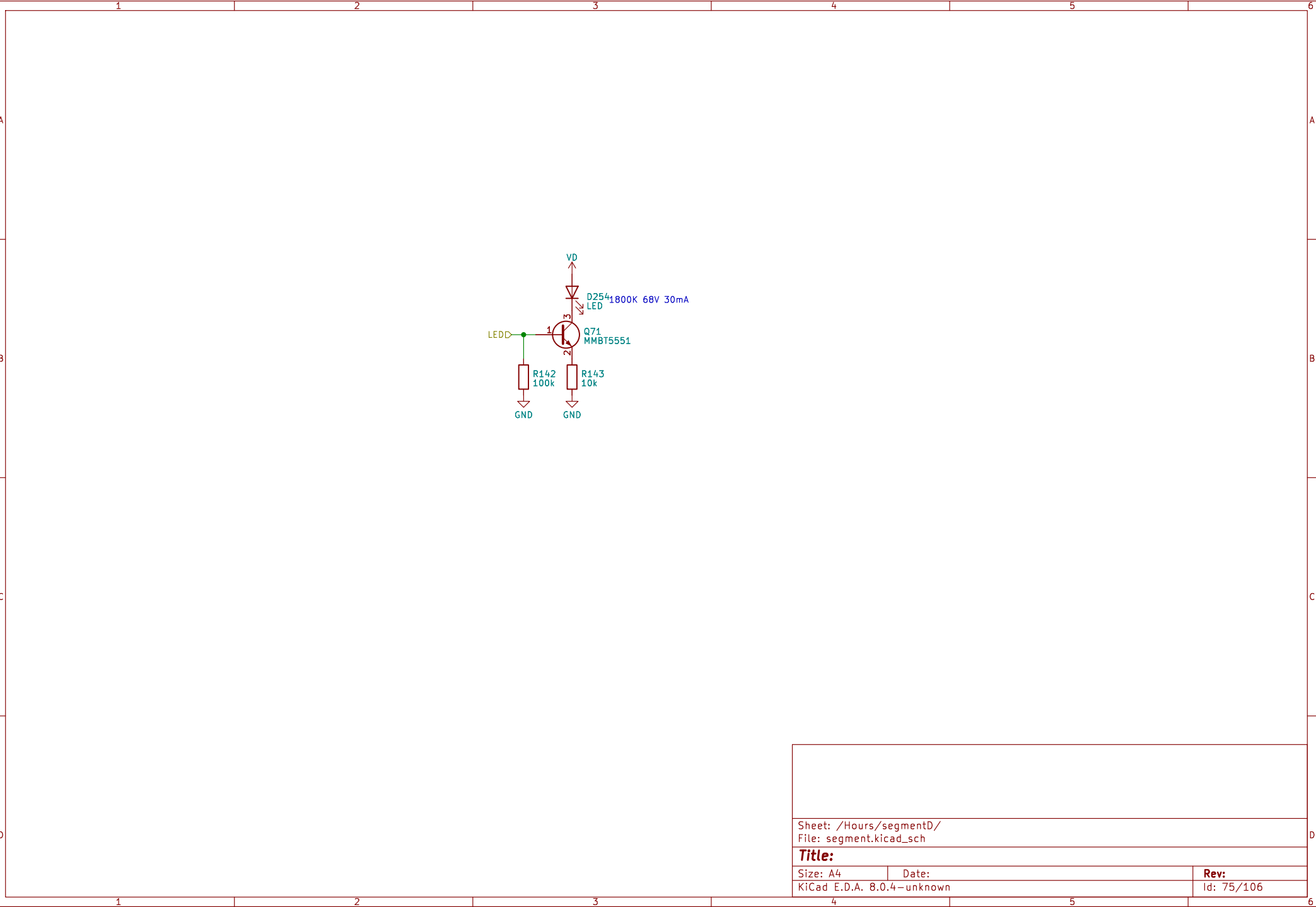
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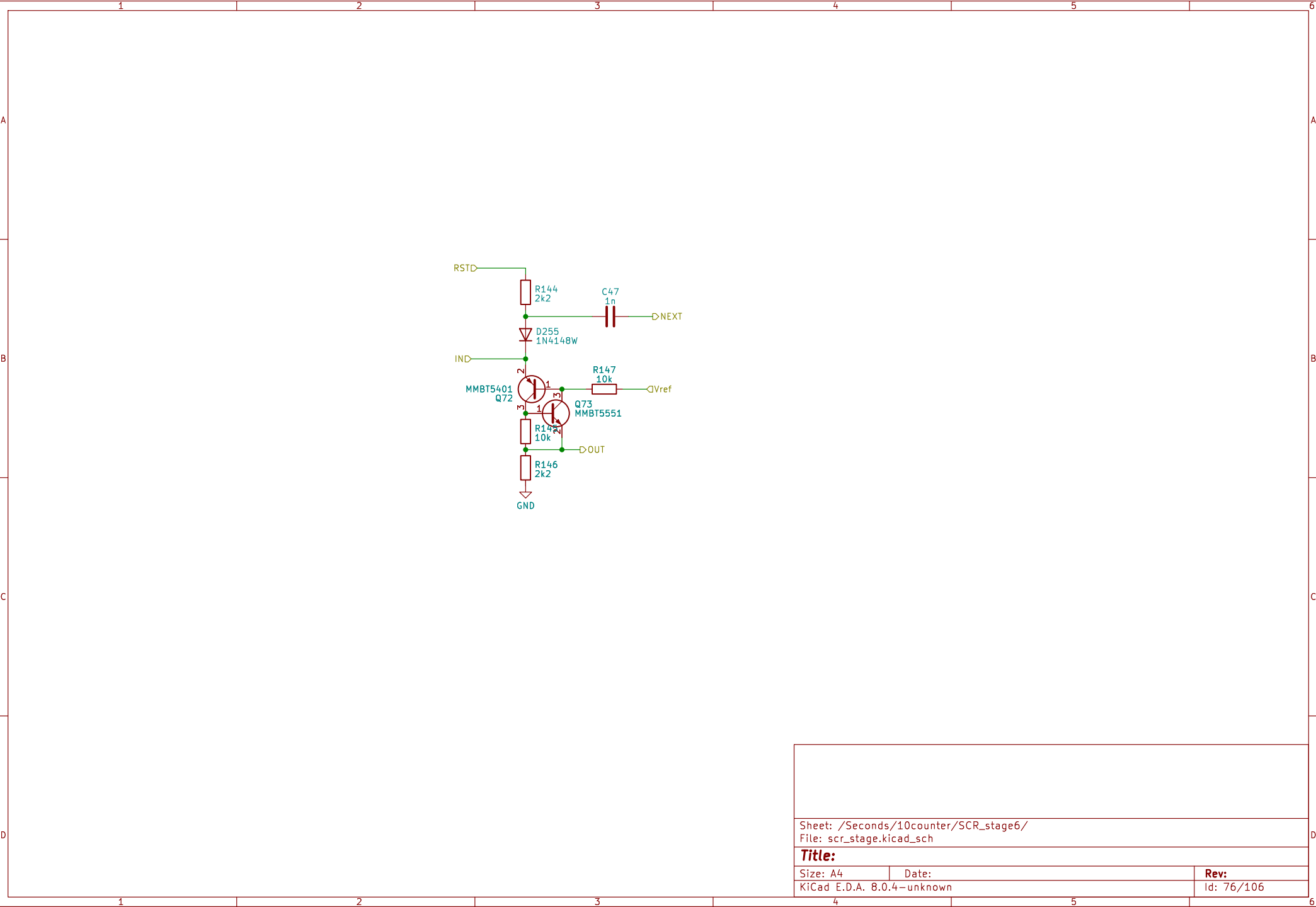
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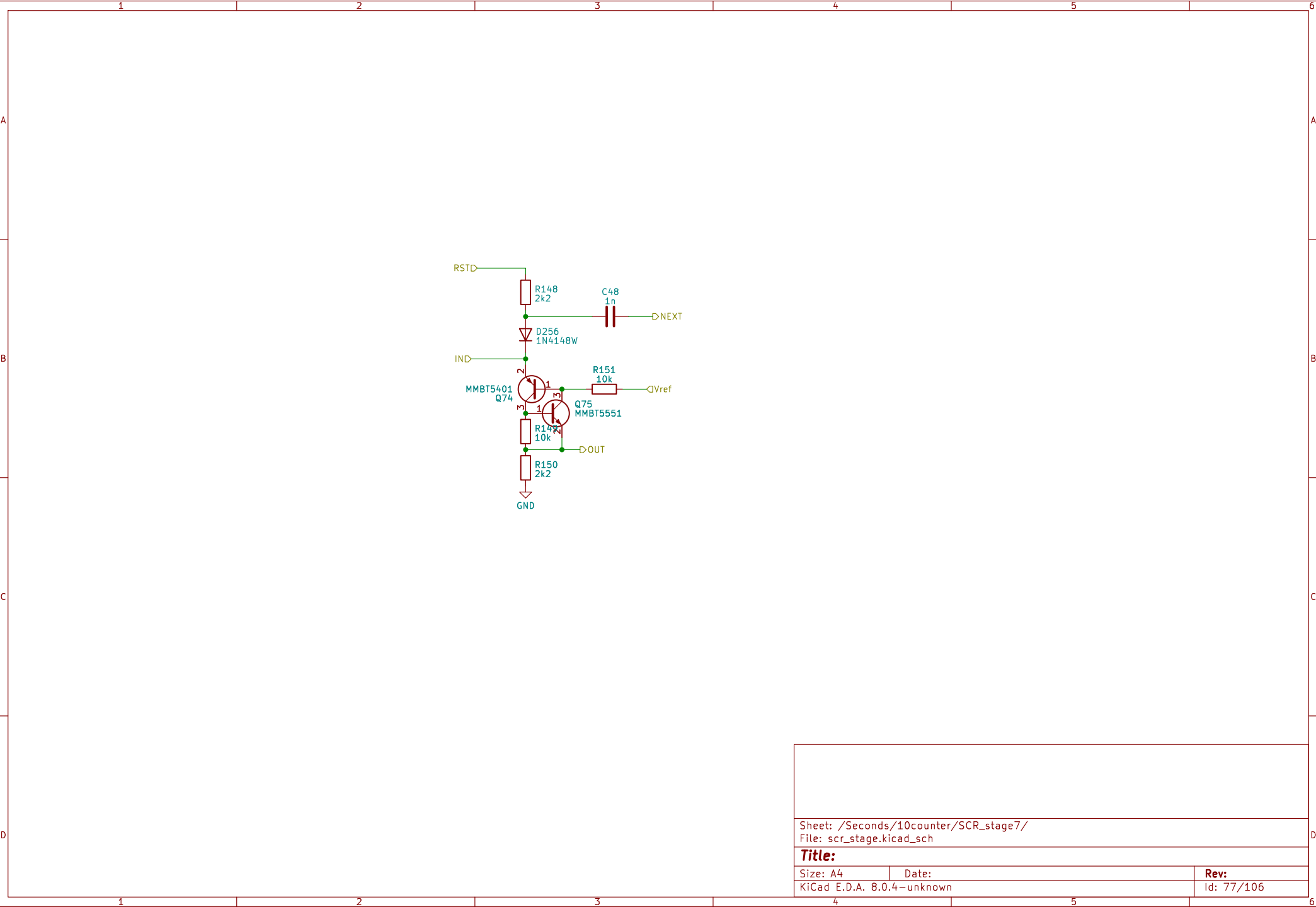
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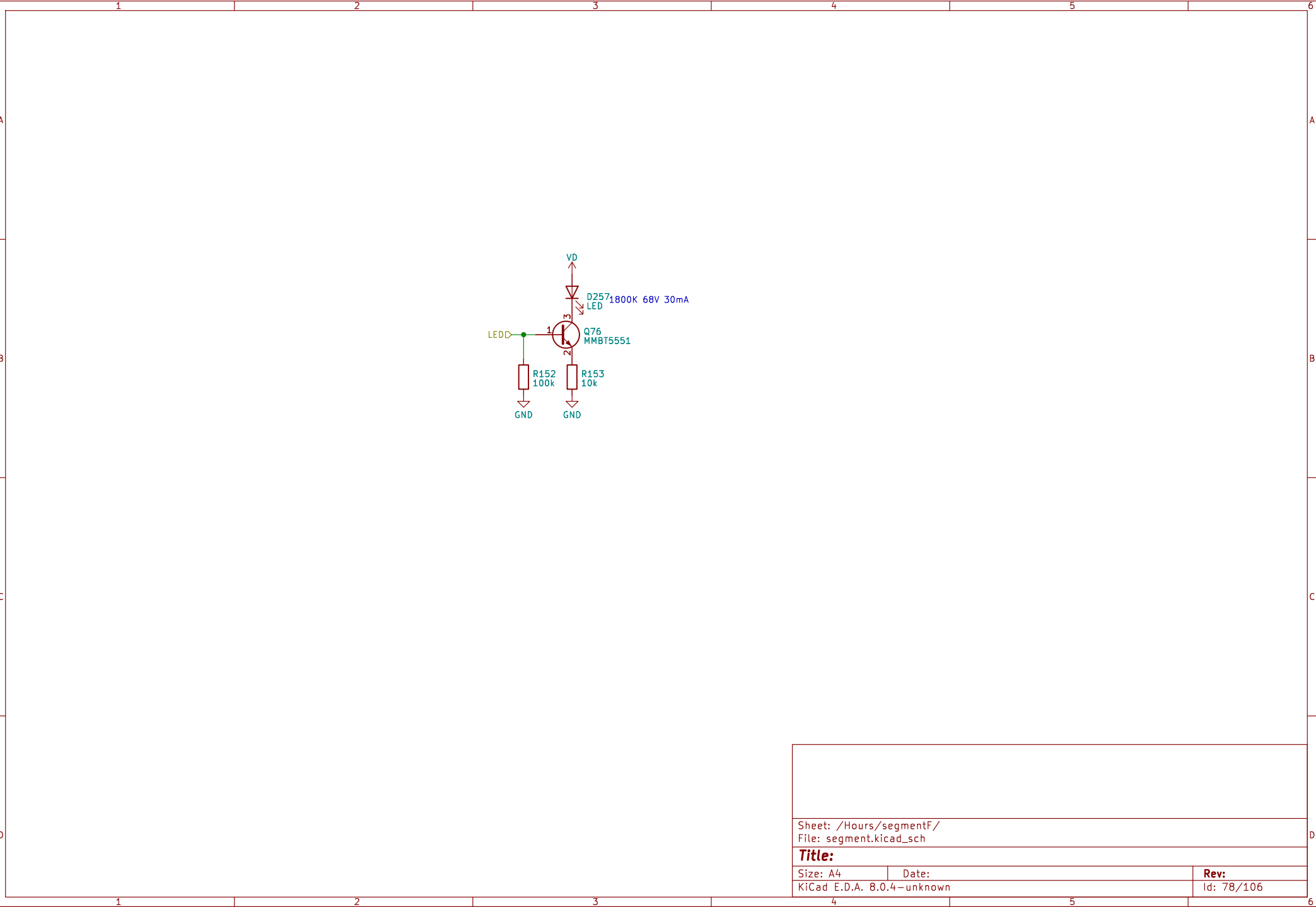
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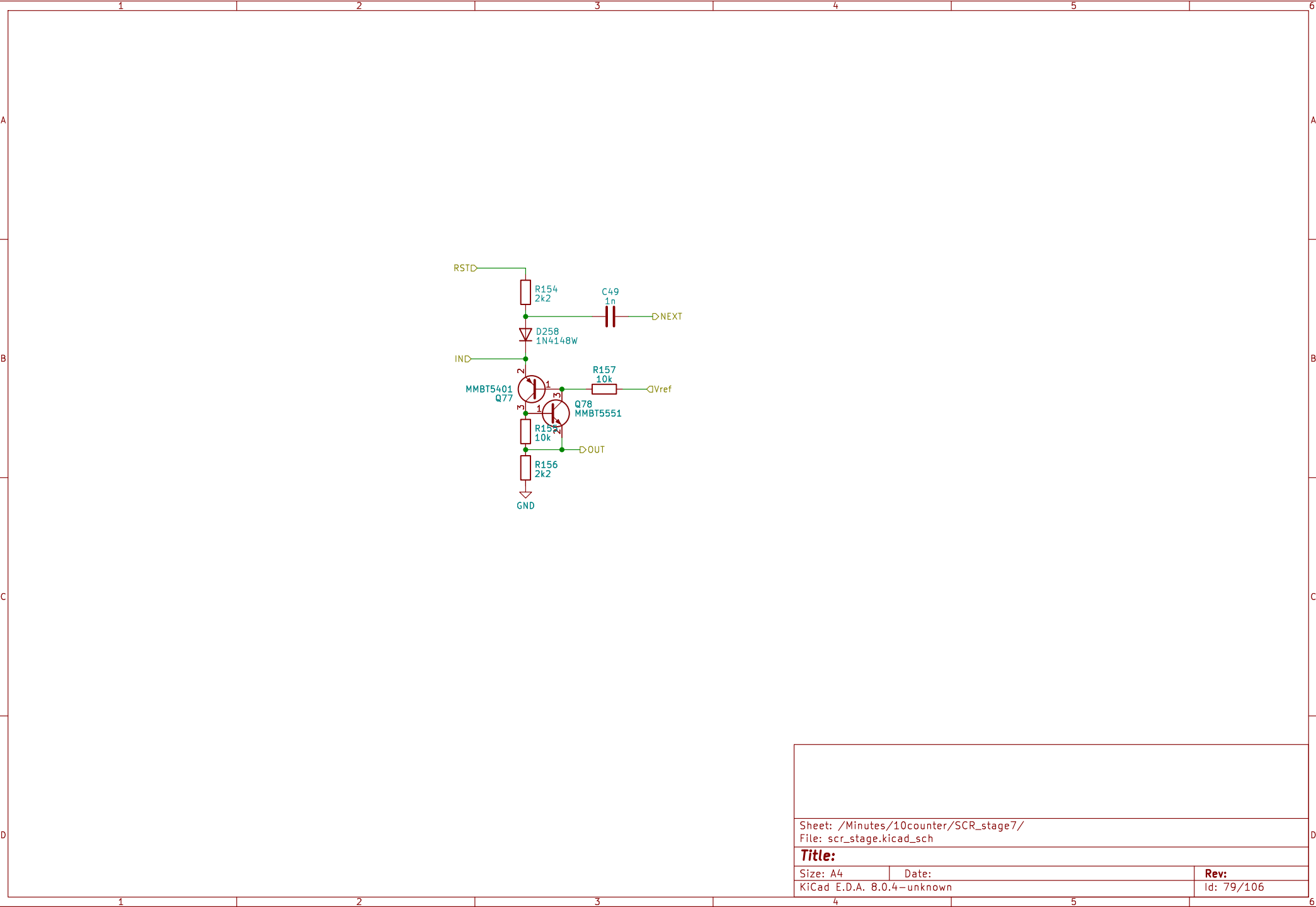


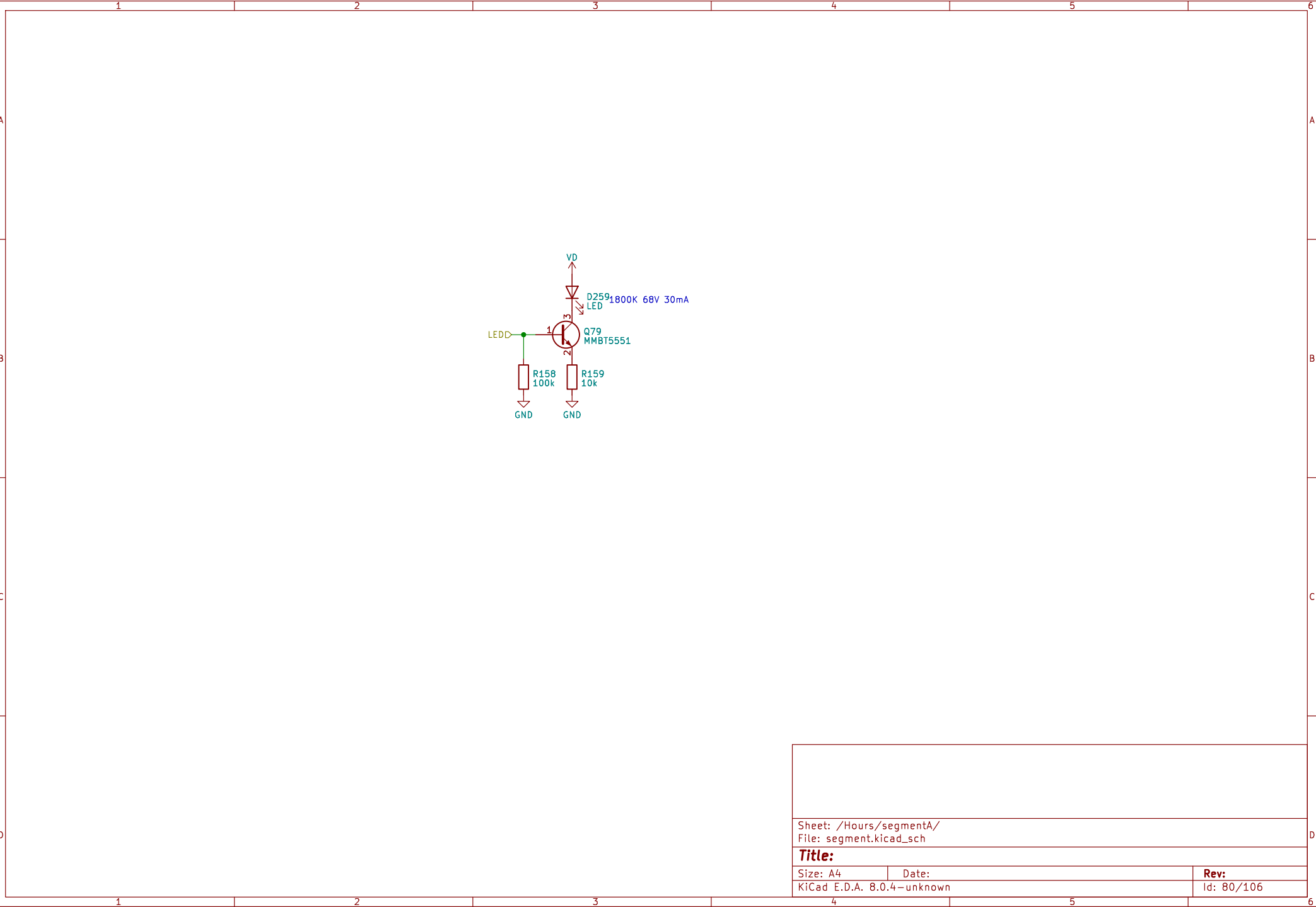


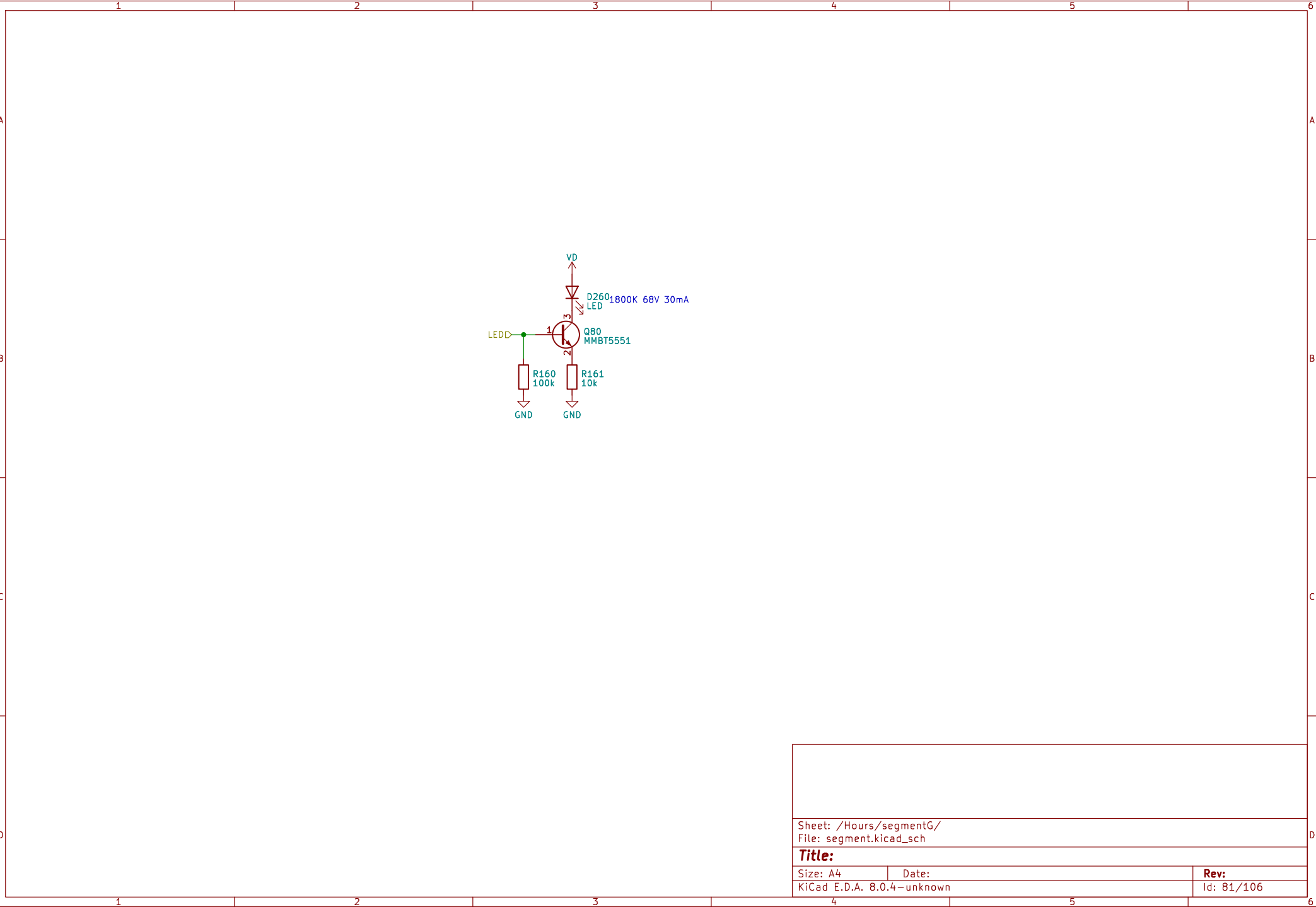


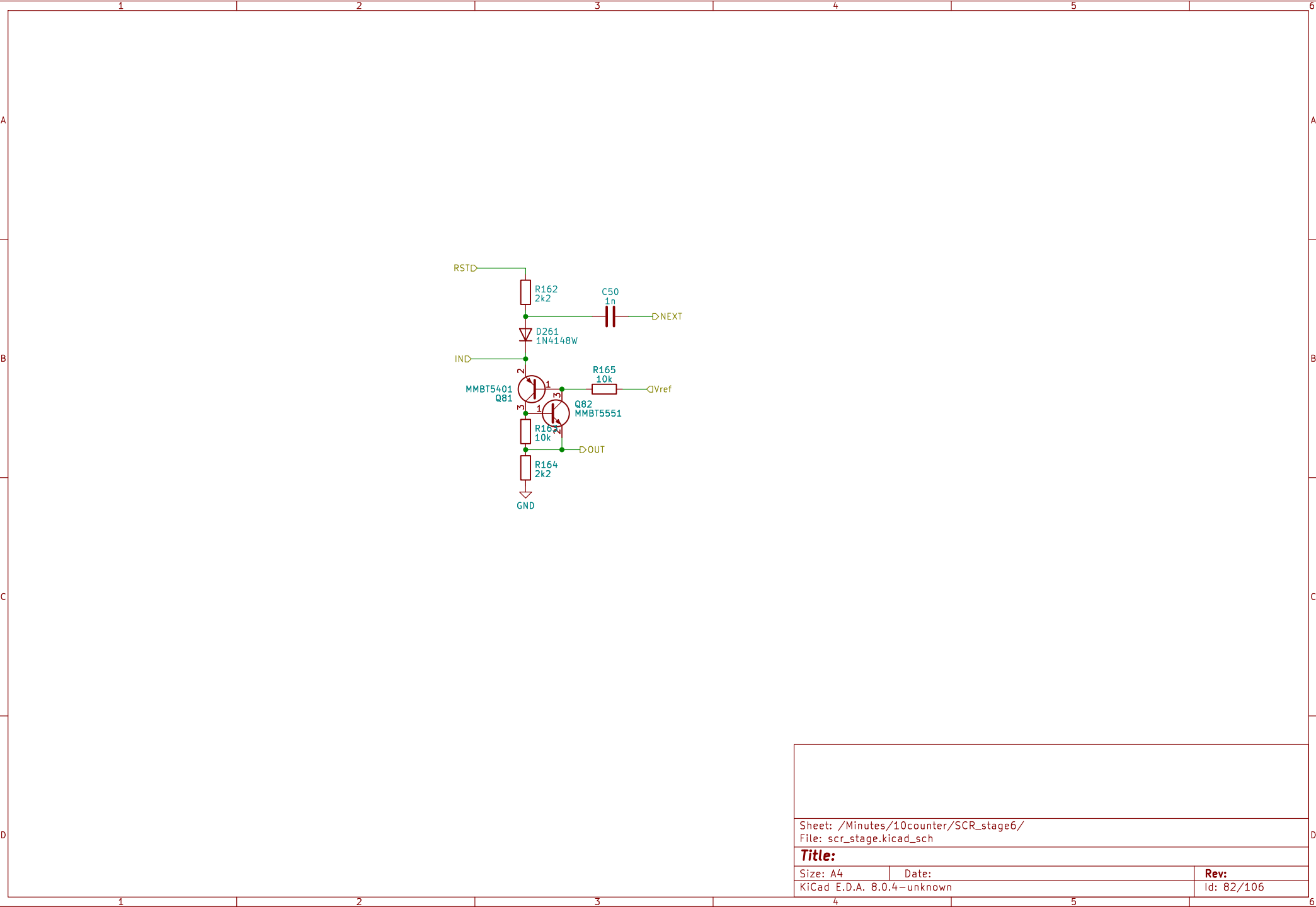


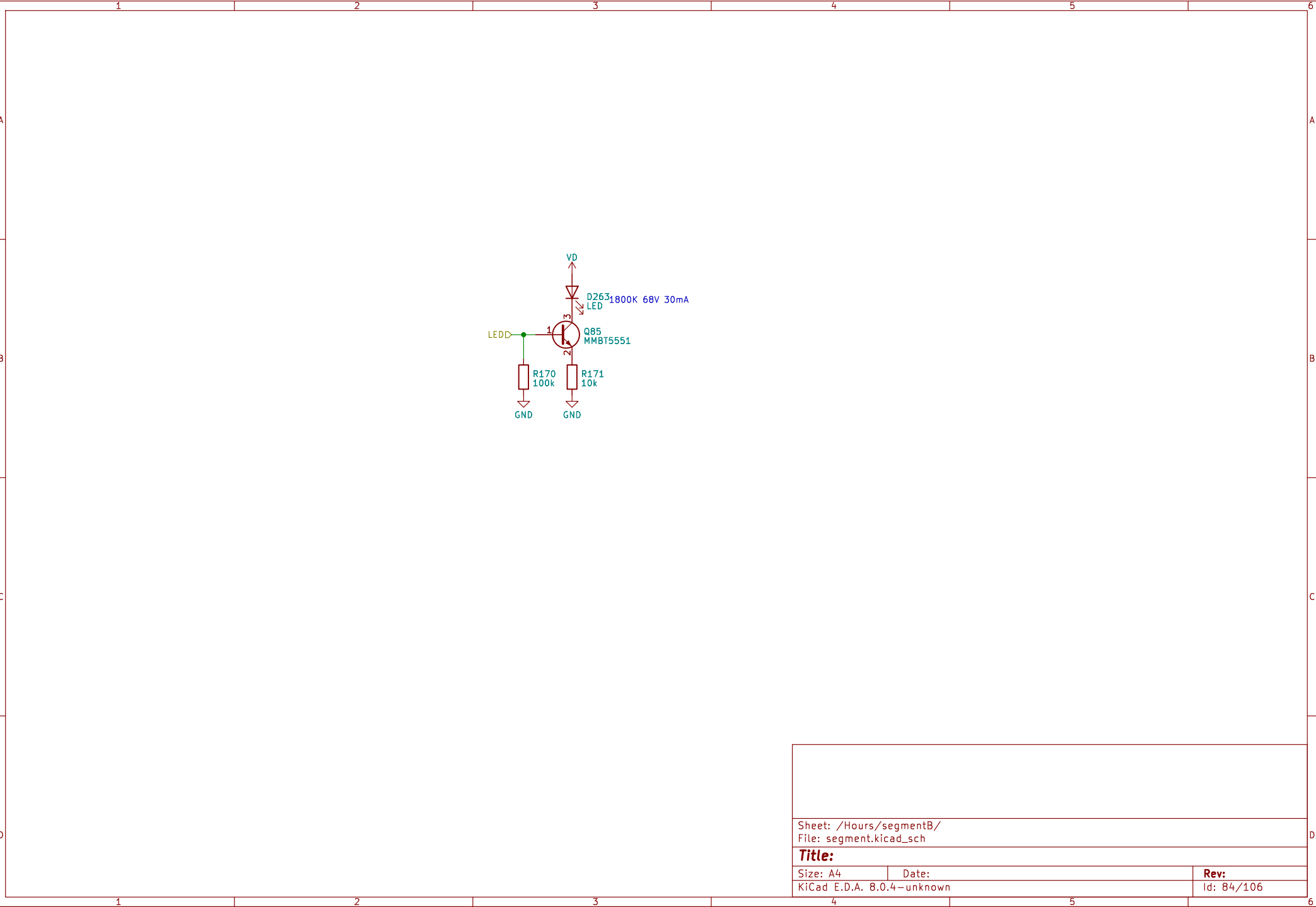




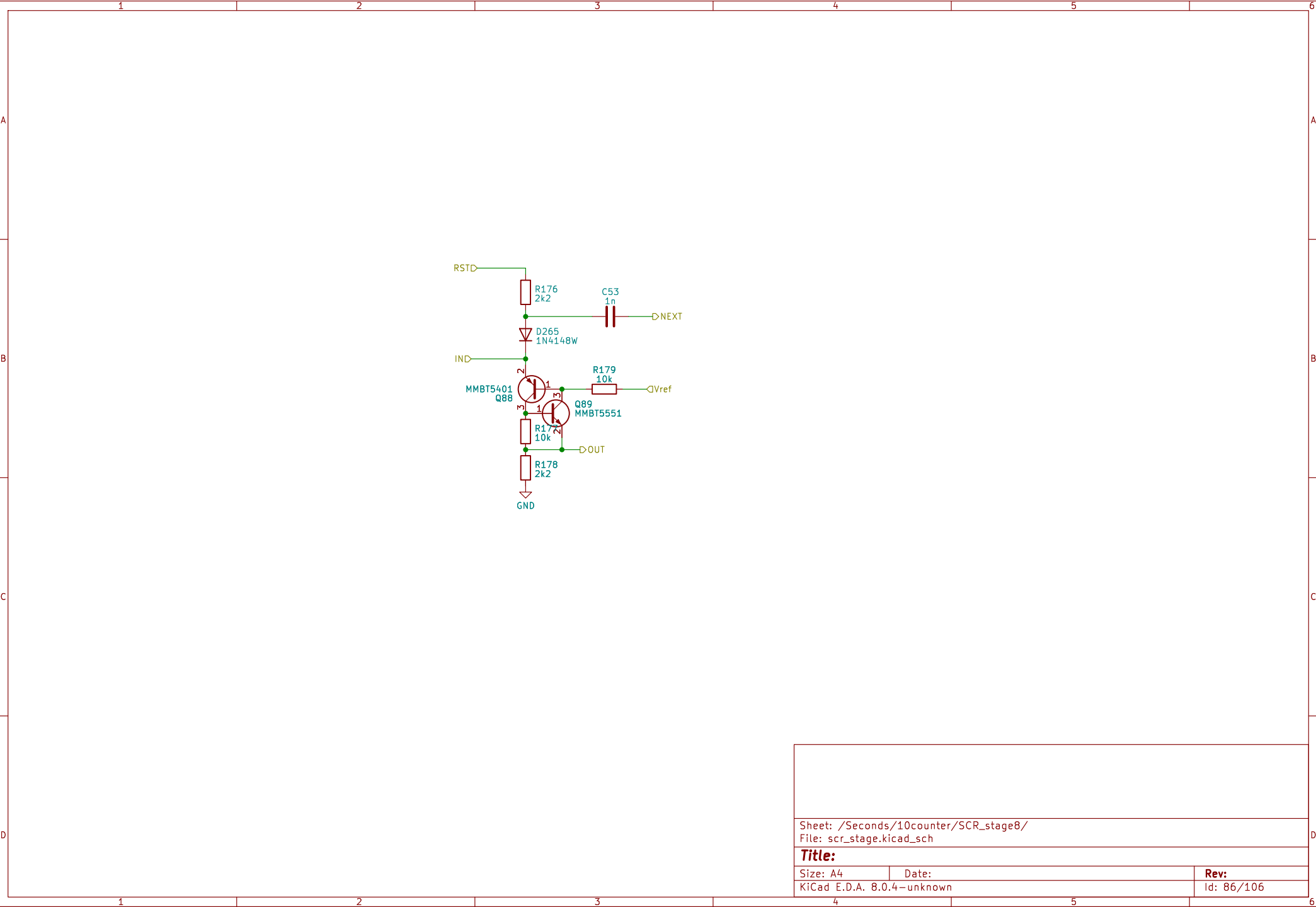


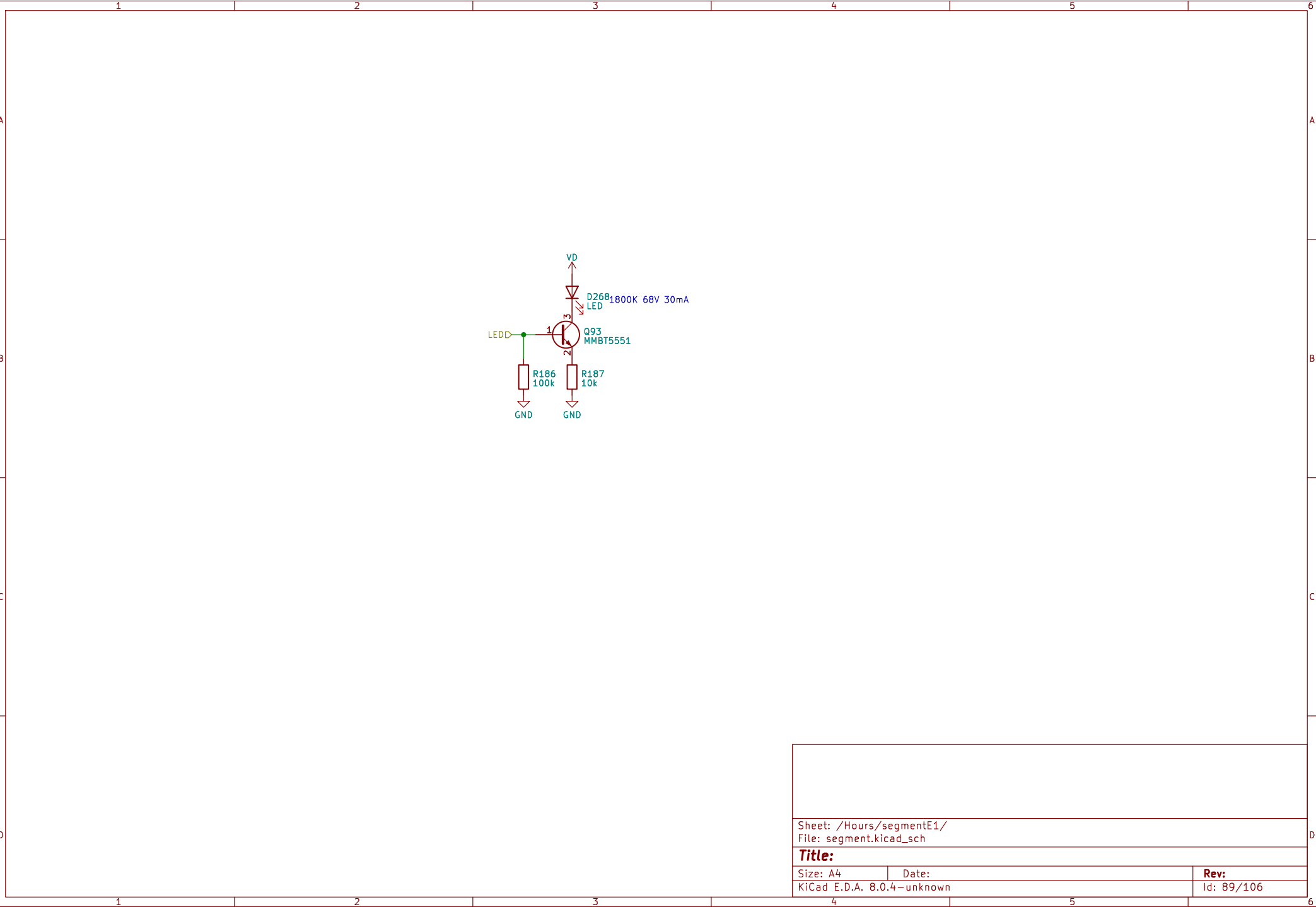


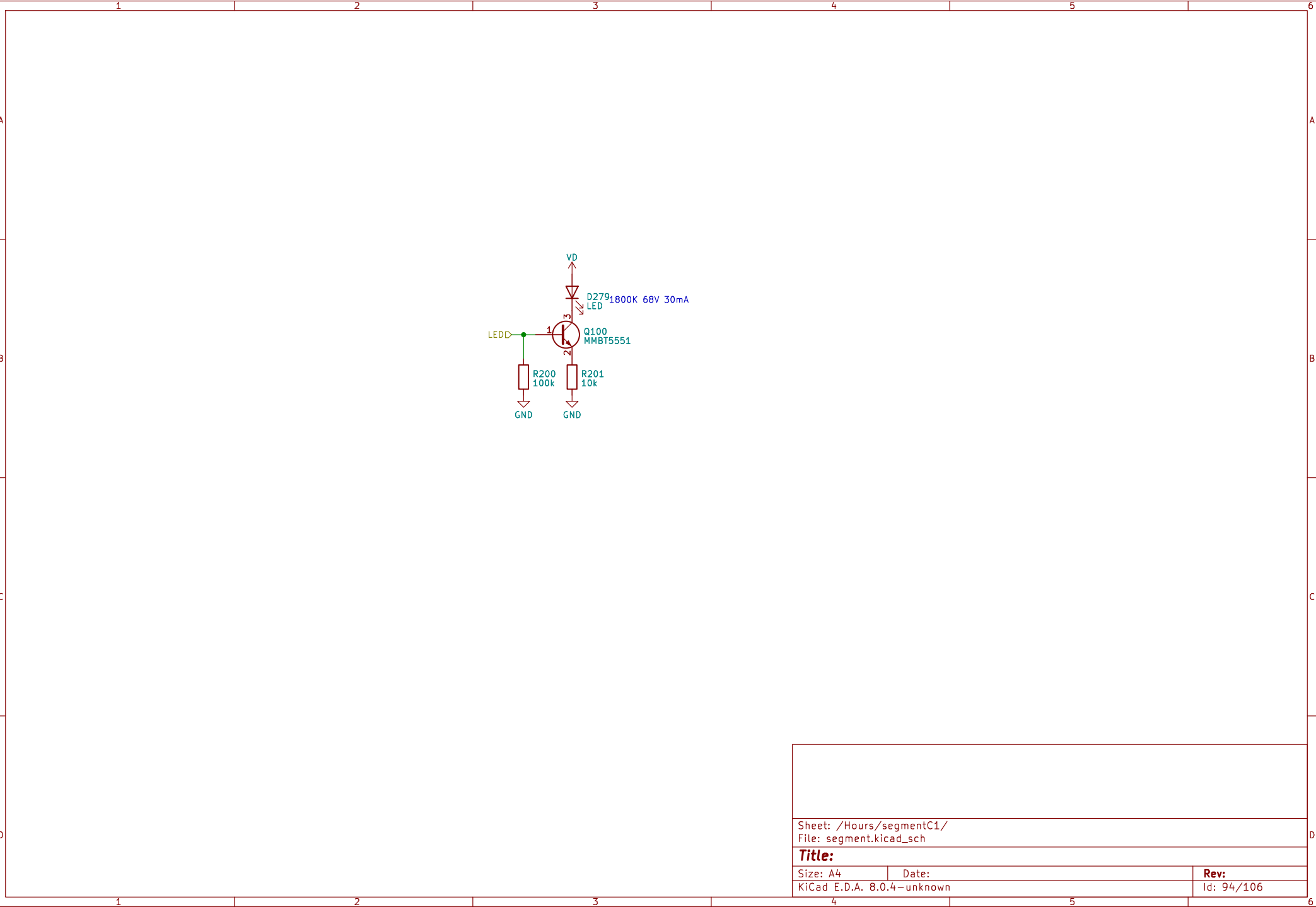


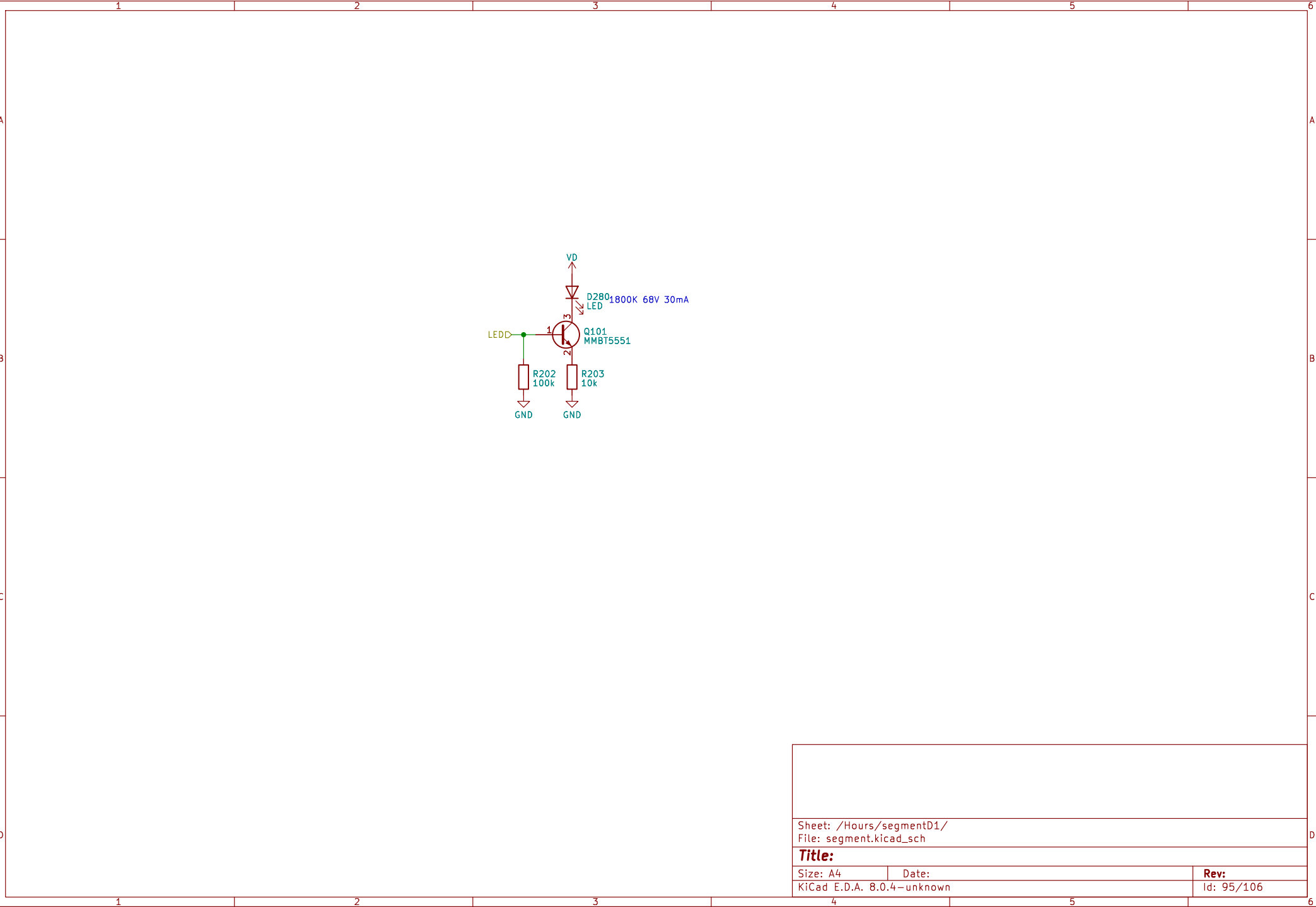


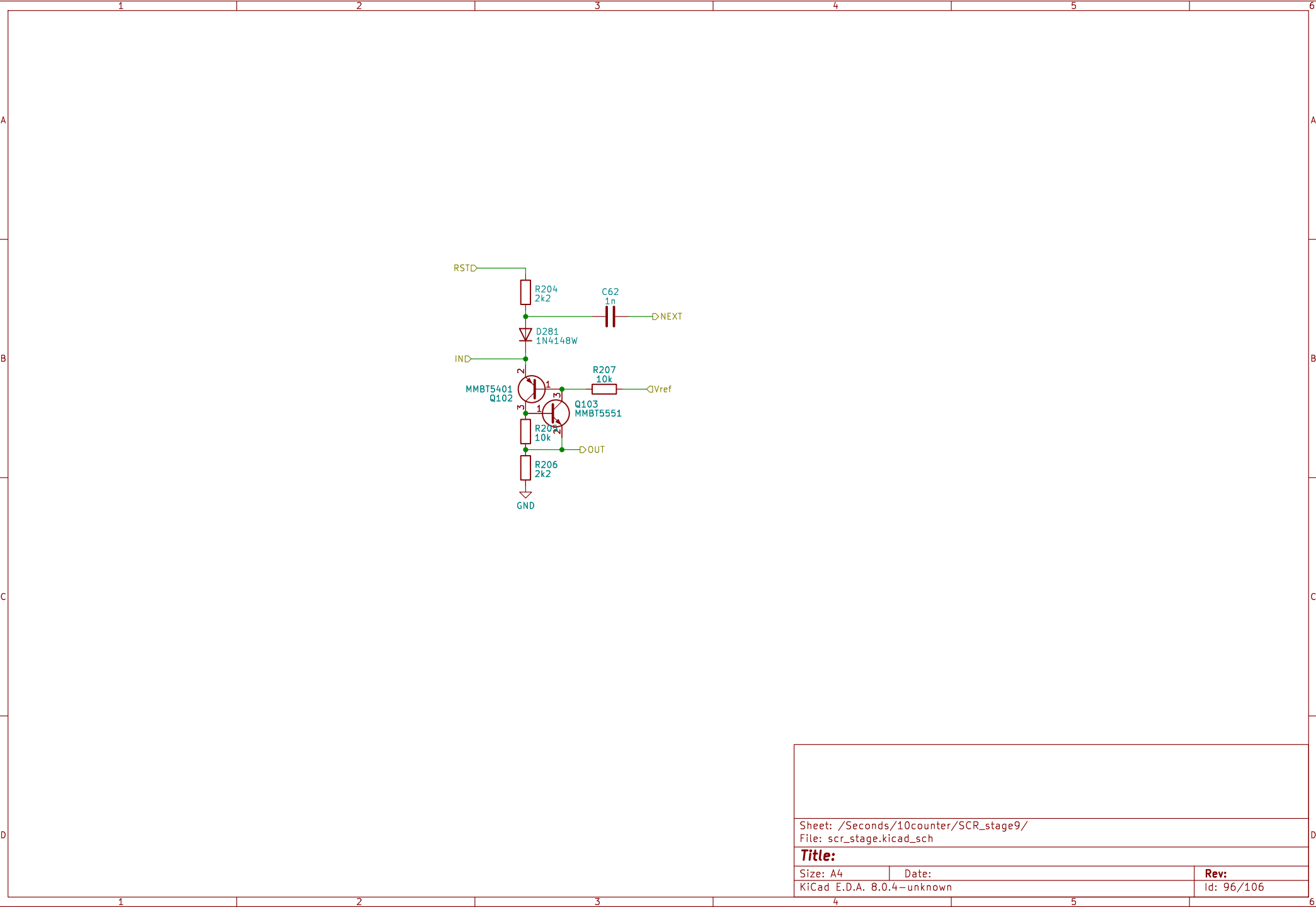


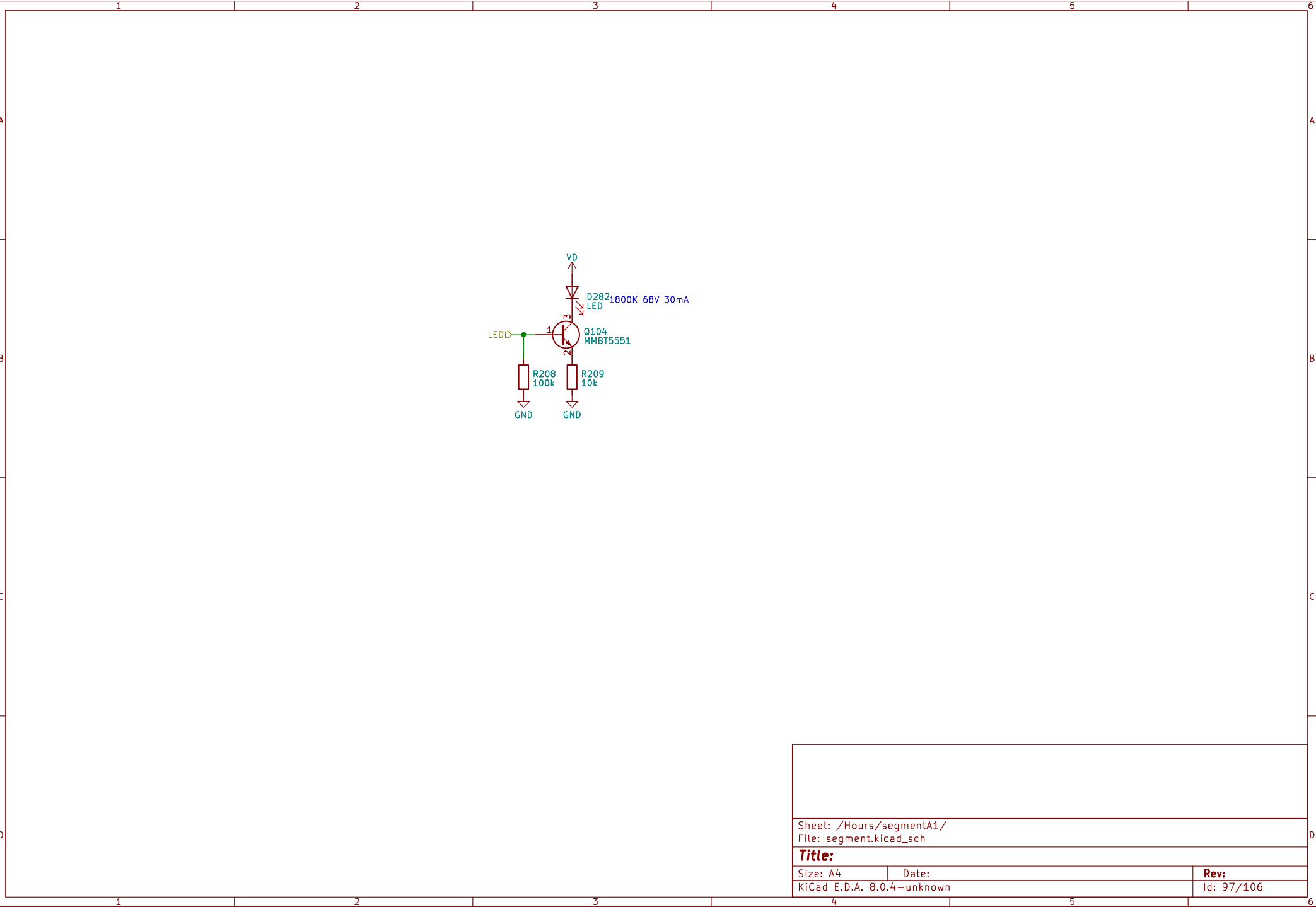


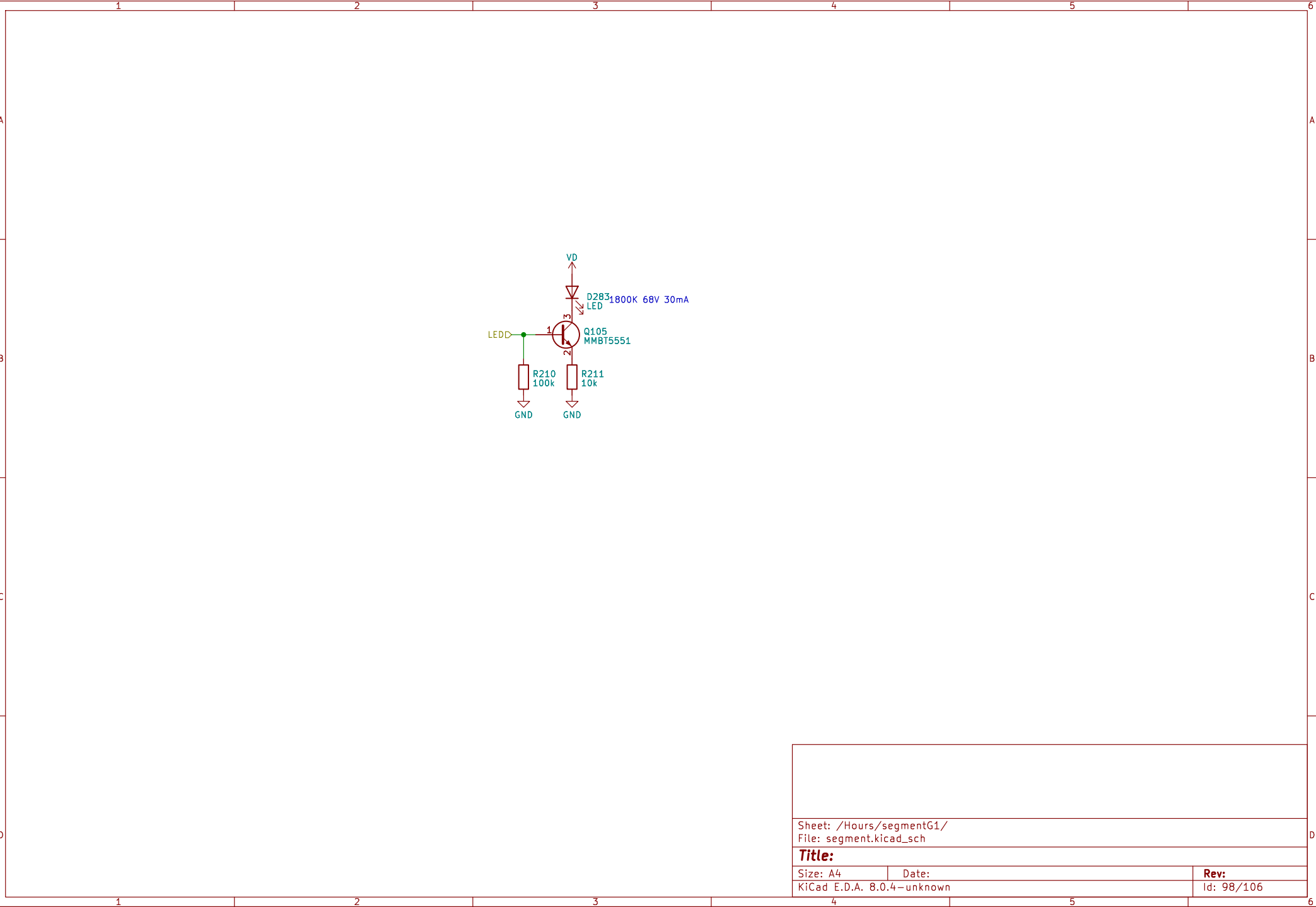


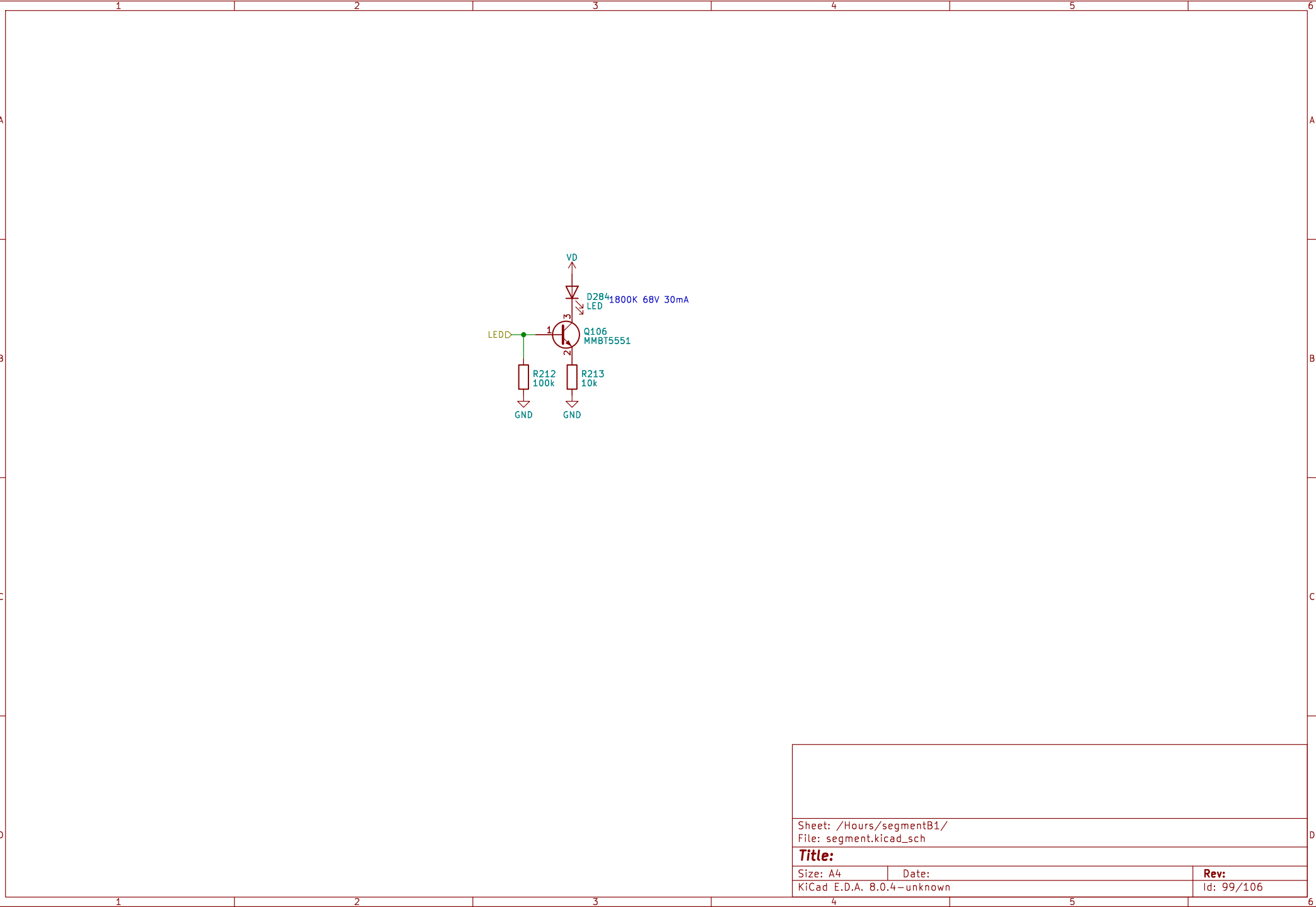




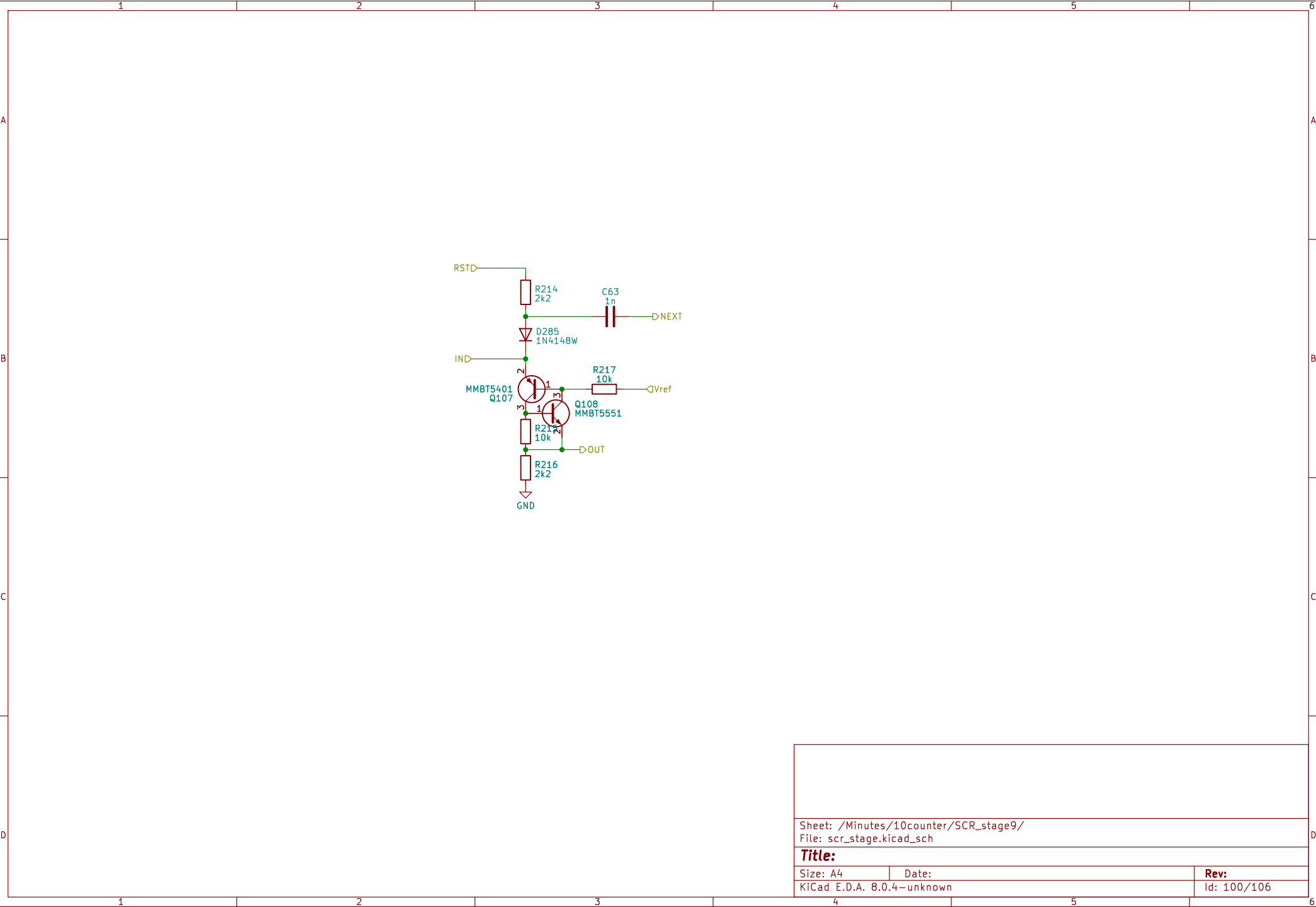


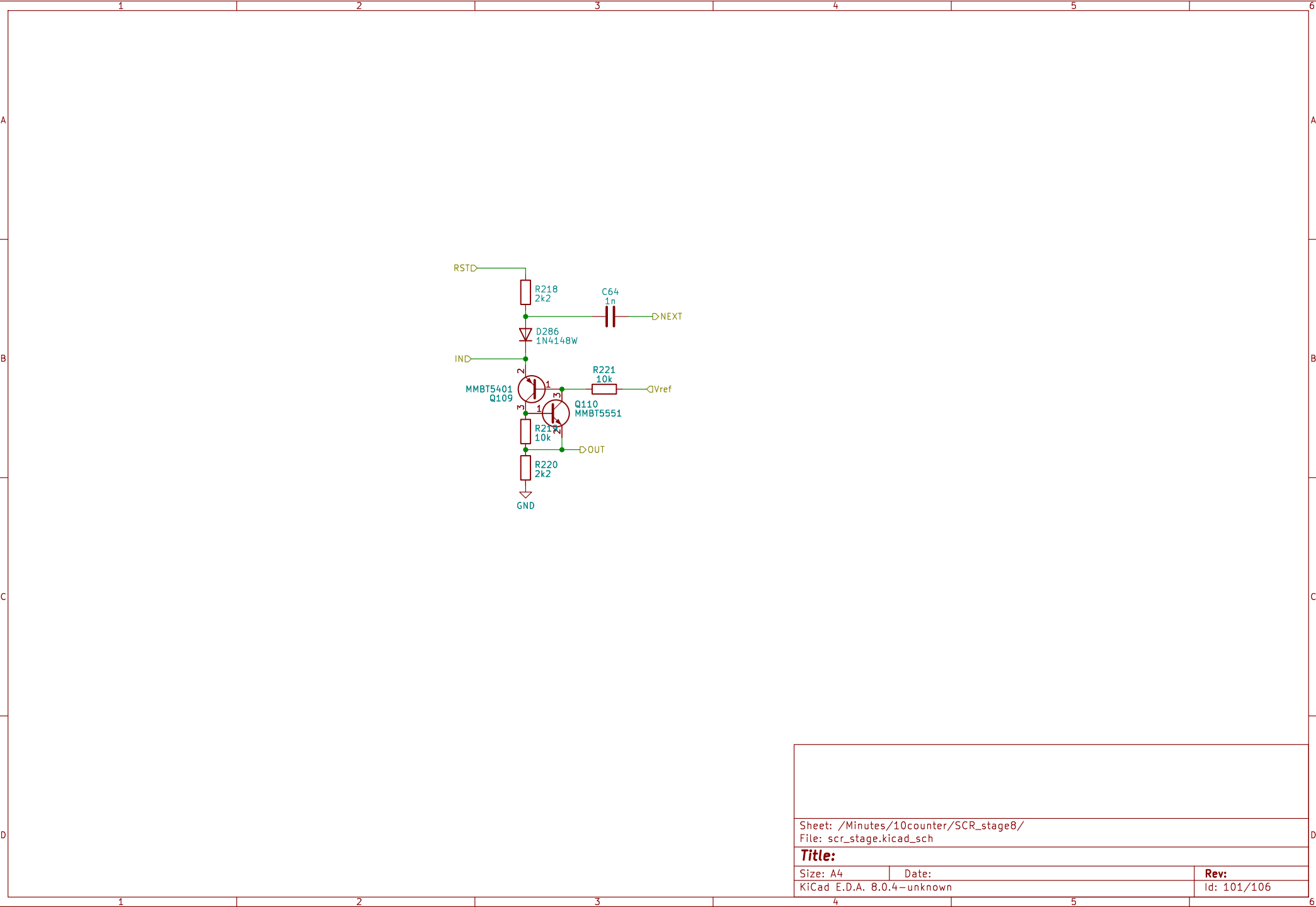








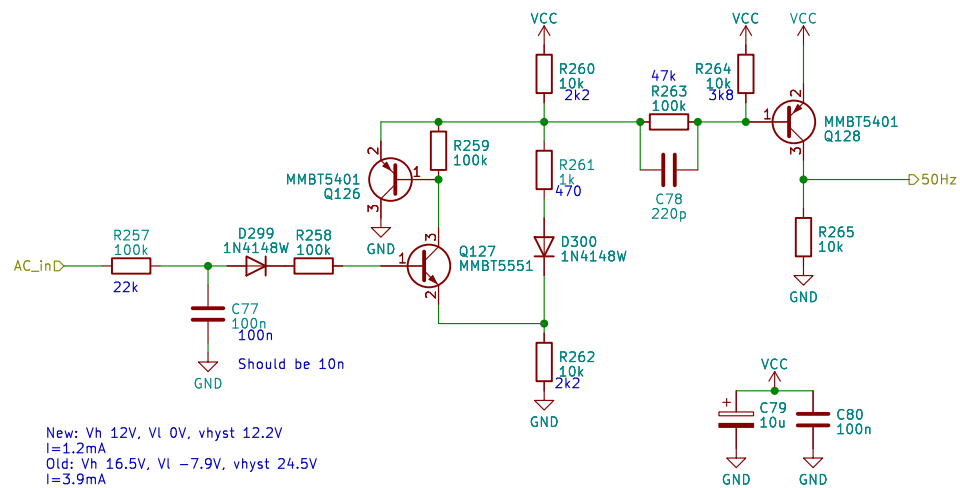












Xavier Bourlot

Sheet: /Sync gen/

File: sync.kicad\_sch

**Title: Transistor clock**

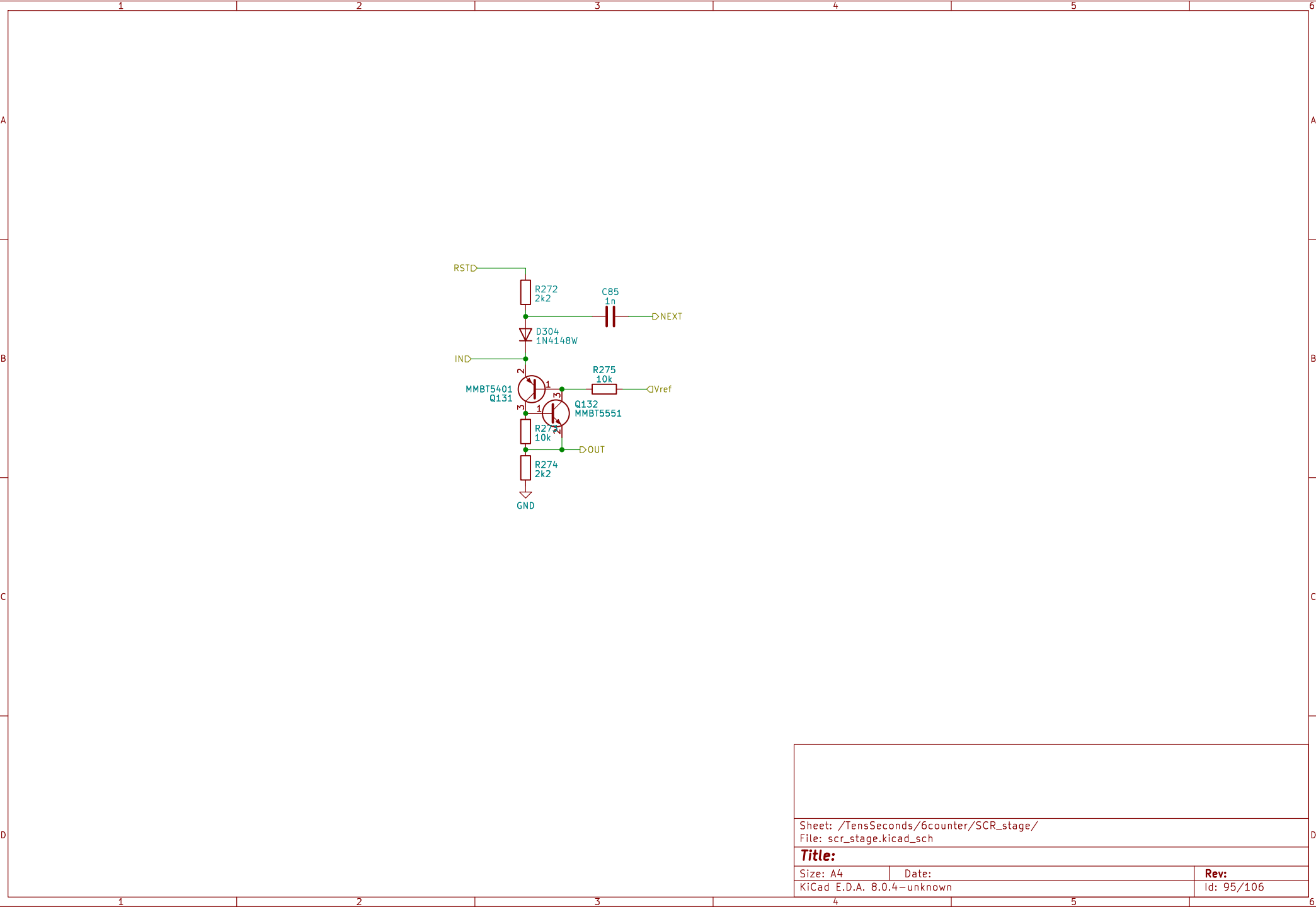
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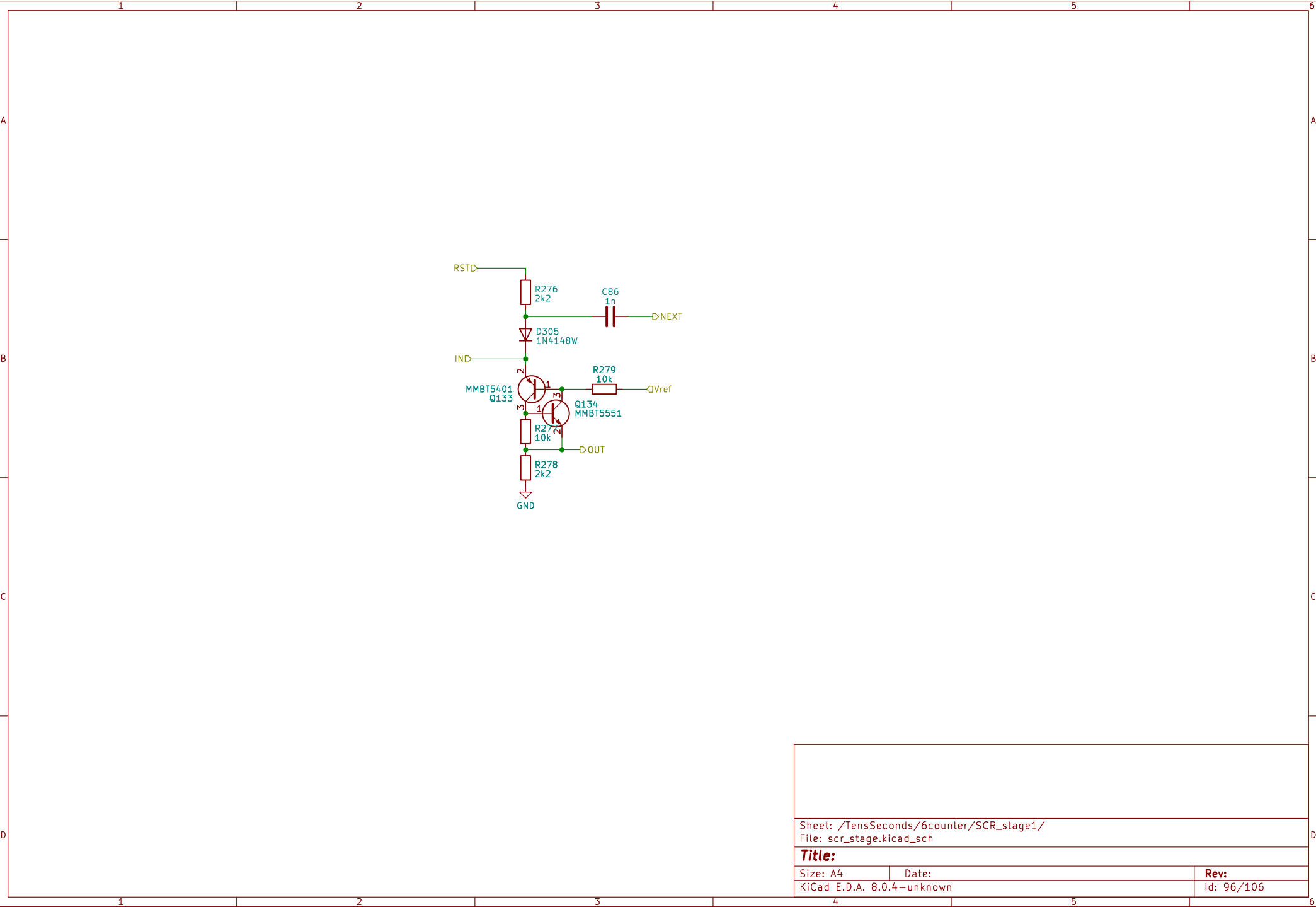
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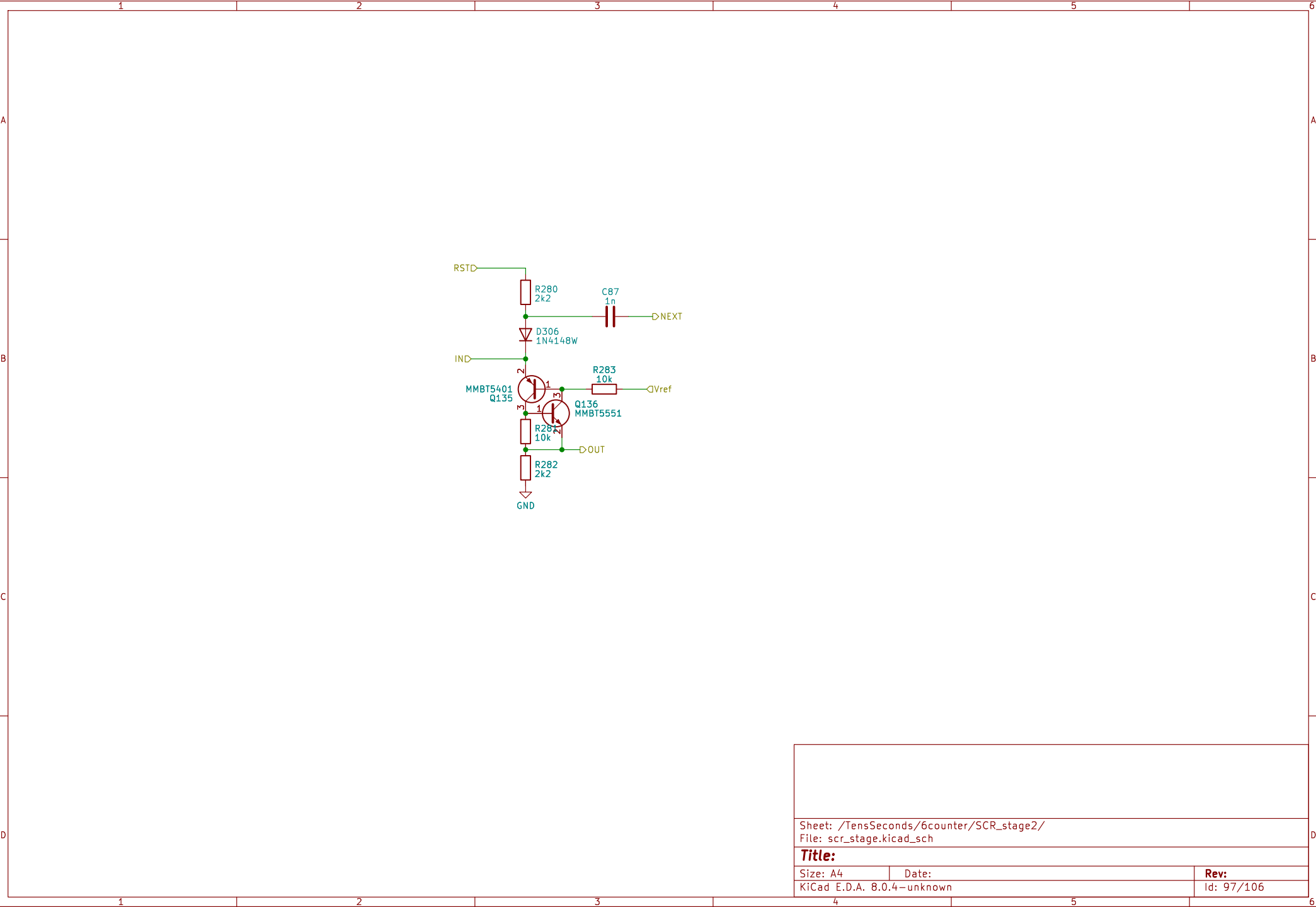
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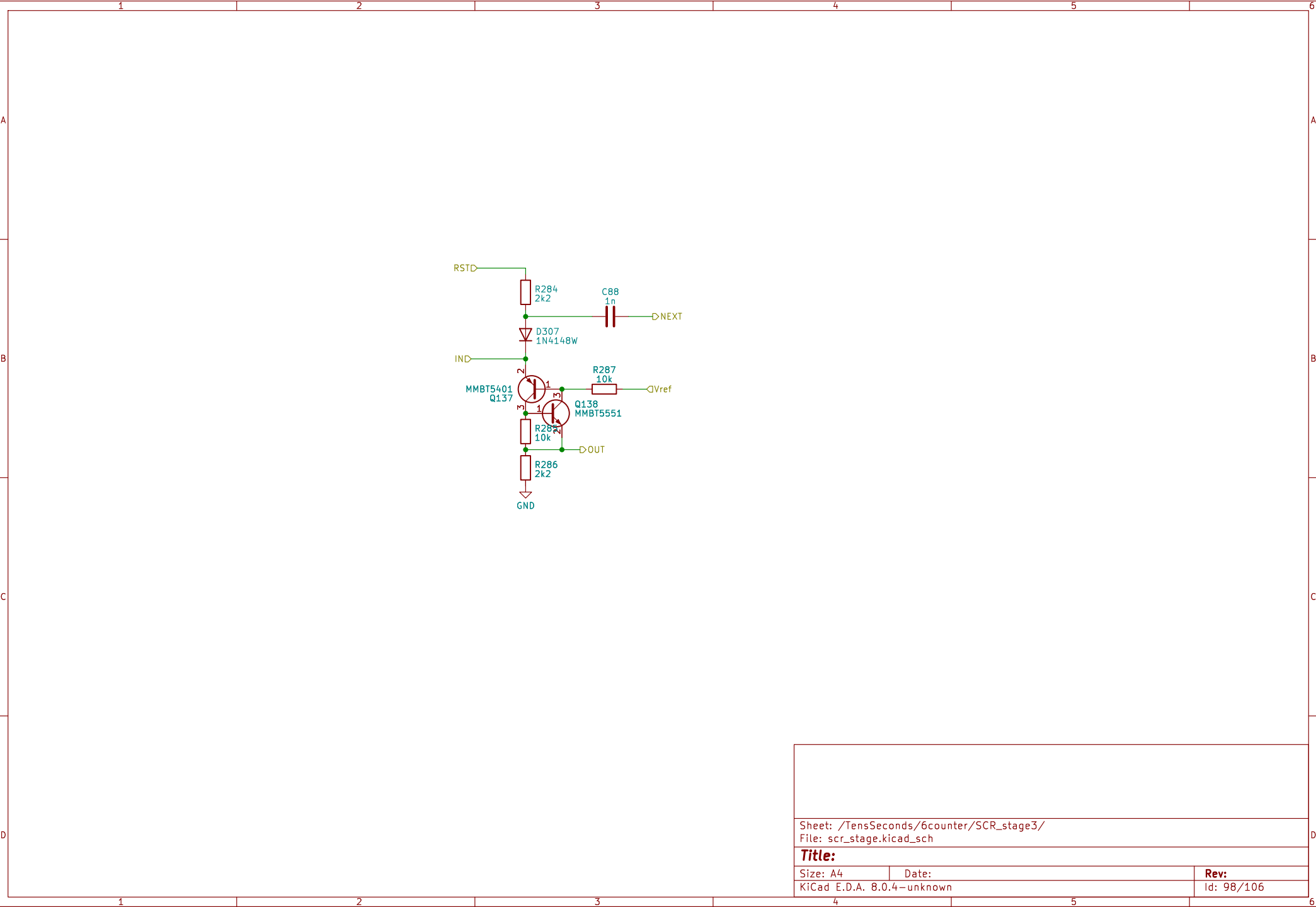
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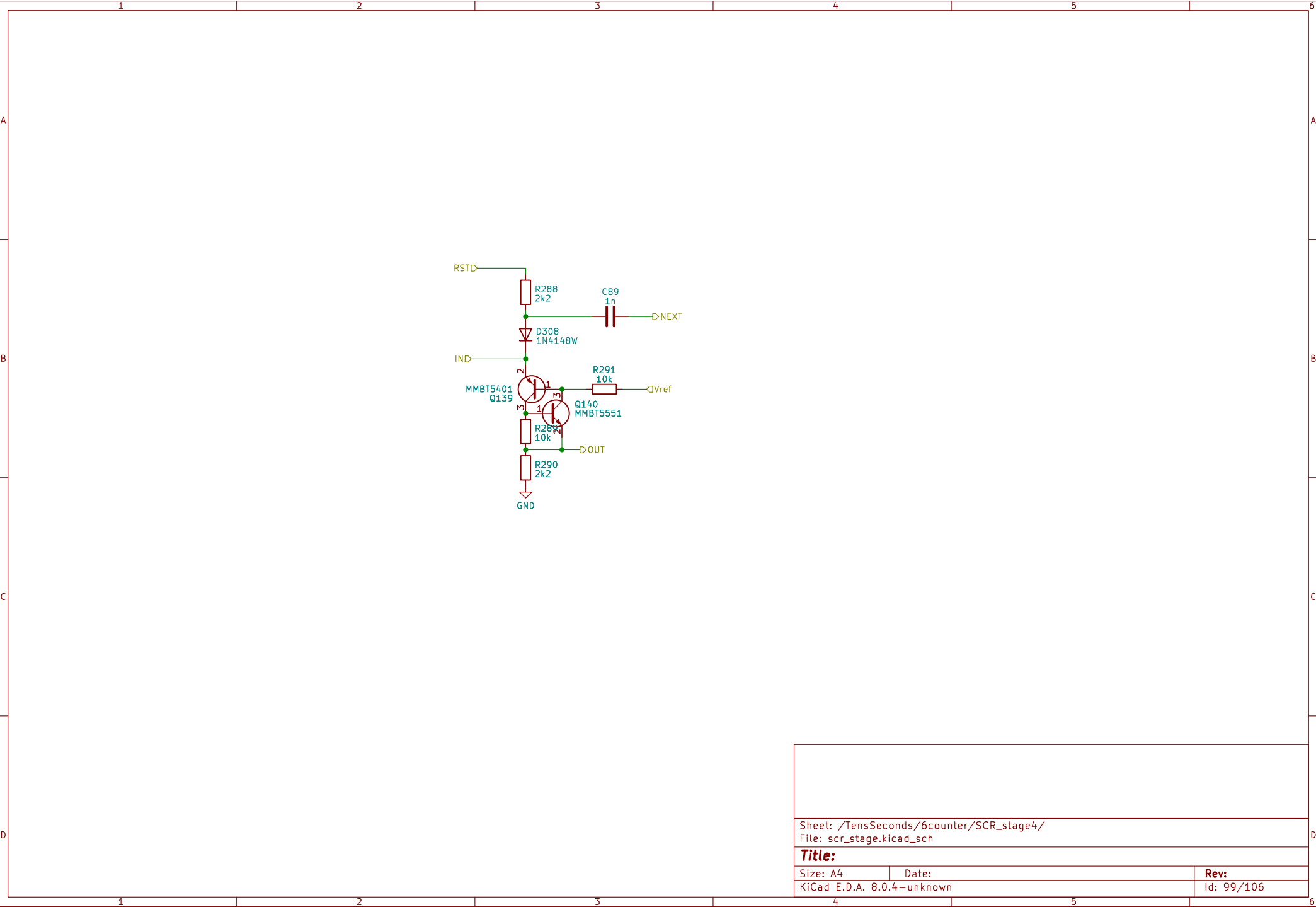




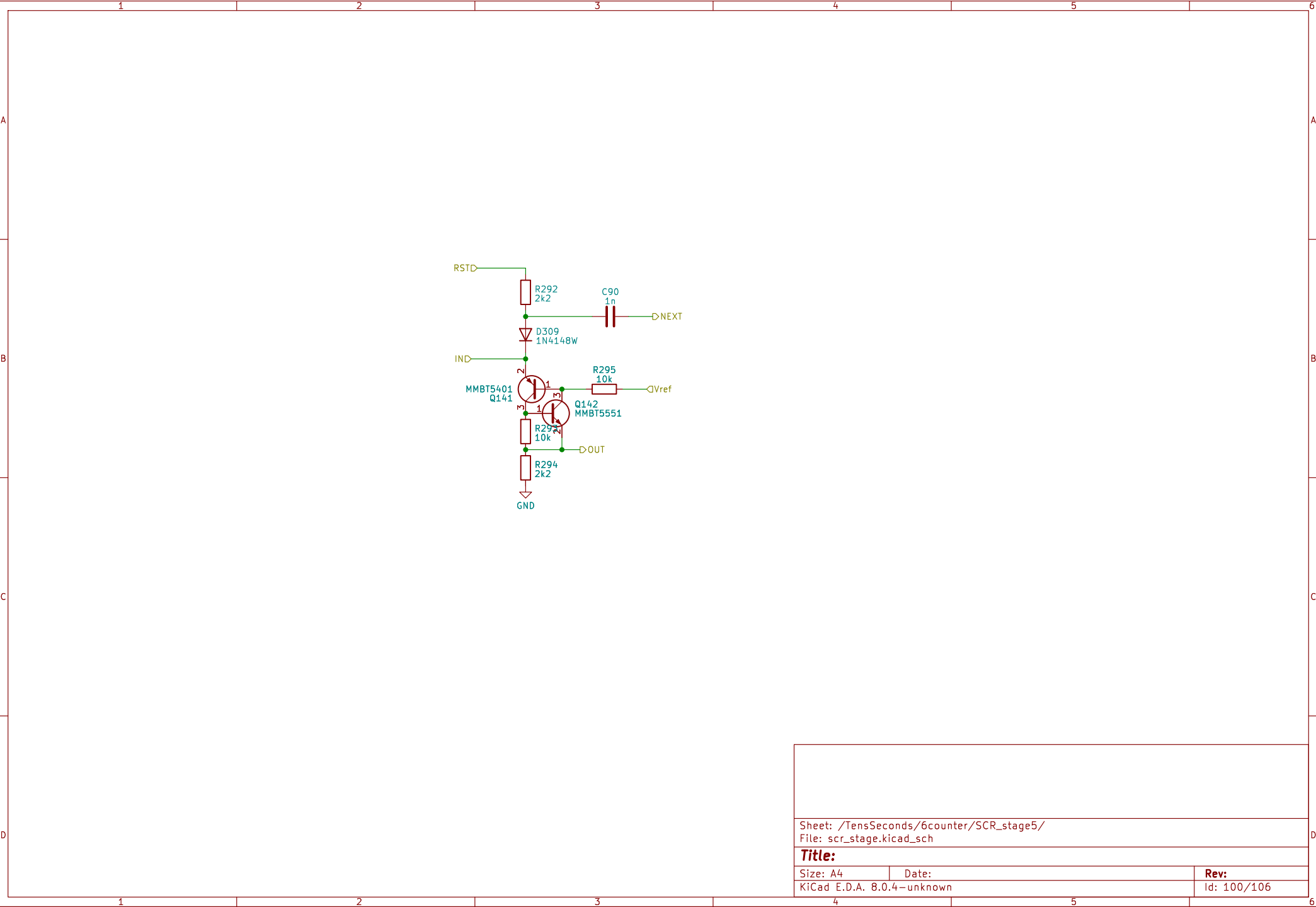








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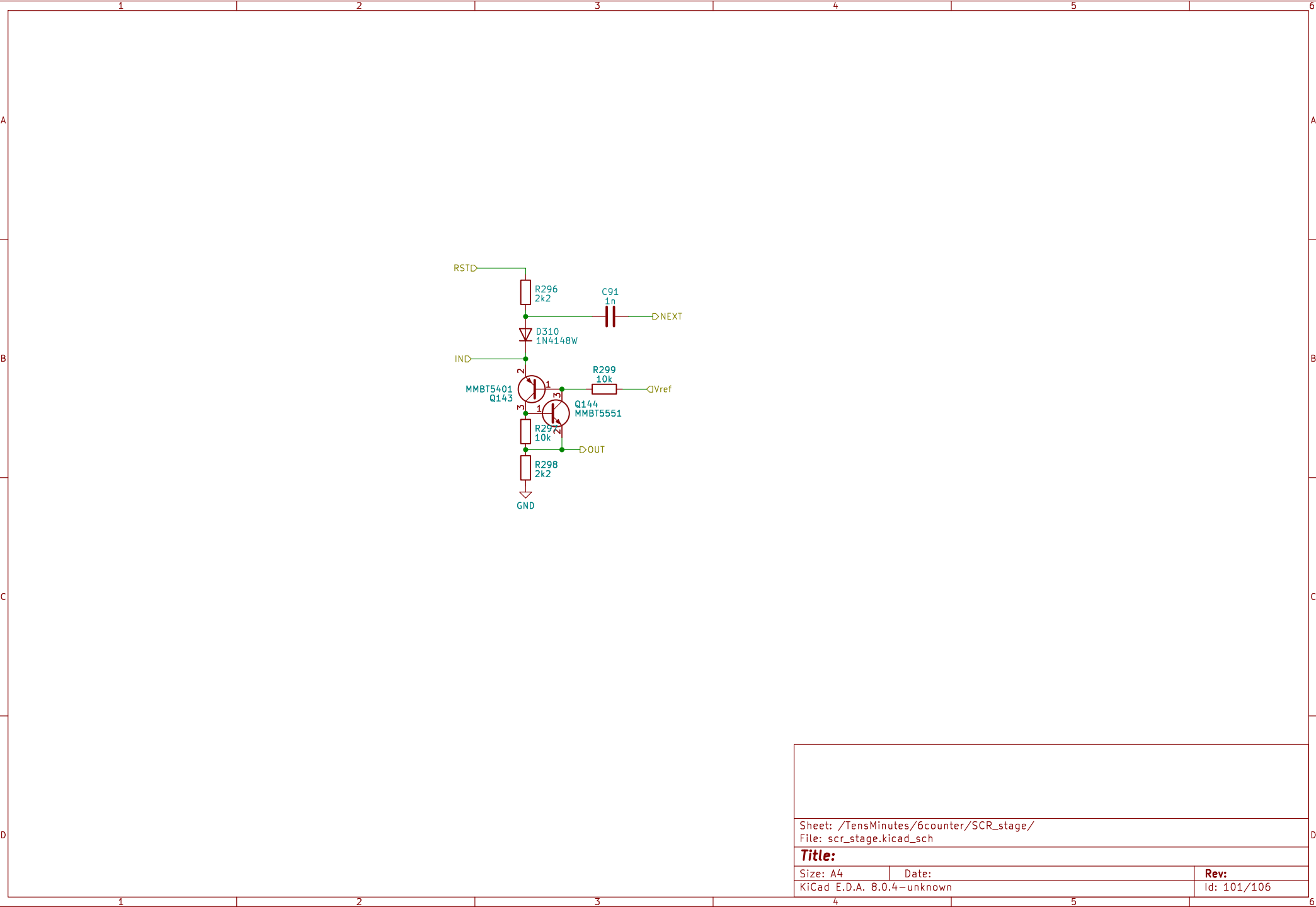
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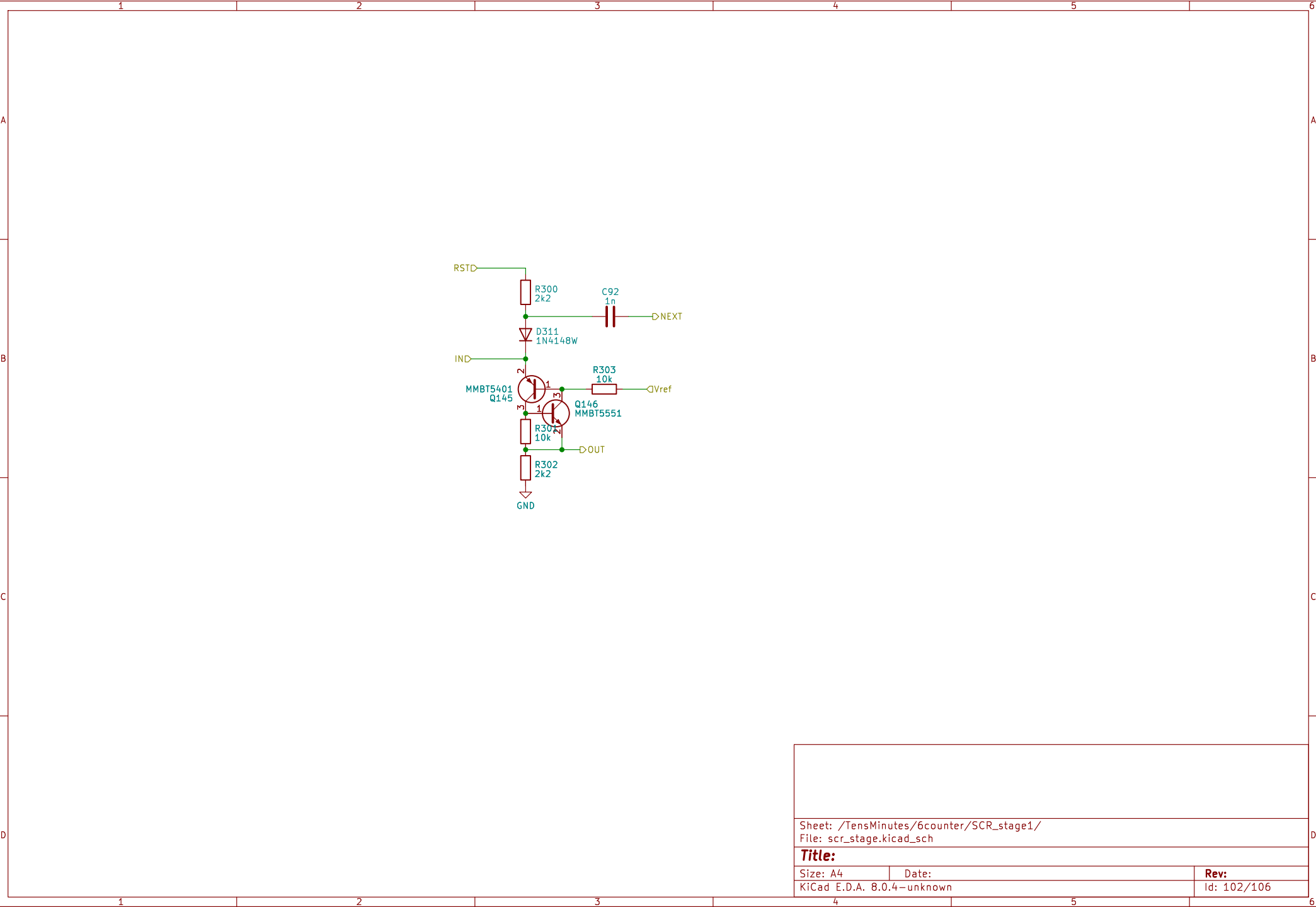
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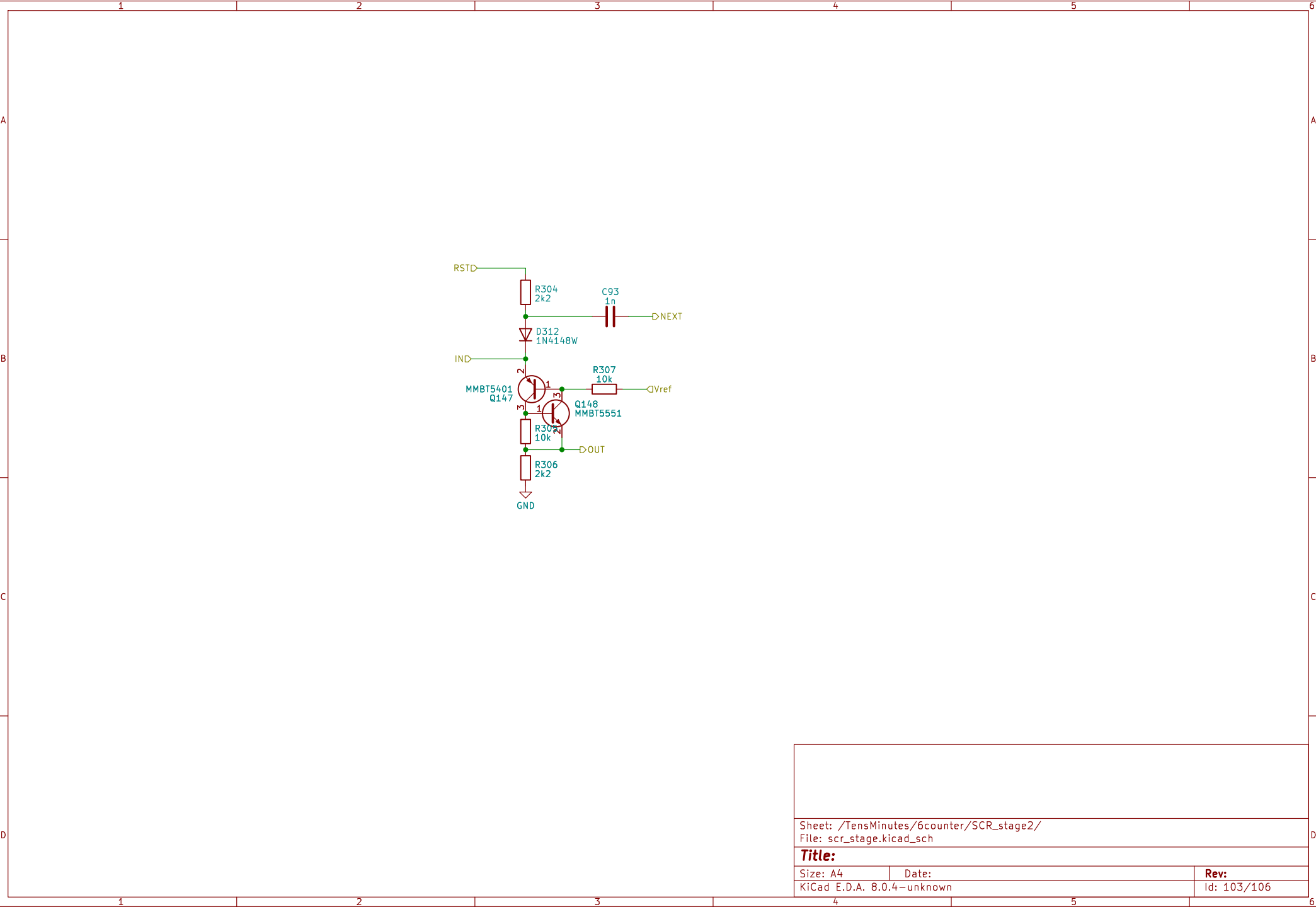
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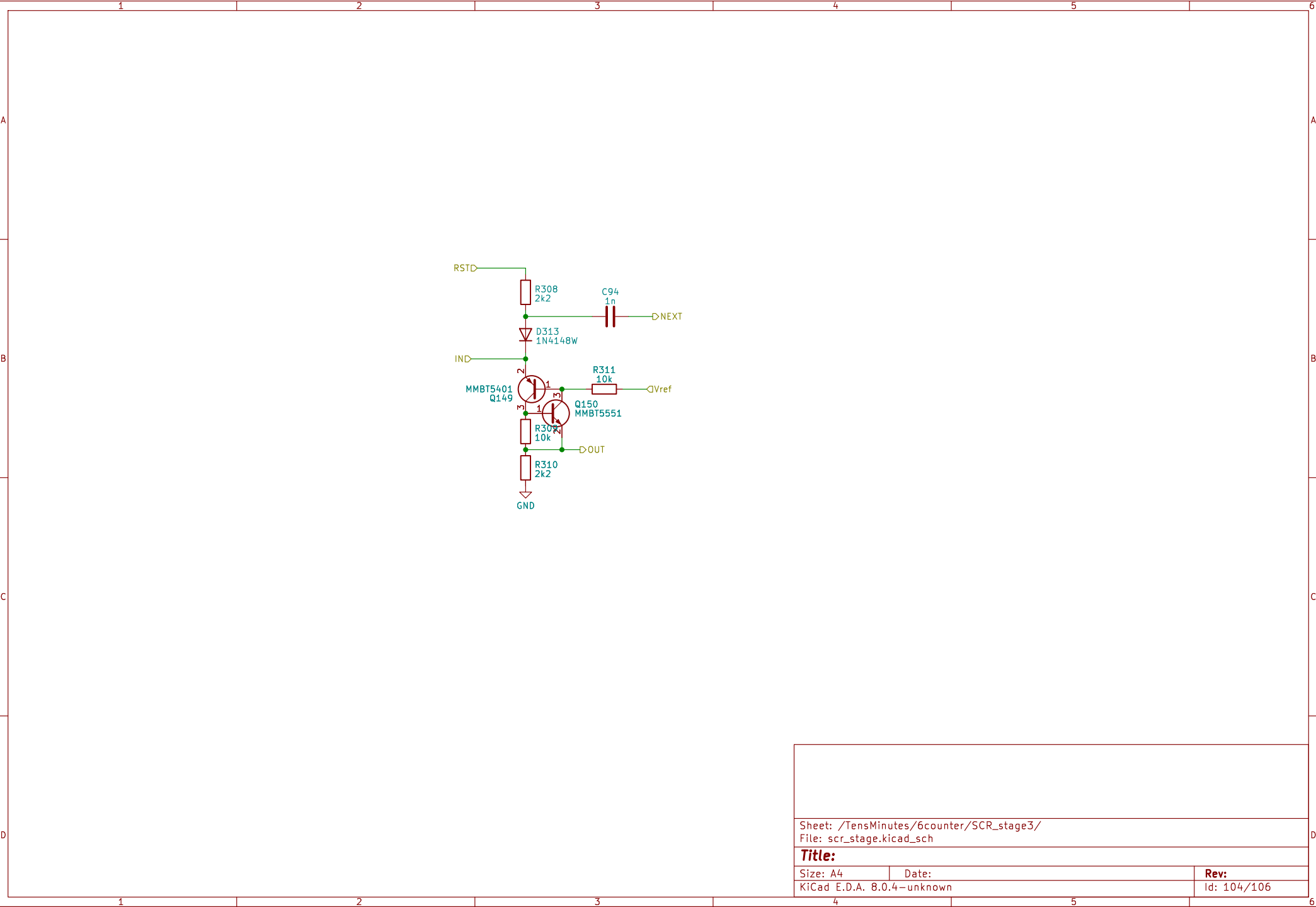
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Id: 100/106

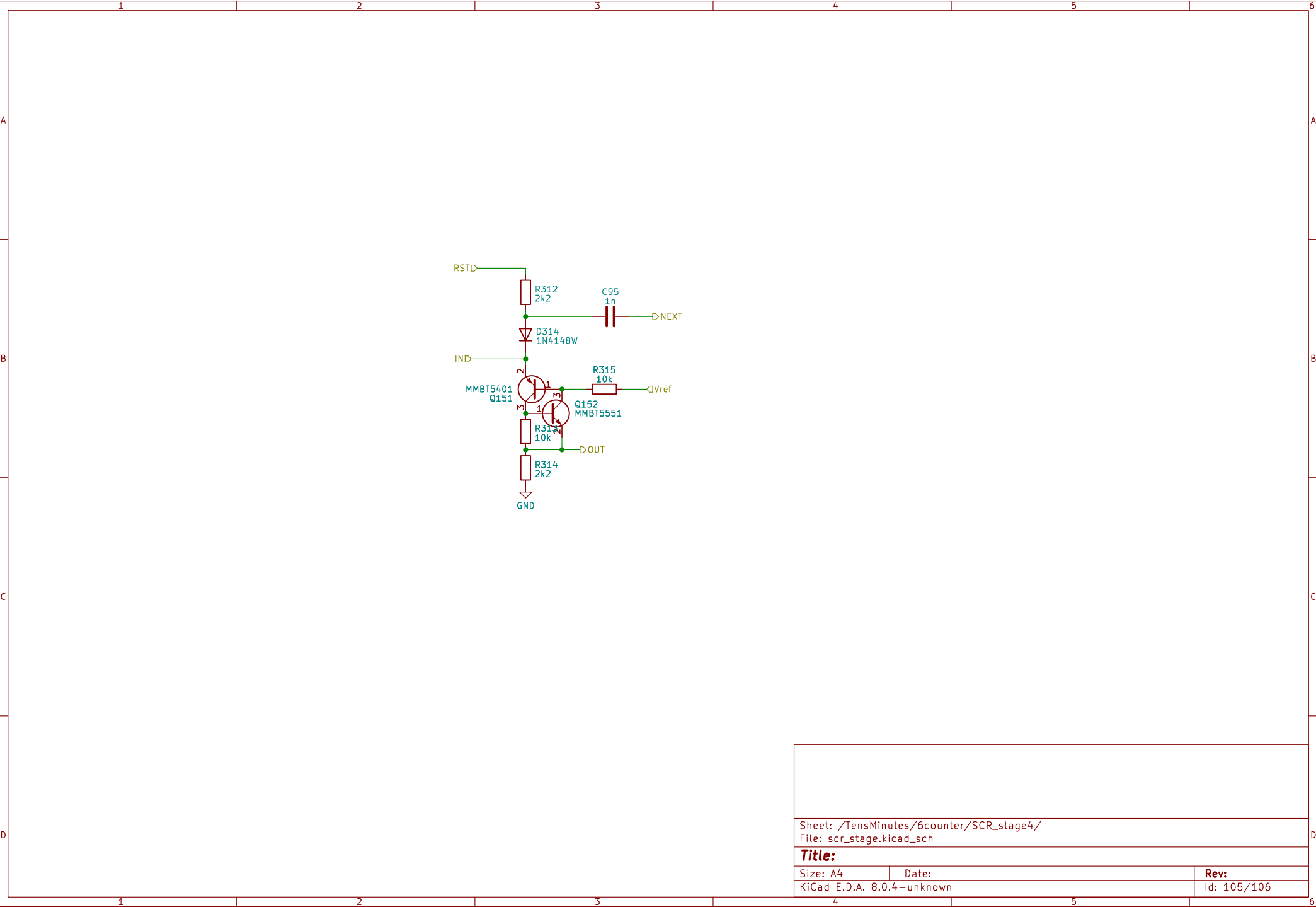












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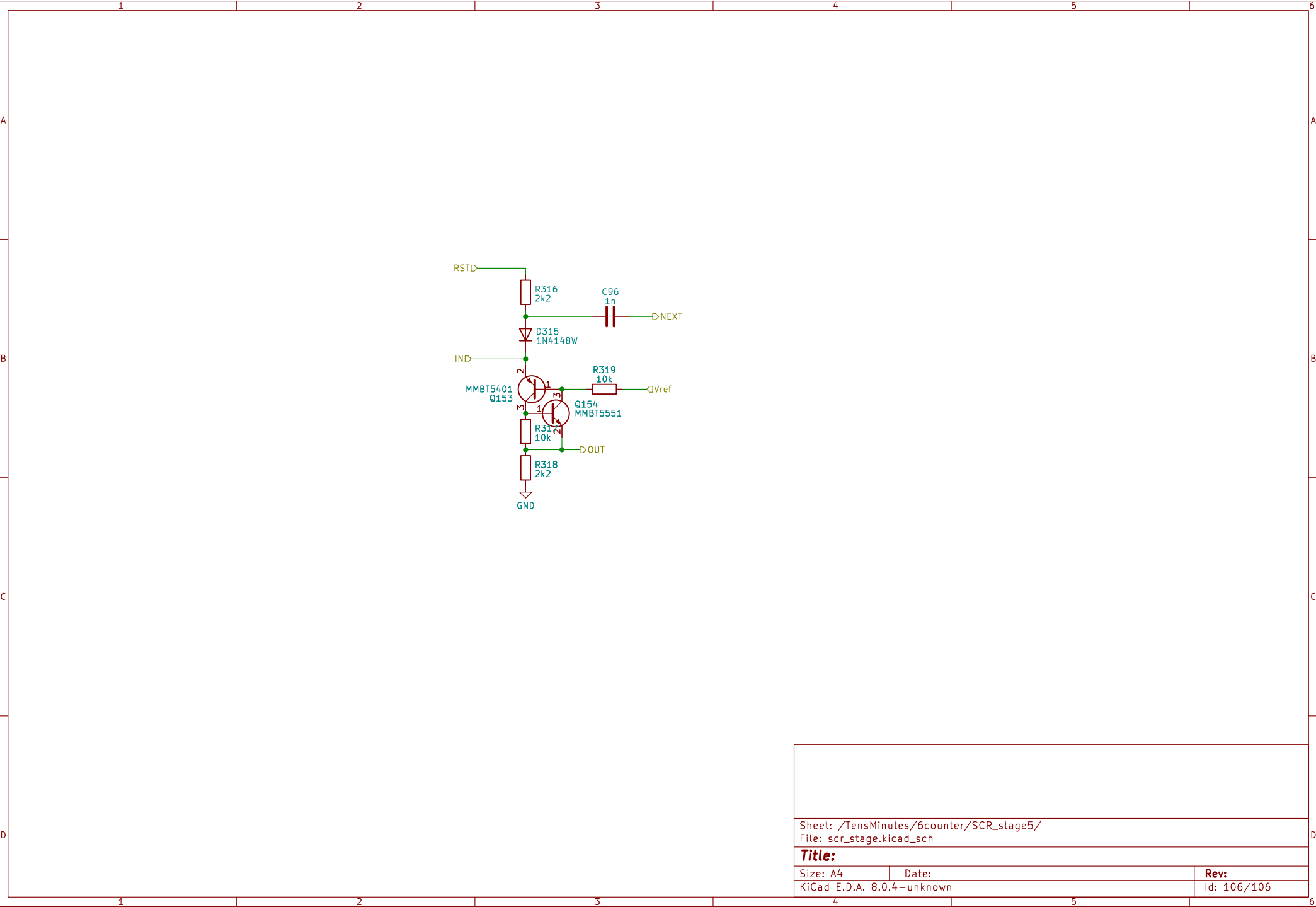
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Id: 105/106



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