Mid-Semester Examination

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Subject: Microprocessors & Microcontrollers

Subject Code: EC-302

Answer to Q. NO: 2

(a)

$$A = 0011\ 0011$$
$$+B = 0111\ 1000$$
$$\overline{1010\ 1011}$$

$$CMA = 0101\ 0100$$

$$ANI = 0011\ 0010$$
$$\overline{0001\ 0000}$$

∴ The accumulator value will be 10 H //

(d) The period of the squar wave is 2 ms.
Thus, the pulse should be in logic 1 for 1 ms and the pulse should be in logic 0 for 1 ms.
The alternate pattern can be generated by loading the accumulator with AA H (10101010)

Program:

```
        MVI  D, AA
ROTATE: MOV  A, D
        RLC
        MOV  D, A
        ANI  01 H
        OUT  PORT1
        MVI  B, COUNT
```

```
DELAY : DCR B
        JNZ DELAY
        JMP ROTATE
```

Now,

System clock period is 325 ns.

Delay outside the Loop : $T_0$ = 46 T-states × 325 ns

= 14.95 µs

Loop Delay : $T_L$ = 14 T-states × 325 ns × (COUNT − 1) + 11 T-states × 325 ns

= 4.5 µs (COUNT − 1) + 3.575 µs

Total delay required = 1 ms

$\therefore T_D = T_0 + T_L$

$\Rightarrow 1 \text{ ms} = [14.95 + 3.575 + 4.5(\text{COUNT}-1)]\ \mu s$

$\Rightarrow 1000 \times 10^{-6} = 18.525 \times 10^{-6} + 4.5 \times 10^{-6}(\text{COUNT}-1)$

$\Rightarrow \frac{981.475 \times 10^{-6}}{4.5 \times 10^{-6}} = \text{COUNT} - 1$

$\Rightarrow 218.10 = \text{COUNT} - 1$

$\Rightarrow \text{COUNT} = 219.10$

$\Rightarrow \text{COUNT} = \text{DB H}$

Answer to Q. No: 3

(a) Difference between Microprocessor and Microcontroller are:

| Microprocessor | Microcontroller |
|---|---|
| (i) Microprocessor consists only of Central Processing Unit | (i) Microcontroller consist of CPU, memory, I/O all integrated into one chip. |
| (ii) Microprocessors are based on von Neumann Model. | (ii) Microcontrollers are based on Havard Architecture. |

(b) The various registers in 8085 are B, C, D, E, H, L

(c) Address bus and data bus are provided with tri state buffers as they allow multiple logic devices to be connected to the same bus without damage or loss of data.

(d) The DAD function add the 16-bits content of a specified register pair to the contents of the HL register pair and stores the sum in HL register. If the result is larger than 16 bits, then only the CY (Carry Flag) is set. No other flags are affected.

Answer to Q.No: 1

(b) SP and PC are 16 bit registers because they contain the memory addresses which are generally 16-bit addresses.

(c) In a 4096 × 8 EPROM chip, the number of address lines are: $\log_2 4096$

$= \log_2 2^{12}$

$= 12 \log_2 2$

$= 12$ //

(d) In a 8K byte ROM, there are 8192 registers

Thus, 13 address lines.

| $A_{15}$ | $A_{14}$ | $A_{13}$ | $A_{12}$ | $A_{11}$ | $A_{10}$ | $A_9$ | $A_8$ | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $= (1000)_H$ |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | $= (2FFF)_H$ |

$\therefore$ $A_{15}$ $A_{14}$ $A_{13}$ $A_{12}$

0 0 0 1

0 0 1 0

As $\overline{CS}$ should be low,

Logic expression is given by: $A_{15} + A_{14} + (A_{13} \cdot A_{12} + \bar{A}_{13} \cdot \bar{A}$

(a) The difference between fetch cycle and read cycle are:

In fetch cycle, the microprocessor fetches the instructions from main memory & executes them. It uses 3 T-states to fetch opcode and 1 T-state to execute them.

In read cycle, the microprocessor initializes a read bus by providing address of memory location. It uses only 3 T-states.

Answer to Q.No: 2

(b)

```
MVI   A, DATA    // DATA = 92 H
ORA   A
                 // OR A with itself
```

It will result in the same number A As accumulator does not contain zero, JP will not execute.

```
XRA   A    // XORing A with A
```

It will result in 0 in accumulator.

```
OUTPRT: OUT F2H
```

∴ Output at port F2H is 00H