Mid-Semester Examination Name: Rekhar Das Scholar ID: 1914048 Sec: A Department: ECE Subject: Microprocessors & Nicrocombrollers Subject code: EC-302 ZIATON MAGNA Ammer to Q. NO: 2 (0) A = 0011001100 Western Wall western 10101011 M 3 F3 & DO O LA CO D O 3 5 7 5 MA :. The accumulator value will be 10 Help lotal (d) The period of the squar wave is 2 ms. Thus, the pulse should be in logic I too I ms and the pulse should be in logic 0 for I ms. The alternate pattern can be generated by loading the accumulator with AAH (10101010) 1-1400) = 100NI-1 Program: U D, AA1 - TUODO = 01.815 + MVI ROTATE: NOV A, D RLC MON DIA H 84 THOOD ANI DIH OUT PORTS MVI B, COUNT

123 transparate DELAY . TO DCR BIOL AL xolores and worked to the downwest votabust - bu JNZ DELAY IN I WORK 1989 MIN JMP ROTATE - SEET-ALT MERE POPULA or single of real Now, System clock period is 325 ms. Delay outside the Loop : To 3 46 T7 states x 325 ns 1103 14.95,48 Loop Delay . Te > 14 Totales x 325 MAX (COUNT-1) + 11 T-States X 325 ms LMA = 4.5 US (COUNT-1) 43.575 MA Total delay required = alons 1. The state sound soups ent to borney ent > 1 ms = [14.95 + 3.575 + 4.5 (COUNT-1)] us \$1000 x10 = 18.525 x10 4 4 5 x10 (COUNT-1) (0101010 3) 981 475 ×10 6 > COUNT-1 1 80 gram \$ 218.10 = COUNT-IAA A WM * COUNT = 219.10 ",A VOM MOTATES 014 > COUNT = ABH A Q WOM 17909 100 THUOD & IVM

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(a) Difference between Microprocessor and Microcomtroller are notion established promoun ent motion ment

Wicroprocessor

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(i) Microprocessor comists only (i) Microcontroller comsist of of central Processing Unit

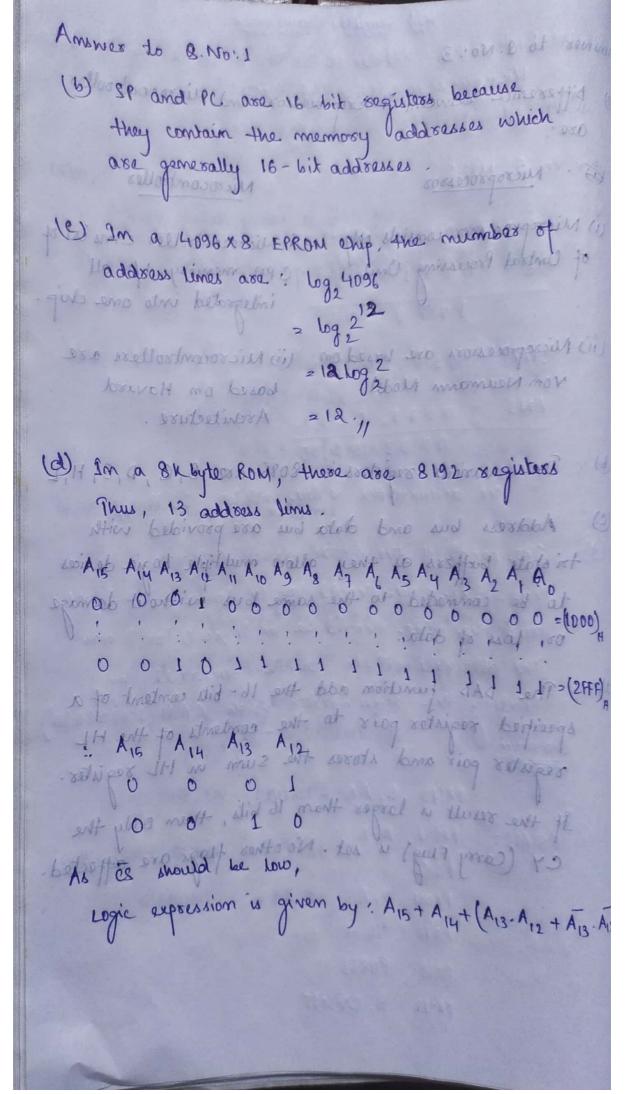
integrated into one chip.

(11) Nicsoprocessors are based on (ii) Nicrocontrollers are Von Noumann Model

based on Havard Architecture.

- (b) The various registers in 8085 are B, C, D, E, H, D
- Address bus and data bus are provided with to state buffers as they allow multiple hogic devices to be commeded to the same bus without damage or low of data.
- (d) The DAD function add the 16-bits content of a specified register pair to the contents of the HL register pair and stores the sum in It's register. If the result is larger than 16 bits, then only the CY (Carry Flag) is set. No other flags are affected.

LOgic expression is given by Alba All (13. Ara + Ala. Ar



(a) The difference between jetch cycle and read cycle are:

In Jetch cycle, the microprocessor Jetches the instructions Joom main memory & executes them. It of uses 3 T-states to Jetch opcode and 1 T-state to execute them.

In read cycle, the microprocessor initializes a read bus by providing address of memory bowhom. It uses only 3 T-states.

Answer to g. No: 2

ORA A // DR A with itself

It will seall in the same number A As accumulator does not contain zero, JP will not execute.

2t will result in 0 in accumulator.

OUTPRT: OUT F2H

:. Output at post FZH is OOH