Section 24 CANFD Interface (RS-CANFD)

This section contains a generic description of the CAN Interface (RS-CANFD).

The first part of this section describes the features specific to RH850/F1KH, RH850/F1KM, such as the number of units, register base addresses, etc.

The remainder of the section describes the functions and registers of RS-CANFD.

24.1 Features of RH850/F1KH, RH850/F1KM RS-CANFD

24.1.1 Number of Units and Channels

This microcontroller has the following number of RS-CANFD units and channels.

Table 24.1 Number of Units (RH850/F1KH-D8)

Product Name	RH850/F1KH-D8 176 Pins	RH850/F1KH-D8 233 Pins	RH850/F1KH-D8 324 Pins
Number of Units	1	1	2
Name	RCFDCn (n = 0)	RCFDCn (n = 0)	RCFDCn (n = 0, 1)

Table 24.2 Number of Units (RH850/F1KM-S4)

Product Name	RH850/F1KM-S4 100 Pins	RH850/F1KM-S4 144 Pins	RH850/F1KM-S4 176 Pins	RH850/F1KM-S4 233 Pins	RH850/F1KM-S4 272 Pins
Number of Units	1	1	1	1	1
Name	RCFDCn (n = 0)	RCFDCn (n = 0)	RCFDCn (n = 0)	RCFDCn (n = 0)	RCFDCn (n = 0)

Table 24.3 Number of Units (RH850/F1KM-S2)

Product Name	RH850/F1KM-S2 100 Pins	RH850/F1KM-S2 144 Pins	RH850/F1KM-S2 176 Pins
Number of Units	1	1	1
Name	RCFDCn (n = 0)	RCFDCn (n = 0)	RCFDCn (n = 0)

Table 24.4 Number of Units (RH850/F1KM-S1)

Product Name	RH850/F1KM-S1 48 Pins	RH850/F1KM-S1 64 Pins	RH850/F1KM-S1 80 Pins	RH850/F1KM-S1 100 Pins
Number of Units	1	1	1	1
Name	RCFDCn (n = 0)	RCFDCn (n = 0)	RCFDCn (n = 0)	RCFDCn (n = 0)

Table 24.5 Unit Configurations and Channels (RH850/F1KH-D8)

Unit Name RCFDCn	Unit Channel Total Number z	Channel Name CANm	RH850/F1KH-D8 176 Pins (8ch)	RH850/F1KH-D8 233 Pins (8ch)	RH850/F1KH-D8 324 Pins (12ch)
RCFDC0	0	CAN0	✓	✓	✓
	1	CAN1	✓	✓	✓
	2	CAN2	✓	✓	✓
	3	CAN3	✓	✓	✓
	4	CAN4	✓	✓	✓
	5	CAN5	✓	✓	✓
	6	CAN6	✓	✓	✓
	7	CAN7	✓	✓	✓
RCFDC1	8	CAN0	—	—	✓
	9	CAN1	—	—	✓
	10	CAN2	—	—	✓
	11	CAN3	—	—	✓

Table 24.6 Unit Configurations and Channels (RH850/F1KM-S4)

Unit Name RCFDCn	Unit Channel Total Number z	Channel Name CANm	RH850/F1KM-S4 100 Pins (8ch)	RH850/F1KM-S4 144 Pins (8ch)	RH850/F1KM-S4 176 Pins (8ch)	RH850/F1KM-S4 233 Pins (8ch)	RH850/F1KM-S4 272 Pins (8ch)
RCFDC0	0	CAN0	✓	✓	✓	✓	✓
	1	CAN1	✓	✓	✓	✓	✓
	2	CAN2	✓	✓	✓	✓	✓
	3	CAN3	✓	✓	✓	✓	✓
	4	CAN4	✓	✓	✓	✓	✓
	5	CAN5	✓	✓	✓	✓	✓
	6	CAN6	✓	✓	✓	✓	✓
	7	CAN7	✓	✓	✓	✓	✓

Table 24.7 Unit Configurations and Channels (RH850/F1KM-S2)

Unit Name RCFDCn	Unit Channel Total Number z	Channel Name CANm	RH850/F1KM-S2 100 Pins (8ch)	RH850/F1KM-S2 144 Pins (8ch)	RH850/F1KM-S2 176 Pins (8ch)
RCFDC0	0	CAN0	✓	✓	✓
	1	CAN1	✓	✓	✓
	2	CAN2	✓	✓	✓
	3	CAN3	✓	✓	✓
	4	CAN4	✓	✓	✓
	5	CAN5	✓	✓	✓
	6	CAN6	✓	✓	✓
	7	CAN7	✓	✓	✓

Table 24.8 Unit Configurations and Channels (RH850/F1KM-S1)

Unit Name RCFDCn	Unit Channel Total Number z	Channel Name CANm	RH850/F1KM-S1 48 Pins (1ch)	RH850/F1KM-S1 64 Pins (3ch)	RH850/F1KM-S1 80 Pins (3ch)	RH850/F1KM-S1 100 Pins (6ch)
RCFDC0	0	CAN0	✓	✓	✓	✓
	1	CAN1	—	✓	✓	✓
	2	CAN2	—	✓	✓	✓
	3	CAN3	—	—	—	✓
	4	CAN4	—	—	—	✓
	5	CAN5	—	—	—	✓

Table 24.9 Indices (RH850/F1KH-D8)

Index	Description
n	Throughout this section, the individual RS-CANFD units are generically indicated by the index “n”; for example, RCFDCnCFDGCTR is the global control register of the RCFDCn unit (n = 0, 1).
m	Throughout this section, the individual channels of RS-CANFD units are generically indicated by the index “m”; for example, RCFDCnCFDCmSTS is the channel m status register (m = 0 to 7 with n = 0, or m = 0 to 3 with n = 1).
z	Throughout this section, the total number of channels of RS-CANFD units is generically indicated by the index “z” (z = 0 to 11).
j	The individual registers associated with receive rule table are generically indicated by the index “j”; for example, RCFDCnCFDGAFLIDj (j = 0 to 15 with both value of index “n” (n = 0, 1)) is the receive rule ID register.
k	The individual transmit/receive FIFO buffers are generically indicated by the index “k”; for example, RCFDCnCFDCFCCk (k = 0 to [channel m × 3 + 2] with both value of index “n” (n = 0, 1)) is the transmit/receive FIFO buffer configuration/control register.
x	The individual receive FIFO buffers are generically identified by the index “x”; for example, RCFDCnCFDRFSTSx (x = 0 to 7 with both value of index “n” (n = 0, 1)) is the receive FIFO buffer status register.
d	Data field registers of transmit/receive FIFO buffers and receive FIFO buffers are identified by “d”; for example, the transmit/receive FIFO buffer data field register is described as RCFDCnCFDCFDFd_k (d = 0 to 15).
q	The individual receive buffers are generically indicated by the index “q”; for example, RCFDCnCFDRMIDq (q = 0 to [channel m × 16 + 15] with both value of index “n” (n = 0, 1)) is the receive buffer ID register.
p	The individual transmit buffers are generically indicated by the index “p”; for example, RCFDCnCFDTMCp (p = 0 to [channel m × 32 + 31] with both value of index “n” (n = 0, 1)) is the transmit buffer control register.
b	Data field registers of receive buffers and transmit buffers are identified by “b”; for example, the receive buffer data field register is described as RCFDCnCFDRMDFb_q (b = 0 to 15 with both value of index “n” (n = 0, 1)).
r	The individual RAM tests for CAN are generically indicated by the index “r”; for example, RCFDCnCFDRPGACCr (r = 0 to 63 with both value of index “n” (n = 0, 1)) is the RAM test page access register.
y	The registers not covered above are indicated by the index “y”; for example, RCFDCnCFDRMNDy (y = 0 to 3 with n = 0 or (y= 0, 1)) with n = 1 is a receive buffer new data register.

Note: The functions and descriptions of registers in this section are for the RS-CANFDn that has 8 channels (m = 0 to 7) for unit 0 (n = 0) and 4 channels (m = 0 to 3) for unit 1 (n = 1). When referring to information with indices, regard the index values as the ones corresponding to your target product. Also, note that, if the value of an index exceeds the range described in this section due to your target product, write the value after reset when writing to bits outside the index range.

Table 24.10 Indices (RH850/F1KM-S4, RH850/F1KM-S2)

Index	Description
n	Throughout this section, the individual RS-CANFD units are generically indicated by the index “n”; for example, RCFDCnCFDGCTR is the global control register of the RCFDCn unit (n = 0).
m	Throughout this section, the individual channels of RS-CANFD units are generically indicated by the index “m”; for example, RCFDCnCFDCmSTS is the channel m status register (m = 0 to 7).
z	Throughout this section, the total number of channels of RS-CANFD units is generically indicated by the index “z” (z = 0 to 7).
j	The individual registers associated with receive rule table are generically indicated by the index “j”; for example, RCFDCnCFDGAFLIDj (j = 0 to 15) is the receive rule ID register.
k	The individual transmit/receive FIFO buffers are generically indicated by the index “k”; for example, RCFDCnCFDCFCCk (k = 0 to [channel m × 3 + 2]) is the transmit/receive FIFO buffer configuration/control register.
x	The individual receive FIFO buffers are generically identified by the index “x”; for example, RCFDCnCFDRFSTSx (x = 0 to 7) is the receive FIFO buffer status register.
d	Data field registers of transmit/receive FIFO buffers and receive FIFO buffers are identified by “d”; for example, the transmit/receive FIFO buffer data field register is described as RCFDCnCFDCFDFd_k (d = 0 to 15).
q	The individual receive buffers are generically indicated by the index “q”; for example, RCFDCnCFDRMIDq (q = 0 to [channel m × 16 + 15]) is the receive buffer ID register.
p	The individual transmit buffers are generically indicated by the index “p”; for example, RCFDCnCFDTMCp (p = 0 to [channel m × 32 + 31]) is the transmit buffer control register.
b	Data field registers of receive buffers and transmit buffers are identified by “b”; for example, the receive buffer data field register is described as RCFDCnCFDRMDFb_q (b = 0 to 15).
r	The individual RAM tests for CAN are generically indicated by the index “r”; for example, RCFDCnCFDRPGACCr (r = 0 to 63) is the RAM test page access register.
y	The registers not covered above are indicated by the index “y”; for example, RCFDCnCFDRMNDy (y = 0 to 3 with n = 0, or y= 0, 1 with n = 1) is a receive buffer new data register.

Note: The functions and descriptions of registers in this section are for the RS-CANFD that has 8 channels (m = 0 to 7). When referring to information with indices, regard the index values as the ones corresponding to your target product. Also, note that, if the value of an index exceeds the range described in this section due to your target product, write the value after reset when writing to bits outside the index range.

Table 24.11 Indices (RH850/F1KM-S1)

Index	Description
n	Throughout this section, the individual RS-CANFD units are generically indicated by the index “n”; for example, RCFDCnCFDGCTR is the global control register of the RCFDCn unit (n = 0).
m	Throughout this section, the individual channels of RS-CANFD units are generically indicated by the index “m”; for example, RCFDCnCFDCmSTS is the channel m status register (m = 0 to 5).
z	Throughout this section, the total number of channels of RS-CANFD units is generically indicated by the index “z” (z = 0 to 5).
j	The individual registers associated with receive rule table are generically indicated by the index “j”; for example, RCFDCnCFDGAFLIDj (j = 0 to 15) is the receive rule ID register.
k	The individual transmit/receive FIFO buffers are generically indicated by the index “k”; for example, RCFDCnCFDCFCCk (k = 0 to [channel m × 3 + 2]) is the transmit/receive FIFO buffer configuration/control register.
x	The individual receive FIFO buffers are generically identified by the index “x”; for example, RCFDCnCFDRFSTSx (x = 0 to 7)*1 is the receive FIFO buffer status register.
d	Data field registers of transmit/receive FIFO buffers and receive FIFO buffers are identified by “d”; for example, the transmit/receive FIFO buffer data field register is described as RCFDCnCFDCFDFd_k (d = 0 to 15).
q	The individual receive buffers are generically indicated by the index “q”; for example, RCFDCnCFDRMIDq (q = 0 to [channel m × 16 + 15]) is the receive buffer ID register.
p	The individual transmit buffers are generically indicated by the index “p”; for example, RCFDCnCFDTMCp (p = 0 to [channel m × 32 + 31]) is the transmit buffer control register.
b	Data field registers of receive buffers and transmit buffers are identified by “b”; for example, the receive buffer data field register is described as RCFDCnCFDRMDFb_q (b = 0 to 15).
r	The individual RAM tests for CAN are generically indicated by the index “r”; for example, RCFDCnCFDRPGACCr (r = 0 to 63) is the RAM test page access register.
y	The registers not covered above are indicated by the index “y”; for example, RCFDCnCFDRMNDy (y = 0 to 2 with n = 0, or y = 0, 1 with n = 1) is a receive buffer new data register.

Note: The functions and descriptions of registers in this section are for the RS-CANFD that has 6 channels (m = 0 to 5). When referring to information with indices, regard the index values as the ones corresponding to your target product. Also, note that, if the value of an index exceeds the range described in this section due to your target product, write the value after reset when writing to bits outside the index range.

Note 1. Only the index “x” of RCFDCnCFDCDTCT regisiter and RCFDCnCFDCDTSTS register for RH850/F1KM-S1 are x = 0 to 5.

The following table lists the values of indices for individual products.

Table 24.12 Indices for Individual Products (RH850/F1KH-D8)

	Indices for Individual Products		
Unit Name	176 Pins	233 Pins	324 Pins
RCFDC0	m = 0 to 7	m = 0 to 7	m = 0 to 7
	z = 0 to 7	z = 0 to 7	z = 0 to 7
	j = 0 to 15	j = 0 to 15	j = 0 to 15
	k = 0 to 23	k = 0 to 23	k = 0 to 23
	x = 0 to 7	x = 0 to 7	x = 0 to 7
	d = 0 to 15	d = 0 to 15	d = 0 to 15
	q = 0 to 127	q = 0 to 127	q = 0 to 127
	p = 0 to 255	p = 0 to 255	p = 0 to 255
	b = 0 to 15	b = 0 to 15	b = 0 to 15
	r = 0 to 63	r = 0 to 63	r = 0 to 63
	y = 0 to 3	y = 0 to 3	y = 0 to 3
RCFDC1	—	—	m = 0 to 3
	—	—	z = 8 to 11
	—	—	j = 0 to 15
	—	—	k = 0 to 11
	—	—	x = 0 to 7
	—	—	d = 0 to 15
	—	—	q = 0 to 63
	—	—	p = 0 to 127
	—	—	b = 0 to 15
	—	—	r = 0 to 63
	—	—	y = 0, 1

Table 24.13 Indices for Individual Products (RH850/F1KM-S4)

	Indices for Individual Products				
Unit Name	100 Pins	144 Pins	176 Pins	233 Pins	272 Pins
RCFDC0	m = 0 to 7	m = 0 to 7	m = 0 to 7	m = 0 to 7	m = 0 to 7
	z = 0 to 7	z = 0 to 7	z = 0 to 7	z = 0 to 7	z = 0 to 7
	j = 0 to 15	j = 0 to 15	j = 0 to 15	j = 0 to 15	j = 0 to 15
	k = 0 to 23	k = 0 to 23	k = 0 to 23	k = 0 to 23	k = 0 to 23
	x = 0 to 7	x = 0 to 7	x = 0 to 7	x = 0 to 7	x = 0 to 7
	d = 0 to 15	d = 0 to 15	d = 0 to 15	d = 0 to 15	d = 0 to 15
	q = 0 to 127	q = 0 to 127	q = 0 to 127	q = 0 to 127	q = 0 to 127
	p = 0 to 255	p = 0 to 255	p = 0 to 255	p = 0 to 255	p = 0 to 255
	b = 0 to 15	b = 0 to 15	b = 0 to 15	b = 0 to 15	b = 0 to 15
	r = 0 to 63	r = 0 to 63	r = 0 to 63	r = 0 to 63	r = 0 to 63
	y = 0 to 3	y = 0 to 3	y = 0 to 3	y = 0 to 3	y = 0 to 3

Table 24.14 Indices for Individual Products (RH850/F1KM-S2)

	Indices for Individual Products		
Unit Name	100 Pins	144 Pins	176 Pins
RCFDC0	m = 0 to 7	m = 0 to 7	m = 0 to 7
	z = 0 to 7	z = 0 to 7	z = 0 to 7
	j = 0 to 15	j = 0 to 15	j = 0 to 15
	k = 0 to 23	k = 0 to 23	k = 0 to 23
	x = 0 to 7	x = 0 to 7	x = 0 to 7
	d = 0 to 15	d = 0 to 15	d = 0 to 15
	q = 0 to 127	q = 0 to 127	q = 0 to 127
	p = 0 to 255	p = 0 to 255	p = 0 to 255
	b = 0 to 15	b = 0 to 15	b = 0 to 15
	r = 0 to 63	r = 0 to 63	r = 0 to 63
	y = 0 to 3	y = 0 to 3	y = 0 to 3

Table 24.15 Indices for Individual Products (RH850/F1KM-S1)

	Indices for Individual Products			
Unit Name	48 Pins	64 Pins	80 Pins	100 Pins
RCFDC0	m = 0	m = 0 to 2	m = 0 to 2	m = 0 to 5
	z = 0	z = 0 to 2	z = 0 to 2	z = 0 to 5
	j = 0 to 15	j = 0 to 15	j = 0 to 15	j = 0 to 15
	k = 0 to 2	k = 0 to 8	k = 0 to 8	k = 0 to 17
	x = 0 to 7*1	x = 0 to 7*1	x = 0 to 7*1	x = 0 to 7*1
	d = 0 to 15	d = 0 to 15	d = 0 to 15	d = 0 to 15
	q = 0 to 15	q = 0 to 47	q = 0 to 47	q = 0 to 95
	p = 0 to 31	p = 0 to 95	p = 0 to 95	p = 0 to 191
	b = 0 to 15	b = 0 to 15	b = 0 to 15	b = 0 to 15
	r = 0 to 63	r = 0 to 63	r = 0 to 63	r = 0 to 63
	y = 0	y = 0, 1	y = 0, 1	y = 0 to 2

Note 1. Only the index “x” of RCFDCnCFDCDTCT regisiter and RCFDCnCFDCDTSTS register for RH850/F1KM-S1 are x = 0 to 5.

24.1.2 Register Base Addresses

RCFDCn base addresses are listed in the following table.

RCFDCn register addresses are given as offsets from the base addresses.

Table 24.16 Register Base Addresses (RH850/F1KH-D8)

Base Address Name	Base Address
<RCFDC0_base>	FFD0 0000_H
<RCFDC1_base>	FFD2 0000_H

Table 24.17 Register Base Address (RH850/F1KM-S4, RH850/F1KM-S2, RH850/F1KM-S1)

Base Address Name	Base Address
<RCFDC0_base>	FFD0 0000_H

24.1.3 Clock Supply

The RCFDCn clock supply is shown in the following table.

Table 24.18 Clock Supply (RH850/F1KH-D8, RH850/F1KM-S4, RH850/F1KM-S2, RH850/F1KM-S1)

Unit Name	Unit Clock Name	Supply Clock Name	Description
RCFDCn	clk_xincan	CKSCLK_ICANOSC	Communication clock from OSC clock
	clkc	CKSCLK_IPERI2	Communication clock
	pclk	CKSCLK_ICAN	Module clock
	Register access clock	CPUCLK_M, CKSCLK_ICAN	Bus clock

The operating frequency of the RCFDCn depends on the transfer rate and the number of channels in use. **Table 24.19, Range of Operating Frequency Depending on the Transfer Rate and the Number of Channels in Use in the RH850/F1KH and RH850/F1KM** shows the range of the frequency.

Table 24.19 Range of Operating Frequency Depending on the Transfer Rate and the Number of Channels in Use in the RH850/F1KH and RH850/F1KM

Condition			Range of Operating Frequency		
Nominal Bit Rate	Data Bit Rate	No. of Channels in Use (max.)	pclk	clk_xincan*1	clkc*1
500 kbps	5 Mbps	8 ch	pclk = 80 MHz	Not applicable	clkc = 40 MHz
1 Mbps	2 Mbps	8 ch	pclk = 80 MHz	Not applicable	clkc = 40 MHz
500 kbps	2 Mbps	2 ch	pclk = 24 MHz	clk_xincan = 12 MHz	Not applicable
500 kbps	2 Mbps	8 ch	pclk = 80 MHz	Not applicable	clkc = 40 MHz

Note 1. Setting the DCS bit in the RCFDCnCFDGCFG register enables to select either clk_xincan or clkc. Set clocks less than or equal to pclk/2.

CAUTION

When the RS-CANFD module is used in stop mode, set the MainOSC as the clock source of the RS-CANFD module. For details about how to set the clock source, see **Section 12AB.4.3.10, RS-CANFD Clock Domains C_ISO_CAN and C_ISO_CANOSC** and **Section 12C.4.3.9, RS-CANFD Clock Domains C_ISO_CAN and C_ISO_CANOSC**.

24.1.4 Interrupt Requests

RCFDCn interrupt requests are listed in the following table.

Table 24.20 Interrupt Requests (RH850/F1KH-D8)

Unit	Interrupt Signal	Description	Interrupt Number	DMA Trigger Number
RCFDC0				
Global	INTRCANGERR0	CAN global error interrupt	22	—
	INTRCANGRECC0	CAN receive FIFO interrupt	23	—
	RSCANFDRF0	Reception FIFO access message buffers0	—	60
	RSCANFDRF1	Reception FIFO access message buffers1	—	61
	RSCANFDRF2	Reception FIFO access message buffers2	—	62
	RSCANFDRF3	Reception FIFO access message buffers3	—	63
	RSCANFDRF4	Reception FIFO access message buffers4	—	68
	RSCANFDRF5	Reception FIFO access message buffers5	—	69
	RSCANFDRF6	Reception FIFO access message buffers6	—	82
	RSCANFDRF7	Reception FIFO access message buffers7	—	83
CAN0	INTRCAN0ERR	CAN0 error interrupt	24	—
	INTRCAN0REC	CAN0 transmit/receive FIFO receive completion interrupt	25	—
	INTRCAN0TRX	CAN0 transmit interrupt	26	—
	RSCANFDCF0	CAN0 common FIFO access message buffers	—	23
CAN1	INTRCAN1ERR	CAN1 error interrupt	113	—
	INTRCAN1REC	CAN1 transmit/receive FIFO receive completion interrupt	114	—
	INTRCAN1TRX	CAN1 transmit interrupt	115	—
	RSCANFDCF1	CAN1 common FIFO access message buffers	—	24
CAN2	INTRCAN2ERR	CAN2 error interrupt	217	—
	INTRCAN2REC	CAN2 transmit/receive FIFO receive completion interrupt	218	—
	INTRCAN2TRX	CAN2 transmit interrupt	219	—
	RSCANFDCF2	CAN2 common FIFO access message buffers	—	26
CAN3	INTRCAN3ERR	CAN3 error interrupt	220	—
	INTRCAN3REC	CAN3 transmit/receive FIFO receive completion interrupt	221	—
	INTRCAN3TRX	CAN3 transmit interrupt	222	—
	RSCANFDCF3	CAN3 common FIFO access message buffers	—	27
CAN4	INTRCAN4ERR	CAN4 error interrupt	272	—
	INTRCAN4REC	CAN4 transmit/receive FIFO receive completion interrupt	273	—
	INTRCAN4TRX	CAN4 transmit interrupt	274	—
	RSCANFDCF4	CAN4 common FIFO access message buffers	—	48
CAN5	INTRCAN5ERR	CAN5 error interrupt	287	—
	INTRCAN5REC	CAN5 transmit/receive FIFO receive completion interrupt	288	—
	INTRCAN5TRX	CAN5 transmit interrupt	289	—
	RSCANFDCF5	CAN5 common FIFO access message buffers	—	49
CAN6	INTRCAN6ERR	CAN6 error interrupt	321	—
	INTRCAN6REC	CAN6 transmit/receive FIFO receive completion interrupt	322	—
	INTRCAN6TRX	CAN6 transmit interrupt	323	—
	RSCANFDCF6	CAN6 common FIFO access message buffers	—	64

Table 24.20 Interrupt Requests (RH850/F1KH-D8)

Unit	Interrupt Signal	Description	Interrupt Number	DMA Trigger Number
CAN7	INTRCAN7ERR	CAN7 error interrupt	332	—
	INTRCAN7REC	CAN7 transmit/receive FIFO receive completion interrupt	333	—
	INTRCAN7TRX	CAN7 transmit interrupt	334	—
	RSCANFDCF7	CAN7 common FIFO access message buffers	—	65
RCFDC1				
Global	INTRCANGERR1	CAN global error interrupt	319	—
	INTRCANGRECC1	CAN receive FIFO interrupt	320	—
	RSCANFDRF8	Reception FIFO access message buffers8	—	96
	RSCANFDRF9	Reception FIFO access message buffers9	—	97
	RSCANFDRF10	Reception FIFO access message buffers10	—	98
	RSCANFDRF11	Reception FIFO access message buffers11	—	99
	RSCANFDRF12	Reception FIFO access message buffers12	—	15
	RSCANFDRF13	Reception FIFO access message buffers13	—	25
	RSCANFDRF14	Reception FIFO access message buffers14	—	84
	RSCANFDRF15	Reception FIFO access message buffers15	—	57
CAN0	INTRCAN8ERR	CAN0 error interrupt	244	—
	INTRCAN8REC	CAN0 transmit/receive FIFO receive completion interrupt	245	—
	INTRCAN8TRX	CAN0 transmit interrupt	246	—
	RSCANFDCF8	CAN0 common FIFO access message buffers	—	92
CAN1	INTRCAN9ERR	CAN1 error interrupt	247	—
	INTRCAN9REC	CAN1 transmit/receive FIFO receive completion interrupt	248	—
	INTRCAN9TRX	CAN1 transmit interrupt	249	—
	RSCANFDCF9	CAN1 common FIFO access message buffers	—	93
CAN2	INTRCAN10ERR	CAN2 error interrupt	250	—
	INTRCAN10REC	CAN2 transmit/receive FIFO receive completion interrupt	251	—
	INTRCAN10TRX	CAN2 transmit interrupt	252	—
	RSCANFDCF10	CAN2 common FIFO access message buffers	—	94
CAN3	INTRCAN11ERR	CAN3 error interrupt	253	—
	INTRCAN11REC	CAN3 transmit/receive FIFO receive completion interrupt	254	—
	INTRCAN11TRX	CAN3 transmit interrupt	255	—
	RSCANFDCF11	CAN3 common FIFO access message buffers	—	95

Table 24.21 Interrupt Requests (RH850/F1KM-S4, RH850/F1KM-S2)

Unit	Interrupt Signal	Description	Interrupt Number	DMA Trigger Number
RCFDC0				
Global	INTRCANGERR0	CAN global error interrupt	22	—
	INTRCANGRECC0	CAN receive FIFO interrupt	23	—
	RSCANFDRF0	Reception FIFO access message buffers0	—	60
	RSCANFDRF1	Reception FIFO access message buffers1	—	61
	RSCANFDRF2	Reception FIFO access message buffers2	—	62
	RSCANFDRF3	Reception FIFO access message buffers3	—	63
	RSCANFDRF4	Reception FIFO access message buffers4	—	68
	RSCANFDRF5	Reception FIFO access message buffers5	—	69
	RSCANFDRF6	Reception FIFO access message buffers6	—	82
	RSCANFDRF7	Reception FIFO access message buffers7	—	83
CAN0	INTRCAN0ERR	CAN0 error interrupt	24	—
	INTRCAN0REC	CAN0 transmit/receive FIFO receive completion interrupt	25	—
	INTRCAN0TRX	CAN0 transmit interrupt	26	—
	RSCANFDCF0	CAN0 common FIFO access message buffers	—	23
CAN1	INTRCAN1ERR	CAN1 error interrupt	113	—
	INTRCAN1REC	CAN1 transmit/receive FIFO receive completion interrupt	114	—
	INTRCAN1TRX	CAN1 transmit interrupt	115	—
	RSCANFDCF1	CAN1 common FIFO access message buffers	—	24
CAN2	INTRCAN2ERR	CAN2 error interrupt	217	—
	INTRCAN2REC	CAN2 transmit/receive FIFO receive completion interrupt	218	—
	INTRCAN2TRX	CAN2 transmit interrupt	219	—
	RSCANFDCF2	CAN2 common FIFO access message buffers	—	26
CAN3	INTRCAN3ERR	CAN3 error interrupt	220	—
	INTRCAN3REC	CAN3 transmit/receive FIFO receive completion interrupt	221	—
	INTRCAN3TRX	CAN3 transmit interrupt	222	—
	RSCANFDCF3	CAN3 common FIFO access message buffers	—	27
CAN4	INTRCAN4ERR	CAN4 error interrupt	272	—
	INTRCAN4REC	CAN4 transmit/receive FIFO receive completion interrupt	273	—
	INTRCAN4TRX	CAN4 transmit interrupt	274	—
	RSCANFDCF4	CAN4 common FIFO access message buffers	—	48
CAN5	INTRCAN5ERR	CAN5 error interrupt	287	—
	INTRCAN5REC	CAN5 transmit/receive FIFO receive completion interrupt	288	—
	INTRCAN5TRX	CAN5 transmit interrupt	289	—
	RSCANFDCF5	CAN5 common FIFO access message buffers	—	49
CAN6	INTRCAN6ERR	CAN6 error interrupt	321	—
	INTRCAN6REC	CAN6 transmit/receive FIFO receive completion interrupt	322	—
	INTRCAN6TRX	CAN6 transmit interrupt	323	—
	RSCANFDCF6	CAN6 common FIFO access message buffers	—	64
CAN7	INTRCAN7ERR	CAN7 error interrupt	332	—
	INTRCAN7REC	CAN7 transmit/receive FIFO receive completion interrupt	333	—
	INTRCAN7TRX	CAN7 transmit interrupt	334	—
	RSCANFDCF7	CAN7 common FIFO access message buffers	—	65

Table 24.22 Interrupt Requests (RH850/F1KM-S1)

Unit	Interrupt Signal	Description	Interrupt Number	DMA Trigger Number
RCFDC0				
Global	INTRCANGERR0	CAN global error interrupt	22	—
	INTRCANGRECC0	CAN receive FIFO interrupt	23	—
	RSCANFDRF0	Reception FIFO access message buffers0	—	60
	RSCANFDRF1	Reception FIFO access message buffers1	—	61
	RSCANFDRF2	Reception FIFO access message buffers2	—	62
	RSCANFDRF3	Reception FIFO access message buffers3	—	63
	RSCANFDRF4	Reception FIFO access message buffers4	—	68
	RSCANFDRF5	Reception FIFO access message buffers5	—	69
CAN0	INTRCAN0ERR	CAN0 error interrupt	24	—
	INTRCAN0REC	CAN0 transmit/receive FIFO receive completion interrupt	25	—
	INTRCAN0TRX	CAN0 transmit interrupt	26	—
	RSCANFDCF0	CAN0 common FIFO access message buffers	—	23
CAN1	INTRCAN1ERR	CAN1 error interrupt	113	—
	INTRCAN1REC	CAN1 transmit/receive FIFO receive completion interrupt	114	—
	INTRCAN1TRX	CAN1 transmit interrupt	115	—
	RSCANFDCF1	CAN1 common FIFO access message buffers	—	24
CAN2	INTRCAN2ERR	CAN2 error interrupt	217	—
	INTRCAN2REC	CAN2 transmit/receive FIFO receive completion interrupt	218	—
	INTRCAN2TRX	CAN2 transmit interrupt	219	—
	RSCANFDCF2	CAN2 common FIFO access message buffers	—	26
CAN3	INTRCAN3ERR	CAN3 error interrupt	220	—
	INTRCAN3REC	CAN3 transmit/receive FIFO receive completion interrupt	221	—
	INTRCAN3TRX	CAN3 transmit interrupt	222	—
	RSCANFDCF3	CAN3 common FIFO access message buffers	—	27
CAN4	INTRCAN4ERR	CAN4 error interrupt	272	—
	INTRCAN4REC	CAN4 transmit/receive FIFO receive completion interrupt	273	—
	INTRCAN4TRX	CAN4 transmit interrupt	274	—
	RSCANFDCF4	CAN4 common FIFO access message buffers	—	48
CAN5	INTRCAN5ERR	CAN5 error interrupt	287	—
	INTRCAN5REC	CAN5 transmit/receive FIFO receive completion interrupt	288	—
	INTRCAN5TRX	CAN5 transmit interrupt	289	—
	RSCANFDCF5	CAN5 common FIFO access message buffers	—	49

NOTE

For the wake-up factors from standby mode, see **Section 14.1.2.1, Wake-Up Factors for Stand-By Modes**.

24.1.5 Reset Sources

RCFDCn reset sources are listed in the following table. RCFDCn is initialized by these reset sources.

Table 24.23 Reset Sources (RH850/F1KH-D8, RH850/F1KM-S4, RH850/F1KM-S2, RH850/F1KM-S1)

Unit Name	Reset Source
RCFDCn	All reset sources (ISORES)

24.1.6 External Input/Output Signals

External input/output signals of RCFDCn are listed below.

Table 24.24 External Input/Output Signals (RH850/F1KH-D8)

Unit Signal Name	Description	Alternative Port Pin Signal
RCFDC0		
CANzRX (z = 0 to 7)	CANm receive data input	CANzRX (z = 0 to 7)
CANzTX (z = 0 to 7)	CANm transmit data output	CANzTX (z = 0 to 7)
RCFDC1		
CANzRX (z = 8 to 11)	CANm receive data input	CANzRX (z = 8 to 11)
CANzTX (z = 8 to 11)	CANm transmit data output	CANzTX (z = 8 to 11)

Table 24.25 External Input/Output Signals (RH850/F1KM-S4, RH850/F1KM-S2)

Unit Signal Name	Description	Alternative Port Pin Signal
RCFDC0		
CANzRX (z = 0 to 7)	CANm receive data input	CANzRX (z = 0 to 7)
CANzTX (z = 0 to 7)	CANm transmit data output	CANzTX (z = 0 to 7)

Table 24.26 External Input/Output Signals (RH850/F1KM-S1)

Unit Signal Name	Description	Alternative Port Pin Signal
RCFDC0		
CANzRX (z = 0 to 5)	CANm receive data input	CANzRX (z = 0 to 5)
CANzTX (z = 0 to 5)	CANm transmit data output	CANzTX (z = 0 to 5)

24.2 Overview

24.2.1 Functional Overview

Table 24.27, RS-CANFD Module Specifications shows the RS-CANFD module specifications that has 8 channels (m = 0 to 7) for unit 0 (n = 0) and 4 channels (m = 0 to 3) for unit 1 (n = 1). **Figure 24.1, RS-CANFD Module Block Diagram** shows the RS-CANFD module block diagram.

Table 24.27 RS-CANFD Module Specifications

Item	Specification
Number of channels	8 (n = 0), 4 (n = 1)
Protocol	ISO11898-1 compliant Using CAN FD frames is selectable by switching interface modes.
Communication speed	Classical CAN only mode : • Maximum 1 Mbps $\text{Communication speed (CANm bit time clock)} = \frac{1}{\text{CANm bit time}}$ CANm bit time = CANmTq × Tq count per bit $\text{CANmTq} = \frac{\text{(NBRP[9: 0] bits in the RCFDCnCFDCmNCFG register + 1)}}{\text{fCAN}}$ fCAN: Frequency of CAN clock (selected by the DCS bit in the RCFDCnCFDGCFG register) CAN FD mode and CAN FD only mode: • Data bit rate: max.5 Mbps (Nominal bit rate ≤ 500 Kbps) • Data bit rate: max.2 Mbps (1Mbps ≥ Nominal bit rate > 500 Kbps) Note : fCAN = 40 MHz $\text{Transmission rate (CANm nominal bit time clock)} = \frac{1}{\text{CANm nominal bit time}}$ $\text{Transmission rate (CANm data bit time clock)} = \frac{1}{\text{CANm data bit time}}$ CANm nominal bit time = CANmTq(N) × Tq count per nominal bit CANm data bit time = CANmTq(D) × Tq count per data bit $\text{CANmTq(N)} = \frac{\text{(NBRP[9: 0] bits in the RCFDCnCFDCmNCFG register + 1)}}{\text{fCAN}}$ $\text{CANmTq(D)} = \frac{\text{(DBRP[7: 0] bits in the RCFDCnCFDCmDCFG register + 1)}}{\text{fCAN}}$ fCAN: Frequency of CAN clock (selected by the DCS bit in the RCFDCnCFDGCFG register) m = 0 to 7 (n = 0), m = 0 to 3 with (n = 1) Tq: Time quantum

Table 24.27 RS-CANFD Module Specifications

Item	Specification
Buffer	RCFDC0: 1280 buffers in total • Individual buffers: 256 buffers (32 buffers × 8 channels) Transmit buffer: 32 buffers per channel Transmit queue: Single queue per channel (shared with the transmit buffer; up to 32 buffers allocatable) • Shared buffers: 1024 buffers for all channels Receive buffer: 0 to 128 buffers Receive FIFO buffer: 8 FIFO buffers (up to 128 buffers allocatable to each) Transmit/receive FIFO buffer: 3 FIFO buffers per channel (up to 128 buffers allocatable to each) • ECC included RCFDC1: 640 buffers in total • Individual buffers: 128 buffers (32 buffers × 4 channels) Transmit buffer: 32 buffers per channel Transmit queue: Single queue per channel (shared with the transmit buffer; up to 32 buffers allocatable) • Shared buffers: 512 buffers for all channels Receive buffer: 0 to 64 buffers Receive FIFO buffer: 8 FIFO buffers (up to 128 buffers allocatable to each) Transmit/receive FIFO buffer: 3 FIFO buffers per channel (up to 128 buffers allocatable to each) • ECC included
Reception function	• Receives data frames and remote frames. • Selects ID format (standard ID, extended ID, or both IDs) to be received. • Sets interrupt enable/disable for each FIFO. • Mirror function (reception of messages transmitted from the own CAN node) • Timestamp function (to record message reception time as a 16-bit timer value)
Reception filter function	• Selects receive messages according to 1024 receive rules. • Sets the number of receive rules (0 to 255) for each channel. • Acceptance filter processing: Sets ID and mask for each receive rule. • DLC filter processing: Enables DLC filter check for each acceptance rule.
Receive message transfer function	• Routing function Transfers receive messages to arbitrary destinations (can be transferred to up to 8 buffers) Transfer destination: Receive buffer, receive FIFO buffer, and/or transmit/receive FIFO buffer • Label addition function Stores label information together with a message in a receive buffer and FIFO buffer.
Transmission function	• Transmits data frames and remote frames. • Selects ID format (standard ID, extended ID, or both IDs) to be transmitted. • Sets interrupt enable/disable for each transmit buffer and transmit/receive FIFO buffer. • Selects ID priority transmission or transmit buffer number priority transmission. • Transmit request can be aborted (possible to confirm with a flag) • One-shot transmission function
Interval transmission function	Transmits messages at configurable intervals (transmit mode or gateway mode of transmit/receive FIFO buffers)
Transmit queue function	Transmits all stored messages according to the ID priority.
Transmit history function	Stores the history information of transmission-completed messages
Gateway function	Transmits a received message automatically.
Bus off recovery mode selection	Selects the method for returning from bus off state. • ISO11898-1 compliant • Automatic entry to channel halt mode at bus-off entry • Automatic entry to channel halt mode at bus-off end • Transition to channel halt mode by program request • Transition to the error-active state by program request (forcible return from the bus off state)

Table 24.27 RS-CANFD Module Specifications

Item	Specification
Error status monitoring	• Monitors CAN protocol errors (stuff error, form error, ACK error, CRC error, bit error, ACK delimiter error, and bus lock). • Detects error status transitions (error warning, error passive, bus off entry, and bus off recovery) • Reads the error counter. • Monitors DLC errors.
Interrupt source	RCFDC0: 26 sources, RCFDC1: 14 sources • Global interrupts (2 sources/unit) (n = 0, 1) Receive FIFO interrupt (1 source/unit) (n = 0, 1) Global error interrupt (1 source/unit) (n = 0, 1) • Channel interrupts (3 sources/channel) CANm transmit interrupt (m = 0 to 7 (n = 0), m = 0 to 3 (n = 1)) 1. CANm transmit interrupt – CANm transmit complete interrupt – CANm transmit abort interrupt – CANm transmit/receive FIFO transmit complete interrupt (in transmit mode, gateway mode) – CANm transmit history interrupt – CANm transmit queue interrupt 2. CANm transmit/receive FIFO receive complete interrupt (in receive mode, gateway mode) 3. CANm error interrupt
CAN stop mode	Reduces power consumption by stopping clock supply to the RS-CANFD module.
CAN clock source	Selects the clkc or the clk_xincan. As for the range of operating frequency, see **Table 24.19, Range of Operating Frequency Depending on the Transfer Rate and the Number of Channels in Use in the RH850/F1KH and RH850/F1KM**.
Test function	Test function for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback) • Restricted operation mode • RAM test (read/write test) • Inter-channel communication test [CRC error test enabled]

24.2.2 Interface Modes

The RS-CANFD has three interface modes.

- Classical CAN only mode: Handles only classical CAN frames.
- CAN FD mode: Handles classical CAN frames and CAN FD frames.
- CAN FD only mode: Handles only CAN FD frames.

Interface modes are switched by the CLOE bit and the FDOE in the RCFDCnCFDCmFDCFG register.

Set interface modes for each channel.

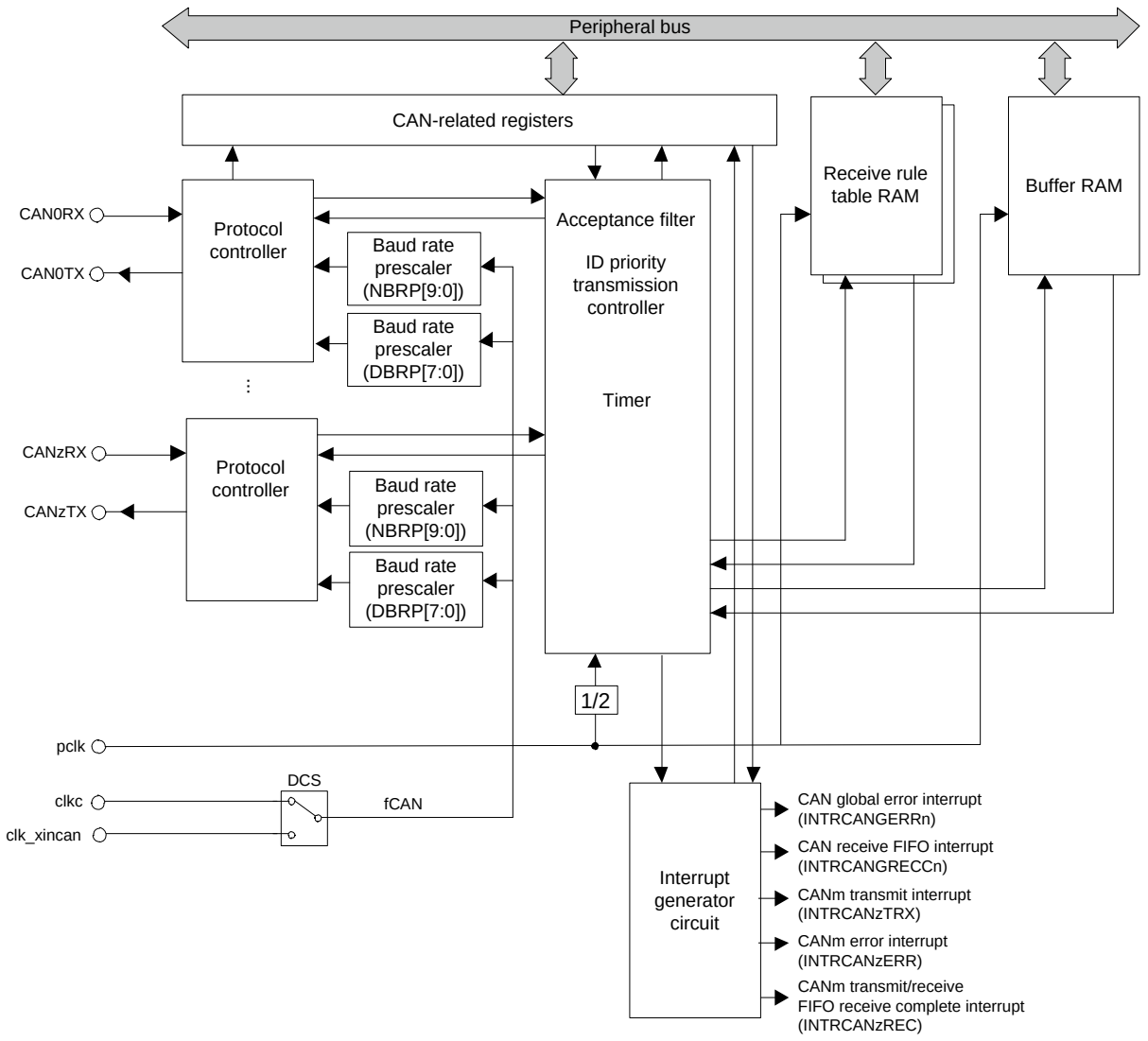
Table 24.28 Description and Configuration of Interface Mode

Interface Mode	Description	Configuration
CAN-FD mode	Classical and CAN-FD frames can be transmitted and received	RCFDCnCFDCmFDCFG.CLOE = 0 RCFDCnCFDCmFDCFG.FDOE = 0
CAN-FD only mode	Only CAN-FD frames can be transmitted and received. Classical frames will cause the detection of an error	RCFDCnCFDCmFDCFG.CLOE = 0 RCFDCnCFDCmFDCFG.FDOE = 1
Classical CAN only mode	Only Classical Frame can be transmitted and received. FD frames will cause the detection of an error	RCFDCnCFDCmFDCFG.CLOE = 1 RCFDCnCFDCmFDCFG.FDOE = 0

24.2.3 CAN FD Protocol

This product supports CAN FD according to the ISO/DIS 11898-1 protocol that specifies the new CRC field including stuff counters.

24.2.4 Block Diagram



Note: n = 0, 1
z = 0 to 11
m = 0 to 7 (n = 0) and m = 0 to 3 (n = 1)
NBRP[9:0]: Bits in the RCFDCnCFDCmNCFG register
DBRP[7:0]: Bits in the RCFDCnCFDCmDCFG register
DCS: Bits in the RCFDCnCFDGCFG register
fCAN: CAN clock

Figure 24.1 RS-CANFD Module Block Diagram

24.3 Registers

This section describes all registers to be used when the RS-CANFD is used.

24.3.1 List of Registers

The following tables list RS-CANFD registers to be used.

For details about <RCFDCn_base>, see **Section 24.1.2, Register Base Addresses**.

For details about registers initialized in Global reset mode or Channel reset mode, see following.

- **Table 24.121, Registers Initialized in Global Reset Mode or Channel Reset Mode**
- **Table 24.122, Registers Initialized Only in Global Reset Mode**

Table 24.29 List of Registers

Module Name	Register Name	Symbol	Address	Guard Group
Channel-related registers				
RCFDCn	Channel nominal bit rate configuration register	RCFDCnCFDCmNCFG	<RCFDCn_base> + 0000_H + (10_H × m)	RCFDCn Chm
RCFDCn	Channel control register	RCFDCnCFDCmCTR	<RCFDCn_base> + 0004_H + (10_H × m)	RCFDCn Chm
RCFDCn	Channel status register	RCFDCnCFDCmSTS	<RCFDCn_base> + 0008_H + (10_H × m)	RCFDCn Chm
RCFDCn	Channel error flag register	RCFDCnCFDCmERFL	<RCFDCn_base> + $000C_H$ + (10_H × m)	RCFDCn Chm
RCFDCn	Channel data bit rate configuration register	RCFDCnCFDCmDCFG	<RCFDCn_base> + 0700_H + (20_H × m)	RCFDCn Chm
RCFDCn	Channel CAN FD configuration register	RCFDCnCFDCmFDCFG	<RCFDCn_base> + 0704_H + (20_H × m)	RCFDCn Chm
RCFDCn	Channel CAN FD control register	RCFDCnCFDCmFDCTR	<RCFDCn_base> + 0708_H + (20_H × m)	RCFDCn Chm
RCFDCn	Channel CAN FD status register	RCFDCnCFDCmFDSTS	<RCFDCn_base> + $070C_H$ + (20_H × m)	RCFDCn Chm
RCFDCn	Channel CAN FD CRC register	RCFDCnCFDCmFDCRC	<RCFDCn_base> + 0710_H + (20_H × m)	RCFDCn Chm
Global-related registers				
RCFDCn	Global configuration register	RCFDCnCFDGCFG	<RCFDCn_base> + 0084_H	RCFDCn global
RCFDCn	Global control register	RCFDCnCFDGCTR	<RCFDCn_base> + 0088_H	RCFDCn global
RCFDCn	Global status register	RCFDCnCFDGSTS	<RCFDCn_base> + $008C_H$	RCFDCn global
RCFDCn	Global error flag register	RCFDCnCFDGERFL	<RCFDCn_base> + 0090_H	RCFDCn global
RCFDCn	Global timestamp counter register	RCFDCnCFDGTSC	<RCFDCn_base> + 0094_H	RCFDCn global
RCFDCn	Global TX interrupt status register 0	RCFDCnCFDGTINTSTS0	<RCFDCn_base> + 0610_H	RCFDCn global
RCFDCn	Global TX interrupt status register 1	RCFDCnCFDGTINTSTS1	<RCFDCn_base> + 0614_H	RCFDCn global
RCFDCn	Global FD configuration register	RCFDCnCFDGFDCFG	<RCFDCn_base> + 0624_H	RCFDCn global
Receive rule-related registers				
RCFDCn	Receive rule entry control register	RCFDCnCFDGAFLECTR	<RCFDCn_base> + 0098_H	RCFDCn global
RCFDCn	Receive rule configuration register 0	RCFDCnCFDGAFLCFG0	<RCFDCn_base> + $009C_H$	RCFDCn global
RCFDCn	Receive rule configuration register 1	RCFDCnCFDGAFLCFG1	<RCFDCn_base> + $00A0_H$	RCFDCn global
RCFDCn	Receive rule ID register	RCFDCnCFDGAFLIDj	<RCFDCn_base> + 1000_H + (10_H × j)	RCFDCn global
RCFDCn	Receive rule mask register	RCFDCnCFDGAFLMj	<RCFDCn_base> + 1004_H + (10_H × j)	RCFDCn global
RCFDCn	Receive rule pointer 0 register	RCFDCnCFDGAFLP0_j	<RCFDCn_base> + 1008_H + (10_H × j)	RCFDCn global
RCFDCn	Receive rule pointer 1 register	RCFDCnCFDGAFLP1_j	<RCFDCn_base> + $100C_H$ + (10_H × j)	RCFDCn global
Receive buffer-related registers				
RCFDCn	Receive buffer number register	RCFDCnCFDRMNB	<RCFDCn_base> + $00A4_H$	RCFDCn global
RCFDCn	Receive buffer new data register	RCFDCnCFDRMNDy	<RCFDCn_base> + $00A8_H$ + (04_H × y)	RCFDCn global
RCFDCn	Receive buffer ID register	RCFDCnCFDRMIDq	<RCFDCn_base> + 2000_H + (80_H × q)	RCFDCn global
RCFDCn	Receive buffer pointer register	RCFDCnCFDRMPTRq	<RCFDCn_base> + 2004_H + (80_H × q)	RCFDCn global
RCFDCn	Receive buffer CAN FD status register	RCFDCnCFDRMFDSTSq	<RCFDCn_base> + 2008_H + (80_H × q)	RCFDCn global
RCFDCn	Receive buffer data field register	RCFDCnCFDRMDFb_q	<RCFDCn_base> + $200C_H$ + (04_H × b) + (80_H × q)	RCFDCn global

Table 24.29 List of Registers

Module Name	Register Name	Symbol	Address	Guard Group
Receive FIFO buffer-related registers				
RCFDCn	Receive FIFO buffer configuration and control register	RCFDCnCFDRFCCx	<RCFDCn_base> + $00B8_H$ + (04_H × x)	RCFDCn global
RCFDCn	Receive FIFO buffer status register	RCFDCnCFDRFSTSx	<RCFDCn_base> + $00D8_H$ + (04_H × x)	RCFDCn global
RCFDCn	Receive FIFO buffer pointer control register	RCFDCnCFDRFPCTRx	<RCFDCn_base> + $00F8_H$ + (04_H × x)	RCFDCn global
RCFDCn	Receive FIFO buffer access id register	RCFDCnCFDRFIDx	<RCFDCn_base> + 6000_H + (80_H × x)	RCFDCn global
RCFDCn	Receive FIFO buffer access pointer register	RCFDCnCFDRFPTRx	<RCFDCn_base> + 6004_H + (80_H × x)	RCFDCn global
RCFDCn	Receive FIFO CAN FD status register	RCFDCnCFDRFFDSTSx	<RCFDCn_base> + 6008_H + (80_H × x)	RCFDCn global
RCFDCn	Receive FIFO buffer access data field register	RCFDCnCFDRFDFd_x	<RCFDCn_base> + $600C_H$ + (04_H × d) + (80_H × x)	RCFDCn global
Transmit/receive FIFO buffer-related registers				
RCFDCn	Transmit/receive FIFO buffer configuration and control register	RCFDCnCFDCFCCk	<RCFDCn_base> + 0118_H + (04_H × k)	RCFDCn global
RCFDCn	Transmit/receive FIFO buffer status register	RCFDCnCFDCFSTSk	<RCFDCn_base> + 0178_H + (04_H × k)	RCFDCn global
RCFDCn	Transmit/receive FIFO buffer pointer control register	RCFDCnCFDCFPCTRk	<RCFDCn_base> + $01D8_H$ + (04_H × k)	RCFDCn global
RCFDCn	Transmit/receive FIFO buffer access id register	RCFDCnCFDCFIDk	<RCFDCn_base> + 6400_H + (80_H × k)	RCFDCn global
RCFDCn	Transmit/receive FIFO buffer access pointer register	RCFDCnCFDCFPTRk	<RCFDCn_base> + 6404_H + (80_H × k)	RCFDCn global
RCFDCn	Transmit/receive FIFO CAN FD configuration/status register	RCFDCnCFDCFFDCSTSk	<RCFDCn_base> + 6408_H + (80_H × k)	RCFDCn global
RCFDCn	Transmit/receive FIFO buffer access data field register	RCFDCnCFDCFDFd_k	<RCFDCn_base> + $640C_H$ + (04_H × d) + (80_H × k)	RCFDCn global
FIFO status-related registers				
RCFDCn	FIFO empty status register	RCFDCnCFDFESTS	<RCFDCn_base> + 0238_H	RCFDCn global
RCFDCn	FIFO full status register	RCFDCnCFDFFSTS	<RCFDCn_base> + $023C_H$	RCFDCn global
RCFDCn	FIFO message lost status register	RCFDCnCFDFMSTS	<RCFDCn_base> + 0240_H	RCFDCn global
RCFDCn	Receive FIFO buffer interrupt flag status register	RCFDCnCFDRFISTS	<RCFDCn_base> + 0244_H	RCFDCn global
RCFDCn	Transmit/receive FIFO buffer receive interrupt flag status register	RCFDCnCFDCFRISTS	<RCFDCn_base> + 0248_H	RCFDCn global
RCFDCn	Transmit/receive FIFO buffer transmit interrupt flag status register	RCFDCnCFDCFTISTS	<RCFDCn_base> + $024C_H$	RCFDCn global
FIFO DMA-related registers				
RCFDCn	DMA enable register	RCFDCnCFDCDTCT	<RCFDCn_base> + 0640_H	RCFDCn global
RCFDCn	DMA status register	RCFDCnCFDCDTSTS	<RCFDCn_base> + 0644_H	RCFDCn global
Transmit buffer-related registers				
RCFDCn	Transmit buffer control register	RCFDCnCFDTMCp	<RCFDCn_base> + 0250_H + (01_H × p)	RCFDCn global
RCFDCn	Transmit buffer status register	RCFDCnCFDTMSTSp	<RCFDCn_base> + 0350_H + (01_H × p)	RCFDCn global
RCFDCn	Transmit buffer ID register	RCFDCnCFDTMIDp	<RCFDCn_base> + 8000_H + (80_H × p)	RCFDCn global
RCFDCn	Transmit buffer pointer register	RCFDCnCFDTMPTRp	<RCFDCn_base> + 8004_H + (80_H × p)	RCFDCn global
RCFDCn	Transmit buffer CAN FD configuration register	RCFDCnCFDTMFDCTRp	<RCFDCn_base> + 8008_H + (80_H × p)	RCFDCn global
RCFDCn	Transmit buffer data field register	RCFDCnCFDTMDFb_p	<RCFDCn_base> + $800C_H$ + (04_H × b) + (80_H × p)	RCFDCn global
RCFDCn	Transmit buffer interrupt enable configuration register	RCFDCnCFDTMIECm	<RCFDCn_base> + $04D0_H$ + (04_H × m)	RCFDCn global
Transmit buffer status-related registers				
RCFDCn	Transmit buffer transmit request status register	RCFDCnCFDTMTRSTSm	<RCFDCn_base> + 0450_H + (04_H × m)	RCFDCn global
RCFDCn	Transmit buffer transmit abort request status register	RCFDCnCFDTMTARSTSm	<RCFDCn_base> + 0470_H + (04_H × m)	RCFDCn global
RCFDCn	Transmit buffer transmit complete status register	RCFDCnCFDTMTCSTSm	<RCFDCn_base> + 0490_H + (04_H × m)	RCFDCn global
RCFDCn	Transmit buffer transmit abort status register	RCFDCnCFDTMTASTSm	<RCFDCn_base> + $04B0_H$ + (04_H × m)	RCFDCn global

Table 24.29 List of Registers

Module Name	Register Name	Symbol	Address	Guard Group
Transmit queue-related registers				
RCFDCn	Transmit queue configuration and control register	RCFDCnCFDTXQCCm	<RCFDCn_base> + 0550_H + (04_H × m)	RCFDCn Chm
RCFDCn	Transmit queue status register	RCFDCnCFDTXQSTSm	<RCFDCn_base> + 0570_H + (04_H × m)	RCFDCn Chm
RCFDCn	Transmit queue pointer control register	RCFDCnCFDTXQPCTRm	<RCFDCn_base> + 0590_H + (04_H × m)	RCFDCn Chm
Transmit history-related registers				
RCFDCn	Transmit history configuration and control register	RCFDCnCFDTHLCCm	<RCFDCn_base> + $05B0_H$ + (04_H × m)	RCFDCn Chm
RCFDCn	Transmit history status register	RCFDCnCFDTHLSTSm	<RCFDCn_base> + $05D0_H$ + (04_H × m)	RCFDCn Chm
RCFDCn	Transmit history pointer control register	RCFDCnCFDTHLPCTRm	<RCFDCn_base> + $05F0_H$ + (04_H × m)	RCFDCn Chm
RCFDCn	Transmit history access register 0	RCFDCnCFDTHLACC0m	<RCFDCn_base> + 10000_H + (08_H × m)	RCFDCn Chm
RCFDCn	Transmit history access register 1	RCFDCnCFDTHLACC1m	<RCFDCn_base> + 10004_H + (08_H × m)	RCFDCn Chm
Test-related registers				
RCFDCn	Global test configuration register	RCFDCnCFDGTSTCFG	<RCFDCn_base> + 0618_H	RCFDCn global
RCFDCn	Global test control register	RCFDCnCFDGTSTCTR	<RCFDCn_base> + $061C_H$	RCFDCn global
RCFDCn	Global lock key register	RCFDCnCFDGLOCKK	<RCFDCn_base> + $062C_H$	RCFDCn global
RCFDCn	RAM test page access register	RCFDCnCFDRPGACCr	<RCFDCn_base> + 10400_H + (04_H × r)	RCFDCn global

Table 24.30 Transmit Buffer p Allocated to Each Channel

	CANm
Transmit buffer p	Transmit buffer 32 × m + 0
	Transmit buffer 32 × m + 1
	Transmit buffer 32 × m + 2
	Transmit buffer 32 × m + 3
	Transmit buffer 32 × m + 4
	Transmit buffer 32 × m + 5
	Transmit buffer 32 × m + 6
	Transmit buffer 32 × m + 7
	Transmit buffer 32 × m + 8
	Transmit buffer 32 × m + 9
	Transmit buffer 32 × m + 10
	Transmit buffer 32 × m + 11
	Transmit buffer 32 × m + 12
	Transmit buffer 32 × m + 13
	Transmit buffer 32 × m + 14
	Transmit buffer 32 × m + 15
	Transmit buffer 32 × m + 16
	Transmit buffer 32 × m + 17
	Transmit buffer 32 × m + 18
	Transmit buffer 32 × m + 19
	Transmit buffer 32 × m + 20
	Transmit buffer 32 × m + 21
	Transmit buffer 32 × m + 22
	Transmit buffer 32 × m + 23
	Transmit buffer 32 × m + 24
	Transmit buffer 32 × m + 25
	Transmit buffer 32 × m + 26
	Transmit buffer 32 × m + 27
	Transmit buffer 32 × m + 28
	Transmit buffer 32 × m + 29
	Transmit buffer 32 × m + 30
	Transmit buffer 32 × m + 31

Table 24.31 Transmit/Receive FIFO Buffer k Allocated to Each Channel

	CANm
Transmit/receive FIFO buffer k	Transmit/receive FIFO buffer 3 × m + 0
	Transmit/receive FIFO buffer 3 × m + 1
	Transmit/receive FIFO buffer 3 × m + 2

Table 24.32 Transmit Buffer p Linked to the Transmit/Receive FIFO Buffer by the Setting of Bits CFTML[4:0]

Setting of Bits CFTML[4:0]	Transmit Buffer p Linked to the Transmit/Receive FIFO Buffer
00000_B	Transmit buffer 32 × m + 0
00001_B	Transmit buffer 32 × m + 1
00010_B	Transmit buffer 32 × m + 2
00011_B	Transmit buffer 32 × m + 3
00100_B	Transmit buffer 32 × m + 4
00101_B	Transmit buffer 32 × m + 5
00110_B	Transmit buffer 32 × m + 6
00111_B	Transmit buffer 32 × m + 7
01000_B	Transmit buffer 32 × m + 8
01001_B	Transmit buffer 32 × m + 9
01010_B	Transmit buffer 32 × m + 10
01011_B	Transmit buffer 32 × m + 11
01100_B	Transmit buffer 32 × m + 12
01101_B	Transmit buffer 32 × m + 13
01110_B	Transmit buffer 32 × m + 14
01111_B	Transmit buffer 32 × m + 15
10000_B	Transmit buffer 32 × m + 16
10001_B	Transmit buffer 32 × m + 17
10010_B	Transmit buffer 32 × m + 18
10011_B	Transmit buffer 32 × m + 19
10100_B	Transmit buffer 32 × m + 20
10101_B	Transmit buffer 32 × m + 21
10110_B	Transmit buffer 32 × m + 22
10111_B	Transmit buffer 32 × m + 23
11000_B	Transmit buffer 32 × m + 24
11001_B	Transmit buffer 32 × m + 25
11010_B	Transmit buffer 32 × m + 26
11011_B	Transmit buffer 32 × m + 27
11100_B	Transmit buffer 32 × m + 28
11101_B	Transmit buffer 32 × m + 29
11110_B	Transmit buffer 32 × m + 30
11111_B	Transmit buffer 32 × m + 31

Table 24.33 Transmit Buffer p Allocated to the Transmit Queue of Each Channel

Setting of Bits TXQDC[4:0]	Transmit Buffer p Allocated to the Transmit Queue
00000_B	Setting prohibited
00001_B	Setting prohibited
00010_B	Transmit buffer 32 × m + 31 to 32 × m + 29
00011_B	Transmit buffer 32 × m + 31 to 32 × m + 28
00100_B	Transmit buffer 32 × m + 31 to 32 × m + 27
00101_B	Transmit buffer 32 × m + 31 to 32 × m + 26
00110_B	Transmit buffer 32 × m + 31 to 32 × m + 25
00111_B	Transmit buffer 32 × m + 31 to 32 × m + 24
01000_B	Transmit buffer 32 × m + 31 to 32 × m + 23
01001_B	Transmit buffer 32 × m + 31 to 32 × m + 22
01010_B	Transmit buffer 32 × m + 31 to 32 × m + 21
01011_B	Transmit buffer 32 × m + 31 to 32 × m + 20
01100_B	Transmit buffer 32 × m + 31 to 32 × m + 19
01101_B	Transmit buffer 32 × m + 31 to 32 × m + 18
01110_B	Transmit buffer 32 × m + 31 to 32 × m + 17
01111_B	Transmit buffer 32 × m + 31 to 32 × m + 16
10000_B	Transmit buffer 32 × m + 31 to 32 × m + 15
10001_B	Transmit buffer 32 × m + 31 to 32 × m + 14
10010_B	Transmit buffer 32 × m + 31 to 32 × m + 13
10011_B	Transmit buffer 32 × m + 31 to 32 × m + 12
10100_B	Transmit buffer 32 × m + 31 to 32 × m + 11
10101_B	Transmit buffer 32 × m + 31 to 32 × m + 10
10110_B	Transmit buffer 32 × m + 31 to 32 × m + 9
10111_B	Transmit buffer 32 × m + 31 to 32 × m + 8
11000_B	Transmit buffer 32 × m + 31 to 32 × m + 7
11001_B	Transmit buffer 32 × m + 31 to 32 × m + 6
11010_B	Transmit buffer 32 × m + 31 to 32 × m + 5
11011_B	Transmit buffer 32 × m + 31 to 32 × m + 4
11100_B	Transmit buffer 32 × m + 31 to 32 × m + 3
11101_B	Transmit buffer 32 × m + 31 to 32 × m + 2
11110_B	Transmit buffer 32 × m + 31 to 32 × m + 1
11111_B	Transmit buffer 32 × m + 31 to 32 × m + 0

24.3.2 Details of Channel-related Registers

24.3.2.1 RCFDCnCFDCmNCFG — Channel Nominal Bit Rate Configuration Register (m = 0 to 7)

Access: RCFDCnCFDCmNCFG register can be read or written in 32-bit units

RCFDCnCFDCmNCFGL, RCFDCnCFDCmNCFGH registers can be read or written in 16-bit units

RCFDCnCFDCmNCFGLL, RCFDCnCFDCmNCFGLH, RCFDCnCFDCmNCFGHL, RCFDCnCFDCmNCFGHH registers can be read or written in 8-bit units

Address: RCFDCnCFDCmNCFG: <RCFDCn_base> + 0000_H + (10_H × m)

RCFDCnCFDCmNCFGL: <RCFDCn_base> + 0000_H + (10_H × m),

RCFDCnCFDCmNCFGH: <RCFDCn_base> + 0002_H + (10_H × m)

RCFDCnCFDCmNCFGLL: <RCFDCn_base> + 0000_H + (10_H × m),

RCFDCnCFDCmNCFGLH: <RCFDCn_base> + 0001_H + (10_H × m),

RCFDCnCFDCmNCFGHL: <RCFDCn_base> + 0002_H + (10_H × m),

RCFDCnCFDCmNCFGHH: <RCFDCn_base> + 0003_H + (10_H × m)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	NTSEG2[4:0]					—	NTSEG1[6:0]						
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NSJW[4:0]					—	NBRP[9:0]									
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 24.34 RCFDCnCFDCmNCFG Register Contents

Bit Position	Bit Name	Function
31 to 29	Reserved	These bits are read as the value after reset. The write value should be the value after reset.
28 to 24	NTSEG2[4:0]	Nominal Bit Rate Time Segment 2 Control b28 b27 b26 b25 b24 0 0 0 0 0: Setting prohibited 0 0 0 0 1: 2 Tq : : 1 1 1 1 0: 31 Tq 1 1 1 1 1: 32 Tq
23	Reserved	This bit is read as the value after reset. The write value should be the value after reset.
22 to 16	NTSEG1[6:0]	Nominal Bit Rate Time Segment 1 Control b22 b21 b20 b19 b18 b17 b16 0 0 0 0 0 0 0: Setting prohibited 0 0 0 0 0 0 1: Setting prohibited 0 0 0 0 0 1 0: Setting prohibited 0 0 0 0 0 1 1: 4 Tq : : 1 1 1 1 1 1 0: 127 Tq 1 1 1 1 1 1 1: 128 Tq

Table 24.34 RCFDCnCFDCmNCFG Register Contents

Bit Position	Bit Name	Function
15 to 11	NSJW[4:0]	Nominal Bit Rate Resynchronization Jump Width Control b15 b14 b13 b12 b11 0 0 0 0 0: 1 Tq 0 0 0 0 1: 2 Tq 0 0 0 1 0: 3 Tq : : 1 1 1 1 0: 31 Tq 1 1 1 1 1: 32 Tq
10	Reserved	This bit is read as the value after reset. The write value should be the value after reset.
9 to 0	NBRP[9:0]	Nominal Bit Rate Prescaler Division Ratio Setting When the set value = P (0 to 1023), the nominal bit rate prescaler divides fCAN by (P + 1).

Modify the RCFDCnCFDCmNCFG register in channel reset mode or channel halt mode. Set this register in channel reset mode, and then transition to channel communication mode or channel halt mode. For the description and settings for bit timing parameters, see **Section 24.10.1, Initial Settings**.

NTSEG2[4:0] Bits

These bits specify a Tq value for the length of phase segment 2 (PHASE_SEG2) of nominal bit rate.

Possible values are 2 Tq to 32 Tq, inclusive.

Set a value smaller than the value of the NTSEG1[6:0] bits.

NTSEG1[6:0] Bits

These bits specify the total length of propagation segment (PROP_SEG) and phase segment 1 (PHASE_SEG1) of nominal bit rate as a Tq value.

Possible values are 4 to 128 Tq.

NSJW[4:0] Bits

These bits specify the resynchronization jump width of nominal bit rate as a Tq value. Possible values are 1 to 32 Tq. Specify a value equal to or smaller than the NTSEG2[4:0] value.

NBRP[9:0] Bits

The clock obtained by dividing the CAN clock (fCAN) by the nominal bit rate prescaler ((NBRP[9:0]) + 1) becomes CANmTq(N) clock (fCANTQ(N)m). One clock of the CANmTq(N) clock becomes one Time Quantum (Tq).

The NBRP[9:0] value and the DBRP[7:0] value should be equal and the two corresponding bit rate values are different according to the respective segment values.

24.3.2.2 RCFDCnCFDCmCTR — Channel Control Register (m = 0 to 7)

Access: RCFDCnCFDCmCTR register can be read or written in 32-bit units

RCFDCnCFDCmCTRL, RCFDCnCFDCmCTRH registers can be read or written in 16-bit units

RCFDCnCFDCmCTRLL, RCFDCnCFDCmCTRLH, RCFDCnCFDCmCTRHL, RCFDCnCFDCmCTRHH registers can be read or written in 8-bit units

Address: RCFDCnCFDCmCTR: <RCFDCn_base> + 0004_H + (10_H × m)

RCFDCnCFDCmCTRL: <RCFDCn_base> + 0004_H + (10_H × m),

RCFDCnCFDCmCTRH: <RCFDCn_base> + 0006_H + (10_H × m)

RCFDCnCFDCmCTRLL: <RCFDCn_base> + 0004_H + (10_H × m),

RCFDCnCFDCmCTRLH: <RCFDCn_base> + 0005_H + (10_H × m),

RCFDCnCFDCmCTRHL: <RCFDCn_base> + 0006_H + (10_H × m),

RCFDCnCFDCmCTRHH: <RCFDCn_base> + 0007_H + (10_H × m)

Value after reset: $0000\ 0005_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ROM	CRCT	—	—	—	CTMS[1:0]		CTME	ERRD	BOM[1:0]		—	TDCVFIE	SOCOIE	EOCOIE	TAIE
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ALIE	BLIE	OLIE	BORIE	BOEIE	EPIE	EWIE	BEIE	—	—	—	—	RTBO	CSLPR	CHMDC[1:0]	
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Table 24.35 RCFDCnCFDCmCTR Register Contents

Bit Position	Bit Name	Function
31	ROM	Restricted Operation Mode Enable 0: Restricted operation mode is disabled. 1: Restricted operation mode is enabled.
30	CRCT	CRC Error Test Enable 0: The first bit of the reception ID field is not inverted. 1: The first bit of the reception ID field is inverted.
29 to 27	Reserved	These bits are read as the value after reset. The write value should be the value after reset.
26, 25	CTMS[1:0]	Communication Test Mode Select b26 b25 0 0: Standard test mode 0 1: Listen-only mode 1 0: Self-test mode 0 (external loopback mode) 1 1: Self-test mode 1 (internal loopback mode)
24	CTME	Communication Test Mode Enable 0: Communication test mode is disabled. 1: Communication test mode is enabled.
23	ERRD	Error Display Mode Select 0: Error flags are displayed only for the first error information after bits 14 to 8 in the RCFDCnCFDCmERFL register are all cleared. 1: Error flags for all error information are displayed.

Table 24.35 RCFDCnCFDCmCTR Register Contents

Bit Position	Bit Name	Function
22, 21	BOM[1:0]	Bus Off Recovery Mode Select b22 b21 0 0: ISO11898-1 compliant 0 1: Entry to channel halt mode automatically at bus-off entry 1 0: Entry to channel halt mode automatically at bus-off end 1 1: Entry to channel halt mode (in bus-off state) by program request
20	Reserved	These bits are read as the value after reset. The write value should be the value after reset.
19	TDCVFIE	Transmitter Delay Compensation Violation Interrupt Enable 0: A transmitter delay compensation violation interrupt is disabled. 1: A transmitter delay compensation violation interrupt is enabled.
18	SOCOIE	Successful Occurrence Counter Overflow Interrupt Enable 0: A successful occurrence counter overflow interrupt is disabled. 1: A successful occurrence counter overflow interrupt is enabled.
17	EOCOIE	Error Occurrence Counter Overflow Interrupt Enable 0: An error occurrence counter overflow interrupt is disabled. 1: An error occurrence counter overflow interrupt is enabled.
16	TAIE	Transmit Abort Interrupt Enable 0: Transmit abort interrupt is disabled. 1: Transmit abort interrupt is enabled.
15	ALIE	Arbitration Lost Interrupt Enable 0: Arbitration lost interrupt is disabled. 1: Arbitration lost interrupt is enabled.
14	BLIE	Bus Lock Interrupt Enable 0: Bus lock interrupt is disabled. 1: Bus lock interrupt is enabled.
13	OLIE	Overload Frame Transmit Interrupt Enable 0: Overload frame transmit interrupt is disabled. 1: Overload frame transmit interrupt is enabled.
12	BORIE	Bus Off Recovery Interrupt Enable 0: Bus off recovery interrupt is disabled. 1: Bus off recovery interrupt is enabled.
11	BOEIE	Bus Off Entry Interrupt Enable 0: Bus off entry interrupt is disabled. 1: Bus off entry interrupt is enabled.
10	EPIE	Error Passive Interrupt Enable 0: Error passive interrupt is disabled. 1: Error passive interrupt is enabled.
9	EWIE	Error Warning Interrupt Enable 0: Error warning interrupt is disabled. 1: Error warning interrupt is enabled.
8	BEIE	Bus Error Interrupt Enable 0: Bus error interrupt is disabled. 1: Bus error interrupt is enabled.
7 to 4	Reserved	These bits are read as the value after reset. The write value should be the value after reset.
3	RTBO	Forcible Return from Bus-off When this bit is set to 1, forcible return from the bus off state is made. This bit is always read as 0.

Table 24.35 RCFDCnCFDCmCTR Register Contents

Bit Position	Bit Name	Function
2	CSLPR	Channel Stop Mode 0: Other than channel stop mode 1: Channel stop mode
1, 0	CHMDC[1:0]	Mode Select b1 b0 0 0: Channel communication mode 0 1: Channel reset mode 1 0: Channel halt mode 1 1: Setting prohibited

ROM Bit

When the ROM bit and the CTME bit in the RCFDCnCFDCmCTR register are set to 1, restricted operation mode is enabled. Use the restricted operation mode only when the CTMS[1:0] value in the RCFDCnCFDCmCTR register is 00_B (standard test mode). Modify this bit only in channel halt mode.

This bit is always 0 in channel reset mode.

CRCT Bit

This bit is used to test the CRC generation circuit in the RS-CANFD module. Setting this bit to 1 inverts the first bit of the ID field when a message is received. With this inversion of bit, the CRC calculation result does not match the normal CRC value of the received frame, which can detect a CRC error (the CERR bit in the RCFDCnCFDCmERFL register is 1). When using this function, note the following.

- This function is available while the CTME bit in the RCFDCnCFDCmCTR register is 1 (communication test mode enabled).
- This function cannot communicate with other CAN nodes. Use this function for inter-channel communication test (the CmICBCE bit in the RCFDCnCFDGTSTCFG register is 1).
- Bit inversion in the ID field may cause bit stuffing rule violation. In that case, no CRC error is detected but a stuff error is detected.

Modify this bit only in channel halt mode. This bit is set to 0 in channel reset mode.

CTMS[1:0] Bits

These bits are used to select a communication test mode. Modify these bits in channel halt mode only. These bits are set to 0 in channel reset mode.

CTME Bit

Setting this bit to 1 enables communication test mode. Modify these bits in channel halt mode. This bit is set to 0 in channel reset mode.

ERRD Bit

This bit is used to control the display mode of bits 14 to 8 in the RCFDCnCFDCmERFL register. When this bit is clear to 0, if any error is detected while the flags of bits 14 to 8 in the RCFDCnCFDCmERFL register are all 0, only the flags of the first error event are set to 1. If two or more errors occur in the first error event, all the flags of the detected errors are set to 1.

When this bit is set to 1, all the flags of errors that have occurred are set to 1 regardless of the error occurrence order.

Modify this bit only in channel reset mode or channel halt mode.

BOM[1:0] Bits

These bits are used to select the bus off recovery mode of the RS-CANFD module.

When the BOM[1:0] bits are set to 00_B, return from the bus off state to the error active state is compliant with the CAN specifications. That is, the RS-CANFD module reenters the CAN communication (error active state) after 11 consecutive recessive bits are detected 128 times. A bus off recovery interrupt request is generated at the time of return from the bus off state. Even if the CHMDC[1:0] bits are set to 10_B (channel halt mode) before recessive bits are detected 128 times, the RS-CANFD module does not transition to channel halt mode until recessive bits are detected 128 times.

When the RS-CANFD module reaches the bus off state when the BOM[1:0] bits are set to 01_B, the CHMDC[1:0] bits in the RCFDCnCFDCmCTR register (m = 0 to 7) are set to 10_B and the RS-CANFD module transitions to channel halt mode. No bus off recovery interrupt request is generated and the TEC[7:0] and REC[7:0] bits in the RCFDCnCFDCmSTS register are cleared to 00_H.

When the RS-CANFD module reaches the bus off state when the BOM[1:0] bits are set to 10_B, the CHMDC[1:0] bits are set to 10_B and the RS-CANFD module transitions to channel halt mode after return from the bus off state (11 consecutive recessive bits are detected 128 times). A bus off recovery interrupt request is generated at the time of return from the bus off state and the TEC[7:0] and REC[7:0] bits are cleared to 00_H.

When the BOM[1:0] bits are set to 11_B and the CHMDC[1:0] bits are set to 10_B while the RS-CANFD module is in the bus off state, the RS-CANFD module transitions to channel halt mode. No bus off recovery interrupt request is generated at the time of return from the bus off state and the TEC[7:0] and REC[7:0] bits are cleared to 00_H. However, if 11 consecutive recessive bits are detected 128 times and the RS-CANFD module has recovered to the error active state from the bus off state before the CHMDC[1:0] bits are set to 10_B, a bus off recovery interrupt request is generated.

If a program writes to the CHMDC[1:0] bit at the same time as the RS-CANFD module transition to channel halt mode (at bus off entry when the BOM[1:0] bits are 01_B or at bus off end when the BOM[1:0] bits are 10_B), the program's writing takes precedence. Modify the BOM[1:0] bits only in channel reset mode.

TDCVFIE Bit

When the TDCVF flag in the RCFDCnCFDCmFDSTS register is set to 1 after the TDCVFIE bit is set to 1, an interrupt request occurs. Modify this bit only in channel reset mode.

SOCOIE Bit

When the SOCO flag in the RCFDCnCFDCmFDSTS register is set to 1 after the SOCOIE bit is set to 1, an interrupt request occurs. Modify this bit only in channel reset mode.

EOCOIE Bit

When the EOCO flag in the RCFDCnCFDCmFDSTS register is set to 1 after the EOCOIE bit is set to 1, an interrupt request occurs. Modify this bit only in channel reset mode.

TAIE Bit

When transmit abort of the transmit buffer is completed with the TAIE bit set to 1, an interrupt request is generated. Modify this bit only in channel reset mode.

ALIE Bit

When the ALF flag in the RCFDCnCFDCmERFL register is set to 1 with the ALIE bit set to 1, an error interrupt request is generated. Modify this bit only in channel reset mode.

BLIE Bit

When the BLF flag in the RCFDCnCFDCmERFL register is set to 1 with the BLIE bit set to 1, an error interrupt request is generated. Modify this bit only in channel reset mode.

OLIE Bit

When the OVLF flag in the RCFDCnCFDCmERFL register is set to 1 with the OLIE bit set to 1, an error interrupt request is generated. Modify this bit only in channel reset mode.

BORIE Bit

When the BORF flag in the RCFDCnCFDCmERFL register is set to 1 with the BORIE bit set to 1, an error interrupt request is generated. Modify this bit only in channel reset mode.

BOEIE Bit

When the BOEF flag in the RCFDCnCFDCmERFL register is set to 1 with the BOEIE bit set to 1, an error interrupt request is generated. Modify this bit only in channel reset mode.

EPIE Bit

When the EPF flag in the RCFDCnCFDCmERFL register is set to 1 with the EPIE bit set to 1, an error interrupt request is generated. Modify this bit only in channel reset mode.

EWIE Bit

When the EWF flag in the RCFDCnCFDCmERFL register is set to 1 with the EWIE bit set to 1, an error interrupt request is generated. Modify this bit only in channel reset mode.

BEIE Bit

When the BEF flag in the RCFDCnCFDCmERFL register is set to 1 with the BEIE bit set to 1, an error interrupt request is generated. Modify this bit only in channel reset mode.

RTBO Bit

Setting this bit to 1 in the bus off state forcibly returns from the bus off state to the error active state. This bit is automatically cleared to 0. Setting this bit to 1 clears the TEC[7:0] and REC[7:0] bits in the RCFDCnCFDCmSTS register to 00_H and also clears the BOSTS flag in the RCFDCnCFDCmSTS register to 0 (not in bus off state). The other registers remain unchanged. No bus off recovery interrupt request is generated upon return from the bus off state in this case. Use this bit only when the BOM[1:0] bits in the RCFDCnCFDCmCTR register are 00_B (ISO11898-1 compliant). A delay of up to 1 CAN bit time occurs after the RTBO bit is set to 1 until the RS-CANFD module transitions to the error active state. Set this bit to 1 in channel communication mode.

CSLPR Bit

Setting this bit to 1 places the channel into channel stop mode. Clearing this bit to 0 makes the channel exit channel stop mode.

This bit should not be modified in channel communication mode or channel halt mode.

CHMDC[1:0] Bits

These bits are used to select a channel mode (channel communication mode, channel reset mode, or channel halt mode). For details, see **Section 24.5.2, Channel Modes**. Setting the CSLPR bit to 1 in channel reset mode allows transition to channel stop mode. Do not set the CHMDC[1:0] bits to 11_B.

When the CAN module has automatically transitioned to channel halt mode based on the setting of the BOM[1:0] bits, the CHMDC[1:0] bits are automatically set to 10_B.

24.3.2.3 RCFDCnCFDCmSTS — Channel Status Register (m = 0 to 7)

Access: RCFDCnCFDCmSTS register can be read or written in 32-bit units

RCFDCnCFDCmSTSL register can be read or written in 16-bit units

RCFDCnCFDCmSTSH register is a read-only register that can be read in 16-bit units

RCFDCnCFDCmSTSLL register is a read-only register that can be read in 8-bit units

RCFDCnCFDCmSTSLH register can be read or written in 8-bit units

RCFDCnCFDCmSTSHL, RCFDCnCFDCmSTSHH registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDCmSTS: <RCFDCn_base> + 0008_H + (10_H × m)

RCFDCnCFDCmSTSL: <RCFDCn_base> + 0008_H + (10_H × m),

RCFDCnCFDCmSTSH: <RCFDCn_base> + $000A_H$ + (10_H × m)

RCFDCnCFDCmSTSLL: <RCFDCn_base> + 0008_H + (10_H × m),

RCFDCnCFDCmSTSLH: <RCFDCn_base> + 0009_H + (10_H × m),

RCFDCnCFDCmSTSHL: <RCFDCn_base> + $000A_H$ + (10_H × m),

RCFDCnCFDCmSTSHH: <RCFDCn_base> + $000B_H$ + (10_H × m)

Value after reset: $0000\ 0005_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TEC[7:0]								REC[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	ESIF	COMSTS	RECSTS	TRMSTS	BOSTS	EPSTS	CSLPSTS	CHLTSTS	CRSTSTS
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
R/W	R	R	R	R	R	R	R	R/W*1	R	R	R	R	R	R	R	R

Note 1. The only effective value for writing to this flag bit is 0, which clears the bit. Otherwise writing to the bit results in retention of its state.

Table 24.36 RCFDCnCFDCmSTS Register Contents

Bit Position	Bit Name	Function
31 to 24	TEC[7:0]	The transmit error counter (TEC) can be read.
23 to 16	REC[7:0]	The receive error counter (REC) can be read.
15 to 9	Reserved	These bits are read as the value after reset. The write value should be the value after reset.
8	ESIF	Error State Indication Flag 0: No CAN FD message whose ESI bit is recessive has been received. 1: At least one CAN FD message whose ESI bit is recessive has been received.
7	COMSTS	Communication Status Flag 0: Communication is not ready. 1: Communication is ready.
6	RECSTS	Receive Status Flag 0: Bus idle, in transmission or bus off state 1: In reception
5	TRMSTS	Transmit Status Flag 0: Bus idle or in reception 1: In transmission or bus off state
4	BOSTS	Bus Off Status Flag 0: Not in bus off state 1: In bus off state

Table 24.36 RCFDCnCFDCmSTS Register Contents

Bit Position	Bit Name	Function
3	EPSTS	Error Passive Status Flag 0: Not in error passive state 1: In error passive state
2	CSLPSTS	Channel Stop Status Flag 0: Not in channel stop mode 1: In channel stop mode
1	CHLTSTS	Channel Halt Status Flag 0: Not in channel halt mode 1: In channel halt mode
0	CRSTSTS	Channel Reset Status Flag 0: Not in channel reset mode 1: In channel reset mode

TEC[7:0] Bits

These bits contain the transmit error counter value. For transmit error counter increment/decrement conditions, see the CAN specification (ISO11898-1).

These bits are cleared to 0 in channel reset mode.

REC[7:0] Bits

These bits contain the receive error counter value. For receive error counter increment/decrement conditions, see the CAN specifications (ISO11898-1).

These bits are cleared to 0 in channel reset mode.

ESIF Flag

When the recessive ESI bit is detected in a successfully received message, this flag is set to 1. In loopback mode or mirror mode, the own transmission message is regarded as a received message. To clear this flag to 0, write 0 to this bit by the program. This bit cannot be set to 1 by the program. If the flag setting (to 1) timing matches the writing 0 (by the program) timing, this flag is set to 1.

This flag is set to 0 in channel reset mode.

COMSTS Flag

This bit indicates that communication is ready.

This flag is set to 1 when the CAN module has detected 11 consecutive recessive bits after it has transitioned from channel reset mode or channel halt mode to channel communication mode. This flag is cleared to 0 in channel reset mode or channel halt mode.

RECSTS Flag

This flag is set to 1 when reception has started, and is cleared to 0 when the bus has become idle or transmission has started.

TRMSTS Flag

This flag is set to 1 when transmission has started, and is cleared to 0 when the bus has become idle or reception has started. This flag remains 1 in the bus off state.

BOSTS Flag

This flag is set to 1 when the bus off state (TEC[7:0] > 255) is entered. It is cleared to 0 when the CAN module has exited the bus off state.

EPSTS Flag

This flag is set to 1 when the RS-CANFD module has entered the error passive state ((128 ≤ TEC[7:0] ≤ 255) or (128 ≤ REC[7:0])), It is cleared to 0 when the RS-CANFD module has exited the error passive state or has entered channel reset mode.

CSLPSTS Flag

This flag is set to 1 when the CAN module has transitioned to channel stop mode, and is cleared to 0 when the CAN module has returned from channel stop mode.

CHLTSTS Flag

This flag is set to 1 when the CAN module has transitioned to channel halt mode, and is cleared to 0 when the CAN module has returned from channel halt mode.

CRSTSTS Flag

This flag is set to 1 when the CAN module has transitioned to channel reset mode, and is cleared to 0 when the CAN module has transitioned to channel communication mode or channel halt mode. This flag remains 1 when the CAN module transitions from channel reset mode to channel stop mode.

24.3.2.4 RCFDCnCFDCmERFL — Channel Error Flag Register (m = 0 to 7)

Access: RCFDCnCFDCmERFL register can be read or written in 32-bit units

RCFDCnCFDCmERFLL register can be read or written in 16-bit units

RCFDCnCFDCmERFLH register is a read-only register that can be read in 16-bit units

RCFDCnCFDCmERFLLL, RCFDCnCFDCmERFLLH registers can be read or written in 8-bit units

RCFDCnCFDCmERFLHL, RCFDCnCFDCmERFLHH registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDCmERFL: <RCFDCn_base> + $000C_H$ + (10_H × m)

RCFDCnCFDCmERFLL: <RCFDCn_base> + $000C_H$ + (10_H × m),

RCFDCnCFDCmERFLH: <RCFDCn_base> + $000E_H$ + (10_H × m)

RCFDCnCFDCmERFLLL: <RCFDCn_base> + $000C_H$ + (10_H × m),

RCFDCnCFDCmERFLLH: <RCFDCn_base> + $000D_H$ + (10_H × m),

RCFDCnCFDCmERFLHL: <RCFDCn_base> + $000E_H$ + (10_H × m),

RCFDCnCFDCmERFLHH: <RCFDCn_base> + $000F_H$ + (10_H × m)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	CRCREG[14:0]														
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	ADERR	B0ERR	B1ERR	CERR	AERR	FERR	SERR	ALF	BLF	OVLF	BORF	BOEF	EPF	EWF	BEF
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1

Note 1. The only effective value for writing to this flag bit is 0, which clears the bit. Otherwise writing to the bit results in retention of its state.

Table 24.37 RCFDCnCFDCmERFL Register Contents

Bit Position	Bit Name	Function
31	Reserved	When read, the value after reset is returned. When writing to this bit, write the value after reset.
30 to 16	CRCREG[14:0]	CRC Calculation Data (CRC length:15 bits) A CRC value calculated based on the transmit message or receive message is indicated.
15	Reserved	When read, the value after reset is returned. When writing to this bit, write the value after reset.
14	ADERR	ACK Delimiter Error Flag 0: No ACK delimiter error is detected. 1: ACK delimiter error is detected.
13	B0ERR	Dominant Bit Error Flag 0: No dominant bit error is detected. 1: Dominant bit error is detected.
12	B1ERR	Recessive Bit Error Flag 0: No recessive bit error is detected. 1: Recessive bit error is detected.
11	CERR	CRC Error Flag 0: No CRC error is detected. 1: CRC error is detected.
10	AERR	ACK Error Flag 0: No ACK error is detected. 1: ACK error is detected.

Table 24.37 RCFDCnCFDCmERFL Register Contents

Bit Position	Bit Name	Function
9	FERR	Form Error Flag 0: No form error is detected. 1: Form error is detected.
8	SERR	Stuff Error Flag 0: No stuff error is detected. 1: Stuff error is detected.
7	ALF	Arbitration-lost Flag 0: No arbitration-lost is detected. 1: Arbitration-lost is detected.
6	BLF	Bus Lock Flag 0: No channel bus lock is detected. 1: Channel bus lock is detected.
5	OVLF	Overload Flag 0: No overload is detected. 1: Overload is detected.
4	BORF	Bus Off Recovery Flag 0: No bus off recovery is detected. 1: Bus off recovery is detected.
3	BOEF	Bus Off Entry Flag 0: No bus off entry is detected. 1: Bus off entry is detected.
2	EPF	Error Passive Flag 0: No error passive is detected. 1: Error passive is detected.
1	EWF	Error Warning Flag 0: No error warning is detected. 1: Error warning is detected.
0	BEF	Bus Error Flag 0: No channel bus error is detected. 1: Channel bus error is detected.

See the CAN specification (ISO11898-1) for a description of error occurrence conditions. To clear each flag of this register, the program must write a 0 to the corresponding bit. These flags cannot be set to 1 by the program. If any of these flags is set to 1 at the same time that the program writes 0 to the flag, the flag is set to 1. Transition to channel reset mode resets these flags to 0.

If the ERRD bit in the RCFDCnCFDCmCTR register is set to 0 (ie, only the flags for the first error event are displayed) and an error related to bits 14 to 8 of RCFDCnCFDCmERFL is detected, the flag bits are only set to 1 by the error event if bits 14 to 8 were all 0 at the time when the error occurred.

CRCREG[14:0] Flag

When the CTME bit in the RCFDCnCFDCmCTR register is set to 1 (communication test mode is enabled), if transmit or receive message is a classical CAN frame (CRC length = 15 bits), this flag is updated and the CRC value calculated based on the message can be read. When a CAN FD frame is sent or received, the value of CRCREG[20:0] bits in the RCFDCnCFDCmFDCRC register is updated. When the CTME bit is set to 0 (communication test mode is disabled), these bits are always read as 0.

This bit is always 0 in channel reset mode.

ADERR Flag

This flag is set to 1 when a form error has been detected in the ACK delimiter during transmission.

B0ERR Flag

This flag is set to 1 when a recessive bit has been detected even though a dominant bit was transmitted.

B1ERR Flag

This flag is set to 1 when a dominant bit has been detected even though a recessive bit was transmitted.

CERR Flag

This flag is set to 1 when a CRC error has been detected.

AERR Flag

This flag is set to 1 when an ACK error has been detected.

FERR Flag

This flag is set to 1 when a form error has been detected.

SERR Flag

This flag is set to 1 when a stuff error has been detected.

ALF Flag

This flag is set to 1 when an arbitration-lost has been detected.

BLF Flag

This flag is set to 1 when 32 consecutive dominant bits have been detected on the CAN bus in channel communication mode. After that, detection of bus lock is restarted when either of the following conditions is met.

- A recessive bit is detected after the BLF bit has been cleared from 1 to 0.
- The CAN module transitions to channel reset mode and returns to channel communication mode after the BLF bit has been cleared from 1 to 0.

OVLF Flag

This flag is set to 1 when the overload frame transmit condition has been detected when performing reception or transmission.

BORF Flag

This flag is set to 1 when 11 consecutive recessive bits have been detected 128 times and the CAN module returns from the bus off state. However, this flag is not set to 1 if the CAN module returns from the bus off state in any of the following ways before 11 consecutive recessive bits are detected 128 times.

- The CHMDC[1:0] bits in the RCFDCnCFDCmCTR register are set to 01_B (channel reset mode).
- The RTBO bit in the RCFDCnCFDCmCTR register is set to 1 (forcible return from the bus off state).
- The BOM[1:0] bits in the RCFDCnCFDCmCTR register are set to 01_B (transition to channel halt mode at bus off entry).

- The CHMDC[1:0] bits in the RCFDCnCFDCmCTR register are set to 10_B (channel halt mode) before 11 consecutive recessive bits are detected 128 times with the BOM[1:0] bits set to 11_B (transition to channel halt mode upon a request from the program during bus off).

BOEF Flag

This flag is set to 1 when the bus off state is entered (TEC[7:0] value > 255). This flag is also set to 1 if the bus off state is entered when the BOM[1:0] bits in the RCFDCnCFDCmCTR register (m = 0 to 7) are set to 01_B (transition to channel halt mode at bus off entry).

EPF Flag

This flag is set to 1 when the error passive state is entered ((128 ≤ TEC[7:0] ≤ 255) or (128 ≤ REC[7:0])). This flag is set to 1 only when the REC[7:0] or TEC[7:0] value first exceeds 127. Therefore, if the program writes 0 to this flag while the value of REC[7:0] or TEC[7:0] remains over 127, this bit is not set to 1 until both REC [7:0] and TEC[7:0] values become 127 or less and then the REC[7:0] or TEC[7:0] value exceeds 127 again.

EWF Flag

This flag is set to 1 only when the REC[7:0] or TEC[7:0] value first exceeds 95. Therefore, if the program writes 0 to this flag while the value of REC[7:0] or TEC[7:0] remains over 95, this bit is not set to 1 until both REC [7:0] and TEC[7:0] values become 95 or less and then the REC[7:0] or TEC[7:0] value exceeds 95 again.

BEF Flag

This flag is set to 1 when any one of the ADERR, B0ERR, B1ERR, CERR, AERR, FERR, and SERR flags in the RCFDCnCFDCmERFL register is set to 1.

NOTE

To clear the flag of this register to 0, use a store instruction to write “0” to the given flag and “1” to the other flags.

24.3.2.5 RCFDCnCFDCmDCFG — Channel Data Bit Rate Configuration Register (m = 0 to 7)

Access: RCFDCnCFDCmDCFG register can be read or written in 32-bit units

RCFDCnCFDCmDCFGL, RCFDCnCFDCmDCFGH registers can be read or written in 16-bit units

RCFDCnCFDCmDCFGLL, RCFDCnCFDCmDCFGHL, RCFDCnCFDCmDCFGHH registers can be read or written in 8-bit units

Address: RCFDCnCFDCmDCFG: <RCFDCn_base> + 0700_H + (20_H × m)

RCFDCnCFDCmDCFGL: <RCFDCn_base> + 0700_H + (20_H × m),

RCFDCnCFDCmDCFGH: <RCFDCn_base> + 0702_H + (20_H × m)

RCFDCnCFDCmDCFGLL: <RCFDCn_base> + 0700_H + (20_H × m),

RCFDCnCFDCmDCFGHL: <RCFDCn_base> + 0702_H + (20_H × m),

RCFDCnCFDCmDCFGHH: <RCFDCn_base> + 0703_H + (20_H × m)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	DSJW[2:0]			—	DTSEG2[2:0]			DTSEG1[3:0]			
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DBRP[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 24.38 RCFDCnCFDCmDCFG Register Contents

Bit Position	Bit Name	Function
31 to 27	Reserved	These bits are read as the value after reset. The write value should be the value after reset.
26 to 24	DSJW[2:0]	Data Bit Rate Resynchronization Jump Width Control b26 b25 b24 0 0 0: 1 Tq 0 0 1: 2 Tq 0 1 0: 3 Tq 0 1 1: 4 Tq 1 0 0: 5 Tq 1 0 1: 6 Tq 1 1 0: 7 Tq 1 1 1: 8 Tq
23	Reserved	This bit is read as the value after reset. The write value should be the value after reset.
22 to 20	DTSEG2[2:0]	Data Bit Rate Time Segment 2 Control b22 b21 b20 0 0 0: Setting prohibited 0 0 1: 2 Tq 0 1 0: 3 Tq 0 1 1: 4 Tq 1 0 0: 5 Tq 1 0 1: 6 Tq 1 1 0: 7 Tq 1 1 1: 8 Tq

Table 24.38 RCFDCnCFDCmDCFG Register Contents

Bit Position	Bit Name	Function
19 to 16	DTSEG1[3:0]	Data Bit Rate Time Segment 1 Control b19 b18 b17 b16 0 0 0 0: Setting prohibited 0 0 0 1: 2 Tq 0 0 1 0: 3 Tq 0 0 1 1: 4 Tq 0 1 0 0: 5 Tq 0 1 0 1: 6 Tq 0 1 1 0: 7 Tq 0 1 1 1: 8 Tq 1 0 0 0: 9 Tq 1 0 0 1: 10 Tq 1 0 1 0: 11 Tq 1 0 1 1: 12 Tq 1 1 0 0: 13 Tq 1 1 0 1: 14 Tq 1 1 1 0: 15 Tq 1 1 1 1: 16 Tq
15 to 8	Reserved	These bits are read as the value after reset. The write value should be the value after reset.
7 to 0	DBRP[7:0]	Data Bit Rate Prescaler Division Ratio Setting When the set value = P (0 to 255), the data bit rate prescaler divides fCAN by (P + 1).

Modify the RCFDCnCFDCmDCFG register in channel reset mode or channel halt mode. Set this register in channel reset mode, and then transition to channel communication mode or channel halt mode. When only classical CAN frames are used in CAN FD mode, set the RCFDCnCFDCmDCFG register to the value equal to the set RCFDCnCFDCmNCFG register value. For the description and settings of bit timing parameters, see **Section 24.10.1, Initial Settings**.

The channel of Classical only mode does not have to perform the configuration of this register.

DSJW[2:0] Bits

These bits specify the resynchronization jump width of data bit rate as a Tq value. Possible values are 1 to 8 Tq. Specify a value equal to or smaller than the DTSEG2[2:0] bits value.

DTSEG2[2:0] Bits

These bits are used to specify a Tq value for the length of phase segment 2 (PHASE_SEG2) of nominal bit rate.

Possible values are 2 to 8 Tq.

Set a value less than or equal to the value of the DTSEG1[3:0] bits.

DTSEG1[3:0] Bits

These bits specify the total length of propagation segment (PROP_SEG) and phase segment 1 (PHASE_SEG1) of data bit rate as a Tq value.

Possible values are 2 to 16 Tq.

DBRP[7:0] Bits

The clock obtained by dividing the CAN clock (fCAN) by the data bit rate prescaler ((DBRP[7:0]) + 1) becomes CANmTq(D) clock (fCANTQ(D)m). One clock of the CANmTq(D) clock becomes one Time Quantum (Tq).

Be sure to specify the same value for both NBRP[9:0] and DBRP[7:0].

To specify different values for the nominal bit rate and the data bit rate, change the values of the RCFDCnCFDCmNCFG.NTSEG1 and NTSEG2 bits and RCFDCnCFDCmDCFG.DTSEG1 and DTSEG2 bits, respectively.

When the TDCE bit is set to 1(Transmitter delay compensation is enabled) in the RCFDCnCFDCmFDCFG register, set the equal value of 1 or less to the bits NBRP[9:0] and DBRP[7:0].

24.3.2.6 RCFDCnCFDCmFDCFG — Channel CAN FD Configuration Register (m = 0 to 7)

Access: RCFDCnCFDCmFDCFG register can be read or written in 32-bit units

RCFDCnCFDCmFDCFGL, RCFDCnCFDCmFDCFGH registers can be read or written in 16-bit units

RCFDCnCFDCmFDCFGLL, RCFDCnCFDCmFDCFGLH, RCFDCnCFDCmFDCFGHL, RCFDCnCFDCmFDCFGHH registers can be read or written in 8-bit units

Address: RCFDCnCFDCmFDCFG: <RCFDCn_base> + 0704_H + (20_H × m)

RCFDCnCFDCmFDCFGL: <RCFDCn_base> + 0704_H + (20_H × m),

RCFDCnCFDCmFDCFGH: <RCFDCn_base> + 0706_H + (20_H × m)

RCFDCnCFDCmFDCFGLL: <RCFDCn_base> + 0704_H + (20_H × m),

RCFDCnCFDCmFDCFGLH: <RCFDCn_base> + 0705_H + (20_H × m),

RCFDCnCFDCmFDCFGHL: <RCFDCn_base> + 0706_H + (20_H × m),

RCFDCnCFDCmFDCFGHH: <RCFDCn_base> + 0707_H + (20_H × m)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	CLOE	REFE	FDOE	—	GWBRS	GWFDF	GWEN	—	TDCO[6:0]						
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	ESIC	TDCE	TDCOC	—	—	—	—	—	EOCCFG[2:0]		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

Table 24.39 RCFDCnCFDCmFDCFG Register Contents

Bit Position	Bit Name	Function
31	Reserved	This bit is read as the value after reset. The write value should be the value after reset.
30	CLOE	Classical CAN only mode enable bit 0: Classical CAN only mode is disabled 1: Classical CAN only mode is enabled
29	REFE	Reception data edge filter enable bit 0: Reception data edge filter is disabled 1: Reception data edge filter is enabled
28	FDOE	FD-only mode enable bit 0: FD-only mode is disabled 1: FD-only mode is enabled
27	Reserved	This bit is read as the value after reset. The write value should be the value after reset.
26	GWBRS	Gateway BRS 0: A frame is transmitted with the BRS bit in the received frame set to 0. 1: A frame is transmitted with the BRS bit in the received frame set to 1.
25	GWFDF	Gateway FDF 0: A frame is transmitted regarding the received frame as a classical CAN frame. 1: A frame is transmitted regarding the received frame as a CAN FD frame.
24	GWEN	CAN-CAN FD Gateway Enable 0: The CAN-CAN FD gateway is disabled. 1: The CAN-CAN FD gateway is enabled.
23	Reserved	This bit is read as the value after reset. The write value should be the value after reset.

Table 24.39 RCFDCnCFDCmFDCFG Register Contents

Bit Position	Bit Name	Function
22 to 16	TDCO[6:0]	Transmitter Delay Compensation Offset These bits are set to the transmitter delay compensation offset value.
15 to 11	Reserved	These bits are read as the value after reset. The write value should be the value after reset.
10	ESIC	Error State Display Mode Select 0: Always displays the node error state. 1: When the node is not in the error passive state: Displays the message buffer error state. When the node is in the error passive state: Displays the node error state.
9	TDCE	Transmitter Delay Compensation Enable 0: Transmitter delay compensation is disabled. 1: Transmitter delay compensation is enabled.
8	TDCOC	Transmitter Delay Compensation Measurement Select 0: Measurement and offset 1: Only offset
7 to 3	Reserved	These bits are read as the value after reset. The write value should be the value after reset.
2 to 0	EOCCFG[2:0]	Error Occurrence Counting Method Select b2 b1 b0 0 0 0: All transmit messages and receive messages 0 0 1: All transmit messages 0 1 0: All receive messages 0 1 1: Setting prohibited 1 0 0: Only data phase of transmitted or received CAN FD message 1 0 1: Only data phase of transmitted CAN FD message 1 1 0: Only data phase of received CAN FD message 1 1 1: Setting prohibited

CLOE Bit

Setting this bit to 1 enables Classical CAN only mode. When data is transmitted, a classical CAN frame will be sent. When a CAN FD frame is received, a form error or a CRC error is detected.

Modify this bit only in channel reset mode.

Do not set RCFDCnCFDCmFDCFG.CLOE and RCFDCnCFDCmFDCFG.FDOE simultaneously.

CLOE Bit	FDOE Bit	Interface Mode
0	0	CAN-FD mode
0	1	FD only mode
1	0	Classical CAN only mode
1	1	Reserved

REFE Bit

Setting this bit to 1 enables reception data edge filtering when the idle condition is detected, and a dominant level with less than 2 time quanta is ignored. A dominant level with more than or equal to 2 time quanta is detected as an edge. Modify this bit only in channel reset mode.

Setting this bit to 0 when using in Classical CAN only mode.

FDOE Bit

Setting this bit to 1 enables FD-only mode. When data is transmitted, a CAN FD frame will be sent regardless of the settings to the CFFDF bit in the RCFDCnCFDCFFDCSTSk register or the TMFDF bit in the RCFDCnCFDTMFDCTRp register. When a classical CAN frame is received, a form error is detected. Modify this bit only in channel reset mode.

In case a Classical frame is confiured for transmitting, the FDF bit is sent as recessive, so a FD frame is sent.

If the DLC is configured bigger than 8, the remaining data bytes are padded with CCh.

Do not set RCFDCnCFDCmFDCFG.CLOE and RCFDCnCFDCmFDCFG.FDOE simultaneously.

GWBRS Bit

When the GWEN bit is 1, the BRS bit in a CAN FD frame to be transmitted by the gateway function is set.

When the GWFDF bit is set to 0, write 0 to this bit. Modify this bit only in channel reset mode.

GWFDF Bit

When the GWEN bit is 1, the FDF bit in a CAN FD frame to be transmitted by the gateway function is set. Modify this bit only in channel reset mode.

GWEN Bit

This bit is used to control the operation of the transmit/receive FIFO buffer with the CFM[1:0] bits in the RCFDCnCFDCFCCk register set to 10_B (gateway mode).

Setting this bit to 1 enables the CAN-CAN FD gateway, enabling transmission in a format different from that of frames received by the gateway function. Received frames are replaced in accordance with the settings of the GWFDF bit and the GWBRS bit. When the DLC value in the received classical CAN frame is 1001_B or more and the GWFDF bit is set to 1 (CAN FD frame), the DLC value is replaced with 1000_B. When the received CAN-FD frame is more than 1001B, and GWFDF bit is set to 0(classical CAN frame), the payload size is cut down to 8 byte. Only 8 bytes of top data performs GW transmission, and the remaining byte cancels it.

While this bit is set to 1, do not perform routing the following frames by using the gateway function.

- Remote frames

Modify this bit only in channel reset mode.

Table 24.40, Operation when the CAN-CAN FD Gateway is Enabled shows the settings and formats of transmit frame and receive frame while the CAN- CAN FD gateway is enabled.

Table 24.40 Operation when the CAN-CAN FD Gateway is Enabled

Receive Frame				Transmit Frame		
Format	BRS Bit	Received DLC Value	GWFDF Bit	Format	BRS Bit	DLC Value to be Transmitted
Classical CAN	None	DLC ≤ 1000_B	0	Classical CAN	None	Not replaced
		DLC > 1000_B				
CAN FD	Arbitrary	DLC ≤ 1000_B				
		DLC > 1000_B				Replaced with 1000_B
Classical CAN	None	DLC ≤ 1000_B	1	CAN FD	According to GWBRS bit setting	Not replaced
		DLC >1000_B				Replaced with 1000_B
CAN FD	Arbitrary	DLC ≤ 1000_B				Not replaced
		DLC > 1000_B				

TDCO[6:0] Bits

These bits set the SSP offset value. How to use this value depends on the TDCOC bit in the RCFDCnCFDCmFDCFG register.

These bits are based on CAN clock frequency(fCAN).

When the TDCOC bit is set to 0, the transmitter delay compensation result equals to the total value of the measured delay value and the TDCO[6:0] value (rounded down to the nearest integer Tq).

When the TDCOC bit is set to 1, the transmitter delay compensation result equals to the TDCO[6:0] value.

The SSP offset value = (set value of TDCO[6:0] bits + 1).

Modify these bits only in channel reset mode or channel halt mode.

ESIC Bit

When the ESIC bit is set to 1, if the channel is in the error active state, the ESI bit value (CFESI bit in the RCFDCnCFDCFFDCSTSk register or TMESI bit in the RCFDCnCFDTMFDCTRp register) set in the transmit/receive FIFO buffer or transmit buffer is transmitted as an ESI bit value of the transmit message. When the channel is in the error passive state or the ESIC bit is set to 0, the channel status is transmitted as an ESI bit value. Modify this bit only in channel reset mode or channel halt mode

Table 24.41 ESI Value to Be Transmitted

ESIC Bit	Channel Status	ESI Value to be Transmitted
0	Error active	0 (error active node)
	Error passive	1 (error passive node)
1	Error active	ESI value set in the transmit/receive FIFO buffer or transmit buffer (CFESI bit in the RCFDCnCFDCFFDCSTSk register or TMESI bit in the RCFDCnCFDTMFDCTRp register)
	Error passive	1 (error passive node)

TDCE Bit

Setting this bit to 1 enables transmitter delay compensation. Modify this bit only in channel reset mode or channel halt mode.

TDCOC Bit

When this bit is set to 0, the SSP position is defined by the total of the measured delay value and the SSP offset value (fixed value).

When this bit is set to 1, the SSP position is defined only by the SSP offset value. Modify this bit only in channel reset mode or channel halt mode.

EOCCFG[2:0] Bits

These bits are used to select a frame format and a transmission/reception direction when the error occurrence counter counts CAN bus errors.

Modify these bits only in channel reset mode or channel halt mode.

24.3.2.7 RCFDCnCFDCmFDCTR — Channel CAN FD Control Register (m = 0 to 7)

Access: RCFDCnCFDCmFDCTR register can be read or written in 32-bit units
RCFDCnCFDCmFDCTRL register can be read or written in 16-bit units
RCFDCnCFDCmFDCTRLL register can be read or written in 8-bit units

Address: RCFDCnCFDCmFDCTR: <RCFDCn_base> + 0708_H + (20_H × m)
RCFDCnCFDCmFDCTRL: <RCFDCn_base> + 0708_H + (20_H × m)
RCFDCnCFDCmFDCTRLL: <RCFDCn_base> + 0708_H + (20_H × m)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOCCLR	EOCCLR
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Table 24.42 RCFDCnCFDCmFDCTR Register Contents

Bit Position	Bit Name	Function
31 to 2	Reserved	These bits are read as the value after reset. The write value should be the value after reset.
1	SOCCLR	Successful Occurrence Counter Clear Setting the SOCCLR bit to 1 clears the successful occurrence counter. This bit is always read as 0.
0	EOCCLR	Error Occurrence Counter Clear Setting the EOCCLR bit to 1 clears the error occurrence counter. This bit is always read as 0.

SOCCLR Bit

Setting this bit to 1 clears the successful occurrence counter (SOC[7:0] bits in the RCFDCnCFDCmFDSTS register). This bit is automatically cleared to 0.

EOCCLR Bit

Setting this bit to 1 clears the error occurrence counter (EOC[7:0] bits in the RCFDCnCFDCmFDSTS register). This bit is automatically cleared to 0.

24.3.2.8 RCFDCnCFDCmFDSTS — Channel CAN FD Status Register (m = 0 to 7)

Access: RCFDCnCFDCmFDSTS register can be read or written in 32-bit units

RCFDCnCFDCmFDSTSL register can be read or written in 16-bit units

RCFDCnCFDCmFDSTSH register is a read-only register that can be read in 16-bit units

RCFDCnCFDCmFDSTSLL, RCFDCnCFDCmFDSTSLH registers can be read or written in 8-bit units

RCFDCnCFDCmFDSTSHL, RCFDCnCFDCmFDSTSHH registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDCmFDSTS: <RCFDCn_base> + $070C_H$ + (20_H × m)

RCFDCnCFDCmFDSTSL: <RCFDCn_base> + $070C_H$ + (20_H × m),

RCFDCnCFDCmFDSTSH: <RCFDCn_base> + $070E_H$ + (20_H × m)

RCFDCnCFDCmFDSTSLL: <RCFDCn_base> + $070C_H$ + (20_H × m),

RCFDCnCFDCmFDSTSLH: <RCFDCn_base> + $070D_H$ + (20_H × m),

RCFDCnCFDCmFDSTSHL: <RCFDCn_base> + $070E_H$ + (20_H × m),

RCFDCnCFDCmFDSTSHH: <RCFDCn_base> + $070F_H$ + (20_H × m)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SOC[7:0]								EOC[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	SOCO	EOCO	TDCVF	TDCR[6:0]						
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R/W*1	R/W*1	R/W*1	R	R	R	R	R	R	R

Note 1. The only effective value for writing to this flag bit is 0, which clears the bit. Otherwise writing to the bit results in retention of its state.

Table 24.43 RCFDCnCFDCmFDSTS Register Contents

Bit Position	Bit Name	Function
31 to 24	SOC[7:0]	Successful Occurrence Counter The successful occurrence counter value can be read.
23 to 16	EOC[7:0]	Error Occurrence Counter The error occurrence counter value can be read.
15 to 10	Reserved	When read, the value after reset is returned. When writing to these bits, write the value after reset.
9	SOCO	Successful Occurrence Counter Overflow Flag 0: The successful occurrence counter does not overflow. 1: The successful occurrence counter has overflowed.
8	EOCO	Error Occurrence Counter Overflow Flag 0: The error occurrence counter does not overflow. 1: The error occurrence counter has overflowed.
7	TDCVF	Transmitter Delay Compensation Violation Flag 0: No transmitter delay compensation violation is present. 1: A transmitter delay compensation violation is present.
6 to 0	TDCR[6:0]	Transmitter Delay Compensation Result Status The transmitter delay compensation result can be read.

SOC[7:0] Bits

These bits show the successful occurrence counter value. The successful occurrence counter is incremented upon completion of message reception or transmission without an error. This counter stops counting when it reaches FF_H. In loopback mode, this counter is incremented twice.

These bits are cleared to 0 by writing 1 to the SOCCLR bit in the RCFDCnCFDCmFDCTR register. These bits are set to 0 in channel reset mode.

EOC[7:0] Bits

These bits show the error occurrence counter value. The error occurrence counter is incremented each time an error occurs according to the condition specified by the EOCCFG[2:0] bits in the RCFDCnCFDCmFDCFG register. This counter stops counting when it reaches FF_H.

These bits are cleared to 0 by writing 1 to the EOCCLR bit in the RCFDCnCFDCmFDCTR register. These bits are set to 0 in channel reset mode.

SOCO Flag

This bit indicates that successful occurrence counter overflow has occurred.

This flag is set to 1 when message reception or transmission is completed while the SOC[7:0] value has reached FF_H. This flag is set to 0 in channel reset mode.

EOCO Flag

This bit indicates that error occurrence counter overflow has occurred.

This flag is set to 1 when a CAN bus error is detected under the condition specified by the EOCCFG[2:0] bits in the RCFDCnCFDCmFDCFG register when the EOC[7:0] value has reached FF_H. This flag is set to 0 in channel reset mode.

TDCVF Flag

This bit indicates violation of transmitter delay compensation.

The transmit data is compared with the reception CAN bus level delayed due to the transceiver’s loop delay. This delay changes due to physical factors such as temperature. Because the TDCR[6:0] flags are updated for each message, temporary maximum delay cannot be confirmed.

This bit is set to 1 when the transmitter delay compensation exceeds the maximum compensation 3 CANm bit times - 2 fCAN (CANm bit time is the value of data bit rate). This flag is set to 0 in channel reset mode.

TDCR[6:0] Flags

These bits indicate the transmitter delay compensation result as a multiple of CAN clock frequency (fCAN).

This result depends on the settings of the TDCOC bit and TDCO[6:0] bits in the RCFDCnCFDCmFDCFG register.

These flags are updated at a falling edge between the FDF bit and res bit when the TDCE bit in the RCFDCnCFDCmFDCFG register is set to 1(transmitter delay compensation enable) and also the TDCOC bit in the RCFDCnCFDCmFDCFG register is set to 0(measurement and offset).

This flag is set to 0 in channel reset mode.

24.3.2.9 RCFDCnCFDCmFDCRC — Channel CAN FD CRC Register (m = 0 to 7)

Access: RCFDCnCFDCmFDCRC register is a read-only register that can be read in 32-bit units
RCFDCnCFDCmFDCRCL, RCFDCnCFDCmFDCRCH registers are read-only registers that can be read in 16-bit units
RCFDCnCFDCmFDCRCLL, RCFDCnCFDCmFDCRCLH, RCFDCnCFDCmFDCRCHL, RCFDCnCFDCmFDCRCHH registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDCmFDCRC: <RCFDCn_base> + 0710_H + (20_H × m)
RCFDCnCFDCmFDCRCL: <RCFDCn_base> + 0710_H + (20_H × m),
RCFDCnCFDCmFDCRCH: <RCFDCn_base> + 0712_H + (20_H × m)
RCFDCnCFDCmFDCRCLL: <RCFDCn_base> + 0710_H + (20_H × m),
RCFDCnCFDCmFDCRCLH: <RCFDCn_base> + 0711_H + (20_H × m),
RCFDCnCFDCmFDCRCHL: <RCFDCn_base> + 0712_H + (20_H × m),
RCFDCnCFDCmFDCRCHH: <RCFDCn_base> + 0713_H + (20_H × m)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	SCNT[3:0]				—	—	—	CRCREG[20:16]				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CRCREG[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 24.44 RCFDCnCFDCmFDCRC Register Contents

Bit Position	Bit Name	Function
31 to 28	Reserved	These bits are read as the value after reset.
27 to 24	SCNT[3:0]	Stuff count bit Indicate a value of the stuff count in a CAN FD frame. Bits 25 to 27 indicates the Gray-coded value of the stuff bit count modulo 8 in the transmitted/received frames. Bit 24 indicates an even parity value of bits 25 to 27.
23 to 21	Reserved	These bits are read as the value after reset.
20 to 0	CRCREG[20:0]	CRC Calculation Data (CRC Length:17 Bit or 21 Bit) These bits show the CRC value calculated based on the transmit message or receive message. When the CRC length is 17 bits, bits b20 to b17 are read as 0.

SCNT[3:0] Flags

When the CTME bit in the RCFDCnCFDCmCTR register is set to 1 (communication test mode enabled), a stuff count bit value of the CAN FD frame can be read if a message transmitted/received is a CAN FD frame. When the CTME bit is 0 (communication test mode disabled), this flag is always read as 0. These flags are updated at the first bit in the CRC field of the CAN FD frame. These bits are cleared to 0 in channel reset mode.

CRCREG[20:0] Flags

When the CTME bit in the RCFDCnCFDCmCTR register is 1 (communication test mode enabled), if transmit or receive message is a CAN FD frame (CRC length = 17 or 21 bits), these flags are updated and the CRC value calculated based on the message can be read. When the CRC length of the message is 17 bits, bits b20 to b17 are always read as 0. When a classical CAN frame is transmitted or received the CRCREG[14:0] value in the RCFDCnCFDCmERFL register is updated. When the CTME bit is 0 (communication test mode disabled), these bits are always read as 0.

These bits are cleared to 0 in channel reset mode.

24.3.3 Details of Global-related Registers

24.3.3.1 RCFDCnCFDGCFG — Global Configuration Register

Access: RCFDCnCFDGCFG register can be read or written in 32-bit units

RCFDCnCFDGCFGL, RCFDCnCFDGCFGH registers can be read or written in 16-bit units

RCFDCnCFDGCFGLL, RCFDCnCFDGCFGLH, RCFDCnCFDGCFGHL, RCFDCnCFDGCFGHH registers can be read or written in 8-bit units

Address: RCFDCnCFDGCFG: <RCFDCn_base> + 0084_H

RCFDCnCFDGCFGL: <RCFDCn_base> + 0084_H,

RCFDCnCFDGCFGH: <RCFDCn_base> + 0086_H

RCFDCnCFDGCFGLL: <RCFDCn_base> + 0084_H,

RCFDCnCFDGCFGLH: <RCFDCn_base> + 0085_H,

RCFDCnCFDGCFGHL: <RCFDCn_base> + 0086_H,

RCFDCnCFDGCFGHH: <RCFDCn_base> + 0087_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ITRCP[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSBTCS[2:0]			TSSS	TSP[3:0]				—	—	CMPOC	DCS	MME	DRE	DCE	TPRI
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 24.45 RCFDCnCFDGCFG Register Contents

Bit Position	Bit Name	Function
31 to 16	ITRCP[15:0]	Interval Timer Prescaler Set When these bits are set to M, the pclk is divided by M. Setting 0000_H is prohibited when the interval timer is in use.
15 to 13	TSBTCS[2:0]	Timestamp Clock Source Select b15 b14 b13 0 0 0: Channel 0 nominal bit time clock 0 0 1: Channel 1 nominal bit time clock 0 1 0: Channel 2 nominal bit time clock 0 1 1: Channel 3 nominal bit time clock 1 0 0: Channel 4 nominal bit time clock 1 0 1: Channel 5 nominal bit time clock 1 1 0: Channel 6 nominal bit time clock 1 1 1: Channel 7 nominal bit time clock
12	TSSS	Timestamp Source Select 0: pclk/2*1 1: Nominal bit time clock

Table 24.45 RCFDCnCFDGCFG Register Contents

Bit Position	Bit Name	Function
11 to 8	TSP[3:0]	Timestamp Clock Source Division b11 b10 b9 b8 0 0 0 0: Not divided 0 0 0 1: Divided by 2 0 0 1 0: Divided by 4 0 0 1 1: Divided by 8 0 1 0 0: Divided by 16 0 1 0 1: Divided by 32 0 1 1 0: Divided by 64 0 1 1 1: Divided by 128 1 0 0 0: Divided by 256 1 0 0 1: Divided by 512 1 0 1 0: Divided by 1024 1 0 1 1: Divided by 2048 1 1 0 0: Divided by 4096 1 1 0 1: Divided by 8192 1 1 1 0: Divided by 16384 1 1 1 1: Divided by 32768
7, 6	Reserved	When read, the value after reset is returned. When writing to these bits, write the value after reset.
5	CMPOC	Payload Overflow Mode Select 0: No message is stored. 1: Messages are stored and payloads exceeding the buffer size are discarded.
4	DCS	CAN Clock Source Select*2 0: clkc 1: clk_xincan
3	MME	Mirror Function Enable 0: Mirror function is disabled. 1: Mirror function is enabled.
2	DRE	DLC Replacement Enable 0: DLC replacement is disabled. 1: DLC replacement is enabled.
1	DCE	DLC Check Enable 0: DLC check is disabled. 1: DLC check is enabled.
0	TPRI	Transmit Priority Select 0: ID priority 1: Transmit buffer number priority

Note 1. When specifying pclk/2 as the timestamp counter count source, set bits TSBTCS[2:0] to 000_B.

Note 2. For the CAN clock frequency settings, see **Table 24.19, Range of Operating Frequency Depending on the Transfer Rate and the Number of Channels in Use in the RH850/F1KH and RH850/F1KM**.

Modify the RCFDCnCFDGCFG register only in global reset mode.

ITRCP[15:0] Bits

These bits are used to set a clock source division value of the interval timer for FIFO buffers. See **Section 24.7.3.1, Interval Transmission Function**.

TSBTCS[2:0] Bits

When the TSSS bit is 1, these bits are used to select the channel of the nominal bit time clock that will be the clock source of the timestamp counter. However, do not select the channel that handles the CAN FD frames.

TSSS Bit

This bit is used to select a clock source of the timestamp counter. Select pclk if there is no channel that handles only classical CAN frames.

TSP[3:0] Bits

A clock obtained by dividing the clock source selected with the TSBTCS[2:0] bits and TSSS bit according to the TSP[3:0] bits is used as the timestamp counter count source.

CMPOC Bit

This bit is used to select operation in case the payload length of received message exceeds the payload storage size of the storage buffer.

When this bit is 0, the received message in which the payload overflows is not stored in the buffer.

When this bit is 1, the received message in which the payload overflows is stored in the buffer, and depending on the DRE bit the received DLC value or the DLC value of the receive rule is stored in the buffer. At this time, payloads exceeding the buffer's payload storage size are discarded.

The buffer's payload storage size is set by the following bits.

- Receive buffer: RMPLS[2:0] bits in the RCFDCnCFDRMNB register
- Receive FIFO buffer: RFPLS[2:0] bits in the RCFDCnCFDRFCCx register
- Transmit/receive FIFO buffer: CFPLS[2:0] bits in the RCFDCnCFDCFCCk register

DCS Bit

When this bit is set to 0, clkc is used as the clock source of the CAN clock (fCAN).

When this bit is set to 1, clk_xincan is used as the clock source of the CAN clock (fCAN). For the CAN clock frequency settings, see **Table 24.19, Range of Operating Frequency Depending on the Transfer Rate and the Number of Channels in Use in the RH850/F1KH and RH850/F1KM**.

MME Bit

Setting this bit to 1 makes the mirror function available.

DRE Bit

When the DRE bit is set to 1, the DLC value of the receive rule is stored in the buffer instead of the DLC value of the received message after the DLC value has passed through the DLC filter. In this case, a value of 00_H is stored in each data byte that exceeds the DLC value of the receive rule.

The DLC replacement function is only available when the DCE bit is set to 1 (DLC check is enabled).

DCE Bit

Setting this bit to 1 makes the DLC check function available. When disabling the DLC check function, set the GAFLDLC[3:0] bits in the RCFDCnCFDGAFLP0_j register to 0000_B before clearing the DCE bit in the RCFDCnCFDGCFG register to 0.

TPRI Bit

This bit is used to set the transmit priority.

When this bit is set to 0, ID priority is selected and the transmit priority complies with the CAN bus arbitration rule (ISO11898-1 specifications). When this bit is set to 1, transmit buffer number priority is selected and the transmit buffer with the smallest number has the highest priority.

When using the transmit queue, this bit should be set to 0.

24.3.3.2 RCFDCnCFDGCTR — Global Control Register

Access: RCFDCnCFDGCTR register can be read or written in 32-bit units

RCFDCnCFDGCTRL, RCFDCnCFDGCTRH registers can be read or written in 16-bit units

RCFDCnCFDGCTRLL, RCFDCnCFDGCTRLH, RCFDCnCFDGCTRHL registers can be read or written in 8-bit units

Address: RCFDCnCFDGCTR: <RCFDCn_base> + 0088_H

RCFDCnCFDGCTRL: <RCFDCn_base> + 0088_H,

RCFDCnCFDGCTRH: <RCFDCn_base> + $008A_H$

RCFDCnCFDGCTRLL: <RCFDCn_base> + 0088_H,

RCFDCnCFDGCTRLH: <RCFDCn_base> + 0089_H,

RCFDCnCFDGCTRHL: <RCFDCn_base> + $008A_H$

Value after reset: $0000\ 0005_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TSRST
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	CMPOFIE	THLEIE	MEIE	DEIE	—	—	—	—	—	GSLPR	GMDC[1:0]	
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

Table 24.46 RCFDCnCFDGCTR Register Contents

Bit Position	Bit Name	Function
31 to 17	Reserved	When read, the value after reset is returned. When writing to these bits, write the value after reset.
16	TSRST	Timestamp Counter Reset Setting the TSRST bit to 1 resets the timestamp counter. This bit is always read as 0.
15 to 12	Reserved	When read, the value after reset is returned. When writing to these bits, write the value after reset.
11	CMPOFIE	Payload Overflow Interrupt Enable 0: A payload overflow interrupt is disabled. 1: A payload overflow interrupt is enabled.
10	THLEIE	Transmit History Buffer Overflow Interrupt Enable 0: Transmit history buffer overflow interrupt is disabled. 1: Transmit history buffer overflow interrupt is enabled.
9	MEIE	FIFO Message Lost Interrupt Enable 0: FIFO message lost interrupt is disabled. 1: FIFO message lost interrupt is enabled.
8	DEIE	DLC Error Interrupt Enable 0: DLC error interrupt is disabled. 1: DLC error interrupt is enabled.
7 to 3	Reserved	When read, the value after reset is returned. When writing to these bits, write the value after reset.
2	GSLPR	Global Stop Mode 0: Other than global stop mode 1: Global stop mode

Table 24.46 RCFDCnCFDGCTR Register Contents

Bit Position	Bit Name	Function
1, 0	GMDC[1:0]	Global Mode Select b1 b0 0 0: Global operating mode 0 1: Global reset mode 1 0: Global test mode 1 1: Setting prohibited

TSRST Bit

This bit is used to reset the timestamp counter. When this bit is set to 1, the RCFDCnCFDGTSC register is cleared to 0000_H.

CMPOFIE Bit

When the CMPOF flag in the RCFDCnCFDGERFL register is set to 1 after the CMPOFIE bit is set to 1, an interrupt request occurs. Modify this bit only in global reset mode.

THLEIE Bit

When the THLEIE bit is set to 1 and the THLES flag in the RCFDCnCFDGERFL register is set to 1, an interrupt request is generated. Modify this bit only in global reset mode.

MEIE Bit

When the MEIE bit is set to 1 and the MES flag in the RCFDCnCFDGERFL register is set to 1, an interrupt request is generated. Modify this bit only in global reset mode.

DEIE Bit

When the DEIE bit is set to 1 and the DEF flag in the RCFDCnCFDGERFL register is set to 1, an interrupt request is generated. Modify this bit only in global reset mode.

GSLPR Bit

Setting this bit to 1 places the RS-CANFD module into global stop mode.

Clearing this bit to 0 makes the RS-CANFD module leave from global stop mode. This bit should not be modified in global operating mode or global test mode.

GMDC[1:0] Bits

These bits are used to select the mode of entire RS-CANFD module (global operating mode, global reset mode, or global test mode). For details, see **Section 24.5.1, Global Modes**. Setting the GSLPR bit to 1 when in global reset mode places the RS-CANFD module in global stop mode.

24.3.3.3 RCFDCnCFDGSTS — Global Status Register

Access: RCFDCnCFDGSTS register is a read-only register that can be read in 32-bit units
RCFDCnCFDGSTSL register is a read-only register that can be read in 16-bit units
RCFDCnCFDGSTSLL register is a read-only register that can be read in 8-bit units

Address: RCFDCnCFDGSTS: <RCFDCn_base> + $008C_H$
RCFDCnCFDGSTSL: <RCFDCn_base> + $008C_H$
RCFDCnCFDGSTSLL: <RCFDCn_base> + $008C_H$

Value after reset: $0000\ 000D_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	GRAMINIT	GSLPSTS	GHLTSTS	GRSTSTS
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 24.47 RCFDCnCFDGSTS Register Contents

Bit Position	Bit Name	Function
31 to 4	Reserved	When read, the value after reset is returned.
3	GRAMINIT	CAN RAM Initialization Status Flag 0: CAN RAM initialization is completed. 1: CAN RAM initialization is ongoing.
2	GSLPSTS	Global Stop Status Flag 0: Not in global stop mode 1: In global stop mode
1	GHLTSTS	Global Test Status Flag 0: Not in global test mode 1: In global test mode
0	GRSTSTS	Global Reset Status Flag 0: Not in global reset mode 1: In global reset mode

GRAMINIT Flag

This flag indicates the initialization status of the CAN RAM.

This flag is set to 1 after the MCU has been reset, and is cleared to 0 when CAN RAM initialization is completed.

GSLPSTS Flag

This flag is set to 1 when the CAN module has transitioned to global stop mode, and is cleared to 0 when the CAN module has returned from global stop mode.

GHLTSTS Flag

This flag is set to 1 when the CAN module has transitioned to global test mode, and is cleared to 0 when the CAN module has exited global test mode.

GRSTSTS Flag

This flag is set to 1 when the CAN module has transitioned to global reset mode, and is cleared to 0 when the CAN module has exited global reset mode. This flag remains 1 even when the CAN module has transitioned from global reset mode to global stop mode.

24.3.3.4 RCFDCnCFDGERFL — Global Error Flag Register

Access: RCFDCnCFDGERFL register can be read or written in 32-bit units

RCFDCnCFDGERFLL, RCFDCnCFDGERFLH registers can be read or written in 16-bit units

RCFDCnCFDGERFLLL, RCFDCnCFDGERFLHL registers can be read or written in 8-bit units

Address: RCFDCnCFDGERFL: <RCFDCn_base> + 0090_H

RCFDCnCFDGERFLL: <RCFDCn_base> + 0090_H,

RCFDCnCFDGERFLH: <RCFDCn_base> + 0092_H

RCFDCnCFDGERFLLL: <RCFDCn_base> + 0090_H,

RCFDCnCFDGERFLHL: <RCFDCn_base> + 0092_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	EEF7	EEF6	EEF5	EEF4	EEF3	EEF2	EEF1	EEF0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	CMPOF	THLES	MES	DEF
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R/W*1	R	R	R/W*1

Note 1. The only effective value for writing to this flag bit is 0, which clears the bit. Otherwise writing to the bit results in retention of its state.

Table 24.48 RCFDCnCFDGERFL Register Contents

Bit Position	Bit Name	Function
31 to 24	Reserved	When read, the value after reset is returned. When writing these bits, write the value after reset.
23	EEF7	ECC Error Flag for Channel 7 0: No 2-bit ECC error when deciding transmission priority 1: A 2-bit ECC error when deciding transmission priority
22	EEF6	ECC Error Flag for Channel 6 0: No 2-bit ECC error when deciding transmission priority 1: A 2-bit ECC error when deciding transmission priority
21	EEF5	ECC Error Flag for Channel 5 0: No 2-bit ECC error when deciding transmission priority 1: A 2-bit ECC error when deciding transmission priority
20	EEF4	ECC Error Flag for Channel 4 0: No 2-bit ECC error when deciding transmission priority 1: A 2-bit ECC error when deciding transmission priority
19	EEF3	ECC Error Flag for Channel 3 0: No 2-bit ECC error when deciding transmission priority 1: A 2-bit ECC error when deciding transmission priority
18	EEF2	ECC Error Flag for Channel 2 0: No 2-bit ECC error when deciding transmission priority 1: A 2-bit ECC error when deciding transmission priority
17	EEF1	ECC Error Flag for Channel 1 0: No 2-bit ECC error when deciding transmission priority 1: A 2-bit ECC error when deciding transmission priority

Table 24.48 RCFDCnCFDGERFL Register Contents

Bit Position	Bit Name	Function
16	EEF0	ECC Error Flag for Channel 0 0: No 2-bit ECC error when deciding transmission priority 1: A 2-bit ECC error when deciding transmission priority
15 to 4	Reserved	When read, the undefined value is returned. When writing these bits, write the value after reset.
3	CMPOF	Payload Overflow Flag 0: No payload overflow has occurred. 1: A payload overflow has occurred.
2	THLES	Transmit History Buffer Overflow Status Flag 0: No transmit history buffer overflow has occurred. 1: A transmit history buffer overflow has occurred.
1	MES	FIFO Message Lost Status Flag 0: No FIFO message lost error has occurred. 1: A FIFO message lost error has occurred.
0	DEF	DLC Error Flag 0: No DLC error has occurred. 1: A DLC error has occurred.

All flags in the RCFDCnCFDGERFL register are cleared to 0 in global reset mode.

EEFm Flag

When a 2-bit ECC error is detected during the transmission priority determination of channel m (m = 0 to 7), the EEFm flag is set to 1, disabling message transmission. This flag can be cleared to 0 by writing 0 by the program.

CMPOF Flag

When a payload overflow occurs in any of channel m (m = 0 to 7), the CMPOF flag is set to 1. This flag can be cleared to 0 by writing 0 to this bit by the program.

THLES Flag

The THLES flag is set to 1 when any one of the THLELT flags in the RCFDCnCFDTHLSTSm register (m = 0 to 7) is set to 1.

This flag is cleared to 0 when the THLELT flags of all channels are set to 0.

MES Flag

The MES flag is set to 1 when any one of the RFMLT flags in the RCFDCnCFDRFSTSx register (x = 0 to 7) or the CFMLT flags in the RCFDCnCFDCFSTSk register (k = 0 to 17) is set to 1.

This flag is cleared to 0 when all RFMLT flags and CFMLT flags are set to 0.

DEF Flag

The DEF flag is set to 1 when an error has been detected during the DLC check. The program can clear this flag by writing 0 to this bit.

To clear the flags of the register to 0, the program must write 0 to the corresponding flag to be cleared. When writing 0, using store instruction, set the bit to be set to “0” to “0”, and the bits not to be set to “0” to “1”.

NOTE

To clear the flag of this register to 0, use a store instruction to write 0 to the given flag and 1 to the other flags.

24.3.3.5 RCFDCnCFDGTSC — Global Timestamp Counter Register

Access: RCFDCnCFDGTSC register is a read-only register that can be read in 32-bit units.

RCFDCnCFDGTSCL register is a read-only register that can be read in 16-bit units.

Address: RCFDCnCFDGTSC: <RCFDCn_base> + 0094_H

RCFDCnCFDGTSCL: <RCFDCn_base> + 0094_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TS[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 24.49 RCFDCnCFDGTSC Register Contents

Bit Position	Bit Name	Function
31 to 16	Reserved	These bits are read as the value after reset.
15 to 0	TS[15:0]	Timestamp Value The timestamp counter value can be read. Counter Value: 0000_H to $FFFF_H$

TS[15:0] Bits

When the TS[15:0] bits are read, the read value shows the timestamp counter (16-bit free-running counter) value at that time. When the SOF is detected, the TS[15:0] value is captured and later stored in the receive buffer or the FIFO buffer. Furthermore, the TS[15:0] value is stored in the transmit history buffer. The timestamp counter is initialized in global reset mode.

The timestamp counter starts and stops counting differently, depending on the count source.

- When the TSSS bit in the RCFDCnCFDGCFG register is 0 (pclk):

  The timestamp counter starts counting when the RS-CANFD module has transitioned to global operating mode.

  This counter stops counting when the RS-CANFD module has transitioned to global stop mode or global test mode.

- When the TSSS bit is 1 (CANm nominal bit time clock):

  The timestamp counter starts counting when the corresponding channel has transitioned to channel communication mode.

  This counter stops counting when the corresponding channel has transitioned to channel reset mode or channel halt mode.

24.3.3.6 RCFDCnCFDGTINTSTS0 — Global TX Interrupt Status Register 0

Access: RCFDCnCFDGTINTSTS0 register is a read-only register that can be read in 32-bit units

RCFDCnCFDGTINTSTS0L, RCFDCnCFDGTINTSTS0H registers are read-only registers that can be read in 16-bit units

RCFDCnCFDGTINTSTS0LL, RCFDCnCFDGTINTSTS0LH, RCFDCnCFDGTINTSTS0HL, RCFDCnCFDGTINTSTS0HH registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDGTINTSTS0: <RCFDCn_base> + 0610_H

RCFDCnCFDGTINTSTS0L: <RCFDCn_base> + 0610_H,

RCFDCnCFDGTINTSTS0H: <RCFDCn_base> + 0612_H

RCFDCnCFDGTINTSTS0LL: <RCFDCn_base> + 0610_H,

RCFDCnCFDGTINTSTS0LH: <RCFDCn_base> + 0611_H,

RCFDCnCFDGTINTSTS0HL: <RCFDCn_base> + 0612_H,

RCFDCnCFDGTINTSTS0HH: <RCFDCn_base> + 0613_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	THIF3	CFTIF3	TQIF3	TAIF3	TSIF3	—	—	—	THIF2	CFTIF2	TQIF2	TAIF2	TSIF2
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R*1	R*1	R*1	R*1	R*1	R	R	R	R*1	R*1	R*1	R*1	R*1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	THIF1	CFTIF1	TQIF1	TAIF1	TSIF1	—	—	—	THIF0	CFTIF0	TQIF0	TAIF0	TSIF0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R*1	R*1	R*1	R*1	R*1	R	R	R	R*1	R*1	R*1	R*1	R*1

Note 1. This bit is automatically cleared in the global reset or channel reset mode.

Table 24.50 RCFDCnCFDGTINTSTS0 Register Contents

Bit Position	Bit Name	Function
31 to 29	Reserved	These bits are read as the value after reset.
28	THIF3	Channel 3 Transmit History Interrupt Status Flag 0: Transmit history interrupt is not requested. 1: Transmit history interrupt is requested.
27	CFTIF3	Channel 3 Transmit/receive FIFO Transmit Interrupt Status Flag 0: Transmit/receive FIFO transmit interrupt is not requested. 1: Transmit/receive FIFO transmit interrupt is requested.
26	TQIF3	Channel 3 Transmit Queue Interrupt Status Flag 0: Transmit queue interrupt is not requested. 1: Transmit queue interrupt is requested.
25	TAIF3	Channel 3 Transmit Buffer Abort Interrupt Status Flag 0: Transmit buffer abort interrupt is not requested. 1: Transmit buffer abort interrupt is requested
24	TSIF3	Channel 3 Transmit Buffer Transmit Complete Interrupt Status Flag 0: Transmit buffer transmit complete interrupt is not requested. 1: Transmit buffer transmit complete interrupt is requested.
23 to 21	Reserved	These bits are read as the value after reset.
20	THIF2	Channel 2 Transmit History Interrupt Status Flag 0: Transmit history interrupt is not requested. 1: Transmit history interrupt is requested.

Table 24.50 RCFDCnCFDGTINTSTS0 Register Contents

Bit Position	Bit Name	Function
19	CFTIF2	Channel 2 Transmit/receive FIFO Transmit Interrupt Status Flag 0: Transmit/receive FIFO transmit interrupt is not requested. 1: Transmit/receive FIFO transmit interrupt is requested.
18	TQIF2	Channel 2 Transmit Queue Interrupt Status Flag 0: Transmit queue interrupt is not requested. 1: Transmit queue interrupt is requested.
17	TAIF2	Channel 2 Transmit Buffer Abort Interrupt Status Flag 0: Transmit buffer abort interrupt is not requested. 1: Transmit buffer abort interrupt is requested.
16	TSIF2	Channel 2 Transmit Buffer Interrupt Status Flag 0: Transmit buffer transmit complete interrupt is not requested. 1: Transmit buffer transmit complete interrupt is requested.
15 to 13	Reserved	These bits are read as the value after reset.
12	THIF1	Channel 1 Transmit History Interrupt Status Flag 0: Transmit history interrupt is not requested. 1: Transmit history interrupt is requested.
11	CFTIF1	Channel 1 Transmit/receive FIFO Transmit Interrupt Status Flag 0: Transmit/receive FIFO transmit interrupt is not requested. 1: Transmit/receive FIFO transmit interrupt is requested.
10	TQIF1	Channel 1 Transmit Queue Interrupt Status Flag 0: Transmit queue interrupt is not requested. 1: Transmit queue interrupt is requested.
9	TAIF1	Channel 1 Transmit Buffer Abort Interrupt Status Flag 0: Transmit buffer abort interrupt is not requested. 1: Transmit buffer abort interrupt is requested.
8	TSIF1	Channel 1 Transmit Buffer Interrupt Status Flag 0: Transmit buffer transmit complete interrupt is not requested. 1: Transmit buffer transmit complete interrupt is requested.
7 to 5	Reserved	These bits are read as the value after reset.
4	THIF0	Channel 0 Transmit History Interrupt Status Flag 0: Transmit history interrupt is not requested. 1: Transmit history interrupt is requested.
3	CFTIF0	Channel 0 Transmit/receive FIFO Transmit Interrupt Status Flag 0: Transmit/receive FIFO transmit interrupt is not requested. 1: Transmit/receive FIFO transmit interrupt is requested.
2	TQIF0	Channel 0 Transmit Queue Interrupt Status Flag 0: Transmit queue interrupt is not requested. 1: Transmit queue interrupt is requested.
1	TAIF0	Channel 0 Transmit Buffer Abort Interrupt Status Flag 0: Transmit buffer abort interrupt is not requested. 1: Transmit buffer abort interrupt is requested.
0	TSIF0	Channel 0 Transmit Buffer Interrupt Status Flag 0: Transmit buffer transmit complete interrupt is not requested. 1: Transmit buffer transmit complete interrupt is requested.

TSIFm Bits

The TSIFm bit is set to 1 when the TMIEp bit in the RCFDCnCFDTMIECm register is set to 1 (transmit buffer interrupt enabled) and the TMTRF[1:0] flags in the corresponding RCFDCnCFDTMSTSp register are set to 10_B (transmit completed without abort request) or 11_B (transmit completed with abort request).

When the TMTRF[1:0] flags are cleared to 00_B under the condition that the TSIFm bit can be set to 1, this flag is cleared to 0. In addition, clearing the TMIEp bit to 0 also clears this flag to 0.

TAIFm Bits

The TAIFm bit is set to 1 when the TAIE bit in the RCFDCnCFDCmCTR register is 1 (transmit abort interrupt enabled) and the TMTRF[1:0] flags in the RCFDCnCFDTMSTSp register are set to 01_B (transmit abort completed).

This flag is cleared to 0 when the TMTRF[1:0] flags are cleared to 00_B after the transmit abort is completed.

TQIFm Bits

When the TXQTXIE bit in the RCFDCnCFDTXQCCm register is set to 1 (transmit queue interrupt enabled) and the TXQTXIF bit in the RCFDCnCFDTXQSTSm register is set to 1 (transmit queue interrupt request), the TQIFm bit is set to 1.

When the TXQTXIF bit (transmit queue interrupt request) in the RCFDCnCFDTXQSTSm register is cleared to 0, this bit is cleared to 0. This flag is also cleared to 0 when the TXQTXIE bit is cleared to 0.

CFTIFm Bits

When the CFTXIE bit in the RCFDCnCFDCFCCk register is set to 1 (transmit/receive FIFO transmit interrupt enabled) and the CFTXIF bit in the RCFDCnCFDCFSTSk register is set to 1 (transmit/receive FIFO transmit interrupt request), the CFTIFm bit is set to 1.

When the CFTXIF bit is cleared to 0 under the conditions that the CFTIFm bit can be set to 1, this bit is cleared to 0. This flag is also cleared to 0 when the CFTXIE bit is cleared to 0.

THIFm Bits

When the THLIE bit in the RCFDCnCFDTHLCCm register is set to 1 (transmit history interrupt enabled) and the THLIF bit in the RCFDCnCFDTHLSTSm register is set to 1 (transmit history interrupt request), the THIFm bit is set to 1.

When the THLIF bit in the RCFDCnCFDTHLSTSm register is cleared to 0, this bit is cleared to 0. This flag is also cleared to 0 when the THLIE bit is cleared to 0.

24.3.3.7 RCFDCnCFDGTINTSTS1 — Global TX Interrupt Status Register 1

Access: RCFDCnCFDGTINTSTS1 register is a read-only register that can be read in 32-bit units

RCFDCnCFDGTINTSTS1L, RCFDCnCFDGTINTSTS1H registers are read-only registers that can be read in 16-bit units

RCFDCnCFDGTINTSTS1LL, RCFDCnCFDGTINTSTS1LH, RCFDCnCFDGTINTSTS1HL, RCFDCnCFDGTINTSTS1HH registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDGTINTSTS1: <RCFDCn_base> + 0614_H

RCFDCnCFDGTINTSTS1L: <RCFDCn_base> + 0614_H,

RCFDCnCFDGTINTSTS1H: <RCFDCn_base> + 0616_H

RCFDCnCFDGTINTSTS1LL: <RCFDCn_base> + 0614_H,

RCFDCnCFDGTINTSTS1LH: <RCFDCn_base> + 0615_H,

RCFDCnCFDGTINTSTS1HL: <RCFDCn_base> + 0616_H,

RCFDCnCFDGTINTSTS1HH: <RCFDCn_base> + 0617_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	THIF7	CFTIF7	TQIF7	TAIF7	TSIF7	—	—	—	THIF6	CFTIF6	TQIF6	TAIF6	TSIF6
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R*1	R*1	R*1	R*1	R*1	R	R	R	R*1	R*1	R*1	R*1	R*1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	THIF5	CFTIF5	TQIF5	TAIF5	TSIF5	—	—	—	THIF4	CFTIF4	TQIF4	TAIF4	TSIF4
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R*1	R*1	R*1	R*1	R*1	R	R	R	R*1	R*1	R*1	R*1	R*1

Note 1. This bit is automatically cleared in the global reset or channel reset mode.

Table 24.51 RCFDCnCFDGTINTSTS1 Register Contents

Bit Position	Bit Name	Function
31 to 29	Reserved	These bits are read as the value after reset.
28	THIF7	Channel 7 Transmit History Interrupt Status Flag 0: Transmit history interrupt is not requested. 1: Transmit history interrupt is requested.
27	CFTIF7	Channel 7 Transmit/receive FIFO Transmit Interrupt Status Flag 0: Transmit/receive FIFO transmit interrupt is not requested. 1: Transmit/receive FIFO transmit interrupt is requested.
26	TQIF7	Channel 7 Transmit Queue Interrupt Status Flag 0: Transmit queue interrupt is not requested. 1: Transmit queue interrupt is requested.
25	TAIF7	Channel 7 Transmit Buffer Abort Interrupt Status Flag 0: Transmit buffer abort interrupt is not requested. 1: Transmit buffer abort interrupt is requested.
24	TSIF7	Channel 7 Transmit Buffer Interrupt Status Flag 0: Transmit buffer transmit complete interrupt is not requested. 1: Transmit buffer transmit complete interrupt is requested
23 to 21	Reserved	These bits are read as the value after reset.
20	THIF6	Channel 6 Transmit History Interrupt Status Flag 0: Transmit history interrupt is not requested. 1: Transmit history interrupt is requested.

Table 24.51 RCFDCnCFDGTINTSTS1 Register Contents

Bit Position	Bit Name	Function
19	CFTIF6	Channel 6 Transmit/receive FIFO Transmit Interrupt Status Flag 0: Transmit/receive FIFO transmit interrupt is not requested. 1: Transmit/receive FIFO transmit interrupt is requested.
18	TQIF6	Channel 6 Transmit Queue Interrupt Status Flag 0: Transmit queue interrupt is not requested. 1: Transmit queue interrupt is requested.
17	TAIF6	Channel 6 Transmit Buffer Abort Interrupt Status Flag 0: Transmit buffer abort interrupt is not requested. 1: Transmit buffer abort interrupt is requested.
16	TSIF6	Channel 6 Transmit Buffer Interrupt Status Flag 0: Transmit buffer transmit complete interrupt is not requested. 1: Transmit buffer transmit complete interrupt is requested
15 to 13	Reserved	These bits are read as the value after reset.
12	THIF5	Channel 5 Transmit History Interrupt Status Flag 0: Transmit history interrupt is not requested. 1: Transmit history interrupt is requested.
11	CFTIF5	Channel 5 Transmit/receive FIFO Transmit Interrupt Status Flag 0: Transmit/receive FIFO transmit interrupt is not requested. 1: Transmit/receive FIFO transmit interrupt is requested.
10	TQIF5	Channel 5 Transmit Queue Interrupt Status Flag 0: Transmit queue interrupt is not requested. 1: Transmit queue interrupt is requested.
9	TAIF5	Channel 5 Transmit Buffer Abort Interrupt Status Flag 0: Transmit buffer abort interrupt is not requested. 1: Transmit buffer abort interrupt is requested.
8	TSIF5	Channel 5 Transmit Buffer Interrupt Status Flag 0: Transmit buffer transmit complete interrupt is not requested. 1: Transmit buffer transmit complete interrupt is requested
7 to 5	Reserved	These bits are read as the value after reset.
4	THIF4	Channel 4 Transmit History Interrupt Status Flag 0: Transmit history interrupt is not requested. 1: Transmit history interrupt is requested.
3	CFTIF4	Channel 4 Transmit/receive FIFO Transmit Interrupt Status Flag 0: Transmit/receive FIFO transmit interrupt is not requested. 1: Transmit/receive FIFO transmit interrupt is requested.
2	TQIF4	Channel 4 Transmit Queue Interrupt Status Flag 0: Transmit queue interrupt is not requested. 1: Transmit queue interrupt is requested.
1	TAIF4	Channel 4 Transmit Buffer Abort Interrupt Status Flag 0: Transmit buffer abort interrupt is not requested. 1: Transmit buffer abort interrupt is requested.
0	TSIF4	Channel 4 Transmit Buffer Interrupt Status Flag 0: Transmit buffer transmit complete interrupt is not requested. 1: Transmit buffer transmit complete interrupt is requested.

TSIFm Bits

The TSIFm bit is set to 1 when the TMIEp bit in the RCFDCnCFDTMIECm register is set to 1 (transmit buffer interrupt enabled) and the TMTRF[1:0] flags in the corresponding RCFDCnCFDTMSTSp register are set to 10_B (transmit completed without abort request) or 11_B (transmit completed with abort request).

When the TMTRF[1:0] flags are cleared to 00_B under the condition that the TSIFm bit can be set to 1, this flag is cleared to 0. In addition, clearing the TMIEp bit to 0 also clears this flag to 0.

TAIFm Bits

The TAIFm bit is set to 1 when the TAIE bit in the RCFDCnCFDCmCTR register is set to 1 (transmit abort interrupt enabled) and the TMTRF[1:0] flags in the RCFDCnCFDTMSTSp register are set to 01_B (transmit abort completed).

This flag is cleared to 0 when the TMTRF[1:0] flags are cleared to 00_B after the transmit abort is completed.

TQIFm Bits

When the TXQTXIE bit in the RCFDCnCFDTXQCCm register is set to 1 (transmit queue interrupt enabled) and the TXQTXIF bit in the RCFDCnCFDTXQSTSm register is set to 1 (transmit queue interrupt request), the TQIFm bit is set to 1.

When the TXQTXIF bit (transmit queue interrupt request) in the RCFDCnCFDTXQSTSm register is cleared to 0, this bit is cleared to 0. Clearing the TXQTXIE bit to 0 also clears this flag to 0.

CFTIFm Bits

When the CFTXIE bit in the RCFDCnCFDCFCCk register is set to 1 (transmit/receive FIFO transmit interrupt enabled) and the CFTXIF bit in the RCFDCnCFDCFSTSk register is set to 1 (transmit/receive FIFO transmit interrupt request), the CFTIFm bit is set to 1.

When the CFTXIF bit is cleared to 0 under the conditions that the CFTIFm bit can be set to 1, this bit is cleared to 0. This flag is also cleared to 0 when the CFTXIE bit is cleared to 0.

THIFm Bits

When the THLIE bit in the RCFDCnCFDTHLCCm register is set to 1 (transmit history interrupt enabled) and the THLIF bit in the RCFDCnCFDTHLSTSm register is set to 1 (transmit history interrupt request), the THIFm bit is set to 1.

When the THLIF bit in the RCFDCnCFDTHLSTSm register is cleared to 0, this bit is cleared to 0. This flag is also cleared to 0 when the THLIE bit is cleared to 0.

24.3.3.8 RCFDCnCFDGFDCFG — Global FD Configuration Register

Access: RCFDCnCFDGFDCFG register can be read or written in 32-bit units
RCFDCnCFDGFDCFGL register can be read or written in 16-bit units
RCFDCnCFDGFDCFGLL, RCFDCnCFDGFDCFGLH registers can be read or written in 8-bit units

Address: RCFDCnCFDGFDCFG: <RCFDCn_base> + 0624_H
RCFDCnCFDGFDCFGL: <RCFDCn_base> + 0624_H
RCFDCnCFDGFDCFGLL: <RCFDCn_base> + 0624_H,
RCFDCnCFDGFDCFGLH: <RCFDCn_base> + 0625_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	TSCCFG[1:0]		—	—	—	—	—	—	—	RPED
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R	R/W

Table 24.52 RCFDCnCFDGFDCFG register Contents

Bit Position	Bit Name	Function
31 to 10	Reserved	These bits are read as the value after reset. The write value should be the value after reset.
9, 8	TSCCFG[1:0]	Time-stamp capture setting bit b9 b8 0 0: Captured at a sample point in the SOF bit. 0 1: Captured when a valid frame has been transmitted/received. 1 0: Captured at a sample point of the res bit.*1 1 1: Setting prohibited.
7 to 1	Reserved	These bits are read as the value after reset. The write value should be the value after reset.
0	RPED	Protocol exception event detection disabled bit 0: Protocol exception event detection is enabled 1: Protocol exception event detection is disabled

Note 1. When a classical CAN frame is transmitted/received, a time-stamp value will be captured at the sample point in the SOF bit.

TSCCFG bit

Select a point where a time-stamp value is captured. Modify this bit only in global reset mode.

RPED bit

Setting this bit to 1 disables the protocol exception event detection. When a protocol exception event is detected while this bit is set to 1, the event is regarded as a form error and an error frame will be output. Modify this bit only in global reset mode.

24.3.4 Details of Receive Rule-related Registers

24.3.4.1 RCFDCnCFDGAFLECTR — Receive Rule Entry Control Register

Access: RCFDCnCFDGAFLECTR register can be read or written in 32-bit units

RCFDCnCFDGAFLECTRL register can be read or written in 16-bit units

RCFDCnCFDGAFLECTRLL, RCFDCnCFDGAFLECTRLH registers can be read or written in 8-bit units

Address: RCFDCnCFDGAFLECTR: <RCFDCn_base> + 0098_H

RCFDCnCFDGAFLECTRL: <RCFDCn_base> + 0098_H

RCFDCnCFDGAFLECTRLL: <RCFDCn_base> + 0098_H,

RCFDCnCFDGAFLECTRLH: <RCFDCn_base> + 0099_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	AFLDAE	—	—	AFLPN[5:0]					
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 24.53 RCFDCnCFDGAFLECTR Register Contents

Bit Position	Bit Name	Function
31 to 9	Reserved	These bits are read as the value after reset. The write value should be the value after reset.
8	AFLDAE	Receive Rule Table Write Enable 0: Receive rule table write is disabled. 1: Receive rule table write is enabled.
7, 6	Reserved	These bits are read as the value after reset. The write value should be the value after reset.
5 to 0	AFLPN[5:0]	Receive Rule Table Page Number Configuration A page number can be selected in the range of page 0 (000000_B) to page 63 (111111_B).

AFLDAE Bit

Setting this bit to 0 disables the write to the receive rule table. After writes to the receive rule table are completed, set this bit to 0 to disable the write to the table. The receive rule table can be read regardless of the value of this bit.

Set the AFLDAE bit to 1 only in global reset mode.

AFLPN[5:0] Bits

These bits are used to set the page number of the receive rule table. Sixteen receive rules can be set per page.

Set these bits to a value within the range of 000000_B to 111111_B.

For details about the receive rule table, see **Section 24.6.1, Data Processing Using the Receive Rule Table**.

24.3.4.2 RCFDCnCFDGAFLCFG0 — Receive Rule Configuration Register 0

Access: RCFDCnCFDGAFLCFG0 register can be read or written in 32-bit units

RCFDCnCFDGAFLCFG0L, RCFDCnCFDGAFLCFG0H registers can be read or written in 16-bit units

RCFDCnCFDGAFLCFG0LL, RCFDCnCFDGAFLCFG0LH, RCFDCnCFDGAFLCFG0HL, RCFDCnCFDGAFLCFG0HH registers can be read or written in 8-bit units

Address: RCFDCnCFDGAFLCFG0: <RCFDCn_base> + $009C_H$

RCFDCnCFDGAFLCFG0L: <RCFDCn_base> + $009C_H$,

RCFDCnCFDGAFLCFG0H: <RCFDCn_base> + $009E_H$

RCFDCnCFDGAFLCFG0LL: <RCFDCn_base> + $009C_H$,

RCFDCnCFDGAFLCFG0LH: <RCFDCn_base> + $009D_H$,

RCFDCnCFDGAFLCFG0HL: <RCFDCn_base> + $009E_H$,

RCFDCnCFDGAFLCFG0HH: <RCFDCn_base> + $009F_H$

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RNC0[7:0]								RNC1[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RNC2[7:0]								RNC3[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 24.54 RCFDCnCFDGAFLCFG0 Register Contents

Bit Position	Bit Name	Function
31 to 24	RNC0[7:0]	Number of Rules for Channel 0 Set the number of receive rules exclusively used for channel 0.
23 to 16	RNC1[7:0]	Number of Rules for Channel 1 Set the number of receive rules exclusively used for channel 1.
15 to 8	RNC2[7:0]	Number of Rules for Channel 2 Set the number of receive rules exclusively used for channel 2.
7 to 0	RNC3[7:0]	Number of Rules for Channel 3 Set the number of receive rules exclusively used for channel 3.

Modify the RCFDCnCFDGAFLCFG0 register only in global reset mode.

Up to 128 × (number of channels) rules can be registered in the receive rule table for the entire unit. The number of receive rules per channel should meet the following conditions.

- The maximum number of rules per channel is 255.
- The total number of rules allocated to each channel does not exceed the number of rules that can be registered for the entire unit.

RNC0[7:0] Bits

These bits are used to set the number of rules to be registered in the channel 0 receive rule table. Set these bits to a value within the range of 00_H to FF_H.

RNC1[7:0] Bits

These bits are used to set the number of rules to be registered in the channel 1 receive rule table. Set these bits to a value within the range of 00_H to FF_H.

RNC2[7:0] Bits

These bits are used to set the number of rules to be registered in the channel 2 receive rule table. Set these bits to a value within the range of 00_H to FF_H.

RNC3[7:0] Bits

These bits are used to set the number of rules to be registered in the channel 3 receive rule table. Set these bits to a value within the range of 00_H to FF_H.

24.3.4.3 RCFDCnCFDGAFLCFG1 — Receive Rule Configuration Register 1

Access: RCFDCnCFDGAFLCFG1 register can be read or written in 32-bit units

RCFDCnCFDGAFLCFG1L, RCFDCnCFDGAFLCFG1H registers can be read or written in 16-bit units

RCFDCnCFDGAFLCFG1LL, RCFDCnCFDGAFLCFG1LH, RCFDCnCFDGAFLCFG1HL, RCFDCnCFDGAFLCFG1HH registers can be read or written in 8-bit units

Address: RCFDCnCFDGAFLCFG1: <RCFDCn_base> + $00A0_H$

RCFDCnCFDGAFLCFG1L: <RCFDCn_base> + $00A0_H$,

RCFDCnCFDGAFLCFG1H: <RCFDCn_base> + $00A2_H$

RCFDCnCFDGAFLCFG1LL: <RCFDCn_base> + $00A0_H$,

RCFDCnCFDGAFLCFG1LH: <RCFDCn_base> + $00A1_H$,

RCFDCnCFDGAFLCFG1HL: <RCFDCn_base> + $00A2_H$,

RCFDCnCFDGAFLCFG1HH: <RCFDCn_base> + $00A3_H$

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RNC4[7:0]								RNC5[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RNC6[7:0]								RNC7[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 24.55 RCFDCnCFDGAFLCFG1 Register Contents

Bit Position	Bit Name	Function
31 to 24	RNC4[7:0]	Number of Rules for Channel 4 Set the number of receive rules exclusively used for channel 4.
23 to 16	RNC5[7:0]	Number of Rules for Channel 5 Set the number of receive rules exclusively used for channel 5.
15 to 8	RNC6[7:0]	Number of Rules for Channel 6 Set the number of receive rules exclusively used for channel 6.
7 to 0	RNC7[7:0]	Number of Rules for Channel 7 Set the number of receive rules exclusively used for channel 7.

Modify the RCFDCnCFDGAFLCFG1 register only in global reset mode.

Up to 128 × (number of channels) rules can be registered in the receive rule table for the entire unit. The number of receive rules per channel should meet the following conditions.

- The maximum number of rules per channel is 255.
- The total number of rules allocated to each channel does not exceed the number of rules that can be registered for the entire unit.

RNC4[7:0] Bits

These bits are used to set the number of rules to be registered in the channel 4 receive rule table. Set these bits to a value within the range of 00_H to FF_H.

RNC5[7:0] Bits

These bits are used to set the number of rules to be registered in the channel 5 receive rule table. Set these bits to a value within the range of 00_H to FF_H.

RNC6[7:0] Bits

These bits are used to set the number of rules to be registered in the channel 6 receive rule table. Set these bits to a value within the range of 00_H to FF_H.

RNC7[7:0] Bits

These bits are used to set the number of rules to be registered in the channel 7 receive rule table. Set these bits to a value within the range of 00_H to FF_H.

24.3.4.4 RCFDCnCFDGAFLIDj — Receive Rule ID Register (j = 0 to 15)

Access: RCFDCnCFDGAFLIDj register can be read or written in 32-bit units

RCFDCnCFDGAFLIDjL, RCFDCnCFDGAFLIDjH registers can be read or written in 16-bit units

RCFDCnCFDGAFLIDjLL, RCFDCnCFDGAFLIDjLH, RCFDCnCFDGAFLIDjHL, RCFDCnCFDGAFLIDjHH registers can be read or written in 8-bit units

Address: RCFDCnCFDGAFLIDj: <RCFDCn_base> + 1000_H + (10_H × j)

RCFDCnCFDGAFLIDjL: <RCFDCn_base> + 1000_H + (10_H × j),

RCFDCnCFDGAFLIDjH: <RCFDCn_base> + 1002_H + (10_H × j)

RCFDCnCFDGAFLIDjLL: <RCFDCn_base> + 1000_H + (10_H × j),

RCFDCnCFDGAFLIDjLH: <RCFDCn_base> + 1001_H + (10_H × j),

RCFDCnCFDGAFLIDjHL: <RCFDCn_base> + 1002_H + (10_H × j),

RCFDCnCFDGAFLIDjHH: <RCFDCn_base> + 1003_H + (10_H × j)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GAFLIDE	GAFLRTR	GAFLLB	GAFLID[28:16]												
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GAFLID[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 24.56 RCFDCnCFDGAFLIDj Register Contents

Bit Position	Bit Name	Function
31	GAFLIDE	IDE Select 0: Standard ID 1: Extended ID
30	GAFLRTR	RTR Select 0: Data frame 1: Remote frame
29	GAFLLB	Receive Rule Target Message Select 0: When a message transmitted from another CAN node is received 1: When the own transmitted message is received
28 to 0	GAFLID[28:0]	ID Set the ID of the receive rule. For the standard ID, set the ID in bits b10 to b0 and set bits b28 to b11 to 0.

Modify the RCFDCnCFDGAFLIDj register when the AFLDAE bit in the RCFDCnCFDGAFLECTR register is set to 1 (receive rule table write is enabled) in global reset mode.

GAFLIDE Bit

This bit is used to select the ID format (standard ID or extended ID) of the receive rule. This bit is compared with the IDE bit in the received message during the acceptance filter processing.

GAFLRTR Bit

This bit is used to select the frame format (data frame or remote frame) of the receive rule. This bit is compared with the RTR bit in the received message during the acceptance filter processing.

GAFLLB Bit

When this bit is set to 0, data processing using the receive rule is performed when receiving messages transmitted from another CAN node.

When this bit is set to 1 when the mirror function is used, data processing using the receive rule is performed when the CAN node is receiving its own transmitted messages.

GAFLID[28:0] Bits

These bits are used to set the ID field of the receive rule. The ID value set by these bits is compared with the ID of the received message during the acceptance filter processing.

24.3.4.5 RCFDCnCFDGAFLMj — Receive Rule Mask Register (j = 0 to 15)

Access: RCFDCnCFDGAFLMj register can be read or written in 32-bit units

RCFDCnCFDGAFLMjL, RCFDCnCFDGAFLMjH registers can be read or written in 16-bit units

RCFDCnCFDGAFLMjLL, RCFDCnCFDGAFLMjLH, RCFDCnCFDGAFLMjHL, RCFDCnCFDGAFLMjHH registers can be read or written in 8-bit units

Address: RCFDCnCFDGAFLMj: <RCFDCn_base> + 1004_H + (10_H × j)

RCFDCnCFDGAFLMjL: <RCFDCn_base> + 1004_H + (10_H × j),

RCFDCnCFDGAFLMjH: <RCFDCn_base> + 1006_H + (10_H × j)

RCFDCnCFDGAFLMjLL: <RCFDCn_base> + 1004_H + (10_H × j),

RCFDCnCFDGAFLMjLH: <RCFDCn_base> + 1005_H + (10_H × j),

RCFDCnCFDGAFLMjHL: <RCFDCn_base> + 1006_H + (10_H × j),

RCFDCnCFDGAFLMjHH: <RCFDCn_base> + 1007_H + (10_H × j)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GAFLIDEM	GAFLRTRM	—	GAFLIDM[28:16]												
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GAFLIDM[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 24.57 RCFDCnCFDGAFLMj Register Contents

Bit Position	Bit Name	Function
31	GAFLIDEM	IDE Mask 0: The IDE bit is not compared. 1: The IDE bit is compared.
30	GAFLRTRM	RTR Mask 0: The RTR bit is not compared. 1: The RTR bit is compared.
29	Reserved	This bit is read as the value after reset. The write value should be the value after reset.
28 to 0	GAFLIDM[28:0]	ID Mask 0: The corresponding ID bit is not compared. 1: The corresponding ID bit is compared.

Modify the RCFDCnCFDGAFLMj register when the AFLDAE bit in the RCFDCnCFDGAFLECTR register is set to 1 (receive rule table write is enabled) in global reset mode.

GAFLIDEM Bit

When this bit is set to 1, filter processing is performed only for messages of the ID format specified by the GAFLIDE bit in the RCFDCnCFDGAFLIDj register.

When this bit is cleared to 0, the IDs of all the receive messages and the specified IDs are regarded as matched. To set the GAFLIDEM bit to 0, set all the GAFLIDM[28:0] bits to 0 at the same time.

GAFLRTRM Bit

This bit is used to mask the RTR bit of the receive rule.

GAFLIDM[28:0] Bits

These bits are used to mask the corresponding ID bit of the receive rule.

24.3.4.6 RCFDCnCFDGAFLP0_j — Receive Rule Pointer 0 Register (j = 0 to 15)

Access: RCFDCnCFDGAFLP0_j register can be read or written in 32-bit units

RCFDCnCFDGAFLP0_jL, RCFDCnCFDGAFLP0_jH registers can be read or written in 16-bit units

RCFDCnCFDGAFLP0_jLL, RCFDCnCFDGAFLP0_jLH, RCFDCnCFDGAFLP0_jHL, RCFDCnCFDGAFLP0_jHH registers can be read or written in 8-bit units

Address: RCFDCnCFDGAFLP0_j: <RCFDCn_base> + 1008_H + (10_H × j)

RCFDCnCFDGAFLP0_jL: <RCFDCn_base> + 1008_H + (10_H × j),

RCFDCnCFDGAFLP0_jH: <RCFDCn_base> + $100A_H$ + (10_H × j)

RCFDCnCFDGAFLP0_jLL: <RCFDCn_base> + 1008_H + (10_H × j),

RCFDCnCFDGAFLP0_jLH: <RCFDCn_base> + 1009_H + (10_H × j),

RCFDCnCFDGAFLP0_jHL: <RCFDCn_base> + $100A_H$ + (10_H × j),

RCFDCnCFDGAFLP0_jHH: <RCFDCn_base> + $100B_H$ + (10_H × j)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GAFLPTR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GAFLRMV	GAFLRMDP[6:0]							—	—	—	—	GAFLDLC[3:0]			
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Table 24.58 RCFDCnCFDGAFLP0_j Register Contents

Bit Position	Bit Name	Function
31 to 16	GAFLPTR[15:0]	Receive Rule Label Set the 16-bit label information.
15	GAFLRMV	Receive Buffer Enable 0: No receive buffer is used. 1: A receive buffer is used.
14 to 8	GAFLRMDP[6:0]	Receive Buffer Number Select Set the receive buffer number to store receive messages.
7 to 4	Reserved	These bits are read as the value after reset. The write value should be the value after reset.

Table 24.58 RCFDCnCFDGAFLP0_j Register Contents

Bit Position	Bit Name	Function					
3 to 0	GAFLDLC[3:0]	Receive Rule DLC					
		b3	b2	b1	b0	Classical CAN Frame	CAN FD Frame
		0	0	0	0	DLC check is disabled	
		0	0	0	1	1 data byte	
		0	0	1	0	2 data bytes	
		0	0	1	1	3 data bytes	
		0	1	0	0	4 data bytes	
		0	1	0	1	5 data bytes	
		0	1	1	0	6 data bytes	
		0	1	1	1	7 data bytes	
		1	0	0	0	8 data bytes	
		1	0	0	1	8 data bytes	12 data bytes
		1	0	1	0		16 data bytes
		1	0	1	1		20 data bytes
		1	1	0	0		24 data bytes
		1	1	0	1		32 data bytes
		1	1	1	0		48 data bytes
		1	1	1	1		64 data bytes

Modify the RCFDCnCFDGAFLP0_j register when the AFLDAE bit in the RCFDCnCFDGAFLECTR register is set to 1 (receive rule table write is enabled) in global reset mode.

GAFLPTR[15:0] Bits

These bits are used to set a 16-bit label to be attached to messages that have passed through the filter. A label is attached when a message is stored in the receive buffer or the FIFO buffer.

GAFLRMV Bit

When this bit is set to 1, receive messages that have passed through the filter are stored in the receive buffer selected by the GAFLRMDP[6:0] bits.

GAFLRMDP[6:0] Bits

These bits are used to select the number of the receive buffer that stores receive messages that have passed through the filter when the GAFLRMV bit is set to 1. Set these bits to a value smaller than the setting value by the NRXMB[7:0] bits in the RCFDCnCFDRMNB register.

GAFLDLC[3:0] Bits

These bits are used to set the minimum data length necessary for receiving messages. If the data length of a message that is being filtered is equal to or larger than the value set by the GAFLDLC[3:0] bits, the message passes the DLC check. Setting these bits to 0000_B disables the DLC check function allowing messages with any data length to pass the DLC check.

24.3.4.7 RCFDCnCFDGAFLP1_j — Receive Rule Pointer 1 Register (j = 0 to 15)

Access: RCFDCnCFDGAFLP1_j register can be read or written in 32-bit units

RCFDCnCFDGAFLP1_jL, RCFDCnCFDGAFLP1_jH registers can be read or written in 16-bit units

RCFDCnCFDGAFLP1_jLL, RCFDCnCFDGAFLP1_jLH, RCFDCnCFDGAFLP1_jHL, RCFDCnCFDGAFLP1_jHH registers can be read or written in 8-bit units

Address: RCFDCnCFDGAFLP1_j: <RCFDCn_base> + $100C_H$ + (10_H × j)

RCFDCnCFDGAFLP1_jL: <RCFDCn_base> +$100C_H$ + (10_H × j),

RCFDCnCFDGAFLP1_jH: <RCFDCn_base> + $100E_H$ + (10_H × j)

RCFDCnCFDGAFLP1_jLL: <RCFDCn_base> + $100C_H$ + (10_H × j),

RCFDCnCFDGAFLP1_jLH: <RCFDCn_base> + $100D_H$ + (10_H × j),

RCFDCnCFDGAFLP1_jHL: <RCFDCn_base> + $100E_H$ + (10_H × j),

RCFDCnCFDGAFLP1_jHH: <RCFDCn_base> + $100F_H$ + (10_H × j)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GAFLFDP[31:16]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GAFLFDP[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 24.59 RCFDCnCFDGAFLP1_j Register Contents

Bit Position	Bit Name	Function
31 to 8	GAFLFDP[31:8]	Transmit/Receive FIFO Buffer k Select (Bit position –8 = target transmit/receive FIFO buffer number k) 0: Transmit/receive FIFO buffer is not selected. 1: Transmit/receive FIFO buffer is selected.
7 to 0	GAFLFDP[7:0]	Receive FIFO Buffer x Select (Bit position = target receive FIFO buffer number x) 0: Receive FIFO buffer is not selected. 1: Receive FIFO buffer is selected.

Modify the RCFDCnCFDGAFLP1_j register when the AFLDAE bit in the RCFDCnCFDGAFLECTR register is set to 1 (receive rule table write is enabled) in global reset mode.

GAFLFDP[31:0] Bits

These bits are used to specify FIFO buffers that store receive messages that have passed through the filter. Up to eight FIFO buffers can be selected. However, when the GAFLRMV bit in the RCFDCnCFDGAFLP0_j register is set to 1 (messages are stored in the receive buffer), up to seven FIFO buffers can be selected. Only receive FIFO buffers and the transmit/receive FIFO buffer for which the CFM[1:0] bits in the RCFDCnCFDCFCCk register are set to 00_B (receive mode) or 10_B (gateway mode) can be selected.

24.3.5 Details of Receive Buffer-related Registers

24.3.5.1 RCFDCnCFDRMNB — Receive Buffer Number Register

Access: RCFDCnCFDRMNB register can be read or written in 32-bit units
RCFDCnCFDRMNBL register can be read or written in 16-bit units
RCFDCnCFDRMNBLL, RCFDCnCFDRMNBLH registers can be read or written in 8-bit units

Address: RCFDCnCFDRMNB: <RCFDCn_base> + $00A4_H$
RCFDCnCFDRMNBL: <RCFDCn_base> + $00A4_H$
RCFDCnCFDRMNBLL: <RCFDCn_base> + $00A4_H$,
RCFDCnCFDRMNBLH: <RCFDCn_base> + $00A5_H$

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	RMPLS[2:0]			NRXMB[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 24.60 RCFDCnCFDRMNB Register Contents

Bit Position	Bit Name	Function
31 to 11	Reserved	These bits are read as the value after reset. The write value should be the value after reset.
10 to 8	RMPLS[2:0]	Receive Buffer Payload Storage Size Select b10 b9 b8 0 0 0: 8byte 0 0 1: 12byte 0 1 0: 16byte 0 1 1: 20byte 1 0 0: 24byte 1 0 1: 32byte 1 1 0: 48byte 1 1 1: 64byte
7 to 0	NRXMB[7:0]	Receive Buffer Number Configuration Set the number of receive buffers. Set a value of 0 to 128.

Modify the RCFDCnCFDRMNB register only in global reset mode.

RMPLS[2:0] Bits

These bits are used to select the maximum payload size that can be stored in the receive buffer.

NRXMB[7:0] Bits

These bits are used to set the total number of receive buffers of the RS-CANFD module. The maximum value is 16 × (number of channels).

Setting all of these bits to 0 makes receive buffers unavailable.

24.3.5.2 RCFDCnCFDRMNDy — Receive Buffer New Data Register (y = 0 to 3)

Access: RCFDCnCFDRMNDy register can be read or written in 32-bit units

RCFDCnCFDRMNDyL, RCFDCnCFDRMNDyH registers can be read or written in 16-bit units

RCFDCnCFDRMNDyLL, RCFDCnCFDRMNDyLH, RCFDCnCFDRMNDyHL, RCFDCnCFDRMNDyHH registers can be read or written in 8-bit units

Address: RCFDCnCFDRMNDy: <RCFDCn_base> + $00A8_H$ + (04_H × y)

RCFDCnCFDRMNDyL: <RCFDCn_base> + $00A8_H$ + (04_H × y),

RCFDCnCFDRMNDyH: <RCFDCn_base> + $00AA_H$ + (04_H × y)

RCFDCnCFDRMNDyLL: <RCFDCn_base> + $00A8_H$ + (04_H × y),

RCFDCnCFDRMNDyLH: <RCFDCn_base> + $00A9_H$ + (04_H × y),

RCFDCnCFDRMNDyHL: <RCFDCn_base> + $00AA_H$ + (04_H × y),

RCFDCnCFDRMNDyHH: <RCFDCn_base> + $00AB_H$ + (04_H × y)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RMNSq (q = y × 32 + 31 to y × 32 + 16 (y = 0, 1, 2, 3))															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RMNSq (q = y × 32 + 15 to y × 32 + 0 (y = 0, 1, 2, 3))															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 24.61 RCFDCnCFDRMNDy Register Contents

Bit Position	Bit Name	Function
31 to 16	RMNSq	Receive Buffer Receive Complete Flag q (q = y × 32 + 31 to y × 32 + 16) 0: There is no new message in receive buffer q. 1: There is a new message in receive buffer q.
15 to 0	RMNSq	Receive Buffer Receive Complete Flag q (q = y × 32 + 15 to y × 32 + 0) 0: There is no new message in receive buffer q. 1: There is a new message in receive buffer q.

Write 0 to the RCFDCnCFDRMNDy register in global operating mode or global test mode.

RMNSq Flags (q = 0 to 127)

Each RMNSq flag is set to 1 when the processing for storing a message in the corresponding receive buffer starts.

To clear a flag to 0, the program must write 0 to the flag. Use a store instruction to write “0” to the flag and “1” to other flags. These bits cannot be set to 0 while a message is being stored. The message storing time depends on the storage payload size of the receive buffer. When the RMPLS[2:0] value in the RCFDCnCFDRMNB register is 000_B (8 bytes), the message storing time is 12 pclk clock cycles.

When the RMPLS[2:0] value is 111_B (64 bytes), the message storing time is 40 pclk clock cycles. (2 pclk clock cycles per 4 bytes of storage payload size). These flags are cleared to 0 in global reset mode.

24.3.5.3 RCFDCnCFDRMIDq — Receive Buffer ID Register (q = 0 to 127)

Access: RCFDCnCFDRMIDq register is a read-only register that can be read in 32-bit units

RCFDCnCFDRMIDqL, RCFDCnCFDRMIDqH registers are read-only registers that can be read in 16-bit units

RCFDCnCFDRMIDqLL, RCFDCnCFDRMIDqLH, RCFDCnCFDRMIDqHL, RCFDCnCFDRMIDqHH registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDRMIDq: <RCFDCn_base> + 2000_H + (80_H × q)

RCFDCnCFDRMIDqL: <RCFDCn_base> + 2000_H + (80_H × q),

RCFDCnCFDRMIDqH: <RCFDCn_base> + 2002_H + (80_H × q)

RCFDCnCFDRMIDqLL: <RCFDCn_base> + 2000_H + (80_H × q),

RCFDCnCFDRMIDqLH: <RCFDCn_base> + 2001_H + (80_H × q),

RCFDCnCFDRMIDqHL: <RCFDCn_base> + 2002_H + (80_H × q),

RCFDCnCFDRMIDqHH: <RCFDCn_base> + 2003_H + (80_H × q)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RMIDE	RMRTR	—	RMID[28:16]												
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RMID[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 24.62 RCFDCnCFDRMIDq Register Contents

Bit Position	Bit Name	Function
31	RMIDE	Receive Buffer IDE 0: Standard ID 1: Extended ID
30	RMRTR	Receive Buffer RTR/RRS • When the received message is a classical CAN frame 0: Data frame 1: Remote frame • When the received message is a CAN FD frame The RRS bit value of the received message can be read.
29	Reserved	This bit is read as the value after reset.
28 to 0	RMID[28:0]	Receive Buffer ID Data These bits contain the standard ID or extended ID of the received message. Read bits b10 to b0 for standard ID. Bits b28 to b11 are read as 0.

RMIDE Bit

This bit indicates the ID format (standard ID or extended ID) of the message stored in the receive buffer.

RMRTR Bit

When the received message is a classical CAN frame, this bit indicates the frame format (data frame or remote frame) of the message stored in the receive buffer. When the received message is a CAN FD frame, this bit indicates the RRS bit value in the message.

RMID[28:0] Bits

These bits contain the ID of the message stored in the receive buffer.

24.3.5.4 RCFDCnCFDRMPTRq — Receive Buffer Pointer Register (q = 0 to 127)

Access: RCFDCnCFDRMPTRq register is a read-only register that can be read in 32-bit units

RCFDCnCFDRMPTRqL, RCFDCnCFDRMPTRqH registers are read-only registers that can be read in 16-bit units

RCFDCnCFDRMPTRqLL, RCFDCnCFDRMPTRqLH, RCFDCnCFDRMPTRqHH registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDRMPTRq: <RCFDCn_base> + 2004_H + (80_H × q)

RCFDCnCFDRMPTRqL: <RCFDCn_base> + 2004_H + (80_H × q),

RCFDCnCFDRMPTRqH: <RCFDCn_base> + 2006_H + (80_H × q)

RCFDCnCFDRMPTRqLL: <RCFDCn_base> + 2004_H + (80_H × q),

RCFDCnCFDRMPTRqLH: <RCFDCn_base> + 2005_H + (80_H × q),

RCFDCnCFDRMPTRqHH: <RCFDCn_base> + 2007_H + (80_H × q)

Value after reset: 0000 0000_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RMDLC[3:0]				—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RMTS[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 24.63 RCFDCnCFDRMPTRq Register Contents

Bit Position	Bit Name	Function
31 to 28	RMDLC[3:0]	Receive Buffer DLC Data
27 to 16	Reserved	These bits are read as the value after reset.
15 to 0	RMTS[15:0]	Receive Buffer Timestamp Data Timestamp value of the received message.

b31	b30	b29	b28	Classical CAN Frame	CAN FD Frame
0	0	0	0	0 data bytes	
0	0	0	1	1 data byte	
0	0	1	0	2 data bytes	
0	0	1	1	3 data bytes	
0	1	0	0	4 data bytes	
0	1	0	1	5 data bytes	
0	1	1	0	6 data bytes	
0	1	1	1	7 data bytes	
1	0	0	0	8 data bytes	
1	0	0	1	8 data bytes	12 data bytes
1	0	1	0		16 data bytes
1	0	1	1		20 data bytes
1	1	0	0		24 data bytes
1	1	0	1		32 data bytes
1	1	1	0		48 data bytes
1	1	1	1		64 data bytes

RMDLC[3:0] Bits

These bits indicate the data length of the message stored in the receive buffer. The number of bytes of the payload to be stored in the receive buffer is determined by the RMPLS[2:0] bits in the RCFDCnCFDRMNB register.

RMTS[15:0] Bits

These bits indicate the timestamp value of the message stored in the receive buffer.

24.3.5.5 RCFDCnCFDRMFDSTSq — Receive Buffer CAN FD Status Register (q = 0 to 127)

Access: RCFDCnCFDRMFDSTSq register is a read-only register that can be read in 32-bit units

RCFDCnCFDRMFDSTSqL, RCFDCnCFDRMFDSTSqH registers are read-only registers that can be read in 16-bit units

RCFDCnCFDRMFDSTSqLL, RCFDCnCFDRMFDSTSqHL, RCFDCnCFDRMFDSTSqHH registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDRMFDSTSq: <RCFDCn_base> + 2008_H + (80_H × q)

RCFDCnCFDRMFDSTSqL: <RCFDCn_base> + 2008_H + (80_H × q),

RCFDCnCFDRMFDSTSqH: <RCFDCn_base> + $200A_H$ + (80_H × q)

RCFDCnCFDRMFDSTSqLL: <RCFDCn_base> + 2008_H + (80_H × q),

RCFDCnCFDRMFDSTSqHL: <RCFDCn_base> + $200A_H$ + (80_H × q),

RCFDCnCFDRMFDSTSqHH: <RCFDCn_base> + $200B_H$ + (80_H × q)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RMPTR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	RMFDF	RMBRS	RMESI
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 24.64 RCFDCnCFDRMFDSTSq Register Contents

Bit Position	Bit Name	Function
31 to 16	RMPTR[15:0]	Receive Buffer Label Data Label information of the received message.
15 to 3	Reserved	These bits are read as the value after reset.
2	RMFDF	FDF 0: Classical CAN frame 1: CAN FD frame
1	RMBRS	BRS 0: The bit rate in the data area does not change. 1: The bit rate in the data area changes.
0	RMESI	ESI 0: Error active node 1: Error passive node

RMPTR[15:0] Bits

These bits indicate the label information of the message stored in the receive buffer.

RMFDF Bit

This bit indicates the FD format (classical CAN frame or CAN FD frame) of the message stored in the receive buffer.

RMBRS Bit

When the RMFDF bit is set to 1, this bit indicates the BRS bit value of the message stored in the receive buffer. When the RMFDF bit is set to 0, this bit is always read as 0.

RMESI Bit

When the RMFDF bit is set to 1, this bit indicates the ESI bit value of the message stored in the receive buffer. When the RMFDF bit is set to 0, this bit is always read as 0.

24.3.5.6 RCFDCnCFDRMDFb_q — Receive Buffer Data Field Register (b = 0 to 15, q = 0 to 127)

Access: RCFDCnCFDRMDFb_q register is a read-only register that can be read in 32-bit units

RCFDCnCFDRMDFb_qL, RCFDCnCFDRMDFb_qH registers are read-only registers that can be read in 16-bit units

RCFDCnCFDRMDFb_qLL, RCFDCnCFDRMDFb_qLH, RCFDCnCFDRMDFb_qHL, RCFDCnCFDRMDFb_qHH registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDRMDFb_q: <RCFDCn_base> + $200C_H$ + (04_H × b) + (80_H × q)

RCFDCnCFDRMDFb_qL: <RCFDCn_base> + $200C_H$ + (04_H × b) + (80_H × q),

RCFDCnCFDRMDFb_qH: <RCFDCn_base> + $200E_H$ + (04_H × b) + (80_H × q)

RCFDCnCFDRMDFb_qLL: <RCFDCn_base> + $200C_H$ + (04_H × b) + (80_H × q),

RCFDCnCFDRMDFb_qLH: <RCFDCn_base> + $200D_H$ + (04_H × b) + (80_H × q),

RCFDCnCFDRMDFb_qHL: <RCFDCn_base> + $200E_H$ + (04_H × b) + (80_H × q),

RCFDCnCFDRMDFb_qHH: <RCFDCn_base> + $200F_H$ + (04_H × b) + (80_H × q)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RMDB4 × b + 3 [7:0]								RMDB4 × b + 2 [7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RMDB4 × b + 1 [7:0]								RMDB4 × b + 0 [7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 24.65 RCFDCnCFDRMDFb_q Register Contents

Bit Position	Bit Name	Function
31 to 24	RMDB4 × b + 3 [7:0]	Receive Buffer Data Byte 4 × b + 3 Receive Buffer Data Byte 4 × b + 2 Receive Buffer Data Byte 4 × b + 1 Receive Buffer Data Byte 4 × b + 0 Data for a message stored in the receive buffer can be read.
23 to 16	RMDB4 × b + 2 [7:0]	
15 to 8	RMDB4 × b + 1 [7:0]	
7 to 0	RMDB4 × b + 0 [7:0]	

When the RMDLC[3:0] value in the RCFDCnCFDRMPTRq register is smaller than the payload storage size of the receive buffer, data bytes for which no data is set are read as 00_H.

Specify the payload storage size of the receive buffer by the RMPLS[2:0] bits in the RCFDCnCFDRMNB register. Do not read or write the RCFDCnCFDRMDFb_q register corresponding to an area that exceeds the specified size.

24.3.6 Details of Receive FIFO Buffer-related Registers

24.3.6.1 RCFDCnCFDRFCCx — Receive FIFO Buffer Configuration and Control Register (x = 0 to 7)

Access: RCFDCnCFDRFCCx register can be read or written in 32-bit units

RCFDCnCFDRFCCxL register can be read or written in 16-bit units

RCFDCnCFDRFCCxLL, RCFDCnCFDRFCCxLH registers can be read or written in 8-bit units

Address: RCFDCnCFDRFCCx: <RCFDCn_base> + $00B8_H$ + (04_H × x)

RCFDCnCFDRFCCxL: <RCFDCn_base> + $00B8_H$ + (04_H × x)

RCFDCnCFDRFCCxLL: <RCFDCn_base> + $00B8_H$ + (04_H × x),

RCFDCnCFDRFCCxLH: <RCFDCn_base> + $00B9_H$ + (04_H × x)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RFIGCV[2:0]			RFIM	—	RFDC[2:0]			—	RFPLS[2:0]			—	—	RFIE	RFE
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R/W	R/W

Table 24.66 RCFDCnCFDRFCCx Register Contents

Bit Position	Bit Name	Function
31 to 16	Reserved	These bits are read as the value after reset. The write value should be the value after reset.
15 to 13	RFIGCV[2:0]	Receive FIFO Interrupt Request Timing Select b15 b14 b13 0 0 0: When FIFO is 1/8 full. 0 0 1: When FIFO is 2/8 full. 0 1 0: When FIFO is 3/8 full. 0 1 1: When FIFO is 4/8 full. 1 0 0: When FIFO is 5/8 full. 1 0 1: When FIFO is 6/8 full. 1 1 0: When FIFO is 7/8 full. 1 1 1: When FIFO is full.
12	RFIM	Receive FIFO Interrupt Source Select 0: An interrupt occurs when the condition set by the RFIGCV[2:0] bits is met. 1: An interrupt occurs each time a message has been received.
11	Reserved	This bit is read as the value after reset. The write value should be the value after reset.

Table 24.66 RCFDCnCFDRFCCx Register Contents

Bit Position	Bit Name	Function
10 to 8	RFDC[2:0]	Receive FIFO Buffer Depth Configuration b10 b9 b8 0 0 0: 0 messages 0 0 1: 4 messages 0 1 0: 8 messages 0 1 1: 16 messages 1 0 0: 32 messages 1 0 1: 48 messages 1 1 0: 64 messages 1 1 1: 128 messages
7	Reserved	This bit is read as the value after reset. The write value should be the value after reset.
6 to 4	RFPLS[2:0]	Receive FIFO Buffer Payload Storage Size Select b6 b5 b4 0 0 0: 8 bytes 0 0 1: 12 bytes 0 1 0: 16 bytes 0 1 1: 20 bytes 1 0 0: 24 bytes 1 0 1: 32 bytes 1 1 0: 48 bytes 1 1 1: 64 bytes
3, 2	Reserved	These bits are read as the value after reset. The write value should be the value after reset.
1	RFIE	Receive FIFO Interrupt Enable 0: Receive FIFO interrupt is disabled. 1: Receive FIFO interrupt is enabled.
0	RFE	Receive FIFO Buffer Enable 0: No receive FIFO buffer is used. 1: Receive FIFO buffers are used.

RFIGCV[2:0] Bits

These bits are used to specify the number of received messages required to generate a receive FIFO interrupt request when the RFIM bit is set to 0 with a fraction for the total number of buffers (the setting of RFDC[2:0]).

When the RFDC[2:0] bits are set to 001_B (4 messages), set the RFIGCV[2:0] bits to 001_B, 011_B, 101_B, or 111_B. Modify these bits only in global reset mode.

RFIM Bit

This bit is used to select a FIFO interrupt source. Modify this bit only in global reset mode.

RFDC[2:0] Bits

These bits are used to select the number of messages that can be stored in a single receive FIFO buffer. When these bits are set to 000_B, no receive FIFO buffer should be used. Modify these bits only in global reset mode.

RFPLS[2:0] Bits

These bits are used to select the maximum payload size that can be stored in the receive FIFO buffer. Modify these bits only in global reset mode.

RFIE Bit

Setting the RFIE bit to 1 enables receive FIFO interrupts. Modify this bit when the RFE bit is set to 0 (no receive FIFO buffer is used).

RFE Bit

Setting the RFE bit to 1 enables the use of FIFO buffers. Clearing this bit to 0 sets the RFEMP flag in the RCFDCnCFDRFSTSx register to 1 (buffer empty). Modify this bit in global operating mode or global test mode. Set this bit to 1 with another instruction after the settings to all bits in the RCFDCnCFDRFCCx register have been done. This bit is cleared to 0 in global reset mode.

24.3.6.2 RCFDCnCFDRFSTSx — Receive FIFO Buffer Status Register (x = 0 to 7)

Access: RCFDCnCFDRFSTSx register can be read or written in 32-bit units
RCFDCnCFDRFSTSxL register can be read or written in 16-bit units
RCFDCnCFDRFSTSxLL register can be read or written in 8-bit units
RCFDCnCFDRFSTSxLH register is a read-only register that can be read in 8-bit units

Address: RCFDCnCFDRFSTSx: <RCFDCn_base> + $00D8_H$ + (04_H × x)
RCFDCnCFDRFSTSxL: <RCFDCn_base> + $00D8_H$ + (04_H × x)
RCFDCnCFDRFSTSxLL: <RCFDCn_base> + $00D8_H$ + (04_H × x),
RCFDCnCFDRFSTSxLH: <RCFDCn_base> + $00D9_H$ + (04_H × x)

Value after reset: $0000\ 0001_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RFMC[7:0]								—	—	—	—	RFIF	RFMLT	RFFLL	RFEMP
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R/W*1	R/W*1	R	R

Note 1. The only effective value for writing to this flag bit is 0, which clears the bit. Otherwise writing to the bit results in retention of its state.

Table 24.67 RCFDCnCFDRFSTSx Register Contents

Bit Position	Bit Name	Function
31 to 16	Reserved	These bits are read as the value after reset. When writing to these bits, write the value after reset.
15 to 8	RFMC[7:0]	Receive FIFO Unread Message Counter The number of unread messages stored in the receive FIFO buffer is displayed.
7 to 4	Reserved	These bits are read as the value after reset. When writing to these bits, write the value after reset.
3	RFIF	Receive FIFO Interrupt Request Flag 0: No receive FIFO interrupt request is present. 1: A receive FIFO interrupt request is present.
2	RFMLT	Receive FIFO Message Lost Flag 0: No receive FIFO message is lost. 1: A receive FIFO message is lost.
1	RFFLL	Receive FIFO Buffer Full Status Flag 0: The receive FIFO buffer is not full. 1: The receive FIFO buffer is full.
0	RFEMP	Receive FIFO Buffer Empty Status Flag 0: The receive FIFO buffer contains unread message. 1: The receive FIFO buffer contains no unread message (buffer empty).

RFMC[7:0] Flag

This flag indicates the number of unread messages in the receive FIFO buffer. This flag becomes 00_H when the RFE bit in the RCFDCnCFDRFCCx register is set to 0. This flag is 00_H in global reset mode.

RFIF Flag

This flag is set to 1 when the receive FIFO interrupt request generation conditions set by the RFIGCV[2:0] bits and the RFIM bit in the RCFDCnCFDRFCCx register are met. This flag is cleared to 0 in global reset mode or by writing 0 to this flag. Modify this bit in global operating mode or global test mode.

To clear the flags of the register to 0, the program must write 0 to the corresponding flags to be cleared. When writing 0, using store instruction, set the bit to be set to “0” to “0”, and the bits not to be set to “0” to “1”.

RFMLT Flag

This flag is set to 1 when an attempt is made to store a new message while the receive FIFO buffer is full. In this case, the new message is discarded.

This flag is cleared to 0 in global reset mode or by writing 0 to this flag. Modify this bit in global operating mode or global test mode.

To clear the flags of the register to 0, the program must write 0 to the corresponding flags to be cleared. When writing 0, using store instruction, set the bit to be set to “0” to “0”, and the bits not to be set to “0” to “1”.

RFFLL Flag

This flag is set to 1 when the number of messages stored in the receive FIFO buffer matches the FIFO buffer depth set by the RFDC[2:0] bits in the RCFDCnCFDRFCCx register.

If the number of messages stored in the receive FIFO buffer becomes smaller than the FIFO buffer depth set by the RFDC[2:0] bits, this flag is cleared to 0. This flag is also cleared to 0 when the RFE bit in the RCFDCnCFDRFCCx register is set to 0 (no receive FIFO buffer is used) or in global reset mode.

RFEMP Flag

This flag is set to 1 when all messages in the receive FIFO buffer have been read. This flag is also set to 1 when the RFE bit in the RCFDCnCFDRFCCx register is 0 or in global reset mode.

This flag is cleared to 0 when a received message is in the receive FIFO buffer.

NOTE

To clear the RFMLT or RFIF flag to 0, use a store instruction to write “0” to the given flag and “1” to the other flags.

24.3.6.3 RCFDCnCFDRFPCTRx — Receive FIFO Buffer Pointer Control Register (x = 0 to 7)

Access: RCFDCnCFDRFPCTRx register is a write-only register that can be written in 32-bit units

RCFDCnCFDRFPCTRxL register is a write-only register that can be written in 16-bit units

RCFDCnCFDRFPCTRxLL register is a write-only register that can be written in 8-bit units

Address: RCFDCnCFDRFPCTRx: <RCFDCn_base> + $00F8_H$ + (04_H × x)

RCFDCnCFDRFPCTRxL: <RCFDCn_base> + $00F8_H$ + (04_H × x)

RCFDCnCFDRFPCTRxLL: <RCFDCn_base> + $00F8_H$ + (04_H × x)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	RFPC[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	W	W	W	W	W	W	W	W

Table 24.68 RCFDCnCFDRFPCTRx Register Contents

Bit Position	Bit Name	Function
31 to 8	Reserved	The write value should be the value after reset.
7 to 0	RFPC[7:0]	Receive FIFO Pointer Control When these bits are set to FF_H, the read pointer moves to the next unread message in the receive FIFO buffer.

When the RFDMAEx value in the RCFDCnCFDCDTCT register is 1 (DMA transfer request enabled), do not write a value to this register.

RFPC[7:0] Bits

When the RFPC[7:0] bits are set to FF_H, the read pointer moves to the next unread message in the receive FIFO buffer. At this time, the RFMC[7:0] (receive FIFO unread message counter) value in the RCFDCnCFDRFSTSx register is decremented by 1. Read the RCFDCnCFDRFIDx, RCFDCnCFDRFPTRx, RCFDCnCFDRFFDSTSx, and RCFDCnCFDRFDFd_x registers to read messages in the receive FIFO buffer, and then write FF_H to the RFPC[7:0] bits.

When writing FF_H to these bits, make sure that the RFE bit in the RCFDCnCFDRFCCx register is set to 1 (receive FIFO buffers are used) and the RFEMP flag in the RCFDCnCFDRFSTSx register is 0 (the receive FIFO buffer contains unread messages).

24.3.6.4 RCFDCnCFDRFIDx — Receive FIFO Buffer Access ID Register (x = 0 to 7)

Access: RCFDCnCFDRFIDx register is a read-only register that can be read in 32-bit units

RCFDCnCFDRFIDxL, RCFDCnCFDRFIDxH registers are read-only registers that can be read in 16-bit units

RCFDCnCFDRFIDxLL, RCFDCnCFDRFIDxLH, RCFDCnCFDRFIDxHL, RCFDCnCFDRFIDxHH registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDRFIDx: <RCFDCn_base> + 6000_H + (80_H × x)

RCFDCnCFDRFIDxL: <RCFDCn_base> + 6000_H + (80_H × x),

RCFDCnCFDRFIDxH: <RCFDCn_base> + 6002_H + (80_H × x)

RCFDCnCFDRFIDxLL: <RCFDCn_base> + 6000_H + (80_H × x),

RCFDCnCFDRFIDxLH: <RCFDCn_base> + 6001_H + (80_H × x),

RCFDCnCFDRFIDxHL: <RCFDCn_base> + 6002_H + (80_H × x),

RCFDCnCFDRFIDxHH: <RCFDCn_base> + 6003_H + (80_H × x)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RFIDE	RFRTR	—	RFID[28:16]												
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RFID[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 24.69 RCFDCnCFDRFIDx Register Contents

Bit Position	Bit Name	Function
31	RFIDE	Receive FIFO Buffer IDE 0: Standard ID 1: Extended ID
30	RFRTR	Receive FIFO Buffer RTR/RRS • When the received message is a classical CAN frame 0: Data frame 1: Remote frame • When the received message is a CAN FD frame The RRS bit value of the received message can be read.
29	Reserved	This bit is read as the value after reset.
28 to 0	RFID[28:0]	Receive FIFO Buffer ID Data The standard ID or extended ID of received message can be read. Read bits b10 to b0 for standard ID. Bits b28 to b11 are read as 0.

RFIDE Bit

This bit indicates the ID format (standard ID or extended ID) of the message stored in the receive FIFO buffer.

RFRTR Bit

When the received message is a classical CAN frame, this bit indicates the frame format (data frame or remote frame) of the message stored in the receive FIFO buffer. When the received message is a CAN FD frame, this bit indicates the RRS bit value in the message.

RFID[28:0] Bits

These bits indicate the ID of the message stored in the receive FIFO buffer.

24.3.6.5 RCFDCnCFDRFPTRx — Receive FIFO Buffer Access Pointer Register (x = 0 to 7)

Access: RCFDCnCFDRFPTRx register is a read-only register that can be read in 32-bit units

RCFDCnCFDRFPTRxL, RCFDCnCFDRFPTRxH registers are read-only registers that can be read in 16-bit units

RCFDCnCFDRFPTRxLL, RCFDCnCFDRFPTRxLH, RCFDCnCFDRFPTRxHH registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDRFPTRx: <RCFDCn_base> + 6004_H + (80_H × x)

RCFDCnCFDRFPTRxL: <RCFDCn_base> + 6004_H + (80_H × x),

RCFDCnCFDRFPTRxH: <RCFDCn_base> + 6006_H + (80_H × x)

RCFDCnCFDRFPTRxLL: <RCFDCn_base> + 6004_H + (80_H × x),

RCFDCnCFDRFPTRxLH: <RCFDCn_base> + 6005_H + (80_H × x),

RCFDCnCFDRFPTRxHH: <RCFDCn_base> + 6007_H + (80_H × x)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RFDLC[3:0]				—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RFTS[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 24.70 RCFDCnCFDRFPTRx Register Contents

Bit Position	Bit Name	Function
31 to 28	RFDLC[3:0]	Receive FIFO Buffer DLC Data

b31	b30	b29	b28	Classical CAN Frame	CAN FD Frame
0	0	0	0	0 data bytes	
0	0	0	1	1 data byte	
0	0	1	0	2 data bytes	
0	0	1	1	3 data bytes	
0	1	0	0	4 data bytes	
0	1	0	1	5 data bytes	
0	1	1	0	6 data bytes	
0	1	1	1	7 data bytes	
1	0	0	0	8 data bytes	
1	0	0	1	8 data bytes	12 data bytes
1	0	1	0		16 data bytes
1	0	1	1		20 data bytes
1	1	0	0		24 data bytes
1	1	0	1		32 data bytes
1	1	1	0		48 data bytes
1	1	1	1		64 data bytes

27 to 16	Reserved	These bits are read as the value after reset.
15 to 0	RFTS[15:0]	Receive FIFO Buffer Timestamp Data Timestamp value of the received message can be read.

RFDLC[3:0] Bits

These bits contain the data length of the message stored in the receive FIFO buffer.

RFTS[15:0] Bits

These bits contain the timestamp value of the message stored in the receive FIFO buffer.

24.3.6.6 RCFDCnCFDRFFDSTSx — Receive FIFO CAN FD Status Register (x = 0 to 7)

Access: RCFDCnCFDRFFDSTSx register is a read-only register that can be read in 32-bit units
RCFDCnCFDRFFDSTSxL, RCFDCnCFDRFFDSTSxH registers are read-only registers that can be read in 16-bit units
RCFDCnCFDRFFDSTSxLL, RCFDCnCFDRFFDSTSxHL, RCFDCnCFDRFFDSTSxHH registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDRFFDSTSx: <RCFDCn_base> + 6008_H + (80_H × x)
RCFDCnCFDRFFDSTSxL: <RCFDCn_base> + 6008_H + (80_H × x),
RCFDCnCFDRFFDSTSxH: <RCFDCn_base> + $600A_H$ + (80_H × x)
RCFDCnCFDRFFDSTSxLL: <RCFDCn_base> + 6008_H + (80_H × x),
RCFDCnCFDRFFDSTSxHL: <RCFDCn_base> + $600A_H$ + (80_H × x),
RCFDCnCFDRFFDSTSxHH: <RCFDCn_base> + $600B_H$ + (80_H × x)

Value after reset: 0000 0000_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RFPTR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	RFFDF	RFBRS	RFESI
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 24.71 RCFDCnCFDRFFDSTSx Register Contents

Bit Position	Bit Name	Function
31 to 16	RFPTR[15:0]	Receive FIFO Buffer Label Data Label information of the received message can be read.
15 to 3	Reserved	These bits are read as the value after reset.
2	RFFDF	FDF 0: Classical CAN frame 1: CAN FD frame
1	RFBRS	BRS 0: The bit rate in the data area does not change. 1: The bit rate in the data area changes.
0	RFESI	ESI 0: Error active node 1: Error passive node

RFPTR[15:0] Bits

These bits contain the label information of the message stored in the receive FIFO buffer.

RFFDF Bit

This bit indicates the FD format (classical CAN frame or CAN FD frame) of the message stored in the receive FIFO buffer.

RFBRS Bit

When the RFFDF bit is set to 1, this bit indicates the BRS bit value of the message stored in the receive FIFO buffer.
When the RFFDF bit is set to 0, this bit is always read as 0.

RFESI Bit

When the RFFDF bit is set to 1, this bit indicates the ESI bit value of the message stored in the receive FIFO buffer.
When the RFFDF bit is set to 0, this bit is always read as 0.

24.3.6.7 RCFDCnCFDRFDFd_x — Receive FIFO Buffer Access Data Field Register (d = 0 to 15, x = 0 to 7)

Access: RCFDCnCFDRFDFd_x register is a read-only register that can be read in 32-bit units

RCFDCnCFDRFDFd_xL, RCFDCnCFDRFDFd_xH registers are read-only registers that can be read in 16-bit units

RCFDCnCFDRFDFd_xLL, RCFDCnCFDRFDFd_xLH, RCFDCnCFDRFDFd_xHL, RCFDCnCFDRFDFd_xHH registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDRFDFd_x: <RCFDCn_base> + $600C_H$ + (04_H × d) + (80_H × x)

RCFDCnCFDRFDFd_xL: <RCFDCn_base> + $600C_H$ + (04_H × d) + (80_H × x),

RCFDCnCFDRFDFd_xH: <RCFDCn_base> + $600E_H$ + (04_H × d) + (80_H × x)

RCFDCnCFDRFDFd_xLL: <RCFDCn_base> + $600C_H$ + (04_H × d) + (80_H × x),

RCFDCnCFDRFDFd_xLH: <RCFDCn_base> + $600D_H$ + (04_H × d) + (80_H × x),

RCFDCnCFDRFDFd_xHL: <RCFDCn_base> + $600E_H$ + (04_H × d) + (80_H × x),

RCFDCnCFDRFDFd_xHH: <RCFDCn_base> + $600F_H$ + (04_H × d) + (80_H × x)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RFDB4 × d + 3 [7:0]								RFDB4 × d + 2 [7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RFDB4 × d + 1 [7:0]								RFDB4 × d + 0 [7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 24.72 RCFDCnCFDRFDFd_x Register Contents

Bit Position	Bit Name	Function
31 to 24	RFDB4 × d + 3 [7:0]	Receive Buffer Data Byte 4 × d + 3
23 to 16	RFDB4 × d + 2 [7:0]	Receive Buffer Data Byte 4 × d + 2 Receive Buffer Data Byte 4 × d + 1 Receive Buffer Data Byte 4 × d + 0
15 to 8	RFDB4 × d + 1 [7:0]	Data for a message stored in the receive buffer can be read.
7 to 0	RFDB4 × d + 0 [7:0]	

When the RFDLC[3:0] value in the RCFDCnCFDRFPTRx register is smaller than the payload storage size of the receive FIFO buffer, data bytes for which no data is set are read as 00_H.

Specify the payload storage size of the receive FIFO buffer by the RFPLS[2:0] bits in the RCFDCnCFDRFCCx register. Do not read or write the RCFDCnCFDRFDFd_x register corresponding to an area that exceeds the specified size.

24.3.7 Transmit/Receive FIFO Buffer-related Registers

24.3.7.1 RCFDCnCFDCFCCk — Transmit/receive FIFO Buffer Configuration and Control Register (k = 0 to 23)

Access: RCFDCnCFDCFCCk register can be read or written in 32-bit units

RCFDCnCFDCFCCkL, RCFDCnCFDCFCCkH registers can be read or written in 16-bit units

RCFDCnCFDCFCCkLL, RCFDCnCFDCFCCkLH, RCFDCnCFDCFCCkHL, RCFDCnCFDCFCCkHH registers can be read or written in 8-bit units

Address: RCFDCnCFDCFCCk: <RCFDCn_base> + 0118_H + (04_H × k)

RCFDCnCFDCFCCkL: <RCFDCn_base> + 0118_H + (04_H × k),

RCFDCnCFDCFCCkH: <RCFDCn_base> + $011A_H$ + (04_H × k)

RCFDCnCFDCFCCkLL: <RCFDCn_base> + 0118_H + (04_H × k),

RCFDCnCFDCFCCkLH: <RCFDCn_base> + 0119_H + (04_H × k),

RCFDCnCFDCFCCkHL: <RCFDCn_base> + $011A_H$ + (04_H × k),

RCFDCnCFDCFCCkHH: <RCFDCn_base> + $011B_H$ + (04_H × k)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CFITT[7:0]								CFDC[2:0]			CFTML[4:0]				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CFIGCV[2:0]			CFIM	CFITR	CFITSS	CFM[1:0]		—	CFPLS[2:0]			—	CFTXIE	CFRXIE	CFE
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Table 24.73 RCFDCnCFDCFCCk Register Contents

Bit Position	Bit Name	Function
31 to 24	CFITT[7:0]	Set a message transmission interval. Set Value: 00_H to FF_H
23 to 21	CFDC[2:0]	Transmit/Receive FIFO Buffer Depth Configuration B23 b22 b21 0 0 0: 0 messages 0 0 1: 4 messages 0 1 0: 8 messages 0 1 1: 16 messages 1 0 0: 32 messages 1 0 1: 48 messages 1 1 0: 64 messages 1 1 1: 128 messages
20 to 16	CFTML[4:0]	Transmit Buffer Link Configuration Set the transmit buffer number to be linked to the transmit/receive FIFO buffer.

Table 24.73 RCFDCnCFDCFCCk Register Contents

Bit Position	Bit Name	Function
15 to 13	CFIGCV[2:0]	Transmit/Receive FIFO Receive Interrupt Request Timing Select b15 b14 b13 0 0 0: When FIFO is 1/8 full. 0 0 1: When FIFO is 2/8 full. 0 1 0: When FIFO is 3/8 full. 0 1 1: When FIFO is 4/8 full. 1 0 0: When FIFO is 5/8 full. 1 0 1: When FIFO is 6/8 full. 1 1 0: When FIFO is 7/8 full. 1 1 1: When FIFO is full.
12	CFIM	Transmit/Receive FIFO Interrupt Source Select 0: • Receive mode/gateway mode When the number of received messages meets the condition set by the CFIGCV[2:0] bits, a FIFO receive interrupt request is generated. • Transmit mode/gateway mode When the buffer becomes empty upon completion of message transmission, a FIFO transmit interrupt request is generated. 1: • Receive mode/gateway mode A FIFO receive interrupt request is generated each time a message has been received. • Transmit mode/gateway mode A FIFO transmit interrupt request is generated each time a message has been transmitted.
11	CFITR	Transmit/Receive FIFO Interval Timer Resolution 0: Clock obtained by dividing pclk/2 by the value of the ITRCP [15:0] bits 1: Clock obtained by dividing pclk/2 by “value of ITRCP [15:0] bits x 10”
10	CFITSS	Transmit/Receive FIFO Interval Timer Clock Source Select 0: Interval timer clock source selected by the CFITR bit 1: Interval timer clock source is the nominal bit time clock for the channel to which the FIFO is linked.
9, 8	CFM[1:0]	Transmit/Receive FIFO Mode Select b9 b8 0 0: Receive mode 0 1: Transmit mode 1 0: Gateway mode 1 1: Setting prohibited
7	Reserved	These bits are read as the value after reset. The write value should be the value after reset.
6 to 4	CFPLS[2:0]	Transmit/Receive FIFO Buffer Payload Storage Size Select b6 b5 b4 0 0 0: 8 bytes 0 0 1: 12 bytes 0 1 0: 16 bytes 0 1 1: 20 bytes 1 0 0: 24 bytes 1 0 1: 32 bytes 1 1 0: 48 bytes 1 1 1: 64 bytes
3	Reserved	These bits are read as the value after reset. The write value should be the value after reset.
2	CFTXIE	Transmit/Receive FIFO Transmit Interrupt Enable 0: Transmit/receive FIFO transmit interrupt is disabled. 1: Transmit/receive FIFO transmit interrupt is enabled.

Table 24.73 RCFDCnCFDCFCCk Register Contents

Bit Position	Bit Name	Function
1	CFRXIE	Transmit/Receive FIFO Receive Interrupt Enable 0: Transmit/receive FIFO receive interrupt is disabled. 1: Transmit/receive FIFO receive interrupt is enabled.
0	CFE	Transmit/Receive FIFO Buffer Enable 0: No transmit/receive FIFO buffer is used. 1: Transmit/receive FIFO buffers are used.

CFITT[7:0] Bits

These bits are used to set a message transmission interval when transmitting messages continuously from a transmit/receive FIFO buffer whose CFM[1:0] bits are set to 01_B (transmit mode) or 10_B (gateway mode).

Clear the CFE bit to 0 (no transmit/receive FIFO buffer is used) before modifying the CFITT[7:0] bits.

CFDC[2:0] Bits

These bits are used to set the number of messages that can be stored in a single transmit/receive FIFO buffer. When these bits are set to 000_B, do not use a transmit/receive FIFO buffer. Modify these bits only in global reset mode.

CFTML[4:0] Bits

These bits are used to set the number of transmit buffer on the channel which will be linked to transmit/ receive FIFO buffer k when the CFM[1:0] bits are set to 01_B (transmit mode) or 10_B (gateway mode). There are three transmit/receive FIFO buffers per channel, so channel number m of FIFO buffer k is calculated as m = k/3 (integer division). The actual assigned transmit buffer number p linked to FIFO buffer k will be ((32 × m) + CFTML[4:0]) (See **Table 24.32, Transmit Buffer p Linked to the Transmit/Receive FIFO Buffer by the Setting of Bits CFTML[4:0]**).

See **Table 24.30, Transmit Buffer p Allocated to Each Channel** and **Table 24.31, Transmit/Receive FIFO Buffer k Allocated to Each Channel**, as for the relationship between transmit/receive FIFO buffer k and transmit buffer p.

Setting the CFDC[2:0] bits to 001_B or more enables the setting of the CFTML[4:0] bits.

Do not link to any transmit buffer which is already allocated to a transmit queue on the same channel or to another transmit/receive FIFO buffer. Modify these bits only in global reset mode.

CFIGCV[2:0] Bits

These bits are used to specify the number of received messages required to generate a transmit/receive FIFO receive interrupt request when the CFM[1:0] bits are set to 00_B (receive mode) or 10_B (gateway mode) and the CFIM bit is set to 0 with a fraction for the total number of buffers (the setting of CFDC[2:0]).

When the CFDC[2:0] bits are set to 001_B (4 messages), set the CFIGCV[2:0] bits to 001_B, 011_B, 101_B, or 111_B.

Modify these bits only in global reset mode.

CFIM Bit

This bit is used to select a transmit/receive FIFO interrupt source. Modify this bit only in global reset mode.

CFITR Bit

This bit is enabled when the CFITSS bit is 0.

When this bit is 0, the interval timer clock source is the pclk/2 clock divided by the value of the ITRCP[15:0] bits in the RCFDCnCFDGCFG register.

When this bit is 1, the interval timer clock source is the pclk/2 clock divided by (the value of the ITRCP[15:0] bits in the RCFDCnCFDGCFG register × 10).

Modify this bit while the CFE bit is set to 0 (no transmit/receive FIFO buffer is used).

CFITSS Bit

When this bit is 0, the clock selected by the CFITR bit is the count source of the interval timer. When this bit is 1, the nominal bit time clock of the channel to which the FIFO is linked is the count source of the interval timer. Use this count source only for the channel which does not handle the CAN FD frames.

Modify this bit while the CFE bit is set to 0 (no transmit/receive FIFO buffer is used).

CFM[1:0] Bits

These bits are used to select transmit/receive FIFO mode. Modify these bits only in global reset mode.

CFPLS[2:0] Bits

These bits are used to select the maximum payload size that can be stored in the transmit/receive FIFO buffer. Modify these bits only in global reset mode.

CFTXIE Bit

When this bit is set to 1 and the CFTXIF flag in the RCFDCnCFDCFSTSk register is set to 1, a transmit/receive FIFO transmit interrupt request is generated.

Modify this bit with the CFE bit set to 0 (no transmit/receive FIFO buffer is used).

CFRXIE Bit

When this bit is set to 1 and the CFRXIF flag in the RCFDCnCFDCFSTSk register is set to 1, a transmit/receive FIFO receive interrupt request is generated.

Modify this bit with the CFE bit set to 0.

CFE Bit

Setting this bit to 1 enables the transmit/receive FIFO buffers.

When this bit is set to 0 in transmit mode or gateway mode, if a message in the transmit/receive FIFO buffer is being transmitted or will be transmitted next, the transmit/receive FIFO buffer becomes empty after completion of transmission of that message, or upon detection of a CAN bus error, or arbitration- lost. In other cases or in receive mode, the transmit/receive FIFO buffer becomes empty immediately.

This bit is cleared to 0 when the following conditions are met.

- Receive mode: Global reset mode
- Transmit mode or gateway mode: Channel reset mode

Modify this bit in the following mode.

- Receive mode: Global operating mode or global test mode
- Transmit mode or gateway mode: Channel communication mode or channel halt mode

After all other bits in the RCFDCnCFDCFCCk register have been set, set this bit to 1 by using another instruction.

24.3.7.2 RCFDCnCFDCFSTSk — Transmit/receive FIFO Buffer Status Register (k = 0 to 23)

Access: RCFDCnCFDCFSTSk register can be read or written in 32-bit units

RCFDCnCFDCFSTSkL register can be read or written in 16-bit units

RCFDCnCFDCFSTSkLL register can be read or written in 8-bit units

RCFDCnCFDCFSTSkLH register is a read-only register that can be read in 8-bit units

Address: RCFDCnCFDCFSTSk: <RCFDCn_base> + 0178_H + (04_H × k)

RCFDCnCFDCFSTSkL: <RCFDCn_base> + 0178_H + (04_H × k)

RCFDCnCFDCFSTSkLL: <RCFDCn_base> + 0178_H + (04_H × k),

RCFDCnCFDCFSTSkLH: <RCFDCn_base> + 0179_H + (04_H × k)

Value after reset: $0000\ 0001_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CFMC[7:0]								—	—	—	CFTXIF	CFRXIF	CFMLT	CFFLL	CFEMP
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R/W*1	R/W*1	R/W*1	R	R

Note 1. The only effective value for writing to this flag bit is 0, which clears the bit. Otherwise writing to the bit results in retention of its state.

Table 24.74 RCFDCnCFDCFSTSk Register Contents

Bit Position	Bit Name	Function
31 to 16	Reserved	These bits are read as the value after reset. When writing to these bits, write the value after reset.
15 to 8	CFMC[7:0]	Transmit/Receive FIFO Message Counter The number of messages stored in the transmit/receive FIFO buffer.
7 to 5	Reserved	These bits are read as the value after reset. When writing to these bits, write the value after reset.
4	CFTXIF	Transmit/Receive FIFO Transmit Interrupt Request Flag 0: No transmit/receive FIFO transmit interrupt request is present. 1: A transmit/receive FIFO transmit interrupt request is present.
3	CFRXIF	Transmit/Receive FIFO Receive Interrupt Request Flag 0: No transmit/receive FIFO receive interrupt request is present. 1: A transmit/receive FIFO receive interrupt request is present.
2	CFMLT	Transmit/Receive FIFO Message Lost Flag 0: No transmit/receive FIFO message is lost. 1: A transmit/receive FIFO message is lost.
1	CFFLL	Transmit/Receive FIFO Buffer Full Status Flag 0: The transmit/receive FIFO buffer is not full. 1: The transmit/receive FIFO buffer is full.
0	CFEMP	Transmit/Receive FIFO Buffer Empty Status Flag 0: The transmit/receive FIFO buffer contains messages. 1: The transmit/receive FIFO buffer contains no message (buffer empty).

CFMC[7:0] Bits

The CFMC[7:0] bits indicate the following values according to the setting of the CFM[1:0] bits in the RCFDCnCFDCFCCk register.

- When CFM[1:0] value is 01_B (transmit mode): Number of untransmitted messages in the buffer
- When CFM[1:0] value is 00_B (receive mode): Number of unread received messages in the buffer
- When CFM[1:0] value is 10_B (gateway mode): Number of untransmitted received messages in the buffer

These bits are cleared to 0 when any of the following conditions is met.

- When CFM[1:0] value is 00_B: In global reset mode
- When CFM[1:0] value is 01_B or 10_B: In channel reset mode
- When the CFE bit in the RCFDCnCFDCFCCk register is cleared to 0.

CFTXIF Flag

The CFTXIF flag is set to 1 when any of the following conditions is met.

- When the CFM[1:0] bits are set to 01_B or 10_B, and the interrupt source selected by the CFIM bit in the RCFDCnCFDCFCCk register occurs

The CFTXIF flag is cleared to 0 when any of the following conditions is met.

- When 0 is written to the CFTXIF flag
- When the CFM[1:0] bits are set to 00_B: In global reset mode
- When the CFM[1:0] bits are set to 01_B or 10_B: In channel reset mode

Write 0 to this flag in global operating mode or global test mode.

To clear the flags of the register to 0, the program must write 0 to the corresponding flag to be cleared. When writing 0, using store instruction, set the bit to be set to “0” to “0”, and the bits not to be set to “0” to “1”.

CFRXIF Flag

The CFRXIF flag is set to 1 when any of the following conditions is met.

- When the CFM[1:0] bits are set to 00_B or 10_B, and the factor selected by the CFIM bit in the RCFDCnCFDCFCCk register occurs

The CFRXIF flag is cleared to 0 when any of the following conditions is met.

- When 0 is written to the CFRXIF flag
- When the CFM[1:0] bits are set to 00_B: In global reset mode
- When the CFM[1:0] bits are set to 01_B or 10_B: In channel reset mode

Write 0 to this flag in global operating mode or global test mode.

To clear the flags of the register to 0, the program must write 0 to the corresponding flag to be cleared. When writing 0, using store instruction, set the bit to be set to “0” to “0”, and the bits not to be set to “0” to “1”.

CFMLT Flag

The CFMLT flag is set to 1 when any of the following conditions is met.

- When an attempt is made to store a new message while the transmit/receive FIFO buffer is full. In this case, the new message is discarded.

The CFMLT flag is cleared to 0 when any of the following conditions is met.

- When 0 is written to the CFMLT flag
- When the CFM[1:0] bits are set to 00_B: In global reset mode
- When the CFM[1:0] bits are set to 01_B or 10_B: In channel reset mode

Write 0 to this flag in global operating mode or global test mode

To clear the flags of the register to 0, the program must write 0 to the corresponding flag to be cleared. When writing 0, using store instruction, set the bit to be set to “0” to “0”, and the bits not to be set to “0” to “1”.

CFFLL Flag

The CFFLL flag is set to 1 when any of the following conditions is met.

- When the number of messages stored in the transmit/receive FIFO buffer matches the FIFO buffer depth set by the CFDC[2:0] bits in the RCFDCnCFDCFCCk register.

The CFFLL flag is cleared to 0 when any of the following conditions is met.

- When the number of messages stored in the transmit/receive FIFO buffer becomes smaller than the FIFO buffer depth set by the CFDC[2:0] bits.
- When the CFE bit in the RCFDCnCFDCFCCk register is 0 (no transmit/receive FIFO buffer is used): When not in the transmit abort
- When the CFM[1:0] bits are set to 00_B: In global reset mode
- When the CFM[1:0] bits are set to 01_B or 10_B: In channel reset mode

CFEMP Flag

The CFEMP flag is set to 1 when any of the following conditions is met.

- When the CFM[1:0] bits are set to 00_B: All messages have been read, or in global reset mode
- When the CFM[1:0] bits are set to 01_B or 10_B: All messages have been transmitted, or in channel reset mode
- When the CFE bit is 0 (no transmit/receive FIFO buffer is used): Not in the transmit abort

The CFEMP flag is cleared to 0 when any of the following conditions is met.

- When the CFM[1:0] bits are set to 00_B or 10_B: At least one received message has been stored in the transmit/receive FIFO buffer.
- When the CFM[1:0] bits are set to 01_B: A value of FF_H has been written to the RCFDCnCFDCFPCTRk register after data was written to the RCFDCnCFDCFIDk, RCFDCnCFDCFPTRk, RCFDCnCFDCFFDCSTSk, and RCFDCnCFDCFDFd_k register

NOTE

To clear CFTXIF, CFRXIF, or CFMLT flag to 0, the program must write 0. When writing, use a store instruction to write “0” to the given flag and “1” to other flags.

24.3.7.3 RCFDCnCFDCFPCTRk — Transmit/receive FIFO Buffer Pointer Control Register (k = 0 to 23)

Access: RCFDCnCFDCFPCTRk register is a write-only register that can be written in 32-bit units

RCFDCnCFDCFPCTRkL register is a write-only register that can be written in 16-bit units

RCFDCnCFDCFPCTRkLL register is a write-only register that can be written in 8-bit units

Address: RCFDCnCFDCFPCTRk: <RCFDCn_base> + $01D8_H$ + (04_H × k)

RCFDCnCFDCFPCTRkL: <RCFDCn_base> + $01D8_H$ + (04_H × k)

RCFDCnCFDCFPCTRkLL: <RCFDCn_base> + $01D8_H$ + (04_H × k)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CFPC[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	W	W	W	W	W	W	W	W

Table 24.75 RCFDCnCFDCFPCTRk Register Contents

Bit Position	Bit Name	Function
31 to 8	Reserved	The write value should be the value after reset.
7 to 0	CFPC[7:0]	Transmit/Receive FIFO Pointer Control • Receive mode: Writing FF_H to these bits moves the read pointer to the next unread message in the transmit/receive FIFO buffer. • Transmit mode: Writing FF_H to these bits moves the write pointer to the next stage of the transmit/receive FIFO buffer. • Gateway mode: Setting prohibited

When the corresponding transmit/receive FIFO buffer is the first transmit/receive FIFO buffer (k = 3 × m) allocated to channel m and when the CFDMAEm bit in the RCFDCnCFDCDTCT register is 1 (DMA transfer request enabled), do not write a value to this register.

CFPC[7:0] Bits

- Receive mode (CFM[1:0] value in the RCFDCnCFDCFCCk register is 00_B):

  Writing FF_H to the CFPC[7:0] bits moves the read pointer to the next unread message in the transmit/receive FIFO buffer. At this time, the CFMC[7:0] value (transmit/receive FIFO message counter) in the RCFDCnCFDCFSTSk register is decremented by 1. Read the RCFDCnCFDCFIDk, RCFDCnCFDCFPTRk, RCFDCnCFDCFFDCSTSk, and RCFDCnCFDCFDFd_k registers to read messages from the transmit/receive FIFO buffer, and then write FF_H to the CFPC[7:0] bits.

  When writing FF_H to these bits, make sure that the CFE bit in the RCFDCnCFDCFCCk register is set to 1 (transmit/receive FIFO buffers are used) and the CFEMP flag in the RCFDCnCFDCFSTSk register is 0 (the transmit/receive FIFO buffer contains messages).

- Transmit mode (CFM[1:0] value in the RCFDCnCFDCFCCk register is 01_B):

  Writing FF_H to the CFPC[7:0] bits stores the data written to the RCFDCnCFDCFIDk, RCFDCnCFDCFPTRk, RCFDCnCFDCFFDCSTSk, and RCFDCnCFDCFDFd_k registers in the transmit/receive FIFO buffer and moves the write pointer to the next stage of the transmit/receive FIFO buffer. At this time, the CFMC[7:0] value is incremented by 1. Write transmit messages to the RCFDCnCFDCFIDk, RCFDCnCFDCFPTRk, RCFDCnCFDCFFDCSTSk, and RCFDCnCFDCFDFd_k registers before writing FF_H to the CFPC[7:0] bits.

  When writing FF_H to these bits, make sure that the CFE bit in the RCFDCnCFDCFCCk register is set to 1 and the CFFLL flag in the RCFDCnCFDCFSTSk register is 0 (the transmit/receive FIFO buffer is not full).

- Gateway mode (CFM[1:0] value in the RCFDCnCFDCFCCk register is 10_B): Setting prohibited

24.3.7.4 RCFDCnCFDCFIDk — Transmit/receive FIFO Buffer Access ID Register (k = 0 to 23)

Access: RCFDCnCFDCFIDk register can be read or written in 32-bit units

RCFDCnCFDCFIDkL, RCFDCnCFDCFIDkH registers can be read or written in 16-bit units

RCFDCnCFDCFIDkLL, RCFDCnCFDCFIDkLH, RCFDCnCFDCFIDkHL, RCFDCnCFDCFIDkHH registers can be read or written in 8-bit units

Address: RCFDCnCFDCFIDk: <RCFDCn_base> + 6400_H + (80_H × k)

RCFDCnCFDCFIDkL: <RCFDCn_base> + 6400_H + (80_H × k),

RCFDCnCFDCFIDkH: <RCFDCn_base> + 6402_H + (80_H × k)

RCFDCnCFDCFIDkLL: <RCFDCn_base> + 6400_H + (80_H × k),

RCFDCnCFDCFIDkLH: <RCFDCn_base> + 6401_H + (80_H × k),

RCFDCnCFDCFIDkHL: <RCFDCn_base> + 6402_H + (80_H × k),

RCFDCnCFDCFIDkHH: <RCFDCn_base> + 6403_H + (80_H × k)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CFIDE	CFRTR	THLEN	CFID[28:16]												
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CFID[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 24.76 RCFDCnCFDCFIDk Register Contents

Bit Position	Bit Name	Function
31	CFIDE	Transmit/Receive FIFO Buffer IDE 0: Standard ID 1: Extended ID
30	CFRTR	Transmit/Receive FIFO Buffer RTR/RRS • When the CFM[1:0] value is 01_B (transmit mode) – When the transmit message is a classical CAN frame 0: Data frame 1: Remote frame – When the transmit message is a CAN FD frame Write 0 to this bit. • When the CFM[1:0] value is 00_B (receive mode) – When the received message is a classical CAN frame 0: Data frame 1: Remote frame – When the received message is a CAN FD frame The RRS bit value of the received message can be read.
29	THLEN	Transmit History Data Store Enable This bit is valid only when the CFM[1:0] value is 01_B (transmit mode). 0: Transmit history data is not stored in the buffer. 1: Transmit history data is stored in the buffer.

Table 24.76 RCFDCnCFDCFIDk Register Contents

Bit Position	Bit Name	Function
28 to 0	CFID[28:0]	Transmit/Receive FIFO Buffer ID Data • When CFM[1:0] value is 01_B (transmit mode): Set standard ID or extended ID. For standard ID, write an ID to bits 10 to 0 and write 0 to bits 28 to 11. • When CFM[1:0] value is 00_B (receive mode): Standard ID or extended ID in the received message can be read. For standard ID, read bits 10 to 0. Bits 28 to 11 are read as 0.

This register can be read or written when the CFM[1:0] value in the RCFDCnCFDCFCCk register is 01_B (transmit mode). This register can be read when the CFM[1:0] value is 00_B (receive mode). This RCFDCnCFDCFIDk register should not be read or written when the CFM[1:0] value is 10_B (gateway mode).

CFIDE Bit

This bit indicates the ID format (standard ID or extended ID) of the received message stored in the transmit/receive FIFO buffer when the CFM[1:0] value is 00_B. When the CFM[1:0] value is 01_B, this bit is used to set the ID format of the message to be transmitted from the transmit/receive FIFO buffer.

CFRTR Bit

If the received message is a classical CAN frame, this bit indicates the data format (data frame or remote frame) of the received message stored in the transmit/receive FIFO buffer when the CFM[1:0] value is 00_B. If the received message is a CAN FD frame, this bit indicates the RRS bit value of the received message.

When the CFM[1:0] value is 01_B, this bit is used to set the data format of the message to be transmitted from the transmit/receive FIFO buffer.

When the CFFDF bit in the RCFDCnCFDCFFDCSTSk register is 1 (CAN FD frame), set this bit to 0.

THLEN Bit

When this bit is set to 1, the transmit history data (label information, buffer number, buffer type, and timestamp) of transmit messages is stored in the transmit history buffer after transmission is completed.

This bit is enabled when the CFM[1:0] value is 01_B (transmit mode).

CFID[28:0] Bits

These bits contain the ID of the received message stored in the transmit/receive FIFO buffer when the CFM[1:0] value is 00_B.

When the CFM[1:0] value is 01_B, these bits are used to set the ID of the message to be transmitted from the transmit/receive FIFO buffer.

24.3.7.5 RCFDCnCFDCFPTRk — Transmit/receive FIFO Buffer Access Pointer Register (k = 0 to 23)

Access: RCFDCnCFDCFPTRk register can be read or written in 32-bit units

RCFDCnCFDCFPTRkL, RCFDCnCFDCFPTRkH registers can be read or written in 16-bit units

RCFDCnCFDCFPTRkLL, RCFDCnCFDCFPTRkLH, RCFDCnCFDCFPTRkHH registers can be read or written in 8-bit units

Address: RCFDCnCFDCFPTRk: <RCFDCn_base> + 6404_H + (80_H × k)

RCFDCnCFDCFPTRkL: <RCFDCn_base> + 6404_H + (80_H × k),

RCFDCnCFDCFPTRkH: <RCFDCn_base> + 6406_H + (80_H × k)

RCFDCnCFDCFPTRkLL: <RCFDCn_base> + 6404_H + (80_H × k),

RCFDCnCFDCFPTRkLH: <RCFDCn_base> + 6405_H + (80_H × k),

RCFDCnCFDCFPTRkHH: <RCFDCn_base> + 6407_H + (80_H × k)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CFDLC[3:0]				—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CFTS[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 24.77 RCFDCnCFDCFPTRk Register Contents

Bit Position	Bit Name	Function
31 to 28	CFDLC[3:0]	Transmit/Receive FIFO Buffer DLC Data

b31	b30	b29	b28	Classical CAN Frame	CAN FD Frame
0	0	0	0	0 data bytes	
0	0	0	1	1 data byte	
0	0	1	0	2 data bytes	
0	0	1	1	3 data bytes	
0	1	0	0	4 data bytes	
0	1	0	1	5 data bytes	
0	1	1	0	6 data bytes	
0	1	1	1	7 data bytes	
1	0	0	0	8 data bytes	
1	0	0	1	8 data bytes	12 data bytes
1	0	1	0		16 data bytes
1	0	1	1		20 data bytes
1	1	0	0		24 data bytes
1	1	0	1		32 data bytes
1	1	1	0		48 data bytes
1	1	1	1		64 data bytes

27 to 16	Reserved	These bits are read as the value after reset. The write value should be the value after reset.
15 to 0	CFTS[15:0]	Transmit/Receive FIFO Buffer Timestamp Data These bits are valid only when the CFM[1:0] value is 00_B (receive mode). The timestamp value of the received message can be read.

This register can be read or written when the CFM[1:0] value in the RCFDCnCFDCFCCk register is 01_B (transmit mode). This register can be read when the CFM[1:0] value is 00_B (receive mode). This register should not be read or written when the CFM[1:0] value is 10_B (gateway mode).

CFDLC[3:0] Bits

These bits indicate the data length of the received message stored in the transmit/receive FIFO buffer when the CFM[1:0] value is 00_B.

When the CFM[1:0] value is 01_B, these bits are used to set the data length of the message to be transmitted from the transmit/receive FIFO buffer.

When the CFDLC[3:0] bits are set to 1001_B or more while the CFFDF bit in the RCFDCnCFDCFFDCSTSk register is 0 (classical CAN frame), 8-byte data is transmitted actually.

A value of 0000_B to 1111_B is settable. If the specified data length exceeds the payload storage size specified by the CFPLS[2:0] bits, excessive payloads are padded by CC_H.

CFTS[15:0] Bits

These bits indicate the timestamp value of the message stored in the transmit/receive FIFO buffer. These bits are valid when the CFM[1:0] value is 00_B.

24.3.7.6 RCFDCnCFDCFFDCSTSk — Transmit/receive FIFO CAN FD Configuration/status Register (k = 0 to 23)

Access: RCFDCnCFDCFFDCSTSk register can be read or written in 32-bit units

RCFDCnCFDCFFDCSTSkL register can be read or written in 16-bit units

RCFDCnCFDCFFDCSTSkH register is a read-only register that can be read in 16-bit units

RCFDCnCFDCFFDCSTSkLL register can be read or written in 8-bit units

RCFDCnCFDCFFDCSTSkHL, RCFDCnCFDCFFDCSTSkHH registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDCFFDCSTSk: <RCFDCn_base> + 6408_H + (80_H × k)

RCFDCnCFDCFFDCSTSkL: <RCFDCn_base> + 6408_H + (80_H × k),

RCFDCnCFDCFFDCSTSkH: <RCFDCn_base> + $640A_H$ + (80_H × k)

RCFDCnCFDCFFDCSTSkLL: <RCFDCn_base> + 6408_H + (80_H × k),

RCFDCnCFDCFFDCSTSkHL: <RCFDCn_base> + $640A_H$ + (80_H × k),

RCFDCnCFDCFFDCSTSkHH: <RCFDCn_base> + $640B_H$ + (80_H × k)

Value after reset: 0000 0000_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CFPTR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	CFFDF	CFBRS	CFESI
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Table 24.78 RCFDCnCFDCFFDCSTSk Register Contents

Bit Position	Bit Name	Function
31 to 16	CFPTR[15:0]	Transmit/Receive FIFO Buffer Label Data • When CFM[1:0] value is 01_B (transmit mode): Set the label information to be stored in the transmit history buffer. Only bits CFPTR[15:0] are valid. • When CFM[1:0] value is 00_B (receive mode): The label information of the received message can be read.
15 to 3	Reserved	These bits are read as the value after reset. The write value should be the value after reset.
2	CFFDF	FDF 0: Classical CAN frame 1: CAN FD frame
1	CFBRS	BRS 0: The bit rate in the data area does not change. 1: The bit rate in the data area changes.
0	CFESI	ESI 0: Error active node 1: Error passive node

This register can be read or written when the CFM[1:0] value in the RCFDCnCFDCFCCk register is 01_B (transmit mode). This register can be read when the CFM[1:0] value is 00_B (receive mode). Do not read or write this register when the CFM[1:0] value is 10_B (gateway mode).

CFPTR[15:0] Bits

These bits indicate the label information attached to the received message stored in the transmit/receive FIFO buffer when the CFM[1:0] value is 00_B. When the CFM[1:0] value is 01_B, the CFPTR[15:0] value is stored in the transmit history buffer when message transmission has been completed.

CFFDF Bit

When the CFM[1:0] value is 00_B, this bit indicates the FD format (classical CAN frame or CAN FD frame) of the message stored in the transmit/receive FIFO buffer. When the CFM[1:0] value is 01_B, this bit is used to set the FD format of the message to be transmitted from the transmit/receive FIFO buffer.

CFBRS Bit

When the CFM[1:0] value is 00_B, if the CFFDF bit is set to 1, this bit indicates the BRS bit value of the message stored in the transmit/receive FIFO buffer. If the CFFDF bit is set to 0, this bit is always read as 0.

When the CFM[1:0] value is 01_B, if the CFFDF bit is set to 1, this bit is used to set the BRS bit value of the message to be transmitted from the transmit/receive FIFO buffer. If the CFFDF bit is set to 0, write 0 to this bit.

CFESI Bit

When the CFM[1:0] value is 00_B, if the CFFDF bit is set to 1, this bit indicates the ESI bit value of the message stored in the transmit/receive FIFO buffer. If the CFFDF bit is set to 0, this bit is always read as 0.

When the CFM[1:0] value is 01_B, if the CFFDF bit is set to 1, this bit is used to set the ESI bit value of the message to be transmitted from the transmit/receive FIFO buffer. The set value is transmitted when the ESIC bit in the RCFDCnCFDCmFDCFG register is set to 1 and the channel is in the error active state. When the channel is in the error passive state, the ESI bit value that shows an error passive node is transmitted regardless of this bit value. When the CFFDF bit is set to 0, write 0 to this bit.

24.3.7.7 RCFDCnCFDCFDFd_k — Transmit/receive FIFO Buffer Access Data Field Register (d = 0 to 15, k = 0 to 23)

Access: RCFDCnCFDCFDFd_k register can be read or written in 32-bit units

RCFDCnCFDCFDFd_kL, RCFDCnCFDCFDFd_kH registers can be read or written in 16-bit units

RCFDCnCFDCFDFd_kLL, RCFDCnCFDCFDFd_kLH, RCFDCnCFDCFDFd_kHL, RCFDCnCFDCFDFd_kHH registers can be read or written in 8-bit units

Address: RCFDCnCFDCFDFd_k: <RCFDCn_base> + $640C_H$ + (04_H × d) + (80_H × k)

RCFDCnCFDCFDFd_kL: <RCFDCn_base> + $640C_H$ + (04_H × d) + (80_H × k),

RCFDCnCFDCFDFd_kH: <RCFDCn_base> + $640E_H$ + (04_H × d) + (80_H × k)

RCFDCnCFDCFDFd_kLL: <RCFDCn_base> + $640C_H$ + (04_H × d) + (80_H × k),

RCFDCnCFDCFDFd_kLH: <RCFDCn_base> + $640D_H$ + (04_H × d) + (80_H × k),

RCFDCnCFDCFDFd_kHL: <RCFDCn_base> + $640E_H$ + (04_H × d) + (80_H × k),

RCFDCnCFDCFDFd_kHH: <RCFDCn_base> + $640F_H$ + (04_H × d) + (80_H × k)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CFDB4 × d + 3 [7:0]								CFDB4 × d + 2 [7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CFDB4 × d + 1 [7:0]								CFDB4 × d + 0 [7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 24.79 RCFDCnCFDCFDFd_k Register Contents

Bit Position	Bit Name	Function
31 to 24	CFDB4 × d + 3 [7:0]	Transmit/Receive FIFO Buffer Data Byte 4 × d + 3
23 to 16	CFDB4 × d + 2 [7:0]	Transmit/Receive FIFO Buffer Data Byte 4 × d + 2
15 to 8	CFDB4 × d + 1 [7:0]	Transmit/Receive FIFO Buffer Data Byte 4 × d + 1
7 to 0	CFDB4 × d + 0 [7:0]	Transmit/Receive FIFO Buffer Data Byte 4 × d + 0 • When CFM[1:0] value is 01_B (transmit mode): Set the transmit/receive FIFO buffer data. • When CFM[1:0] value is 00_B (receive mode): The message data stored in the transmit/receive FIFO buffer can be read.

This register can be read or written when the CFM[1:0] value in the RCFDCnCFDCFCCk register is 01_B (transmit mode).

This register can be read when the CFM[1:0] value is 00_B (receive mode). When the CFDLC[3:0] value in the RCFDCnCFDCFPTRk register is smaller than the payload storage size of the transmit/receive FIFO buffer, data bytes for which no data is set are read as 00_H.

Specify the payload storage size of the transmit/receive FIFO buffer by the CFPLS[2:0] bits in the RCFDCnCFDCFCCk register. Do not read or write the RCFDCnCFDCFDFd_k register corresponding to an area that exceeds the specified size.

This register should not be read or written when the CFM[1:0] value is 10_B (gateway mode).

24.3.8 Details of FIFO Status-related Registers

24.3.8.1 RCFDCnCFDFESTS — FIFO Empty Status Register

Access: RCFDCnCFDFESTS register is a read-only register that can be read in 32-bit units

RCFDCnCFDFESTSL, RCFDCnCFDFESTSH registers are read-only registers that can be read in 16-bit units

RCFDCnCFDFESTSLL, RCFDCnCFDFESTSLH, RCFDCnCFDFESTSHL, RCFDCnCFDFESTSHH registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDFESTS: <RCFDCn_base> + 0238_H

RCFDCnCFDFESTSL: <RCFDCn_base> + 0238_H,

RCFDCnCFDFESTSH: <RCFDCn_base> + $023A_H$

RCFDCnCFDFESTSLL: <RCFDCn_base> + 0238_H,

RCFDCnCFDFESTSLH: <RCFDCn_base> + 0239_H,

RCFDCnCFDFESTSHL: <RCFDCn_base> + $023A_H$,

RCFDCnCFDFESTSHH: <RCFDCn_base> + $023B_H$

Value after reset: FFFF $FFFF_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CF23EMP	CF22EMP	CF21EMP	CF20EMP	CF19EMP	CF18EMP	CF17EMP	CF16EMP	CF15EMP	CF14EMP	CF13EMP	CF12EMP	CF11EMP	CF10EMP	CF9EMP	CF8EMP
Value after reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CF7EMP	CF6EMP	CF5EMP	CF4EMP	CF3EMP	CF2EMP	CF1EMP	CF0EMP	RF7EMP	RF6EMP	RF5EMP	RF4EMP	RF3EMP	RF2EMP	RF1EMP	RF0EMP
Value after reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 24.80 RCFDCnCFDFESTS Register Contents

Bit Position	Bit Name	Function
31	CF23EMP	Transmit/Receive FIFO Buffer Empty Status Flag 0: Transmit/receive FIFO buffer k contains a message. 1: Transmit/receive FIFO buffer k contains no message. (k = 0 to 23)
30	CF22EMP	
29	CF21EMP	
28	CF20EMP	
27	CF19EMP	
26	CF18EMP	
25	CF17EMP	
24	CF16EMP	
23	CF15EMP	
22	CF14EMP	
21	CF13EMP	
20	CF12EMP	
19	CF11EMP	
18	CF10EMP	
17	CF9EMP	
16	CF8EMP	
15	CF7EMP	
14	CF6EMP	

Table 24.80 RCFDCnCFDFESTS Register Contents

Bit Position	Bit Name	Function
13	CF5EMP	Transmit/Receive FIFO Buffer Empty Status Flag 0: Transmit/receive FIFO buffer k contains a message. 1: Transmit/receive FIFO buffer k contains no message. (k = 0 to 23)
12	CF4EMP	
11	CF3EMP	
10	CF2EMP	
9	CF1EMP	
8	CF0EMP	
7	RF7EMP	Receive FIFO Buffer Empty Status Flag 0: Receive FIFO buffer x contains an unread message. 1: Receive FIFO buffer x contains no unread message . (x = 0 to 7)
6	RF6EMP	
5	RF5EMP	
4	RF4EMP	
3	RF3EMP	
2	RF2EMP	
1	RF1EMP	
0	RF0EMP	

The RCFDCnCFDFESTS register is set to FFFF $FFFF_H$ in global reset mode.

CFkEMP Flag (k = 0 to 23)

The CFkEMP flag is set to 1 when the CFEMP flag in the RCFDCnCFDCFSTSk register is set to 1 (the transmit/receive FIFO buffer contains no message (buffer empty)). When the CFEMP flag is cleared to 0 (the transmit/receive FIFO buffer contains messages), the CFkEMP flag is cleared to 0.

RFxEMP Flag (x = 0 to 7)

The RFxEMP flag is set to 1 when the RFEMP flag in the RCFDCnCFDRFSTSx register is set to 1 (the receive FIFO buffer contains no unread message). When the RFEMP flag is cleared to 0 (the receive FIFO buffer contains unread messages), the RFxEMP flag is cleared to 0.

24.3.8.2 RCFDCnCFDFFSTS — FIFO Full Status Register

Access: RCFDCnCFDFFSTS register is a read-only register that can be read in 32-bit units

RCFDCnCFDFFSTSL, RCFDCnCFDFFSTSH registers are read-only registers that can be read in 16-bit units

RCFDCnCFDFFSTSLL, RCFDCnCFDFFSTSLH, RCFDCnCFDFFSTSHL, RCFDCnCFDFFSTSHH registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDFFSTS: <RCFDCn_base> + $023C_H$

RCFDCnCFDFFSTSL: <RCFDCn_base> + $023C_H$,

RCFDCnCFDFFSTSH: <RCFDCn_base> + $023E_H$

RCFDCnCFDFFSTSLL: <RCFDCn_base> + $023C_H$,

RCFDCnCFDFFSTSLH: <RCFDCn_base> + $023D_H$,

RCFDCnCFDFFSTSHL: <RCFDCn_base> + $023E_H$,

RCFDCnCFDFFSTSHH: <RCFDCn_base> + $023F_H$

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CF23FLL	CF22FLL	CF21FLL	CF20FLL	CF19FLL	CF18FLL	CF17FLL	CF16FLL	CF15FLL	CF14FLL	CF13FLL	CF12FLL	CF11FLL	CF10FLL	CF9FLL	CF8FLL
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CF7FLL	CF6FLL	CF5FLL	CF4FLL	CF3FLL	CF2FLL	CF1FLL	CF0FLL	RF7FLL	RF6FLL	RF5FLL	RF4FLL	RF3FLL	RF2FLL	RF1FLL	RF0FLL
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 24.81 RCFDCnCFDFFSTS Register Contents

Bit Position	Bit Name	Function
31	CF23FLL	Transmit/Receive FIFO Buffer Full Status Flag 0: Transmit/receive FIFO buffer k is not full. 1: Transmit/receive FIFO buffer k is full. (k = 0 to 23)
30	CF22FLL	
29	CF21FLL	
28	CF20FLL	
27	CF19FLL	
26	CF18FLL	
25	CF17FLL	
24	CF16FLL	
23	CF15FLL	
22	CF14FLL	
21	CF13FLL	
20	CF12FLL	
19	CF11FLL	
18	CF10FLL	
17	CF9FLL	
16	CF8FLL	
15	CF7FLL	
14	CF6FLL	
13	CF5FLL	
12	CF4FLL	

Table 24.81 RCFDCnCFDFFSTS Register Contents

Bit Position	Bit Name	Function
11	CF3EMP	Transmit/Receive FIFO Buffer Full Status Flag 0: Transmit/receive FIFO buffer k is not full. 1: Transmit/receive FIFO buffer k is full. (k = 0 to 23)
10	CF2EMP	
9	CF1EMP	
8	CF0EMP	
7	RF7FLL	Receive FIFO Buffer Full Status Flag 0: Receive FIFO buffer x is not full. 1: Receive FIFO buffer x is full. (x = 0 to 7)
6	RF6FLL	
5	RF5FLL	
4	RF4FLL	
3	RF3FLL	
2	RF2FLL	
1	RF1FLL	
0	RF0FLL	

The RCFDCnCFDFFSTS register is cleared to 0000 0000_H in global reset mode.

CFkFLL Flag (k = 0 to 23)

The CFkFLL flag is set to 1 when the CFFLL flag in the RCFDCnCFDCFSTSk register is set to 1 (the transmit/receive FIFO buffer is full).

When the CFFLL flag is cleared to 0 (the transmit/receive FIFO buffer is not full), the CFkFLL flag is cleared to 0.

RFxFLL Flag (x = 0 to 7)

The RFxFLL flag is set to 1 when the RFFLL flag in the RCFDCnCFDRFSTSx register is set to 1 (the receive FIFO buffer is full). When the RFFLL flag is cleared to 0 (the receive FIFO buffer is not full), the RFxFLL flag is cleared to 0.

24.3.8.3 RCFDCnCFDFMSTS — FIFO Message Lost Status Register

Access: RCFDCnCFDFMSTS register is a read-only register that can be read in 32-bit units

RCFDCnCFDFMSTSL, RCFDCnCFDFMSTSH registers are read-only registers that can be read in 16-bit units

RCFDCnCFDFMSTSLL, RCFDCnCFDFMSTSLH, RCFDCnCFDFMSTSHL, RCFDCnCFDFMSTSHH registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDFMSTS: <RCFDCn_base> + 0240_H

RCFDCnCFDFMSTSL: <RCFDCn_base> + 0240_H,

RCFDCnCFDFMSTSH: <RCFDCn_base> + 0242_H

RCFDCnCFDFMSTSLL: <RCFDCn_base> + 0240_H,

RCFDCnCFDFMSTSLH: <RCFDCn_base> + 0241_H,

RCFDCnCFDFMSTSHL: <RCFDCn_base> + 0242_H,

RCFDCnCFDFMSTSHH: <RCFDCn_base> + 0243_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CF23MLT	CF22MLT	CF21MLT	CF20MLT	CF19MLT	CF18MLT	CF17MLT	CF16MLT	CF15MLT	CF14MLT	CF13MLT	CF12MLT	CF11MLT	CF10MLT	CF9MLT	CF8MLT
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CF7MLT	CF6MLT	CF5MLT	CF4MLT	CF3MLT	CF2MLT	CF1MLT	CF0MLT	RF7MLT	RF6MLT	RF5MLT	RF4MLT	RF3MLT	RF2MLT	RF1MLT	RF0MLT
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 24.82 RCFDCnCFDFMSTS Register Contents

Bit Position	Bit Name	Function
31	CF23MLT	Transmit/Receive FIFO Buffer Message Lost Status Flag 0: No transmit/receive FIFO buffer k message is lost. 1: A transmit/receive FIFO buffer k message is lost. (k = 0 to 23)
30	CF22MLT	
29	CF21MLT	
28	CF20MLT	
27	CF19MLT	
26	CF18MLT	
25	CF17MLT	
24	CF16MLT	
23	CF15MLT	
22	CF14MLT	
21	CF13MLT	
20	CF12MLT	
19	CF11MLT	
18	CF10MLT	
17	CF9MLT	
16	CF8MLT	
15	CF7MLT	
14	CF6MLT	
13	CF5MLT	
12	CF4MLT	

Table 24.82 RCFDCnCFDFMSTS Register Contents

Bit Position	Bit Name	Function
11	CF3MLT	Transmit/Receive FIFO Buffer Message Lost Status Flag 0: No transmit/receive FIFO buffer k message is lost. 1: A transmit/receive FIFO buffer k message is lost. (k = 0 to 23)
10	CF2MLT	
9	CF1MLT	
8	CF0MLT	
7	RF7MLT	Receive FIFO Buffer Message Lost Status Flag 0: No receive FIFO buffer x message is lost. 1: A receive FIFO buffer x message is lost. (x = 0 to 7)
6	RF6MLT	
5	RF5MLT	
4	RF4MLT	
3	RF3MLT	
2	RF2MLT	
1	RF1MLT	
0	RF0MLT	

The RCFDCnCFDFMSTS register is cleared to 0000 0000_H in global reset mode.

CFkMLT Flag (k = 0 to 23)

The CFkMLT flag is set to 1 when the CFMLT flag in the RCFDCnCFDCFSTSk register is set to 1 (a transmit/receive FIFO message is lost). When the CFMLT flag is cleared to 0, the CFkMLT flag is cleared to 0.

RFxMLT Flag (x = 0 to 7)

The RFxMLT flag is set to 1 when the RFMLT flag in the RCFDCnCFDRFSTSx register is set to 1 (a receive FIFO message is lost). When the RFMLT flag is cleared to 0, the RFxMLT flag is cleared to 0.

24.3.8.4 RCFDCnCFDRFISTS — Receive FIFO Buffer Interrupt Flag Status Register

Access: RCFDCnCFDRFISTS register is a read-only register that can be read in 32-bit units
RCFDCnCFDRFISTSL register is a read-only register that can be read in 16-bit units
RCFDCnCFDRFISTSLL register is a read-only register that can be read in 8-bit units

Address: RCFDCnCFDRFISTS: <RCFDCn_base> + 0244_H
RCFDCnCFDRFISTSL: <RCFDCn_base> + 0244_H
RCFDCnCFDRFISTSLL: <RCFDCn_base> + 0244_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	RF7IF	RF6IF	RF5IF	RF4IF	RF3IF	RF2IF	RF1IF	RF0IF
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 24.83 RCFDCnCFDRFISTS Register Contents

Bit Position	Bit Name	Function
31 to 8	Reserved	These bits are read as the value after reset.
7	RF7IF	Receive FIFO Buffer Interrupt Request Status Flag 0: No receive FIFO buffer x interrupt request is present. 1: A receive FIFO buffer x interrupt request is present. (x = 0 to 7)
6	RF6IF	
5	RF5IF	
4	RF4IF	
3	RF3IF	
2	RF2IF	
1	RF1IF	
0	RF0IF	

The RCFDCnCFDRFISTS register is cleared to $0000\ 0000_H$ in global reset mode.

RFxIF Flag (x = 0 to 7)

The RFxIF flag is set to 1 when the RFIF flag in the RCFDCnCFDRFSTSx register is set to 1 (a receive FIFO interrupt request is present). When the RFIF flag is cleared to 0, the RFxIF flag is cleared to 0.

24.3.8.5 RCFDCnCFDCFRISTS — Transmit/receive FIFO Buffer Receive Interrupt Flag Status Register

Access: RCFDCnCFDCFRISTS register is a read-only register that can be read in 32-bit units

RCFDCnCFDCFRISTSL, RCFDCnCFDCFRISTSH registers are read-only registers that can be read in 16-bit units

RCFDCnCFDCFRISTSLL, RCFDCnCFDCFRISTSLH, RCFDCnCFDCFRISTSHL registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDCFRISTS: <RCFDCn_base> + 0248_H

RCFDCnCFDCFRISTSL: <RCFDCn_base> + 0248_H,

RCFDCnCFDCFRISTSH: <RCFDCn_base> + $024A_H$

RCFDCnCFDCFRISTSLL: <RCFDCn_base> + 0248_H,

RCFDCnCFDCFRISTSLH: <RCFDCn_base> + 0249_H,

RCFDCnCFDCFRISTSHL: <RCFDCn_base> + $024A_H$

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	CF23RXIF	CF22RXIF	CF21RXIF	CF20RXIF	CF19RXIF	CF18RXIF	CF17RXIF	CF16RXIF
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CF15RXIF	CF14RXIF	CF13RXIF	CF12RXIF	CF11RXIF	CF10RXIF	CF9RXIF	CF8RXIF	CF7RXIF	CF6RXIF	CF5RXIF	CF4RXIF	CF3RXIF	CF2RXIF	CF1RXIF	CF0RXIF
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 24.84 RCFDCnCFDCFRISTS Register Contents

Bit Position	Bit Name	Function
31 to 24	Reserved	These bits are read as the value after reset.
23	CF23RXIF	Transmit/Receive FIFO Buffer Receive Interrupt Request Status Flag 0: No transmit/receive FIFO buffer k receive interrupt request is present. 1: A transmit/receive FIFO buffer k receive interrupt request is present. (k = 0 to 23)
22	CF22RXIF	
21	CF21RXIF	
20	CF20RXIF	
19	CF19RXIF	
18	CF18RXIF	
17	CF17RXIF	
16	CF16RXIF	
15	CF15RXIF	
14	CF14RXIF	
13	CF13RXIF	
12	CF12RXIF	
11	CF11RXIF	
10	CF10RXIF	
9	CF9RXIF	
8	CF8RXIF	
7	CF7RXIF	
6	CF6RXIF	

Table 24.84 RCFDCnCFDCFRISTS Register Contents

Bit Position	Bit Name	Function
5	CF5RXIF	Transmit/Receive FIFO Buffer Receive Interrupt Request Status Flag 0: No transmit/receive FIFO buffer k receive interrupt request is present. 1: A transmit/receive FIFO buffer k receive interrupt request is present. (k = 0 to 23)
4	CF4RXIF	
3	CF3RXIF	
2	CF2RXIF	
1	CF1RXIF	
0	CF0RXIF	

The RCFDCnCFDCFRISTS register is cleared to 0000 0000_H in global reset mode.

CFkRXIF Flag (k = 0 to 23)

The CFkRXIF flag is set to 1 when the CFRXIF flag in the RCFDCnCFDCFSTSk register is set to 1 (a transmit/receive FIFO receive interrupt request is present). When the CFRXIF flag is cleared to 0, the CFkRXIF flag is cleared to 0.

24.3.8.6 RCFDCnCFDCFTISTS — Transmit/receive FIFO Buffer Transmit Interrupt Flag Status Register

Access: RCFDCnCFDCFTISTS register is a read-only register that can be read in 32-bit units

RCFDCnCFDCFTISTSL, RCFDCnCFDCFTISTSH registers are read-only registers that can be read in 16-bit units

RCFDCnCFDCFTISTSLL, RCFDCnCFDCFTISTSLH, RCFDCnCFDCFTISTSHL registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDCFTISTS: <RCFDCn_base> + $024C_H$

RCFDCnCFDCFTISTSL: <RCFDCn_base> + $024C_H$,

RCFDCnCFDCFTISTSH: <RCFDCn_base> + $024E_H$

RCFDCnCFDCFTISTSLL: <RCFDCn_base> + $024C_H$,

RCFDCnCFDCFTISTSLH: <RCFDCn_base> + $024D_H$,

RCFDCnCFDCFTISTSHL: <RCFDCn_base> + $024E_H$

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	CF23TXIF	CF22TXIF	CF21TXIF	CF20TXIF	CF19TXIF	CF18TXIF	CF17TXIF	CF16TXIF
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CF15TXIF	CF14TXIF	CF13TXIF	CF12TXIF	CF11TXIF	CF10TXIF	CF9TXIF	CF8TXIF	CF7TXIF	CF6TXIF	CF5TXIF	CF4TXIF	CF3TXIF	CF2TXIF	CF1TXIF	CF0TXIF
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 24.85 RCFDCnCFDCFTISTS Register Contents

Bit Position	Bit Name	Function
31 to 24	Reserved	These bits are read as the value after reset.
23	CF23TXIF	Transmit/Receive FIFO Buffer Transmit Interrupt Request Status Flag 0: No transmit/receive FIFO buffer k transmit interrupt request is present. 1: A transmit/receive FIFO buffer k transmit interrupt request is present. (k = 0 to 23)
22	CF22TXIF	
21	CF21TXIF	
20	CF20TXIF	
19	CF19TXIF	
18	CF18TXIF	
17	CF17TXIF	
16	CF16TXIF	
15	CF15TXIF	
14	CF14TXIF	
13	CF13TXIF	
12	CF12TXIF	
11	CF11TXIF	
10	CF10TXIF	
9	CF9TXIF	
8	CF8TXIF	
7	CF7TXIF	
6	CF6TXIF	
5	CF5TXIF	
4	CF4TXIF	

Table 24.85 RCFDCnCFDCFTISTS Register Contents

Bit Position	Bit Name	Function
3	CF3TXIF	Transmit/Receive FIFO Buffer Transmit Interrupt Request Status Flag 0: No transmit/receive FIFO buffer k transmit interrupt request is present. 1: A transmit/receive FIFO buffer k transmit interrupt request is present. (k = 0 to 23)
2	CF2TXIF	
1	CF1TXIF	
0	CF0TXIF	

The RCFDCnCFDCFTISTS register is cleared to 0000 0000_H in global reset mode.

CFkTXIF Flag (k = 0 to 23)

The CFkTXIF flag is set to 1 when the CFTXIF flag in the RCFDCnCFDCFSTSk register is set to 1 (a transmit/receive FIFO transmit interrupt request is present). When the CFTXIF flag is cleared to 0, the CFkTXIF flag is cleared to 0.

24.3.9 Details of FIFO DMA-related Registers

24.3.9.1 RCFDCnCFDCDTCT — DMA Enable Register

Access: RCFDCnCFDCDTCT register can be read or written in 32-bit units

RCFDCnCFDCDTCTL register can be read or written in 16-bit units

RCFDCnCFDCDTCTLL, RCFDCnCFDCDTCTLH registers can be read or written in 8-bit units

Address: RCFDCnCFDCDTCT: <RCFDCn_base> + 0640_H

RCFDCnCFDCDTCTL: <RCFDCn_base> + 0640_H

RCFDCnCFDCDTCTLL: <RCFDCn_base> + 0640_H,

RCFDCnCFDCDTCTLH: <RCFDCn_base> + 0641_H

Value after reset: 0000 0000_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CFDMAE7	CFDMAE6	CFDMAE5	CFDMAE4	CFDMAE3	CFDMAE2	CFDMAE1	CFDMAE0	RFDMAE7	RFDMAE6	RFDMAE5	RFDMAE4	RFDMAE3	RFDMAE2	RFDMAE1	RFDMAE0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 24.86 RCFDCnCFDCDTCT Register Contents

Bit Position	Bit Name	Function
31 to 16	Reserved	These bits are read as the value after reset. The write value should be the value after reset.
15	CFDMAE7	Transmit/Receive FIFO Buffer 21 DMA Enable 0: A DMA transfer request of transmit/receive FIFO buffer 21 is disabled. 1: A DMA transfer request of transmit/receive FIFO buffer 21 is enabled.
14	CFDMAE6	Transmit/Receive FIFO Buffer 18 DMA Enable 0: A DMA transfer request of transmit/receive FIFO buffer 18 is disabled. 1: A DMA transfer request of transmit/receive FIFO buffer 18 is enabled.
13	CFDMAE5	Transmit/Receive FIFO Buffer 15 DMA Enable 0: A DMA transfer request of transmit/receive FIFO buffer 15 is disabled. 1: A DMA transfer request of transmit/receive FIFO buffer 15 is enabled.
12	CFDMAE4	Transmit/Receive FIFO Buffer 12 DMA Enable 0: A DMA transfer request of transmit/receive FIFO buffer 12 is disabled. 1: A DMA transfer request of transmit/receive FIFO buffer 12 is enabled.
11	CFDMAE3	Transmit/Receive FIFO Buffer 9 DMA Enable 0: A DMA transfer request of transmit/receive FIFO buffer 9 is disabled. 1: A DMA transfer request of transmit/receive FIFO buffer 9 is enabled.
10	CFDMAE2	Transmit/Receive FIFO Buffer 6 DMA Enable 0: A DMA transfer request of transmit/receive FIFO buffer 6 is disabled. 1: A DMA transfer request of transmit/receive FIFO buffer 6 is enabled.

Table 24.86 RCFDCnCFDCDTCT Register Contents

Bit Position	Bit Name	Function
9	CFDMAE1	Transmit/Receive FIFO Buffer 3 DMA Enable 0: A DMA transfer request of transmit/receive FIFO buffer 3 is disabled. 1: A DMA transfer request of transmit/receive FIFO buffer 3 is enabled.
8	CFDMAE0	Transmit/Receive FIFO Buffer 0 DMA Enable 0: A DMA transfer request of transmit/receive FIFO buffer 0 is disabled. 1: A DMA transfer request of transmit/receive FIFO buffer 0 is enabled.
7	RFDMAE7	RH850/F1KH-D8, RH850/F1KM-S4, RH850/F1KM-S2: Receive FIFO Buffer x DMA Enable 0: A DMA transfer request of receive FIFO buffer x is disabled. 1: A DMA transfer request of receive FIFO buffer x is enabled. (x = 0 to 7) RH850/F1KM-S1: Receive FIFO Buffer x DMA Enable 0: A DMA transfer request of receive FIFO buffer x is disabled. 1: A DMA transfer request of receive FIFO buffer x is enabled. (x = 0 to 5)
6	RFDMAE6	
5	RFDMAE5	
4	RFDMAE4	
3	RFDMAE3	
2	RFDMAE2	
1	RFDMAE1	
0	RFDMAE0	

Modify the RCFDCnCFDCDTCT register in global operating mode or global test mode.

CFDMAEm Bit

This bit is used to enable DMA transfer for transmit/receive FIFO buffer 3 × m (the first transmit/ receive FIFO buffer allocated to channel m). DMA transfer is enabled only for transmit/receive FIFO buffers for which the CFM[1:0] bits in the RCFDCnCFDCFCCk register is set to 00_B (receive mode).

Set this bit to 0 when the CFM[1:0] value is 01_B (transmit mode) or 10_B (gateway mode).

RFDMAEx Bit

This bit is used to enable DMA transfer for receive FIFO buffer x.

24.3.9.2 RCFDCnCFDCDTSTS — DMA Status Register

Access: RCFDCnCFDCDTSTS register is a read-only register that can be read in 32-bit units

RCFDCnCFDCDTSTSL register is a read-only register that can be read in 16-bit units

RCFDCnCFDCDTSTSLL, RCFDCnCFDCDTSTSLH registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDCDTSTS: <RCFDCn_base> + 0644_H

RCFDCnCFDCDTSTSL: <RCFDCn_base> + 0644_H

RCFDCnCFDCDTSTSLL: <RCFDCn_base> + 0644_H,

RCFDCnCFDCDTSTSLH: <RCFDCn_base> + 0645_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CFDMASTS7	CFDMASTS6	CFDMASTS5	CFDMASTS4	CFDMASTS3	CFDMASTS2	CFDMASTS1	CFDMASTS0	RFDMASTS7	RFDMASTS6	RFDMASTS5	RFDMASTS4	RFDMASTS3	RFDMASTS2	RFDMASTS1	RFDMASTS0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 24.87 RCFDCnCFDCDTSTS Register Contents

Bit Position	Bit Name	Function
31 to 16	Reserved	These bits are read as the value after reset.
15	CFDMASTS7	Transmit/Receive FIFO Buffer 21 DMA Status 0: DMA transfer of transmit/receive FIFO buffer 21 is not in progress. 1: DMA transfer of transmit/receive FIFO buffer 21 is in progress.
14	CFDMASTS6	Transmit/Receive FIFO Buffer 18 DMA Status 0: DMA transfer of transmit/receive FIFO buffer 18 is not in progress. 1: DMA transfer of transmit/receive FIFO buffer 18 is in progress.
13	CFDMASTS5	Transmit/Receive FIFO Buffer 15 DMA Status 0: DMA transfer of transmit/receive FIFO buffer 15 is not in progress. 1: DMA transfer of transmit/receive FIFO buffer 15 is in progress.
12	CFDMASTS4	Transmit/Receive FIFO Buffer 12 DMA Status 0: DMA transfer of transmit/receive FIFO buffer 12 is not in progress. 1: DMA transfer of transmit/receive FIFO buffer 12 is in progress.
11	CFDMASTS3	Transmit/Receive FIFO Buffer 9 DMA Status 0: DMA transfer of transmit/receive FIFO buffer 9 is not in progress. 1: DMA transfer of transmit/receive FIFO buffer 9 is in progress.
10	CFDMASTS2	Transmit/Receive FIFO Buffer 6 DMA Status 0: DMA transfer of transmit/receive FIFO buffer 6 is not in progress. 1: DMA transfer of transmit/receive FIFO buffer 6 is in progress.
9	CFDMASTS1	Transmit/Receive FIFO Buffer 3 DMA Status 0: DMA transfer of transmit/receive FIFO buffer 3 is not in progress. 1: DMA transfer of transmit/receive FIFO buffer 3 is in progress.

Table 24.87 RCFDCnCFDCDTSTS Register Contents

Bit Position	Bit Name	Function
8	CFDMASTS0	Transmit/Receive FIFO Buffer 0 DMA Status 0: DMA transfer of transmit/receive FIFO buffer 0 is not in progress. 1: DMA transfer of transmit/receive FIFO buffer 0 is in progress.
7	RFDMASTS7	RH850/F1KH-D8, RH850/F1KM-S4, RH850/F1KM-S2: Receive FIFO Buffer x DMA Status 0: DMA transfer of receive FIFO buffer x is not in progress. 1: DMA transfer of receive FIFO buffer x is in progress. (x = 0 to 7) RH850/F1KM-S1: Receive FIFO Buffer x DMA Status 0: DMA transfer of receive FIFO buffer x is not in progress. 1: DMA transfer of receive FIFO buffer x is in progress. (x = 0 to 5)
6	RFDMASTS6	
5	RFDMASTS5	
4	RFDMASTS4	
3	RFDMASTS3	
2	RFDMASTS2	
1	RFDMASTS1	
0	RFDMASTS0	

CFDMASTSm Bit

When DMA transfer is enabled (CFDMAEm bit in the RCFDCnCFDCDTCT register is 1) for the transmit/receive FIFO buffer 3 × m (the first transmit/receive FIFO buffer allocated to channel m) while the transmit/receive FIFO buffer contains one of more messages, the CFDMASTSm bit is set to 1 indicating that DMA transfer is in progress.

When all messages in the transmit/receive FIFO buffer have been transferred or DMA transfer is disabled (CFDMAEm bit is 0), the CFDMASTSm bit is cleared to 0 indicating that DMA transfer has been completed. If the CFDMAEm bit is set to 0 during DMA transfer, the CFDMASTSm bit is cleared to 0 after the ongoing DMA transfer has been completed (when the message that is being transferred has been transferred to the last byte in the payload storage area).

These bits are cleared to 0 in global reset mode.

RFDMASTSx Bit

When DMA transfer is enabled (corresponding RFDMAEx bit in the RCFDCnCFDCDTCT register is 1) for the receive FIFO buffer x and the receive FIFO buffer contains one of more messages, the RFDMASTSx bit is set to 1 indicating that DMA transfer is in progress.

When all messages in the receive FIFO buffer x have been transferred or DMA transfer is disabled (RFDMAEx bit = 0), the RFDMASTSx bit is cleared to 0 indicating that DMA transfer has been completed. If the RFDMAEx bit is set to 0 during DMA transfer, the RFDMASTSx bit is cleared to 0 after the ongoing DMA transfer has been completed (when the message that is being transferred has been transferred to the last byte in the payload storage area) These bits are cleared to 0 in global reset mode.

24.3.10 Details of Transmit Buffer-related Registers

24.3.10.1 RCFDCnCFDTMCp — Transmit Buffer Control Register (p = 0 to 255)

Access: RCFDCnCFDTMCp register can be read or written in 8-bit units

Address: RCFDCnCFDTMCp: <RCFDCn_base> + 0250_H + (01_H × p)

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	TMOM	TMTAR	TMTR
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R/W	R/W*1	R/W*1

Note 1. The only effective value for writing to this bit is 1, which sets the bit. Otherwise writing to the bit results in retention of its state.

Table 24.88 RCFDCnCFDTMCp Register Contents

Bit Position	Bit Name	Function
7 to 3	Reserved	These bits are read as the value after reset. The write value should be the value after reset.
2	TMOM	One-Shot Transmission Enable 0: One-shot transmission is disabled. 1: One-shot transmission is enabled.
1	TMTAR	Transmit Abort Request 0: Transmit abort is not requested. 1: Transmit abort is requested.
0	TMTR	Transmit Request 0: Transmission is not requested. 1: Transmission is requested.

When the RCFDCnCFDTMCp register meets any of the following conditions, set it to 00_H.

- The RCFDCnCFDTMCp register corresponds to the transmit buffer number selected by the CFTML[4:0] bits in the RCFDCnCFDCFCCk register (p = m × 32 + the value of CFTML[4:0] bits).
- The RCFDCnCFDTMCp register corresponds to the transmit buffer allocated to the transmit queue by the TXQDC[4:0] bits in the RCFDCnCFDTXQCCm (m = 0 to 7) register (p = (m × 32 + 31) to (m × 32 + 31 – the value of TXQDC[4:0] bits)).

All of the bits in the RCFDCnCFDTMCp register are cleared to 0 in channel reset mode. Modify the RCFDCnCFDTMCp register in channel communication mode or channel halt mode.

TMOM Bit

Setting this bit to 1 enables one-shot transmission. If transmission fails, retransmission defined in the CAN protocol is not performed.

Modify the TMOM bit when the TMTRM flag in the RCFDCnCFDTMSTSp register is set to 0. Set the TMOM bit to 1 together with the TMTR bit.

TMTAR Bit

Setting this bit to 1 generates a transmit abort request for the message stored in the transmit buffer. However, a message that is being transmitted or one that will be transmitted next cannot be aborted.

The TMTAR bit can be set to 1 when TMTR bit is 1.

The TMTAR bit is cleared to 0 when any of the following conditions is met, but cannot be cleared by the program writing 0 to the bit.

- Transmission has been completed.
- Transmit abort has been completed.
- An error or arbitration-lost has been detected.

If this bit becomes 0 at the same time as the program writes 1 to this bit, this bit becomes 0.

TMTR Bit

Setting this bit to 1 transmits the message stored in the transmit buffer.

The TMTR bit is cleared to 0 when any of the following conditions is met, but cannot be cleared by the program writing 0 to the bit.

- Transmission has been completed.
- Transmit abort has been completed after the TMTAR bit was set to 1.
- An error or arbitration-lost has been detected with the TMOM bit set to 1.

Set the TMTR bit to 1 when the value of TMTRF[1:0] in the RCFDCnCFDTMSTSp register is 00_B.

24.3.10.2 RCFDCnCFDTMSTSp — Transmit Buffer Status Register (p = 0 to 255)

Access: RCFDCnCFDTMSTSp register can be read or written in 8-bit units

Address: RCFDCnCFDTMSTSp: <RCFDCn_base> + 0350_H + (01_H × p)

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	—	TMTARM	TMTRM	TMTRF[1:0]		TMTSTS
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R/W	R/W	R

Table 24.89 RCFDCnCFDTMSTSp Register Contents

Bit Position	Bit Name	Function
7 to 5	Reserved	These bits are read as the value after reset. The write value should be the value after reset.
4	TMTARM	Transmit Buffer Transmit Abort Request Status Flag 0: No transmit abort request is present. 1: A transmit abort request is present.
3	TMTRM	Transmit Buffer Transmit Request Status Flag 0: No transmit request is present. 1: A transmit request is present.
2, 1	TMTRF[1:0]	Transmit Buffer Transmit Result Status Flag b2 b1 0 0: Transmission is in progress or no transmit request is present. 0 1: Transmit abort has been completed. 1 0: Transmission has been completed (without transmit abort request). 1 1: Transmission has been completed (with transmit abort request).
0	TMTSTS	Transmit Buffer Transmit Status Flag 0: Transmission is not in progress. 1: Transmission is in progress.

All of the bits in the RCFDCnCFDTMSTSp register are cleared to 0 in channel reset mode.

TMTARM Flag

The TMTARM flag is set to 1 when the TMTAR bit in the RCFDCnCFDTMCp register is set to 1. The TMTARM flag is set to 0 when the TMTAR bit in the RCFDCnCFDTMCp register is set to 0.

TMTRM Flag

The TMTRM flag is set to 1 when the TMTR bit in the RCFDCnCFDTMCp register is set to 1. The TMTRM flag is set to 0 when the TMTR bit in the RCFDCnCFDTMCp register is set to 0.

TMTRF[1:0] Flag

This flag indicates the result of transmission from the transmit buffer.

00_B: Transmission is in progress or no transmit request is present.

01_B: Transmission from the transmit buffer was aborted.

10_B: Transmission has been completed with the TMTAR bit in the RCFDCnCFDTMCp register set to 0 (transmit abort is not requested).

11_B: Transmission has been completed with the TMTAR bit in the RCFDCnCFDTMCp register set to 1 (transmit abort is requested).

Write 00_B to the TMTRF[1:0] flag in channel communication mode or channel halt mode. Do not write any value other than 00_B to this flag.

TMTSTS Flag

This flag is set to 1 when transmission from the transmit buffer starts, and is cleared to 0 when transmission from the transmit buffer has been completed or terminated due to a bus error or arbitration lost.

24.3.10.3 RCFDCnCFDTMIDp — Transmit Buffer ID Register (p = 0 to 255)

Access: RCFDCnCFDTMIDp register can be read or written in 32-bit units

RCFDCnCFDTMIDpL, RCFDCnCFDTMIDpH registers can be read or written in 16-bit units

RCFDCnCFDTMIDpLL, RCFDCnCFDTMIDpLH, RCFDCnCFDTMIDpHL, RCFDCnCFDTMIDpHH registers can be read or written in 8-bit units

Address: RCFDCnCFDTMIDp: <RCFDCn_base> + 8000_H + (80_H × p)

RCFDCnCFDTMIDpL: <RCFDCn_base> + 8000_H + (80_H × p),

RCFDCnCFDTMIDpH: <RCFDCn_base> + 8002_H + (80_H × p)

RCFDCnCFDTMIDpLL: <RCFDCn_base> + 8000_H + (80_H × p),

RCFDCnCFDTMIDpLH: <RCFDCn_base> + 8001_H + (80_H × p),

RCFDCnCFDTMIDpHL: <RCFDCn_base> + 8002_H + (80_H × p),

RCFDCnCFDTMIDpHH: <RCFDCn_base> + 8003_H + (80_H × p)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TMIDE	TMRTR	THLEN	TMID[28:16]												
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TMID[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 24.90 RCFDCnCFDTMIDp Register Contents

Bit Position	Bit Name	Function
31	TMIDE	Transmit Buffer IDE 0: Standard ID 1: Extended ID
30	TMRTR	Transmit Buffer RTR/RRS • When the transmit message is a classical CAN frame 0: Data frame 1: Remote frame • When the transmit message is a CAN FD frame Write 0 to this bit.
29	THLEN	Transmit History Data Store Enable 0: Transmit history data is not stored in the buffer. 1: Transmit history data is stored in the buffer.
28 to 0	TMID[28:0]	Transmit Buffer ID Data Set standard ID or extended ID. For standard ID, write an ID to bits 10 to 0 and write 0 to bits 28 to 11.

Modify this register when the TMTRM bit in the corresponding RCFDCnCFDTMSTSp register is set to 0 (no transmit request is present). If this register is linked to a transmit/receive FIFO buffer, do not write data to this register. If this register is allocated to the transmit queue, only write data to a transmit buffer p (p = m × 32 + 31) for the corresponding channel.

TMIDE Bit

This bit is used to set the ID format of the message to be transmitted from the transmit buffer.

TMRTR Bit

This bit is used to set the data format of the message to be transmitted from the transmit buffer.

Set this bit to 0 when the TMFDF bit in the RCFDCnCFDTMFDCTRp register is 1 (CAN FD frame).

THLEN Bit

When this bit is set to 1, the transmit history data (label information, buffer number, buffer type, and timestamp) of transmit messages is stored in the transmit history buffer after transmission is completed.

TMID[28:0] Bits

These bits are used to set the ID of the message to be transmitted from the transmit buffer.

24.3.10.4 RCFDCnCFDTMPTRp — Transmit Buffer Pointer Register (p = 0 to 255)

Access: RCFDCnCFDTMPTRp register can be read or written in 32-bit units
RCFDCnCFDTMPTRpH register can be read or written in 16-bit units
RCFDCnCFDTMPTRpHH register can be read or written in 8-bit units

Address: RCFDCnCFDTMPTRp: <RCFDCn_base> + 8004_H + (80_H × p)
RCFDCnCFDTMPTRpH: <RCFDCn_base> + 8006_H + (80_H × p)
RCFDCnCFDTMPTRpHH: <RCFDCn_base> + 8007_H + (80_H × p)

Value after reset: 0000 0000_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TMDLC[3:0]				—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 24.91 RCFDCnCFDTMPTRp Register Contents

Bit Position	Bit Name	Function
31 to 28	TMDLC[3:0]	Transmit Buffer DLC Data
27 to 0	Reserved	When read, the value after reset is returned. When writing to these bits, write the value after reset.

b31	b30	b29	b28	Classical CAN Frame	CAN FD Frame
0	0	0	0	0 data bytes	
0	0	0	1	1 data byte	
0	0	1	0	2 data bytes	
0	0	1	1	3 data bytes	
0	1	0	0	4 data bytes	
0	1	0	1	5 data bytes	
0	1	1	0	6 data bytes	
0	1	1	1	7 data bytes	
1	0	0	0	8 data bytes	
1	0	0	1	8 data bytes	12 data bytes
1	0	1	0		16 data bytes
1	0	1	1		20 data bytes
1	1	0	0		24 data bytes
1	1	0	1		32 data bytes
1	1	1	0		48 data bytes
1	1	1	1		64 data bytes

Modify this register when the TMTRM bit in the corresponding RCFDCnCFDTMSTSp register is set to 0 (no transmit request is present). If this register is linked to a transmit/receive FIFO buffer, do not write to this register. If this register is allocated to the transmit queue, only write to a transmit buffer p (p = m × 32 + 31) for the corresponding channel.

TMDLC[3:0] Bits

These bits are used to set the data length of the message to be transmitted from the transmit buffer when the TMRTR bit in the RCFDCnCFDTMIDp register is set to 0 (data frame).

When the TMDLC[3:0] bits are set to 1001_B or more while the TMFDF bit in the RCFDCnCFDTMFDCTRp register is 0 (classical CAN frame), 8-byte data is transmitted actually. When the TMRTR bit is 1 (remote frame), these bits set the length of the message to be requested.

24.3.10.5 RCFDCnCFDTMFDCTRp — Transmit Buffer CAN FD Configuration Register (p = 0 to 255)

Access: RCFDCnCFDTMFDCTRp register can be read or written in 32-bit units

RCFDCnCFDTMFDCTRpL, RCFDCnCFDTMFDCTRpH registers can be read or written in 16-bit units

RCFDCnCFDTMFDCTRpLL, RCFDCnCFDTMFDCTRpHL, RCFDCnCFDTMFDCTRpHH registers can be read or written in 8-bit units

Address: RCFDCnCFDTMFDCTRp: <RCFDCn_base> + 8008_H + (80_H × p)

RCFDCnCFDTMFDCTRpL: <RCFDCn_base> + 8008_H + (80_H × p),

RCFDCnCFDTMFDCTRpH: <RCFDCn_base> + $800A_H$ + (80_H × p)

RCFDCnCFDTMFDCTRpLL: <RCFDCn_base> + 8008_H + (80_H × p),

RCFDCnCFDTMFDCTRpHL: <RCFDCn_base> + $800A_H$ + (80_H × p),

RCFDCnCFDTMFDCTRpHH: <RCFDCn_base> + $800B_H$ + (80_H × p)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TMPTR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	TMFDF	TMBRS	TMESI
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Table 24.92 RCFDCnCFDTMFDCTRp Register Contents

Bit Position	Bit Name	Function
31 to 16	TMPTR[15:0]	Transmit Buffer Label Data Set the label information to be stored in the transmit history buffer.
15 to 3	Reserved	These bits are read as the value after reset. The write value should be the value after reset.
2	TMFDF	FDF 0: Classical CAN frame 1: CAN FD frame
1	TMBRS	BRS 0: The bit rate in the data area does not change. 1: The bit rate in the data area changes.
0	TMESI	ESI 0: Error active node 1: Error passive node

Modify this register when the TMTRM bit in the corresponding RCFDCnCFDTMSTSp register is set to 0 (transmission not requested). When this register is linked to the transmit/receive FIFO buffer, do not write data to this register. When this register is allocated to the transmit queue, write data only to transmit buffer p (p = m × 32 + 31) of the corresponding channel.

TMPTR[15:0] Bits

When message transmission has been completed, the TMPTR[15:0] value is stored in the transmit history buffer.

TMFDF Bit

This bit is used to set the FD format of the message to be transmitted from the transmit buffer.

TMBRS Bit

When this bit is set to 1 while the TMFDF bit is set to 1, the data area of a transmit message is transmitted at the data bit rate. When the TMFDF bit is set to 0, write 0 to this bit.

TMESI Bit

This bit is used to set the ESI bit value of the message to be transmitted from the transmit buffer when the TMFDF bit is set to 1. The set value is transmitted when the ESIC bit in the RCFDCnCFDCmFDCFG register is set to 1 and the channel is in the error active state. When the channel is in the error passive state, the ESI bit value that shows an error passive node is transmitted regardless of this bit value. When the TMFDF bit is set to 0, write 0 to this bit.

24.3.10.6 RCFDCnCFDTMDFb_p — Transmit Buffer Data Field Register (b = 0 to 15, p = 0 to 255)

Access: RCFDCnCFDTMDFb_p register can be read or written in 32-bit units

RCFDCnCFDTMDFb_pL, RCFDCnCFDTMDFb_pH registers can be read or written in 16-bit units

RCFDCnCFDTMDFb_pLL, RCFDCnCFDTMDFb_pLH, RCFDCnCFDTMDFb_pHL, RCFDCnCFDTMDFb_pHH registers can be read or written in 8-bit units

Address: RCFDCnCFDTMDFb_p: <RCFDCn_base> + $800C_H$ + (04_H × b) + (80_H × p)

RCFDCnCFDTMDFb_pL: <RCFDCn_base> + $800C_H$ + (04_H × b) + (80_H × p),

RCFDCnCFDTMDFb_pH: <RCFDCn_base> + $800E_H$ + (04_H × b) + (80_H × p)

RCFDCnCFDTMDFb_pLL: <RCFDCn_base> + $800C_H$ + (04_H × b) + (80_H × p),

RCFDCnCFDTMDFb_pLH: <RCFDCn_base> + $800D_H$ + (04_H × b) + (80_H × p),

RCFDCnCFDTMDFb_pHL: <RCFDCn_base> + $800E_H$ + (04_H × b) + (80_H × p),

RCFDCnCFDTMDFb_pHH: <RCFDCn_base> + $800F_H$ + (04_H × b) + (80_H × p)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TMDB4 × b + 3 [7:0]								TMDB4 × b + 2 [7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TMDB4 × b + 1 [7:0]								TMDB4 × b + 0 [7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 24.93 RCFDCnCFDTMDFb_p Register Contents

Bit Position	Bit Name	Function
31 to 24	TMDB4 × b + 3 [7:0]	Transmit Buffer Data Byte 4 × b + 3 Transmit Buffer Data Byte 4 × b + 2 Transmit Buffer Data Byte 4 × b + 1 Transmit Buffer Data Byte 4 × b + 0 Set the transmit buffer data.
23 to 16	TMDB4 × b + 2 [7:0]	
15 to 8	TMDB4 × b + 1 [7:0]	
7 to 0	TMDB4 × b + 0 [7:0]	

Modify this register when the TMTRM bit in the corresponding RCFDCnCFDTMSTSp register is set to 0 (no transmit request is present). If this register is linked to a transmit/receive FIFO buffer, do not write to this register. If this register is allocated to the transmit queue, only write to a transmit buffer p (p = m × 32 + 31) for the corresponding channel.

24.3.10.7 RCFDCnCFDTMIECm — Transmit Buffer Interrupt Enable Configuration Register (m = 0 to 7)

Access: RCFDCnCFDTMIECm register can be read or written in 32-bit units

RCFDCnCFDTMIECmL, RCFDCnCFDTMIECmH registers can be read or written in 16-bit units

RCFDCnCFDTMIECmLL, RCFDCnCFDTMIECmLH, RCFDCnCFDTMIECmHL, RCFDCnCFDTMIECmHH registers can be read or written in 8-bit units

Address: RCFDCnCFDTMIECm: <RCFDCn_base> + $04D0_H$ + (04_H × m)

RCFDCnCFDTMIECmL: <RCFDCn_base> + $04D0_H$ + (04_H × m),

RCFDCnCFDTMIECmH: <RCFDCn_base> + $04D2_H$ + (04_H × m)

RCFDCnCFDTMIECmLL: <RCFDCn_base> + $04D0_H$ + (04_H × m),

RCFDCnCFDTMIECmLH: <RCFDCn_base> + $04D1_H$ + (04_H × m),

RCFDCnCFDTMIECmHL: <RCFDCn_base> + $04D2_H$ + (04_H × m),

RCFDCnCFDTMIECmHH: <RCFDCn_base> + $04D3_H$ + (04_H × m)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TMIEp (p = m × 32 + 31 to m × 32 + 16 (m = 0 to 7))															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TMIEp (p = m × 32 + 15 to m × 32 + 0 (m = 0 to 7))															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 24.94 RCFDCnCFDTMIECm Register Contents

Bit Position	Bit Name	Function
31 to 16	TMIEp	Transmit Buffer Interrupt Enable p (p = m × 32 + 31 to m × 32 + 16) 0: Transmit buffer interrupt is disabled 1: Transmit buffer interrupt is enabled
15 to 0	TMIEp	Transmit Buffer Interrupt Enable p (p = m × 32 + 15 to m × 32 + 0) 0: Transmit buffer interrupt is disabled. 1: Transmit buffer interrupt is enabled.

TMIEp Bits (p = 0 to 255)

When any of these bits is set to 1 and the corresponding transmission has been completed, a transmit buffer interrupt request is generated.

Modify these bits when the TMTRM flag in the corresponding RCFDCnCFDTMSTSp register is 0 (no transmit request is present).

Write 0 to bits corresponding to transmit buffers linked to transmit/receive FIFO buffers or transmit buffers allocated to the transmit queue.

Table 24.95, TMIEp Bit Assignment shows the bit assignment.

Table 24.95 TMIEp Bit Assignment

Bit Position	Channel	Transmit Buffer Number
0	0	0
1	0	1
.	.	.
.	.	.
31	0	31
32	1	0
.	.	.
.	.	.
62	1	30
63	1	31
64	2	0
65	2	1
.	.	.
.	.	.
95	2	31
96	3	0
.	.	.
.	.	.
126	3	30
127	3	31
128	4	0
129	4	1
.	.	.
.	.	.
158	4	30
159	4	31
160	5	0
161	5	1
.	.	.
.	.	.
191	5	31
192	6	0
.	.	.
.	.	.
222	6	30
223	6	31
224	7	0
225	7	1
.	.	.
.	.	.
254	7	30
255	7	31

24.3.11 Details of Transmit Buffer Status-related Registers

24.3.11.1 RCFDCnCFDTMTRSTSm — Transmit Buffer Transmit Request Status Register (m = 0 to 7)

Access: RCFDCnCFDTMTRSTSm register is a read-only register that can be read in 32-bit units

RCFDCnCFDTMTRSTSmL, RCFDCnCFDTMTRSTSmH registers are read-only registers that can be read in 16-bit units

RCFDCnCFDTMTRSTSmLL, RCFDCnCFDTMTRSTSmLH, RCFDCnCFDTMTRSTSmHL, RCFDCnCFDTMTRSTSmHH registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDTMTRSTSm: <RCFDCn_base> + 0450_H + (04_H × m)

RCFDCnCFDTMTRSTSmL: <RCFDCn_base> + 0450_H + (04_H × m),

RCFDCnCFDTMTRSTSmH: <RCFDCn_base> + 0452_H + (04_H × m)

RCFDCnCFDTMTRSTSmLL: <RCFDCn_base> + 0450_H + (04_H × m),

RCFDCnCFDTMTRSTSmLH: <RCFDCn_base> + 0451_H + (04_H × m),

RCFDCnCFDTMTRSTSmHL: <RCFDCn_base> + 0452_H + (04_H × m),

RCFDCnCFDTMTRSTSmHH: <RCFDCn_base> + 0453_H + (04_H × m)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TMTRSTSp (p = m × 32 + 31 to m × 32 + 16 (m = 0 to 7))															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TMTRSTSp (p = m × 32 + 15 to m × 32 + 0 (m = 0 to 7))															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 24.96 RCFDCnCFDTMTRSTSm Register Contents

Bit Position	Bit Name	Function
31 to 16	TMTRSTSp	Transmit Buffer Transmit Request Status Flag p (p = m × 32 + 31 to m × 32 + 16) 0: No transmit request is present. 1: A transmit request is present.
15 to 0	TMTRSTSp	Transmit Buffer Transmit Request Status Flag p (p = m × 32 + 15 to m × 32 + 0) 0: No transmit request is present. 1: A transmit request is present.

TMTRSTSp Flags (p = 0 to 255)

These flags indicate the status of the TMTR bit in the RCFDCnCFDTMCp register.

When the TMTR bit is set to 1 (transmission is requested), the corresponding TMTRSTSp flag is set to 1.

The corresponding TMTRSTSp flag is cleared to 0 when the TMTR bit is set to 0 (transmission is not requested) or in channel reset mode.

Table 24.97, TMTRSTSp Bit Assignment shows the bit assignment.

Table 24.97 TMTRSTSp Bit Assignment

Bit Position	Channel	Transmit Buffer Number
0	0	0
1	0	1
.	.	.
.	.	.
31	0	31
32	1	0
.	.	.
.	.	.
62	1	30
63	1	31
64	2	0
65	2	1
.	.	.
.	.	.
95	2	31
96	3	0
.	.	.
.	.	.
126	3	30
127	3	31
128	4	0
129	4	1
.	.	.
.	.	.
158	4	30
159	4	31
160	5	0
161	5	1
.	.	.
.	.	.
191	5	31
192	6	0
.	.	.
.	.	.
222	6	30
223	6	31
224	7	0
225	7	1
.	.	.
.	.	.
254	7	30
255	7	31

24.3.11.2 RCFDCnCFDTMTARSTSm — Transmit Buffer Transmit Abort Request Status Register (m = 0 to 7)

Access: RCFDCnCFDTMTARSTSm register is a read-only register that can be read in 32-bit units

RCFDCnCFDTMTARSTSmL, RCFDCnCFDTMTARSTSmH registers are read-only registers that can be read in 16-bit units

RCFDCnCFDTMTARSTSmLL, RCFDCnCFDTMTARSTSmLH, RCFDCnCFDTMTARSTSmHL, RCFDCnCFDTMTARSTSmHH registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDTMTARSTSm: <RCFDCn_base> + 0470_H + (04_H × m)

RCFDCnCFDTMTARSTSmL: <RCFDCn_base> + 0470_H + (04_H × m),

RCFDCnCFDTMTARSTSmH: <RCFDCn_base> + 0472_H + (04_H × m)

RCFDCnCFDTMTARSTSmLL: <RCFDCn_base> + 0470_H + (04_H × m),

RCFDCnCFDTMTARSTSmLH: <RCFDCn_base> + 0471_H + (04_H × m),

RCFDCnCFDTMTARSTSmHL: <RCFDCn_base> + 0472_H + (04_H × m),

RCFDCnCFDTMTARSTSmHH: <RCFDCn_base> + 0473_H + (04_H × m)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TMTARSTSp (p = m × 32 + 31 to m × 32 + 16 (m = 0 to 7))															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TMTARSTSp (p = m × 32 + 15 to m × 32 + 0 (m = 0 to 7))															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 24.98 RCFDCnCFDTMTARSTSm Register Contents

Bit Position	Bit Name	Function
31 to 16	TMTARSTSp	Transmit Buffer Transmit Abort Request Status Flag p (p = m × 32 + 31 to m × 32 + 16) 0: No transmit abort request is present. 1: A transmit abort request is present.
15 to 0	TMTARSTSp	Transmit Buffer Transmit Abort Request Status Flag p (p = m × 32 + 15 to m × 32 + 0) 0: No transmit abort request is present. 1: A transmit abort request is present.

TMTARSTSp Flags (p = 0 to 255)

These flags indicate the status of the TMTAR bit in the RCFDCnCFDTMCp register.

When the TMTAR bit is set to 1 (transmit abort is requested), the corresponding TMTARSTSp flag is set to 1.

The corresponding TMTARSTSp flag is cleared to 0 when the TMTAR bit is set to 0 (transmit abort is not requested) or in channel reset mode.

Table 24.99, TMTARSTSp Bit Assignment shows the bit assignment.

Table 24.99 TMTARSTSp Bit Assignment

Bit Position	Channel	Transmit Buffer Number
0	0	0
1	0	1
.	.	.
.	.	.
31	0	31
32	1	0
.	.	.
.	.	.
62	1	30
63	1	31
64	2	0
65	2	1
.	.	.
.	.	.
95	2	31
96	3	0
.	.	.
.	.	.
126	3	30
127	3	31
128	4	0
129	4	1
.	.	.
.	.	.
158	4	30
159	4	31
160	5	0
161	5	1
.	.	.
.	.	.
191	5	31
192	6	0
.	.	.
.	.	.
222	6	30
223	6	31
224	7	0
225	7	1
.	.	.
.	.	.
254	7	30
255	7	31

24.3.11.3 RCFDCnCFDTMTCSTSm — Transmit Buffer Transmit Complete Status Register (m = 0 to 7)

Access: RCFDCnCFDTMTCSTSm register is a read-only register that can be read in 32-bit units

RCFDCnCFDTMTCSTSmL, RCFDCnCFDTMTCSTSmH registers are read-only registers that can be read in 16-bit units

RCFDCnCFDTMTCSTSmLL, RCFDCnCFDTMTCSTSmLH, RCFDCnCFDTMTCSTSmHL, RCFDCnCFDTMTCSTSmHH registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDTMTCSTSm: <RCFDCn_base> + 0490_H + (04_H × m)

RCFDCnCFDTMTCSTSmL: <RCFDCn_base> + 0490_H + (04_H × m),

RCFDCnCFDTMTCSTSmH: <RCFDCn_base> + 0492_H + (04_H × m)

RCFDCnCFDTMTCSTSmLL: <RCFDCn_base> + 0490_H + (04_H × m),

RCFDCnCFDTMTCSTSmLH: <RCFDCn_base> + 0491_H + (04_H × m),

RCFDCnCFDTMTCSTSmHL: <RCFDCn_base> + 0492_H + (04_H × m),

RCFDCnCFDTMTCSTSmHH: <RCFDCn_base> + 0493_H + (04_H × m)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TMTCSTSp (p = m × 32 + 31 to m × 32 + 16 (m = 0 to 7))															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TMTCSTSp (p = m × 32 + 15 to m × 32 + 0 (m = 0 to 7))															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 24.100 RCFDCnCFDTMTCSTSm Register Contents

Bit Position	Bit Name	Function
31 to 16	TMTCSTSp	Transmit Buffer Transmit Complete Status Flag p (p = m × 32 + 31 to m × 32 + 16) 0: Transmission has not been completed. 1: Transmission has been completed.
15 to 0	TMTCSTSp	Transmit Buffer Transmit Complete Status Flag p (p = m × 32 + 15 to m × 32 + 0) 0: Transmission has not been completed. 1: Transmission has been completed.

TMTCSTSp Flags (p = 0 to 255)

When the TMTRF[1:0] flag in the RCFDCnCFDTMSTSp register is set to 10_B (transmission has been completed (without transmit abort request)) or 11_B (transmission has been completed (with transmit abort request)), the corresponding TMTCSTSp flag is set to 1.

To clear the TMTCSTSp flag to 0, set the corresponding TMTRF[1:0] flag to 00_B. This flag is cleared to 0 in channel reset mode.

Table 24.101, TMTCSTSp Bit Assignment shows the bit assignment.

Table 24.101 TMTCSTSp Bit Assignment

Bit Position	Channel	Transmit Buffer Number
0	0	0
1	0	1
.	.	.
.	.	.
31	0	31
32	1	0
.	.	.
.	.	.
62	1	30
63	1	31
64	2	0
65	2	1
.	.	.
.	.	.
95	2	31
96	3	0
.	.	.
.	.	.
126	3	30
127	3	31
128	4	0
129	4	1
.	.	.
.	.	.
158	4	30
159	4	31
160	5	0
161	5	1
.	.	.
.	.	.
191	5	31
192	6	0
.	.	.
.	.	.
222	6	30
223	6	31
224	7	0
225	7	1
.	.	.
.	.	.
254	7	30
255	7	31

24.3.11.4 RCFDCnCFDTMTASTSm — Transmit Buffer Transmit Abort Status Register (m = 0 to 7)

Access: RCFDCnCFDTMTASTSm register is a read-only register that can be read in 32-bit units

RCFDCnCFDTMTASTSmL, RCFDCnCFDTMTASTSmH registers are read-only registers that can be read in 16-bit units

RCFDCnCFDTMTASTSmLL, RCFDCnCFDTMTASTSmLH, RCFDCnCFDTMTASTSmHL, RCFDCnCFDTMTASTSmHH registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDTMTASTSm: <RCFDCn_base> + $04B0_H$ + (04_H × m)

RCFDCnCFDTMTASTSmL: <RCFDCn_base> + $04B0_H$ + (04_H × m),

RCFDCnCFDTMTASTSmH: <RCFDCn_base> + $04B2_H$ + (04_H × m)

RCFDCnCFDTMTASTSmLL: <RCFDCn_base> + $04B0_H$ + (04_H × m),

RCFDCnCFDTMTASTSmLH: <RCFDCn_base> + $04B1_H$ + (04_H × m),

RCFDCnCFDTMTASTSmHL: <RCFDCn_base> + $04B2_H$ + (04_H × m),

RCFDCnCFDTMTASTSmHH: <RCFDCn_base> + $04B3_H$ + (04_H × m)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TMTASTSp (p = m × 32 + 31 to m × 32 × 16 (m = 0 to 7))															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TMTASTSp (p = m × 32 + 15 to m × 32 + 0 (m = 0 to 7))															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 24.102 RCFDCnCFDTMTASTSm Register Contents

Bit Position	Bit Name	Function
31 to 16	TMTASTSp	Transmit Buffer Transmit Abort Status Flag p (p = m × 32 + 31 to m × 32 + 16) 0: Transmission is not aborted 1: Transmission is aborted
15 to 0	TMTASTSp	Transmit Buffer Transmit Abort Status Flag p (p = m × 32 + 15 to m × 32 + 0) 0: Transmission is not aborted. 1: Transmission is aborted.

TMTASTSp Flags (p = 0 to 255)

When the TMTRF[1:0] flag in the RCFDCnCFDTMSTSp register is set to 01_B (transmit abort has been completed), the corresponding TMTASTSp flag is set to 1.

To clear the TMTASTSp flag to 0, set the corresponding TMTRF[1:0] flag to 00_B. This flag is cleared to 0 in channel reset mode.

Table 24.103, TMTASTSp Bit Assignment shows the bit assignment.

Table 24.103 TMTASTSp Bit Assignment

Bit Position	Channel	Transmit Buffer Number
0	0	0
1	0	1
.	.	.
.	.	.
31	0	31
32	1	0
.	.	.
.	.	.
62	1	30
63	1	31
64	2	0
65	2	1
.	.	.
.	.	.
95	2	31
96	3	0
.	.	.
.	.	.
126	3	30
127	3	31
128	4	0
129	4	1
.	.	.
.	.	.
158	4	30
159	4	31
160	5	0
161	5	1
.	.	.
.	.	.
191	5	31
192	6	0
.	.	.
.	.	.
222	6	30
223	6	31
224	7	0
225	7	1
.	.	.
.	.	.
254	7	30
255	7	31

24.3.12 Details of Transmit Queue-related Registers

24.3.12.1 RCFDCnCFDTXQCCm — Transmit Queue Configuration and Control Register (m = 0 to 7)

Access: RCFDCnCFDTXQCCm register can be read or written in 32-bit units

RCFDCnCFDTXQCCmL register can be read or written in 16-bit units

RCFDCnCFDTXQCCmLL, RCFDCnCFDTXQCCmLH registers can be read or written in 8-bit units

Address: RCFDCnCFDTXQCCm: <RCFDCn_base> + 0550_H + (04_H × m)

RCFDCnCFDTXQCCmL: <RCFDCn_base> + 0550_H + (04_H × m)

RCFDCnCFDTXQCCmLL: <RCFDCn_base> + 0550_H + (04_H × m),

RCFDCnCFDTXQCCmLH: <RCFDCn_base> + 0551_H + (04_H × m)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	TXQDC[4:0]					TXQIM	—	TXQTXIE	—	—	—	—	TXQE
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R	R	R	R	R/W

Table 24.104 RCFDCnCFDTXQCCm Register Contents

Bit Position	Bit Name	Function
31 to 13	Reserved	When read, the value after reset is returned. When writing to these bits, write the value after reset.
12 to 8	TXQDC[4:0]	Transmit Queue Depth Configuration Setting these bits to g (g = 2 to 31) makes the (g + 1) transmit queue available. Setting these bits to 0 disables the transmit queue. Setting these bits to 1 is prohibited.
7	TXQIM	Transmit Queue Interrupt Source Select 0: When the transmit queue becomes empty upon completion of message transmission, a transmit queue interrupt request is generated. 1: A transmit queue interrupt request is generated each time a message has been transmitted.
6	Reserved	When read, the value after reset is returned. When writing to these bits, write the value after reset.
5	TXQTXIE	Transmit Queue Interrupt Enable 0: Transmit queue interrupt is disabled. 1: Transmit queue interrupt is enabled.
4 to 1	Reserved	When read, the value after reset is returned. When writing to these bits, write the value after reset.
0	TXQE	Transmit Queue Enable 0: The transmit queue is not used. 1: The transmit queue is used.

TXQDC[4:0] Bits

These bits are used to specify the number of transmit buffers to be allocated to the transmit queues. Transmit buffers are allocated to transmit queues in descending order of buffer number, that is, from (m × 32 + 31) to (m × 32 + 0) (See **Table 24.33, Transmit Buffer p Allocated to the Transmit Queue of Each Channel**). For examples of how buffer allocation is done, see **Figure 24.9, Allocation of Transmit Queues and Transmit/Receive FIFO Buffer Links**.

Modify these bits only in channel reset mode.

TXQIM Bit

This bit is used to select a transmit queue interrupt source. Modify this bit in channel reset mode.

TXQTXIE Bit

When the TXQTXIE bit is set to 1 and the source selected by the TXQIM bit occurs, an interrupt request is generated.

Set the TXQE bit to 0 before modifying the TXQTXIE bit.

TXQE Bit

Setting this bit to 1 enables the transmit queue. Modify this bit in channel communication mode or channel halt mode. This bit is cleared to 0 in channel reset mode.

Before setting the TXQE bit to 1, set the TXQDC[4:0] bits to 00010_B or more.

24.3.12.2 RCFDCnCFDTXQSTSm — Transmit Queue Status Register (m = 0 to 7)

Access: RCFDCnCFDTXQSTSm register can be read or written in 32-bit units
RCFDCnCFDTXQSTSmL register can be read or written in 16-bit units
RCFDCnCFDTXQSTSmLL register can be read or written in 8-bit units

Address: RCFDCnCFDTXQSTSm: <RCFDCn_base> + 0570_H + (04_H × m)
RCFDCnCFDTXQSTSmL: <RCFDCn_base> + 0570_H + (04_H × m)
RCFDCnCFDTXQSTSmLL: <RCFDCn_base> + 0570_H + (04_H × m)

Value after reset: $0000\ 0001_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQTXIF	TXQFLL	TXQEMP
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W*1	R	R

Note 1. The only effective value for writing to this flag bit is 0, which clears the bit. Otherwise writing to the bit results in retention of its state.

Table 24.105 RCFDCnCFDTXQSTSm Register Contents

Bit Position	Bit Name	Function
31 to 14	Reserved	When read, the value after reset is returned. When writing to these bits, write the value after reset.
13 to 8	Reserved	When read, the undefined value is returned. When writing to these bits, write the value after reset.
7 to 3	Reserved	When read, the value after reset is returned. When writing to these bits, write the value after reset.
2	TXQTXIF	Transmit Queue Interrupt Request Flag 0: No transmit queue interrupt request is present. 1: A transmit queue interrupt request is present.
1	TXQFLL	Transmit Queue Full Status Flag 0: The transmit queue is not full. 1: The transmit queue is full.
0	TXQEMP	Transmit Queue Empty Status Flag 0: The transmit queue contains messages. 1: The transmit queue contains no message (transmit queue empty).

TXQTXIF Flag

The TXQTXIF flag is set to 1 when the interrupt source specified by the TXQIM bit in the RCFDCnCFDTXQCCm register has occurred.

The TXQTXIF flag is cleared to 0 in channel reset mode or by writing 0 to this flag. This flag is not cleared to 0 by setting the TXQE bit in the RCFDCnCFDTXQCCm register to 0 (the transmit queue is not used).

TXQFLL Flag

The TXQFLL flag is set to 1 when the number of messages stored in the transmit queue matches the transmit queue depth set by the TXQDC[4:0] bits in the RCFDCnCFDTXQCCm register.

This flag is cleared to 0 in any of the following cases.

- The number of messages set for the transmit queue is smaller than the transmit queue depth set by the TXQDC[4:0] bits.
- In channel reset mode

TXQEMP Flag

The TXQEMP flag is cleared to 0 when even a single message is stored in the transmit queue. This flag is set to 1 in any of the following cases.

- The TXQE bit is set to 0 (the transmit queue is not used).
- The transmit queue becomes empty.
- In channel reset mode

24.3.12.3 RCFDCnCFDTXQPCTRm — Transmit Queue Pointer Control Register (m = 0 to 7)

Access: RCFDCnCFDTXQPCTRm register is a write-only register that can be written in 32-bit units
RCFDCnCFDTXQPCTRmL register is a write-only register that can be written in 16-bit units
RCFDCnCFDTXQPCTRmLL register is a write-only register that can be written in 8-bit units

Address: RCFDCnCFDTXQPCTRm: <RCFDCn_base> + 0590_H + (04_H × m)
RCFDCnCFDTXQPCTRmL: <RCFDCn_base> + 0590_H + (04_H × m)
RCFDCnCFDTXQPCTRmLL: <RCFDCn_base> + 0590_H + (04_H × m)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	TXQPC[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	W	W	W	W	W	W	W	W

Table 24.106 RCFDCnCFDTXQPCTRm Register Contents

Bit Position	Bit Name	Function
31 to 8	Reserved	The write value should be the value after reset.
7 to 0	TXQPC[7:0]	Transmit Queue Pointer Control Writing FF_H to these bits moves the write pointer of the transmit queue to the next queue buffer.

TXQPC[7:0] Bits

Writing FF_H to the TXQPC[7:0] bits moves the write pointer to the next transmit queue buffer and generates a transmit request for the message. Write transmit messages to the RCFDCnCFDTMIDp, RCFDCnCFDTMPTRp, RCFDCnCFDTMFDCTRp, and RCFDCnCFDTMDFb_p registers (p = 31, 63, 95, 127, 159, 191, 223 and 255) before writing FF_H to the TXQPC[7:0] bits.

When writing FF_H to these bits, make sure that the TXQE bit in the RCFDCnCFDTXQCCm register is set to 1 (the transmit queue is used) and the TXQFLL flag in the RCFDCnCFDTXQSTSm register is 0 (he transmit queue is not full).

24.3.13 Details of Transmit History-related Registers

24.3.13.1 RCFDCnCFDTHLCCm — Transmit History Configuration and Control Register (m = 0 to 7)

Access: RCFDCnCFDTHLCCm register can be read or written in 32-bit units

RCFDCnCFDTHLCCmL register can be read or written in 16-bit units

RCFDCnCFDTHLCCmLL, RCFDCnCFDTHLCCmLH registers can be read or written in 8-bit units

Address: RCFDCnCFDTHLCCm: <RCFDCn_base> + $05B0_H$ + (04_H × m)

RCFDCnCFDTHLCCmL: <RCFDCn_base> + $05B0_H$ + (04_H × m)

RCFDCnCFDTHLCCmLL: <RCFDCn_base> + $05B0_H$ + (04_H × m),

RCFDCnCFDTHLCCmLH: <RCFDCn_base> + $05B1_H$ + (04_H × m)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	THLDTE	THLIM	THLIE	—	—	—	—	—	—	—	THLE
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R/W

Table 24.107 RCFDCnCFDTHLCCm Register Contents

Bit Position	Bit Name	Function
31 to 11	Reserved	When read, the value after reset is returned. When writing to these bits, write the value after reset.
10	THLDTE	Transmit History Target Buffer Select 0: Entries from transmit/receive FIFO buffers and transmit queue 1: Entries from transmit buffers, transmit/receive FIFO buffers, and transmit queue
9	THLIM	Transmit History Interrupt Source Select 0: When 24 items of data have been stored in the transmit history buffer 1: Each time transmit history data is stored in the transmit history buffer
8	THLIE	Transmit History Interrupt Enable 0: Transmit history interrupt is disabled. 1: Transmit history interrupt is enabled.
7 to 1	Reserved	When read, the value after reset is returned. When writing to these bits, write the value after reset.
0	THLE	Transmit History Buffer Enable 0: Transmit history buffer is not used. 1: Transmit history buffer is used.

THLDTE Bit

When this bit is set to 0, the transmit history data of messages transmitted from transmit/receive FIFO buffers and the transmit queue is stored in the transmit history buffer. When this bit is set to 1, the transmit history data of messages transmitted from transmit buffers, transmit/receive FIFO buffers, and the transmit queue is stored in the transmit history buffer.

Modify this bit only in channel reset mode.

THLIM Bit

This bit is used to select a transmit history interrupt source. Modify this bit only in channel reset mode.

THLIE Bit

When the THLIE bit is set to 1 and the source selected by the THLIM bit has occurred, a transmit history interrupt request is generated. Modify the THLIE bit only when the THLE bit is set to 0.

THLE Bit

Setting this bit to 1 enables the transmit history buffer. When data transmission from the buffer selected by the THLDTE bit has been completed, the transmit history data of transmit messages is stored in the transmit history buffer.

Modify this bit in channel communication mode or channel halt mode. This bit is cleared to 0 in channel reset mode.

24.3.13.2 RCFDCnCFDTHLSTSm — Transmit History Status Register (m = 0 to 7)

Access: RCFDCnCFDTHLSTSm register can be read or written in 32-bit units

RCFDCnCFDTHLSTSmL register can be read or written in 16-bit units

RCFDCnCFDTHLSTSmLL register can be read or written in 8-bit units

RCFDCnCFDTHLSTSmLH register is a read-only register that can be read in 8-bit units

Address: RCFDCnCFDTHLSTSm: <RCFDCn_base> + $05D0_H$ + (04_H × m)

RCFDCnCFDTHLSTSmL: <RCFDCn_base> + $05D0_H$ + (04_H × m)

RCFDCnCFDTHLSTSmLL: <RCFDCn_base> + $05D0_H$ + (04_H × m),

RCFDCnCFDTHLSTSmLH: <RCFDCn_base> + $05D1_H$ + (04_H × m)

Value after reset: $0000\ 0001_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	THLMC[5:0]						—	—	—	—	THLIF	THLELT	THLFLL	THLEMP
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R/W*1	R/W*1	R	R

Note 1. The only effective value for writing to this flag bit is 0, which clears the bit. Otherwise writing to the bit results in retention of its state.

Table 24.108 RCFDCnCFDTHLSTSm Register Contents

Bit Position	Bit Name	Function
31 to 14	Reserved	When read, the value after reset is returned. When writing to these bits, write the value after reset.
13 to 8	THLMC[5:0]	Transmit History Buffer Unread Data Counter These bits indicate the number of unread data stored in the transmit history buffer.
7 to 4	Reserved	When read, the value after reset is returned. When writing to these bits, write the value after reset.
3	THLIF	Transmit History Interrupt Request Flag 0: No transmit history interrupt request is present. 1: A transmit history interrupt request is present.
2	THLELT	Transmit History Buffer Overflow Flag 0: Transmit history buffer overflow has not occurred. 1: Transmit history buffer overflow has occurred.
1	THLFLL	Transmit history Buffer Full Status Flag 0: Transmit history buffer is not full. 1: Transmit history buffer is full.
0	THLEMP	Transmit History Buffer Empty Status Flag 0: Transmit history buffer contains unread data. 1: Transmit history buffer contains no unread data (buffer empty).

THLMC[5:0] Bits

These bits indicate the number of unread data stored in the transmit history buffer. These bits are cleared to 0 in channel reset mode.

THLIF Flag

The THLIF flag is set to 1 when the interrupt source specified with the THLIM bit in the RCFDCnCFDTHLCCm register occurs.

This flag is cleared to 0 in channel reset mode or by the program writing 0 to this flag.

To clear the flags of the register to 0, the program must write 0 to the corresponding flag to be cleared. When writing 0, using store instruction, set the bit to be set to “0” to “0”, and the bits not to be set to “0” to “1”.

THLELT Flag

The THLELT flag is set to 1 when an attempt is made to store new transmit history data while the transmit history buffer is full. In this case, the new data is discarded. This flag becomes 0 in channel reset mode or by the program writing 0 to this flag.

To clear the flags of the register to 0, the program must write 0 to the corresponding flag to be cleared.

When writing 0, using store instruction, set the bit to be set to “0” to “0”, and the bits not to be set to “0” to “1”.

THLFLL Flag

The THLFLL flag is set to 1 when 32 items of data have been stored in the transmit history buffer, and is cleared to 0 when the number of data stored in the transmit history buffer has decreased to less than 32. This bit is also cleared to 0 in channel reset mode or when the THLE bit in the RCFDCnCFDTHLCCm register is set to 0 (transmit history buffer is not used).

THLEMP Flag

The THLEMP flag is cleared to 0 when even a single item of transmit history data has been stored in the transmit history buffer.

This flag is set to 1 when all the data in the transmit history buffer has been read. This flag is also set to 1 in channel reset mode or when the THLE bit in the RCFDCnCFDTHLCCm register is set to 0 (transmit history buffer is not used).

NOTE

To clear THLIF or THLELT flag to 0, the program must write 0. When writing, use a store instruction to write “0” to the given flag and “1” to other flags.

24.3.13.3 RCFDCnCFDTHLPCTRm — Transmit History Pointer Control Register (m = 0 to 7)

Access: RCFDCnCFDTHLPCTRm register is a write-only register that can be written in 32-bit units
RCFDCnCFDTHLPCTRmL register is a write-only register that can be written in 16-bit units
RCFDCnCFDTHLPCTRmLL register is a write-only register that can be written in 8-bit units

Address: RCFDCnCFDTHLPCTRm: <RCFDCn_base> + $05F0_H$ + (04_H × m)
RCFDCnCFDTHLPCTRmL: <RCFDCn_base> + $05F0_H$ + (04_H × m)
RCFDCnCFDTHLPCTRmLL: <RCFDCn_base> + $05F0_H$ + (04_H × m)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	THLPC[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	W	W	W	W	W	W	W	W

Table 24.109 RCFDCnCFDTHLPCTRm Register Contents

Bit Position	Bit Name	Function
31 to 8	Reserved	When writing to these bits, write the value after reset.
7 to 0	THLPC[7:0]	Transmit History List Pointer Control Writing FF_H to these bits moves the read pointer to the next unread data in the transmit history buffer.

THLPC[7:0] Bits

When the THLPC[7:0] bits are set to FF_H, the read pointer moves to the next data in the transmit history buffer. At this time, the THLMC[5:0] (transmit history buffer unread data counter) value in the RCFDCnCFDTHLSTSm register is decremented by 1. Write FF_H to the THLPC[7:0] bits after reading from the RCFDCnCFDTHLACC0m register and the RCFDCnCFDTHLACC1m register.

When writing FF_H to these bits, make sure that the THLE bit in the RCFDCnCFDTHLCCm register is set to 1 (transmit history buffer is used) and the THLEMP flag in the RCFDCnCFDTHLSTSm register is 0.

24.3.13.4 RCFDCnCFDTHLACC0m — Transmit History Access Register 0 (m = 0 to 7)

Access: RCFDCnCFDTHLACC0m register is a read-only register that can be read in 32-bit units

RCFDCnCFDTHLACC0mL, RCFDCnCFDTHLACC0mH registers are read-only registers that can be read in 16-bit units

RCFDCnCFDTHLACC0mLL, RCFDCnCFDTHLACC0mHL, RCFDCnCFDTHLACC0mHH registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDTHLACC0m: <RCFDCn_base> + 10000_H + (08_H × m)

RCFDCnCFDTHLACC0mL: <RCFDCn_base> + 10000_H + (08_H × m),

RCFDCnCFDTHLACC0mH: <RCFDCn_base> + 10002_H + (08_H × m)

RCFDCnCFDTHLACC0mLL: <RCFDCn_base> + 10000_H + (08_H × m),

RCFDCnCFDTHLACC0mHL: <RCFDCn_base> + 10002_H + (08_H × m),

RCFDCnCFDTHLACC0mHH: <RCFDCn_base> + 10003_H + (08_H × m)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TMTS[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	BN[4:0]					BT[2:0]		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 24.110 RCFDCnCFDTHLACC0m Register Contents

Bit Position	Bit Name	Function
31 to 16	TMTS[15:0]	Timestamp Data The timestamp data of stored data can be read.
15 to 8	Reserved	When read, the value after reset is returned.
7 to 3	BN[4:0]	Buffer Number Data The buffer number of transmit source (transmit buffer, transmit/receive FIFO or transmit queue) can be read.
2 to 0	BT[2:0]	Buffer Type Data b2 b1 b0 0 0 1: Transmit buffer 0 1 0: Transmit/receive FIFO buffer 1 0 0: Transmit queue

TMTS[15:0] Bits

Timestamp values in transmit history data stored in the transmit history buffer are displayed.

BN[4:0] Bits

These bits indicate the transmit source buffer number in the transmit history data stored in the transmit history buffer.

BT[2:0] Bits

These bits indicate the type of the transmit source buffer in the transmit history data stored in the transmit history buffer.

24.3.13.5 RCFDCnCFDTHLACC1m — Transmit History Access Register 1 (m = 0 to 7)

Access: RCFDCnCFDTHLACC1m register is a read-only register that can be read in 32-bit units

RCFDCnCFDTHLACC1mL register is a read-only register that can be read in 16-bit units

RCFDCnCFDTHLACC1mLL, RCFDCnCFDTHLACC1mLH registers are read-only registers that can be read in 8-bit units

Address: RCFDCnCFDTHLACC1m: <RCFDCn_base> + 10004_H + (08_H × m)

RCFDCnCFDTHLACC1mL: <RCFDCn_base> + 10004_H + (08_H × m)

RCFDCnCFDTHLACC1mLL: <RCFDCn_base> + 10004_H + (08_H × m),

RCFDCnCFDTHLACC1mLH: <RCFDCn_base> +10005_H + (08_H × m)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TID[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 24.111 RCFDCnCFDTHLACC1m Register Contents

Bit Position	Bit Name	Function
31 to 16	Reserved	These bits are read as the value after reset.
15 to 0	TID[15:0]	Label Data The label information of stored data can be read.

TID[15:0] Bits

These bits indicate the label information of transmit history data stored in the transmit history buffer.

24.3.14 Details of Test-related Registers

24.3.14.1 RCFDCnCFDGTSTCFG — Global Test Configuration Register

Access: RCFDCnCFDGTSTCFG register can be read or written in 32-bit units

RCFDCnCFDGTSTCFGL, RCFDCnCFDGTSTCFGH registers can be read or written in 16-bit units

RCFDCnCFDGTSTCFGLL, RCFDCnCFDGTSTCFGHL, RCFDCnCFDGTSTCFGHH registers can be read or written in 8-bit units

Address: RCFDCnCFDGTSTCFG: <RCFDCn_base> + 0618_H

RCFDCnCFDGTSTCFGL: <RCFDCn_base> + 0618_H,

RCFDCnCFDGTSTCFGH: <RCFDCn_base> + $061A_H$

RCFDCnCFDGTSTCFGLL: <RCFDCn_base> + 0618_H,

RCFDCnCFDGTSTCFGHL: <RCFDCn_base> + $061A_H$,

RCFDCnCFDGTSTCFGHH: <RCFDCn_base> + $061B_H$

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	RTMPS[8:0]								
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	C7ICBCE	C6ICBCE	C5ICBCE	C4ICBCE	C3ICBCE	C2ICBCE	C1ICBCE	C0ICBCE
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 24.112 RCFDCnCFDGTSTCFG Register Contents

Bit Position	Bit Name	Function
31 to 25	Reserved	When read, the value after reset is returned. When writing to these bits, write the value after reset.
24 to 16	RTMPS[8:0]	RAM Test Page Configuration Set a value within a range of page 0 to page 33 × (m + 1).
15 to 8	Reserved	When read, the value after reset is returned. When writing to these bits, write the value after reset.
7	C7ICBCE	CAN7 Inter-channel Communication Test Enable 0: CAN7 inter-channel communication test is disabled. 1: CAN7 inter-channel communication test is enabled.
6	C6ICBCE	CAN6 Inter-channel Communication Test Enable 0: CAN6 inter-channel communication test is disabled. 1: CAN6 inter-channel communication test is enabled.
5	C5ICBCE	CAN5 Inter-channel Communication Test Enable 0: CAN5 inter-channel communication test is disabled. 1: CAN5 inter-channel communication test is enabled.
4	C4ICBCE	CAN4 Inter-channel Communication Test Enable 0: CAN4 inter-channel communication test is disabled. 1: CAN4 inter-channel communication test is enabled.

Table 24.112 RCFDCnCFDGTSTCFG Register Contents

Bit Position	Bit Name	Function
3	C3ICBCE	CAN3 Inter-channel Communication Test Enable 0: CAN3 inter-channel communication test is disabled. 1: CAN3 inter-channel communication test is enabled.
2	C2ICBCE	CAN2 Inter-channel Communication Test Enable 0: CAN2 inter-channel communication test is disabled. 1: CAN2 inter-channel communication test is enabled.
1	C1ICBCE	CAN1 Inter-channel Communication Test Enable 0: CAN1 inter-channel communication test is disabled. 1: CAN1 inter-channel communication test is enabled.
0	C0ICBCE	CAN0 Inter-channel Communication Test Enable 0: CAN0 inter-channel communication test is disabled. 1: CAN0 inter-channel communication test is enabled.

Modify the RCFDCnCFDGTSTCFG register only in global test mode.

RTMPS[8:0] Bits

- RCFDC0 with 8 channels

  These bits are used to set the RAM test target page number for RAM test. Set a value in the range of 00_H to 108_H, inclusive.

- RCFDC0 with 6 channels

  These bits are used to set the RAM test target page number for RAM test. Set a value in the range of 00_H to $C6_H$, inclusive. Should not access more than 192 Bytes in the last page.

- RCFDC1 with 4 channels

  These bits are used to set the RAM test target page number for RAM test. Set a value in the range of 00_H to 84_H, inclusive. Should not access more than 128 Bytes in the last page.

C7ICBCE Bit

Setting this bit to 1 enables the channel 7 inter-channel communication test. This bit is cleared to 0 in global reset mode.

C6ICBCE Bit

Setting this bit to 1 enables the channel 6 inter-channel communication test. This bit is cleared to 0 in global reset mode.

C5ICBCE Bit

Setting this bit to 1 enables the channel 5 inter-channel communication test. This bit is cleared to 0 in global reset mode.

C4ICBCE Bit

Setting this bit to 1 enables the channel 4 inter-channel communication test. This bit is cleared to 0 in global reset mode.

C3ICBCE Bit

Setting this bit to 1 enables the channel 3 inter-channel communication test. This bit is cleared to 0 in global reset mode.

C2ICBCE Bit

Setting this bit to 1 enables the channel 2 inter-channel communication test. This bit is cleared to 0 in global reset mode.

C1ICBCE Bit

Setting this bit to 1 enables the channel 1 inter-channel communication test. This bit is cleared to 0 in global reset mode.

C0ICBCE Bit

Setting this bit to 1 enables the channel 0 inter-channel communication test. This bit is cleared to 0 in global reset mode.

24.3.14.2 RCFDCnCFDGTSTCTR — Global Test Control Register

Access: RCFDCnCFDGTSTCTR register can be read or written in 32-bit units
RCFDCnCFDGTSTCTRL register can be read or written in 16-bit units
RCFDCnCFDGTSTCTRLL register can be read or written in 8-bit units

Address: RCFDCnCFDGTSTCTR: <RCFDCn_base> + $061C_H$
RCFDCnCFDGTSTCTRL: <RCFDCn_base> + $061C_H$
RCFDCnCFDGTSTCTRLL: <RCFDCn_base> + $061C_H$

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	RTME	—	ICBCTME
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W

Table 24.113 RCFDCnCFDGTSTCTR Register Contents

Bit Position	Bit Name	Function
31 to 3	Reserved	When read, the value after reset is returned. When writing to these bits, write the value after reset.
2	RTME	RAM Test Enable 0: RAM test is disabled. 1: RAM test is enabled.
1	Reserved	When read, the value after reset is returned. When writing to these bits, write the value after reset.
0	ICBCTME	Inter-channel Communication Test Enable 0: Inter-channel communication test is disabled 1: Inter-channel communication test is enabled

RTME Bit

Setting this bit to 1 enables the RAM test. Modify this bit only in global test mode.

This bit is cleared to 0 in global reset mode (See **Figure 24.37, RAM Test Setting Procedure**).

1. Set the GMDC[1:0] bits in the RCFDCnCFDGCTR register to 10_B (Global test mode).
2. Set the RTME bit to 1.
3. Check that the RTME bit is set to 1.

ICBCTME Bit

When this bit is set to 1, a communication test is enabled between the channels for which the CmICBCE bit (m = 0 to 7) in the RCFDCnCFDGTSTCFG register has been set to 1. Modify the ICBCTME bit only in global test mode.

This bit is cleared to 0 in global reset mode.

24.3.14.3 RCFDCnCFDGLOCKK — Global Lock Key Register

Access: RCFDCnCFDGLOCKK register is a write-only register that can be written in 32-bit units.
RCFDCnCFDGLOCKKL register is a write-only register that can be written in 16-bit units.

Address: RCFDCnCFDGLOCKK: <RCFDCn_base> + $062C_H$
RCFDCnCFDGLOCKKL: <RCFDCn_base> + $062C_H$

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LOCK[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	W*1	W*1	W*1	W*1	W*1	W*1	W*1	W*1	W*1	W*1	W*1	W*1	W*1	W*1	W*1	W*1

Note 1. Writing to these bits is effective only when the RS-CANFD module is in global test mode.

Table 24.114 RCFDCnCFDGLOCKK Register Contents

Bit Position	Bit Name	Function
31 to 16	Reserved	When writing these bits, write the value after reset.
15 to 0	LOCK[15:0]	Lock Key These bits are key bits to release protection of test mode.

The RCFDCnCFDGLOCKK register releases protection of special test bits and is write only.

For the protection release data, see **Section 24.10.4.2, Procedure for Releasing the Protection**.

LOCK[15:0] Bits

Writing the protection release data to the LOCK[15:0] bits in succession enables writing 1 to the RTME bit in the RCFDCnCFDGTSTCTR register.

After the protection has been released, writing to the I/O register area (<RCFDCn_base> + 0000_H to <RCFDCn_base> + $07FF_H$) of the CAN (except the RAM) enables the protection again.

Reading from the I/O register area of the CAN or reading from/writing to other areas does not enable the protection.

24.3.14.4 RCFDCnCFDRPGACCr — RAM Test Page Access Register (r = 0 to 63)

Access: RCFDCnCFDRPGACCr register can be read or written in 32-bit units

RCFDCnCFDRPGACCrL, RCFDCnCFDRPGACCrH registers can be read or written in 16-bit units

RCFDCnCFDRPGACCrLL, RCFDCnCFDRPGACCrLH, RCFDCnCFDRPGACCrHL, RCFDCnCFDRPGACCrHH registers can be read or written in 8-bit units

Address: RCFDCnCFDRPGACCr: <RCFDCn_base> + 10400_H + (04_H × r)

RCFDCnCFDRPGACCrL: <RCFDCn_base> + 10400_H + (04_H × r),

RCFDCnCFDRPGACCrH: <RCFDCn_base> + 10402_H + (04_H × r)

RCFDCnCFDRPGACCrLL: <RCFDCn_base> + 10400_H + (04_H × r),

RCFDCnCFDRPGACCrLH: <RCFDCn_base> + 10401_H + (04_H × r),

RCFDCnCFDRPGACCrHL: <RCFDCn_base> + 10402_H + (04_H × r),

RCFDCnCFDRPGACCrHH: <RCFDCn_base> + 10403_H + (04_H × r)

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RDTA[31:16]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDTA[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 24.115 RCFDCnCFDRPGACCr Register Contents

Bit Position	Bit Name	Function
31 to 0	RDTA[31:0]	RAM Data Test Access RAM data for CAN can be read and written.

Modify the RCFDCnCFDRPGACCr register in global test mode with the RTME bit in the RCFDCnCFDGTSTCTR register set to 1 (RAM test is enabled).

The RCFDCnCFDRPGACCr register can be read and written when the RTME bit is set to 1.

24.4 Interrupt Sources and DMA Trigger

24.4.1 Interrupt Sources

The RS-CANFD module has 26 interrupts for unit 0 and 14 interrupts for unit 1 are grouped into global interrupts and channel interrupts.

- Global interrupts (2 sources/unit): Receive FIFO interrupt Global error interrupt
- Channel interrupts (3 sources/channel): (m = 0 to 7 (n = 0), m = 0 to 3 (n = 1))

1. CANm transmit interrupt
   - CANm transmit complete interrupt
   - CANm transmit abort interrupt
   - CANm transmit/receive FIFO transmit complete interrupt (in transmit mode, gateway mode)
   - CANm transmit history interrupt
   - CANm transmit queue Interrupt
2. CANm transmit/receive FIFO receive complete interrupt (in receive mode, gateway mode)
3. CANm error interrupt

CANm transmit/receive FIFO receive complete interrupt (in receive mode, gateway mode) CANm error interrupt

When an interrupt request is generated, the corresponding interrupt request flag is set to 1 (interrupt request present). In this case, when the interrupt enable bit is set to 1 (enabling interrupts), an interrupt request is output from the RS-CANFD module. (Generation of interrupts also depends on the interrupt control register settings of the interrupt controller.)

Setting the interrupt request flag to 0 (no interrupt request present) or setting the interrupt enable bit to 0 (disabling interrupts) clears the current interrupt request. The current interrupt request is still output until the interrupt request flag is cleared.

Table 24.116, List of CAN Interrupt Sources lists the CAN interrupt sources. **Figure 24.2, CAN Global Interrupt Block Diagram** shows the CAN global interrupt block diagram. **Figure 24.3, CAN Channel Interrupt Block Diagram** shows the CAN channel interrupt block diagram.

Table 24.116 List of CAN Interrupt Sources

	Interrupt Source		Corresponding Interrupt Request Flag	Corresponding Interrupt Enable Bit
Global interrupts	Receive FIFO	Receive FIFO 0	RFIF in the RCFDCnCFDRFSTS0 register	RFIE in the RCFDCnCFDRFCC0 register
		Receive FIFO 1	RFIF in the RCFDCnCFDRFSTS1 register	RFIE in the RCFDCnCFDRFCC1 register
		Receive FIFO 2	RFIF in the RCFDCnCFDRFSTS2 register	RFIE in the RCFDCnCFDRFCC2 register
		Receive FIFO 3	RFIF in the RCFDCnCFDRFSTS3 register	RFIE in the RCFDCnCFDRFCC3 register
		Receive FIFO 4	RFIF in the RCFDCnCFDRFSTS4 register	RFIE in the RCFDCnCFDRFCC4 register
		Receive FIFO 5	RFIF in the RCFDCnCFDRFSTS5 register	RFIE in the RCFDCnCFDRFCC5 register
		Receive FIFO 6	RFIF in the RCFDCnCFDRFSTS6 register	RFIE in the RCFDCnCFDRFCC6 register
		Receive FIFO 7	RFIF in the RCFDCnCFDRFSTS7 register	RFIE in the RCFDCnCFDRFCC7 register
	Global error		DEF in the RCFDCnCFDGERFL register	DEIE in the RCFDCnCFDGCTR register
			MES in the RCFDCnCFDGERFL register	MEIE in the RCFDCnCFDGCTR register
			THLES in the RCFDCnCFDGERFL register	THLEIE in the RCFDCnCFDGCTR register
			CMPOF in the RCFDCnCFDGERFL register	CMPOFIE in the RCFDCnCFDGCTR register
Channel interrupts (m = 0 to 7 (n = 0), m = 0 to 3 (n = 1))	CANm transmit	CANm transmit complete	TMTRF[1:0] in the RCFDCnCFDTMSTSp register	TMIEp in the RCFDCnCFDTMIECm register
		CANm transmit abort	TMTRF[1:0] in the RCFDCnCFDTMSTSp register	TAIE in the RCFDCnCFDCmCTR register
		CANm transmit/ receive FIFO transmit complete	CFTXIF in the RCFDCnCFDCFSTSk register	CFTXIE in the RCFDCnCFDCFCCk register
		CANm transmit queue	TXQTXIF in the RCFDCnCFDTXQSTSm register	TXQTXIE in the RCFDCnCFDTXQCCm register
		CANm transmit history	THLIF in the RCFDCnCFDTHLSTSm register	THLIE in the RCFDCnCFDTHLCCm register
	CANm transmit/receive FIFO receive complete		CFRXIF in the RCFDCnCFDCFSTSk register	CFRXIE in the RCFDCnCFDCFCCk register
	CANm error		BEF in the RCFDCnCFDCmERFL register	BEIE in the RCFDCnCFDCmCTR register
			ALF in the RCFDCnCFDCmERFL register	ALIE in the RCFDCnCFDCmCTR register
			BLF in the RCFDCnCFDCmERFL register	BLIE in the RCFDCnCFDCmCTR register
			OVLF in the RCFDCnCFDCmERFL register	OLIE in the RCFDCnCFDCmCTR register
			BORF in the RCFDCnCFDCmERFL register	BORIE in the RCFDCnCFDCmCTR register
			BOEF in the RCFDCnCFDCmERFL register	BOEIE in the RCFDCnCFDCmCTR register
			EPF in the RCFDCnCFDCmERFL register	EPIE in the RCFDCnCFDCmCTR register
			EWF in the RCFDCnCFDCmERFL register	EWIE in the RCFDCnCFDCmCTR register
			SOCO in the RCFDCnCFDCmFDSTS register	SOCOIE in the RCFDCnCFDCmCTR register
			EOCO in the RCFDCnCFDCmFDSTS register	EOCOIE in the RCFDCnCFDCmCTR register
			TDCVF in the RCFDCnCFDCmFDSTS register	TDCVFIE in the RCFDCnCFDCmCTR register

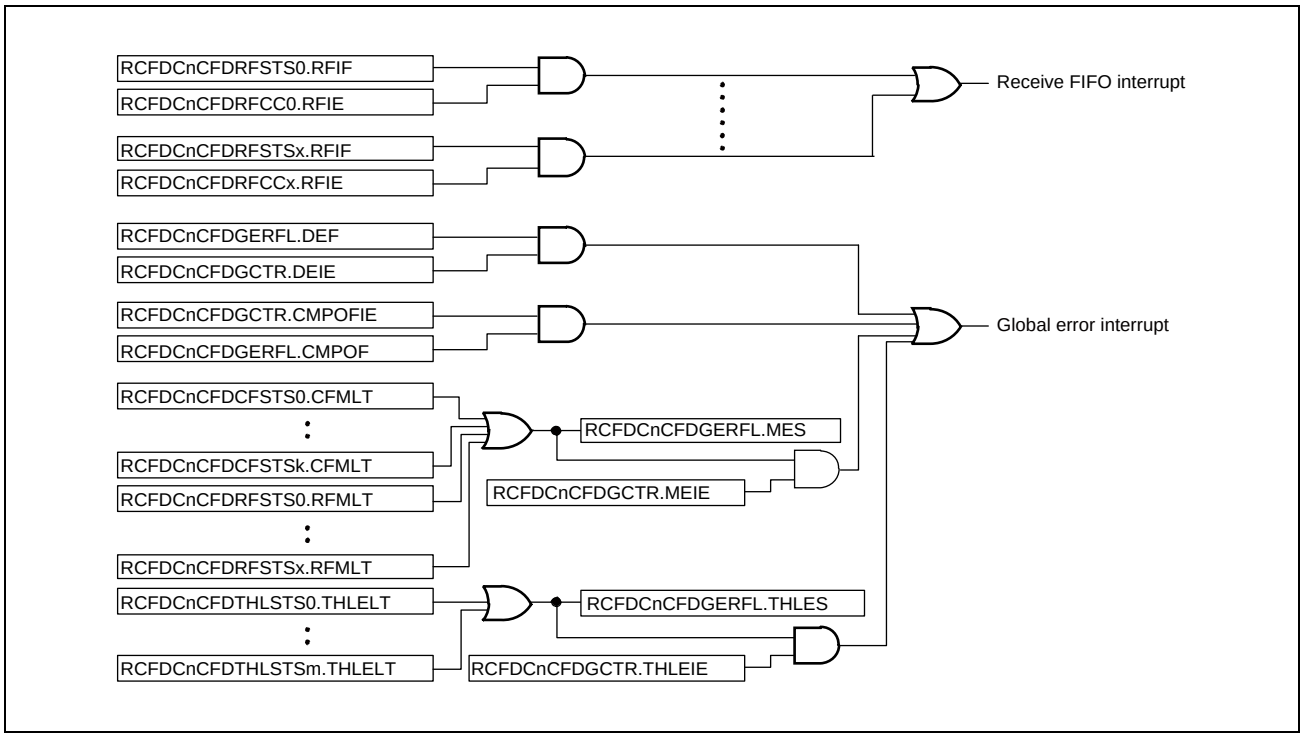


Figure 24.2 CAN Global Interrupt Block Diagram

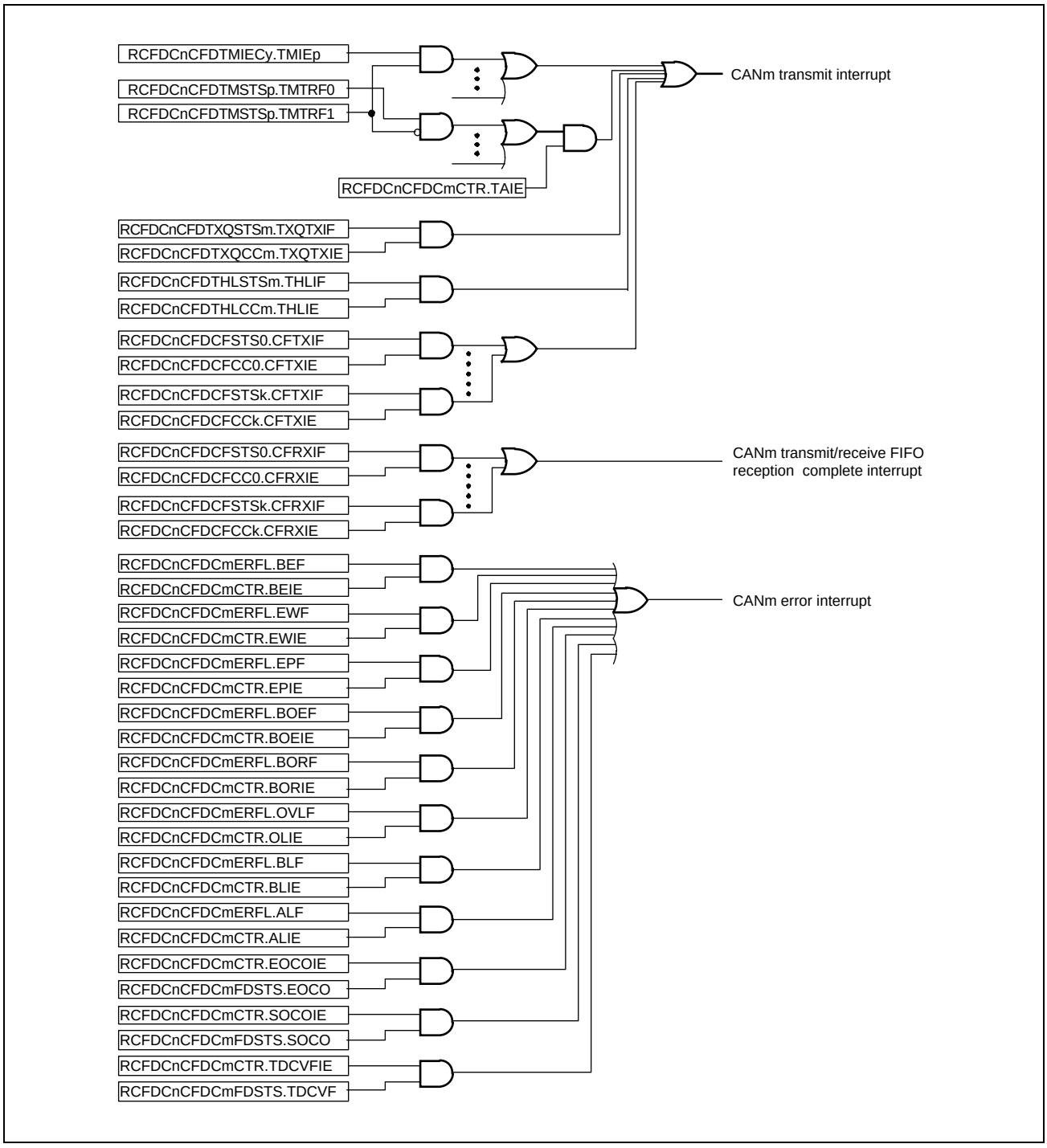


Figure 24.3 CAN Channel Interrupt Block Diagram

24.4.2 DMA Trigger

FIFO buffers used for reception can be related to DMA channels. The following 16 FIFO buffers can be related.

- All receive FIFO buffers x (x = 0 to 7)
- The first transmit/receive FIFO buffer k (k = 3 × m, m = 0 to 7) allocated to channel m

When the DMA enable bit (RFDMAEx or CFDMAEm bit in the RCFDCnCFDCDTCT register) is set to 1 and an unread message is remaining in the related FIFO, a DMA transfer request trigger is generated.

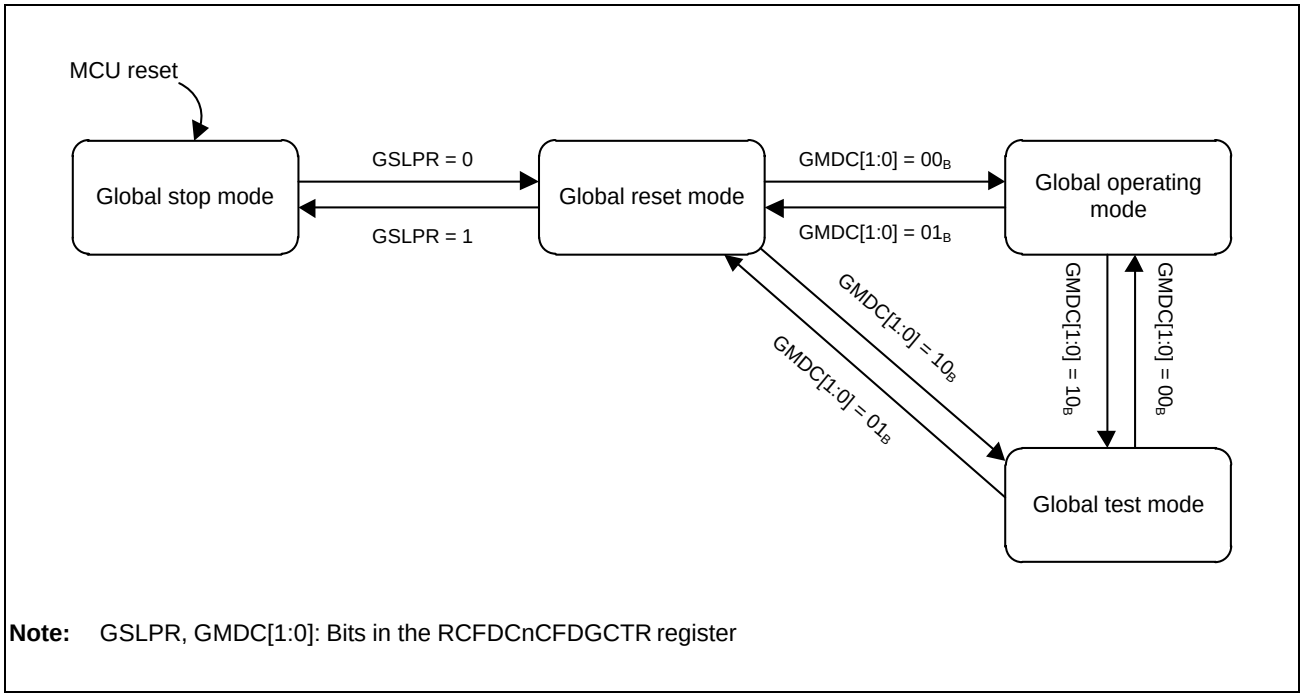
24.5 CAN Modes

The RS-CANFD module has four global modes to control the entire RS-CANFD module status and four channel modes to control individual channel status. Details of global modes are described in **Section 24.5.1, Global Modes**, and details of channel modes are described in **Section 24.5.2, Channel Modes**.

- Global stop mode: Stops the clocks of the entire module to achieve low power consumption.
- Global reset mode: Performs initial settings for the entire module.
- Global test mode: Performs test settings and performs the RAM test.
- Global operating mode: Makes the entire module operable.
- Channel stop mode: Stops the channel clock.
- Channel reset mode: Performs initial settings for the channels.
- Channel halt mode: Stops CAN communication and allows channel testing.
- Channel communication mode: Performs CAN communication.

24.5.1 Global Modes

Figure 24.4, Transitions of Global Modes shows the transitions of global modes.



Note: GSLPR, GMDC[1:0]: Bits in the RCFDCnCFDGCTR register

Figure 24.4 Transitions of Global Modes

In some cases, global mode transitions also force channel mode transitions. **Table 24.117, Transitions of Channel Modes Depending on Global Mode Setting (GMDC[1:0] and GSLPR Bits)** shows the channel mode transitions depending on the global mode setting dictated by the GMDC[1:0] bits and the GSLPR bit.

Table 24.117 Transitions of Channel Modes Depending on Global Mode Setting (GMDC[1:0] and GSLPR Bits)

	Channel Mode after Setting			
Channel Mode before Setting	GMDC[1:0] = 00_B GSLPR = 0 (Global Operation)	GMDC[1:0] = 10_B GSLPR = 0 (Global Test)	GMDC[1:0] = 01_B GSLPR = 0 (Global Reset)	GMDC[1:0] = 01_B GSLPR = 1 (Global Stop)
Channel communication	Channel communication	Channel halt	Channel reset	Transition prohibited
Channel halt	Channel halt	Channel halt	Channel reset	Transition prohibited
Channel reset	Channel reset	Channel reset	Channel reset	Channel stop
Channel stop	Channel stop	Channel stop	Channel stop	Channel stop

Note: GMDC[1:0], GSLPR: Bits in the RCFDCnCFDGCTR register

Table 24.118, Global Mode Transition Time shows the global mode transition time.

Table 24.118 Global Mode Transition Time

Mode before Transition	Mode after Transition	Maximum Transition Time
Global stop	Global reset	Three pclk cycles
Global reset	Global stop	Three pclk cycles
Global reset	Global test	Ten pclk cycles
Global reset	Global operating	Ten pclk cycles
Global test	Global reset	Two CAN bit times*1,*2
Global test	Global operating	Three pclk cycles
Global operating	Global reset	Two CAN bit times*1,*2
Global operating	Global test	Three CAN frames*1

Note 1. CAN frame time and CAN bit time of the lowest communication speed of the channels in use

Note 2. This time value is the CAN bit time of the nominal bit rate.

24.5.1.1 Global Stop Mode

In global stop mode, clocks of the CAN do not run and therefore power consumption is reduced. CAN registers can be read, but writing data to them is prohibited. Register values are retained. Only the clock used by the CPU for writing to the GSLPR bit runs in this mode.

After the MCU is reset, the CAN module transitions to global stop mode. Setting the GSLPR bit in the RCFDCnCFDGCTR register to 1 (in global stop mode) in global reset mode sets the CSLPR bit in each RCFDCnCFDCmCTR register to 1 (channel stop mode). Afterwards, if all channels are forced to transition to channel stop mode, the CAN module transitions to global stop mode. The GSLPR bit should not be modified in global operating mode or global test mode.

24.5.1.2 Global Reset Mode

In global reset mode, RS-CANFD module settings are performed. When the RS-CANFD module transitions to global reset mode, some registers are initialized. For registers to be initialized, see **Table 24.121, Registers Initialized in Global Reset Mode or Channel Reset Mode** and **Table 24.122, Registers Initialized Only in Global Reset Mode**.

Setting the GMDC[1:0] bits in the RCFDCnCFDGCTR register to 01_B sets the CHMDC[1:0] bits in each RCFDCnCFDCmCTR registers (m = 0 to 7) to 01_B (channel reset mode). If all channels are forced to transition to channel reset mode, the CAN module transitions to global reset mode.

Channels that are already in channel reset mode or channel stop mode do not transition (because the CHMDC[1:0] bits have already been set to 01_B).

24.5.1.3 Global Test Mode

In global test mode, settings for test-related registers are performed. When the CAN module transitions to global test mode, all CAN communications are disabled.

Setting the GMDC[1:0] bits in the RCFDCnCFDGCTR register to 10_B sets the CHMDC[1:0] bits in each RCFDCnCFDCmCTR register to 10_B (channel halt mode). If all channels are forced to transition to channel halt mode, the CAN module transitions to global test mode. Channels that are in channel stop mode, channel reset mode, or channel halt mode do not transition.

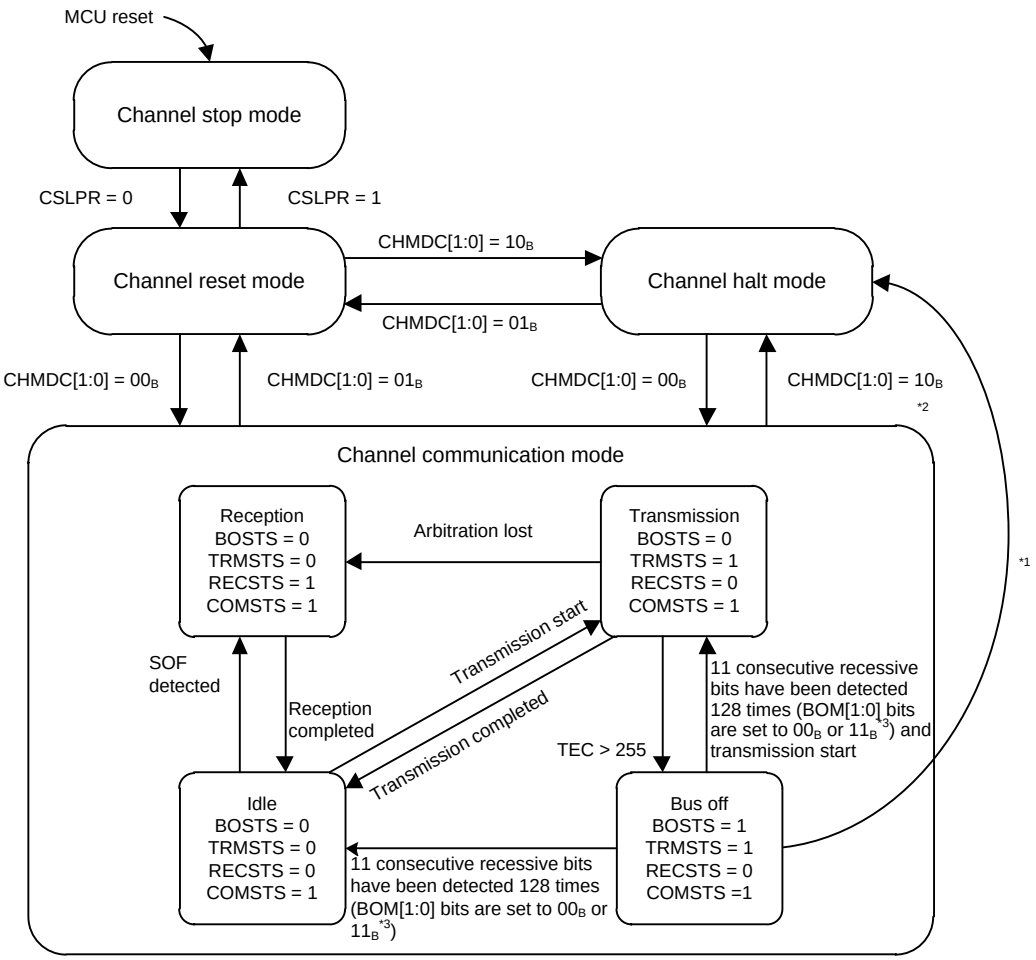
24.5.1.4 Global Operating Mode

The RS-CANFD module operates in global operating mode.

When the GMDC[1:0] bits in the RCFDCnCFDGCTR register are set to 00_B, the RS-CANFD module transitions to global operating mode.

24.5.2 Channel Modes

Figure 24.5, Channel Mode State Transition Chart shows a channel mode state transition chart. **Table 24.119, Channel Mode Transition Time** shows the channel mode transition time.



Note: CHMDC[1:0], CSLPR, BOM[1:0]: Bits in the RCFDCnCFDCmCTR register (m = 0 to 7) BOSTS, TRMSTS, RECSTS, COMSTS: Bits in the RCFDCnCFDCmSTS register

Note 1. Timing of transition from bus off state to channel halt mode
- When BOM[1:0] = 01_B: Transition to channel halt mode when TEC exceeds 255
- When BOM[1:0] = 10_B: Transition to channel halt mode when 11 consecutive recessive bits have been detected 128 times
- When BOM[1:0] = 11_B: Transition to channel halt mode when the CHMDC[1:0] bits are set to 10_B

Note 2. While the CAN bus is locked at the dominant level, transition to channel halt mode is not made. In that case, enter channel reset mode.

Note 3. When 11 consecutive recessive bits are detected 128 times before the CHMDC[1:0] bits are set to 10_B.

Figure 24.5 Channel Mode State Transition Chart

Table 24.119 Channel Mode Transition Time

Mode before Transition	Mode after Transition	Maximum Transition Time
Channel stop	Channel reset	Three pclk cycles
Channel reset	Channel stop	Three pclk cycles
Channel reset	Channel halt	Three CANm bit times*1
Channel reset	Channel communication	Four CANm bit times*1
Channel halt	Channel reset	Two CANm bit times*1
Channel halt	Channel communication	Four CANm bit times*1
Channel communication	Channel reset	Two CANm bit times*1
Channel communication	Channel halt	Two CANm frames

Note 1. This time value is the CANm bit time of the nominal bit rate.

24.5.2.1 Channel Stop Mode

In channel stop mode, clocks are not supplied to channels and therefore power consumption is reduced. Channel-related registers can be read, but writing data to them is prohibited (except write to CSLPR bit). Register values are retained.

Each channel enters channel stop mode after the MCU is reset. Channels also transition to channel stop mode when the CSLPR bit in the RCFDCnCFDCmCTR register (m = 0 to 7) is set to 1 (channel stop mode) in channel reset mode. The CSLPR bit should not be modified in channel communication mode and channel halt mode.

24.5.2.2 Channel Reset Mode

In channel reset mode, channel settings are performed. When a channel transitions to channel reset mode, some channel-related registers are initialized. For registers to be initialized, see **Table 24.121, Registers Initialized in Global Reset Mode or Channel Reset Mode**.

When the CHMDC[1:0] bits in the RCFDCnCFDCmCTR register are set to 01_B (channel reset mode) during CAN communication, communication is terminated before it is completed and the channel transitions to channel reset mode. **Table 24.120, Operation when a Channel Transitions to Channel Reset Mode/Channel Halt Mode** shows the operation when the CHMDC[1:0] bits are set to 01_B (channel reset mode) during CAN communication.

24.5.2.3 Channel Halt Mode

In channel halt mode, settings for test-related registers of channels are performed. When a channel transitions to channel halt mode, CAN communication of the channel stops.

Table 24.120, Operation when a Channel Transitions to Channel Reset Mode/Channel Halt Mode shows operation when the CHMDC[1:0] bits are set to 10_B (channel halt mode) during CAN communication.

Table 24.120 Operation when a Channel Transitions to Channel Reset Mode/Channel Halt Mode

Mode	During Reception	During Transmission	Bus Off State
Channel reset (CHMDC[1:0] = 01_B)	Transitions to channel reset mode before reception is completed.*1	Transitions to channel reset mode before transmission is completed.*1	Transitions to channel reset mode before bus off recovery.
Channel halt*3 (CHMDC[1:0] = 10_B)	Transitions to channel halt mode after reception is completed.*2	Transitions to channel halt mode after transmission is completed.	[When BOM[1:0] = 00_B] Transitions to channel halt mode (CHMDC[1:0] = 10_B) only after bus off recovery. [When BOM[1:0] = 01_B] Transitions to channel halt mode automatically when the condition for transition to bus off state is met. [When BOM[1:0] = 10_B] Transitions to channel halt mode automatically after bus off recovery. [When BOM[1:0] = 11_B] Transitions to channel halt mode immediately after the CHMDC[1:0] bits are set to 10_B before bus off recovery.

Note 1. To allow transition to channel reset mode after communication is completed, set the CHMDC[1:0] bits to 10_B and confirm that communication has been completed and transition to channel halt mode has been made, and then set the CHMDC[1:0] bits to 01_B.

Note 2. While the CAN bus is locked at the dominant level, transition to channel halt mode is not made. In that case, enter channel reset mode. The CAN bus status can be confirmed with the BLF flag of the RCFDCnCFDCmERFL register that becomes 1 when dominant lock is detected.

Note 3. When the transition from channel reset mode to channel halt mode is to be made, set the RCFDCnCFDCmNCFG register and the RCFDCnCFDCmDCFG register, and then make a transition.

24.5.2.4 Channel Communication Mode

In channel communication mode, CAN communication is performed. Each channel has the following communication states during CAN communication.

- Idle: Neither reception nor transmission is in progress.
- Reception: Receiving a message sent from another node.
- Transmission: Transmitting a message.
- Bus off: Isolated from CAN communication.

When the CHMDC[1:0] bits in the RCFDCnCFDCmCTR register are set to 00_B, the channel transitions to channel communication mode. After that, once 11 consecutive recessive bits have been detected, the COMSTS flag in the RCFDCnCFDCmSTS register (m = 0 to 7) is set to 1

(communication is ready) and transmission and reception are enabled on the CAN network as an active node. At this time, transmission and reception of messages can be started.

24.5.2.5 Bus Off State

A channel transitions to the bus off state according to the transmit/receive error counter increment/decrement rules of the CAN specifications.

The conditions for returning from the bus off state are determined by the BOM[1:0] bits in the RCFDCnCFDCmCTR register.

- When BOM[1:0] = 00_B:

  Bus off recovery is compliant with the CAN specifications. After 11 consecutive recessive bits have been detected 128 times, a channel returns from the bus off state to the CAN communication ready state (error active state). At that time, the TEC[7:0] and REC[7:0] bits in the RCFDCnCFDCmSTS register are initialized to 00_H, the BORF flag in the

  RCFDCnCFDCmERFL register is set to 1 (bus off recovery is detected), and a bus off recovery interrupt request is generated. When the CHMDC[1:0] bits in the RCFDCnCFDCmCTR register are set to 10_B (channel halt mode) in the bus off state, the channel transitions to channel halt mode after bus off recovery has been completed (11 consecutive recessive bits have been detected 128 times).

- When BOM[1:0] = 01_B:

  When a channel transitions to the bus off state, the CHMDC[1:0] bits are set to 10_B and the channel transitions to channel halt mode. At that time, the TEC[7:0] and REC[7:0] bits are initialized to 00_H. The BORF flag is not set to 1, and bus off recovery interrupt request is not generated.

- When BOM[1:0] = 10_B:

  When a channel has transitioned to the bus off state, the CHMDC[1:0] bits are set to 10_B. After bus off recovery has been completed (11 consecutive recessive bits have been detected 128 times), the channel transitions to channel halt mode. At that time, the TEC[7:0] and REC[7:0] bits are initialized to 00_H, the BORF flag is set to 1, and a bus off recovery interrupt request is generated.

- When BOM[1:0] = 11_B:

  When the CHMDC[1:0] bits are set to 10_B in the bus off state, the channel transitions to channel halt mode before bus off recovery is completed. At that time, the TEC[7:0] and REC[7:0] bits are initialized to 00_H, but the BORF flag is not set to 1. Also, a bus off recovery interrupt is not generated.

  However, the BORF flag becomes 1 and a bus off recovery interrupt request is generated if a CAN module transitions to error active state (by detecting 11 consecutive recessive bits 128 times) before CHMDC[1:0] bits are set to 10_B.

If the RS-CANFD module causes the channel to transition to channel halt mode simultaneously with a program write to the CHMDC[1:0] bits, the program write takes precedence. An automatic transition to channel halt mode when the BOM[1:0] bits are set to 01_B or 10_B is made only when the CHMDC[1:0] bits are 00_B (channel communication mode).

Furthermore, setting the RTBO bit in the RCFDCnCFDCmCTR register to 1 allows a forced return from the bus off state. As soon as the RTBO bit is set to 1, the state changes to the error active state. After 11 consecutive recessive bits have been detected, the CAN module becomes ready for communication. In this case, the BORF flag is not set to 1 and the TEC[7:0] and REC[7:0] bits are initialized to 00_H. Write 1 to the RTBO bit only when the BOM[1:0] value is 00_B. Writing 1 to the RTBO bit in a state other than the bus off state is ignored, and the RTBO bit is immediately set to 0.

24.5.3 Initializing Registers by Transition to CAN Mode

Table 24.121, Registers Initialized in Global Reset Mode or Channel Reset Mode lists bits and flags to be initialized by a transition to channel reset mode. These bits and flags are also initialized by a transition to global reset mode. Furthermore, **Table 24.122, Registers Initialized Only in Global Reset Mode** lists bits and flags to be initialized only by a transition to global reset mode.

Table 24.121 Registers Initialized in Global Reset Mode or Channel Reset Mode

Register	Bit / Flag
RCFDCnCFDCmCTR register	ROM, CRCT, CTMS[1:0], CTME, CHMDC[1:0]
RCFDCnCFDCmSTS register	CHLTSTS, EPSTS, BOSTS, TRMSTS, RECSTS, COMSTS, ESIF, REC[7:0], TEC[7:0]
RCFDCnCFDCmERFL register	CRCREG[14:0], ADERR, B0ERR, B1ERR, CERR, AERR, FERR, SERR, ALF, BLF, OVLF, BORF, BOEF, EPF, EWF, BEF
RCFDCnCFDCmFDCTR register	EOCCLR, SOCCLR
RCFDCnCFDCmFDSTS register	SOC[7:0], EOC[7:0], SOCO, EOCO, TDCVF, TDCR[6:0]
RCFDCnCFDCmFDCRC register	CRCREG[20:0],SCNT[3:0]
RCFDCnCFDCFCCk register	When transmit/receive FIFO buffer is in transmit mode or gateway mode: CFE
RCFDCnCFDCFSTSk register	When transmit/receive FIFO buffer is in transmit mode or gateway mode: CFMC[7:0], CFFLL, CFEMP, CFMLT, CFRXIF, CFTXIF
RCFDCnCFDCFTISTS register	CFkTXIF
RCFDCnCFDTMCp register	TMOM, TMTAR, TMTR
RCFDCnCFDTMSTSp register	TMTARM, TMTRM, TMTRF[1:0], TMTSTS
RCFDCnCFDTMTRSTSm register	TMTRSTSp (Bits of corresponding channel are initialized in channel reset mode.)
RCFDCnCFDTMTARSTSm register	TMTARSTSp (Bits of corresponding channel are initialized in channel reset mode.)
RCFDCnCFDTMTCSTSm register	TMTCSTSp (Bits of corresponding channel are initialized in channel reset mode.)
RCFDCnCFDTMTASTSm register	TMTASTSp (Bits of corresponding channel are initialized in channel reset mode.)
RCFDCnCFDTXQCCm register	TXQE
RCFDCnCFDTXQSTSm register	TXQTXIF, TXQFLL, TXQEMP
RCFDCnCFDTHLCCm register	THLE
RCFDCnCFDTHLSTSm register	THLMC[5:0], THLIF, THLELT, THLFLL, THLEMP
RCFDCnCFDGTINTSTS0 register	TSIFm, TAIFm, TQIFm, CFTIFm, THIFm (m = 0 to 3)
RCFDCnCFDGTINTSTS1 register	TSIFm, TAIFm, TQIFm, CFTIFm, THIFm (m = 4 to 7)

Table 24.122 Registers Initialized Only in Global Reset Mode

Register	Bit / Flag
RCFDCnCFDGSTS register	GHLTSTS
RCFDCnCFDGERFL register	EEF0, EEF1, EEF2, EEF3, EEF4, EEF5, CMPOF, THLES, MES, DEF
RCFDCnCFDGTSC register	TS[15:0]
RCFDCnCFDRMNDy register	RMNSq
RCFDCnCFDRFCCx register	RFE
RCFDCnCFDRFSTSx register	RFMC[7:0], RFIF, RFMLT, RFFLL, RFEMP
RCFDCnCFDCFCCk register	When transmit/receive FIFO buffer is in receive mode: CFE
RCFDCnCFDCFSTSk register	When transmit/receive FIFO buffer is in receive mode: CFMC[7:0], CFFLL, CFEMP, CFTXIF, CFRXIF, CFMLT
RCFDCnCFDFESTS register	CFkEMP, RFxEMP
RCFDCnCFDFFSTS register	CFkFLL, RFxFLL
RCFDCnCFDFMSTS register	CFkMLT, RFxMLT
RCFDCnCFDRFISTS register	RFxIF
RCFDCnCFDCFRISTS register	CFkRXIF
RCFDCnCFDCDTCT register	CFDMAEm, RFDMAEx
RCFDCnCFDCDTSTS register	CFDMASTSm, RFDMASTSx
RCFDCnCFDGTSTCFG register	RTMPS[8:0], C0ICBCE, C1ICBCE, C2ICBCE, C3ICBCE, C4ICBCE, C5ICBCE, C6ICBCE, C7ICBCE
RCFDCnCFDGTSTCTR register	RTME, ICBCTME

24.6 Reception Functions

There are two reception types.

- Reception by receive buffers:

  Zero to 128 receive buffers can be shared by all channels. Since messages stored in receive buffers are overwritten at each reception, the latest receive data can always be read.

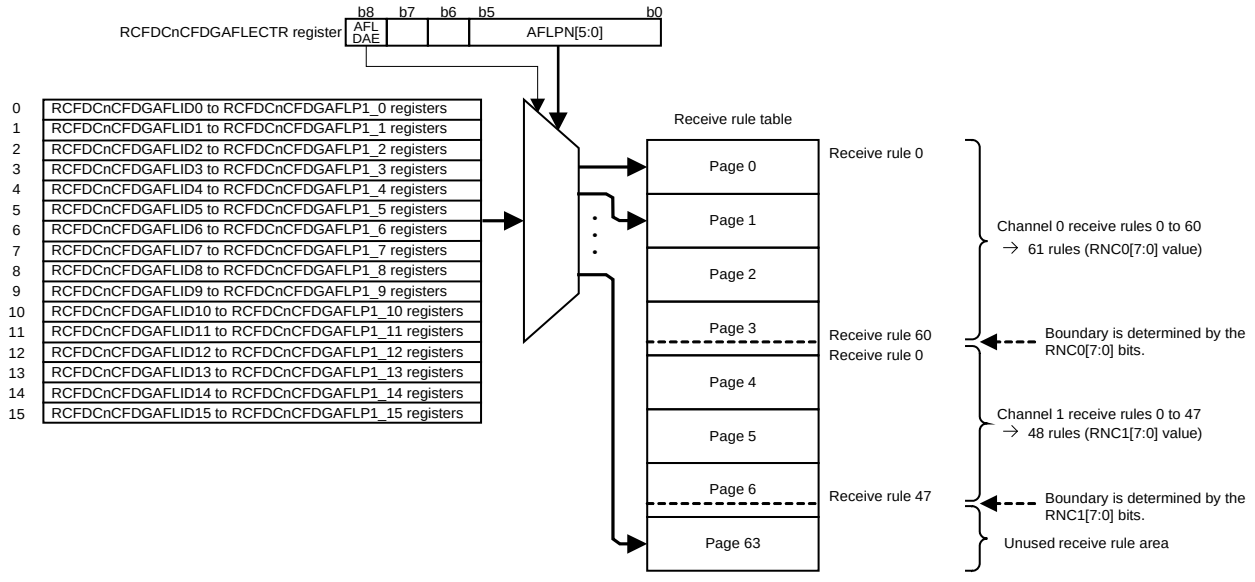
- Reception by receive FIFO buffers and transmit/receive FIFO buffers (receive mode):

  Eight receive FIFO buffers can be shared by all channels and three dedicated transmit/receive FIFO buffers are provided for each channel. Messages of up to the number of buffer stages specified with the RFDC[2:0] and CFDC[2:0] bits can be stored in FIFO buffers and can be read sequentially from the oldest.

24.6.1 Data Processing Using the Receive Rule Table

Data processing using the receive rule table allows dispatching of selected messages to the specified buffer. Data processing includes acceptance filter processing, DLC filter processing, routing processing, label addition processing, and mirror function processing.

Up to 255 receive rules can be registered per channel and up to (128 × number of channels) total receive rules can be registered in the entire module. (Up to 1024 receive rules can be registered in this module that has eight channels.) Set receive rules for each channel. Receive rules cannot be shared with other channels. If receive rules are not set, no messages can be received. **Figure 24.6, Registration of Receive Rules (for Setting Channel 0 and 1)** illustrates how receive rules are registered.



Note: RNC0[7:0], RNC1[7:0]: Bits in the RCFDCnCFDGAFLCFG0 register

Figure 24.6 Registration of Receive Rules (for Setting Channel 0 and 1)

CAUTION

Receive rules for each channel must be set in contiguous blocks. Channel 1 rules and channel 0 rules must be set separately.

Each receive rule consists of 16 bytes in the RCFDCnCFDGAFLIDj, RCFDCnCFDGAFLMj, RCFDCnCFDGAFLP0_j, and RCFDCnCFDGAFLP1_j registers (j = 0 to 15). The RCFDCnCFDGAFLIDj register is used to set GAFLID, GAFLIDE bit, GAFLRTR bit, and the mirror function, the RCFDCnCFDGAFLMj register is used to set mask, the RCFDCnCFDGAFLP0_j register is used to set label information to be added, DLC value, and storage receive buffer, and the RCFDCnCFDGAFLP1_j register is used to set storage FIFO buffer. Up to 16 receive rules can be set per page.

24.6.1.1 Acceptance Filter Processing

In the acceptance filter processing, the ID data, IDE bit, and RTR bit in a received message are compared with the ID data, IDE bit, and RTR bit set in the receive rule of the corresponding channel. When all these bits match, the message passes through the acceptance filter processing. The ID data, IDE bit, and RTR bit in the received message which correspond to the bits set to 0 (bits are not compared) in the RCFDCnCFDGAFLMj register are not compared and are regarded as matched.

Check begins with the receive rule with the smallest number for the corresponding channel. When all the bits to be compared in a received message match the bits set in the receive rule or when all the receive rules are compared without any match, filter processing stops. If there is no matching receive rule, the received message is not stored in the receive buffer or FIFO buffer.

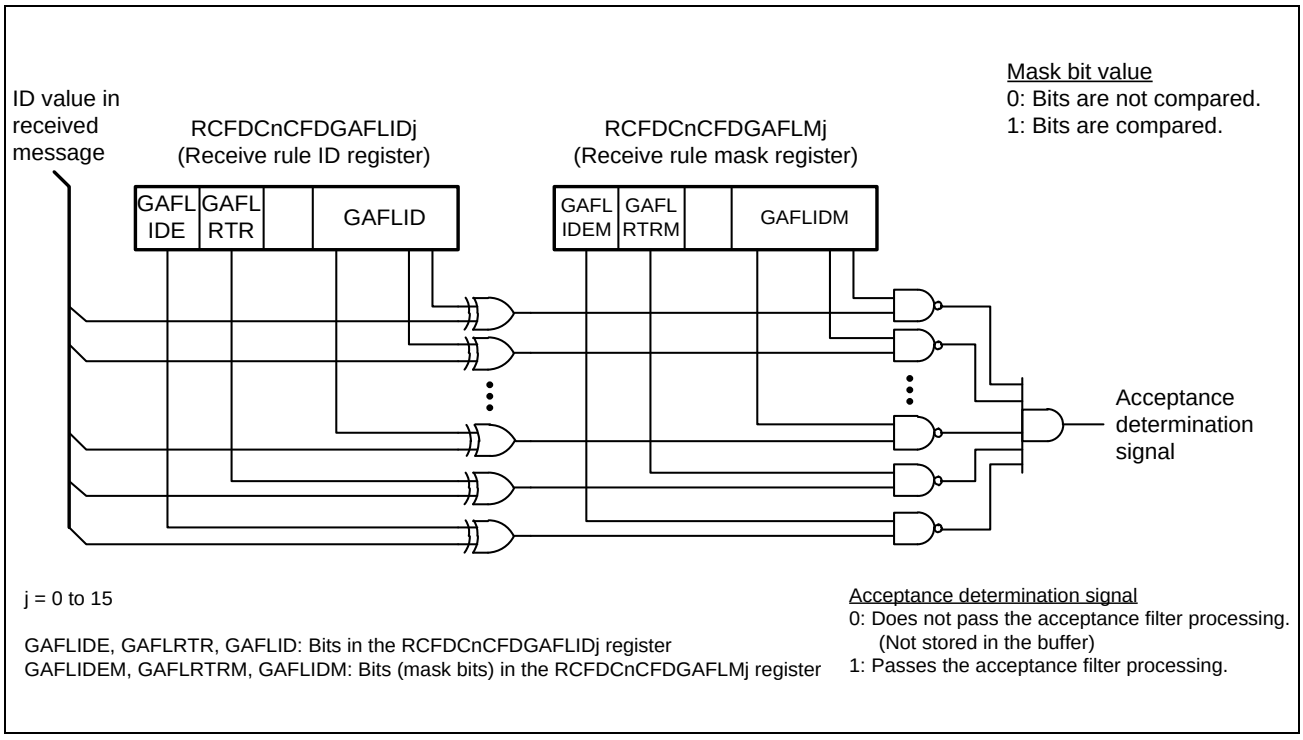


Figure 24.7 Acceptance Filter Function

24.6.1.2 DLC Filter Processing

When the DCE bit in the RCFDCnCFDGCFG register is set to 1 (DLC check is enabled), DLC filter processing is performed for messages that pass through the acceptance filter processing. When the DLC value in a message is equal to or larger than the DLC value set in the receive rule, the message passes through the DLC filter processing.

When a message has passed through the DLC filter processing with the DRE bit in the RCFDCnCFDGCFG register set to 0 (DLC replacement is disabled), the DLC value in the received message is stored in the buffer. In this case, all the data bytes in the received message are stored in the buffer.

When a message has passed through the DLC filter processing with the DRE bit in the RCFDCnCFDGCFG register set to 1 (DLC replacement is enabled), the DLC value in the receive rule is stored in the buffer instead of the DLC value in the received message. In this case, a value of 00_H is stored in each data byte beyond the number of bytes which is indicated by the DLC value in the receive rule.

When the DLC value in the received message is smaller than that in the receive rule, the message does not pass through the DLC filter processing. In this case, the message is not stored in the receive buffer or the FIFO buffer and the DEF flag in the RCFDCnCFDGERFL register is set to 1 (a DLC error is present).

24.6.1.3 Routing Processing

Messages that passed through the acceptance filter processing and the DLC filter processing are stored in receive buffers, receive FIFO buffers, and/or transmit/receive FIFO buffers (set to receive mode or gateway mode). Message storage destination is set by the GAFLRMV and GAFLRMDP[6:0] bits in the RCFDCnCFDGAFLP0_j register (j = 0 to 15) and by the RCFDCnCFDGAFLP1_j register. Messages that passed through the acceptance filter processing and the DLC filter processing can be stored in up to eight buffers.

If the payload length of the received message exceeds the payload storage size of the storage buffer, the CMPOF flag in the RCFDCnCFDGERFL register is set to 1 (payload overflow) and the processing is handled according to the CMPOC bit in the RCFDCnCFDGCFG register. When the CMPOC bit is 0, the received message which exceeds the payload storage size is not stored in the buffer. When the CMPOC bit is 1, the received message is stored in the buffer with payloads exceeding the storage size being discarded, and depending on the DRE bit in the RCFDCnCFDGCFG register the received DLC value or the DLC value of the receive rule is stored in the buffer.

24.6.1.4 Label Addition Processing

It is possible to add 16-bit label information to messages that passed through the filter processing and store them in buffers. This label information is set in the GAFLPTR[15:0] bits in the RCFDCnCFDGAFLP0_j register.

24.6.1.5 Mirror Function Processing

The mirror function allows the CAN node to receive its own transmitted messages. The mirror function is enabled by setting the MME bit in the RCFDCnCFDGCFG register to 1 (mirror function is enabled).

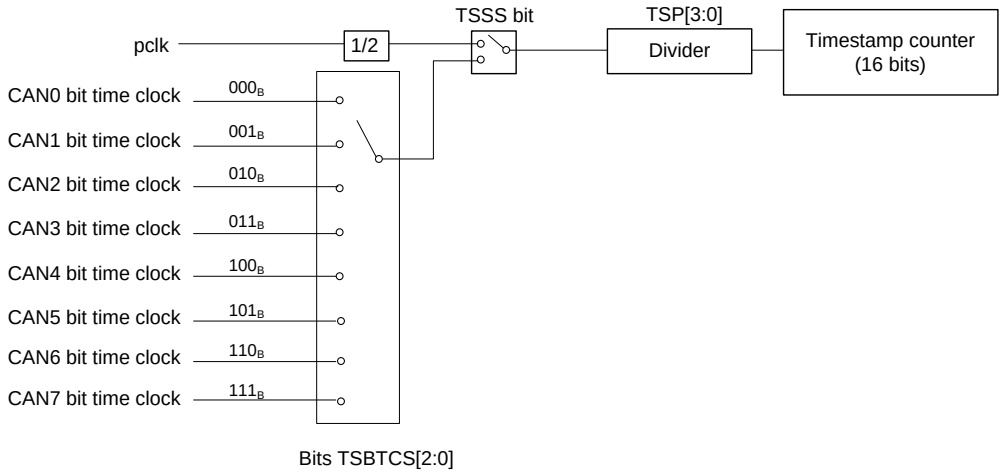
When the mirror function is in use, receive rules for which the GAFLLB bit in the RCFDCnCFDGAFLIDj register is set to 0 are used for data processing when receiving messages transmitted from other CAN nodes. When the CAN node is receiving its own transmitted messages, receive rules for which the GAFLLB bit is set to 1 are used for data processing.

24.6.1.6 Timestamp

The timestamp counter is a 16-bit free-running counter used for recording message receive time and transmission time. The timestamp counter value is fetched at the timing set with the TSCCFG[1:0] bits in the RCFDCnCFDGCFG register and is then stored in a receive buffer or a FIFO buffer together with the message ID and data during data reception. The clock source of the timestamp counter is selected by the TSBTCS[2:0] and TSSS bits in the RCFDCnCFDGCFG register. The clock source is selectable from pclk/2 or nominal CANm bit time clock(m = 0 to 7). However, do not select the nominal CANm bit time clock of channels that handle CAN FD frames. The timestamp counter count source is obtained by dividing the selected clock source by the TSP[3:0] value in the RCFDCnCFDGCFG register.

When the CANm bit time clock or nominal CANm bit time clock is used as a clock source, the timestamp counter stops when the corresponding channel transitions to channel reset mode or channel halt mode. When the pclk/2 is used as a clock source, the timestamp function is not affected by channel mode.

The timestamp counter value is reset to 0000_H by setting the TSRST bit in the RCFDCnCFDGCTR register to 1.



Note: TSBTCS[2:0], TSSS, TSP[3:0]: Bits in the RCFDCnCFDGCFG register
When specifying pclk/2 as the timestamp counter count source, set bits TSBTCS[2:0] to 000_B

Figure 24.8 Timestamp Function Block Diagram

24.7 Transmission Functions

There are three types of transmission. The transmittable payload length is 64 bytes in every transmission types.

- Transmission using transmit buffers:
  Each channel has 32 buffers.
- Transmission using transmit/receive FIFO buffers (transmit mode):
  Each channel has three FIFO buffers. Up to 128 messages can be contained in a single FIFO buffer. Each FIFO buffer is used with a link to a transmit buffer. Only the message to be transmitted next in a FIFO buffer becomes the target of transmit priority determination. Messages are transmitted sequentially on a first-in, first- out basis.
- Transmission using transmit queues:
  Up to 32 transmit buffers per channel can be allocated to the transmit queues. Transmit buffer ((32 × m) + 31) is used as an access window of a corresponding channel. Transmit buffers are allocated to transmit queues in descending order of buffer number. All messages in transmit queues, which are targets of priority determination, are transmitted in the order of ID number.

Figure 24.9, Allocation of Transmit Queues and Transmit/Receive FIFO Buffer Links shows the allocation of transmit queues and transmit/receive FIFO buffer link.

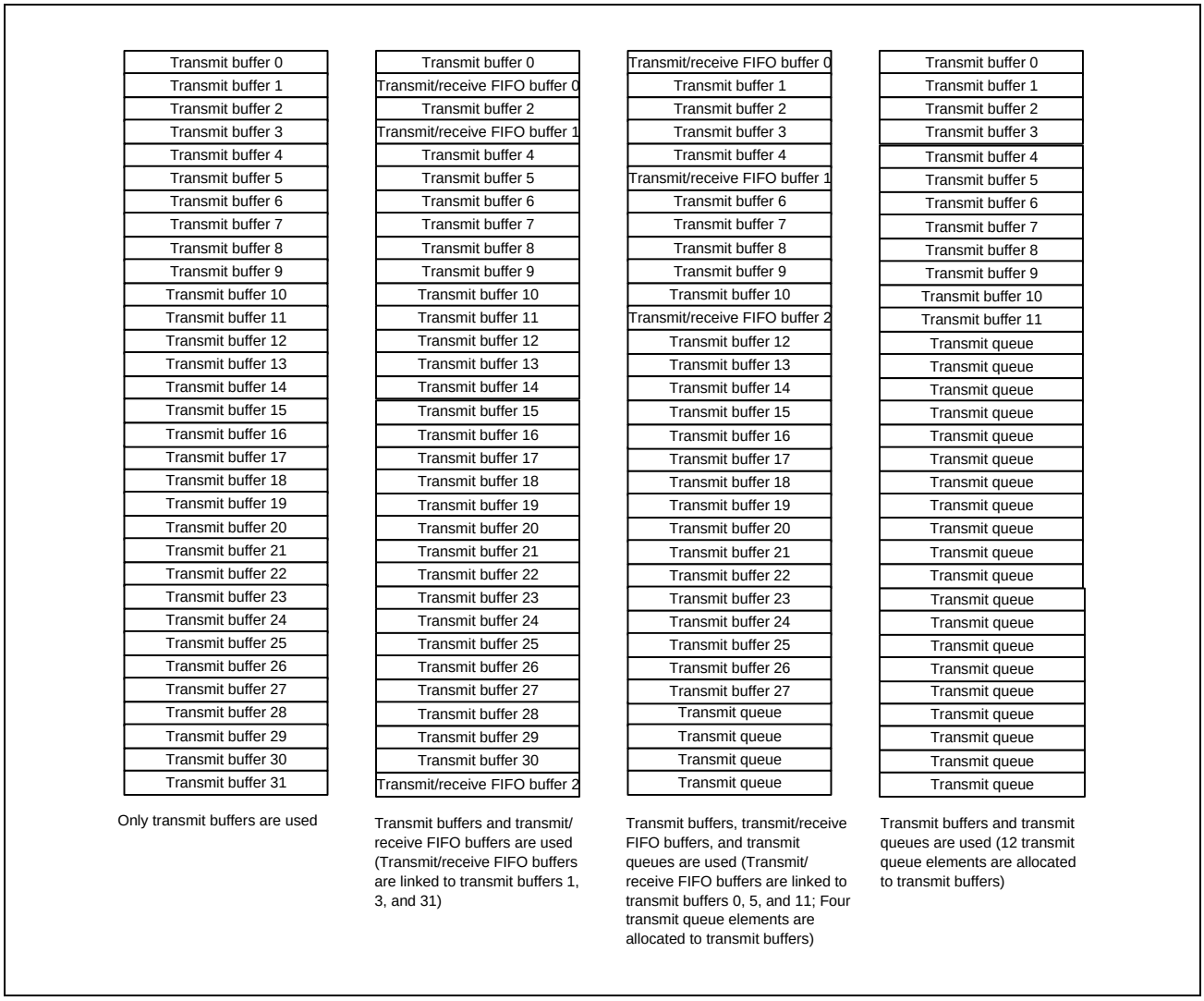


Figure 24.9 Allocation of Transmit Queues and Transmit/Receive FIFO Buffer Links

24.7.1 Transmit Priority Determination

If transmit requests are issued from multiple buffers or from the queue on the same channel, transmit priority is determined using one of the following methods.

- ID priority (TPRI bit = 0)
- Transmit buffer number priority (TPRI bit = 1)

All CAN channels use the setting of the TPRI bit in the RCFDCnCFDGCFG register.

When the TPRI bit is set to 0, messages are transmitted according to the priority of stored message IDs. ID priority conforms to the CAN bus arbitration specification defined in the CAN specifications. All IDs of pending transmit messages are targets of priority determination, regardless of whether they are stored in transmit buffers, transmit/receive FIFO buffers (set to transmit mode or gateway mode), or the transmit queue. If even a single transmit queue is used, select ID priority. When transmit/receive FIFO buffers are used, the oldest message in a FIFO buffer becomes the target of priority determination. When a message is being transmitted from a transmit/receive FIFO buffer, the next message in the FIFO buffer becomes the target of priority determination. When a transmit queue is used, all messages in the transmit queue are targets of priority determination. If the same ID is set for two or more buffers, the buffer with the smaller buffer number takes precedence.

When the TPRI bit is set to 1, the message in the transmit buffer with the smallest buffer number among all buffers with a transmit request is transmitted first. When transmit/receive FIFO buffers are linked to transmit buffers, transmit priority is determined according to linked transmit buffer numbers.

When messages are retransmitted due to an arbitration-lost or an error, transmit priority determination is made again regardless of the TPRI bit setting. When a 2-bit ECC error is detected in the priority determination processing, no message is transmitted.

24.7.2 Transmission Using Transmit Buffers

Setting the transmit request bit (TMTR bit in the RCFDCnCFDTMCp register) in a transmit buffer to 1 (transmission is requested) allows transmission of data frames or remote frames.

The transmit result is shown by the TMTRF[1:0] flag in the corresponding RCFDCnCFDTMSTSp register (p = 0 to 255). When transmit completes successfully, the TMTRF[1:0] flag is set to 10_B (transmission has been completed (without transmit abort request)) or 11_B (transmission has been completed (with transmit abort request)).

24.7.2.1 Transmit Abort Function

With respect to transmit buffers for which the TMTRM bit in the RCFDCnCFDTMSTSp register is set to 1 (a transmit request is present), when the TMTAR bit in the RCFDCnCFDTMCp register is set to 1 (transmit abort is requested), the transmit request is canceled. When transmit abort is completed, the TMTRF[1:0] flag in the RCFDCnCFDTMSTSp register is set to 01_B (transmit abort has been completed) and the transmit request is canceled (clearing the TMTRM bit to 0).

A message that is being transmitted or a message to be transmitted next according to the transmit priority determination cannot be aborted. However, when an arbitration-lost or an error occurs during transmission of a message for which the TMTAR bit is set to 1, retransmission is not performed.

24.7.2.2 One-Shot Transmission Function (Retransmission Disabling Function)

When the TMOM bit in the RCFDCnCFDTMCp register is set to 1 (one-shot transmission is enabled), transmission is performed only once. Even if an arbitration-lost or an error occurs, retransmission is not performed.

The one-shot transmit result is shown by the TMTRF[1:0] flag in the corresponding RCFDCnCFDTMSTSp register. When one-shot transmission completes successfully, the TMTRF[1:0] flag is set to 10_B or 11_B. When an arbitration-lost or an error occurs, the TMTRF[1:0] lag is set to 01_B (transmit abort has been completed).

24.7.3 Transmission Using FIFO Buffers

Multiple messages can be stored in a single transmit/receive FIFO buffer, up to the number specified by the FIFO buffer depth, which is set by the CFDC[2:0] bits in the RCFDCnCFDCFCCk register (k = 0 to 23). Messages are transmitted sequentially on a first-in, first-out basis.

Each transmit/receive FIFO buffer is linked to a transmit buffer selected by the CFTML[4:0] bits in the RCFDCnCFDCFCCk register. When the CFE bit in the RCFDCnCFDCFCCk register is set to 1 (transmit/receive FIFO buffers are used), transmit/receive FIFO buffers become targets of transmit priority determination. Priority of only the next transmit message is determined in the FIFO buffer.

When the CFE bit is set to 0 (no transmit/receive FIFO buffer is used), the CFEMP flag is set to 1 (the transmit/receive FIFO buffer contains no message (buffer empty)) at the timing below.

- The transmit/receive FIFO buffer becomes empty immediately if the message in it is not being transmitted or is not to be transmitted next.
- The transmit/receive FIFO buffer becomes empty after transmission completion, CAN bus error detection, arbitration-lost or the transition to channel halt mode in the case that a message in it is being transmitted or to be transmitted next.

When the CFE bit is cleared to 0, all messages in transmit/receive FIFO buffers are lost and messages cannot be stored in FIFO buffers. Confirm that the CFEMP flag is set to 1 before setting the CFE bit to 1 again.

24.7.3.1 Interval Transmission Function

A message transmission interval time can be set to space the transmission of messages from the same FIFO buffer when using a transmit/receive FIFO buffer set to transmit mode or gateway mode.

Immediately after the first message has been transmitted successfully from the FIFO buffer with the CFE bit in the RCFDCnCFDCFCCk register set to 1, the interval timer starts counting (after EOF7 of the CAN protocol). After that, when the interval time has passed, the next message is transmitted. The interval timer stops in channel reset mode or by clearing the CFE bit to 0.

The interval time is set by the CFITT[7:0] bits in the RCFDCnCFDCFCCk register. When the interval timer is not used, set the CFITT[7:0] bits to 00_H.

Select an interval timer count source using the CFITR and CFITSS bits in the RCFDCnCFDCFCCk register. When the CFITR and CFITSS bits are set to 00_B, the count source is obtained by dividing pclk/2 by the value of the ITRCP[15:0] bits. When the CFITR and CFITSS bits are set to 10_B, the count source is obtained by dividing pclk/2 by (the value of the ITRCP[15:0] bits × 10). When the CFITR and CFITSS bits are set to $x1_B$, the CANm bit time clock becomes a count source in Classical CAN only mode and the nominal CANm bit time clock becomes a count source in CAN FD mode. (Use this count source only for the channel which does not handle the CAN FD frames in CAN FD mode.)

The interval time is calculated by the following equations where M is the value of ITRCP[15:0] and N is the value of CFITT[7:0].

- When CFITR and CFITSS = 00_B

$$\frac{1}{\text{pclk frequency}} \times 2 \times M \times N$$

- When CFITR and CFITSS = 10_B:

$$\frac{1}{\text{pclk frequency}} \times 2 \times M \times 10 \times N$$

- When CFITR and CFITSS = $x1_B$:

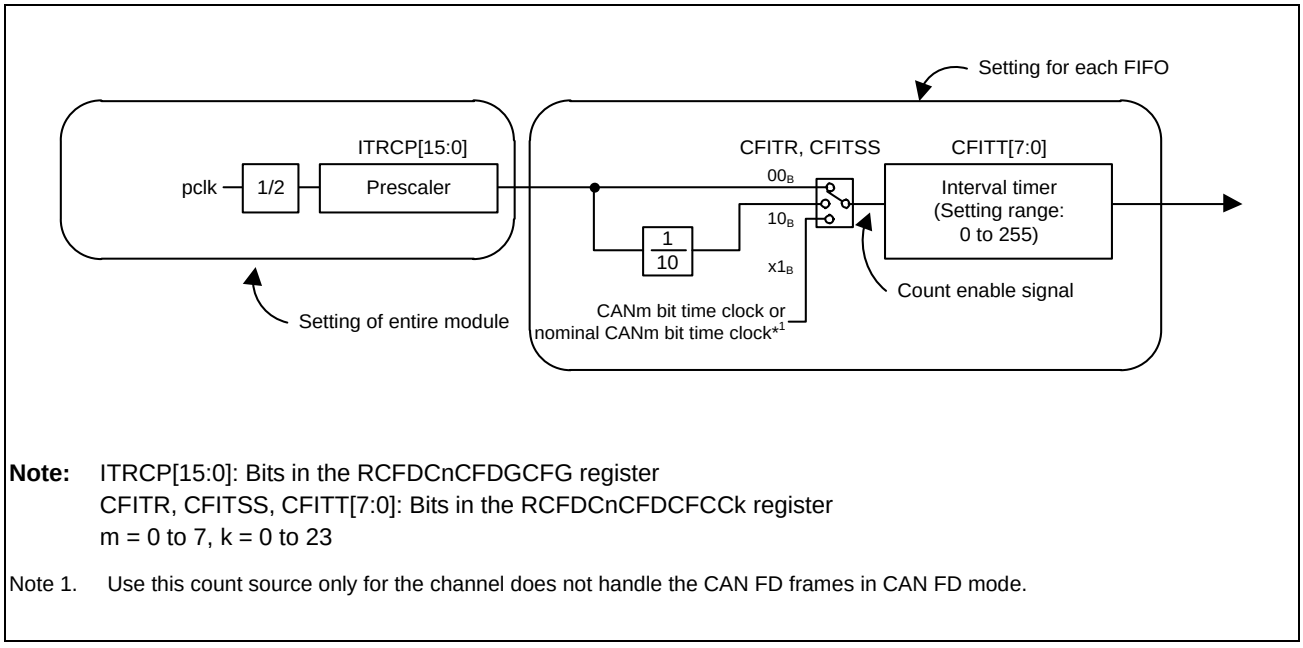
  Classical CAN only mode:

$$\frac{1}{\text{CANm bit time clock frequency}} \times N$$

  CAN FD mode and CAN FD only mode:

$$\frac{1}{\text{Nominal CANm bit time clock frequency}} \times N$$

Figure 24.10, Interval Timer Block Diagram shows the interval timer block diagram.

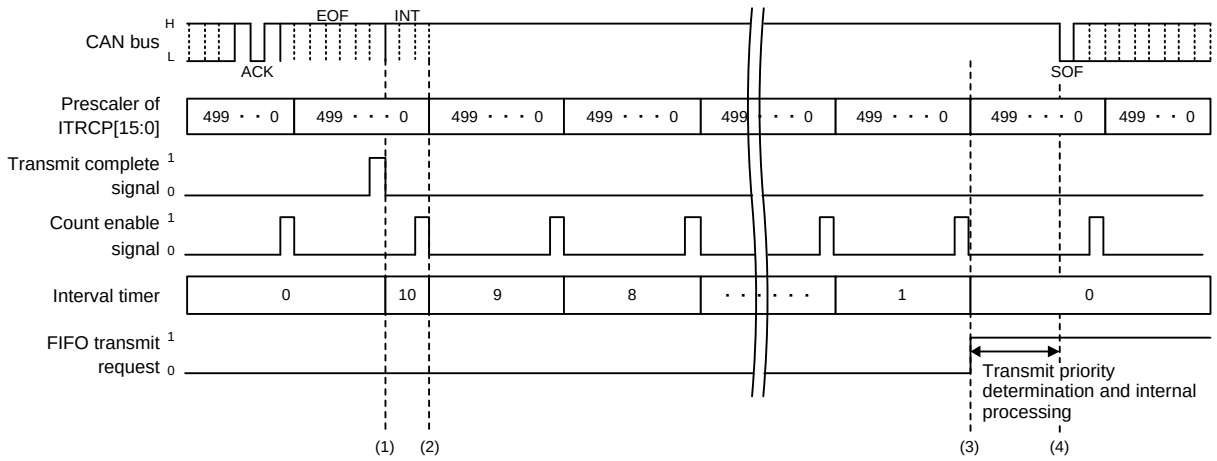


Note: ITRCP[15:0]: Bits in the RCFDCnCFDGCFG register
CFITR, CFITSS, CFITT[7:0]: Bits in the RCFDCnCFDCFCCk register
m = 0 to 7, k = 0 to 23

Note 1. Use this count source only for the channel does not handle the CAN FD frames in CAN FD mode.

Figure 24.10 Interval Timer Block Diagram

Figure 24.11, Interval Timer Timing Chart shows the interval timer timing diagram.



$$\text{Interval time (theoretical value)} = \frac{2}{\text{pclk frequency}} \times (\text{set ITRCP[15:0] value}) \times \text{set CFITT[7:0] value}$$

Note: ITRCP[15:0]: Bits in the RCFDCnCFDGCFG register (The set value is 500 in this figure.)
CFITT[7:0]: Bits in the RCFDCnCFDCFCCk register (The set value is 10 in this figure.)

Figure 24.11 Interval Timer Timing Chart

(1) The interval timer starts counting upon completion of transmission. Since the prescaler is not initialized at the time of transmission completion, the first interval time contains an error of up to one count of the interval timer.

(2) The interval timer is decremented by 1 upon the next count enable signal.

(3) When the interval timer has decreased to 0, the transmit/receive FIFO buffer issues a transmit request.

(4) The transmit/receive FIFO buffer is determined for the next transmission by the priority determination, it starts transmitting data. Transmission starts usually with a delay of three CANm bit time clock cycles or less from the issue of transmit request. If multiple internal processes (such as receive filter processing, message routing, and transmit priority determination) take place in all channels, a delay of up to 1164 pclk cycles may be generated.

24.7.4 Transmission Using Transmit Queues

3 to 32 buffers are allocated to a transmit queue for each channel, and transmit buffer ((32 × m) + 31) is used as an access window of a corresponding channel.

All messages in a transmit queue are targets of transmit priority determination and are transmitted in the ID priority order regardless of storage sequence. If two messages having the same ID are stored in a transmit queue, these messages are not always transmitted in the order of their storage in the transmit queue.

Setting the TXQE bit in the RCFDCnCFDTXQCCm register to 0 disables transmit queues. When the TXQE bit is set to 0, the TXQEMP flag in the RCFDCnCFDTXQSTSm register is set to 1 (the transmit queue contains no messages (transmit queue empty)) at the timing below.

- The transmit queue becomes empty immediately when no message in it is being transmitted or will be transmitted next.
- The transmit queue becomes empty after transmission completion, CAN bus error detection, arbitration-lost, or the transition to channel halt mode when a message in it is being transmitted or will be transmitted next.

When the TXQE bit is cleared to 0, all messages in transmit queues are lost and messages cannot be stored in transmit queues. Confirm that the TXQEMP flag is set to 1 before setting the TXQE bit to 1 again.

24.7.5 Transmit Data Padding (in CAN FD Mode and in CAN FD only Mode)

When the payload length indicated by the set DLC value in a transmit message exceeds the payload storage area size of a buffer to be used for transmission, excessive payloads are padded by CC_H.

This processing is performed in the following cases.

- Transmit/receive FIFO set to transmission or gateway mode:

When the payload length of the transmit DLC exceeds the transmit/receive FIFO payload storage area size set by the CFPLS[2:0] bits in the RCFDCnCFDCFCCk register.

This processing is also performed in FD only mode, if a Classical Frame is configured with a DLC bigger than 8.

24.7.6 Transmit History Function

Information about transmission-completed messages can be stored in the transmit history buffer. Each channel has a single transmit history buffer that can contain 32 sets of transmit history data.

A message transmit source buffer type can be selected by the THLDTE bit in the RCFDCnCFDTHLCCm register. The THLEN bit in the RCFDCnCFDCFIDk register (k = 0 to 23) and the RCFDCnCFDTMIDp register (p = 0 to 255)determines whether transmit history data is stored for each message.

A timestamp value is always included in the transmit history data..

The following information on a transmitted message will be stored in the transmit history buffer after the successful completion of transmission.

Storage of the transmit history data after the successful completion of transmission may take up to 448 pclk cycles.

- Buffer type

  001_B: Transmit buffer

  010_B: Transmit/receive FIFO buffer

  100_B: Transmit queue

- Buffer number:

  Number of source transmit buffer, transmit queue, or transmit/receive FIFO buffer. This number depends on buffer types. See **Table 24.123, Transmit History Data Buffer Numbers**.

- Label data: Label information of the transmit message
- Timestamp: Timestamp value of the transmit message

Table 24.123 Transmit History Data Buffer Numbers

Buffer Type / Buffer No.	001_B	010_B	100_B
00000_B	Transmit buffer 32 × m + 0	Buffer numbers of the transmit buffer linked to the transmit/receive FIFO buffer by the CFTML[4:0] bits in the RCFDCnCFDCFCCk register (k = 0 to 23)	Buffer numbers of the transmit buffer allocated to the transmit queue that performed transmission
00001_B	Transmit buffer 32 × m + 1		
00010_B	Transmit buffer 32 × m + 2		
00011_B	Transmit buffer 32 × m + 3		
00100_B	Transmit buffer 32 × m + 4		
00101_B	Transmit buffer 32 × m + 5		
00110_B	Transmit buffer 32 × m + 6		
00111_B	Transmit buffer 32 × m + 7		
01000_B	Transmit buffer 32 × m + 8		
01001_B	Transmit buffer 32 × m + 9		
01010_B	Transmit buffer 32 × m + 10		
01011_B	Transmit buffer 32 × m + 11		
01100_B	Transmit buffer 32 × m + 12		
01101_B	Transmit buffer 32 × m + 13		
01110_B	Transmit buffer 32 × m + 14		
01111_B	Transmit buffer 32 × m + 15		
10000_B	Transmit buffer 32 × m + 16		
10001_B	Transmit buffer 32 × m + 17		
10010_B	Transmit buffer 32 × m + 18		
10011_B	Transmit buffer 32 × m + 19		
10100_B	Transmit buffer 32 × m + 20		
10101_B	Transmit buffer 32 × m + 21		
10110_B	Transmit buffer 32 × m + 22		
10111_B	Transmit buffer 32 × m + 23		
11000_B	Transmit buffer 32 × m + 24		
11001_B	Transmit buffer 32 × m + 25		
11010_B	Transmit buffer 32 × m + 26		
11011_B	Transmit buffer 32 × m + 27		
11100_B	Transmit buffer 32 × m + 28		
11101_B	Transmit buffer 32 × m + 29		
11110_B	Transmit buffer 32 × m + 30		
11111_B	Transmit buffer 32 × m + 31		

Label data is used to identify each message. Unique label data can be added to each message transmitted from a transmit buffer, transmit queue, or transmit/receive FIFO buffer.

The timestamp value is fetched from the timestamp counter at the SOF (start of frame) timing of the message. For details about the timestamp counter, see **Section 24.6.1.6, Timestamp**.

Transmit history data can be read from the RCFDCnCFDTHLACC0m register and the RCFDCnCFDTHLACC1m register. If an attempt is made to store new transmit history data while the buffer is full, the buffer overflows and the new data is discarded.

24.8 Gateway Function

When a transmit/receive FIFO buffer is set to gateway mode, receive messages can be transmitted from an arbitrary channel without CPU intervention.

When the CFM[1:0] bits in the RCFDCnCFDCFCCk register are set to 10_B (gateway mode) for the transmit/receive FIFO buffer selected by the RCFDCnCFDGAFLP1_j register of a channel being used for transmission, messages that pass through filter processing according to the receive rule are stored in the specified transmit/receive FIFO buffer and are automatically transmitted from the buffer.

Messages stored in a transmit/receive FIFO buffer are transmitted sequentially on a first-in, first-out basis. Only the message to be transmitted next becomes the target of transmit priority determination.

Transmit/receive FIFO buffers in the gateway mode are disabled by setting the CFE bit in the

RCFDCnCFDCFCCk register to 0 and the CFEMP flag becomes 1 according to the timing below.

- The transmit/receive FIFO buffer becomes empty immediately when the message in it is not being transmitted and will not to be transmitted next.
- The transmit/receive FIFO buffer becomes empty after transmission completion, CAN bus error detection, or arbitration-lost when the message in it is being transmitted or will be transmitted next.

When the CFE bit is cleared to 0, all messages in transmit/receive FIFO buffers are lost and messages can no longer be stored in transmit/receive FIFO buffers. Confirm that the CFEMP flag is set to 1 before setting the CFE bit to 1 again.

24.8.1 CAN-CAN FD Gateway

When the gateway function is used, a frame to be transmitted can be replaced with a classical CAN frame or a CAN FD frame.

Setting the GWEN bit in the RCFDCnCFDCmFDCFG register to 1 enables the CAN-CAN FD gateway. The FDF and BRS bits in the transmit frame can be selected by the GWFDF and GWBRS bits in the RCFDCnCFDCmFDCFG register. When the DLC value of the received CAN frame is 1001_B or more and the GWFDF bit is 1 (CAN FD frame), the DLC value is replaced with 1000_B.

When the CAN-CAN FD gateway is enabled, do not perform routing for the following frames.

- Remote frames

24.9 Test Function

The test function is classified into communication tests and global tests.

- Communication tests: Performed for each channel.
  - Standard test mode
  - Listen-only mode
  - Self-test mode 0 (external loopback mode)
  - Self-test mode 1 (internal loopback mode)
  - Restricted operation mode
- Global tests: Performed for the entire module
  - RAM test (read/write test)
  - Inter-channel communication test [CRC error test enabled]

24.9.1 Standard Test Mode

CRC tests are enabled in standard test mode. The CRC value calculated by the RS-CANFD module based on the transmit message or receive message is stored in the register. This CRC value is stored in the CRCREG[14:0] bits in the RCFDCnCFDCmERFL register when the message is a classical CAN frame (CRC length = 15 bits) or in the CRCREG[20:0] bits in the RCFDCnCFDCmFDCRC register when the message is a CAN FD frame (CRC length = 17 or 21 bits). Use the inter-channel communication test function for CRC error tests. For details, see **Section 24.9.6.1, CRC Error Test**.

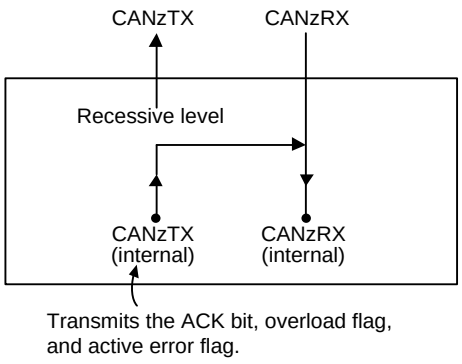
24.9.2 Listen-Only Mode

Listen-only mode allows reception of data frames and remote frames. Only recessive bits are transmitted on the CAN bus, and the ACK bit, overload flag, and active error flag are not transmitted.

Listen-only mode is available for detecting the communication speed.

Do not make a transmit request from any buffer or queue in listen-only mode.

Figure 24.12, Connection when Listen-Only Mode is Selected shows the connection when listen-only mode is selected.



Note: z = 0 to 11

Figure 24.12 Connection when Listen-Only Mode is Selected

24.9.3 Self-Test Mode (Loopback Mode)

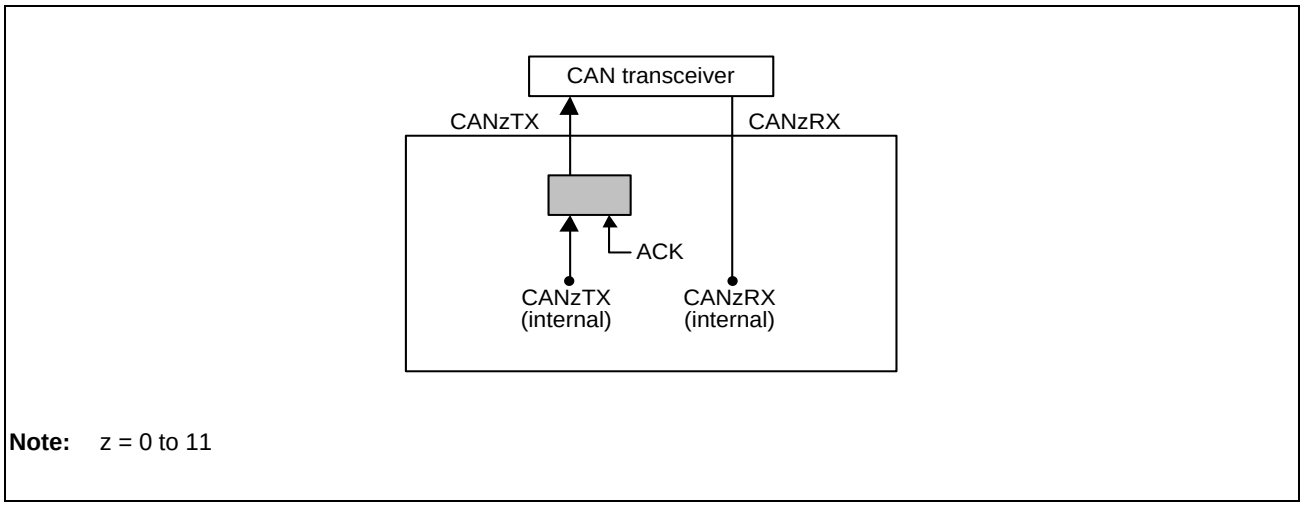
In self-test mode, transmitted messages are compared with the receive rule of the own channel and the messages are stored in a buffer if they have passed through the filter processing. Messages transmitted from other CAN nodes are compared only with the receive rule for which the GAFLLB bit in the RCFDCnCFDGAFLIDj register (j = 0 to 15) is set to 0 (when a message transmitted from another CAN node is received).

If the mirror function and self-test mode are both enabled, the self-test mode setting takes precedence.

24.9.3.1 Self-Test Mode 0 (External Loopback Mode)

Self-test mode 0 is used to perform a loopback test within a channel including the CAN transceiver. In self-test mode 0, transmitted messages are handled as messages received through the CAN transceiver and are stored in a buffer. An ACK bit is generated to receive messages transmitted from the own CAN node.

Figure 24.13, Connection when Self-Test Mode 0 is Selected shows the connection when self-test mode 0 is selected.



Note: z = 0 to 11

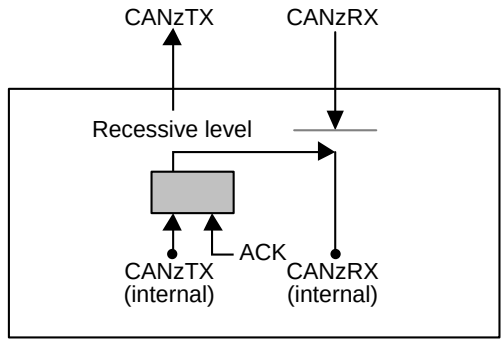
Figure 24.13 Connection when Self-Test Mode 0 is Selected

24.9.3.2 Self-Test Mode 1 (Internal Loopback Mode)

In self-test mode 1, transmitted messages are handled as received messages and are stored in a buffer. An ACK bit is generated to receive messages transmitted from the own CAN node.

In self-test mode 1, internal feedback from the internal CANzTX pin (z = 0 to 11) to the internal CANzRX pin is performed. The external CANzRX pin input is isolated. The external CANzTX pin outputs only recessive bits.

Figure 24.14, Connection when Self-Test Mode 1 is Selected shows the connection when self-test mode 1 is selected.



Note: z = 0 to 11

Figure 24.14 Connection when Self-Test Mode 1 is Selected

24.9.4 Restricted Operation Mode (CAN FD Mode and CAN FD Only Mode)

In restricted operation mode, an ACK bit is generated when a valid data frame and a remote frame have been received, but these frames are not transmitted even if an error frame or an overload frame transmit condition is detected. When a condition is detected, operation is suspended until the bus idle state comes for resynchronization with the CAN communication. The receive error counter (REC) and the transmit error counter (TEC) do not change due to an error.

A desired transmission request can be made for transmission without restrictions.

24.9.5 RAM Test

The RAM test function allows accesses to all CAN RAM addresses.

When the RAM test function is used, the RAM is divided into pages of 256 bytes each. RAM test page are set by the RTMPS[8:0] bits in the RCFDCnCFDGTSTCFG register. Data in the set page can be read from and written to the RCFDCnCFDRPGACCr register (r = 0 to 63).

The available total RAM size:

- RCFDC0 with 8 channels: 67840 bytes (10900_H).
- RCFDC0 with 6 channels: 50880 bytes ($C6C0_H$).
- RCFDC1 with 4 channels: 33920 bytes (8480_H).

24.9.6 Inter-Channel Communication Test

The inter-channel communication test function allows communication test by internally connecting CAN channels to each other. During this test, channels are isolated from the external CAN bus.

Before starting data transmission/reception in channel communication mode, make transmission/reception settings for each channel.

Set the channels not participating in test to Channel halt mode.

Figure 24.15, Connection for Inter-Channel Communication Test shows the connection for inter-channel communication test.

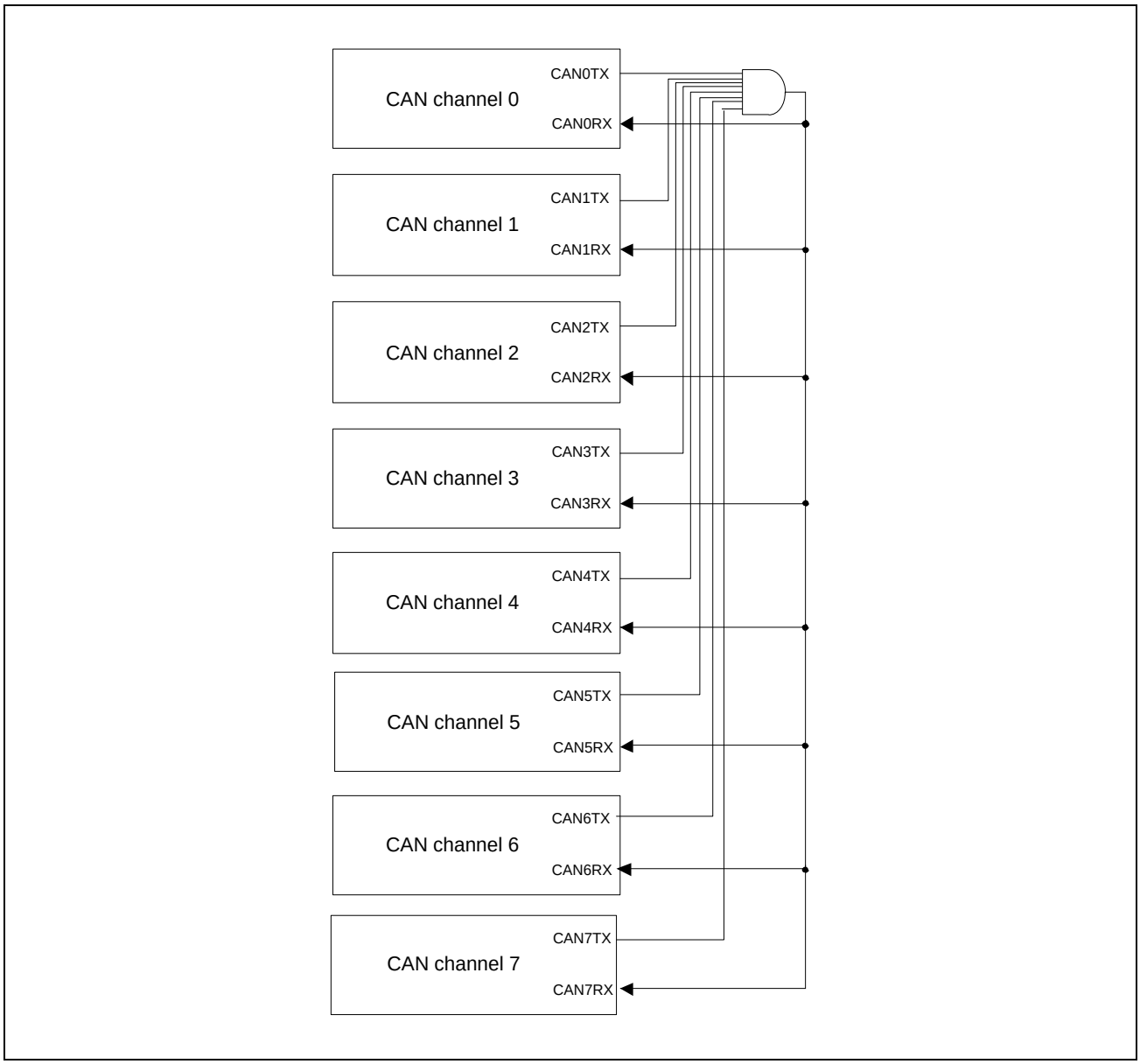


Figure 24.15 Connection for Inter-Channel Communication Test

24.9.6.1 CRC Error Test

A CRC error test is enabled during an inter-channel communication test. The following shows an example of channel 0 CRC error test procedure during a communication test between channel 0 and channel 1.

Preconditions

- Inter-channel communication test is enabled.
- Channel 0 and channel 1 are in standard test mode.

Procedure

1. Make a setting to send a message from the transmit buffer p of channel 1.
2. Set the CRCT bit in the RCFDCnCFDC0CTR register to 1 (to enable inversion of the first bit in the received ID field).
3. Set the TMTR bit in the RCFDCnCFDTMCp register to 1 (to issue a transmission request to the transmit buffer p of channel 1).
4. Wait for occurrence of a CAN0 error interrupt due to a channel bus error.
5. Read the CRCREG[14:0] bits in the RCFDCnCFDCmERFL register or the CRCREG[20:0] bits in the RCFDCnCFDCmFDCRC register of channel 0 and channel 1, and confirm that the CRC values are different on the transmission and the reception side.
6. Confirm that the CERR bit in RCFDCnCFDC0ERFL is 1 (CRC error detected).

The CRC error test function generates an incorrect CRC value by inverting the first bit in the received ID field. Therefore, note that not a CRC error but a stuff error (continuous 6-bit data of the same level) is detected when a message in which ID's upper 5-bit value is 10000_B or ID's upper 6-bit value is 011111_B is received.

The CRC generation circuit of the RS-CANFD module is contained in the protocol controller of each channel. Another CRC calculation test is not necessary during transmission because the same circuit is used for both transmission and reception.

24.10 RS-CANFD Setting Procedure

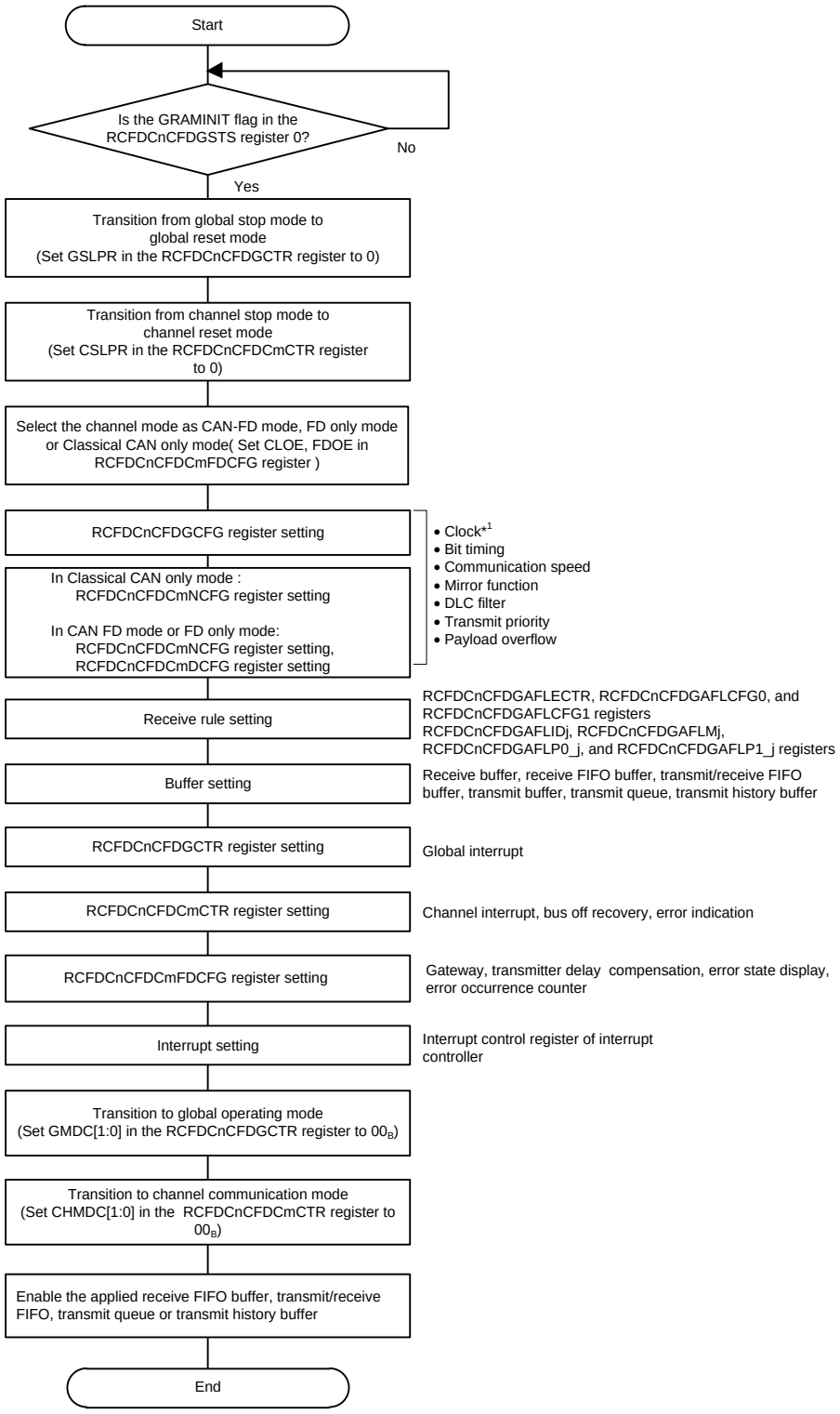
24.10.1 Initial Settings

The RS-CANFD module initializes the CAN RAM after the MCU is reset.

The RAM initialization time:

- RCFDC0 with 8 channels: 25730 pclk cycles.
- RCFDC0 with 6 channels: 19298 pclk cycles.
- RCFDC1 with 4 channels: 12866 pclk cycles.

The GRAMINIT flag in the RCFDCnCFDGSTS register is set to 1 (CAN RAM initialization is ongoing) during the RAM initialization and is cleared to 0 (CAN RAM initialization is finished) when the initialization is completed. Make CAN settings after the GRAMINIT flag is cleared to 0. **Figure 24.16, CAN Setting Procedure after the MCU is Reset** shows the CAN setting procedure after the MCU is reset.



Note: m = 0 to 7, j = 0 to 15

Note 1. For the setting of CAN clock frequency, see **Table 24.19, Range of Operating Frequency Depending on the Transfer Rate and the Number of Channels in Use in the RH850/F1KH and RH850/F1KM**.

Figure 24.16 CAN Setting Procedure after the MCU is Reset

24.10.1.1 Clock Setting

Set the CAN clock (fCAN) as a clock source of the RS-CANFD module. Select the clk_xincan or clkc using the DCS bit in the RCFDCnCFDGCFG register.

24.10.1.2 Bit Timing Setting

In the CAN protocol, one bit of a communication frame consists of three segments SS, TSEG1, and TSEG2, of which two segments TSEG1 and TSEG2 can be set by the corresponding registers for each channel. Two bit rates (nominal bit rate and data bit rate) are provided. Set the nominal bit rate in the RCFDCnCFDCmNCFG register and set the data bit rate in the RCFDCnCFDCmDCFG register. Sample point timing can be determined by setting these two segments. This timing can be adjusted in units of 1 Time Quantum (hereafter referred to as Tq). A single Tq is the cycle of clock obtained by dividing the clock selected by the DCS bit in the RCFDCnCFDGCFG register. Set a division ratio by the NBRP[9:0] bits in the RCFDCnCFDCmNCFG register and the DBRP[7:0] bits in the RCFDCnCFDCmDCFG register (CANmTq(N) clock and CANmTq(D) clock).

Be sure to specify the same values for both NBRP[9:0] and DBRP[7:0].

To specify different values for the nominal bit rate and the data bit rate, change the values of the RCFDCnCFDCmNCFG.NTSEG1 and NTSEG2 bits and RCFDCnCFDCmDCFG.DTSEG1 and DTSEG2 bits, respectively.

When the TDCE bit is set to 1(Transmitter delay compensation is enabled) in the RCFDCnCFDCmFDCFG register, set the equal value of 1 or less to the bits NBRP[9:0] and DBRP[7:0] .

Figure 24.17, Bit Timing Chart shows the bit timing chart. **Table 24.124, Example of Bit Timing Settings** shows an example of bit timing setting.

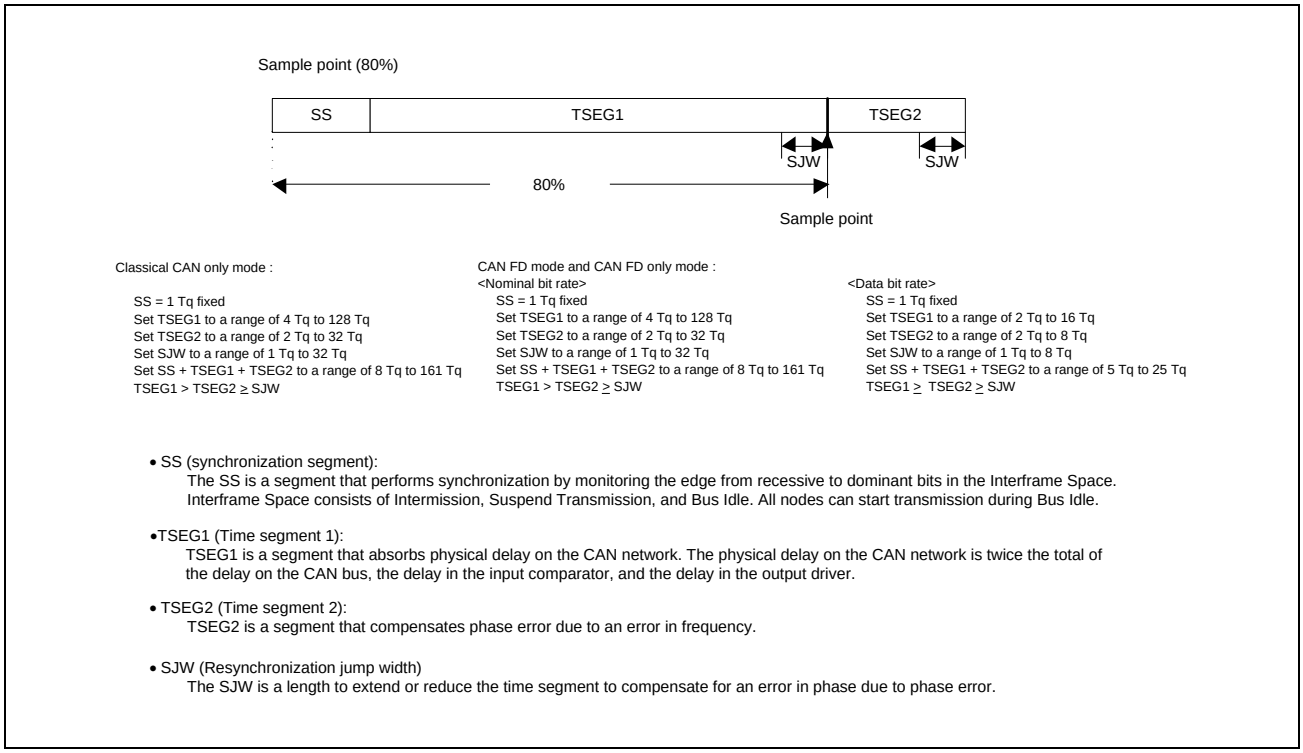


Figure 24.17 Bit Timing Chart

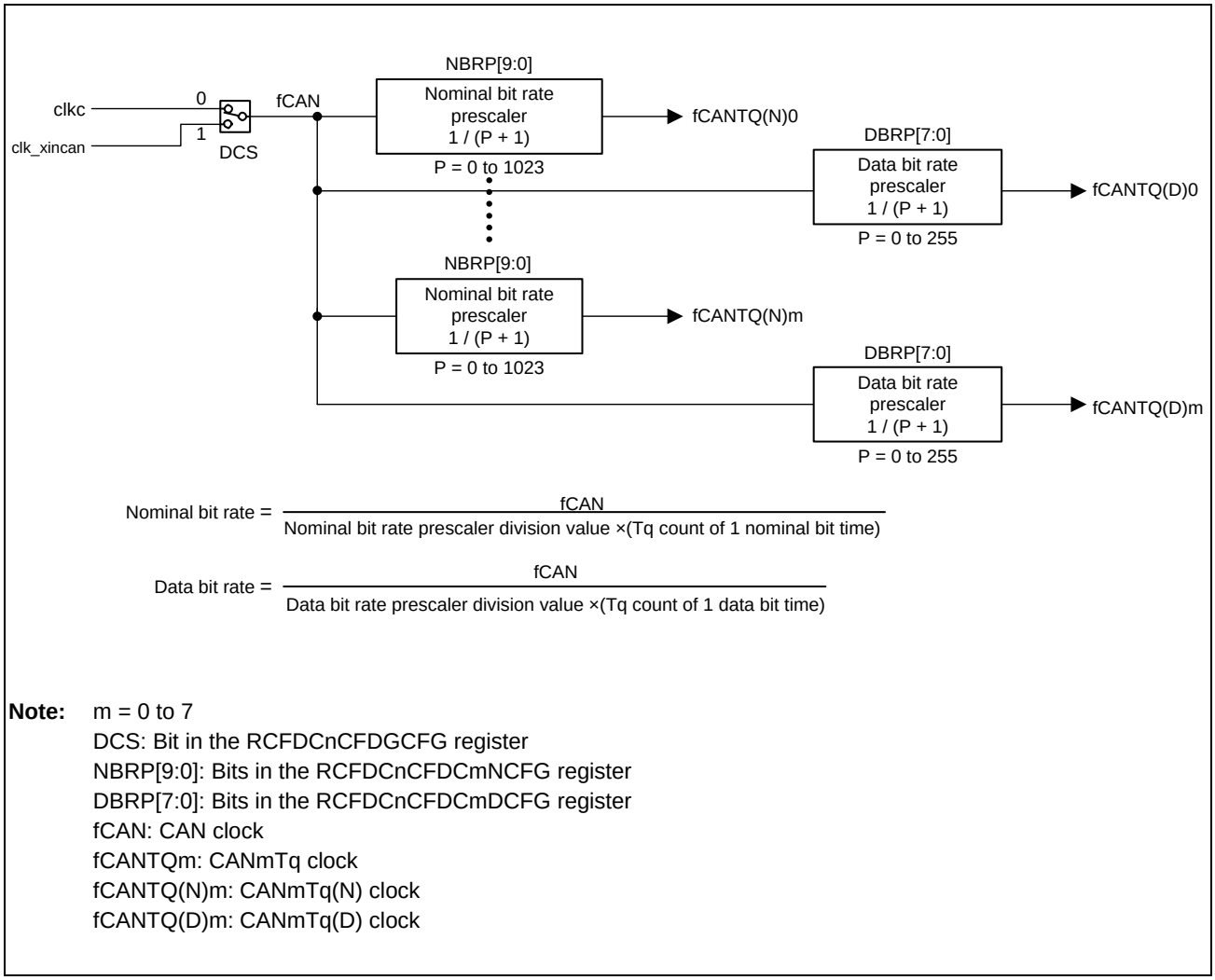
Table 24.124 Example of Bit Timing Settings

1 Bit	Set Value (Tq)				Sample Point (%) Note: See **Table 24.27, RS-CANFD Module Specifications**.
	SS	TSEG1	TSEG2	SJW	
8 Tq	1	4	3	1	62.50
	1	5	2	1	75.00
10 Tq	1	6	3	1	70.00
	1	7	2	1	80.00
16 Tq	1	10	5	1	68.75
	1	11	4	1	75.00
20 Tq	1	12	7	1	65.00
	1	13	6	1	70.00
50 Tq	1	39	10	4	80.00

24.10.1.3 Communication Speed Setting

Set the CAN communication speed for each channel using the fCAN, baud rate prescaler division value, and Tq count per bit time. Set two types of transmission rate (arbitration phase and data phase) for each channel.

Figure 24.18, CAN Clock Control Block Diagram shows the CAN clock control block diagram, and **Table 24.125, Example of Communication Speed Setting (Classical CAN only mode)** shows an example of the communication speed setting.



Note: m = 0 to 7
DCS: Bit in the RCFDCnCFDGCFG register
NBRP[9:0]: Bits in the RCFDCnCFDCmNCFG register
DBRP[7:0]: Bits in the RCFDCnCFDCmDCFG register
fCAN: CAN clock
fCANTQm: CANmTq clock
fCANTQ(N)m: CANmTq(N) clock
fCANTQ(D)m: CANmTq(D) clock

Figure 24.18 CAN Clock Control Block Diagram

Table 24.125 Example of Communication Speed Setting (Classical CAN only mode)

fCAN / Communication Speed	40 MHz	32 MHz	24 MHz	20 MHz	16 MHz	8 MHz
1 Mbps	8 Tq (5) 20 Tq (2)	8 Tq (4) 16 Tq (2)	8 Tq (3) 12 Tq (2) 24 Tq (1)	10 Tq (2) 20 Tq (1)	8 Tq (2) 16 Tq (1)	8 Tq (1)
500 Kbps	8 Tq (10) 20 Tq (4)	8 Tq (8) 16 Tq (4)	8 Tq (6) 12 Tq (4) 24 Tq (2)	10 Tq (4) 20 Tq (2)	8 Tq (4) 16 Tq (2)	8 Tq (2) 16 Tq (1)
250 Kbps	8 Tq (20) 20 Tq (8)	8 Tq (16) 16 Tq (8)	8 Tq (12) 12 Tq (8) 24 Tq (4)	10 Tq (8) 20 Tq (4)	8 Tq (8) 16 Tq (4)	8 Tq (4) 16 Tq (2)
125 Kbps	8 Tq (40) 20 Tq (16)	8 Tq (32) 16 Tq (16)	8 Tq (24) 12 Tq (16) 24 Tq (8)	10 Tq (16) 20 Tq (8)	8 Tq (16) 16 Tq (8)	8 Tq (8) 16 Tq (4)

Table 24.126 Example of Transmission Rate Setting (Nominal Bit Rate and Data Bit Rate in CAN FD mode and CAN FD only mode)

fCAN / Communication Rate	40 MHz	20 MHz
Nominal bit rate 500 kbps Data bit rate 5 Mbps	Nominal bit rate 80 Tq (1) Data bit rate 8Tq (1)	None
Nominal bit rate 1M bps Data bit rate 2 Mbps	Nominal bit rate 40 Tq (1) Data bit rate 20Tq (1)	Nominal bit rate 20 Tq (1) Data bit rate 10 Tq (1)

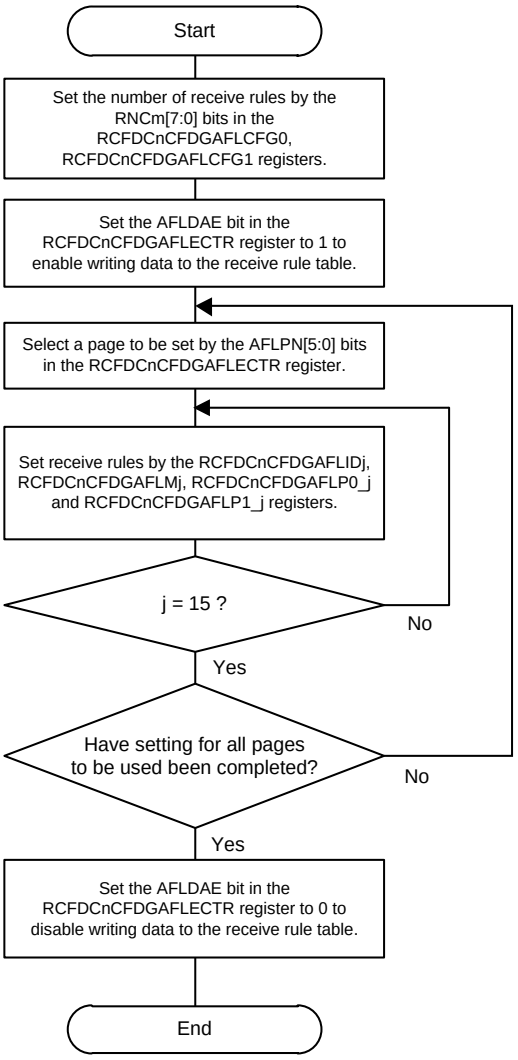
Note: Values in ( ) are baud rate prescaler division values.

24.10.1.4 Receive Rule Setting

Receive rules can be set using receive rule-related registers.

Up to 16 receive rules can be registered per page. Specify pages 0 to 63 (for 8-channel unit) by the AFLPN[5:0] bits in the RCFDCnCFDGAFLECTR register. Set receive rule table write enable/disable using the AFLDAE bit.

Figure 24.19, Receive Rule Setting Procedure shows the receive rule setting procedure.



Note: m = 0 to 7, j = 0 to 15

Figure 24.19 Receive Rule Setting Procedure

24.10.1.5 Buffer Setting

Set the number of buffers to be used (number of messages to be stored) and interrupt sources. And also set the payload storage size. For transmit/receive FIFO buffers that are set to transmit mode, set transmit buffers to be linked.

Up to 28672 bytes of the RAM can be used in receive buffers and FIFO buffers. Configure the buffers so that the following conditions are met.

Number of receive buffers × (12 + payload storage size) + total of (number of depth × (12 + payload storage size)) of receive FIFO buffers x + total of (number of depth × (12 + payload storage size)) of transmit/receive FIFO buffers k ≤ 28672 bytes

NOTE

The size of the RAM is for the RS-CANFDs that has 8 channels (m = 0 to 7) of IP design logic.
Regard the size of the RAM as the ones corresponding to your target product (3584 × (m+1) bytes).

Figure 24.20, Buffer Configuration shows the buffer configuration. **Figure 24.21, Buffer Setting Procedure** shows the buffer setting procedure.

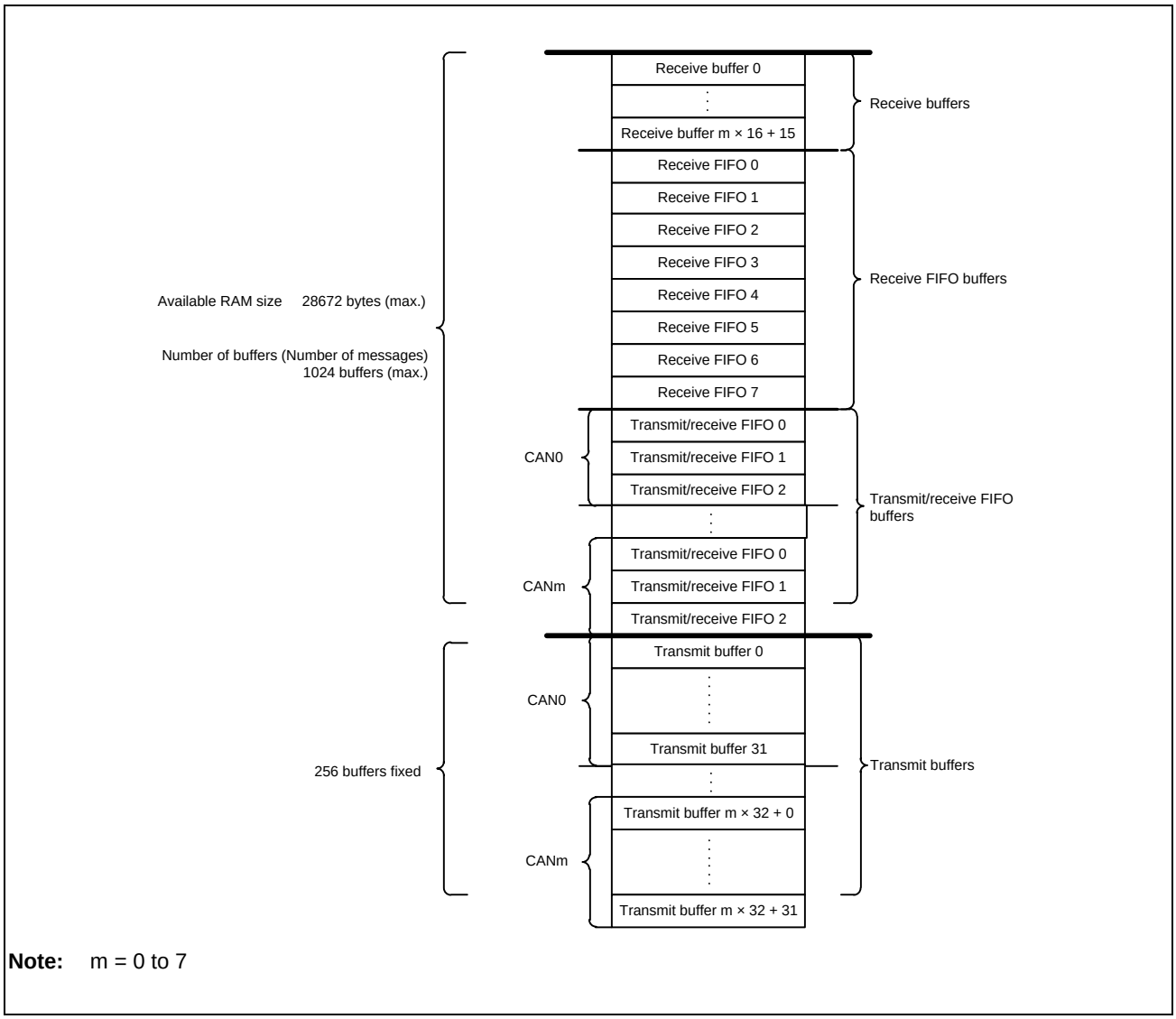
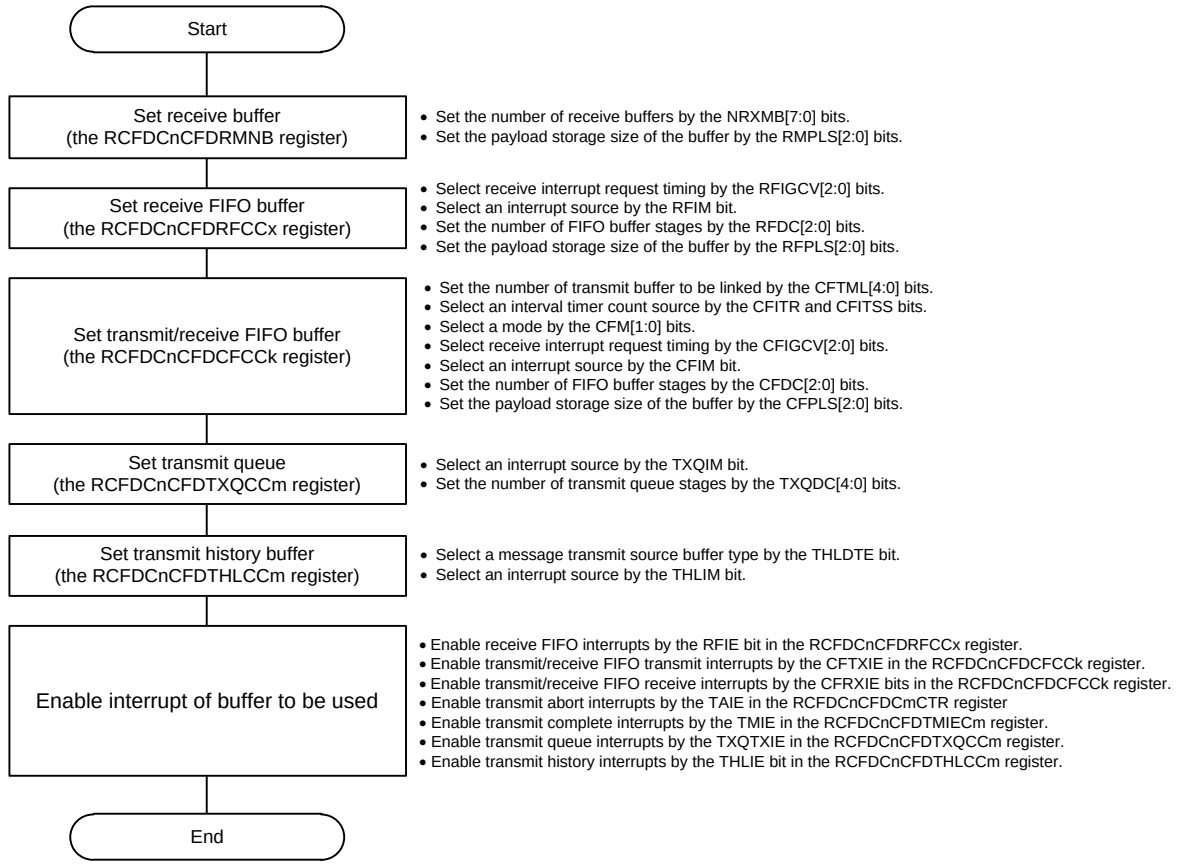


Figure 24.20 Buffer Configuration

CAUTION

Receive buffers, receive FIFO buffers, transmit/receive FIFO buffers, and transmit buffers are located in succession.



Note: k = 0 to 23, x = 0 to 7

Figure 24.21 Buffer Setting Procedure

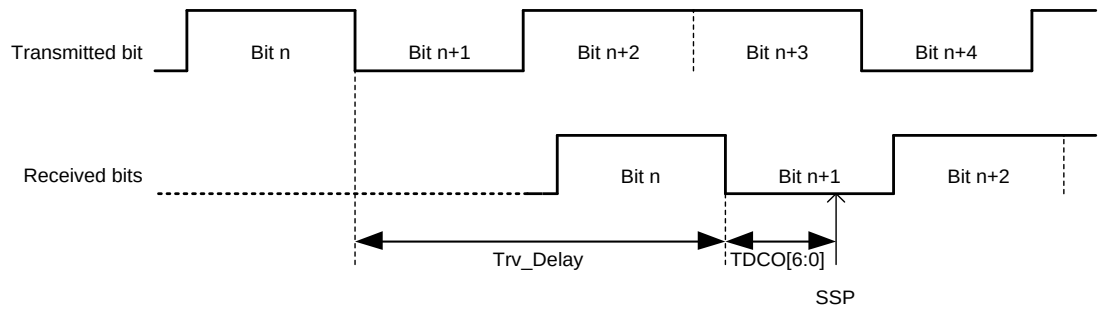
24.10.1.6 Transmitter Delay Compensation

A high baud rate is used in the data phase in CAN FD mode and CAN FD only mode. Transmitter delay compensation is provided as a function to accept propagation delay in data phase.

To use this function, set the TDCE bit in the RCFDCnCFDCmFDCFG register to 1. Also set the secondary sample point (SSP) timing used in the data phase by the TDCOC bit and TDCO[6:0] bits in the RCFDCnCFDCmFDCFG register.

When the TDCOC bit is 0, the SSP timing equals the total value of the delay measured by the RS- CANFD module and the TDCO[6:0] value. (This value is rounded off to the nearest integer of Tq.)

Usually, the TDCO[6:0] value must be equal to SS + TSEG1, the sample point timing



Note: Bit n: Bit in the data phase
TDCO[6:0]: Bits in the RCFDCnCFDCmFDCFG register

Figure 24.22 SSP timing

When the TDCOC bit is 1, the SSP timing is determined only by the TDCO[6:0] value. (When the DBRP[7:0] value in the RCFDCnCFDCmDCFG register is larger than 0, the TDCO[6:0] value is also rounded off to the nearest integer of Tq.)

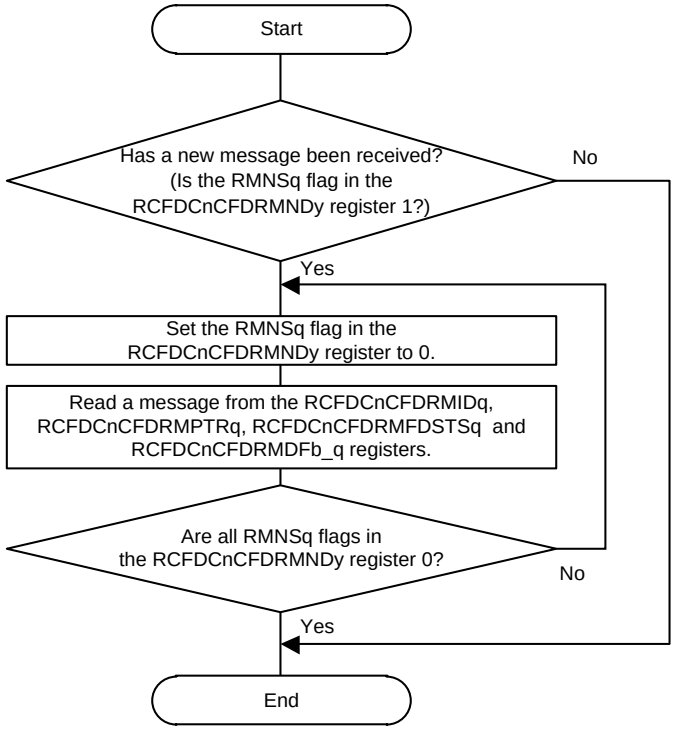
The RS-CANFD module compensates a delay up to (3 CANm bit time - 2 fCAN). (CANm bit time is data bit rate value.)

When the TDCE bit is set to 1(Transmitter delay compensation is enabled) in the RCFDCnCFDCmFDCFG register, set the equal value of 1 or less to the bits NBRP[9:0] and DBRP[7:0].

24.10.2 Reception Procedure

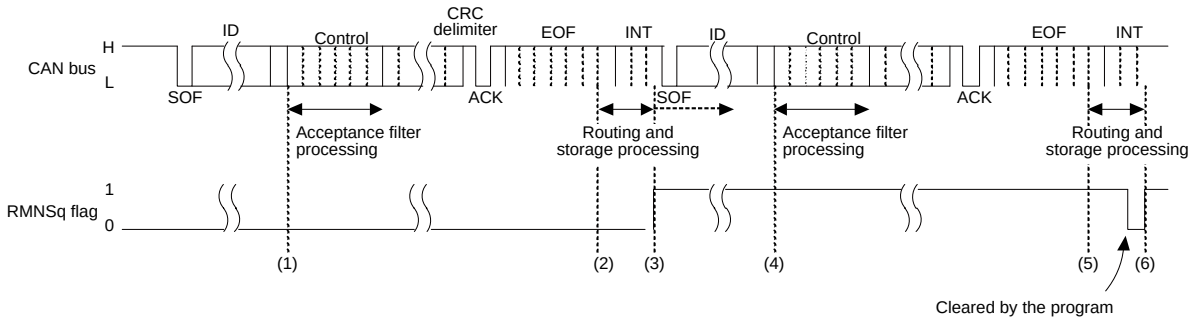
24.10.2.1 Receive Buffer Reading Procedure

When the processing to store received messages in a receive buffer starts, the RMNSq flag in the RCFDCnCFDRMNDy register (y = 0 to 3, q = 0 to 127) is set to 1 (receive buffer q contains a new message). Messages can be read from registers RCFDCnCFDRMIDq, RCFDCnCFDRMPTRq, RCFDCnCFDRMFDSTSq, and RCFDCnCFDRMDFb_q (b = 0 to 15). If the next message is received before reading the message out of buffer, the message will be overwritten. **Figure 24.23, Receive Buffer Reading Procedure** shows the receive buffer reading procedure. This procedure ensures the consistency of messages read from registers RCFDCnCFDRMIDq, RCFDCnCFDRMPTRq, RCFDCnCFDRMFDSTSq, and RCFDCnCFDRMDFb_q.



Note: y = 0 to 3, q = 0 to 127, b = 0 to 15

Figure 24.23 Receive Buffer Reading Procedure



Note: y = 0 to 3, q = 0 to 127
RMNSq: Flag in the RCFDCnCFDRMNDy register

Figure 24.24 Receive Buffer Reception Timing Chart

(1) When the ID field in a message has been received, the acceptance filter processing starts.

(2) When the message matches the receive rule of the corresponding channel and the message has been successfully received, the routing processing to transfer the message to the specified buffer starts. When the DCE bit in the RCFDCnCFDGCFG register is set to 1 (DLC check is enabled), the DLC filter processing starts at this time.

(3) When the message has passed through the DLC filter processing, the processing to store the message in the specified receive buffer starts.
When the message storage processing starts, the RMNSq flag in the corresponding RCFDCnCFDRMNDy register is set to 1 (the receive buffer contains a new message). If other channels are performing filter processing or transmit priority determination processing, the routing processing and the storage processing may be delayed.

(4) When the ID field of the next message has been received, the acceptance filter processing starts.

(5) When the message matches the receive rule of the corresponding channel and the message has been successfully received, the routing processing to transfer the message to the specified buffer starts. When the DCE bit in the RCFDCnCFDGCFG register is set to 1 (DLC check is enabled), the DLC filter processing starts at this time.

(6) When the corresponding RMNSq flag is cleared to 0 (the receive buffer contains no new message), this flag is set to 1 again when the message storage processing starts. Even if the RMNSq flag remains 1, a new message is overwritten to the receive buffer. The RMNSq flag can not be cleared to 0 during storage of messages.

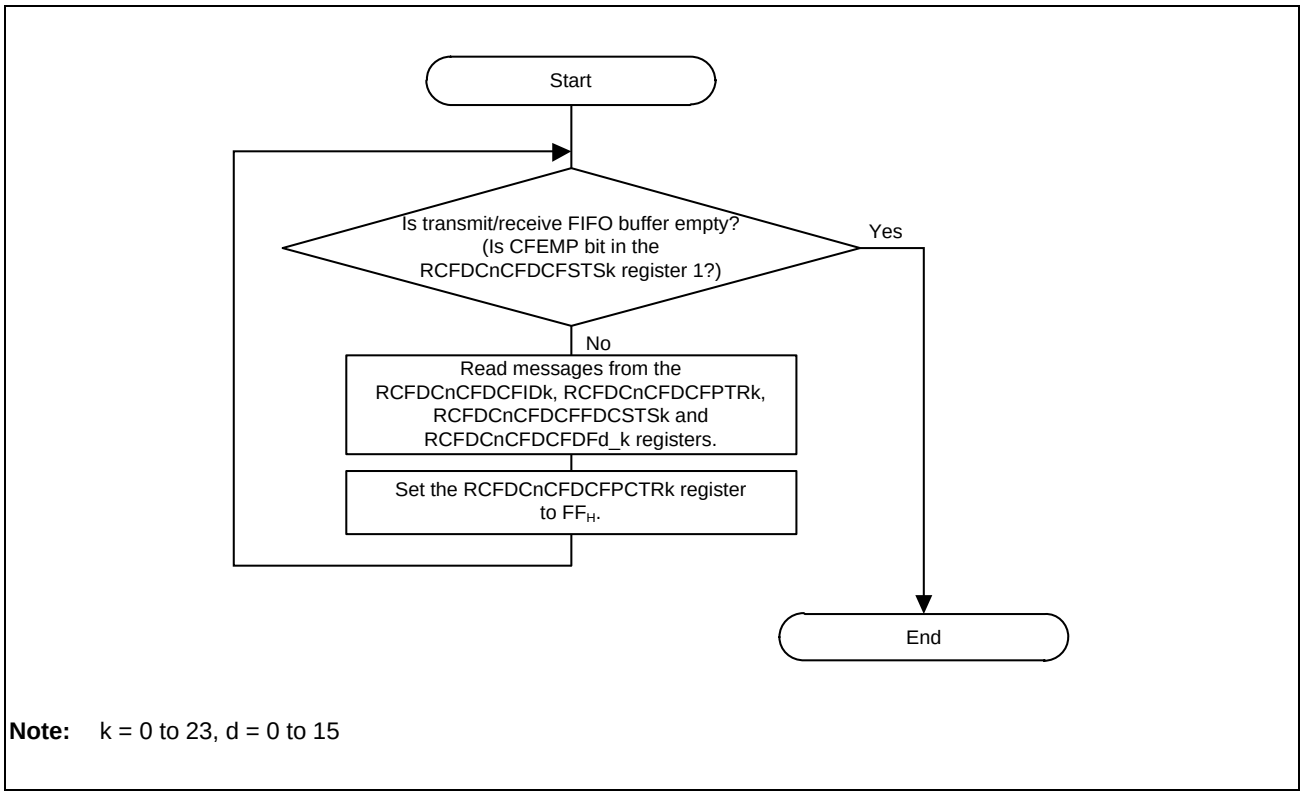
24.10.2.2 FIFO Buffer Reading Procedure

When received messages have been stored in one or more receive FIFO buffers or a transmit/receive FIFO buffer that is set to receive mode or gateway mode, the corresponding message counter (RFMC[7:0] bits in the RCFDCnCFDRFSTSx register (x = 0 to 7) or CFMC[7:0] bits in the RCFDCnCFDCFSTSk register (k = 0 to 23)) is incremented by 1. At this time, when the RFIE bit (receive FIFO interrupt is enabled) in the RCFDCnCFDRFCCx register or the CFRXIE bit (transmit/receive FIFO receive interrupt is enabled) in the RCFDCnCFDCFCCk register is set to 1, an interrupt request is generated. Received messages can be read from the RCFDCnCFDRFIDx, RCFDCnCFDRFPTRx, RCFDCnCFDRFFDSTSx, and RCFDCnCFDRFDFd_x (d = 0 to 15) registers for receive FIFO buffers, or from the RCFDCnCFDCFIDk, RCFDCnCFDCFPTRk, RCFDCnCFDCFFDCSTSk and RCFDCnCFDCFDFd_k registers for transmit/receive FIFO buffers. Messages in FIFO buffers can be read sequentially on a first-in, first-out basis.

When the message counter value matches the FIFO buffer depth (a value set by the RFDC[2:0] bits in the RCFDCnCFDRFCCx register or the CFDC[2:0] bits in the RCFDCnCFDCFCCk register), the RFFLL or CFFLL flag is set to 1 (the receive FIFO buffer is full).

When all messages have been read out of the FIFO buffer, the RFEMP flag in the RCFDCnCFDRFSTSx register or the CFEMP flag in the RCFDCnCFDCFSTSk register is set to 1 (the receive FIFO buffer contains no unread message (buffer empty)).

If the RFE bit or the CFE bit is cleared to 0 (no receive FIFO buffer is used) with the interrupt request flag (RFIF flag in the RCFDCnCFDRFSTSx register or CFRXIF flag in the RCFDCnCFDCFSTSk register) set to 1 (a receive FIFO interrupt request is present), the interrupt request flag is not automatically cleared to 0. The program must clear the interrupt request flag to 0.



Note: k = 0 to 23, d = 0 to 15

Figure 24.25 Transmit/Receive FIFO Buffer Reading Procedure

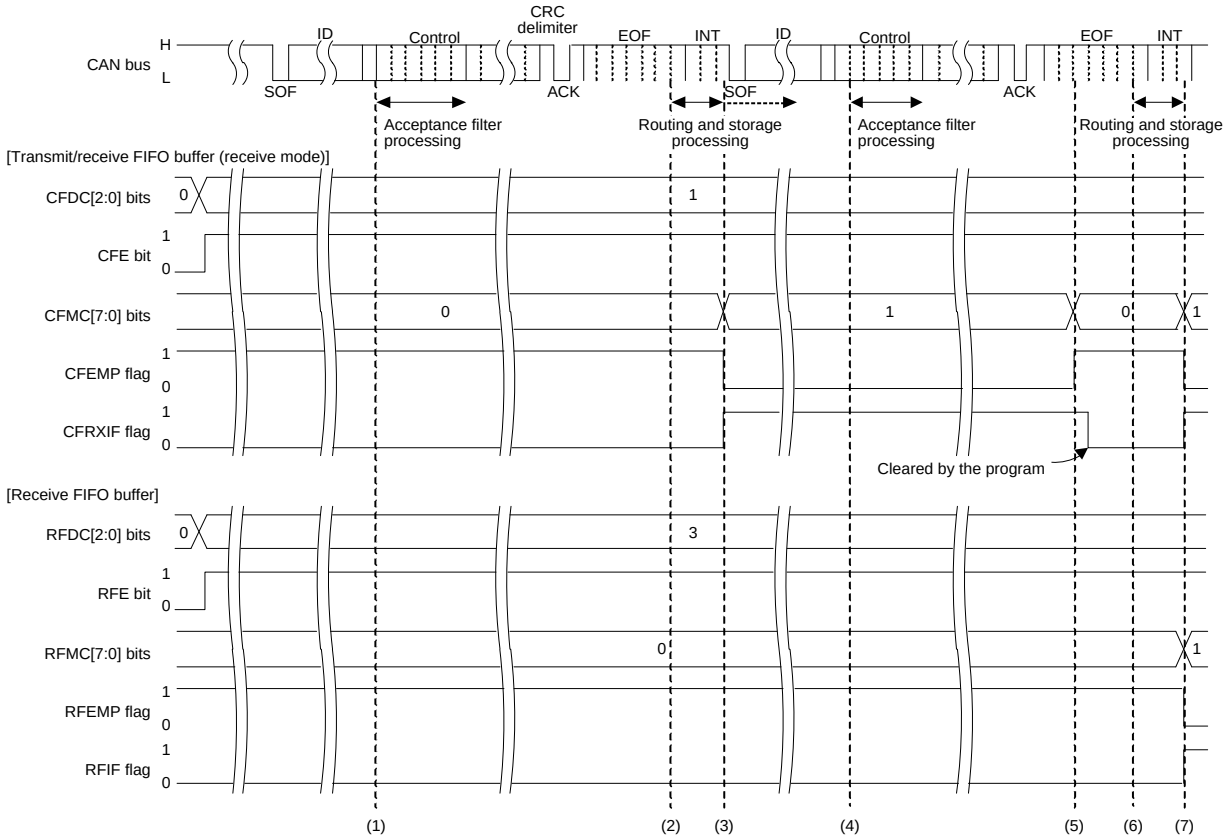
When reading a message, do not read the RCFDCnCFDRFDFd_x or RCFDCnCFDCFDFd_k register corresponding to the area exceeding the payload storage size specified by the RFPLS[2:0] bits in the RCFDCnCFDRFCCx register or the CFPLS[2:0] bits in the RCFDCnCFDCFCCk register.

Table 24.127 Payload Storage Area of Receive FIFO Buffer

Set RFPLS[2:0] Value	Payload Storage Size	Corresponding Data Field Registers
000_B	8 bytes	RCFDCnCFDRFDF0_x to RCFDCnCFDRFDF1_x
001_B	12 bytes	RCFDCnCFDRFDF0_x to RCFDCnCFDRFDF2_x
010_B	16 bytes	RCFDCnCFDRFDF0_x to RCFDCnCFDRFDF3_x
011_B	20 bytes	RCFDCnCFDRFDF0_x to RCFDCnCFDRFDF4_x
100_B	24 bytes	RCFDCnCFDRFDF0_x to RCFDCnCFDRFDF5_x
101_B	32 bytes	RCFDCnCFDRFDF0_x to RCFDCnCFDRFDF7_x
110_B	48 bytes	RCFDCnCFDRFDF0_x to RCFDCnCFDRFDF11_x
111_B	64 bytes	RCFDCnCFDRFDF0_x to RCFDCnCFDRFDF15_x

Table 24.128 Payload Storage Area of Transmit/Receive FIFO Buffer

Set CFPLS[2:0] Value	Payload Storage Size	Corresponding Data Field Registers
000_B	8 bytes	RCFDCnCFDCFDF0_k to RCFDCnCFDCFDF1_k
001_B	12 bytes	RCFDCnCFDCFDF0_k to RCFDCnCFDCFDF2_k
010_B	16 bytes	RCFDCnCFDCFDF0_k to RCFDCnCFDCFDF3_k
011_B	20 bytes	RCFDCnCFDCFDF0_k to RCFDCnCFDCFDF4_k
100_B	24 bytes	RCFDCnCFDCFDF0_k to RCFDCnCFDCFDF5_k
101_B	32 bytes	RCFDCnCFDCFDF0_k to RCFDCnCFDCFDF7_k
110_B	48 bytes	RCFDCnCFDCFDF0_k to RCFDCnCFDCFDF11_k
111_B	64 bytes	RCFDCnCFDCFDF0_k to RCFDCnCFDCFDF15_k



Note: CFDC[2:0], CFE: Bits in the RCFDCnCFDCFCCk register
CFMC[7:0], CFEMP, CFRXIF: Flags in the RCFDCnCFDCFSTSk register
RFDC[2:0], RFE: Bits in the RCFDCnCFDRFCCx register
RFMC[7:0], RFEMP, RFIF: Flags in the RCFDCnCFDRFSTSx register
k = 0 to 23, x = 0 to 7

Figure 24.26 FIFO Buffer Reception Timing Chart

(1) When the ID field in a message has been received, the acceptance filter processing starts.

(2) When the message matches the receive rule of the corresponding channel and the message has been successfully received, the routing processing to transfer the message to the specified buffer starts. When the DCE bit in the RCFDCnCFDGCFG register is set to 1 (DLC check is enabled), the DLC filter processing starts at this time.

(3) When the message has passed through the DLC filter processing and the CFE bit in the RCFDCnCFDCFCCk register is 1 (transmit/receive FIFO buffers are used) and the CFDC[2:0] value in the RCFDCnCFDCFCCk register is 001_B or more, the message is stored in the transmit/receive FIFO buffer that is set to receive mode. The CFMC[7:0] value in the RCFDCnCFDCFSTSk register is incremented and becomes 01_H. When the CFIM bit in the RCFDCnCFDCFCCk register is set to 1 (a FIFO receive interrupt request is generated each time a message has been received), the CFRXIF flag in the RCFDCnCFDCFSTSk register is set to 1 (a transmit/receive FIFO receive interrupt request is present). The CFRXIF flag can be reset to 0 by the program.

(4) When the ID field of the next message has been received, the acceptance filter processing starts.

(5) Read received messages from the RCFDCnCFDCFIDk, RCFDCnCFDCFPTRk, and RCFDCnCFDCFDFd_k registers and write FF_H to the RCFDCnCFDCFPCTRk register. This causes the CFMC[7:0] bits in the

RCFDCnCFDCFSTSk register to be decremented. When CFMC[7:0] becomes 00_H, the CFEMP flag in the RCFDCnCFDCFSTSk register becomes 1 (the transmit/receive FIFO buffer contains no message (buffer empty)).

(6) When the message matches the receive rule of the corresponding channel and the message has been successfully received, the routing processing to transfer the message to the specified buffer starts. When the DCE bit in the RCFDCnCFDGCFG register is set to 1 (DLC check is enabled), the DLC filter processing starts at this time.

(7) The message is stored in the transmit/receive FIFO buffer set in receive mode when the message has passed through the DLC filter process if the CFE bit is set to 1 (transmit/receive FIFO buffers are used), and the CFDC[2:0] bits are set to 001_B or more. The CFMC[7:0] bit value is incremented by 1 to be 01_H. When the CFIM bit is set to 1 (an interrupt occurs each time a message has been received), the CFRXIF flag is set to 1 (a transmit/receive FIFO receive interrupt request is present).
The message is stored in the receive FIFO buffer if the RFE bit in the RCFDCnCFDRFCCx register is set to 1 (receive FIFO buffers are used), and the RFDC[2:0] bits in the RCFDCnCFDRFCCx register are set to 001_B or more. The RFMC[7:0] bits in the RCFDCnCFDRFSTSx register are set to 01_H by being incremented by 1. When the RFIM bit in the RCFDCnCFDRFCCx register is set to 1 (an interrupt request occurs each time a message has been received), the RFIF flag in the RCFDCnCFDRFSTSx register is set to 1 (a receive FIFO interrupt request is present).

24.10.2.3 FIFO Buffer Reading Procedure by DMA Transfer

The following FIFO buffers can be read by DMA transfer.

- RH850/F1KH-D8, RH850/F1KM-S4, RH850/F1KM-S2:
  All receive FIFO buffers x (x = 0 to 7)
  RH850/F1KM-S1:
  The receive FIFO buffers x except for the following (x = 0 to 7)
  The receive FIFO buffer x DMA enable (RCFDCnCFDCDTCT) and the receive FIFO buffer x DMA status (RCFDCnCFDCDTSTS) (x = 0 to 5)
- The first transmit/receive FIFO buffer k allocated to channel m (k = 3 × m, m = 0 to 7)

The DMA enable bit (RFDMAEx or CFDMAEm bit in the RCFDCnCFDCDTCT register) can be set at any time. However, before setting the DMA enable bit to 1 (to enable DMA transfer requests), set the receive interrupt enable bit (RFIE bit in the RCFDCnCFDRFCCx register or CFRXIE bit in the RCFDCnCFDCFCCk register) of related FIFO buffers to 0 (to disable interrupts). When DMA transfer requests are enabled, do not write a value to the FIFO control register (RCFDCnCFDRFCCx register or RCFDCnCFDCFCCk register).

When an unread message is remaining in a DMA transfer-enabled FIFO buffer, a DMA transfer request trigger is generated. Specify the address of the FIFO access register address*[1] for the transfer source address, and adjust the transfer size so that data can be read to the end of the payload storage area with a single trigger. The end of the payload storage area depends on the payload storage size specified by the RFPLS[2:0] bits in the RCFDCnCFDRFCCx register or the CFPLS[2:0] bits in the RCFDCnCFDCFCCk register.

After the end of the payload stored in the FIFO buffer has been read, the RFMC[7:0] value in the RCFDCnCFDRFSTSx register or the CFMC[7:0] value in the RCFDCnCFDCFSTSk register is automatically decremented by 1. After that, if an unread message is remaining in the FIFO buffer, a trigger is generated again.

When the RFDMAEx or CFDMAEm bit is set to 0 (to disable DMA transfer requests) during DMA transfer, wait until the DMA transfer status (RFDMASTSx or CFDMASTSm bit in the RCFDCnCFDCDTSTS register) is cleared to 0 (DMA transfer disabled), and then start the next processing (enabling DMA transfer again etc.). When disabling DMA transfer, examine how to process a message remaining in the FIFO buffer and a newly arriving message. When the FIFO buffer is enabled, it continues to receive messages.

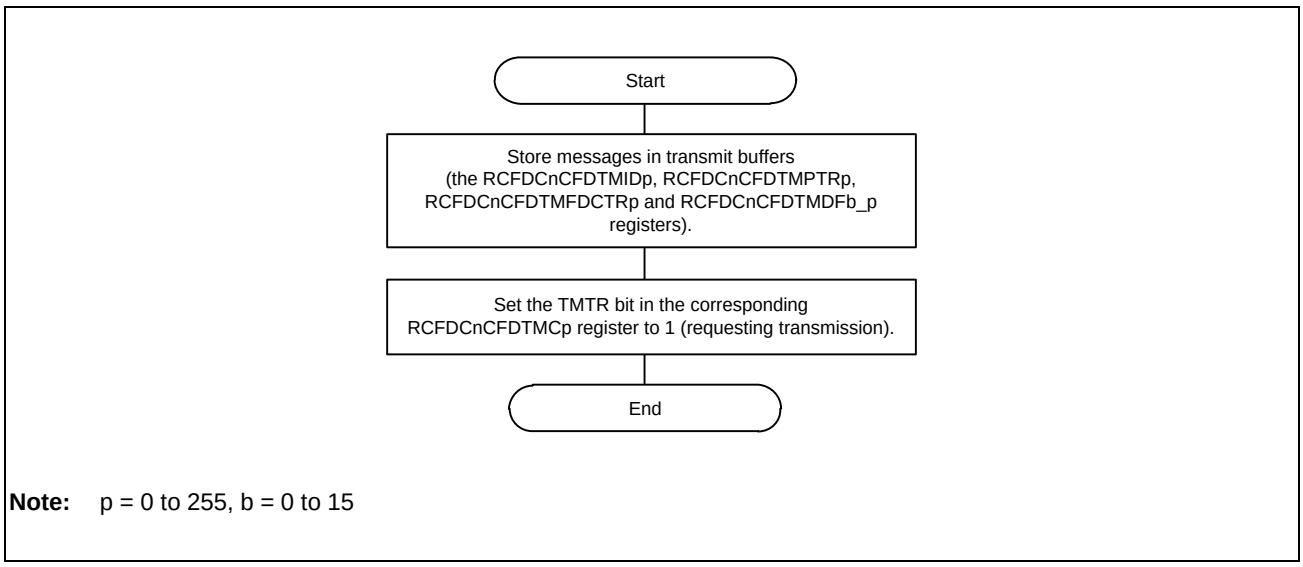
Note 1.
- Receive FIFO buffer
  RCFDCnCFDRFIDx, RCFDCnCFDRFPTRx, RCFDCnCFDRFFDSTSx, RCFDCnCFDRFDFd_x
- Transmit/Receive FIFO buffer
  RCFDCnCFDCFIDk, RCFDCnCFDCFPTRk, RCFDCnCFDCFFDCSTSk, RCFDCnCFDCFDFd_k

24.10.3 Transmission Procedure

24.10.3.1 Procedure for Transmission from Transmit Buffers

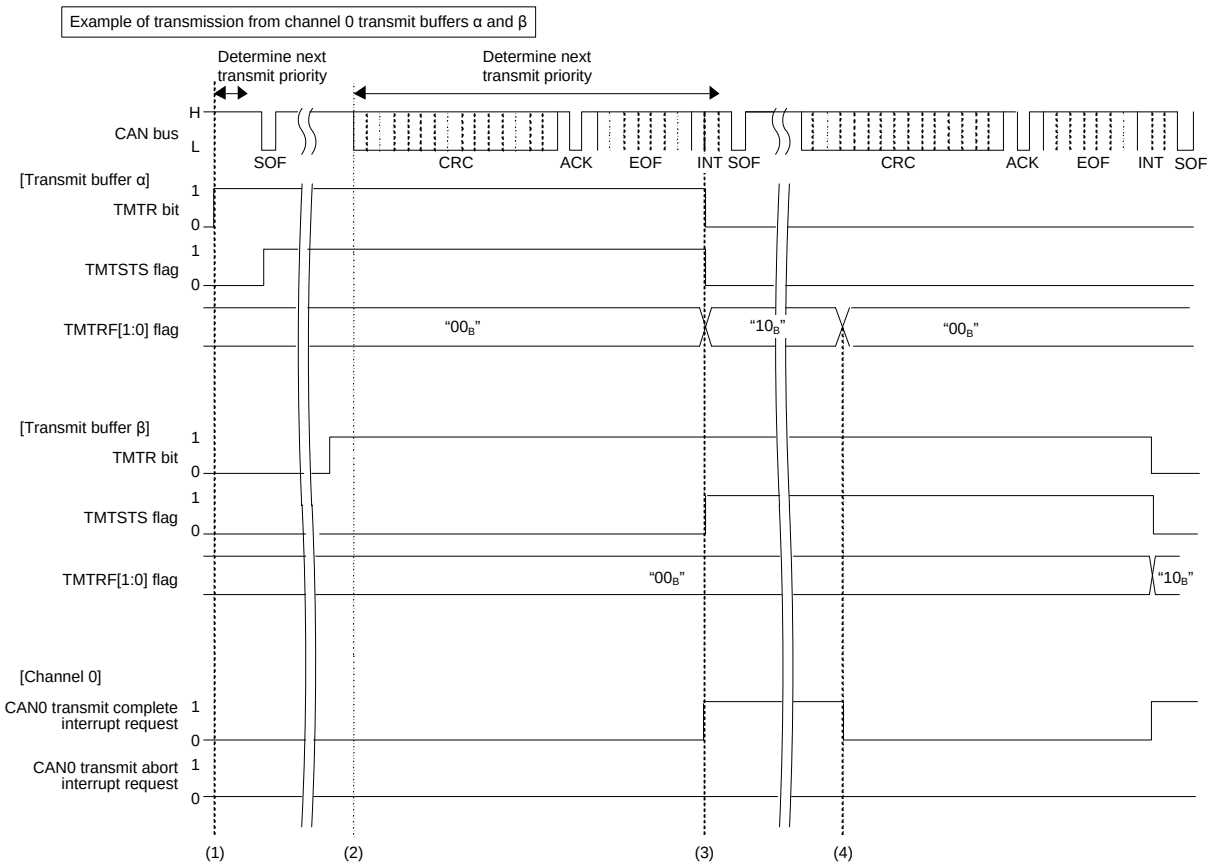
Figure 24.27, Procedure for Transmission from Transmit Buffers shows the procedure for transmission from transmit buffers.

Figure 24.28, Transmit Buffer Transmission Timing Chart (Transmission Completed Successfully) shows a timing chart where messages are transmitted from two transmit buffers in the same channel and transmission has been successfully completed. **Figure 24.29, Transmit Buffer Transmission Timing Chart (Transmit Abort Completed)** shows a timing chart where messages are transmitted from two transmit buffers in the same channel and transmit abort has been completed.



Note: p = 0 to 255, b = 0 to 15

Figure 24.27 Procedure for Transmission from Transmit Buffers



Note: α = 0 to 31, β = 0 to 31
TMTR: Bit in the RCFDCnCFDTMCp register
TMTSTS, TMTRF[1:0]: Flags in the RCFDCnCFDTMSTSp register

Figure 24.28 Transmit Buffer Transmission Timing Chart (Transmission Completed Successfully)

(1) When the TMTR bit in the RCFDCnCFDTMCα register is set to 1 while the CAN bus is idle, the transmit priority determination processing starts to determine the highest-priority transmit buffer. If transmit buffer α is determined to be the highest-priority transmit buffer, the TMTSTS flag in the corresponding RCFDCnCFDTMSTSα register is set to 1 (transmission is in progress) and the CAN channel starts transmitting data.

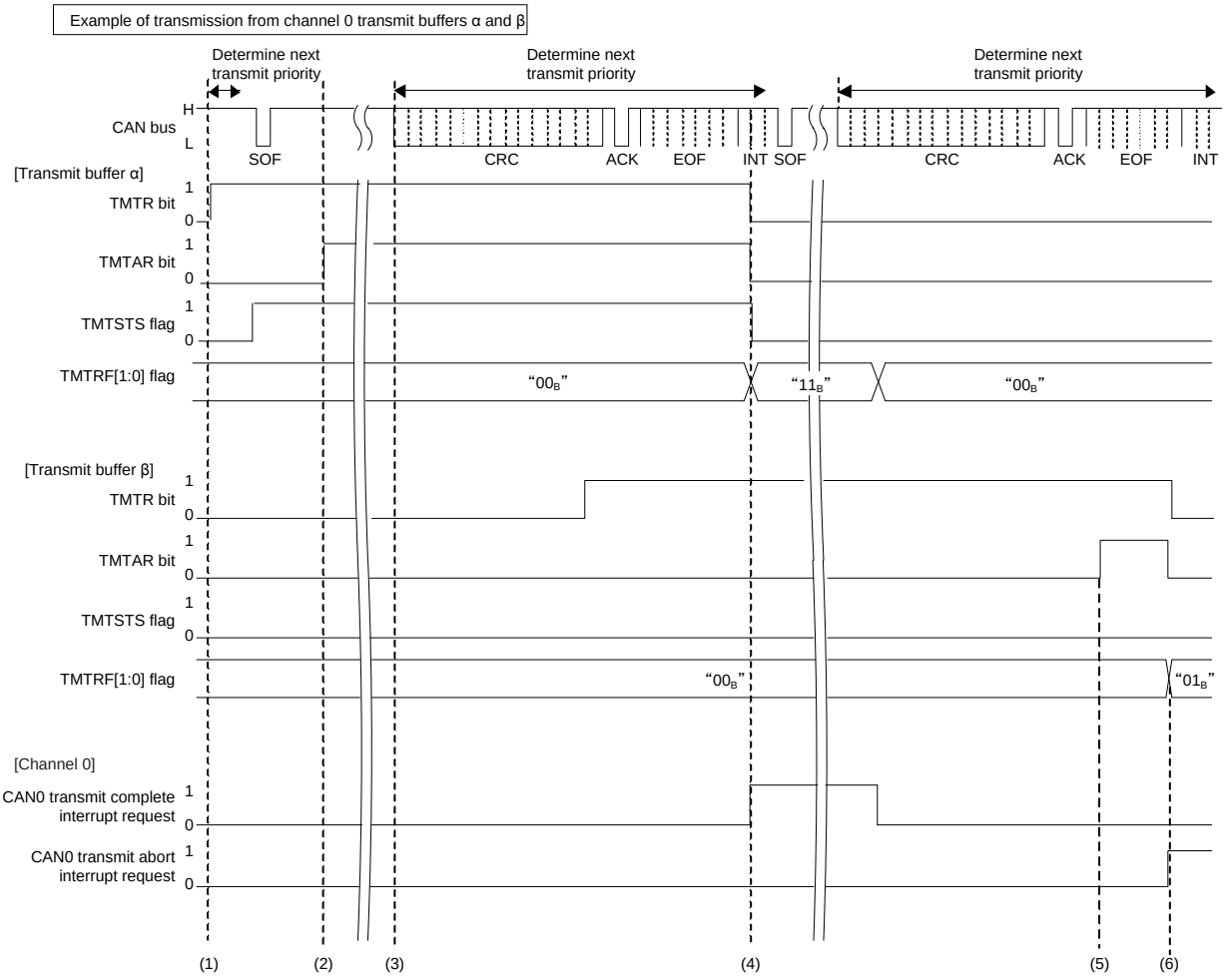
(2) When a transmit request from a buffer is present, the priority determination starts at the first bit of CRC field for the next transmission. The determination time may delay if the transmit priority determination processing is performed on another channel. However, the delay does not occur between transmissions because the determination processing is completed by the third bit of the intermission.

(3) When transmission completes successfully, the TMTRF[1:0] flag in the RCFDCnCFDTMSTSα register is set to 10_B (transmission has been completed (without transmit abort request)) and the TMTSTS flag and the TMTR bit in the RCFDCnCFDTMCα register are cleared to 0. When the TMIEα bit in the RCFDCnCFDTMIEC0 register is 1 (transmit buffer interrupt is enabled), a CAN0 transmit complete interrupt request is generated. To clear the interrupt request, set the TMTRF[1:0] flag to 00_B (transmission is in progress or no transmit request is present).

(4) Before starting the next transmission, set the TMTRF[1:0] flag to 00_B. Write the next message to the transmit buffer, and then set the TMTR bit to 1 (transmission is requested). The TMTR bit can be set to 1 only when the TMTRF[1:0] flag value is 00_B.

If an arbitration-lost occurs after transmission is started, the TMTSTS flag is cleared to 0. The transmit priority determination is reexecuted at the beginning of the CRC field to search the highest- priority transmit buffer. If an error has occurred during transmission or after arbitration loss, the priority determination processing is reexecuted during transmission of an error frame.

When a 2-bit ECC error is detected during the priority determination processing, no data is transmitted.



Note: α = 0 to 31, β = 0 to 31
TMTR, TMTAR: Bits in the RCFDCnCFDTMCp register
TMTSTS, TMTRF[1:0]: Flags in the RCFDCnCFDTMSTSp register

Figure 24.29 Transmit Buffer Transmission Timing Chart (Transmit Abort Completed)

(1) When the TMTR bit in the RCFDCnCFDTMCα register is set to 1 while the CAN bus is idle, the transmit priority determination processing starts to determine the highest-priority transmit buffer. If transmit buffer α is determined to be the highest-priority transmit buffer, the TMTSTS flag in the corresponding RCFDCnCFDTMSTSα register is set to 1 (transmission is in progress) and the CAN channel starts transmitting data.

(2) When it is determined that the transmit buffer is used for the next transmission or transmission is in progress, message transmission is not aborted unless an error or arbitration loss occurs even if the TMTAR bit is set to 1 (transmit abort is requested).

(3) The priority determination starts at the first bit of the CRC field for the next transmission. In this timing chart, buffer β is not selected as the next transmit buffer. The determination time may delay if the transmit priority determination processing is performed on another channel. However, the delay does not occur during transmission because the determination processing is completed by the third bit of the intermission.

(4) When transmission completes successfully, the TMTRF[1:0] flag in the RCFDCnCFDTMSTSα register is set to 11_B (transmission has been completed (with transmit abort request)) and the TMTSTS flag and the TMTR bit in the RCFDCnCFDTMCα register are cleared to 0. When the TMIEα value in the RCFDCnCFDTMIEC0 register is 1 (transmit buffer interrupt is enabled), a CAN0 transmit complete interrupt request is generated. To clear the interrupt request, set the TMTRF[1:0] flag to 00_B (transmission is in progress or no transmit request is present).

(5) While another CAN node is transmitting data on the CAN bus (TMTSTS flag = 0), if the TMTAR bit is set to 1 while the corresponding channel is determining transmit priority, the TMTR bit cannot be cleared to 0.

(6) After the internal processing time has passed, the transmission is terminated and the TMTRF[1:0] flag is set to 01_B. When the transmit buffer is not transmitting data and is not selected as the next transmit buffer and priority determination is not being made, an abort request is immediately accepted and the TMTRF[1:0] flag is set to 01_B. At this time, the TMTR and TMTAR bits are cleared to 0. When transmit abort is completed with the TAIE bit in the RCFDCnCFDCmCTR register set to 1 (transmit abort interrupt is enabled), an interrupt request is generated. To clear the interrupt request, set the TMTRF[1:0] flag to 00_B.

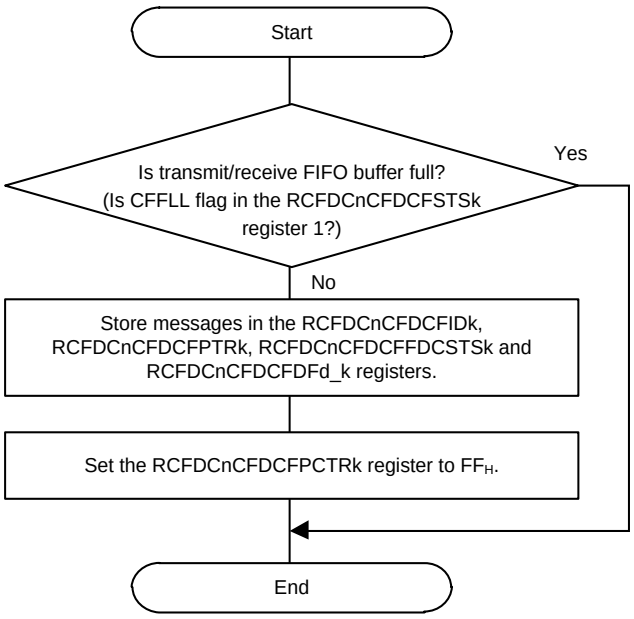
If an arbitration loss occurs after the CAN channel started transmission, the TMTSTS bit is cleared to 0. The transmit priority determination is reexecuted at the beginning of the CRC field to search the highest-priority transmit buffer. If an error has occurred during transmission or after arbitration loss, the priority determination processing is reexecuted during transmission of an error frame.

When a 2-bit ECC error is detected during the priority determination processing, no data is transmitted.

24.10.3.2 Procedure for Transmission from Transmit/Receive FIFO Buffers

Figure 24.30, Procedure for Transmission from Transmit/Receive FIFO Buffers shows the procedure for transmission from transmit/receive FIFO buffers.

Figure 24.31, Transmit/Receive FIFO Buffer Transmission Timing Chart (Transmission Completed Successfully) shows a timing chart where messages are transmitted from two transmit/receive FIFO buffers in the same channel and transmission has been successfully completed. **Figure 24.32, Transmit/Receive FIFO Buffer Transmission Timing Chart (Transmit Abort Completed)** shows a timing chart where messages are transmitted from two transmit/receive FIFO buffers in the same channel and transmit abort has been completed.



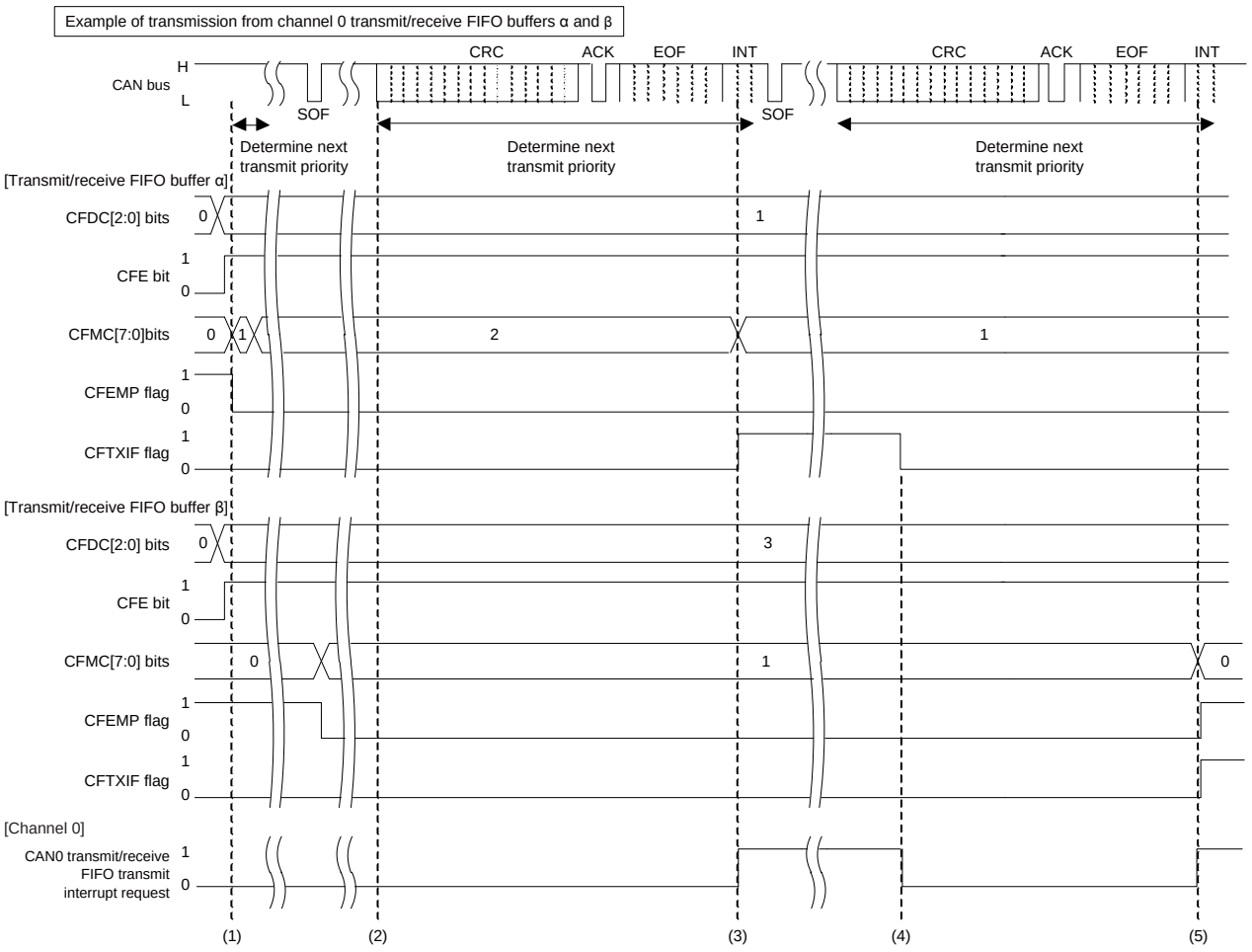
Note: k = 0 to 23, d = 0 to 15

Figure 24.30 Procedure for Transmission from Transmit/Receive FIFO Buffers

When storing a message, do not write a value to the RCFDCnCFDCFDFd_k register corresponding to the area exceeding the payload storage size specified by the CFPLS[2:0] bits in the RCFDCnCFDCFCCk register.

Table 24.129 Payload Storage Area of Transmit/Receive FIFO Buffer

Set CFPLS[2:0] Value	Payload Storage Size	Corresponding Data Field Registers
000_B	8 bytes	RCFDCnCFDCFDF0_k to RCFDCnCFDCFDF1_k
001_B	12 bytes	RCFDCnCFDCFDF0_k to RCFDCnCFDCFDF2_k
010_B	16 bytes	RCFDCnCFDCFDF0_k to RCFDCnCFDCFDF3_k
011_B	20 bytes	RCFDCnCFDCFDF0_k to RCFDCnCFDCFDF4_k
100_B	24 bytes	RCFDCnCFDCFDF0_k to RCFDCnCFDCFDF5_k
101_B	32 bytes	RCFDCnCFDCFDF0_k to RCFDCnCFDCFDF7_k
110_B	48 bytes	RCFDCnCFDCFDF0_k to RCFDCnCFDCFDF11_k
111_B	64 bytes	RCFDCnCFDCFDF0_k to RCFDCnCFDCFDF15_k



Note: α = 0 to 2, β = 0 to 2
CFDC[2:0],CFE: Bits in the RCFDCnCFDCFCCk register
CFMC[7:0], CFEMP, CFTXIF: Flags in the RCFDCnCFDCFSTSk register

Figure 24.31 Transmit/Receive FIFO Buffer Transmission Timing Chart (Transmission Completed Successfully)

(1) While the CAN bus is idle, when the CFE bit in the RCFDCnCFDCFCCα register is 1 (transmit/receive FIFO buffers are used) and the CFDC[2:0] value in the RCFDCnCFDCFCCα register is 001_B (4 messages) or more and the CFMC[7:0] value in the RCFDCnCFDCFSTSα register is 01_H or more, the priority determination processing starts to determine the highest-priority transmit message. When the highest-priority transmit message has been determined, transmission of the message starts. In this figure, the message is transmitted from transmit/receive FIFO buffer α of channel 0.

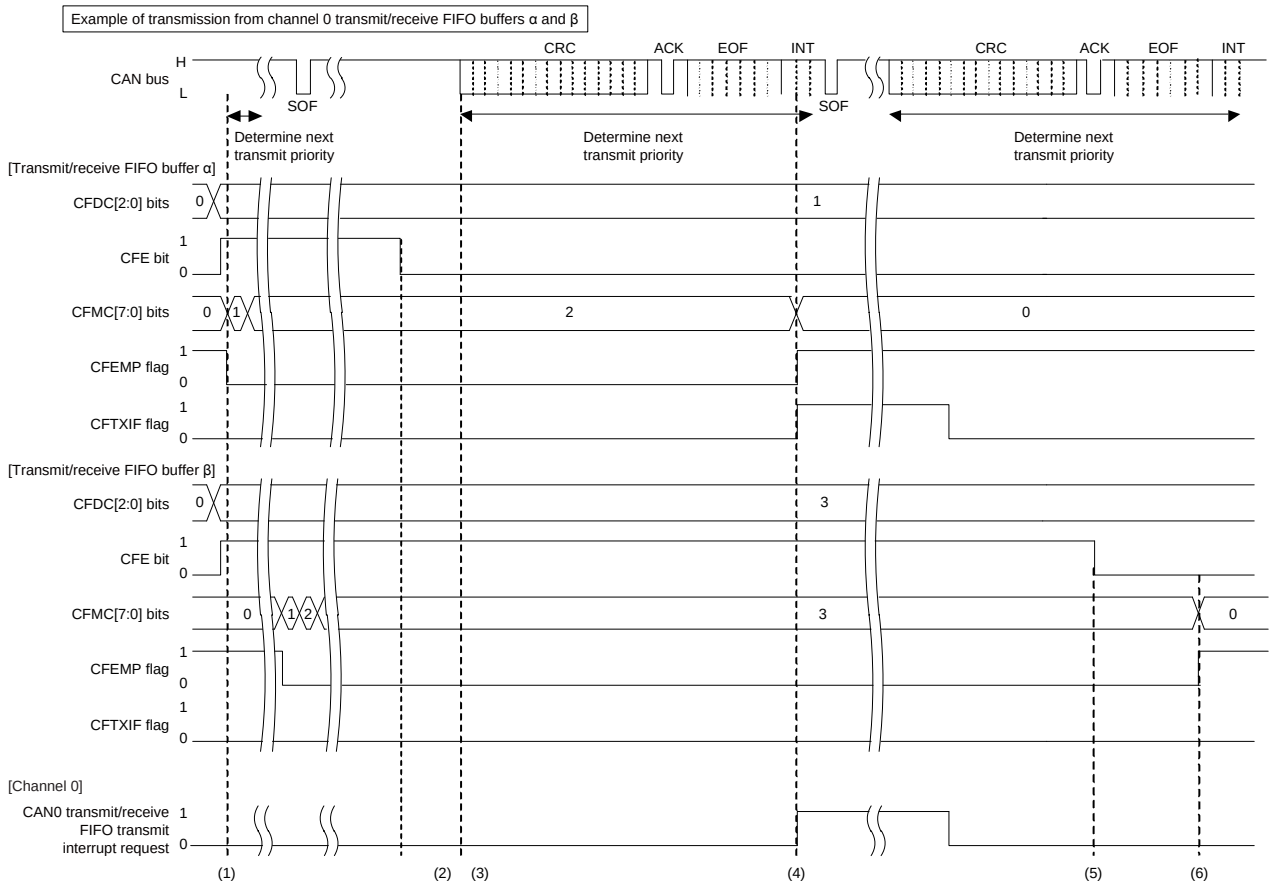
(2) When a transmit request from a buffer is present, the priority determination starts at the first bit of the CRC field for the next transmission. The determination time may delay if the transmit priority determination processing is performed on another channel. However, the delay does not occur during transmission because the determination processing is completed by the third bit of the intermission.

(3) When transmission completes successfully, the CFMC[7:0] value in the RCFDCnCFDCFSTSα register is decremented by 1. Setting the CFIM bit in the RCFDCnCFDCFCCα register to 1 (a FIFO transmit interrupt request is generated each time a message has been transmitted) sets the CFTXIF flag in the RCFDCnCFDCFSTSα register to 1 (a transmit/receive FIFO transmit interrupt request is present).

(4) The program can clear the CFTXIF flag.

(5) Message transmission from transmit/receive FIFO buffer β of channel 0 completes and the CFMC[7:0] value in the RCFDCnCFDCFSTSβ register is decremented by 1. The CFMC[7:0] bits are cleared to 00_H and therefore the CFEMP flag in the RCFDCnCFDCFSTSβ register is set to 1 (the transmit/receive FIFO buffer contains no message (buffer empty)).

Transmission is continued until the CFEMP flag is set to 1. It is possible to continuously store transmit messages in FIFO buffers until the CFFLL flag in the RCFDCnCFDCFSTSα and RCFDCnCFDCFSTSβ registers is set to 1 (the transmit/receive FIFO buffer is full).



Note: α = 0 to 2, β = 0 to 2
CFDC[2:0], CFE: Bits in the RCFDCnCFDCFCCk register
CFMC[7:0], CFEMP, CFTXIF: Flags in the RCFDCnCFDCFSTSk register

Figure 24.32 Transmit/Receive FIFO Buffer Transmission Timing Chart (Transmit Abort Completed)

(1) While the CAN bus is idle, when the CFE bit in the RCFDCnCFDCFCCα register is 1 (transmit/receive FIFO buffers are used) and the CFDC[2:0] value in the RCFDCnCFDCFCCα register is 001_B (4 messages) or more and the CFMC[7:0] value in the RCFDCnCFDCFSTSα register is 01_H or more, the priority determination processing starts to determine the highest-priority transmit message. When the highest-priority transmit message has been determined, transmission of the message starts. In this figure, the message is transmitted from transmit/receive FIFO buffer α of channel 0.

(2) When transmission is in progress or it is determined that the transmit/receive FIFO buffer is used for the next transmission, message transmission is not aborted unless an error or arbitration loss occurs even if the CFE bit is set to 0 (no transmit/receive FIFO buffer is used).

(3) When a transmit request from a buffer is present, the priority determination starts at the first bit of the CRC field for the next transmission. In this figure, transmit/receive FIFO buffer β is not selected as a buffer for the next transmission. The determination time may delay if the transmit priority determination processing is performed on another channel. However, the delay does not occur during transmission because the determination processing is completed by the third bit of the intermission.

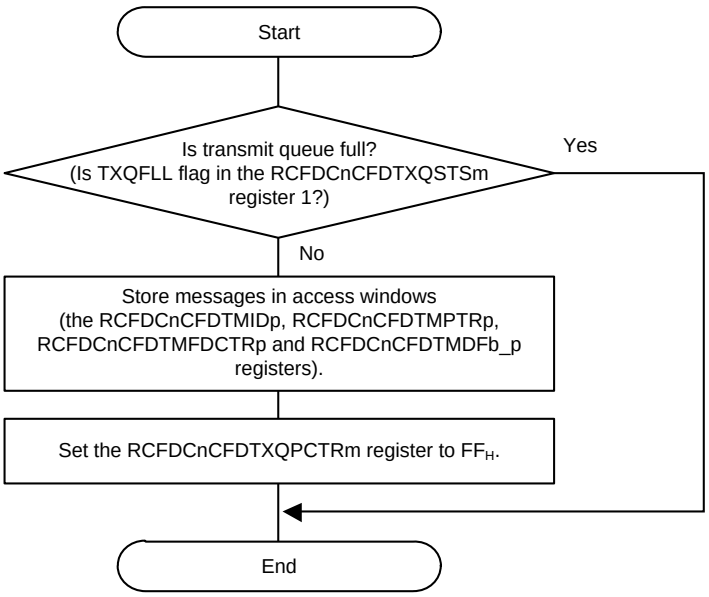
(4) When transmit completes successfully, the CFMC[7:0] value is cleared to 00_H. Setting the CFIM bit to 1 (a FIFO transmit interrupt request is generated each time a message has been transmitted) sets the CFTXIF flag in the RCFDCnCFDCFSTSα register to 1 (a transmit/receive FIFO transmit interrupt request is present). The program can clear the CFTXIF flag.

(5) If another CAN node on the CAN bus is transmitting data (not from transmit/receive FIFO buffer β), transmit/receive FIFO buffers β cannot be disabled immediately even if the CFE bit in the RCFDCnCFDCFCCβ register is cleared to 0 (no transmit/receive FIFO buffer is used) during transmit priority determination. (The CFEMP flag in the RCFDCnCFDCFSTSβ register is not set to 1 (the transmit/receive FIFO buffer contains no message (buffer empty)) immediately.)

(6) After the internal processing time has passed, transmit/receive FIFO buffers β are disabled and the CFMC[7:0] bits in the RCFDCnCFDCFSTSβ register are cleared to 00_H and the CFEMP flag is set to 1. When the transmit/receive FIFO buffer β is not transmitting data and is not selected as the next transmit buffer and priority determination is not in progress, the transmit/receive FIFO buffer β is immediately disabled. (The CFMC[7:0] bits are cleared to 00_H and the CFEMP flag is set to 1.)

24.10.3.3 Procedure for Transmission from the Transmit Queue

Figure 24.33, Procedure for Transmission from the Transmit Queue shows the procedure for transmission from the transmit queue.



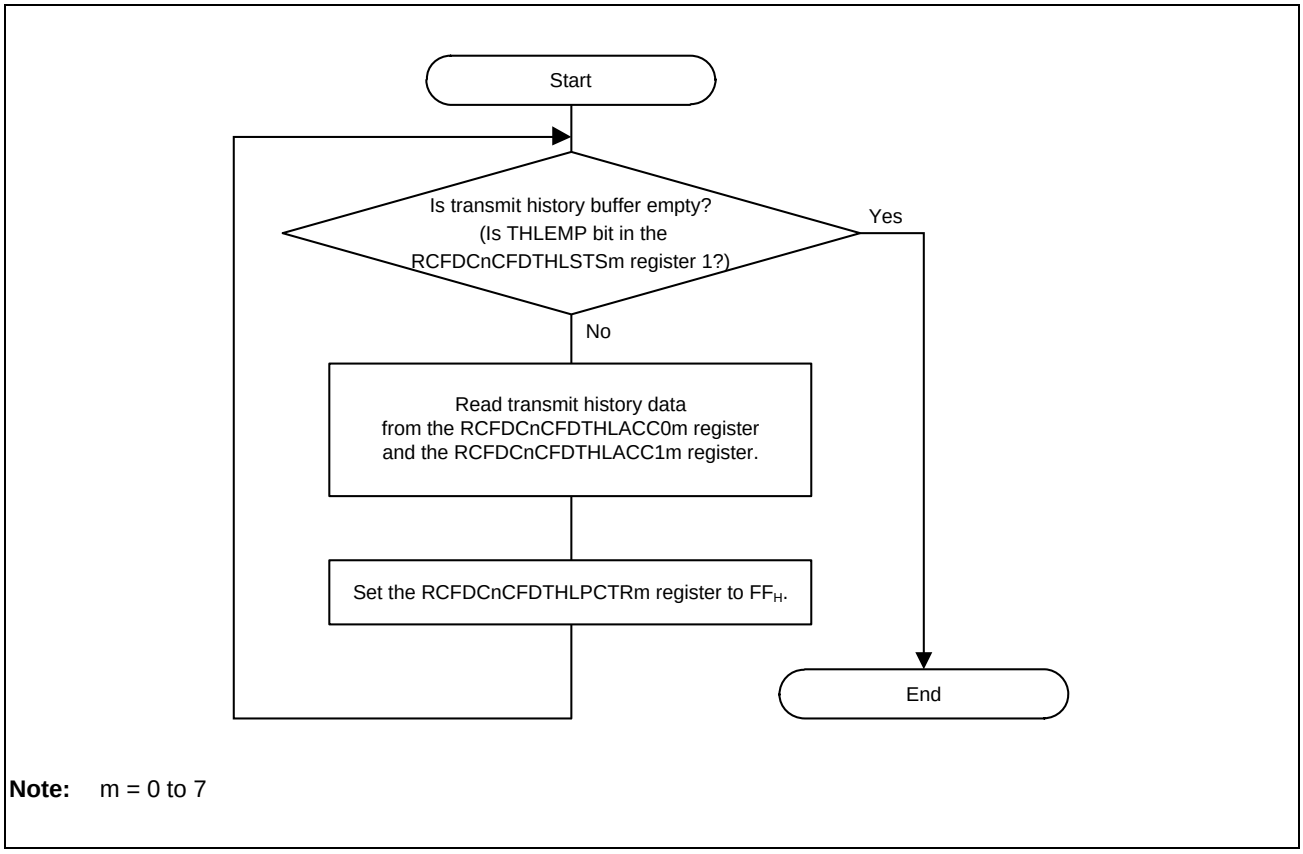
Note: p = m × 32 + 31, m = 0 to 7

Figure 24.33 Procedure for Transmission from the Transmit Queue

24.10.3.4 Transmit History Buffer Reading Procedure

Transmit history data can be read from the RCFDCnCFDTHLACC0m register and the RCFDCnCFDTHLACC1m register.

The next data can be accessed by writing FF_H to the corresponding RCFDCnCFDTHLPCTRm register (m = 0 to 7) after reading a set of data. **Figure 24.34, Transmit History Buffer Reading Procedure** shows the transmit history buffer reading procedure.



Note: m = 0 to 7

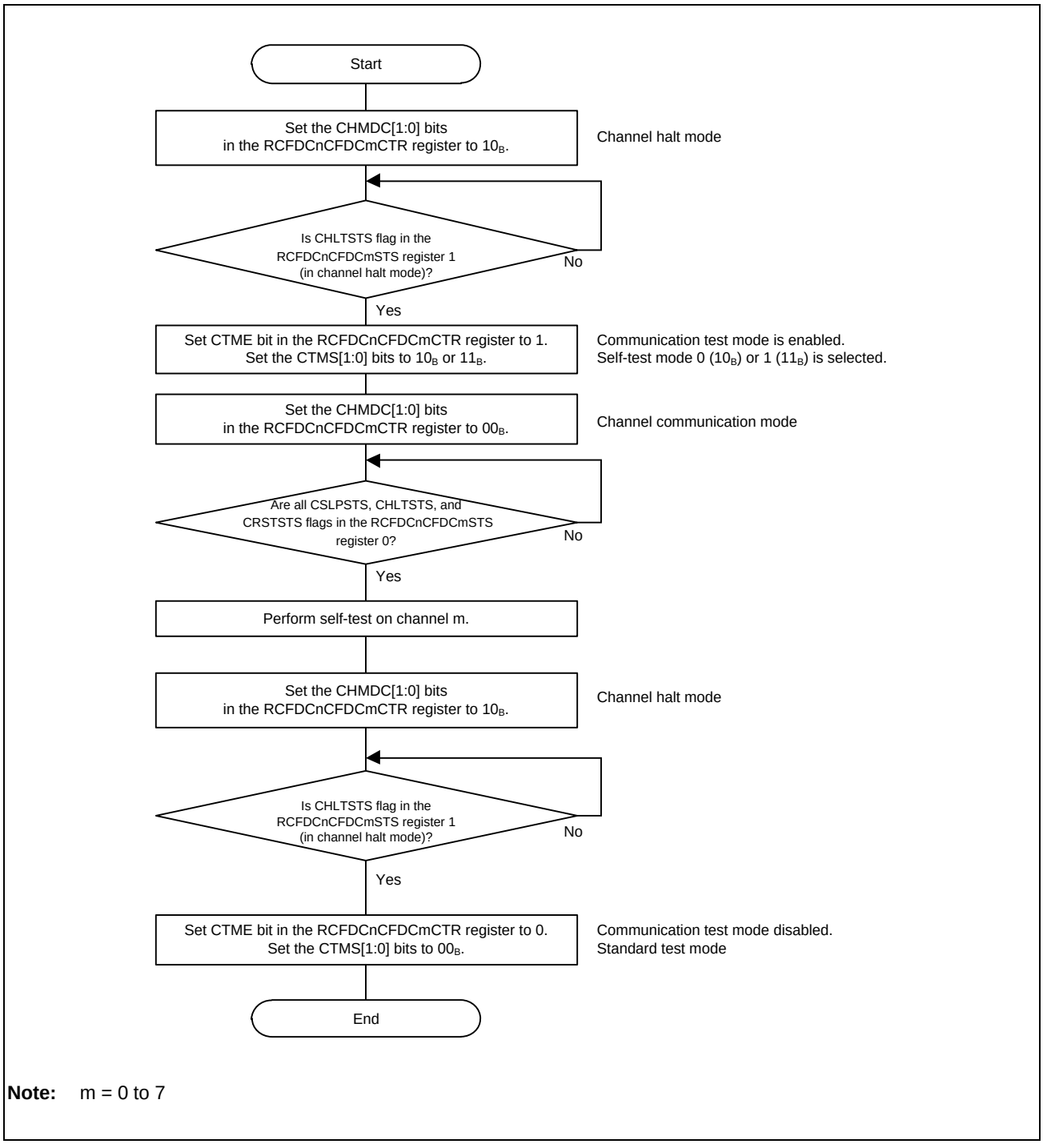
Figure 24.34 Transmit History Buffer Reading Procedure

24.10.4 Test Settings

24.10.4.1 Self-Test Mode Setting Procedure

Self-test mode allows communication test on a channel basis by enabling a CAN node to receive its own transmitted messages.

Figure 24.35, Self-Test Mode Setting Procedure shows the self-test mode setting procedure.



Note: m = 0 to 7

Figure 24.35 Self-Test Mode Setting Procedure

24.10.4.2 Procedure for Releasing the Protection

Since the global test function in **Table 24.130, Protection Release Data for Test Function** is protected, write the protection release data 1 and release data 2 in succession to the LOCK[15:0] bits in the RCFDCnCFDGLOCKK register, then set the target test bit to 1.

Table 24.130 Protection Release Data for Test Function

Test Function	Protection Release Data 1	Protection Release Data 2	Target Bit
RAM test	7575_H	$8A8A_H$	RTME bit in the RCFDCnCFDGTSTCTR register

If an incorrect value is written to the LOCK[15:0] bits, restart from writing the protection release data1.
Figure 24.36, Protection Release Procedure shows the procedure for releasing the protection.

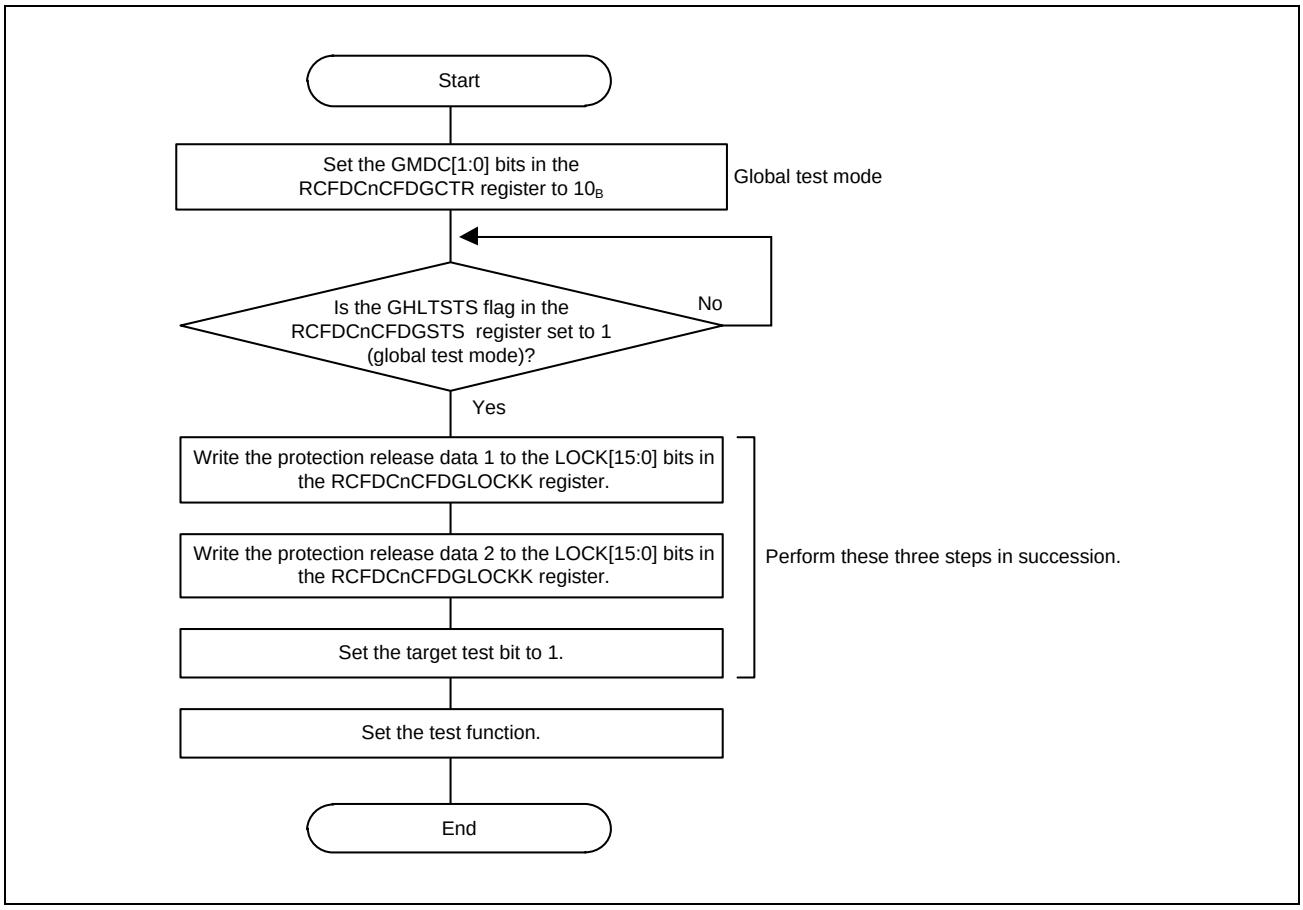
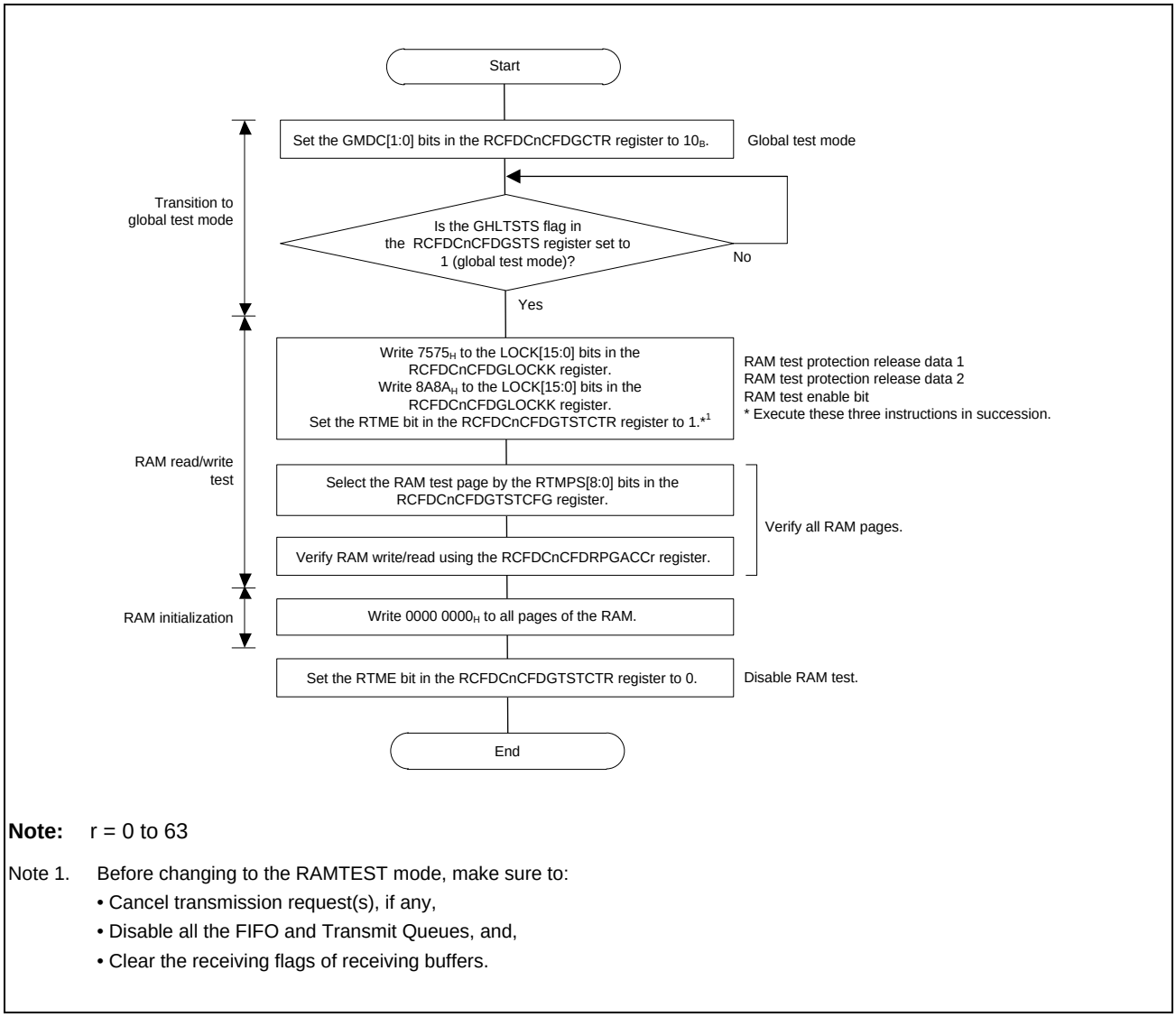


Figure 24.36 Protection Release Procedure

24.10.4.3 RAM Test Setting Procedure

RAM tests include CAN RAM read/write test. The read/write test verifies that data written to the RAM is read correctly. Before ending the RAM test, write 0000 0000_H to all pages of the CAN RAM.

Figure 24.37, RAM Test Setting Procedure shows the RAM test setting procedure.



Note: r = 0 to 63

Note 1. Before changing to the RAMTEST mode, make sure to:
- Cancel transmission request(s), if any,
- Disable all the FIFO and Transmit Queues, and,
- Clear the receiving flags of receiving buffers.

Figure 24.37 RAM Test Setting Procedure

24.10.4.4 Inter-Channel Communication Test Setting Procedure

Communication testing can be performed by transmitting and receiving data between different channels.

Figure 24.38, Inter-Channel Communication Test Setting Procedure (Example of Communication Test between Channel 0 and Channel 1) shows the inter-channel communication test setting procedure.

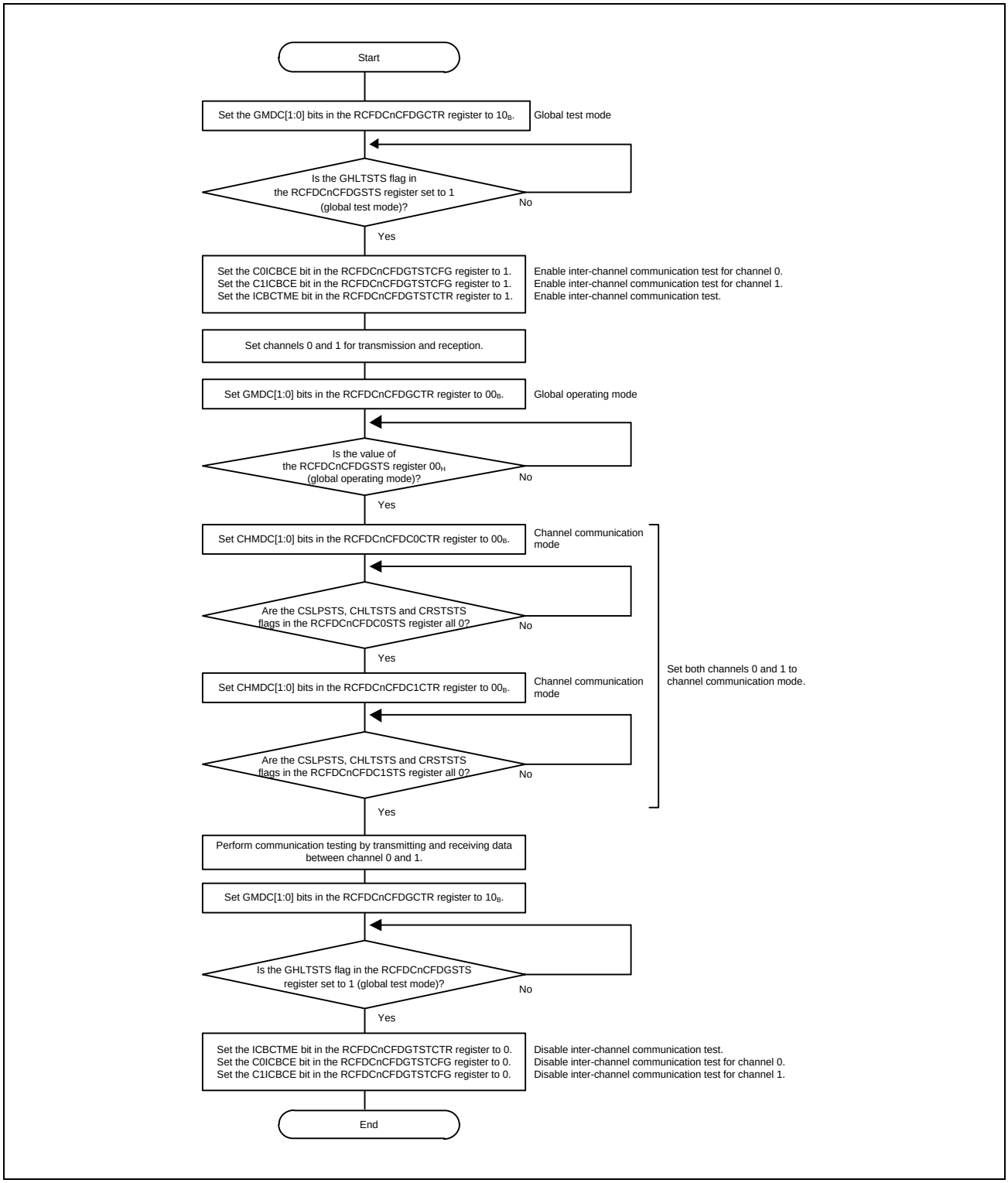


Figure 24.38 Inter-Channel Communication Test Setting Procedure (Example of Communication Test between Channel 0 and Channel 1)

24.11 Notes on the RS-CANFD Module

- When changing a global mode, check the GSLPSTS, GHLTSTS, and GRSTSTS flags in the RCFDCnCFDGSTS register for transitions. When changing a channel mode, check the CSLPSTS, CHLTSTS, and CRSTSTS flags in the RCFDCnCFDCmSTS register (m = 0 to 7) for transitions.
- When only classical CAN frames are used in CAN FD mode, set the RCFDCnCFDCmDCFG register to the value equal to the set RCFDCnCFDCmNCFG register value.
- The acceptance filter processing checks receive rules sequentially in ascending order from the smallest rule number. If the same ID, IDE bit, or RTR bit value is set for multiple receive rules, the smallest number of receive rule is used for the acceptance filter processing. If the message does not pass through the subsequent DLC filter processing, the data processing is terminated without returning to the acceptance filter processing and the message is not stored in the buffer.
- When linking transmit buffers to transmit/receive FIFO buffers or allocating transmit buffers to transmit queues, set the control register (RCFDCnCFDTMCp) of the corresponding transmit buffer to 00_H. The status register (RCFDCnCFDTMSTSp) of the corresponding transmit buffer should not be used. Flags in other status registers (registers RCFDCnCFDTMTRSTS0 to RCFDCnCFDTMTRSTS7, RCFDCnCFDTMTARSTS0 to RCFDCnCFDTMTARSTS7, RCFDCnCFDTMTCSTS0 to RCFDCnCFDTMTCSTS7, and RCFDCnCFDTMTASTS0 to RCFDCnCFDTMTASTS7), which correspond to transmit buffers linked to transmit/receive FIFO buffers or allocated to transmit queues remain unchanged. Set the enable bit in the corresponding interrupt enable register (registers RCFDCnCFDTMIEC0 to RCFDCnCFDTMIEC7) to 0 (transmit buffer interrupt is disabled).
- Only a single transmit/receive FIFO buffer can be linked to a transmit buffer. Do not link two or more transmit/receive FIFO buffers to transmit buffers of the same number.
- When the CANm bit time clock is selected as a timestamp counter clock source, the timestamp counter stops when the corresponding channel has transitioned to channel reset mode or channel halt mode.
- In case of an attempt to store a newly received message when the receive FIFO buffer and the transmit/receive FIFO buffer are full, the new message is discarded. If you wish to store a new transmit message in the transmit/receive FIFO buffer or the transmit queue, check that the transmit/receive FIFO buffer or the transmit queue is not full.
- In the case of registers that access the RAM, the value after reset shown in **Section 24.3, Registers** indicate the values cleared by initialization of the CAN RAM. Values before clear are undefined. The following registers apply.
  - Receive rule (RCFDCnCFDGAFLIDj, RCFDCnCFDGAFLMj, RCFDCnCFDGAFLP0_j, RCFDCnCFDGAFLP1_j registers)
  - Receive buffers (RCFDCnCFDRMIDq, RCFDCnCFDRMPTRq, RCFDCnCFDRMFDSTSq, RCFDCnCFDRMDFb_q registers)
  - Receive FIFO buffer access registers (RCFDCnCFDRFIDx, RCFDCnCFDRFPTRx, RCFDCnCFDRFFDSTSx, and RCFDCnCFDRFDFd_x registers)
  - Transmit/receive FIFO buffer access registers (RCFDCnCFDCFIDk, RCFDCnCFDCFPTRk, RCFDCnCFDCFFDCSTSk, and RCFDCnCFDCFDFd_k registers)
  - Transmit buffers (RCFDCnCFDTMIDp, RCFDCnCFDTMPTRp, RCFDCnCFDTMFDCTRp, and RCFDCnCFDTMDFb_p registers)
  - Transmit history access registers (RCFDCnCFDTHLACC0m, RCFDCnCFDTHLACC1m registers)
  - RAM test page access register (RCFDCnCFDRPGACCr register)

- The values of unused receive buffers (RCFDCnCFDRMIDq, RCFDCnCFDRMPTRq, RCFDCnCFDRMFDSTSq, and RCFDCnCFDRMDFb_q registers), receive FIFO buffer access registers (RCFDCnCFDRFIDx, RCFDCnCFDRFPTRx, RCFDCnCFDRFFDSTSx, and RCFDCnCFDRFDFd_x registers) and transmit/receive FIFO buffer access registers (RCFDCnCFDCFIDk, RCFDCnCFDCFPTRk, RCFDCnCFDCFFDCSTSk, and RCFDCnCFDCFDFd_k registers) are undefined when the RS-CANFD module transitions to global operation mode or global test mode after exiting from global reset mode.

24.12 Detection and Correction of Errors in RS-CANFD RAM

For details of ECC, see **Section 40A.2.6, ECC for Peripheral RAM**, **Section 40B.2.6, ECC for Peripheral RAM**, **Section 40C.2.5, ECC for Peripheral RAM**.