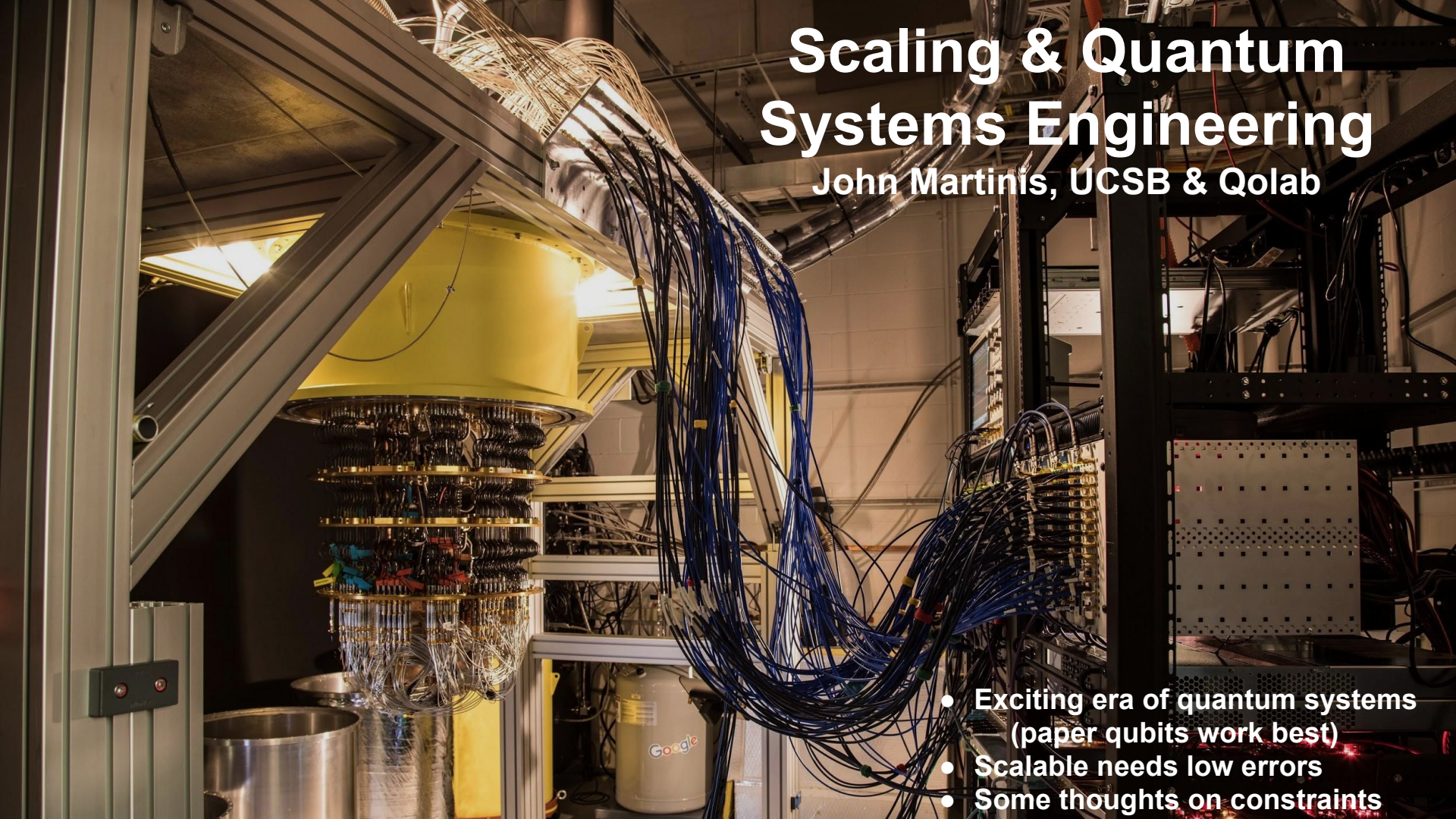
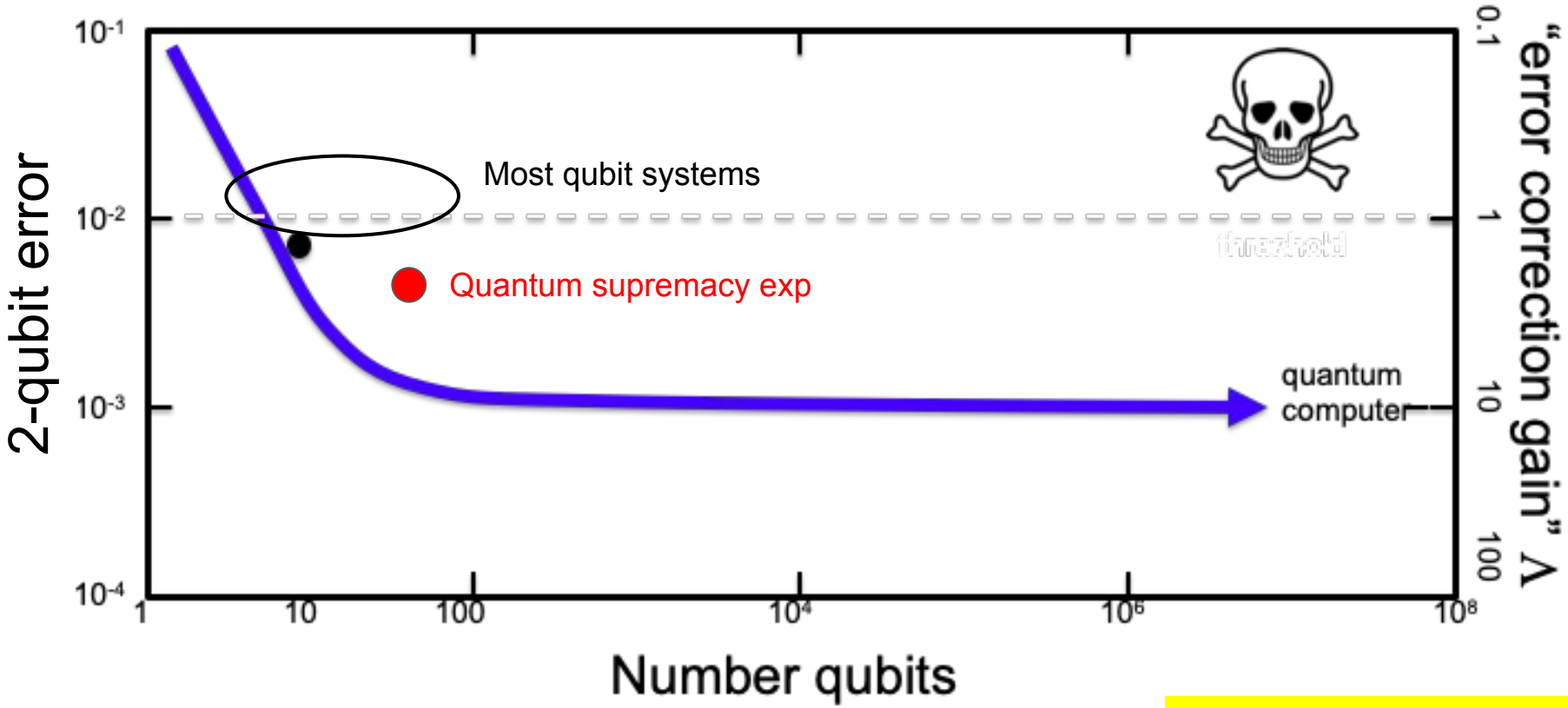


Scaling & Quantum Systems Engineering

John Martinis, UCSB & Qolab

- Exciting era of quantum systems (paper qubits work best)
- Scalable needs low errors
- Some thoughts on constraints

Progress Towards Error Correction (Scaling)



In same device:
more qubits and connectivity, lower errors

Need to specify average, not hero gates

Qubit Control

Analog control
Optimal (shaped) waveforms

After years of research, errors ~1%
Typically degrade for array
No error tradeoffs to simplify control

Sycamore array: 2-qubit gates 0.6%
Improve coherence time, control
Retain control flexibility

Need complex control
Thy: 2 param's/gate
Exp: 100 param's/qubit

Information complexity
1 Gs/s shaped waveform
10kB waveform memory

Scaling of control uses CMOS

Outline

1) Quantum Systems Engineering - tradeoffs
2) Error correction - surface code
3) Technical readiness level - maturity
4) Software and scaling
5) Scalable control system - info. constraints, size
6) Testing - 40% of effort

    (Cloud services as system testing)

    System benchmarking - XEB

    Surface code experiment

Quantum Systems Engineering

- For one device, qubits have
  - Coherence
  - Coupling
  - Measurement
  - Low errors

competing requirements

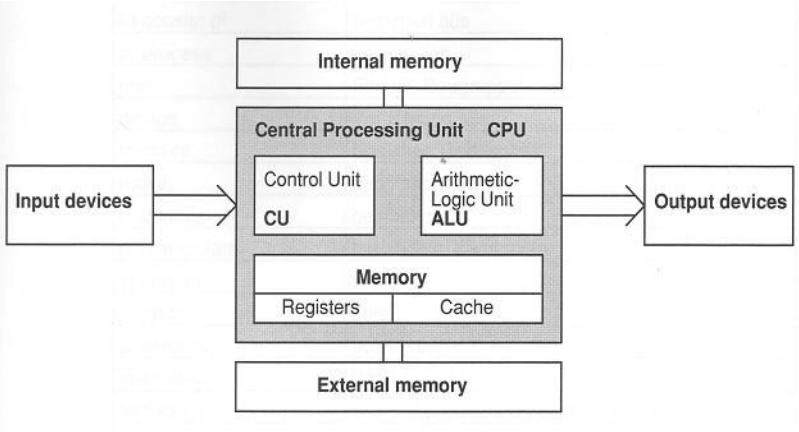
- Good control <u>each</u> qubit
- Room for control circuitry
- Reprogrammable
- Flexible architecture
- Scalable

general purpose

What's so hard?

Systems vs. Control:

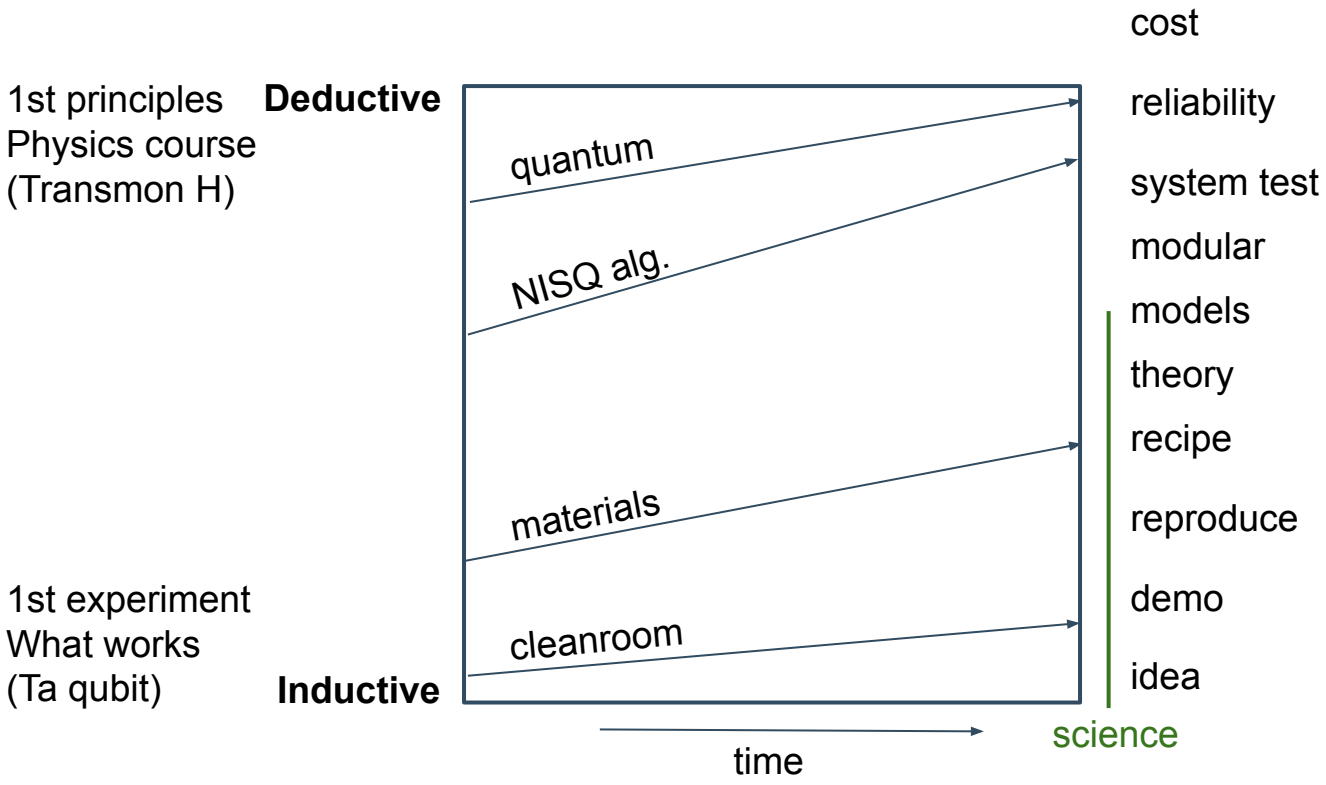
- Can't copy quantum information
- Hard to separate into sub-functions



Example: System Spec's for Error correction

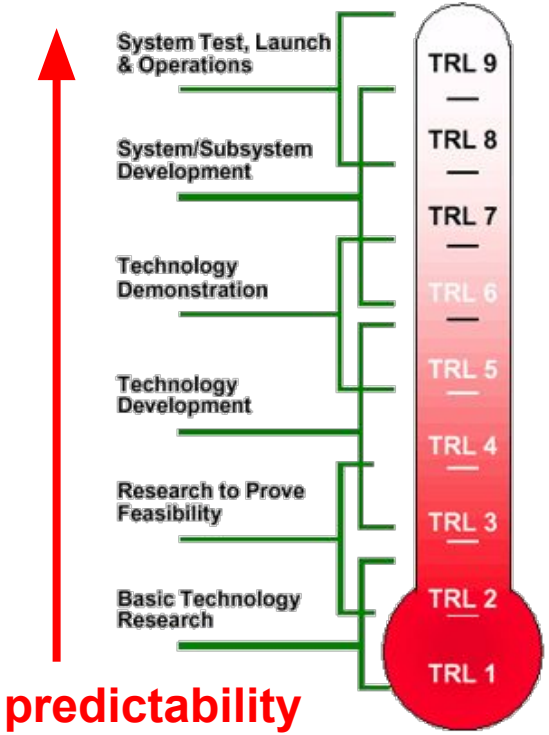
Surf Code	System Requirement
0.1%	10x below threshold
1000	Qubit number for 10^{-10} error
4 NN	Architecture (connectivity)
SupComp	Error decoding complexity
Larger	Logical qubits
Yes	1-logical gate
Braiding	CNOT gate
Physical	Measurement
Yes	Parallel logical gates
Yes	Long distance logical gates
90%	T-state distillation overhead
Ok?	Sensitivity to correlated errors (ɣ-rays)

Technical Readiness Level



- Need to predict to optimize and scale
- Tend to overestimate deductive knowledge

TRL



- Practical tool

Software: How to Scale

1) Designs must be turned into software to scale
   Hardware: need step-by-step recipe

2) Stack easy; interfaces are subtle and critical

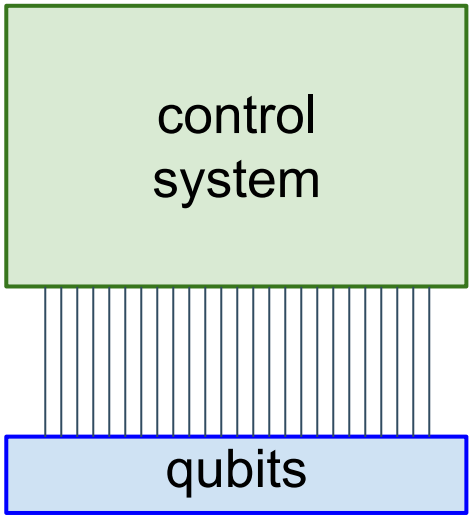
3) Interface example: control system
   a) Program waveforms to FPGA: slower, but general
   b) Program gates to FPGA: faster, but more constrained
   c) After a), then b) to microprocessor next to FPGA

4) Reliability is key to scaling
   a) Good specifications & documentation
   b) Testing
   c) Expert code review
   d) Continuous software testing of system

Information Constraints on Scalable Control

arXiv: 2012:14270

Present technology



100+ param's per qubit
for error optimization

Large area & volume

Large qubits?

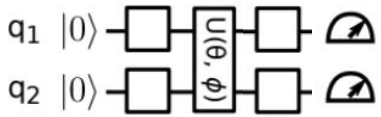
Maybe future

Eng. margin to
simplify control

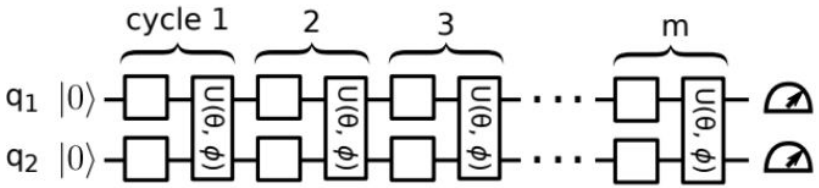
If low error qubits
(<0.01%)

Error Characterization

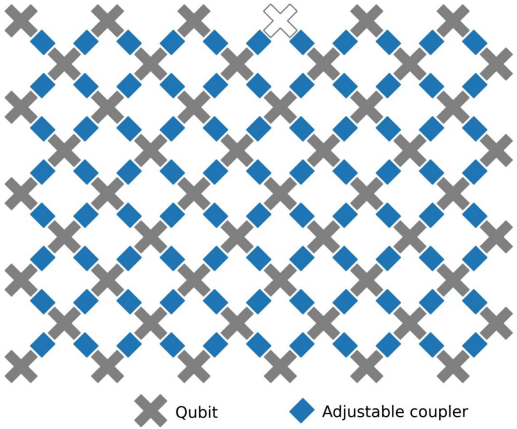
1) Quantum state and process tomography
   a) Most fundamental
   b) Full quantum description with phases
   c) Hard to separate out SPAM (state prep. and meas.) errors
   d) Not obvious how to improve gates
   e) Scales badly 2^{4N}, difficult beyond few qubits
   f) (Not what needed for error correction)



2) Randomized benchmarking (RB)
   a) Errors from random but repeated gates
   b) Subtracts away SPAM
   c) More scalable, but hard to invert for large number
   d) Uses Clifford gates, not matched to analog control
3) Cross-entropy benchmarking (XEB)
   a) Similar to RB
   b) But for arbitrary gates: best fit + error
   c) Can measure purity (decoherence only)
   d) Can be used to optimize, even every gate
   e) Works up to 30-50 qubits (or more with appx.'s)
   f) Predicts performance with error probability (not ampl.)

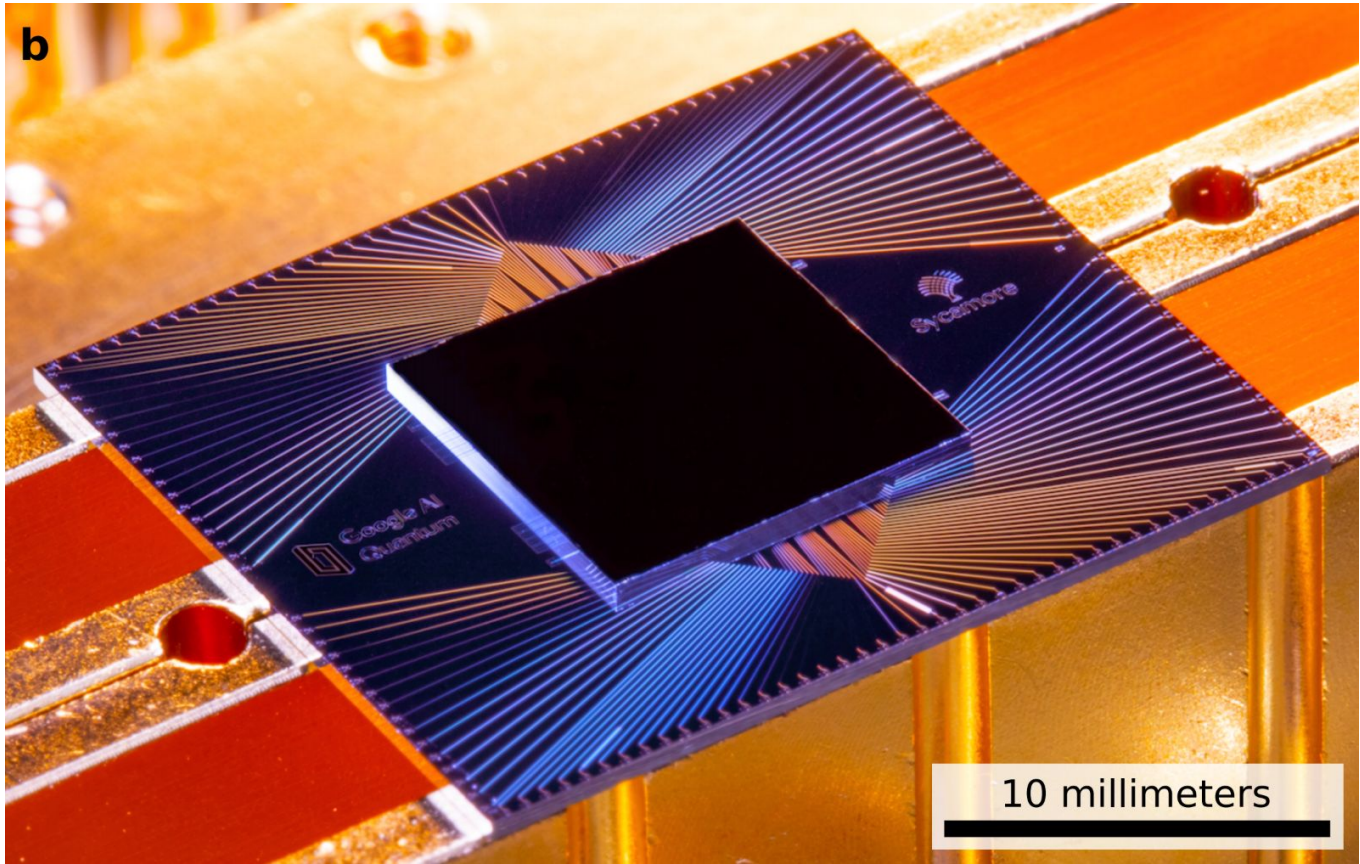


Testing the 54-qubit Sycamore Processor

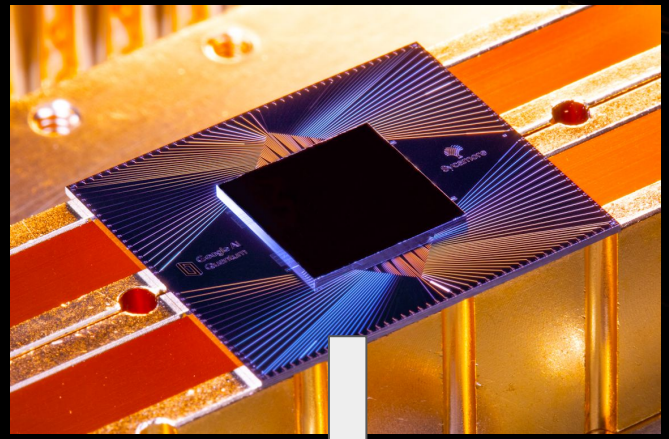


4-NN: Forward compatible SC error correction

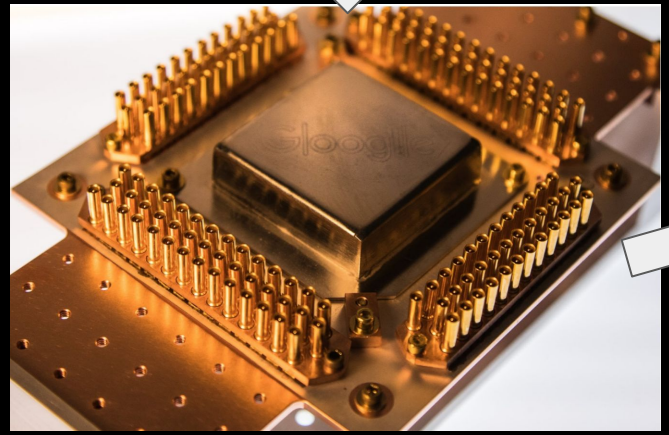
Adjustable coupler:
+: low off errors
fast
-: more control wires



Fabrication

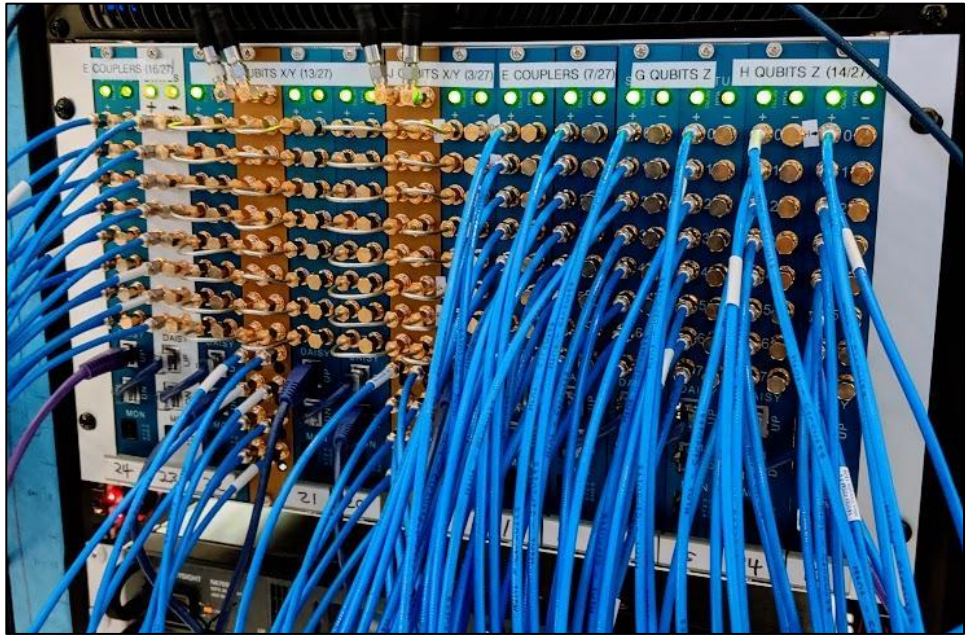


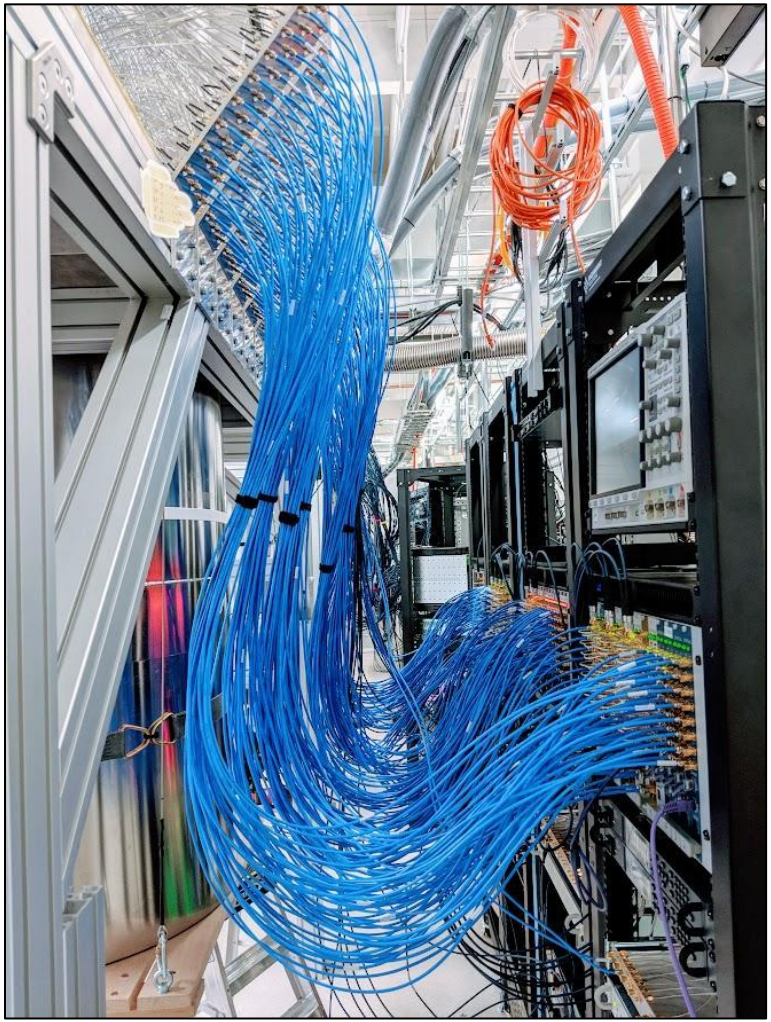
Packaging



Dilution refrigerator

Control Hardware

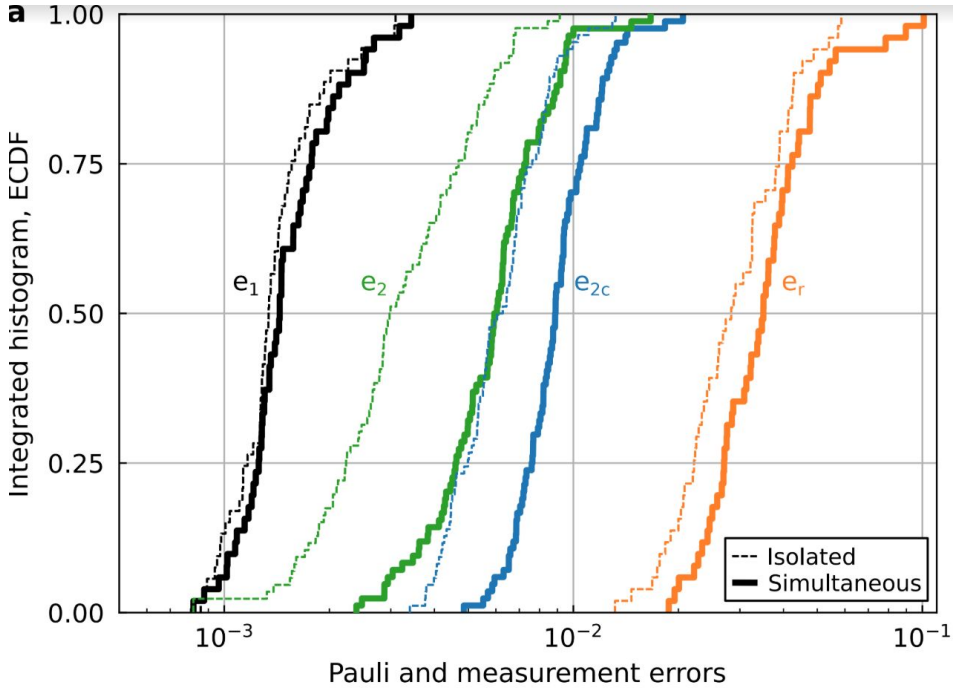


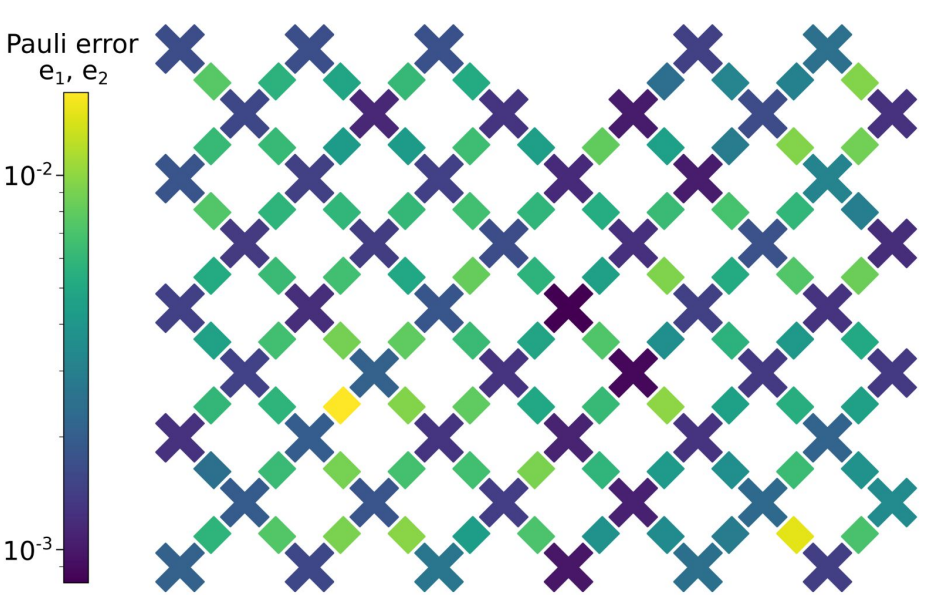


Custom built
High speed
High precision

Google AI Quantum

Low Errors using Fast 2-Qubit Gates (12 ns)

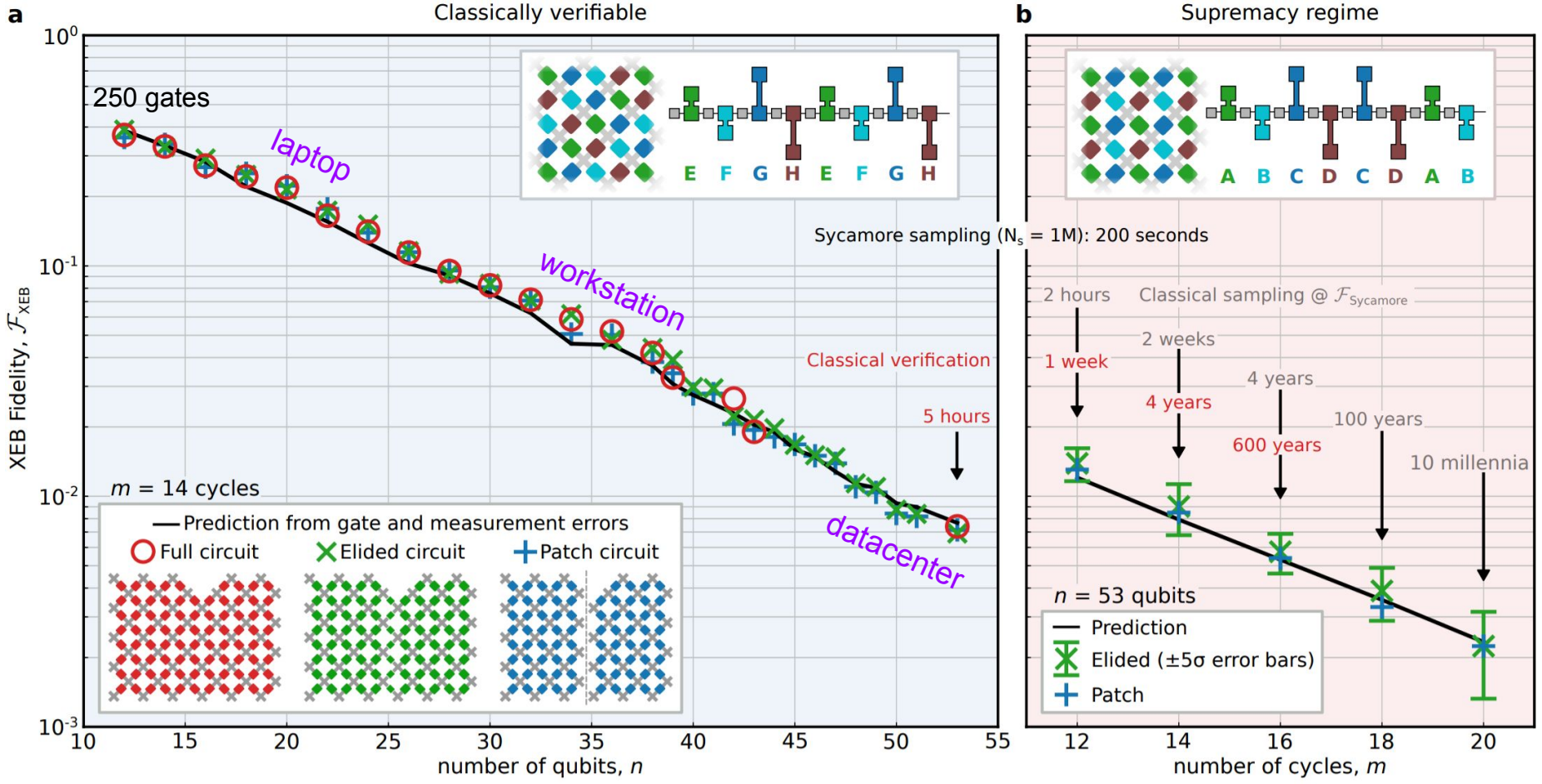




Average error	Isolated	Simultaneous
Single-qubit (e_1)	0.15%	0.16%
Two-qubit (e_2)	0.36%	0.62%
Two-qubit, cycle (e_{2c})	0.65%	0.93%
Readout (e_r)	3.1%	3.8%

Need to quote:
All qubits
Average and **Simultaneous**

Quantum Supremacy Data



Summary

1) Scaling also includes Quantum Systems Engineering
2) Low errors is a scaling issue
3) Technical readiness - better physics
4) Information constraints on control
5) Importance of testing & benchmarks