SONY

IMX990 series / IMX991 series

Tentative Support Package

The data except this specification conform to those of each product.

1. Product type

IMX990 series :
IMX990-AABA-C, IMX990-AABJ-C

IMX991 series :
IMX991-AABA-C, IMX991-AABJ-C

2. Description

This support package is intended to support product development.

3. Description Items

- ◆Guideline for designing the printed circuit board
- ◆SLVS output interface
- ◆Communication port (4-wire serial / I^2C)
- ◆Pattern Generator (PG) function
- ◆How to get sensor information
- ◆Lens design guideline

Contents

4. Guideline for designing the printed circuit board

In this section we explain the design guideline of the printed circuit board layout and mount.

4.1. Application circuit.

4.1.1. Power supply pins

(1) Please design the suitable filter in power supply line to reduce influence of a power supply noise and to prevent an unnecessary radiation. Especially, the parts to analog and pixel power supply pin need to choose the one that is small direct current resistance because that pin is sensitive to the voltage change. The voltage change becomes the factor of horizontal line noise.

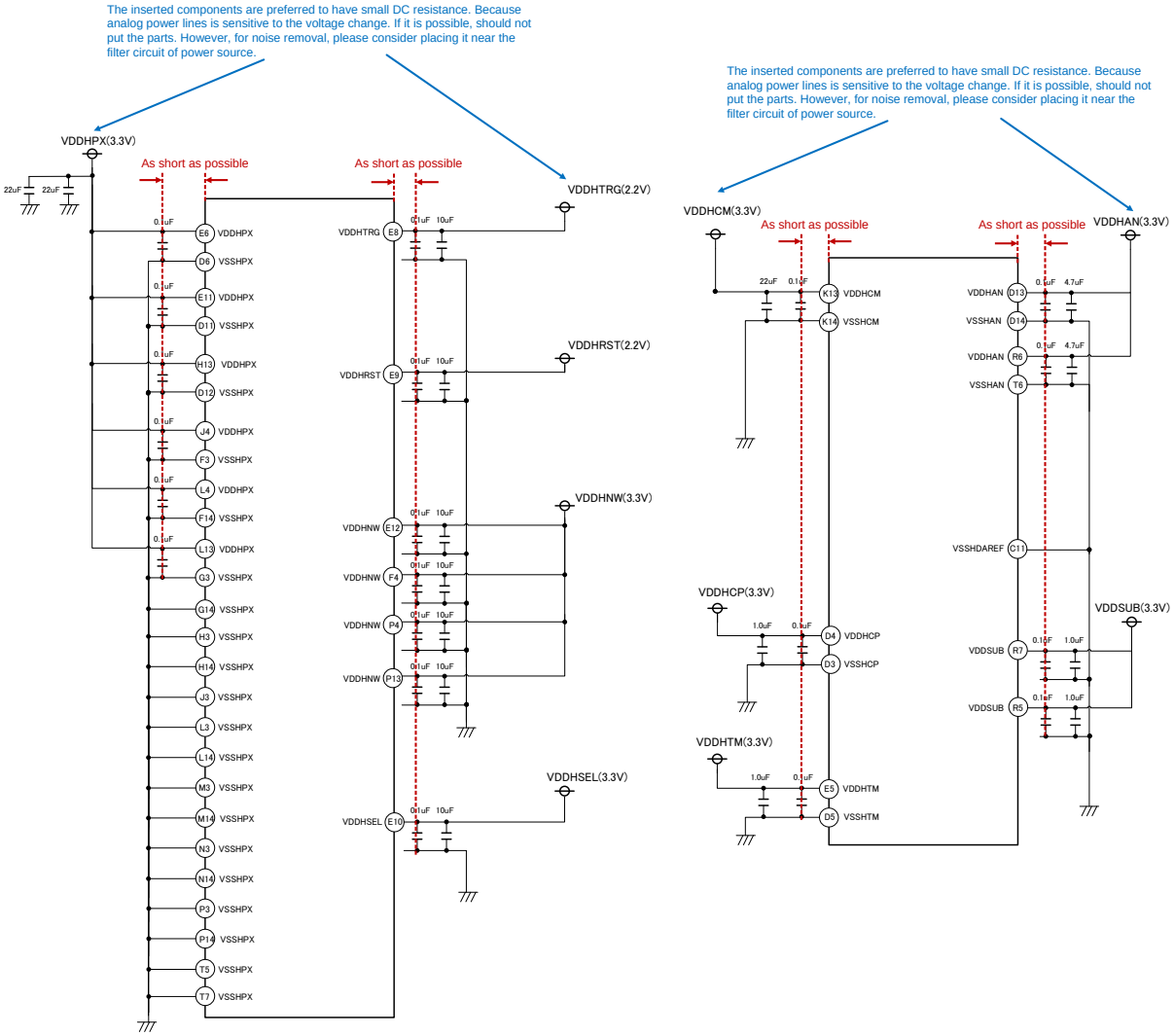
(2) We suggest that the use of reasonable noise filters on the power line for suppressing the radiation noise from the lines.

(3) VDDDR, VDDFM, VDDHNW is sensitive signals for noise. So these pins and other power supply should not have the common impedance.

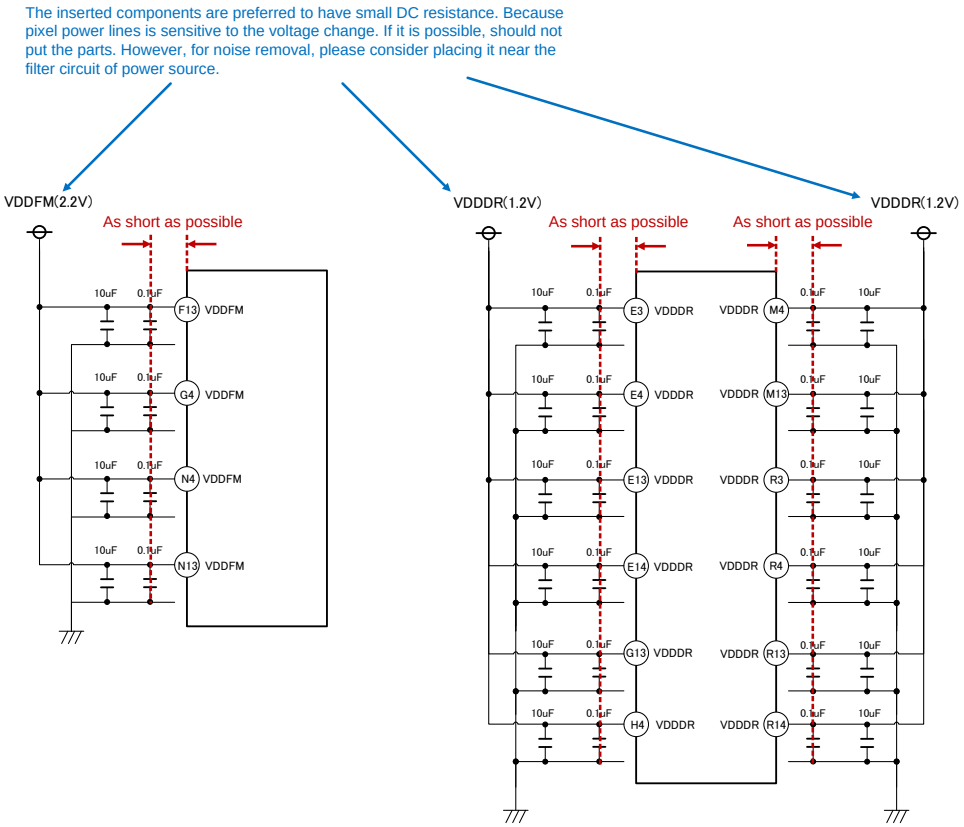
(4) Please mount peripheral parts (capacitor) near the element as much as possible.

(5) Please make patterns of Power supply (3.3V, 2.2V, 1.8V, 1.2V) as wide as possible.

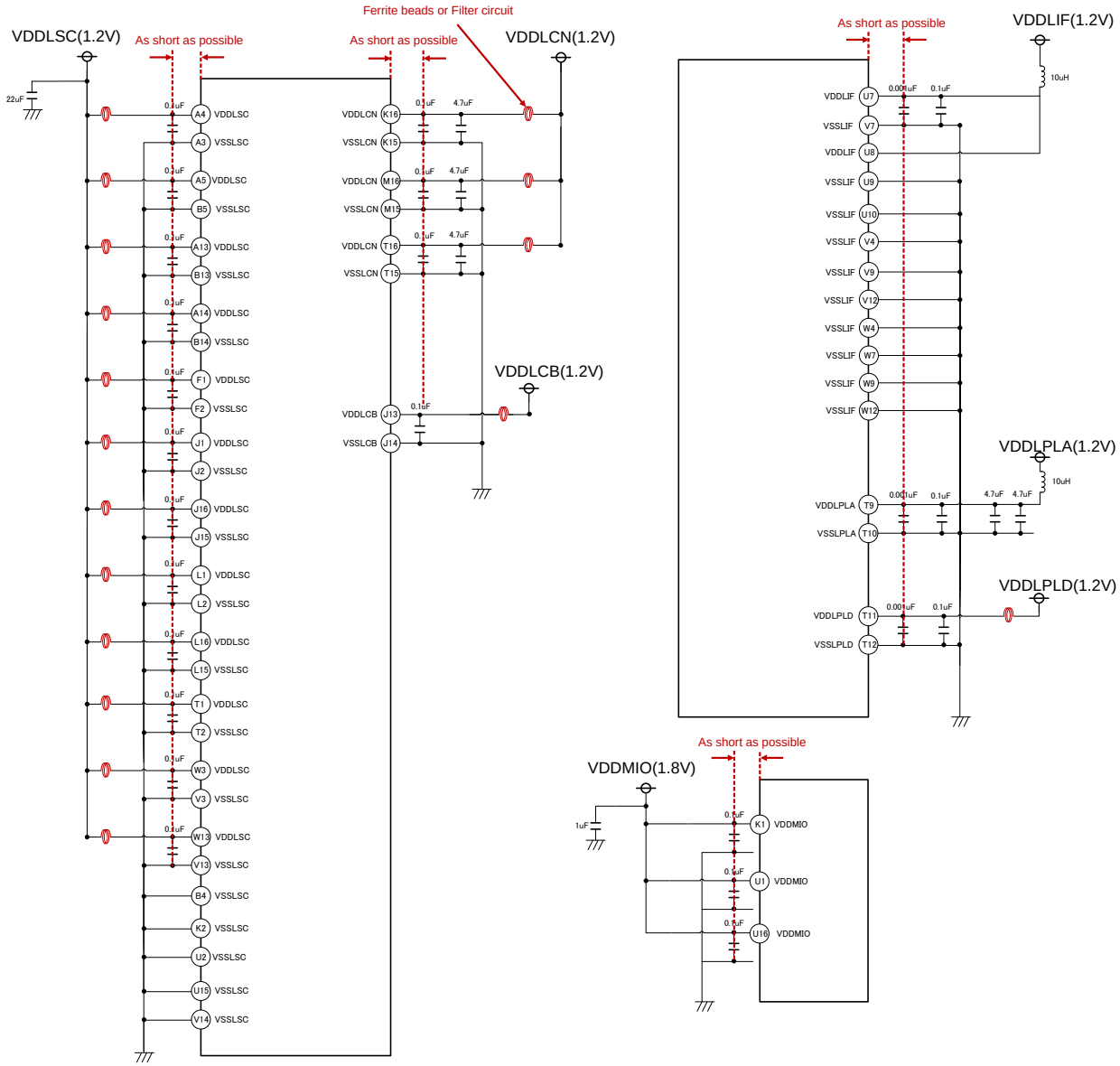
(6) Please put capacitors at each power pin. And avoid putting a capacitor of total capacity value at multiple pins in order to reduce parts.



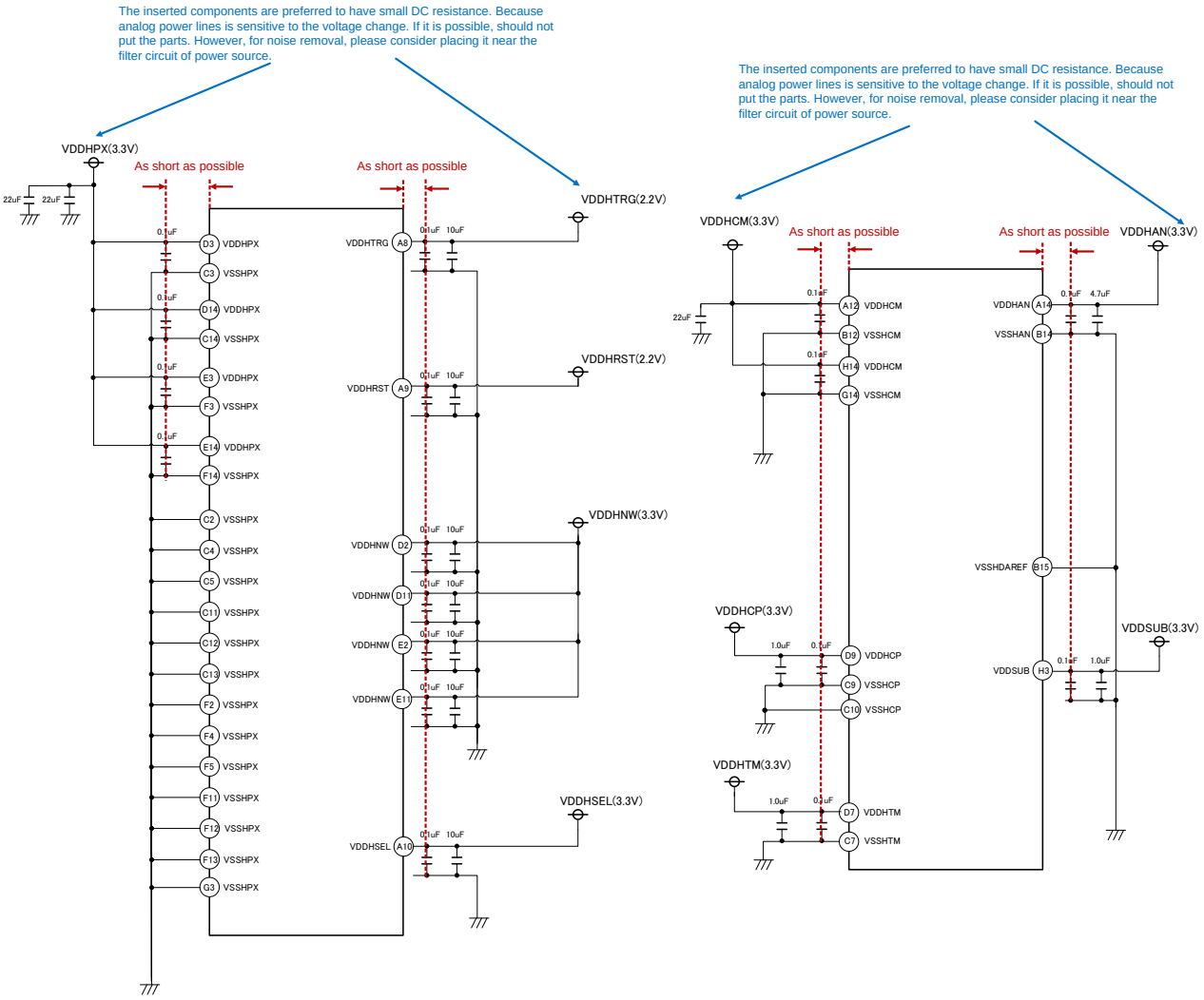
Reference design for analog power supply pins (IMX990-AABJ, IMX991AABJ).



Reference design for pixel power supply pins (IMX990-AABJ, IMX991AABJ).

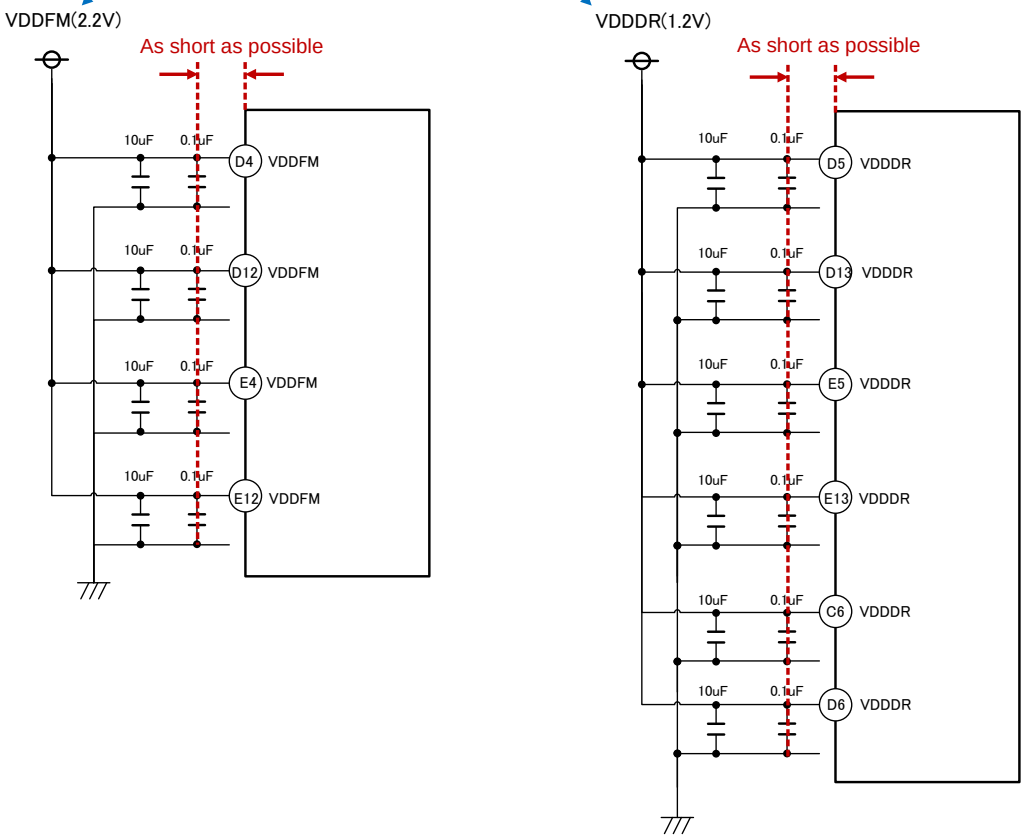


Reference design for digital power supply pins (IMX990-AABJ, IMX991-AABJ).

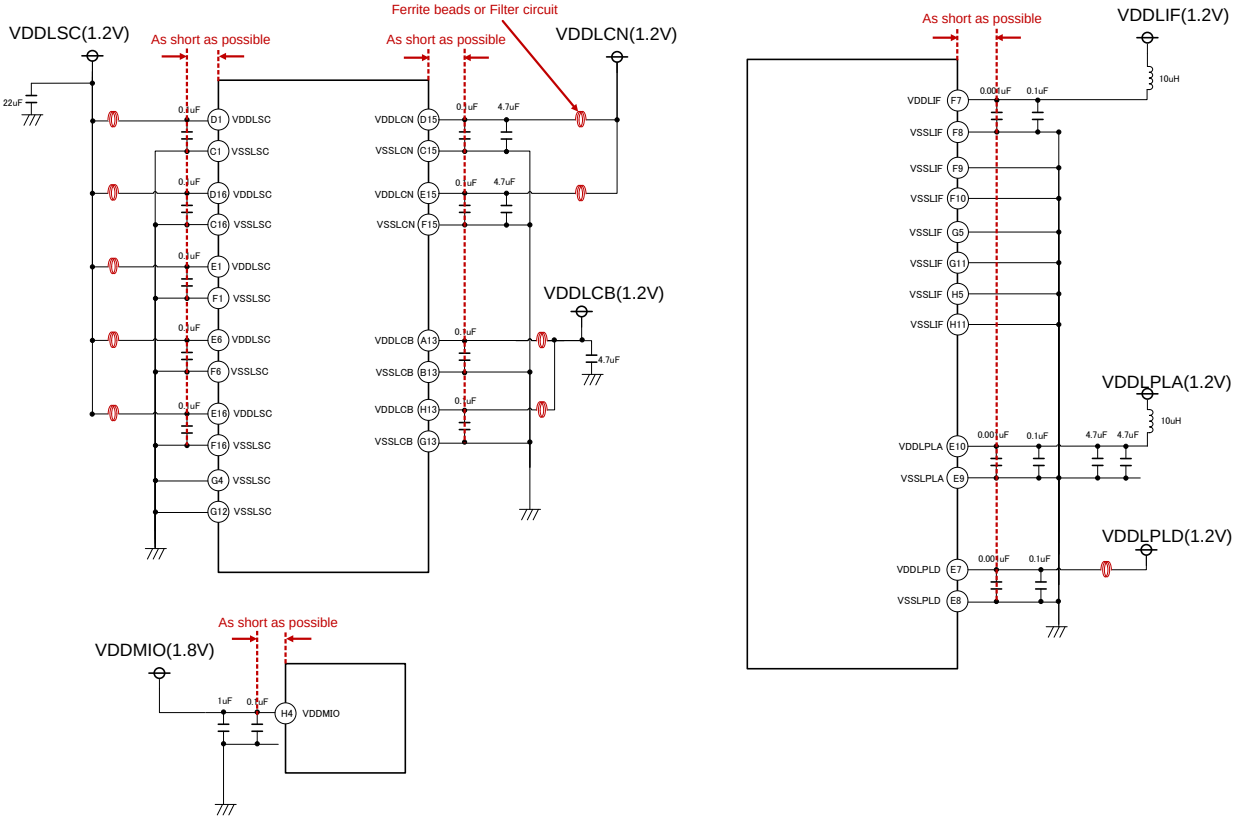


Reference design for analog power supply pins (IMX990-AABA, IMX991-AABA).

The inserted components are preferred to have small DC resistance. Because pixel power lines is sensitive to the voltage change. If it is possible, should not put the parts. However, for noise removal, please consider placing it near the filter circuit of power source.

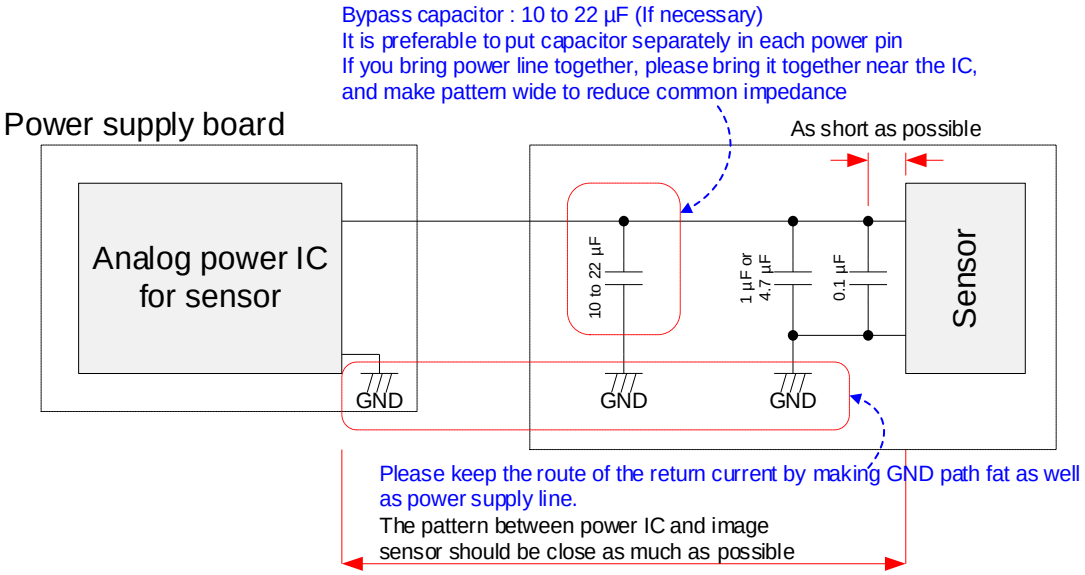


Reference design for pixel power supply pins (IMX990-AABA, IMX991-AABA).



Reference design for digital power supply pins (IMX990-AABA, IMX991-AABA).

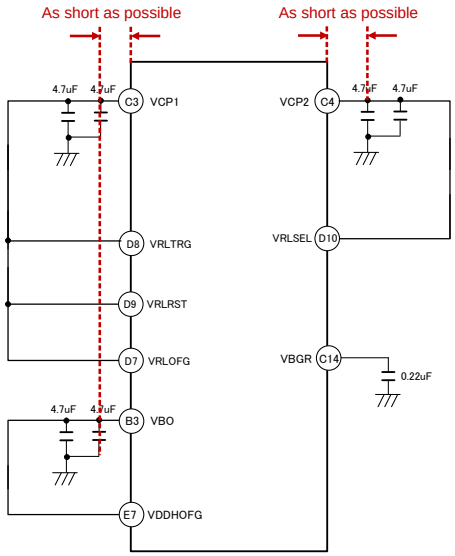
(7) We recommend to implement the power supply IC as close to the sensor as possible. If cannot, use wider power supply pattern of lower DC resistance, implement the large (10uF or more) decoupling capacitor close to the sensor. With regard to pattern, please refer to “Notes for designing pattern of printed circuit board”.



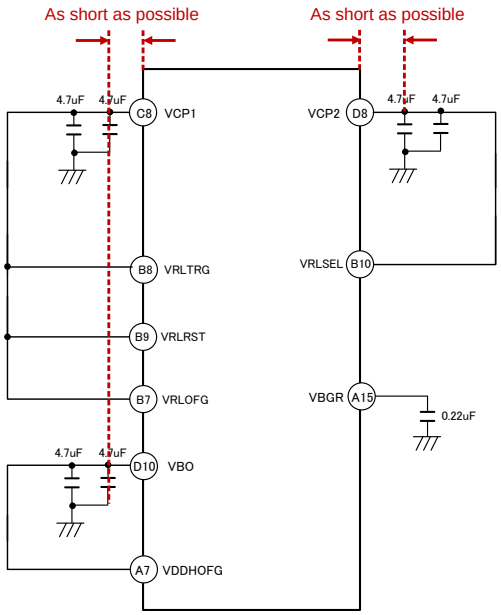
Layout of power supply IC and decoupling capacitors of large capacity

4.1.2. Other Pins

VCP1, VCP2, VB pin is sensitive to noise. Please place the capacitors near the pins. As for the capacity of a capacitor, it is desirable to insert the value according to the example of an application circuit.



Reference design for other pins (IMX990-AABJ, IMX991-AABJ).



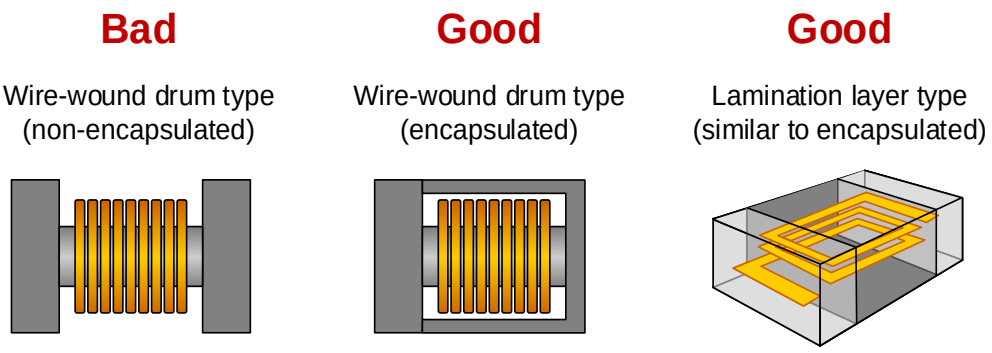
Reference design for other pins (IMX990-AABA, IMX991-AABA).

4.2. (Reference) Component

The following describes the components used reference information. When in actual use, please contact the manufacture for each component.

4.2.1. Power supply IC

Please select the power supply IC of better PSRR characteristics. Fluctuation of the power supply voltage will cause the horizontal line noise. In that case, we recommend that you use a series regulator.
Please note that when using switching power regulator of the following points.
(1) When using switching power regulator, magnetic field inducted by inductor might cause the noise of the image.
(2) Encapsulated (shield) type inductor is recommended.
(3) Mounting direction of the inductor also affects (increase or decrease) the noise level.



Encapsulated/non-encapsulated type inductor

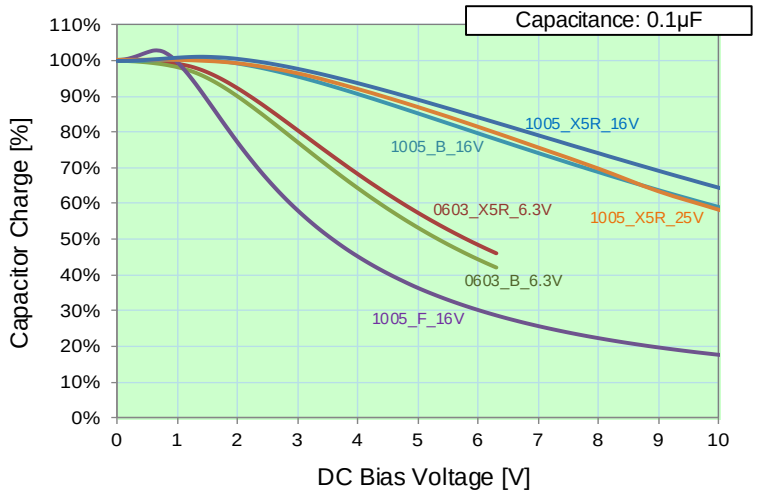
4.2.2. Decoupling capacitors

Please use non-polar capacitors. It is possible to operate the sensor by using typical ceramic capacitors.

(1) All the power supply voltage are smaller than 3.3 V so you can use any 1608M size capacitors of any characteristics in the graph. When you use 1005M size capacitors, you should select characteristics-B device. Characteristics-F device should not be chosen.

(2) Decoupling capacitors for each pin are sensitive to image quality. Please implement sufficient capacity of the decoupling capacitors according to the power supply condition. If you use capacity that is small one and large one, please put the small one near the sensor. Please refer to Application circuit for details.

(3) The capacity of the laminated layer ceramic capacitors will decrease in regard to the impressed DC bias voltage by piezo-electric effect. It will be more obvious when using smaller size and larger capacity, please check the specification sheet of each devices.
(Graph below shows the characteristics.)



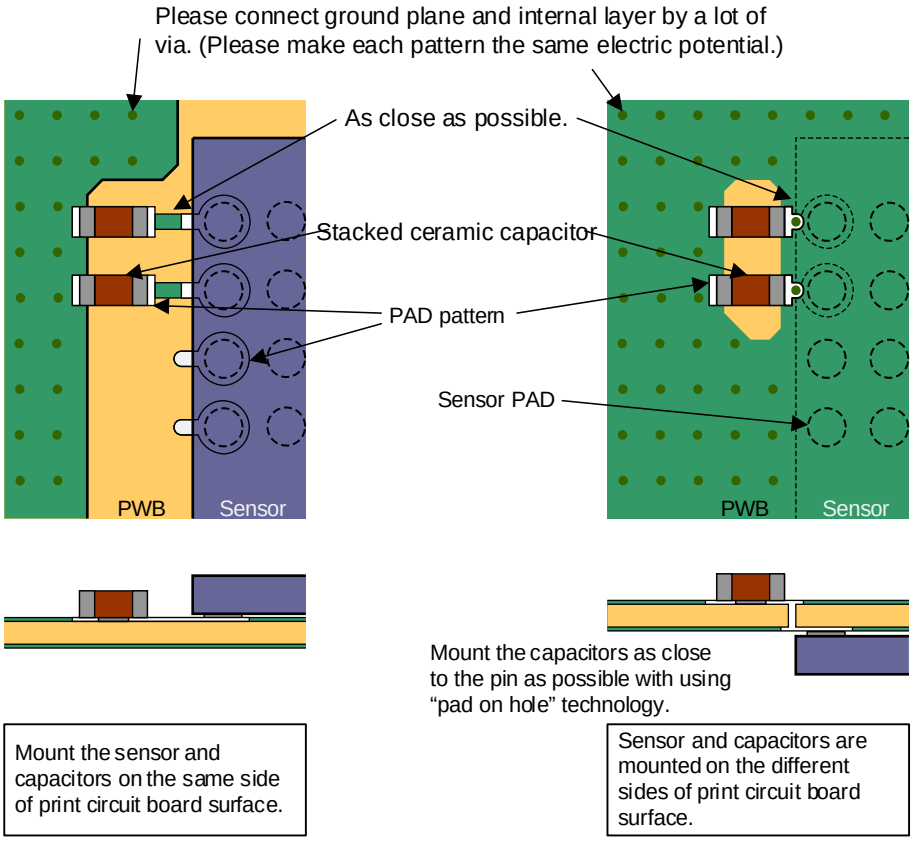
DC bias vs. capacity

4.3. Notes for designing patterns of printed circuit board.

4.3.1. Power supply pins

(1) The peripheral devices (capacitors) of the sensor should be mounted as close to the power supply pins as possible. Longer wire length might cause the degradation of the image quality.

(2) Surface power/ground plane and inner layer power/ground plane should be connected with enough number of the vias (Vertical Interconnect Access) . Please make each pattern the same electric potential.

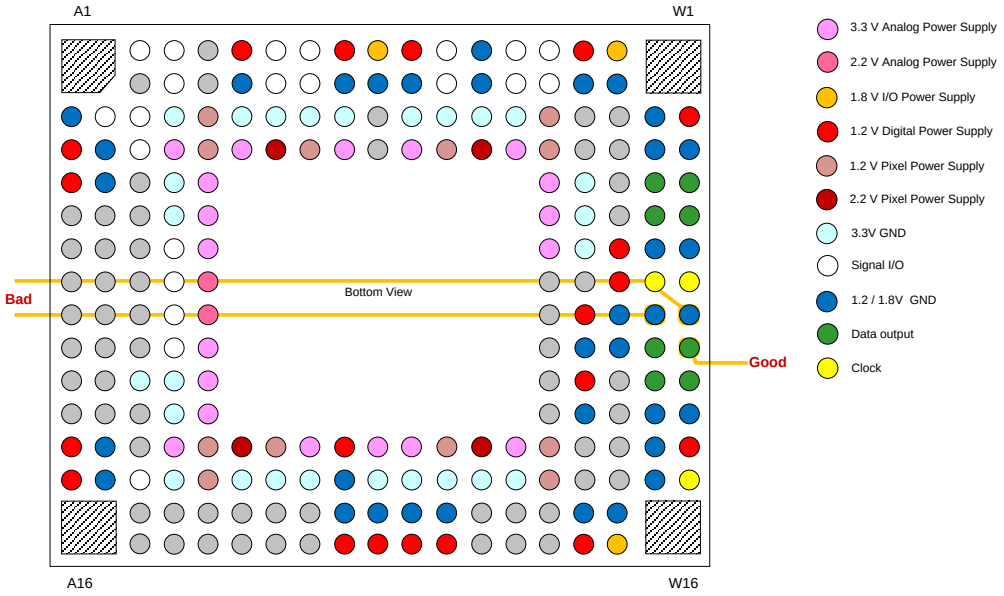


Example of capacitor mounting

(3) The noise on the VDDDR, VDDFM, VDDHNW pins degrades the image quality. So these pins and other power supply pins should not have the common impedance.

(4) Loop of the ground pattern might propagate the noise to the other patterns (ex. Power supply pattern) so the ground pattern recommends Land pattern. Its recommended to use the common single GND plane for Analog GND and Digital GND.

(5) Digital signal pattern on the other layer should not be in parallel with the power supply patterns, terminals of VCP1, VCP2, VBO, VRLSEL, VRLRST, VRLTRG, VRLOFG, VDDHOFG and these lines.



Signal Wire Routing (IMX990-AABJ, IMX991-AABJ)

Signal Wire Routing (IMX990-AABA, IMX991-AABA)

(6)GND Line

Insert a GND line between differential lanes to reduce crosstalk.

When it is physically impossible to insert a GND line, separate the lanes. (Guideline: 3 times the lane width)

4.4. Wiring patterns for image output signals

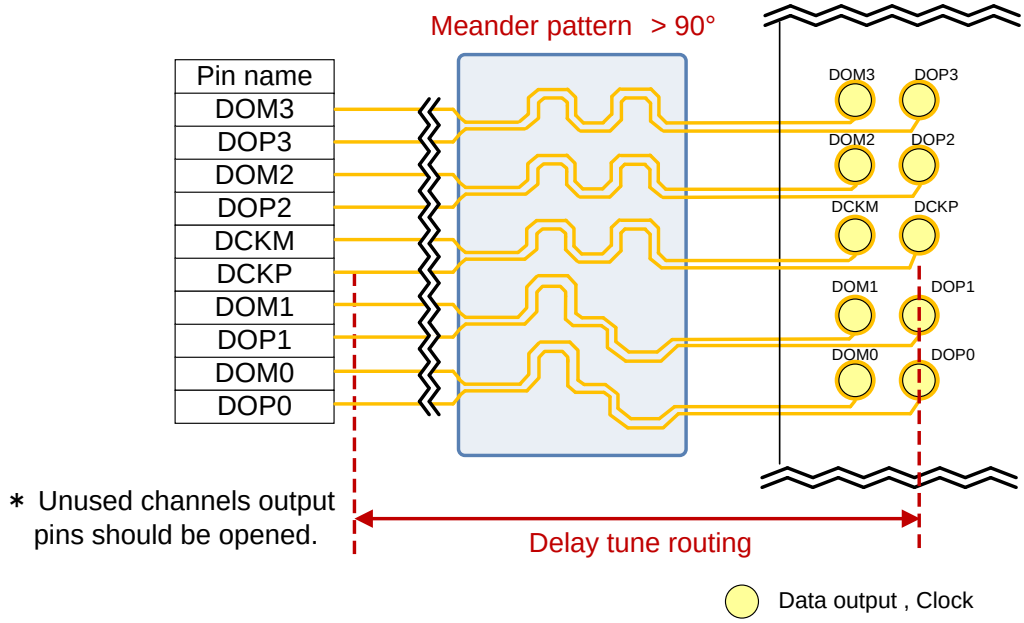
This sensor is supported output format below. This section described about wiring pattern for the following format.

- ◆ SLVS output

4.4.1. SLVS output

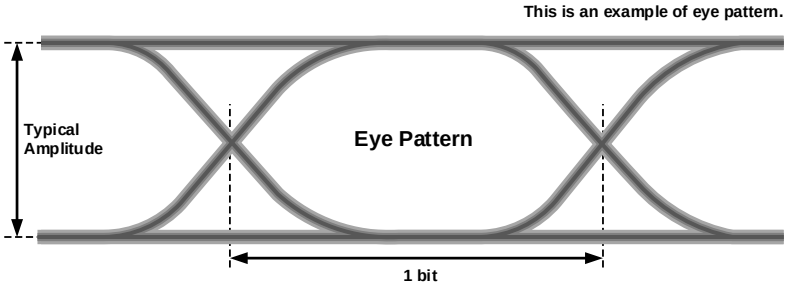
(1) When choosing SLVS output mode, signal wires (DOPx and DOMx, DCKP and DCKM) must be paired.
(2) We recommend delay tune wiring for image signals, especially delay of each differential pair signal and Data and its Strobe signal should be controlled by using meander wiring. Turning point angle of the wire should be greater or equal to 90 degree. (obtuse angle)
(3) Decoupling capacitors for power supply for image signal output (VDDLIF) should be mounted close to the power supply pins of the package of the sensor with using small size (1005M or 0603M) laminated layer ceramic capacitor.

Meander pattern should make pattern as close to the output pins (near the sensor) as possible.



Example of wiring patterns for SLVS output signal

<For your reference>
Validity of the image signal can be checked by “eye pattern” of the signals. With the adequate loading and delay tuned condition, you can see clear “eye pattern” with sufficient margin of the threshold and the noise level for the receiver.



Eye pattern of the image signal

5. Serial Communication Port

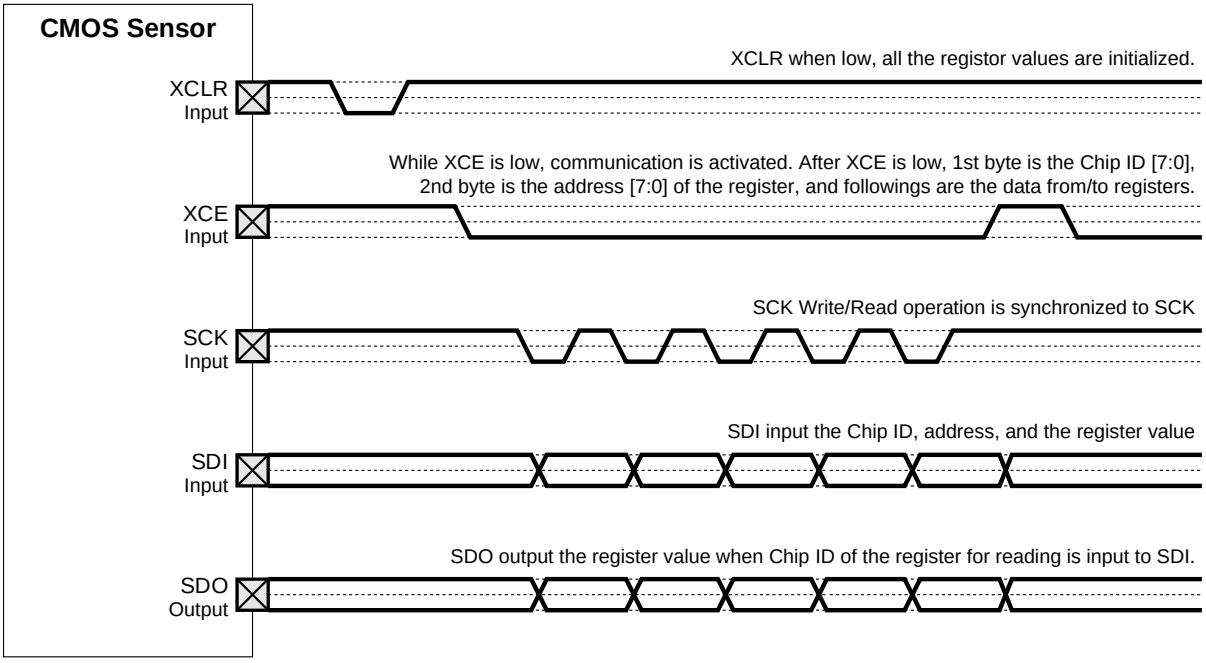
This sensor has 4-wire serial communication and I^2C serial communication.
This section describes the operation of the serial interfaces.

5.1. 4-wire serial communication

Characteristics of 4-wire serial interface.

(1) 3-wire serial interface consists of serial data input (SDI), serial clock (SCK), and chip enable (XCE). SDO is the data output port for read out the value in the registers.
(2) Data transfer is done in unit of 8bit (1byte). In case of continuous communication, no limitation for the numbers of byte for the communications. (However, limited by communication period.)
(3) LSB first protocol.
Ex.) When sending 28h LSB first: 0001 0100.

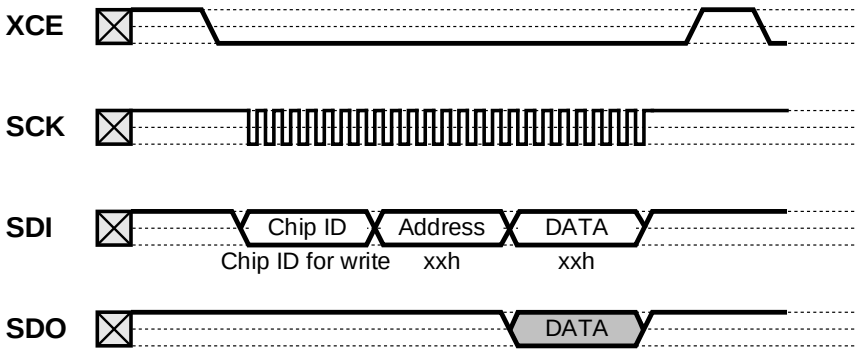
Terminal name	function	description
XCLR	Initialize the system	Initialize the register value.
XCE	Enable the communication	Communication is active for XCE is low.
SCK	Serial clock for communication	Maximum frequency is 13.5 MHz
SDI	Serial data input	Change the value at falling edge of SCK, latch the value by rising edge
SDO	Serial data output	Output the value synchronous to the falling edge of SCK



4-wire Communication Function

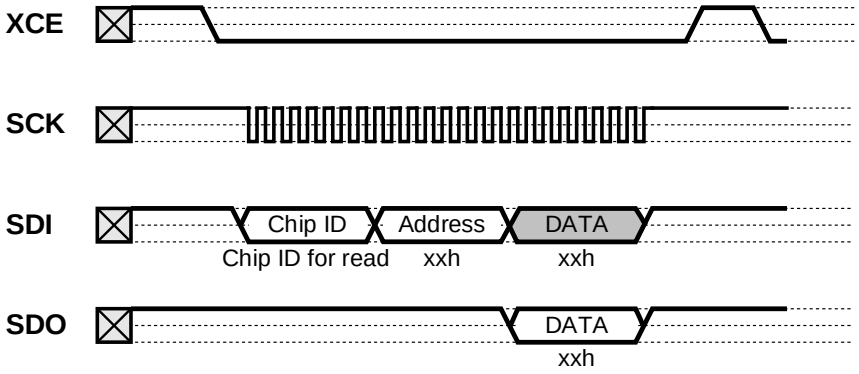
5.1.1. Register write/read operation

Both of register write and read operation, Chip ID, address and register value are declared to SDI. When Chip ID is the registers for writing, value is written to the register designated by the address. When Chip ID is the registers for reading, the value is read out from the register designated by the address. Write and read operation can be done continuously while XCE is low.



Write Operation

When write operation, the order of the commands to SDI is as follows. 1st byte: Chip ID is selected the registers for writing, 2nd byte: address to write, 3rd byte and after: register value. SDO output the current value (Before write) of the register designated by the address.



Read Operation

When read operation, the order of the commands to SDI is as follow. 1st byte: Chip ID is selected the registers for reading, 2nd byte: address to read, 3rd byte and after : invalid data SDO output the value of the register designated by the address.

The example of communication timing to writing to continuous address as shown table 1 is shown below.

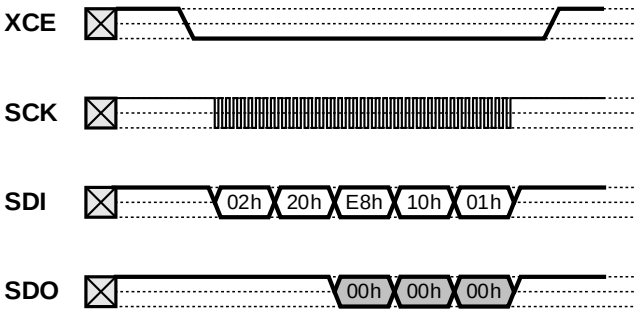


Table1. The example of writing registers

Address	bit	Default value	Setting value	
			before	After
20h	[7:0]	00h	00h	E8h
21h	[7:0]	00h	00h	10h
22h	[7:0]	00h	00h	01h

Write operation to continuous address

Write E8h to address 20h first. And with keeping XCE low, by writing 10h, 01h in succession, these values are set to consecutive addresses (21h and 22h). The example of reading communication timing to writing to continuous address as shown table 1 as shown table 2 is shown below.

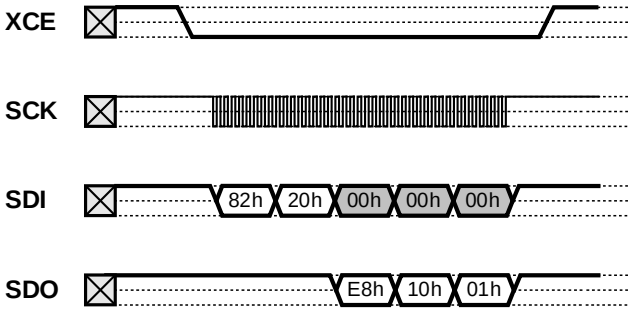


Table2. The example of reading registers

Address	bit	Default value	Setting value	
			before	After
20h	[7:0]	00h	E8h	E8h
21h	[7:0]	00h	10h	10h
22h	[7:0]	00h	01h	01h

Read operation to continuous address

In case of reading out the value from the registers, write the registers for reading as the Chip ID then designate the address to read. After that input the dummy data to SDI. In read mode, input data are discarded and no register is updated, current register values are output from SDO continuously.

5.2. I²C serial communication

Characteristics of 4-wire serial interface.

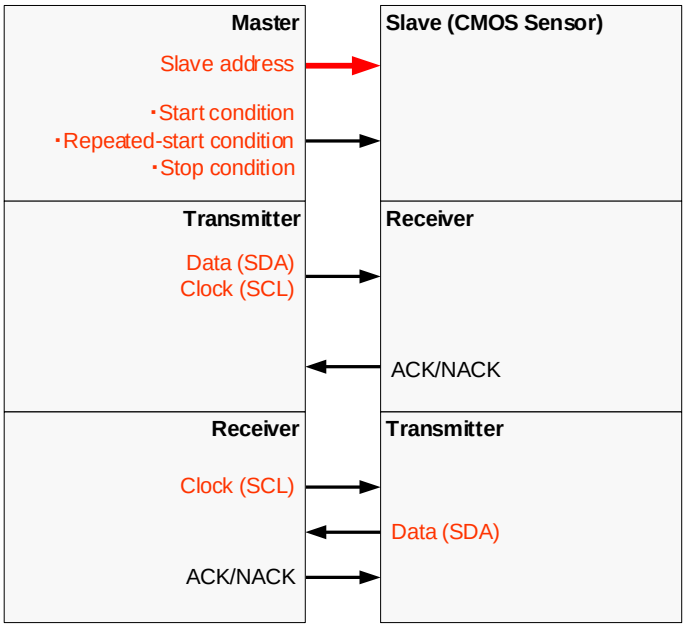
(1) I²C consists of 2 wires of serial data and serial clock.
(2) Unit of the communication is 8 bits (1 byte), bi-directional communication. And in case of continuous communication, no limitation for the numbers of byte for the communications. (However, limited by communication period.) Acknowledge bit (ACK/NACK) is required at the end of communication.
(3) MSB first protocol
e.g.) When sending 28h MSB first: 0010 1000.
(4) I²C is the bi-directional communication and the “master” side controls the communication, the “slave” side is controlled by master. The “master” always provides the clock.
(5) While communication, the device transferring the data is the “transmitter”, and the device receiving the data is the “receiver”. The “receiver” provides acknowledge bit.
(6) This sensor is slave.

I²C Communication mode for this sensor

Mode	Data rate	Correspondant
Standard mode	100 kbps	Available
Fast mode	400 kbps	Available
Fast mode Plus	1 Mbps	N/A
High speed mode	3.4 Mbps	N/A

SLAVE Address

Refer to the data sheet of the image sensor.



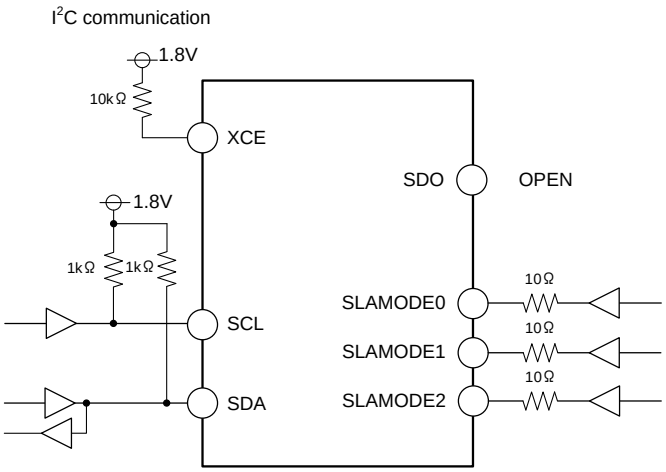
Relation between the sensor and the ISP when I²C communication.

Master execute the following communication.

- ◆ Generate slave address (declare the device to be slave. Sensor is the slave here.)
- ◆ Generate “start condition”, “repeated start condition”, and “stop condition”.

While communication, the device transforming the data is the “transmitter”, and the device receiving the data is the “receiver”.Master can work as both transmitter and receiver, slave also work as both.
Transmitter generates the data (SDA), and receiver generates the acknowledge Bit (ACK/NACK).
Master always generates the clock (SCL).

Reference design for I²C serial communication is shown below. Please connect XCE and OV_{DD} when I²C communication. In addition, SCL, SDA, please pull up to 1 kΩ OV_{DD}.



Reference design for I²C serial communication

5.2.1. Overview of the communication protocol

Data is transferred by SDA port. The transition timing of the SDA follows the rule below.

- State control (start, restart, stop of the communication) is done while SCL is “high”.
- When data transfer, SDA toggles while SCL is “low”

5.2.1.1. State control (start, restart, stop of the communication)

The conditions of start (start condition), restart (repeated start condition), and stop (stop condition) of the communication is shown below. State control is done by master device.

State condition	condition
Start condition	SDA toggles from High to Low while SCL is high
Repeated start condition	start condition while stop condition is of the previous data transfer is not Declared
Stop condition	SDA toggles from Low to High while SCL is High.

5.2.1.2. Acknowledge bit

Data transfer is done in unit of 8 bits (1 byte). The acknowledge bit is generated for every 8 bits data transfer and added after the last (8th) bit to indicate that receiver normally received the data. When receiver wants to stop the communication by the internal interrupt or etc. receiver generates the negative acknowledge bit (NACK).

- Master must send the slave address after declaration of the “Start condition” and “Repeated start condition”.
- When slave generators the negative acknowledge bit, master declares the stop condition and stops the communication immediately.

6. Note for access to register

When writing the value to registers, we recommend “Read-modify-write” to avoid the trouble caused by inadequate over write of the register. For example “VREVERSE” value is assigned to address of 04h [0], “HREVERSE” value is assigned to address of 04h [1]. When update HREVERSE value after writing VREVERSE, VREVERSE value in address of 04h [0] should be kept. “Read-modify-write” can prevent the wrong overwrite of the value

Ex.) In case of writhing the value 1d to VREVERSE and HREVERSE

In case of “no Read-modify-write”

1) HREVERSE = 1d ⋯ set value 02h to address: 04h

Address: 04h

0	0	0	0	0	0	1	0

2) VREVERSE = 1d ⋯ set value 01h to address: 04h

01h

Address: 04h

0	0	0	0	0	0	0	1

HREVERSE=0d VREVERSE=1d

Writing the VREVERSE value 01h to address 04h without considering HREVERSE bit in 04h [1], HREVERSE will be changed.

In case of “Read-modify-write”

1) HREVERSE = 1d ⋯ set value 02h to address: 04h

Address: 04h

0	0	0	0	0	0	1	0

2) Read register value

0	0	0	0	0	0	1	0

Read out the current value and store the value in the memory area of MCU

3) VREVERSE = 1d ⋯ set value 01h to address: 04h

01h

Address: 04h

0	0	0	0	0	0	1	1

Bit operation “add” with the value stored in step 2)

03h

Address: 04h

0	0	0	0	0	0	1	1

HREVERSE=1d VREVERSE=1d

Write value after bit operation (No overwrite of VREVERSE value)

7. Pattern Generator

This chapter explains the pattern generator (PG) function.

7.1. Register map for pattern generator function

The Register map for Pattern Generator is shown below.
Please set via sensor standby.
Please refer to the datasheet for registers setup other than those lists.

Chip ID = 07 (Write: Chip ID = 07h, Read: Chip ID = 87h, I²C: 35h)**

Address		Bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
20h	3520h	[7:0]		Fixed to 1Fh	10h	10h	S
40h	3540h	[7:0]		Fixed to 00h	00h	00h	S
50h	3550h	0	PGREGEN [0]	PG operation enabled 0h : PG OFF 1h : PG ON	0	02h	S
		1	PGTHRU [0]	Back Ground Transient 0h : Invalid PGMODE=00h / 06h; The background is fixed to "0h". PGMODE=04h / 05h; The background is set to PGDATA2. 1h : Valid	1		S
		2	PGCLKEN [0]	Clock control for PG 0h : Clock stop 1h : Clock operation Set to “1h” when using Pattern Generator	0		S
		3		Fixed to 0	0		-
		4		Fixed to 0	0		-
		5		Fixed to 0	0		-
		6		Fixed to 0	0		-
		7		Fixed to 0	0		-
51h	3551h	0 1 2 3 4	PGMODE [4:0]	PG mode setting 00h: Multiple pixels Pattern IMX425 and IMX432 don’t support this Pattern 01h: Sequence Pattern 1 02h: Sequence Pattern 2 03h: Gradation Pattern 04h: Horizontal 1 Row Pattern 05h: Vertical 1 Column Pattern 06h: Horizontal 1 Row and Vertical 1 Column Pattern 07h: Stripe Pattern of the arbitrary value 08h: Checks pattern of the arbitrary value 0Ah: Color bar which changes horizontally 0Bh: Color bar which changes vertically Others: Setting prohibited	1Fh	1Fh	S
		5		Fixed to 0	0		-
		6		Fixed to 0	0		-
		7		Fixed to 0	0		-

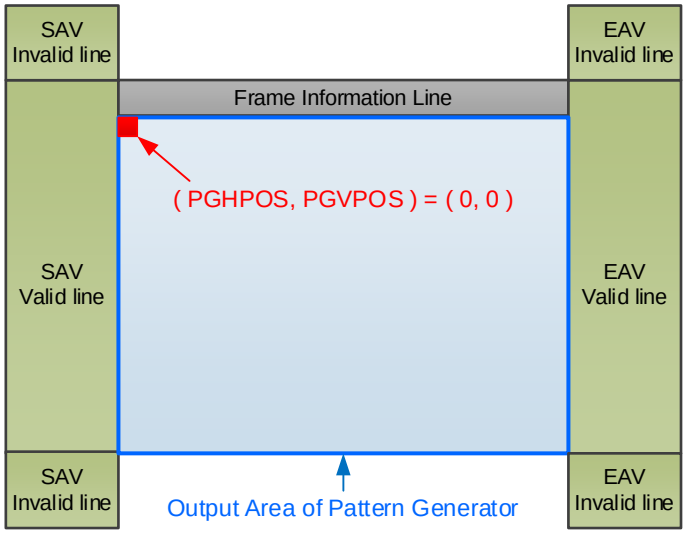
Address		Bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
54h	3554h	0	PGHPOS [12:0]	LSB	0000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6		Horizontal Start Address 0 or more is valid.			
		7					
55h	3555h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		-
		6		Fixed to 0	0		-
		7		Fixed to 0	0		-
56h	3556h	0	PGVPOS [11:0]	LSB	000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6		Vertical Start Address 0 or more is valid.			
		7					
57h	3557h	0				00h	
		1					
		2					
		3		MSB			
		4		Fixed to 0	0		-
		5		Fixed to 0	0		-
		6		Fixed to 0	0		-
		7		Fixed to 0	0		-
58h	3558h	0	PGHPSTEP [7:0]	Interval of horizontal pixels 00h is prohibited	00h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
59h	3559h	0	PGVPSTEP [7:0]	Interval of vertical pixels 00h is prohibited	00h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					

Address		Bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
5Ah	355Ah	0	PGHPNUM [7:0]	Number of horizontal pixels 00h is prohibited	01h	01h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
5Bh	355Bh	0	PGVPNUM [7:0]	Number of vertical pixels 00h is prohibited	01h	01h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
5Ch	355Ch	0	PGDATA1 [12:0]	LSB	0000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6		Set PGDATA1			
		7					
5Dh	355Dh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		-
		6		Fixed to 0	0		-
		7		Fixed to 0	0		-
5Eh	355Eh	0	PGDATA2 [12:0]	LSB	0000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6		Set PGDATA2			
		7					
5Fh	355Fh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		-
		6		Fixed to 0	0		-
		7		Fixed to 0	0		-
61h	3561h	[7:0]		Do not rewrite	-	-	-
62h	3562h	0	PGHGSTEP [1:0]	The increment of gradation pattern 00b:+1 / 01b:+2 / 10b:+4 / 11b: prohibited	0h	00h	S
		1					
		2		Fixed to 0	0		-
		3		Fixed to 0	0		-
		4		Fixed to 0	0		-
		5		Fixed to 0	0		-
		6		Fixed to 0	0		-
		7		Fixed to 0	0		-

Address		Bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
63h to BFh	3563h to 35BFh	[7:0] to [7:0]		Do not rewrite	-	-	-
C0h	35C0h	0	BLKLEVEL [11:0]	LSB	03Ch	3Ch	V
		1					
		2					
		3					
		4					
		5		Black level offset value setting Set to “000h” when using Pattern Generator			
		6					
		7					
C1h	35C1h	0				00h	
		1					
		2					
		3		MSB			
		4		Fixed to 0	0		-
		5		Fixed to 0	0		-
		6		Fixed to 0	0		-
		7		Fixed to 0	0		-

7.2. Common setting item for the PG

The output area of the PG pattern is the effective area of each mode. (The area shown in the blue of the following figure is output area.) In a pattern (0, 4, 5, 6) that specifies the location, the origin of horizontal is the next pixel of SAV 4th and the origin of vertical is the next line of frame information line. By the register PGTHRU, the background can be selected to "Fixed 0h (pattern 0, 6)" and "Setting PGDATA2 (pattern 4, 5)" and "Through" (imaging data). The figure below shows the details.



PG settings

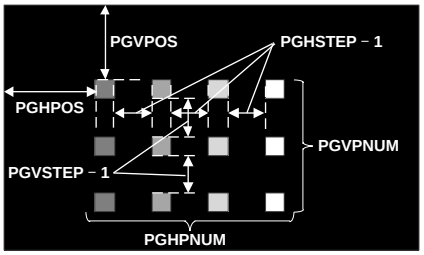
The output range for each output resolution is limited with the value of the following table.

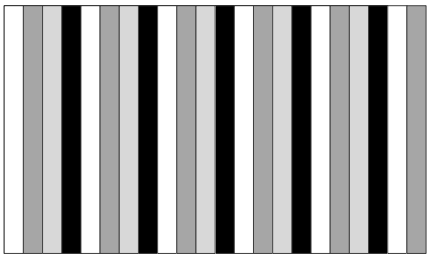
The range of the signal output

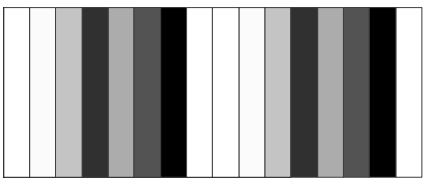
Resolution	Output value	
	Min.	Max.
8bit	01h	FEh
10bit	001h	3FEh
12bit	001h	FFEh

7.3. List of Pattern

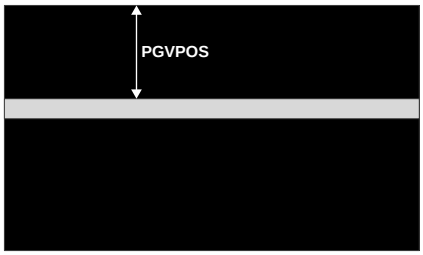
The pattern which it outputs by this function is shown below.

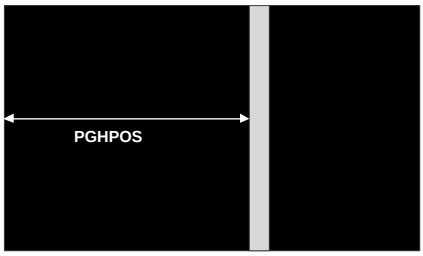
0. Multiple pixels Pattern		
Register	Pattern	Notes
PGMODE = 00h PGDATA1 PGDATA2 PGHPOS PGVPOS PGHPSTEP PGVPSTEP PGHPNUM PGVPNUM		Generate multiple pixels pattern. PGDATA1: Data pattern at the location specified by PGVPOS and PGHPOS The output level of the next point to the right is PGDATA1 + PGDATA2. Since (every each vertical line) The output level is increasing at PGDATA1 + PGDATA2 × n (n = 2, 3, 4…). It clips with the MAX value and returns to the startup level. PGVPOS: Specify the vertical start address PGHPOS: Specify the horizontal start address PGHPSTEP: Interval of horizontal pixels (0h is prohibited) PGVPSTEP: Interval of vertical pixels (0h is prohibited) PGHPNUM: Number of horizontal pixels (0h is prohibited) PGVPNUM: Number of vertical pixels (0h is prohibited)

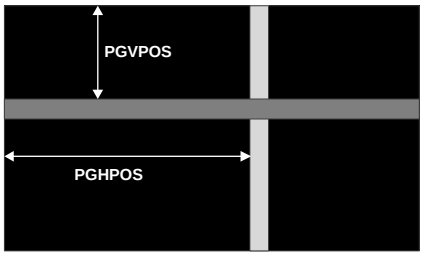
1. Sequence Pattern 1		
Register	Pattern	Notes
PGMODE = 01h		Outputs the sequential pattern of 1 pixel width 12 bit: FFFh / 555h / AAAh / 000h 10 bit: 3FFh / 155h / 2AAh / 000h 8 bit: FFh / 55h / AAh / 00h

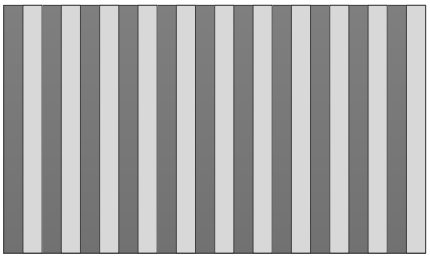
2. Sequence Pattern 2		
Register	Pattern	Notes
PGMODE = 02h		Outputs the following sequential pattern 12bit: FFFh / FFFh / FC0h / FC0h / C3Ch / C3Ch / 333h / 333h / AAAh / AAAh / 555h / 555h / 000h / 000h / FFFh / FFFh 10bit: 3FFh / 3FFh / 3F0h / 3F0h / 30Fh / 30Fh / 0CCh / 0CCh / 2AAh / 2AAh / 155h / 155h / 000h / 000h / 3FFh / 3FFh 8bit: FFh / FFh / FCh / FCh / C3h / C3h / 33h / 33h / AAh / AAh / 55h / 55h / 00h / 00h / FFh / FFh

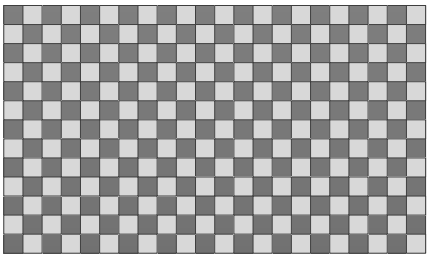
3. Gradation Pattern		
Register	Pattern	Notes
PGMODE = 03h PGHGSTEP		Outputs the following gradation pattern Minimum to Maximum* It reaches the max and increases from 000h again. * Maximum : 12 bit: 4095d 10 bit: 1023d 8 bit: 255d PGHGSTEP: increment 00b: +1 / 01b: +2 / 10b: +4 / 11b: prohibited

4. Horizontal 1 Row Pattern		
Register	Pattern	Notes
PGMODE = 04h PGDATA1 PGDATA2 PGVPOS		Outputs 1 row pattern with 1 pixel width at registered address. (Valid in the effective pixel region) PGDATA1: Specify the output value PGDATA2: Specify the background value PGVPOS: Specify the vertical address

5. Vertical 1 Column Pattern		
Register	Pattern	Notes
PGMODE = 05h PGDATA1 PGDATA2 PGHPOS		Outputs 1 column pattern with 1 pixel width at registered address. (Valid in the effective pixel region) PGDATA1: Specify the output value PGDATA2: Specify the background value PGHPOS: Specify the horizontal address

6. Horizontal 1 Row and Vertical 1 Column Pattern		
Register	Pattern	Notes
PGMODE = 06h PGDATA1 PGDATA2 PGHPOS PGVPOS		Outputs 1column/row pattern with 1 pixel width at registered address. (Valid in the effective pixel region) PGDATA1: Specify the output value of the column. PGDATA2: Specify the output value of the row. PGHPOS: Specify the horizontal address for column. PGVPOS: Specify the vertical address for row.

7. Stripe Pattern of the arbitrary value		
Register	Pattern	Notes
PGMODE = 07h PGDATA1 PGDATA2		Outputs the vertical stripe pattern of the arbitrary value by 1-pixel width. PGDATA1: Specify the output value PGDATA2: Specify the output value

8. Checks pattern of the arbitrary value		
Register	Pattern	Notes
PGMODE = 08h PGDATA1 PGDATA2		Outputs the checkered pattern of the one pixel spacing with the arbitrary value. PGDATA1: Specify the output value PGDATA2: Specify the output value

8. How to get sensor information

The sensor information of type name can be confirmed by reading the values of the register as shown below.
Register access is possible after power-on, standby cancel and wait for 29ms.
The details are referred to "Sensor Setting Flow" of datasheet.

8.1. Register map for sensor information

The Register map for sensor information is shown below.
Please refer to the datasheet for registers setup other than those lists.

Chip ID = 0Ah (Write: Chip ID = 0Ah, Read: Chip ID = 8Ah, I^2C: 38h)**

Address	bit	Register Name	Description	Reflection timing
16h	5		Type name Information	Read only
	6			
	7			
17h	[6:0]			

8.2. The description of reading data

8.2.1. Type name Information

Data	Type name
1 1 1 1 0 1 1 1 1 0	IMX990
1 1 1 1 0 1 1 1 1 1	IMX991

9. Lens design guideline

This section describes the information to select the lens.

9.1. Optical system

9.1.1. IMX990 Optical dimension

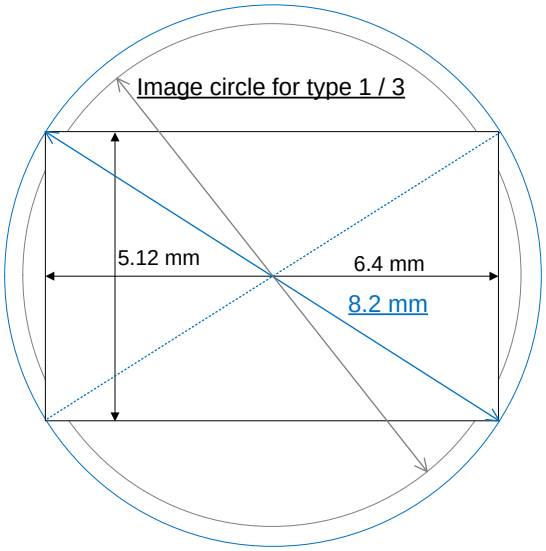
◆ Image size
All-pixel scan mode: Diagonal 8.2 mm (type 1 / 2)

◆ Number of recommended recording pixels
All-pixel scan mode: 1280 (H) × 1024 (V) approx. 1.31 M pixels

◆ Unit cell size
5 µm (H) × 5 µm (V)

◆ Recommended Exit Pupil Distance
- 100 mm to - ∞

Image formation on this image sensor with the lens for type 1.0 is shown below.



All-pixel

Relation between Image Circle and the Pixel Area

9.1.2. IMX991

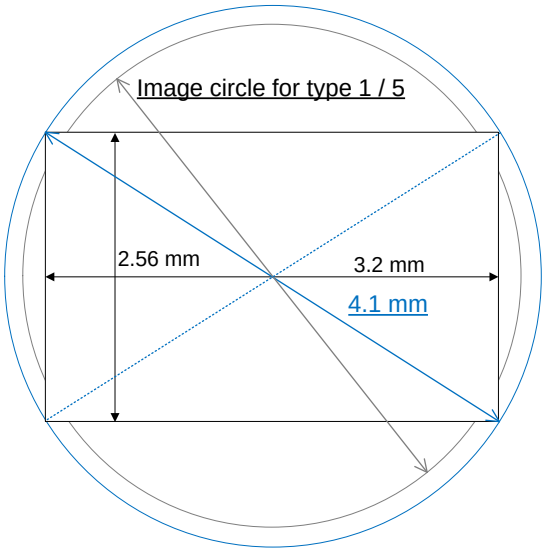
◆ Image size
All-pixel scan mode: Diagonal 4.1 mm (type 1 / 4)

◆ Number of active pixels
All-pixel scan mode: 640 (H) × 512 (V) approx. 0.33 M pixels

◆ Unit cell size
5 µm (H) × 5 µm (V)

◆ Recommended Exit Pupil Distance
- 100 mm to - ∞

Image formation on this image sensor with the lens for type 1.0 is shown below.



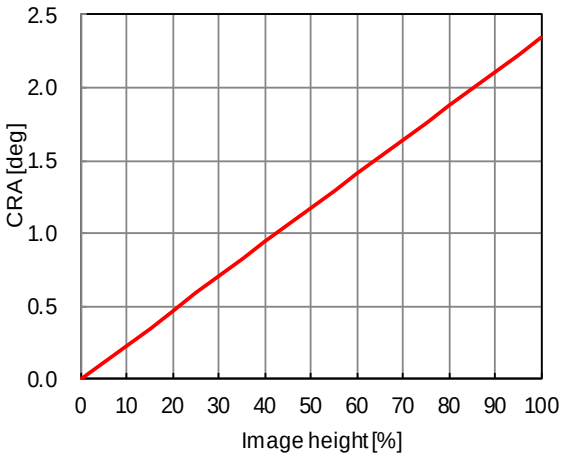
All-pixel

Relation between Image Circle and the Pixel Area

9.1.3. CRA characteristics of recommended lens

The recommended CRA characteristics are 0.0 degrees all over the image height (0 to 100 %), because the target E.P.D. is infinite.
*We assume that the worst case of E.P.D. is -100mm. The CRA characteristics of -100mm E.P.D. are described below. The real CRA should be smaller than the table below.

CRA characteristics of IMX990



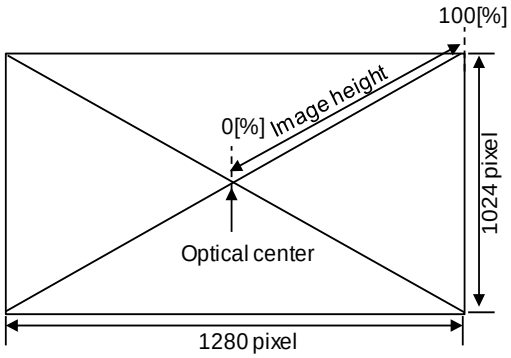


Image height		CRA
(%)	(mm)	(deg)
0	0.00	0.00
5	0.20	0.12
10	0.41	0.23
15	0.61	0.35
20	0.82	0.47
25	1.02	0.59
30	1.23	0.70
35	1.43	0.82
40	1.64	0.94
45	1.84	1.06
50	2.05	1.17
55	2.25	1.29
60	2.46	1.41
65	2.66	1.53
70	2.87	1.64
75	3.07	1.76
80	3.28	1.88
85	3.48	1.99
90	3.69	2.11
95	3.89	2.23
100	4.10	2.35

CRA characteristics of IMX991

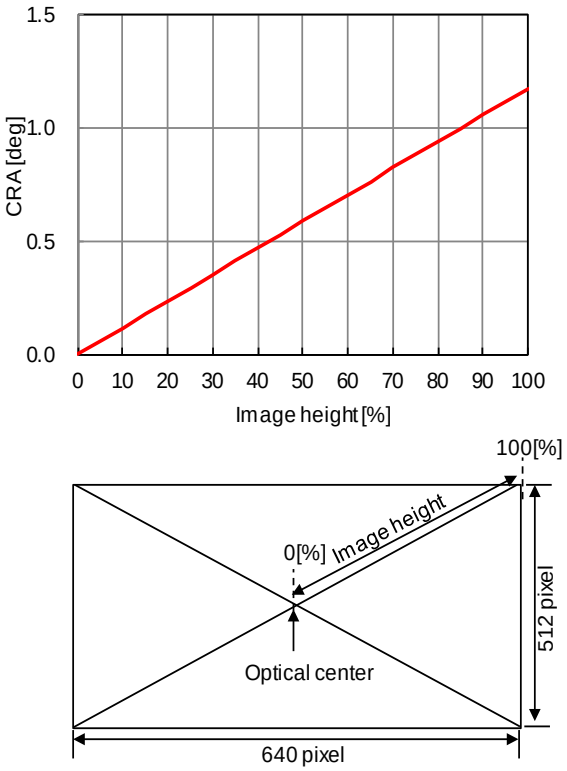
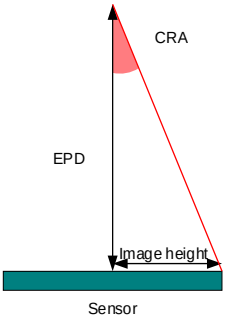


Image height		CRA
(%)	(mm)	(deg)
0	0.00	0.00
5	0.10	0.06
10	0.20	0.12
15	0.31	0.18
20	0.41	0.23
25	0.51	0.29
30	0.61	0.35
35	0.72	0.41
40	0.82	0.47
45	0.92	0.53
50	1.02	0.59
55	1.13	0.65
60	1.23	0.70
65	1.33	0.76
70	1.43	0.82
75	1.54	0.88
80	1.64	0.94
85	1.74	1.00
90	1.84	1.06
95	1.95	1.12
100	2.05	1.17

9.1.4. CRA characteristics

CRA (Chief Ray Angle) indicates the optimum angle of the chief ray for the image height, independent from the aperture size of the lens. This sensor assumes the recommended EPD (Recommended exit pupil distance) is farther than -100 mm and the angle of chief ray is theoretically directional light (perpendicular for the imaging plane). CRA characteristics table shown above is calculated with assuming short exit pupil distance case, precisely -100 mm.



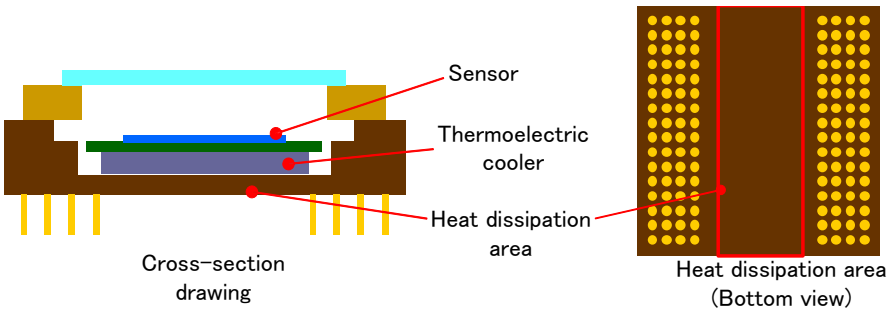
CRA characteristics

10. Heat dissipation when using thermoelectric cooler (IMX990-AABA, IMX991-AABA)

This section describes about the heat dissipation when using thermoelectric cooler.

10.1. Structure of IMX990-AABA and IMX991-AABA

The cross-section drawing and the heat dissipation area of this product is shown in the figure below.



The cross-section drawing and the heat dissipation area

The heat dissipation from the heat dissipation area on the package is necessary when cooling the sensor by the built-in thermoelectric cooler. The cooling performance may be degraded if the heat dissipation is not enough, .
.

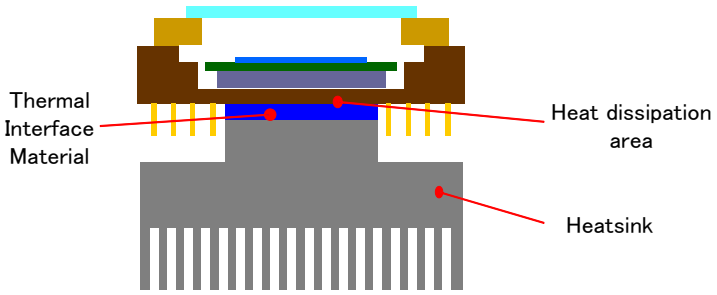
10.2. Heatsink Selection

Please select a heatsink which has enough cooling capacity because the cooling performance of the thermoelectric cooler depends on the heat dissipation environment.

10.3. Mounting heatsink

Please note the following.

(1) Make sure that there is no dust or dirt between the heatsink and the heat dissipation area.
(2) The contact area between the heatsink and the heat dissipation area should be as large as possible.
(3) It is recommended to insert a TIM (Thermal Interface Material) which has high adhesion and low thermal resistance on the contact area in order to reduce the thermal resistance between the heat sink and the heat dissipation area.



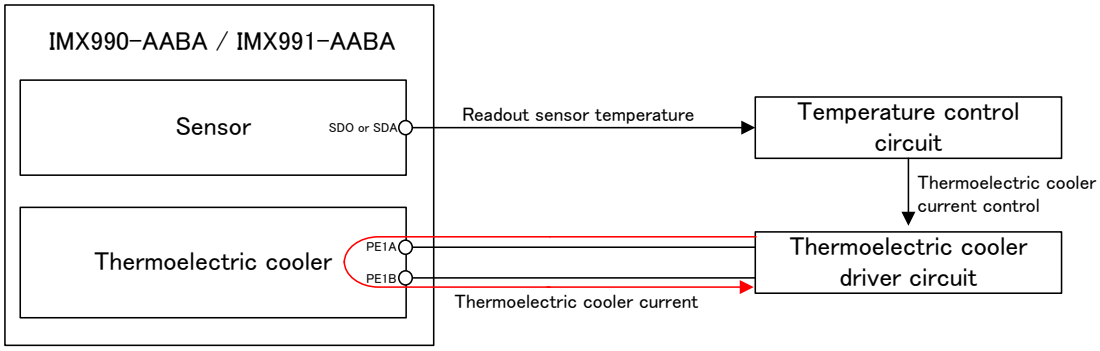
Example of mounting heatsink

11. Control of built-in thermoelectric cooler (IMX990-AABA, IMX991-AABA)

This section describes an example of built-in thermoelectric cooler control system.

11.1. Example of built-in thermoelectric cooler control system

The following describes an example of built-in thermoelectric cooler control system.



The example of controlling of built-in thermoelectric cooler

11.2. Explanation of each block

(1) IMX990-AABA / IMX991-AABA

This product includes the sensor and the thermoelectric cooler. The sensor has a built-in digital thermometer therefore the junction temperature of the sensor can be readout by the serial communication. Please refer to the section “Digital Thermometer” in the datasheet for the usage of the digital thermometer. The sensor temperature can be controlled by sending electric current between PE1A pin and PE1B pin of the thermoelectric cooler. The sensor is cooled when the electric current direction is from PE1A to PE1B. Note the direction of the electric current because the sensor is warmed when the electric current direction is from PE1B to PE1A.

(2) Temperature control circuit

This circuit readouts the sensor temperature by the serial communication, compares the sensor temperature with the setting temperature, and controls the electric current sent by the thermoelectric cooler driver circuit

(3) Thermoelectric cooler driver circuit

This circuit sends electric current between PE1A pin and PE1B pin of the thermoelectric cooler according to the input from the temperature control circuit. The power supply and the ground of this circuit should not have the common impedance with the power supply and the ground of the sensor. Note that the voltage and the current between PE1A and PE1B must be within the absolute maximum ratings.

12. Revision History

Date of change	Revision	Page	Contain of change
2020 / 05 / 29	0.1	–	First edition