SONY

Diagonal 8.2 mm (Type 1 / 2) SWIR Image Sensor with Square Pixel

Tentative

IMX990-AABA-C

SenSWIR

Description

The IMX990-AABA-C is a diagonal 8.2 mm (Type 1 / 2) CMOS active pixel type solid-state image sensor with a square pixel array and 1.31 M effective pixels. This chip features a global shutter with variable charge-integration time. This chip has a wide waveband (0.4 µm to 1.7 µm) with high sensitivity, high resolution, low dark current and low power consumption.
(Applications: FA cameras, Scientific Researches)

Features

- ◆CMOS active pixel type dots
- ◆Visible + SWIR wideband sensor (0.4 µm to 1.7 µm)
- ◆Built-in timing adjustment circuit, H/V driver and serial communication circuit
- ◆Global shutter function
- ◆Input frequency
  37.125 MHz / 74.25 MHz / 54 MHz
- ◆Number of recommended recording pixels: 1280 (H) × 1024 (V) approx. 1.31 M pixels

  Readout mode
  All - pixel scan mode
  Vertical / Horizontal 1 / 2 Subsampling mode
  ROI mode
  Vertical / Horizontal - Normal / Inverted readout mode
- ◆8-bit / 10-bit / 12-bit A/D converter
- ◆Readout rate
  Maximum frame rate in

  All - pixel scan mode: 8bit : 134.73 frame/s, 10 bit: 125.27 frame/s, 12bit: 71.53 frame/s
- ◆Variable-speed shutter function (resolution 1 H units)
- ◆PGA function
  0 dB to 18 dB: Analog Gain (0.1 dB step)
  18.1 dB to 42 dB: Analog Gain: 18 dB + Digital Gain: 0.1 dB to 24 dB (0.1 dB step)
- ◆I/O interface
  SLVS (2 ch / 4 ch switching) output
- ◆Recommended exit pupil distance: –100 mm to -∞
- ◆Built-in digital thermometer
- ◆Built-in thermoelectoric cooler

*The registers on this document may be possibly changed.

Device Structure

- ◆ SWIR image sensor
- ◆ Image size
  Diagonal 8.2 mm (Type 1 / 2) Approx. 1.31 M pixels
- ◆ Total number of pixels
  1392 (H) × 1056 (V) Approx. 1.47 M pixels
- ◆ Number of effective pixels
  1296 (H) × 1032 (V) Approx. 1.34 M pixels
- ◆ Number of active pixels
  1296 (H) × 1032 (V) Approx. 1.34 M pixels
- ◆ Number of recommended recording pixels
  1280 (H) × 1024 (V) Approx. 1.31 M pixels
- ◆ Unit cell size
  5 µm (H) × 5 µm (V)
- ◆ Optical black
  Horizontal (H) direction: Front 0 pixels, rear 96 pixels
  Vertical (V) direction: Front 24 pixels, rear 0 pixels
- ◆ Substrate material
  Silicon
- ◆ FPA material
  InGaAs

Absolute Maximum Ratings

Item	Symbol	Rating			Unit	Remarks
Supply voltage (Analog 3.3 V)	AV_{DD1}	–0.3	to	+4.0	V	
Supply voltage (Analog 2.2 V)	AV_{DD2}	–0.3	to	+4.0	V	
Supply voltage (Interface 1.8 V)	OV_{DD}	–0.3	to	+3.3	V	
Supply voltage (Digital 1.2 V)	DV_{DD}	–0.3	to	+2.0	V	
Supply voltage (Pixel 2.2V)	TV_{DD}	–0.3	to	+3.0	V	VDDFM
Supply voltage (Pixel 1.2V)	BV_{DD}	–0.3	To	+2.0	V	VDDDR
Input voltage	VI	–0.3	to	OV_{DD} +0.3	V	Not exceed 3.3 V
Output voltage	VO	–0.3	to	OV_{DD} +0.3	V	Not exceed 3.3 V
Operating temperature	Topr1	0	to	+75	˚C	Built-in digital thermometer output value
	Topr2	0	to	+75	˚C	Ta
Storage temperature	Tstg	–40	to	+85	˚C	
Thermoelectric cooler voltage	Vcooler	–9.6	to	+9.6	V	Voltage difference between PE1A and PE1B
Thermoelectric cooler current	Icooler	–1.8	to	+1.8	A	Current from PE1A to PE1B

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (Analog 3.3 V)	AV_{DD1}	3.15	3.30	3.45	V
Supply voltage (Analog 2.2 V)	AV_{DD2}	2.10	2.20	2.30	V
Supply voltage (Interface 1.8 V)	OV_{DD}	1.70	1.80	1.90	V
Supply voltage (Digital 1.2 V)	DV_{DD}	1.10	1.20	1.30	V
Supply voltage (Pixel 2.2V)	TVdd	2.15	2.20	2.25	V
Supply voltage (Pixel 1.2V)	BVdd	1.15	1.20	1.25	V
Performance guarantee temperature	Tspec	—	+15*	—	˚C

*Built-in digital thermometer output value

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General-0.0.9

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    Chip ID = 04 (Write: Chip ID = 04h, Read: Chip ID = 84h, I^2C: 32**h) ... 42
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    Chip ID = 0C (Write: Chip ID = 0Ch, Read: Chip ID = 8Ch, I^2C: 3A**h) ... 49
    Chip ID = 10 (Write: Chip ID = 10h, Read: Chip ID = 90h, I^2C: 3E**h) ... 49
    Chip ID = 11 (Write: Chip ID = 11h, Read: Chip ID = 91h, I^2C: 3F**h) ... 49
    Chip ID = 12 (Write: Chip ID = 12h, Read: Chip ID = 92h, I^2C: 40**h) ... 49
    Chip ID = 13 (Write: Chip ID = 13h, Read: Chip ID = 93h, I^2C: 41**h) ... 49

Chip ID = 14 (Write: Chip ID = 14h, Read: Chip ID = 94h, I²C: 42**h) 49
Chip ID = 15 (Write: Chip ID = 15h, Read: Chip ID = 95h, I²C: 43**h) 49
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Chip ID = 17 (Write: Chip ID = 17h, Read: Chip ID = 97h, I²C: 45**h) 49
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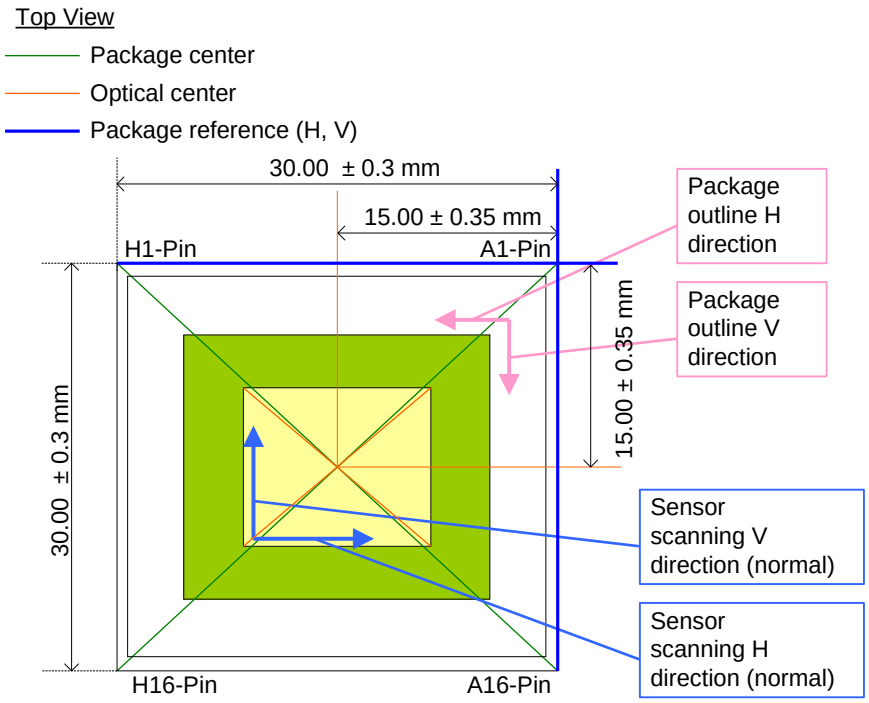
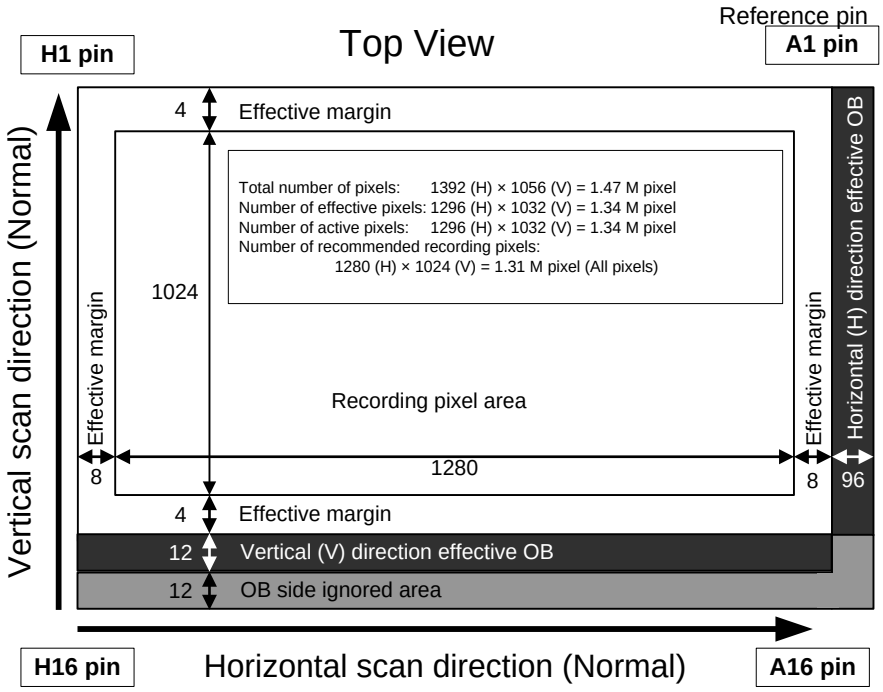
Chip Center and Optical Center (TBD)



Optical Center

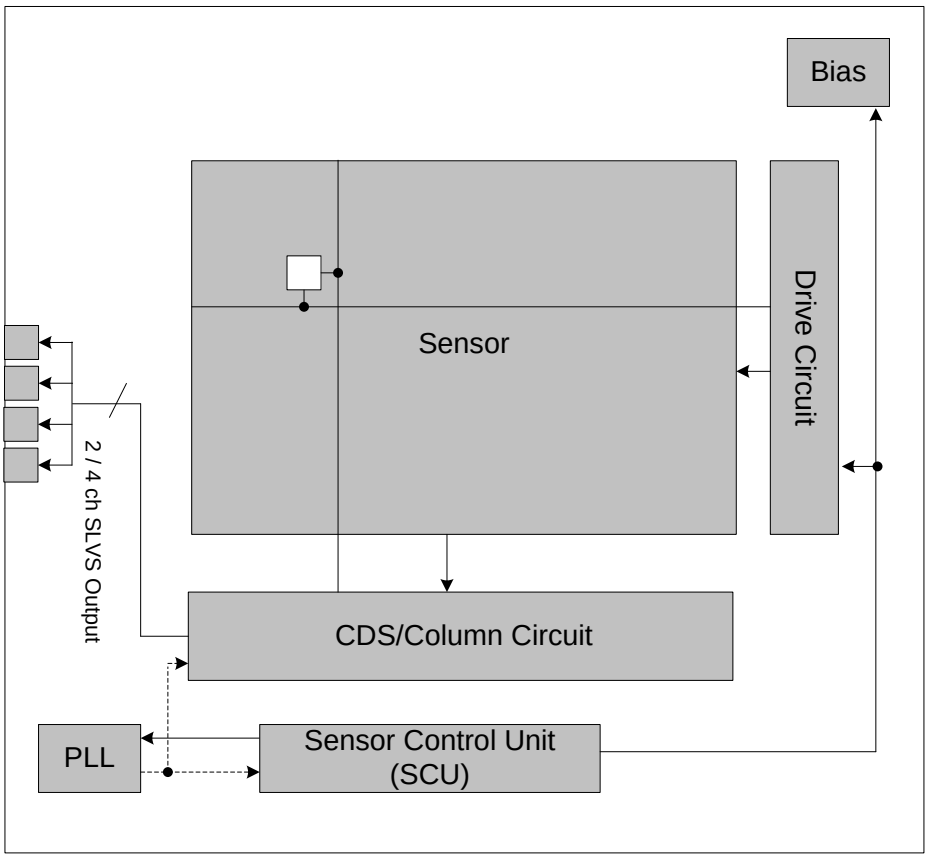
Pixel Arrangement



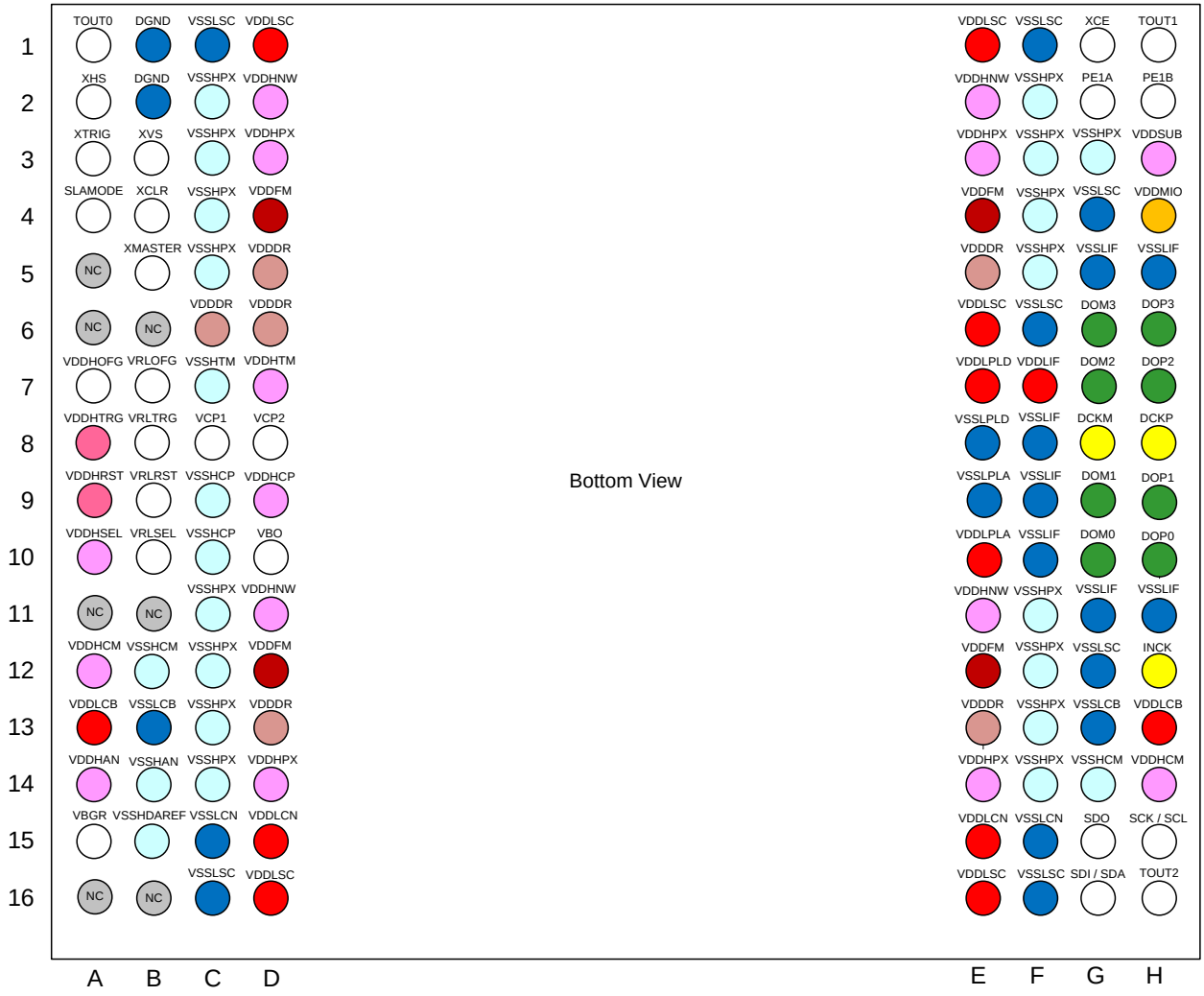
Pixel Arrangement

Block Diagram and Pin Configuration

(Top View)



Block Diagram



- 3.3 V Analog Power Supply
- 2.2 V Analog Power Supply
- 1.8 V I/O Power Supply
- 1.2 V Digital Power Supply
- 1.2 V Pixel Power Supply
- 2.2 V Pixel Power Supply
- 3.3V GND
- Signal I/O
- 1.2 / 1.8V GND
- Data output
- Clock

Pin Configuration

Pin Description

No.	Pin No.	I/O	Analog / Digital	Symbol	Description
1	A1	O	D	TOUT0	Pulse0 output pin
2	A2	I/O	D	XHS	Horizontal sync signal
3	A3	I	D	XTRIG	Trigger input 1
4	A4	I	D	SLAMODE	Slave address select (37h: High, 36h: Low, 1Ah: both polarities)
5	A5	—	—	N.C.	—
6	A6	—	—	N.C.	—
7	A7	Power	A	VDDHOFG	connect to VBO
8	A8	Power	A	VDDHTRG	2.2 V power supply
9	A9	Power	A	VDDHRST	2.2 V power supply
10	A10	Power	A	VDDHSEL	3.3 V power supply
11	A11	—	—	N.C.	—
12	A12	Power	A	VDDHCM	3.3 V power supply
13	A13	Power	A	VDDLCB	1.2 V power supply
14	A14	Power	A	VDDHAN	3.3 V power supply
15	A15	O	A	VBGR	Connect to 0.22 µF to GND
16	A16	—	—	N.C.	—
17	B1	—	—	DGND	Connect to 1.2V GND
18	B2	—	—	DGND	Connect to 1.2V GND
19	B3	I/O	D	XVS	Vertical sync signal
20	B4	I	D	XCLR	System clear (Normal: High, Clear: Low)
21	B5	I	D	XMASTER	Master / Slave select
22	B6	—	—	N.C.	—
23	B7	I	A	VRLOFG	Connect to VCP1
24	B8	I	A	VRLTRG	Connect to VCP1
25	B9	I	A	VRLRST	Connect to VCP1
26	B10	I	A	VRLSEL	Connect to VCP2
27	B11	—	—	N.C.	—
28	B12	GND	A	VSSHCM	3.3 V GND
29	B13	GND	A	VSSLCB	1.2 V GND
30	B14	GND	A	VSSHAN	3.3 V GND
31	B15	GND	A	VSSHDAREF	3.3 V GND
32	B16	—	—	N.C.	—
33	C1	GND	D	VSSLSC	1.2 V GND
34	C2	GND	A	VSSHPX	3.3 V GND
35	C3	GND	A	VSSHPX	3.3 V GND
36	C4	GND	A	VSSHPX	3.3 V GND
37	C5	GND	A	VSSHPX	3.3 V GND
38	C6	Power	A	VDDDR	1.2 V pixel power supply
39	C7	GND	A	VSSHTM	3.3 V GND
40	C8	O	A	VCP1	Connect to VRLOFG, VRLRST, VRLTRG (Connect to 4.7 µF × 2 to GND)
41	C9	GND	A	VSSHCP	3.3 V GND
42	C10	GND	A	VSSHCP	3.3 V GND
43	C11	GND	A	VSSHPX	3.3 V GND
44	C12	GND	A	VSSHPX	3.3 V GND
45	C13	GND	A	VSSHPX	3.3 V GND
46	C14	GND	A	VSSHPX	3.3 V GND
47	C15	GND	D	VSSLCN	1.2 V GND
48	C16	GND	D	VSSLSC	1.2 V GND
49	D1	Power	D	VDDLSC	1.2 V power supply
50	D2	Power	A	VDDHNW	3.3 V power supply
51	D3	Power	A	VDDHPX	3.3 V power supply
52	D4	Power	A	VDDFM	2.2 V pixel power supply
53	D5	Power	A	VDDDR	1.2 V pixel power supply
54	D6	Power	A	VDDDR	1.2 V pixel power supply
55	D7	Power	A	VDDHTM	3.3 V power supply
56	D8	O	A	VCP2	Connect to VRLSEL (Connect to 4.7 µF × 2 to GND)
57	D9	Power	A	VDDHCP	3.3 V power supply
58	D10	O	A	VBO	Connect to VDDHOFG (Connect to 4.7 µF × 2 to GND)
59	D11	Power	A	VDDHNW	3.3 V power supply

No.	Pin No.	I/O	Analog / Digital	Symbol	Description
60	D12	Power	A	VDDFM	2.2 V pixel power supply
61	D13	Power	A	VDDDR	1.2 V pixel power supply
62	D14	Power	A	VDDHPX	3.3 V power supply
63	D15	Power	D	VDDLCN	1.2 V power supply
64	D16	Power	D	VDDLSC	1.2 V power supply
65	E1	Power	D	VDDLSC	1.2 V power supply
66	E2	Power	A	VDDHNW	3.3 V power supply
67	E3	Power	A	VDDHPX	3.3 V power supply
68	E4	Power	A	VDDFM	2.2 V pixel power supply
69	E5	Power	A	VDDDR	1.2 V pixel power supply
70	E6	Power	D	VDDLSC	1.2 V power supply
71	E7	Power	D	VDDLPLD	1.2 V power supply
72	E8	GND	D	VSSLPLD	1.2 V GND
73	E9	GND	D	VSSLPLA	1.2 V GND
74	E10	Power	D	VDDLPLA	1.2 V power supply
75	E11	Power	A	VDDHNW	3.3 V power supply
76	E12	Power	A	VDDFM	2.2 V pixel power supply
77	E13	Power	A	VDDDR	1.2 V pixel power supply
78	E14	Power	A	VDDHPX	3.3 V power supply
79	E15	Power	D	VDDLCN	1.2 V power supply
80	E16	Power	D	VDDLSC	1.2 V power supply
81	F1	GND	D	VSSLSC	1.2 V GND
82	F2	GND	A	VSSHPX	3.3 V GND
83	F3	GND	A	VSSHPX	3.3 V GND
84	F4	GND	A	VSSHPX	3.3 V GND
85	F5	GND	A	VSSHPX	3.3 V GND
86	F6	GND	D	VSSLSC	1.2 V GND
87	F7	Power	D	VDDLIF	1.2 V power supply
88	F8	GND	D	VSSLIF	1.2 V GND
89	F9	GND	D	VSSLIF	1.2 V GND
90	F10	GND	D	VSSLIF	1.2 V GND
91	F11	GND	A	VSSHPX	3.3 V GND
92	F12	GND	A	VSSHPX	3.3 V GND
93	F13	GND	A	VSSHPX	3.3 V GND
94	F14	GND	A	VSSHPX	3.3 V GND
95	F15	GND	D	VSSLCN	1.2 V GND
96	F16	GND	D	VSSLSC	1.2 V GND
97	G1	I	D	XCE	4 - wire: Serial communication I/F XCE pin
98	G2	I	A	PE1A	Built-in thermoelectric cooler pin (+)
99	G3	GND	A	VSSHPX	3.3 V GND
100	G4	GND	D	VSSLSC	1.2 V GND
101	G5	GND	D	VSSLIF	1.2 V GND
102	G6	O	D	DOM3	SLVS IF output (Data)
103	G7	O	D	DOM2	SLVS IF output (Data)
104	G8	O	D	DCKM	Digital output timing clock
105	G9	O	D	DOM1	SLVS IF output (Data)
106	G10	O	D	DOM0	SLVS IF output (Data)
107	G11	GND	D	VSSLIF	1.2 V GND
108	G12	GND	D	VSSLSC	1.2 V GND
109	G13	GND	A	VSSLCB	1.2 V GND
110	G14	GND	A	VSSHCM	3.3 V GND
111	G15	O	D	SDO	4-wire: Serial communication I/F SDO pin I2C: OPEN
112	G16	I/O	D	SDI / SDA	4-wire: Serial communication I/F SDI pin I2C: Serial data line
113	H1	O	D	TOUT1	Pulse1 output pin
114	H2	I	A	PE1B	Built-in thermoelectric cooler pin (-)
115	H3	Power	A	VDDSUB	3.3 V power supply
116	H4	Power	D	VDDMIO	1.8 V power supply
117	H5	GND	D	VSSLIF	1.2 V GND
118	H6	O	D	DOP3	SLVS IF output (Data)
119	H7	O	D	DOP2	SLVS IF output (Data)
120	H8	O	D	DCKP	Digital output timing clock
121	H9	O	D	DOP1	SLVS IF output (Data)
122	H10	O	D	DOP0	SLVS IF output (Data)
123	H11	GND	D	VSSLIF	1.2 V GND
124	H12	I	D	INCK	Master clock input

No.	Pin No.	I/O	Analog / Digital	Symbol	Description
125	H13	Power	A	VDDLCB	1.2 V power supply
126	H14	Power	A	VDDHCM	3.3 V power supply
127	H15	I	D	SCK / SCL	4 - wire: Serial communication I/F SCK pin I2C: Serial clock line"
128	H16	O	D	TOUT2	Pulse2 output pin

* N.C. pins in the table above should be left open on the board.

Electrical Characteristics

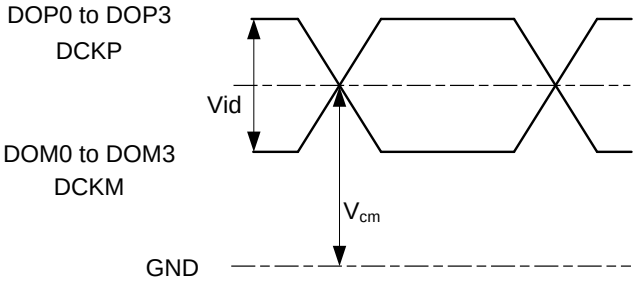
DC Characteristics

Item		Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Analog (3.3 V)	$V_{DD}Hx$[*1]	AV_{DD1}	—	3.15	3.30	3.45	V
	Analog (2.2 V)	VDDHTRG, VDDHRST	AV_{DD2}	—	2.1	2.2	2.3	V
	Interface	$V_{DD}Mx$	OV_{DD}	—	1.70	1.80	1.90	V
	Digital	$V_{DD}Lx$	DV_{DD}	—	1.10	1.20	1.30	V
	Pixel (2.2 V)	VDDFM	TV_{DD}	—	2.15	2.20	2.25	V
	Pixel (1.2 V)	VDDDR	BV_{DD}	—	1.15	1.20	1.25	V
Digital input voltage		XHS XVS XCLR INCK XMASTER SLAMODE SCK SDI XCE XTRIG	VIH	XVS / XHS in Slave mode	0.7 × OV_{DD}	—	—	V
			VIL		—	—	0.3 × OV_{DD}	V
Digital output voltage		XHS XVS SDO TOUT0 TOUT1 TOUT2	VOH	XVS / XHS in Master mode	OV_{DD} -0.4	—	—	V
			VOL		—	—	0.4	V

[*1] Except for VDDHTRG and VDDHRST

SLVS Output DC Characteristics

Single end output



Definition of the characteristics of SLVS (Single end output)

Symbol	Item	Min.	Typ.	Max.	Unit	Remarks
Ro	Sensor output impedance	30	—	65	Ω	—
Vcm	Voltage center	150	—	250	mV	[*1]
|Vid|	Differential voltage	140	—	300	mV	[*1]

[*1] Rin = 100Ω.

Power Consumption

Item	Pins	Symbol	Typ.	Max.	Unit
Operating current SLVS 4 ch 10 bit 125.27 frame/s	$V_{DD}H$ *1	IAV_{DD1}	62	150	mA
	VDDHRST VDDHTRG	IAV_{DD2}	1 *2	2 *2	mA
	$V_{DD}M$	IOV_{DD}	1	2	mA
	$V_{DD}L$	IDV_{DD}	140	240	mA
	VDDFM	ITV_{DD}	1	2	mA
	VDDDR	IBV_{DD}	1	2	mA
Standby current	$V_{DD}H$ *1	IAV_{DD1}_STB	—	1	mA
	VDDHRST VDDHTRG	IAV_{DD2}_STB	—	0.1 *2	mA
	$V_{DD}M$	IOV_{DD}_STB	—	0.1	mA
	$V_{DD}L$	IDV_{DD}_STB	—	10	mA
	VDDFM	ITV_{DD} _STB	—	0.1	mA
	VDDDR	IBV_{DD} _STB	—	0.1	mA

*1 Except for VDDHTRG and VDDHRST

*2 Summation of VDDHTRG and VDDHRST

Operating current:

(Typical value condition) : Supply voltage: 3.30 V / 2.20 V / 1.80 V / 1.20 V / 2.2 V / 1.2 V, Tj = 15 ˚C

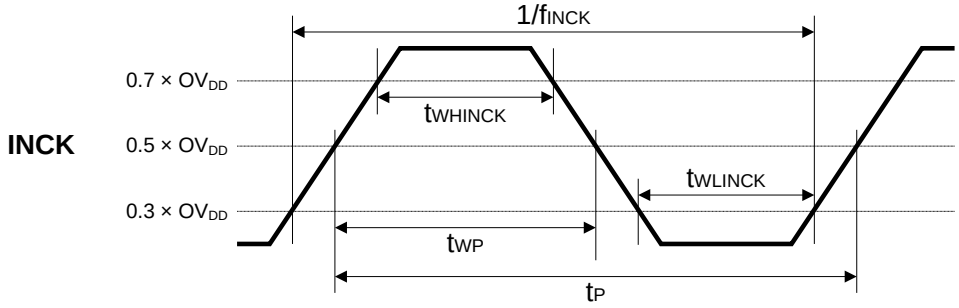
(Maximum value condition) : Supply voltage: 3.45 V / 2.30 V / 1.90 V / 1.30 V / 2.25V / 1.25 V, Tj = 15 ˚C
Worst state of internal circuit operating current consumption.

Standby current:

(Maximum value condition) : Supply voltage: 3.45 V / 2.30 V / 1.90 V / 1.30 V / 2.25V / 1.25 V, Ta = 15 ˚C,
INCK = 0 V, Thermoelectric cooler OFF
The device in the light-obstructed state.

AC Characteristics

Master Clock (INCK) Waveform Diagram

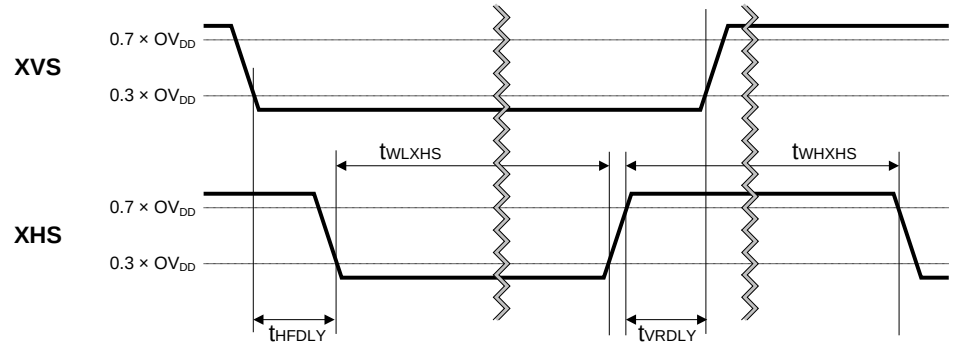


Duty Ratio = t_{WP} / t_P × 100

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	f_{INCK} × 0.96	f_{INCK}	f_{INCK} × 1.02	MHz	f_{INCK} = 37.125 MHz, 74.25 MHz, 54 MHz
INCK Low level pulse width	t_{WLINCK}	4	—	—	ns	
INCK High level pulse width	t_{WHINCK}	4	—	—	ns	
INCK clock duty	—	40.0	50.0	60.0	%	Define with 0.5 × OV_{DD}

* The INCK fluctuation affects the frame rate.

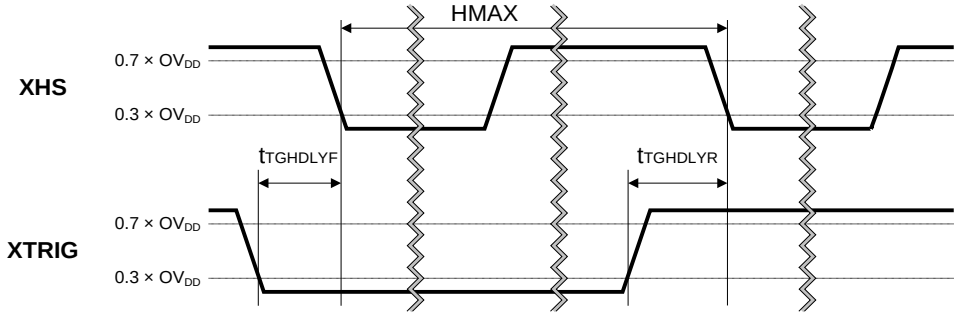
XVS / XHS Input Characteristics in Slave Mode (XMASTER = High)



Item	Symbol	Min.	Typ.	Max.	Unit
XHS Low level pulse width	t_{WLXHS}	$4/f_{INCK}$	—	—	ns
XHS High level pulse width	t_{WHXHS}	$4/f_{INCK}$	—	—	ns
XVS - XHS fall width	t_{HFDLY}	$1/f_{INCK}$	—	—	ns
XHS - XVS rise width	t_{VRDLY}	$1/f_{INCK}$	—	—	ns

Synchronization cannot be performed from XVS and XHS signal in mater mode. Detect the sync code.

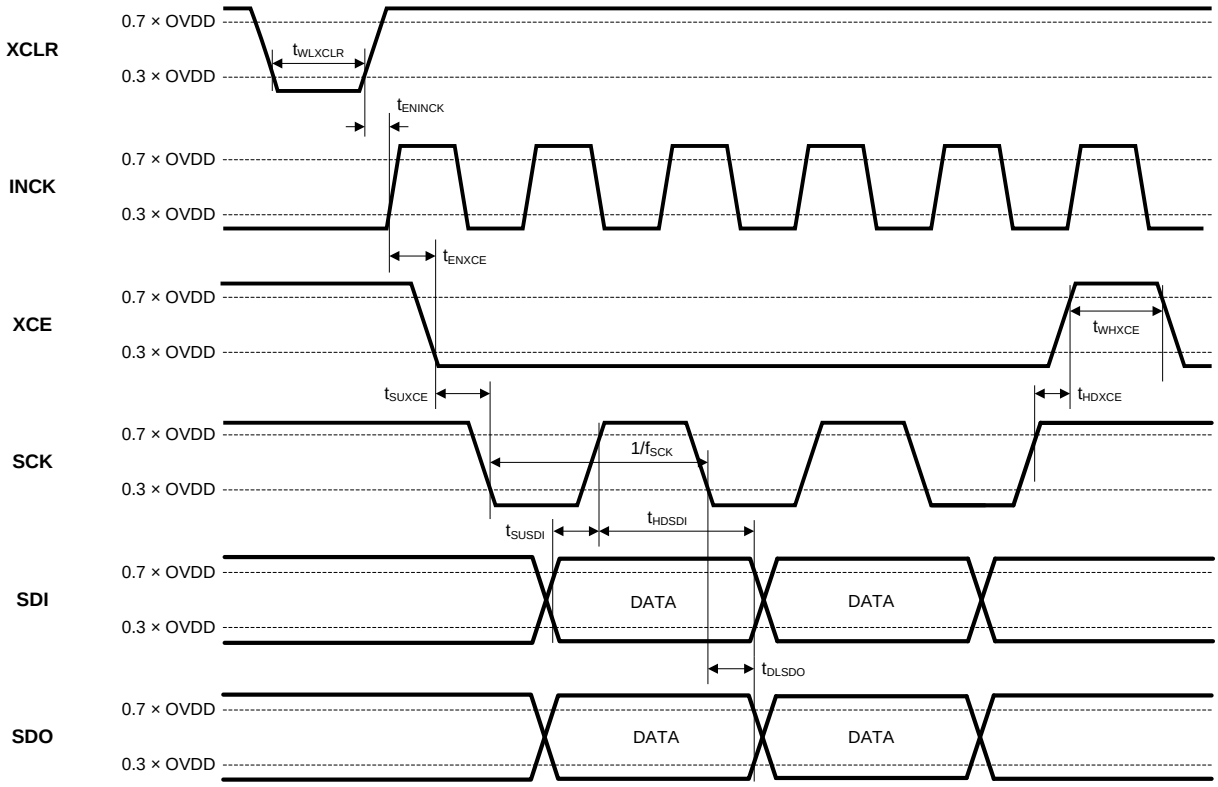
XTRIG Input Characteristics in Slave Mode (XMASTER = High) only



Item	Symbol	Min.	Typ.	Max.	Unit
XTRIG fall - XHS fall width	$t_{TGHDLYF}$	10	—	HMAX-10	INCK
XTRIG rise - XHS fall width	$t_{TGHDLYR}$	10	—	HMAX-10	INCK

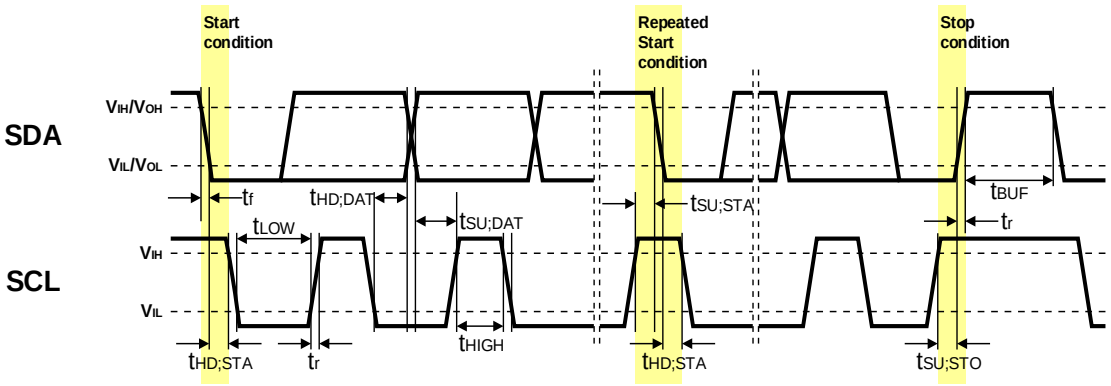
Serial Communication

4-wire



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCK clock frequency	f_{SCK}	—	—	13.5	MHz	
XCLR Low level pulse width	t_{WLXCLR}	$4/f_{INCK}$	—	—	ns	
INCK effective margin	t_{ENINCK}	1	—	—	µs	
XCE effective margin	t_{ENXCE}	20	—	—	µs	
XCE input setup time	t_{SUXCE}	20	—	—	ns	
XCE input hold time	t_{HDXCE}	20	—	—	ns	
XCE High level pulse width	t_{WHXCE}	20	—	—	ns	
SDI input setup time	t_{SUSDI}	10	—	—	ns	
SDI input hold time	t_{HDSDI}	10	—	—	ns	
SDO output delay time	t_{DLSDO}	0	—	25	ns	Output load capacitance: 20 pF

I²C



I²C Specification

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Low level input voltage	V_{IL}	-0.3	—	0.3 × OV_{DD}	V	
High level input voltage	V_{IH}	0.7 × OV_{DD}	—	1.9	V	
Low level output voltage	V_{OL}	0	—	0.2 × OV_{DD}	V	OV_{DD} < 2 V, Sink 3 mA
High level output voltage	V_{OH}	0.8 × OV_{DD}	—	—	V	
Output fall time	tof	—	—	250	ns	Load 10 pF – 400 pF, 0.7 × OV_{DD} – 0.3 × OV_{DD}
Input current	Ii	-10	—	10	µA	0.1 × OV_{DD} – 0.9 × OV_{DD}
Capacitance for SCK (/SCL) , SDI (/SDA)	Ci	—	—	10	pF	

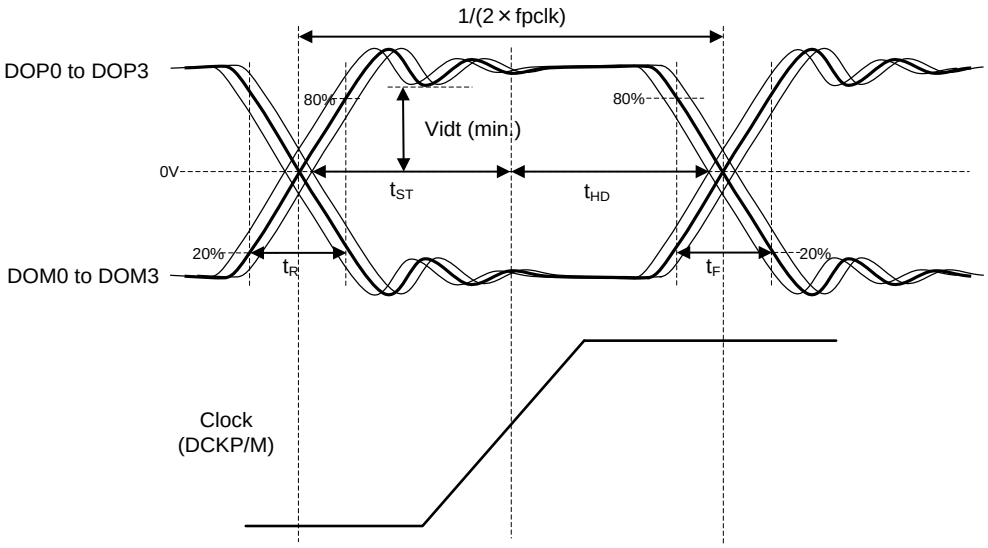
I²C AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	0	—	400	kHz
Hold time (Start Condition)	t_{HDSTA}	0.6	—	—	µs
Low period of the SCL clock	t_{LOW}	1.3	—	—	µs
High period of the SCL clock	t_{HIGH}	0.6	—	—	µs
Set-up time (Repeated Start Condition)	t_{SUSTA}	0.6	—	—	µs
Data hold time	t_{HDDAT}	0	—	0.9	µs
Data set-up time	t_{SUDAT}	100	—	—	ns
Rise time of both SDA and SCL signals	t_R	—	—	300	ns
Fall time of both SDA and SCL signals	t_F	—	—	300	ns
Set-up time (Stop Condition)	t_{SUSTO}	0.6	—	—	µs
Bus free time between a Stop and Start Condition	t_{BUF}	1.3	—	—	µs

SLVS Output AC Characteristics

Symbol	Item	Min.	Typ.	Max.	Unit	Remarks
f_{clk}	Output frequency	—	594	—	Mbps	—
f_{pclk}	Clock frequency	—	297	—	MHz	—
t_{ST}	Setup time	505	—	—	ps	*1
t_{HD}	Hold time	505	—	—	ps	*1
t_R	DOP/DOM rise time	—	—	300	ps	*1, *2
t_F	DOP/DOM fall time	—	—	300	ps	*1, *2
|Vidt|	Differential voltage	140	—	—	mV	*1

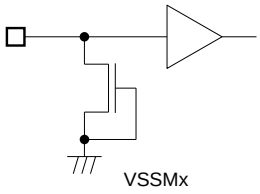
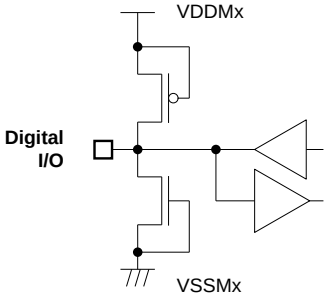
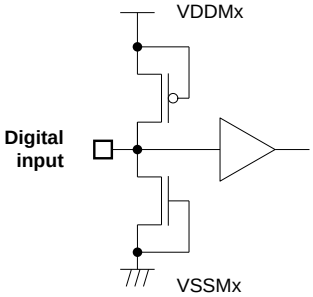
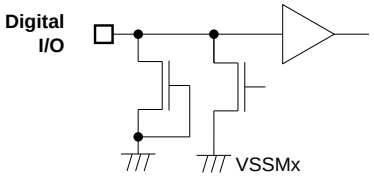
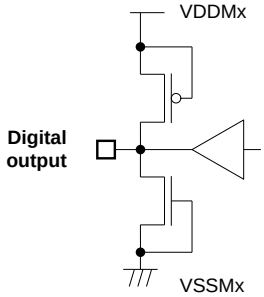
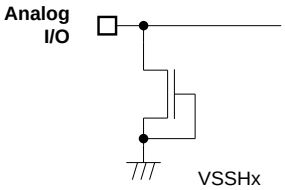
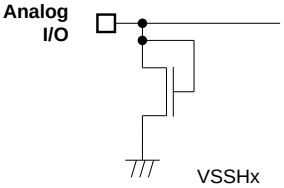
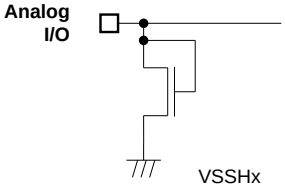
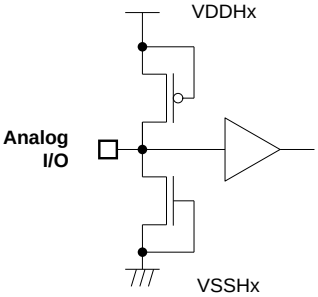
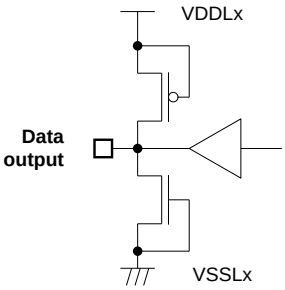
*1 Rin = 100Ω
*2 Differential 20% - 80%



Define of the characteristics of the SLVS

I/O Equivalent Circuit Diagram

□ : External pin

Symbol	Equivalent circuit	Symbol	Equivalent circuit
INCK		XVS XHS	
XCLR XCE XMASTER XTRIG SLAMODE		SDI / SDA SCK / SCL	
SDO		VBO VDDHOFG	
VCP1 VCP2		VRLOFG VRLTRX VRLTRY VRLSEL VRLTRG	
VBGR		DOPx DOMx DCKP DCKM x : 0 to 3	

Spectral Sensitivity Characteristics

(Tj = 15 ˚C, Characteristics in the package status)

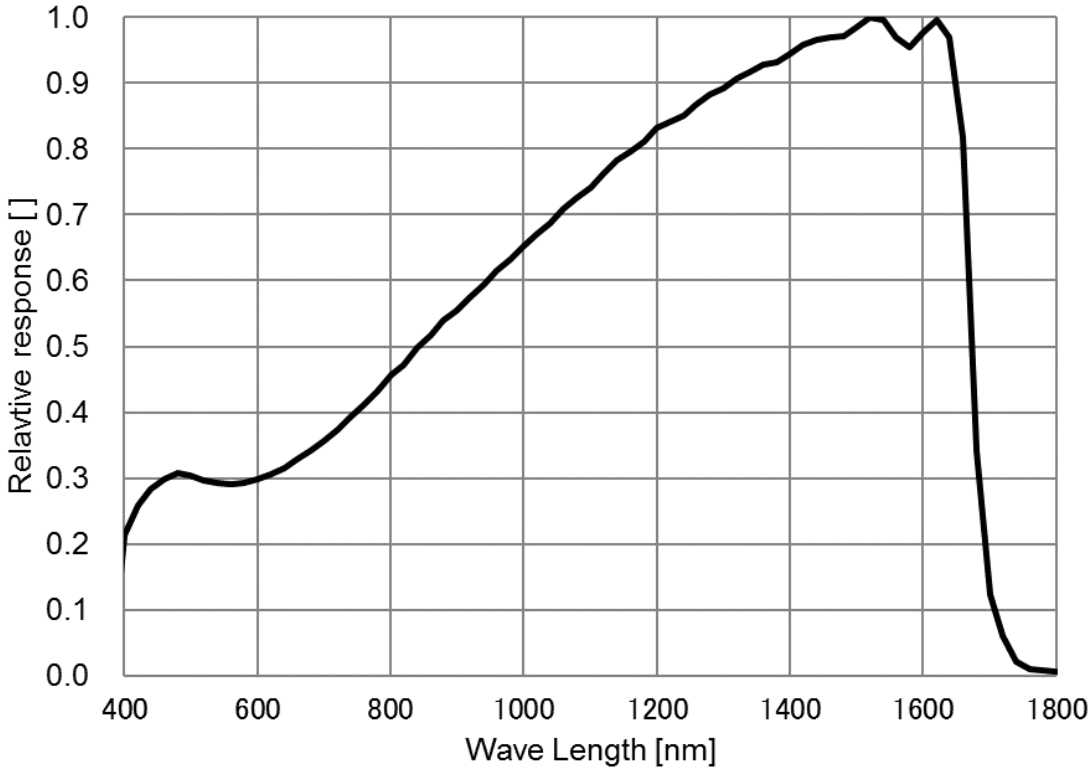


Image Sensor Characteristics

(AV_{DD1} = 3.3 V, AV_{DD2} = 2.2 V, TV_{DD} = 2.2 V, BV_{DD} = 1.2 V, OV_{DD} = 1.8 V, DV_{DD} = 1.2 V, All pixel scan mode, AD: 10 bit, Tj = 15 ˚C, Gain = 0 dB)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
Sensitivity	S	291 (102.7)	343 (121)	—	Digit (mV)	1	1/30 s storage
Saturation signal	Vsat2D	1022 (361[*1])	—	—	Digit (mV)	2	Zone 0 ～ II'
Video signal shading	SH01	—	—	20	%	3	Zone 0, I
	SH2D	—	—	25	%		Zone 0 ～ II'
Dark signal	Vdt	—	—	2.83 (1.0)	Digit (mV)	4	1/30 s storage
Dark signal shading	ΔVdt	—	—	4.53 (1.6)	Digit (mV)	5	1/30 s storage

Note) 1. Converted value into mV using 1Digit = 0.08823mV for 12-bit output, 1Digit = 0.3529 mV for 10-bit output, and 1Digit = 0.3529 mV for 8-bit output.
2. The video signal shading is the measured value in the wafer status and does not include characteristics of the seal glass.

[*1] In case of 8 bit, Vsat2D becomes 1/4 of it at 10 bit.

Zone Definition of Video Signal Shading

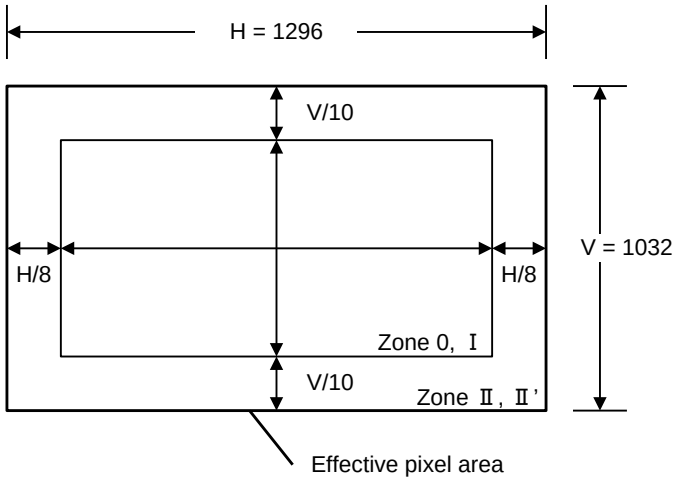


Image Sensor Characteristics Measurement Method

Measurement Conditions

In the following measurements, the device drive conditions are at the typical values of the bias conditions and clock voltage conditions.
In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the signal output of the measurement system.

Definition of standard imaging conditions

◆ Standard imaging condition I:
A light source with wavelength 1550 nm, full width at half maximum 50 nm, irradiance on the sensor surface 12.0 mW / m^2, and light uniformity on the sensor surface within ± 2.5% is used at F = 8.0 environment.

◆ Standard image condition II:
A light source with wavelength 1550 nm, full width at half maximum 50 nm, and light uniformity on the sensor surface within ± 2.5% is used. Irradiance on the sensor surface is adjusted in each testing item.

Measurement Method

1. Sensitivity
   Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/30 s, measure the signal outputs (S) at the center of the screen.

2. Saturation signal
   Set the measurement condition to the standard imaging condition II. After adjusting the luminous intensity to 10 times the intensity with the average value of the signal outputs, 121 mV, measure the minimum values of the signal outputs.

3. Video signal shading
   Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/30 s, measure the average value(Vave [mV]), the maximum value (Vmax [mV]) and the minimum value (Vmin [mV]) of the signal outputs, and substitute the values into the following formula.

   $$SH = (Vmax – Vmin) / Vave \times 100 [\%]$$

4. Dark signal
   With the device junction temperature of 15 ˚C and the device in the light-obstructed state, divide the output difference between 1/3 s integration at 3 frame/s and 1/30 s integration at 30 frame/s by 9, and calculate the signal output converted to 1/30 s integration. Measure the average value of this output (Vdt [mV]).

5. Dark signal shading
   With the device junction temperature of 15 ˚C and the device in the light-obstructed state, measure the maximum value (Vdmax [mV]) and the minimum value (Vdmin [mV]) of the dark signal output converted to 1/30 s integration. The measuring values substitute into the following formula.

   $$\Delta Vdt = Vdmax – Vdmin [mV]$$

Setting Registers Using Serial Communication

Description of Setting Registers (4-wire)

The serial data input order is LSB-first transfer. The table below shows the various data types and descriptions.

Serial Data Transfer Order

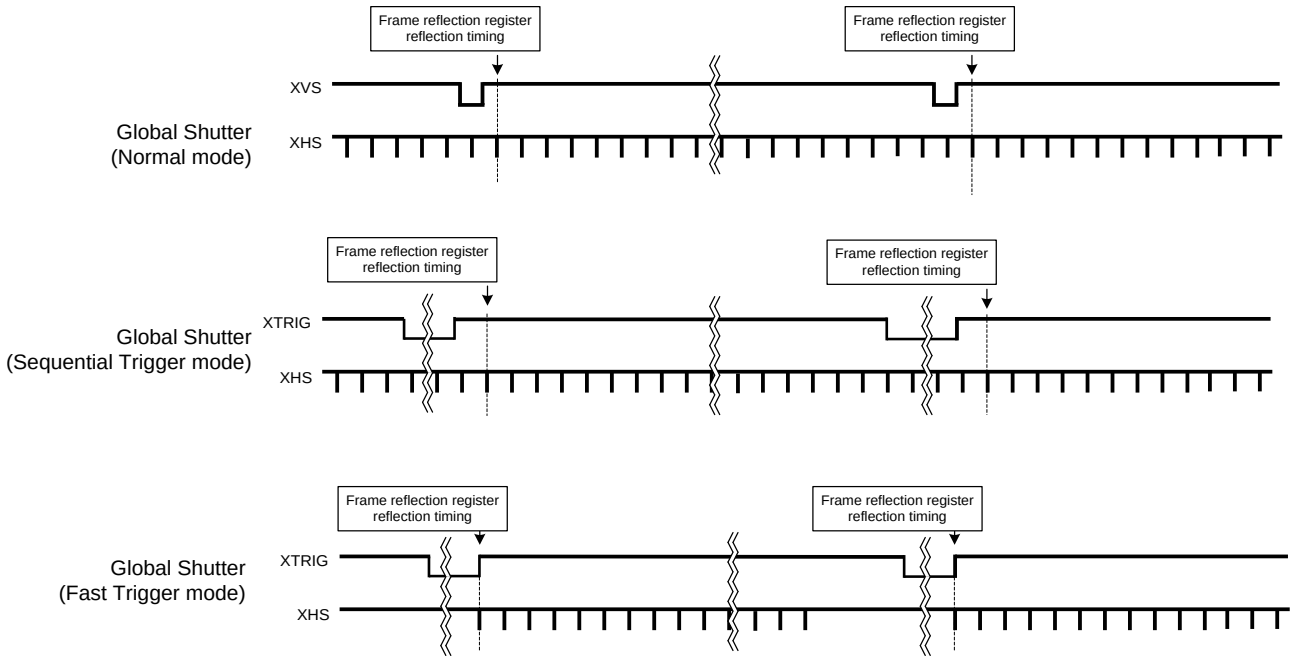
Chip ID	Start address	Data	Data	Data	…
(8 bit)	(8 bit)	(8 bit)	(8 bit)	(8 bit)	(8 bit)

Type and Description

Type	Description
Chip ID	Chip ID: 02 Write: 02h / Read: 82h
	Chip ID: 03 Write: 03h / Read: 83h
	Chip ID: 04 Write: 04h / Read: 84h
	Chip ID: 05 Write: 05h / Read: 85h
	Chip ID: 06 Write: 06h / Read: 86h
	Chip ID: 07 Write: 07h / Read: 87h
	Chip ID: 08 Write: 08h / Read: 88h
	Chip ID: 09 Write: 09h / Read: 89h
	Chip ID: 0A Write: 0Ah / Read: 8Ah
	Chip ID: 0B Write: 0Bh / Read: 8Bh
	Chip ID: 0C Write: 0Ch / Read: 8Ch
	Chip ID: 10 Write: 10h / Read: 90h
	Chip ID: 11 Write: 11h / Read: 91h
	Chip ID: 12 Write: 12h / Read: 92h
	Chip ID: 13 Write: 13h / Read: 93h
	Chip ID: 14 Write: 14h / Read: 94h
	Chip ID: 15 Write: 15h / Read: 95h
	Chip ID: 16 Write: 16h / Read: 96h
	Chip ID: 17 Write: 17h / Read: 97h
	Chip ID: 18 Write: 18h / Read: 98h
	Chip ID: 19 Write: 19h / Read: 99h
Address	Designate the address according to the Register Map. When using a communication method that designates continuous addresses, the address is automatically incremented from the previously transmitted address.
Data	Input the setting values according to the Register Map.

Register Communication Timing (4-wire)

Perform serial communication in sensor standby mode or within streaming. For the registers marked "V" in the item of Reflection timing, they are reflected by frame reflection timing in the figure below. For the registers noted “Immediately” in the item of Reflection timing, the settings are reflected when the communication is performed.



Register Write and Read (4-wire)

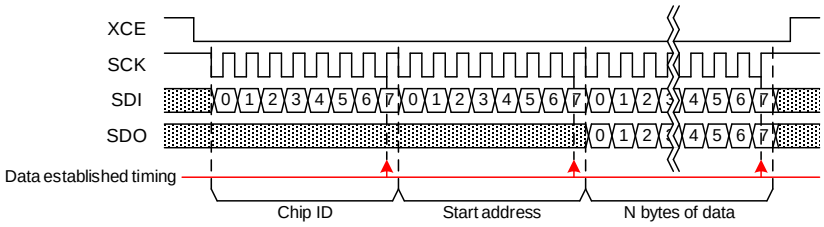
◆Follow the communication procedure below when writing registers.

(1) Set XCE Low to enable the chip's communication function. Serial data input is executed using SCK and SDI.
(2) Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
(3) Input the Chip ID (CID = 02h to 0Ch, 10h to 19h) to the first byte. If the Chip ID differs, subsequent data is ignored.
(4) Input the start address to the second byte. The address is automatically incremented.
(5) Input the data to the third and subsequent bytes. The data in the third byte is written to the register address designated by the second byte, and the register address is automatically incremented thereafter when writing the data for the fourth and subsequent bytes. Normal register data is loaded to the inside of the sensor and established in 8-bit units.
(6) The register values starting from the register address designated by the second byte are output from the SDO pin. The register values before the write operation are output. The actual register values are the input data.
(7) Set XCE High to end communication.

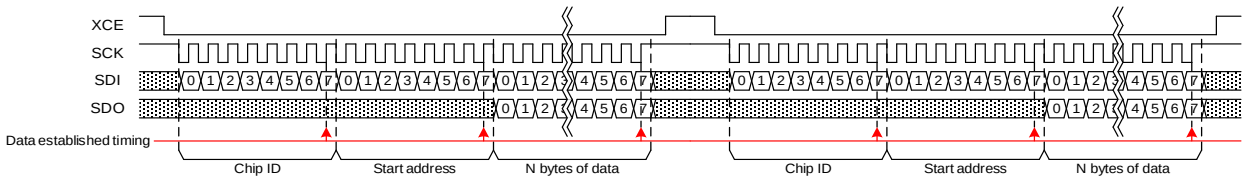
◆Follow the communication procedure below when reading registers.

(1) Set XCE Low to enable the chip's communication function. Serial data input is executed using SCK and SDI.
(2) Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
(3) Input Chip ID (CID = 82h to 8Ch, 90h to 99h) to the first byte. If the Chip ID differs, subsequent data is ignored.
(4) Input the start address to the second byte. The address is automatically incremented.
(5) Input data to the third and subsequent bytes. Input dummy data in order to read the registers. The dummy data is not written to the registers. To read continuous data, input the necessary number of bytes of dummy data.
(6) The register values starting from the register address designated by the second byte are output from the SDO pin. The input data is not written, so the actual register values are output.
(7) Set XCE High to end communication.

Note) When writing data to multiple registers with discontinuous addresses, access to undesired registers can be avoided by repeating the above procedure multiple times.



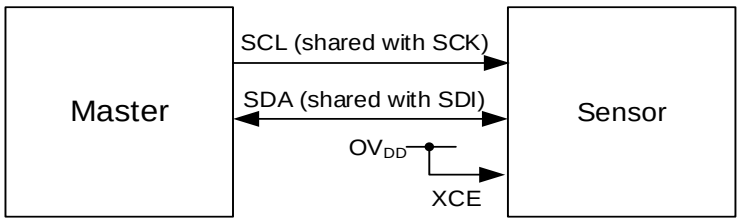
Serial Communication (Continuous Addresses)



Serial Communication (Discontinuous Addresses)

Description of Setting Registers (I^2C)

The serial data input order is MSB-first transfer. The table below shows the various data types and descriptions.



Pin connection of serial communication

The sensor can use two kinds of slave addresses by switching the polarity of SLAMODE Pin for one I^2C bus, and can use a common slave address in both polarities of SLAMODE Pin for one I^2C bus.

SLAVE Address (SLAMODE = 0)

MSB							LSB
0	1	1	0	1	1	0	R / W

SLAVE Address (SLAMODE = 1)

MSB							LSB
0	1	1	0	1	1	1	R / W

SLAVE Address (SLAMODE = 0 / 1)

MSB							LSB
0	0	1	1	0	1	0	R / W

* R/W is data direction bit

R/W

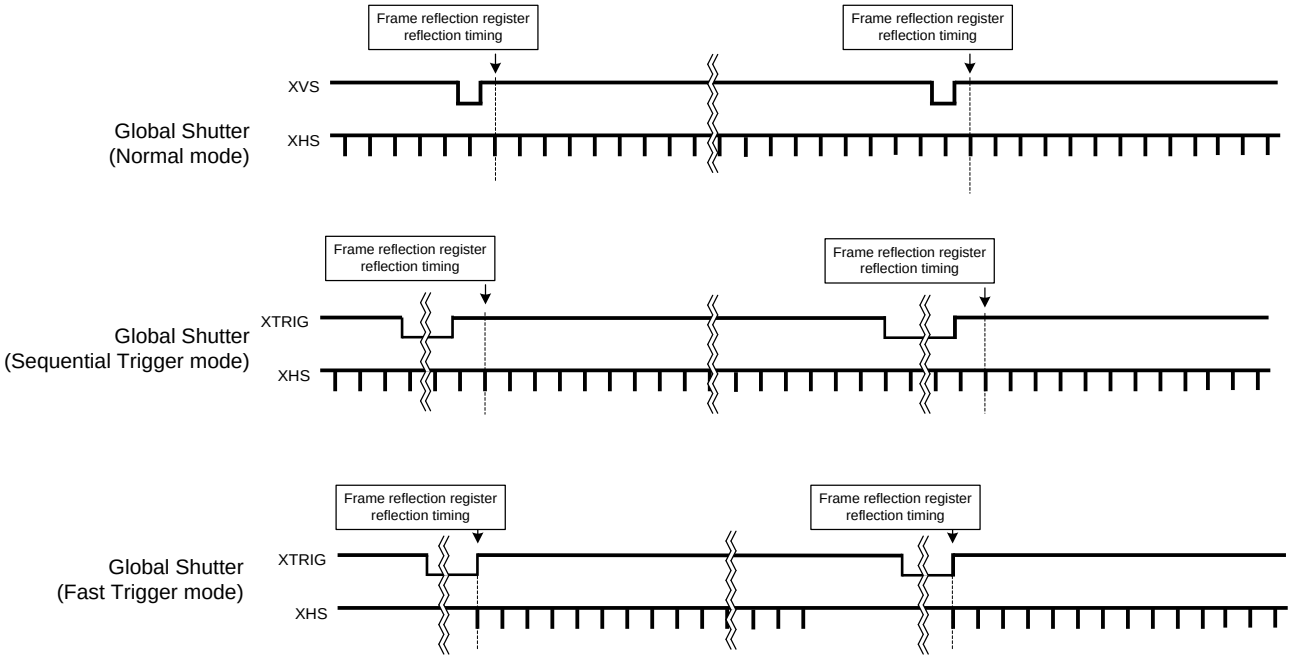
R / W bit	Data direction
0	Write (Master → Sensor)
1	Read (Sensor → Master)

I^2C pin description

Symbol	Description
SCL (common to SCK)	Serial clock input
SDA (common to SDI)	Serial data communication

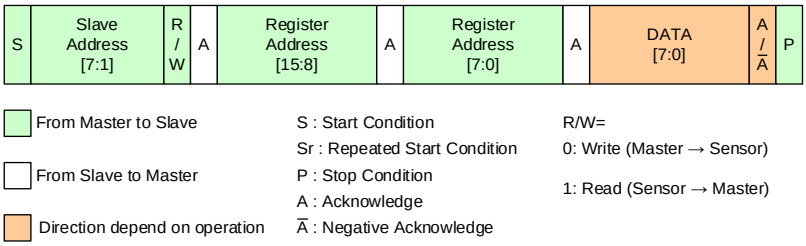
Register Communication Timing (I^2C)

For the registers marked "V" in the item of Reflection timing, they are reflected by frame reflection timing in the figure below. For the registers noted “Immediately” in the item of Reflection timing, the settings are reflected when the communication is performed. Using REGHOLD function is recommended for register setting using I^2C communication. For REGHOLD function, see “Register Transmission Setting” in “Description of Functions”.



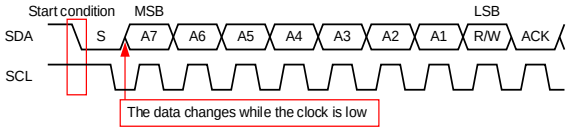
I²C Communication Protocol

I²C serial communication supports a 16-bit register address and 8-bit data message type.

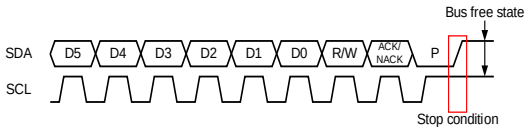


Communication protocol

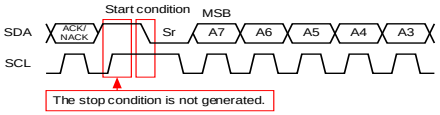
Data is transferred serially, MSB first in 8-bit units. After each data byte is transferred, A (Acknowledge) / Ā (Negative Acknowledge) is transferred. Data (SDA) is transferred at the clock (SCL) cycle. SDA can change only while SCL is Low, so the SDA value must be held while SCL is High. The Start Condition is defined by SDA changing from High to Low while SCL is High. When the Stop Condition is not generated in the previous communication phase and Start Condition for the next communication is generated, that Start Condition is recognized as a Repeated Start Condition.



Start Condition

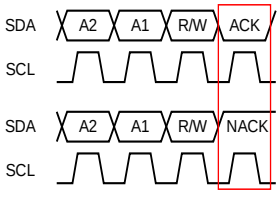


Stop Condition



Repeated Start Condition

After transfer of each data byte, the Master or the sensor transmits an Acknowledge / Negative Acknowledge and release (does not drive) SDA. When Negative Acknowledge is generated, the Master must immediately generate the Stop Condition and end the communication.



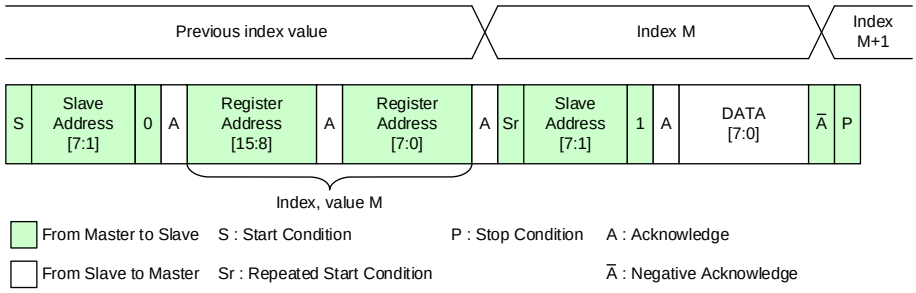
Acknowledge and Negative Acknowledge

I²C Serial Communication Read/Write Operation

This sensor supports the following four read operations and two write operations.

Single Read from Random Location

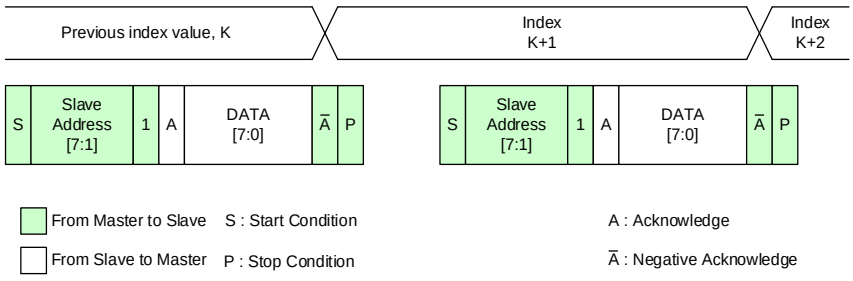
The sensor has an index function that indicates which address it is focusing on. In reading the data at an optional single address, the Master must set the index value to the address to be read. For this purpose it performs dummy write operation up to the register address. The upper level of the figure below shows the sensor internal index value, and the lower level of the figure shows the SDA I/O data flow. The Master sets the sensor index value to M by designating the sensor slave address with a write request, then designating the address (M). Then, the Master generates the Start Condition. The Start Condition is generated without generating the Stop Condition, so it becomes the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge immediately followed by the index address data on SDA. After the Master receives the data, it generates a Negative Acknowledge and the Stop Condition to end the communication.



Single Read from Random Location

Single Read from Current Location

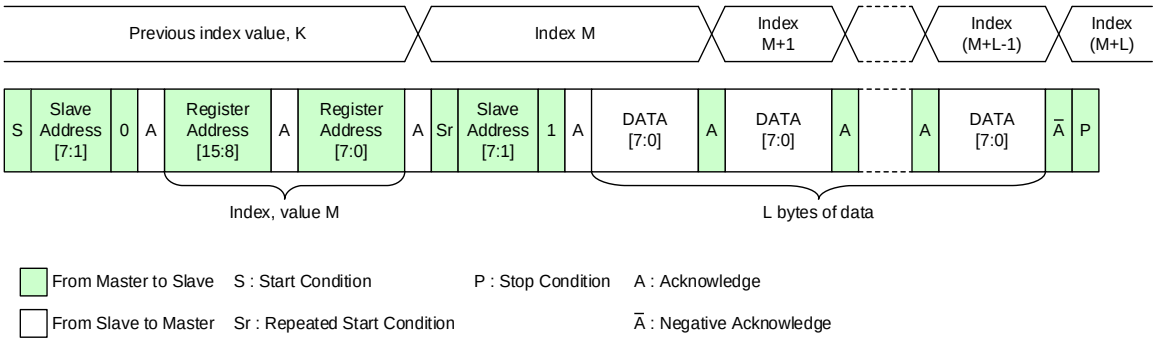
After the slave address is transmitted by a write request, that address is designated by the next communication and the index holds that value. In addition, when data read/write is performed, the index is incremented by the subsequent Acknowledge/Negative Acknowledge timing. When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after Acknowledge. After receiving the data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication, but the index value is incremented, so the data at the next address can be read by sending the slave address with a read request.



Single Read from Current Location

Sequential Read Starting from Random Location

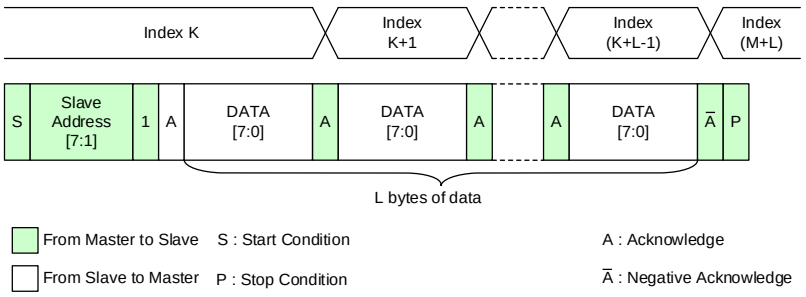
In reading data sequentially, which is starting from an optional address, the Master must set the index value to the start of the addresses to be read. For this purpose, dummy write operation includes the register address setting. The Master sets the sensor index value to M by designating the sensor slave address with a read request, then designating the address (M). Then, the Master generates the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the index address data on SDA. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Random Location

Sequential Read Starting from Current Location

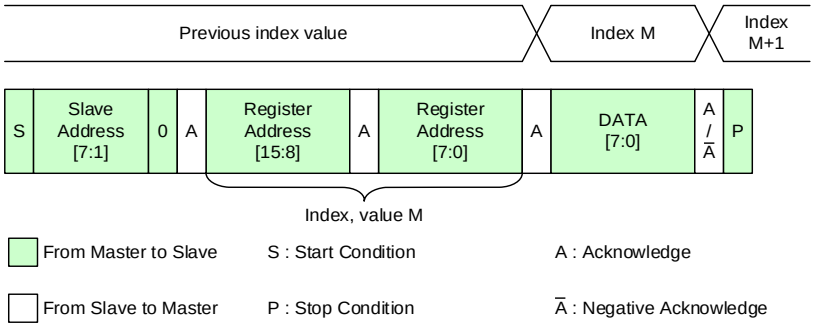
When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after the Acknowledge. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Current Location

Single Write to Random Location

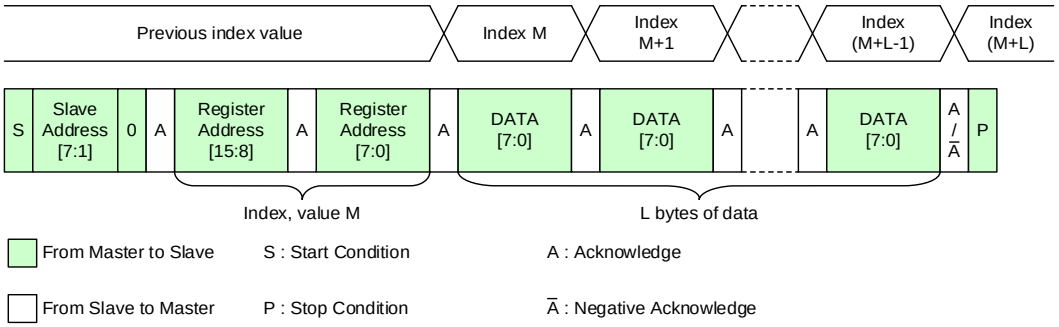
The Master sets the sensor index value to M by designating the sensor slave address with a write request, and designating the address (M). After that the Master can write the value in the designated register by transmitting the data to be written. After writing the necessary data, the Master generates the Stop Condition to end the communication.



Single Write to Random Location

Sequential Write Starting from Random Location

The Master can write a value to register address M by designating the sensor slave address with a write request, designating the address (M), and then transmitting the data to be written. After the sensor receives the write data, it outputs an Acknowledge and at the same time increments the register address, so the Master can write to the next address simply by continuing to transmit data. After the Master writes the necessary number of bytes, it generates the Stop Condition to end the communication.



Sequential Write Starting from Random Location

Register Map (There is a possible to change the registers on this document.)

This sensor has a total of 5376 bytes of registers, composed of registers with address 00h to FFh that correspond to Chip ID = 02h to 0Ch, 10h to 19h. Use the initial values for empty address. Some registers must be change from the initial values, so the sensor control side should be capable of setting 5376 bytes.

There are three different register reflection timings.
About the Reflection timing column of the Register Map, registers noted as "I" are reflected immediately after writing to register, registers noted as "S" are set during standby mode and reflected after standby canceled, registers noted as "V" are reflected at “Fame reflection register reflection timing” on the figure described in the section of “Setting Registers with Serial Communication”.

Do not perform communication to addresses and setting not listed in the Register Map. Doing so may result in operation errors.

Chip ID = 02 (Write: Chip ID = 02h, Read: Chip ID = 82h, I²C: 30**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
00h	3000h	0	STANDBY [0]	Standby mode 0: Normal operation 1: Standby	1	01h	I
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
0Ch	300Ch	0	XMSTA	Setting of master mode operation 0: Master mode operation start 1: Master mode operation stop	1	01h	I
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
34h	3034h	0	REGHOLD	Register hold 0: Invalid 1: Valid	0	00h	I
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
3Ch	303Ch	0	WINMODE	Drive mode setting of V direction 0: All-pixel mode. 1: 1/2 Subsampling mode Others: Setting prohibited	0	00h	S
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4	HMODE	Drive mode setting of H direction 0: All-pixel 1: 1/2 Subsampling mode	0		S
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
D4h	30D4h	0	VMAX [23:0]	LSB	000436h	36h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
D5h	30D5h	0				04h	
		1					
		2					
		3		When sensor master mode vertical span setting. (Number of operation lines count from 1)			
		4					
		5					
		6					
		7					
D6h	30D6h	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
D8h	30D8h	0	HMAX [15:0]	LSB	0235h	35h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7		When sensor master mode horizontal span setting. (Number of operation clocks count from 1)			
D9h	30D9h	0				02h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
DCh	30DCh	0	FREQ [1:0]	Set to data rate. 0: Normal 1: Data rate 1/2 Others: Setting prohibited	0h	00h	S
		1					
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
E2h	30E2h	0	GTWAIT [7:0]	Refer to the register list in each Readout mode	6h	6h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
E3h	30E3h	0	GSDLY [7:0]	Refer to the register list in each Readout mode	4h	4h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					

Chip ID = 03 (Write: Chip ID = 03h, Read: Chip ID = 83h, I²C: 31**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
04h	3104h	0	FID0_ROIH1ON [0]	The horizontal setting of FID0 ROI area (1, y) (y = 1 to 8) 0: Disable 1: Enable	0	00h	V
		1	FID0_ROIV1ON [1]	The vertical setting of FID0 ROI area (x, 1) (x = 1 to 8) 0: Disable 1: Enable	0		V
		2	FID0_ROIH2ON [2]	The horizontal setting of FID0 ROI area (2, y) (y = 1 to 8) 0: Disable 1: Enable	0		V
		3	FID0_ROIV2ON [3]	The vertical setting of FID0 ROI area (x, 2) (x = 1 to 8) 0: Disable 1: Enable	0		V
		4	FID0_ROIH3ON [4]	The horizontal setting of FID0 ROI area (3, y) (y = 1 to 8) 0: Disable 1: Enable	0		V
		5	FID0_ROIV3ON [5]	The vertical setting of FID0 ROI area (x, 3) (x = 1 to 8) 0: Disable 1: Enable	0		V
		6	FID0_ROIH4ON [6]	The horizontal setting of FID0 ROI area (4, y) (y = 1 to 8) 0: Disable 1: Enable	0		V
		7	FID0_ROIV4ON [7]	The vertical setting of FID0 ROI area (x, 4) (x = 1 to 8) 0: Disable 1: Enable	0		V
05h	3105h	0	FID0_ROIH5ON [0]	The horizontal setting of FID0 ROI area (5, y) (y = 1 to 8) 0: Disable 1: Enable	0	00h	V
		1	FID0_ROIV5ON [1]	The vertical setting of FID0 ROI area (x, 5) (x = 1 to 8) 0: Disable 1: Enable	0		V
		2	FID0_ROIH6ON [2]	The horizontal setting of FID0 ROI area (6, y) (y = 1 to 8) 0: Disable 1: Enable	0		V
		3	FID0_ROIV6ON [3]	The vertical setting of FID0 ROI area (x, 6) (x = 1 to 8) 0: Disable 1: Enable	0		V
		4	FID0_ROIH7ON [4]	The horizontal setting of FID0 ROI area (7, y) (y = 1 to 8) 0: Disable 1: Enable	0		V
		5	FID0_ROIV7ON [5]	The vertical setting of FID0 ROI area (x, 7) (x = 1 to 8) 0: Disable 1: Enable	0		V
		6	FID0_ROIH8ON [6]	The horizontal setting of FID0 ROI area (8, y) (y = 1 to 8) 0: Disable 1: Enable	0		V
		7	FID0_ROIV8ON [7]	The vertical setting of FID0 ROI area (x, 8) (x = 1 to 8) 0: Disable 1: Enable	0		V

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
20h	3120h	[7:0]	FID0_ROIPH1 [12:0]	Designation of horizontal cropping position for FID0 on area (1, y) (y = 1 to 8) *Set the value of multiple of 8	0000h	00h	V
21h	3121h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
22h	3122h	[7:0]	FID0_ROIPV1 [11:0]	Designation of vertical cropping position for FID0 on area (x, 1) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	V
23h	3123h	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
24h	3124h	[7:0]	FID0_ROIWH1 [12:0]	Designation of horizontal cropping size for FID0 on area (1, y) (y = 1 to 8) *Set the value of multiple of 4	0000h	00h	V
25h	3125h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
26h	3126h	[7:0]	FID0_ROIWV1 [11:0]	Designation of vertical cropping size for FID0 on area (x, 1) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	V
27h	3127h	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
28h	3128h	[7:0]	FID0_ROIPH2 [12:0]	Designation of horizontal cropping position for FID0 on area (2, y) (y = 1 to 8) *Set the value of multiple of 8	0000h	00h	V
29h	3129h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
2Ah	312Ah	[7:0]	FID0_ROIPV2 [11:0]	Designation of vertical cropping position for FID0 on area (x, 2) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	V
2Bh	312Bh	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
2Ch	312Ch	[7:0]	FID0_ROIWH2 [12:0]	Designation of horizontal cropping size for FID0 on area (2, y) (y = 1 to 8) *Set the value of multiple of 4	0000h	00h	V
2Dh	312Dh	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
2Eh	312Eh	[7:0]	FID0_ROIWV2 [11:0]	Designation of vertical cropping size for FID0 on area (x, 2) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	V
2Fh	312Fh	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
30h	3130h	[7:0]	FID0_ROIPH3 [12:0]	Designation of horizontal cropping position for FID0 on area (3, y) (y = 1 to 8) *Set the value of multiple of 8	0000h	00h	V
31h	3131h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
32h	3132h	[7:0]	FID0_ROIPV3 [11:0]	Designation of vertical cropping position for FID0 on area (x, 3) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	V
33h	3133h	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
34h	3134h	[7:0]	FID0_ROIWH3 [12:0]	Designation of horizontal cropping size for FID0 on area (3, y) (y = 1 to 8) *Set the value of multiple of 4	0000h	00h	V
35h	3135h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
36h	3136h	[7:0]	FID0_ROIWV3 [11:0]	Designation of vertical cropping size for FID0 on area (x, 3) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	V
37h	3137h	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
38h	3138h	[7:0]	FID0_ROIPH4 [12:0]	Designation of horizontal cropping position for FID0 on area (4, y) (y = 1 to 8) *Set the value of multiple of 8	0000h	00h	V
39h	3139h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
3Ah	313Ah	[7:0]	FID0_ROIPV4 [11:0]	Designation of vertical cropping position for FID0 on area (x, 4) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	V
3Bh	313Bh	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
3Ch	313Ch	[7:0]	FID0_ROIWH4 [12:0]	Designation of horizontal cropping size for FID0 on area (4, y) (y = 1 to 8) *Set the value of multiple of 4	0000h	00h	V
3Dh	313Dh	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
3Eh	313Eh	[7:0]	FID0_ROIWV4 [11:0]	Designation of vertical cropping size for FID0 on area (x, 4) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	V
3Fh	313Fh	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
40h	3140h	[7:0]	FID0_ROIPH5 [12:0]	Designation of horizontal cropping position for FID0 on area (5, y) (y = 1 to 8) *Set the value of multiple of 8	0000h	00h	V
41h	3141h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
42h	3142h	[7:0]	FID0_ROIPV5 [11:0]	Designation of vertical cropping position for FID0 on area (x, 5) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	V
43h	3143h	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
44h	3144h	[7:0]	FID0_ROIWH5 [12:0]	Designation of horizontal cropping size for FID0 on area (5, y) (y = 1 to 8) *Set the value of multiple of 4	0000h	00h	V
45h	3145h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
46h	3146h	[7:0]	FID0_ROIWV5 [11:0]	Designation of vertical cropping size for FID0 on area (x, 5) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	V
47h	3147h	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
48h	3148h	[7:0]	FID0_ROIPH6 [12:0]	Designation of horizontal cropping position for FID0 on area (6, y) (y = 1 to 8) *Set the value of multiple of 8	0000h	00h	V
49h	3149h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
4Ah	314Ah	[7:0]	FID0_ROIPV6 [11:0]	Designation of vertical cropping position for FID0 on area (x, 6) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	V
4Bh	314Bh	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
4Ch	314Ch	[7:0]	FID0_ROIWH6 [12:0]	Designation of horizontal cropping size for FID0 on area (6, y) (y = 1 to 8) *Set the value of multiple of 4	0000h	00h	V
4Dh	314Dh	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
4Eh	314Eh	[7:0]	FID0_ROIWV6 [11:0]	Designation of vertical cropping size for FID0 on area (x, 6) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	V
4Fh	314Fh	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
50h	3150h	[7:0]	FID0_ROIPH7 [12:0]	Designation of horizontal cropping position for FID0 on area (7, y) (y = 1 to 8) *Set the value of multiple of 8	0000h	00h	V
51h	3151h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
52h	3152h	[7:0]	FID0_ROIPV7 [11:0]	Designation of vertical cropping position for FID0 on area (x, 7) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	V
53h	3153h	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
54h	3154h	[7:0]	FID0_ROIWH7 [12:0]	Designation of horizontal cropping size for FID0 on area (7, y) (y = 1 to 8) *Set the value of multiple of 4	0000h	00h	V
55h	3155h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
56h	3156h	[7:0]	FID0_ROIWV7 [11:0]	Designation of vertical cropping size for FID0 on area (x, 7) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	V
57h	3157h	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
58h	3158h	[7:0]	FID0_ROIPH8 [12:0]	Designation of horizontal cropping position for FID0 on area (8, y) (y = 1 to 8) *Set the value of multiple of 8	0000h	00h	V
59h	3159h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
5Ah	315Ah	[7:0]	FID0_ROIPV8 [11:0]	Designation of vertical cropping position for FID0 on area (x, 8) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	V
5Bh	315Bh	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
5Ch	315Ch	[7:0]	FID0_ROIWH8 [12:0]	Designation of horizontal cropping size for FID0 on area (8, y) (y = 1 to 8) *Set the value of multiple of 4	0000h	00h	V
5Dh	315Dh	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
5Eh	315Fh	[7:0]	FID0_ROIWV8 [11:0]	Designation of vertical cropping size for FID0 on area (x, 8) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	V
5Fh	315Fh	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—

Chip ID = 04 (Write: Chip ID = 04h, Read: Chip ID = 84h, I²C: 32**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
00h	3200h	0		Fixed to 1	1	05h	—
		1		Fixed to 0	0		
		2		Fixed to 1	1		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5	ADBIT [6:5]	AD conversion bits setting 0h: 10 bit 1h: 12 bit 2h: 8 bit 3h: Setting prohibited	0h		S
		6					
		7		Fixed to 0	0		—
04h	3204h	0	VREVERSE	Vertical (V) direction readout inversion control 0: Normal 1: Inverted	0	00h	V
		1	HREVERSE	Horizontal (H) direction readout inversion control 0: Normal 1: Inverted	0		V
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
20h	3220h	0	INCKSEL0 [7:0]	Set according to INCK frequency and drive mode.	52h	52h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
21h	3221h	0	INCKSEL1 [7:0]	Set according to INCK frequency and drive mode.	20h	20h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
24h	3224h	0	INCKSEL2 [7:0]	Set according to INCK frequency and drive mode.	52h	52h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
25h	3225h	0	INCKSEL3 [7:0]	Set according to INCK frequency and drive mode.	20h	20h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
26h	3226h	0	FREQ_SYNC [7:0]	Refer to the register list in each Readout mode	93h	93h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
30h	3230h	0		Fixed to 1	1	11h	—
		1	FASTTRIG	Selection of trigger mode 0: Except for Fast trigger mode 1: Fast trigger mode	0		S
		2	LLBLANK	Refer to the register list in each readout mode	04h		S
		3					
		4					
		5					
		6					
		7					
31h	3231h	0				00h	
		1					
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
32h	3232h	0	VINT_EN	Setting of Interrupt mode in Trigger Mode 0: V interrupt is disabled 1: V interrupt is enabled	1	01h	S
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
40h	3240h	0	SHS [23:0]	LSB	000018h	18h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
41h	3241h	0				00h	
		1					
		2					
		3		Storage time adjustment Designated in line unit			
		4					
		5					
		6					
		7					
42h	3242h	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			

Chip ID = 05 (Write: Chip ID = 05h, Read: Chip ID = 85h, I²C: 33**h)

Please refer to the other register map file for the register that has not been described.

Chip ID = 06 (Write: Chip ID = 06h, Read: Chip ID = 86h, I²C: 34**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
00h	3400h	0	TRIGEN	Global shutter mode setting 0: Normal mode 1: Trigger mode	0	00h	I[*1]
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
30h	3430h	0	ODBIT [1:0]	Number of output bit setting 0h: 10 bit 1h: 12 bit 2h: 8 bit 3h: Setting prohibited	0h	00h	S
		1					
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
35h	3435h	0	TOUT1SEL [1:0]	TOUT1 pin setting 0h: Low fixed 3h: Pulse output	0h	00h	S
		1					
		2	TOUT2SEL [3:2]	TOUT2 pin setting 0h: Low fixed 3h: Pulse output	0h		S
		3					
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
3Ah	343Ah	0	TRIG_TOUT1_SEL [3:0]	TOUT1 output setting 0h: Low fixed 1h: Pulse1 output	0h	00h	S
		1					
		2					
		3					
		4	TRIG_TOUT2_SEL [7:4]	TOUT2 output setting 0h: Low fixed 2h: Pulse2 output	0h		S
		5					
		6					
		7					
3Ch	343Ch	0		Fixed to 0	0	C0h	—
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4	SYNCSEL [5:4]	XHS, XVS pin setting 0h: Normal Output 3h: Hi-Z	0h		S
		5					
		6		Fixed to 1	1		—
		7		Fixed to 1	1		—

[*1] Refer to “Mode Transitions of Global Shutter Operation”

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
44h	3444h	0	STBSLVS [3:0]	Channel standby control of SLVS 2h: activate 4 ch 3h: activate 2 ch Others: Setting prohibited	2h	02h	S
		1					
		2					
		3					
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
45h	3445h	0	OPORTSEL [3:0]	SLVS channel selection 3h: 4 ch 4h: 2 ch Others: Setting prohibited	3h	03h	S
		1					
		2					
		3					
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
78h	3478h	0	PULSE1_EN_NOR [0]	Pulse1 output in normal mode 0: Disable 1: Enable	0	00h	S
		1	PULSE1_EN_TRIG [1]	Pulse1 output in trigger mode 0: Disable 1: Enable	0		S
		2	PULSE1_POL [2]	Pulse1 polarity selection 0: High active 1: Low active	0		S
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
79h	3479h	0	PULSE1_UP [23:0]	LSB	000000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
7Ah	347Ah	0		Pulse1 active period start timing setting Designated in line units from reference point (For details, see the “Pulse Output Function”)		00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7					
7Bh	347Bh	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
7Ch	347Ch	0	PULSE1_DN [23:0]	LSB	000000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
7Dh	347Dh	0				00h	
		1					
		2					
		3		Pulse1 active period end timing setting Designated in line units from readout start (For details, see the “Pulse Output Function”)			
		4					
		5					
		6					
		7					
7Eh	347Eh	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
80h	3480h	0	PULSE2_EN_NOR [0]	Pulse2 output in normal mode 0: Disable 1: Enable	0	00h	S
		1	PULSE2_EN_TRIG [1]	Pulse2 output in trigger mode 0: Disable 1: Enable	0		S
		2	PULSE2_POL [2]	Pulse2 polarity selection 0: High active 1: Low active	0		S
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 1	0		S
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
81h	3481h	0	PULSE2_UP [23:0]	LSB	000000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
82h	3482h	0				00h	
		1					
		2					
		3		Pulse2 active period start timing setting Designated in line units from reference point (For details, see the “Pulse Output Function”)			
		4					
		5					
		6					
		7					
83h	3483h	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
84h	3484h	0	PULSE2_DN [23:0]	LSB	000000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
85h	3485h	0				00h	
		1					
		2					
		3		Pulse2 active period end timing setting Designated in line units from reference point (For details, see the “Pulse Output Function”)			
		4					
		5					
		6					
		7					
86h	3486h	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
90h	3490h	0	TMP_OUT[11:0]	Output of the digital thermometer. Read only.	00h	00h	—
		1					
		2					
		3					
		4					
		5					
		6					
		7					
91h	3491h	0				00h	
		1					
		2					
		3					
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Chip ID = 07 (Write: Chip ID = 07h, Read: Chip ID = 87h, I²C: 35**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
02h	3502h	0	GAINUPDSL	Setting of Gain Reflection Timing at Normal mode. 0: Gain reflect at the frame 1: Gain reflect at the next frame (Same timing as SHS reflecting output.) Set 0 at Triger modes.	0	00h	S
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
14h	3514h	0	GAIN [8:0]	LSB Gain setting 0 dB (000d) to 42 dB (420d) 0.1 dB Step (Refer to Address 02h about detail of Reflection Timing.)	000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
15h	3515h	0		MSB		00h	
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
88h	3588h	0	TMDLATCH	Thermometer output is updated when this register is set from 0h to 1h.	0	30h	I
		1		Fixed to 1	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 1	1		—
		5		Fixed to 1	1		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
C0h	35C0h	0	BLKLEVEL [11:0]	LSB Black level offset value setting Recommended value. 00Fh: 8 bit 03Ch: 10 bit 0F0h: 12 bit	03Ch	3Ch	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
C1h	35C1h	0				00h	
		1					
		2					
		3		MSB			
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Chip ID = 08 (Write: Chip ID = 08h, Read: Chip ID = 88h, I²C: 36h)**

Please refer to the other register map file for the register that has not been described.

Chip ID = 09 (Write: Chip ID = 09h, Read: Chip ID = 89h, I²C: 37h)**

Please refer to the other register map file for the register that has not been described.

Chip ID = 0A (Write: Chip ID = 0Ah, Read: Chip ID = 8Ah, I²C: 38h)**

Please refer to the other register map file for the register that has not been described.

Chip ID = 0B (Write: Chip ID = 0Bh, Read: Chip ID = 8Bh, I²C: 39h)**

Please refer to the other register map file for the register that has not been described.

Chip ID = 0C (Write: Chip ID = 0Ch, Read: Chip ID = 8Ch, I²C: 3Ah)**

Please refer to the other register map file for the register that has not been described.

Chip ID = 10 (Write: Chip ID = 10h, Read: Chip ID = 90h, I²C: 3Eh)**

Please refer to the other register map file for the register that has not been described.

Chip ID = 11 (Write: Chip ID = 11h, Read: Chip ID = 91h, I²C: 3Fh)**

Please refer to the other register map file for the register that has not been described.

Chip ID = 12 (Write: Chip ID = 12h, Read: Chip ID = 92h, I²C: 40h)**

Please refer to the other register map file for the register that has not been described.

Chip ID = 13 (Write: Chip ID = 13h, Read: Chip ID = 93h, I²C: 41h)**

Please refer to the other register map file for the register that has not been described.

Chip ID = 14 (Write: Chip ID = 14h, Read: Chip ID = 94h, I²C: 42h)**

Please refer to the other register map file for the register that has not been described.

Chip ID = 15 (Write: Chip ID = 15h, Read: Chip ID = 95h, I²C: 43h)**

Please refer to the other register map file for the register that has not been described.

Chip ID = 16 (Write: Chip ID = 16h, Read: Chip ID = 96h, I²C: 44h)**

Please refer to the other register map file for the register that has not been described.

Chip ID = 17 (Write: Chip ID = 17h, Read: Chip ID = 97h, I²C: 45h)**

Please refer to the other register map file for the register that has not been described.

Chip ID = 18 (Write: Chip ID = 18h, Read: Chip ID = 98h, I²C: 46h)**

Please refer to the other register map file for the register that has not been described.

Chip ID = 19 (Write: Chip ID = 19h, Read: Chip ID = 99h, I²C: 47h)**

Please refer to the other register map file for the register that has not been described.

Readout Drive Modes

The table below lists the operating modes available with this sensor. (Each value is the Max. frame rate of each number of ch.)

FREQ (CID = 02h, Address = DCh, [1:0]) = 0h

Drive mode	Frame rate [frame/s]	Data rate [Gbps]	SLVS ch[*1]	A/D conversion	Number of recording pixels		Total number of pixels (Average)[*3]		Number of INCK in 1H		
					H	V	H	V	INCK: 37.125 MHz	INCK: 74.25 MHz	INCK: 54 MHz
All pixel	134.73	2.376	4	8	1280	1024	2064	1068	258.0	516.0	375.3
	92.69	1.188	2				1500		375.0	750.0	545.5
	125.27	2.376	4	10			1776		277.5	555.0	403.7
	74.76	1.188	2				1488		465.0	930.0	676.4
	71.53	2.376	4	12			2592		486.0	972.0	706.9
	62.97	1.188	2				1472		552.0	1104.0	802.9
All pixel (Vertical / Horizontal 1/2 subsampling)	260.68	2.376	4	8	640	512	2064	552	258.0	516.0	375.3
	260.68	1.188	2				1032		258.0	516.0	375.3
	242.36	2.376	4	10			1776		277.5	555.0	403.7
	242.36	1.188	2				888		277.5	555.0	403.7
	138.39	2.376	4	12			2592		486.0	972.0	706.9
	138.39	1.188	2				1296		486.0	972.0	706.9
ROI	[*2]	2.376	4	8	[*1]	[*1]	2064	[*2]	258.0	516.0	375.3
	[*2]	1.188	2				1500		375.0	750.0	545.5
	[*2]	2.376	4	10			1776		277.5	555.0	403.7
	[*2]	1.188	2				1488		465.0	930.0	676.4
	[*2]	2.376	4	12			2592		486.0	972.0	707.0
	[*2]	1.188	2				1472		552.0	1104.0	803.0

FREQ (CID = 02h, Address = DCh, [1:0]) = 1h

Drive mode	Frame rate [frame/s]	Data rate [Gbps]	SLVS ch[*1]	A/D conversion	Number of recording pixels		Total number of pixels (Average)[*3]		Number of INCK in 1H		
					H	V	H	V	INCK: 37.125 MHz	INCK: 74.25 MHz	INCK: 54 MHz
All pixel	91.71	1.188	4	8	1280	1024	1516	1068	379.0	758.0	551.3
	47.81	0.594	2				1454		727.0	1454.0	1057.5
	73.96	1.188	4	10			1504		470.0	940.0	683.6
	38.41	0.594	2				1448		905.0	1810.0	1316.4
	62.29	1.188	4	12			1488		558.0	1116.0	811.7
	32.18	0.594	2				1440		1080.0	2160.0	1571.0
All pixel (Vertical / Horizontal 1/2 subsampling)	260.67	1.188	4	8	640	512	1032	552	258.0	516.0	375.3
	177.45	0.594	2				758		379.0	758.0	551.3
	242.36	1.188	4	10			888		277.5	555.0	403.7
	143.09	0.594	2				752		470.0	940.0	683.6
	138.38	1.188	4	12			1296		486.0	972.0	707.0
	120.52	0.594	2				744		558.0	1116.0	811.7
ROI	[*2]	1.188	4	8	[*1]	[*1]	1516	[*2]	379.0	758.0	551.3
	[*2]	0.594	2				1454		727.0	1454.0	1057.5
	[*2]	1.188	4	10			1504		470.0	940.0	683.6
	[*2]	0.594	2				1448		905.0	1810.0	1316.4
	[*2]	1.188	4	12			1488		558.0	1116.0	811.7
	[*2]	0.594	2				1440		1080.0	2160.0	1571.0

[*1] Designated cropping area (ROI).

[*2] See the section of “ROI mode”.

[*3] It is possible that the blank pixel number of 1H changes by 1 pixel.
For the setting value to register HMAX / VMAX, see the section of each drive mode settings.

Restriction on Image Data Output

If the shutter releases on outputting the image data in this product, blank code is inserted in the image data because of shutter stabilization wait time.
The insertion timing of shutter stabilization wait time changes depending on the shutter release timing.
During the shutter stabilization wait time, the sync codes is not output. Refer to the sync codes from the sensor and perform synchronization.

Please refer to the Application Note for the effect of the shutter release on the image qualities during the image data outputs.

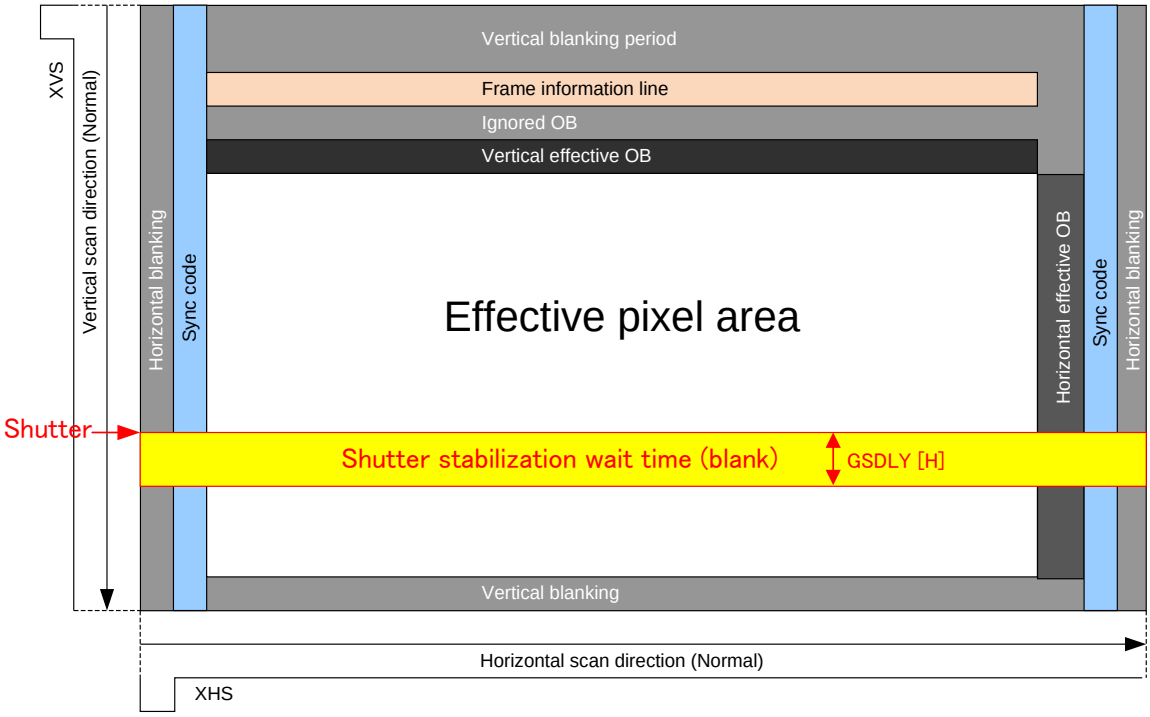


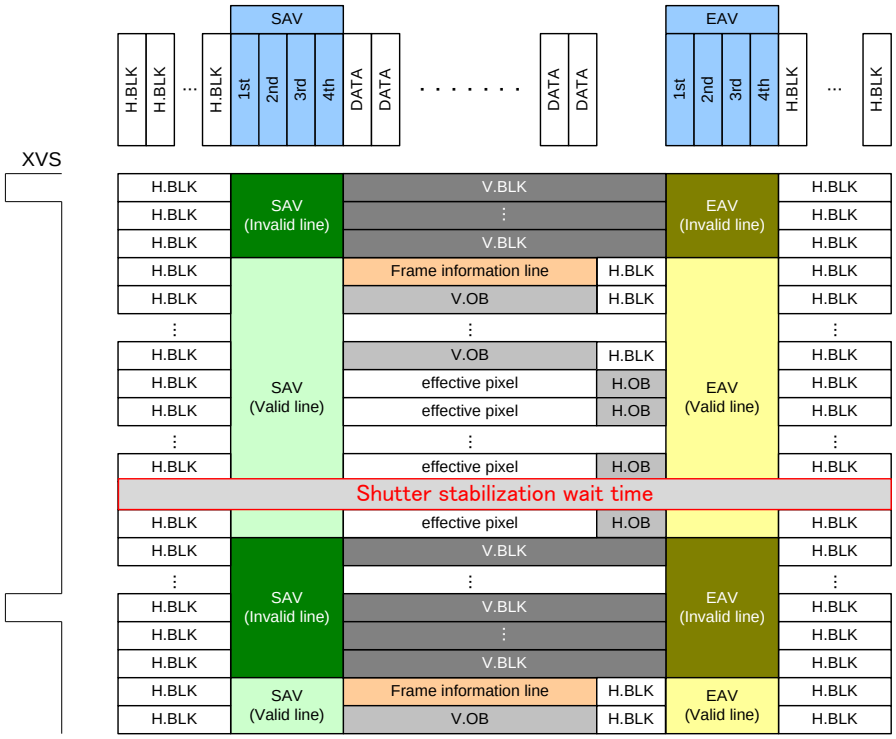
Image Drawing of Sutter stabilization wait time inserted

Refer to the register list of each scan mode for GSDLY.

Image Data Output Format

Sync code

The sync code is added immediately before and after “dummy signal + OB signal + effective pixel data” and then output. The sync code is output in order of 1st, 2nd, 3rd and 4th. The fixed value is output for 1st to 3rd. (BLK: Blanking period)



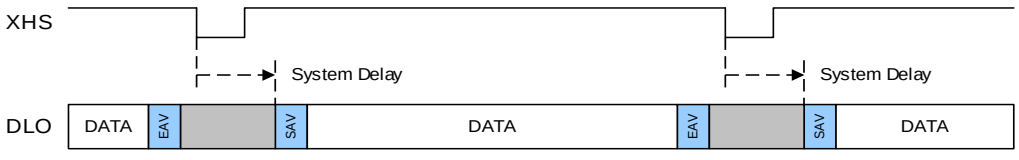
Sync Code Output Timing

List of Sync Code

Sync code	1st code			2nd code			3rd code			4th code		
	8 bit	10 bit	12 bit	8 bit	10 bit	12 bit	8 bit	10 bit	12 bit	8 bit	10 bit	12 bit
SAV (Valid line)	FFh	3FFh	FFFh	00h	000h	000h	00h	000h	000h	80h	200h	800h
EAV (Valid line)	FFh	3FFh	FFFh	00h	000h	000h	00h	000h	000h	9Dh	274h	9D0h
SAV (Invalid line)	FFh	3FFh	FFFh	00h	000h	000h	00h	000h	000h	ABh	2ACh	AB0h
EAV (Invalid line)	FFh	3FFh	FFFh	00h	000h	000h	00h	000h	000h	B6h	2D8h	B60h

Sync Code Output Timing

The sensor output signal passes through the internal circuits and is output with a latency time (system delay) relative to the horizontal sync signal. This system delay value is undefined for each line, so refer to the sync codes output from the sensor and perform synchronization.

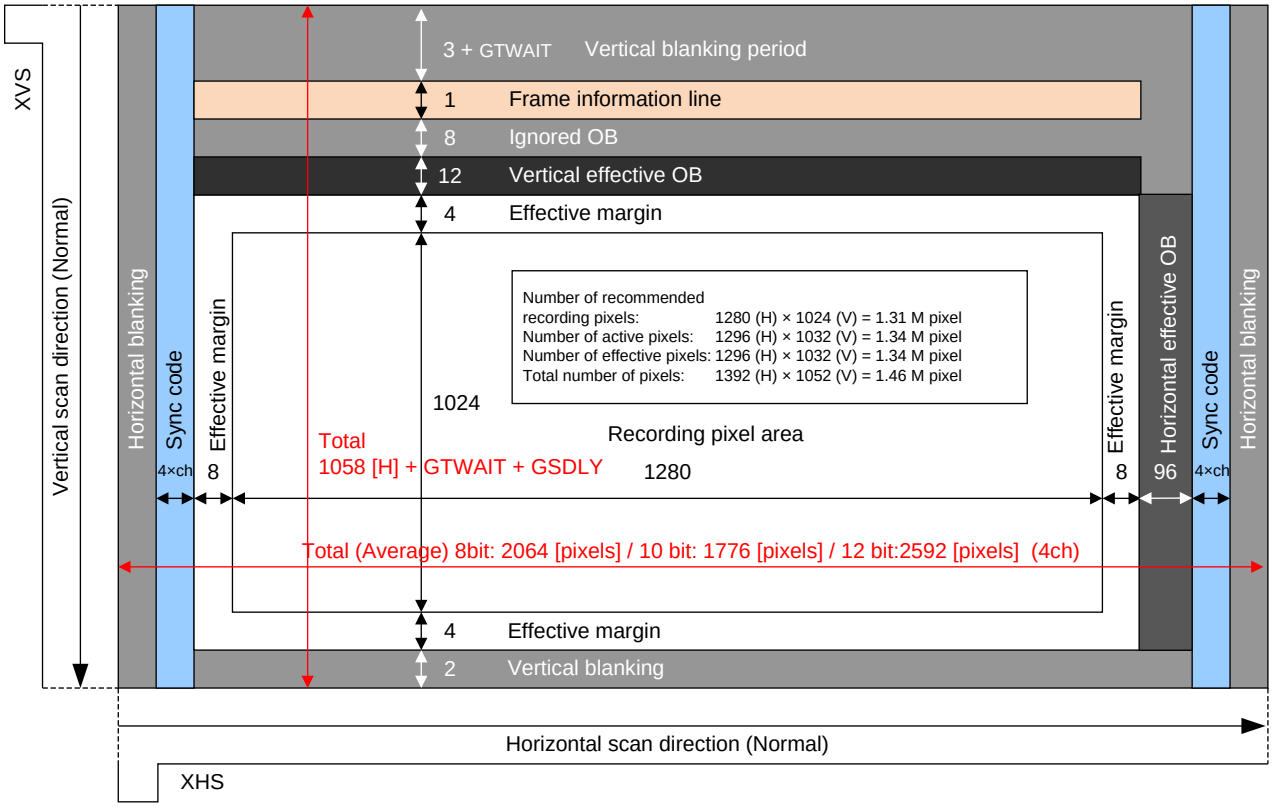


All - pixel scan

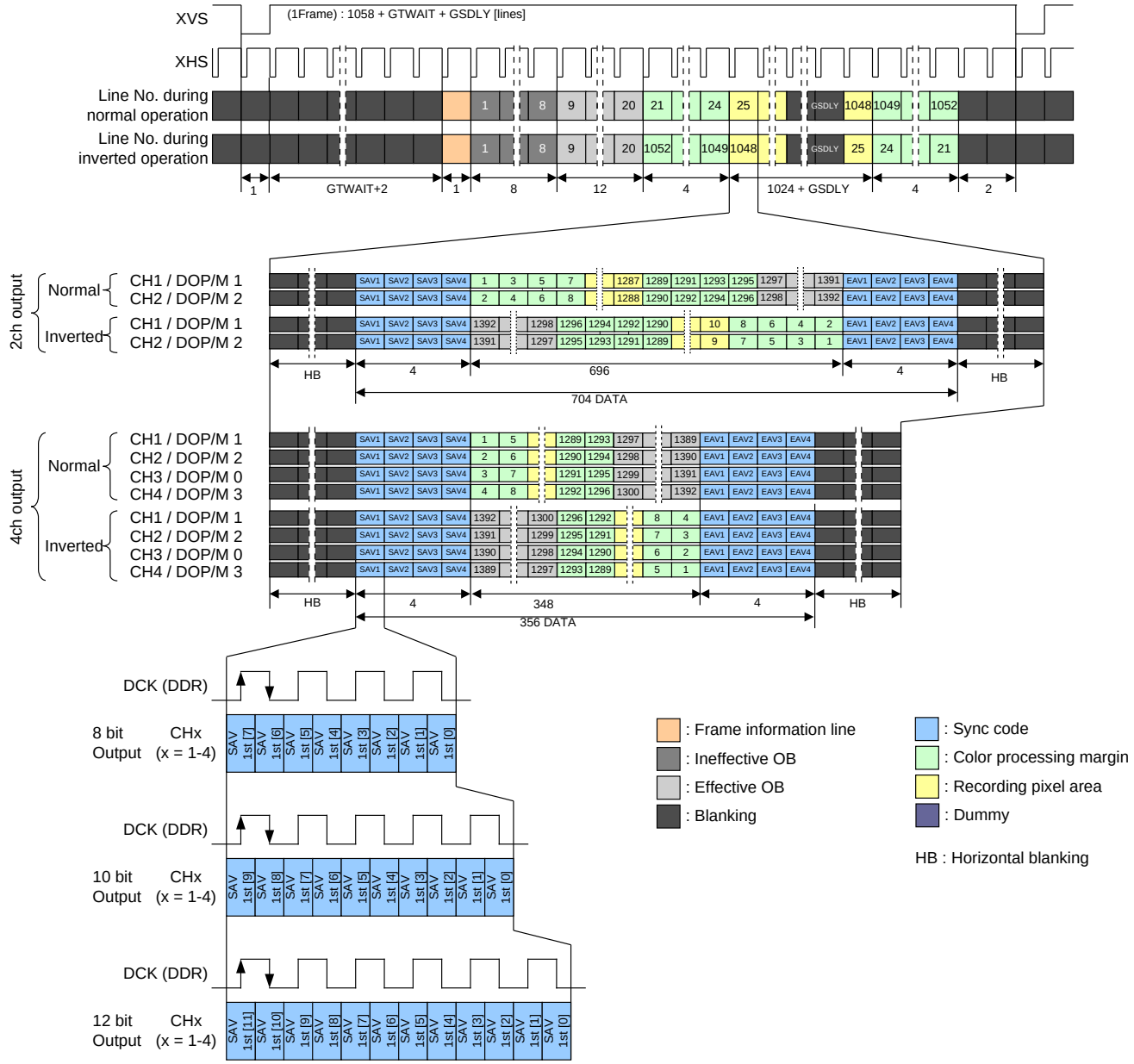
Register List of All - pixel scan mode

Please refer to the other register map file for the register that has not been described.

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 8 bit		AD = 10 bit		AD = 12 bit		
				SLVS 4 ch	SLVS 2 ch	SLVS 4 ch	SLVS 2 ch	SLVS 4 ch	SLVS 2 ch	
				134.73 [frame/s]	92.70 [frame/s]	125.27 [frame/s]	74.76 [frame/s]	71.53 [frame/s]	62.97 [frame/s]	FREQ = 0h
				91.72 [frame/s]	47.81 [frame/s]	73.96 [frame/s]	38.41 [frame/s]	62.30 [frame/s]	32.19 [frame/s]	FREQ = 1h
Chip ID = 02h										
3Ch	[0]	WINMODE	0	0						All-pixel mode
	[4]	HMODE	0	0						All-pixel
D4h	[7:0]	VMAX	436h	42Ch						
D5h	[7:0]									
D6h	[7:0]									
D8h	[7:0]	HMAX	235h	204h	2EEh	22Bh	3A2h	3CCh	450h	FREQ = 0h
D9h	[7:0]			2F6h	5AEh	3ABh	712h	45Ch	870h	FREQ = 1h
DCh	[1:0]	FREQ	0h	0h / 1h						
E2h	[7:0]	GTWAIT	6h	6h						
E3h	[7:0]	GSDLY	4h	4h						
Chip ID = 04h										
00h	[6:5]	ADBIT	0h	2h		0h		1h		0: 10 bit 1: 12 bit 2: 8 bit
20h	[7:0]	INCKSEL0	52h	INCK = 37.125 MHz / 54 MHz: 50h INCK = 74.25 MHz: 52h						
21h	[7:0]	INCKSEL1	20h	INCK = 37.125 MHz / 74.25 MHz: 20h INCK = 54 MHz: 16h						
24h	[7:0]	INCKSEL2	52h	INCK = 37.125 MHz / 54 MHz: 50h INCK = 74.25 MHz: 52h						
25h	[7:0]	INCKSEL3	20h	INCK = 37.125 MHz / 74.25 MHz: 20h INCK = 54 MHz: 16h						
26h	[7:0]	FREQ_SYNC	93h	FREQ = 0: 93h FREQ = 1: A3h						
30h	[7:2]	LLBLANK	04h	04h						
31h	[1:0]									
Chip ID = 06h										
30h	[1:0]	ODBIT	0h	2h		0h		1h		0: 10 bit 1: 12 bit 2: 8 bit
44h	[3:0]	STBSLVS	1h	2h	N/A	2h	N/A	2h	N/A	4 ch SLVS
				N/A	3h	N/A	3h	N/A	3h	2 ch SLVS
45h	[3:0]	OPORTSEL	1h	3h	N/A	3h	N/A	3h	N/A	4 ch SLVS
				N/A	4h	N/A	4h	N/A	4h	2 ch SLVS
Chip ID = 07h										
C0h	[7:0]	BLKLEVEL	03Ch	00Fh		03Ch		0F0h		Recommended value
C1h	[3:0]									



Pixel Array Image Drawing in All - pixel scan Mode



Drive Timing Chart for Serial Output in All - pixel Scan Mode

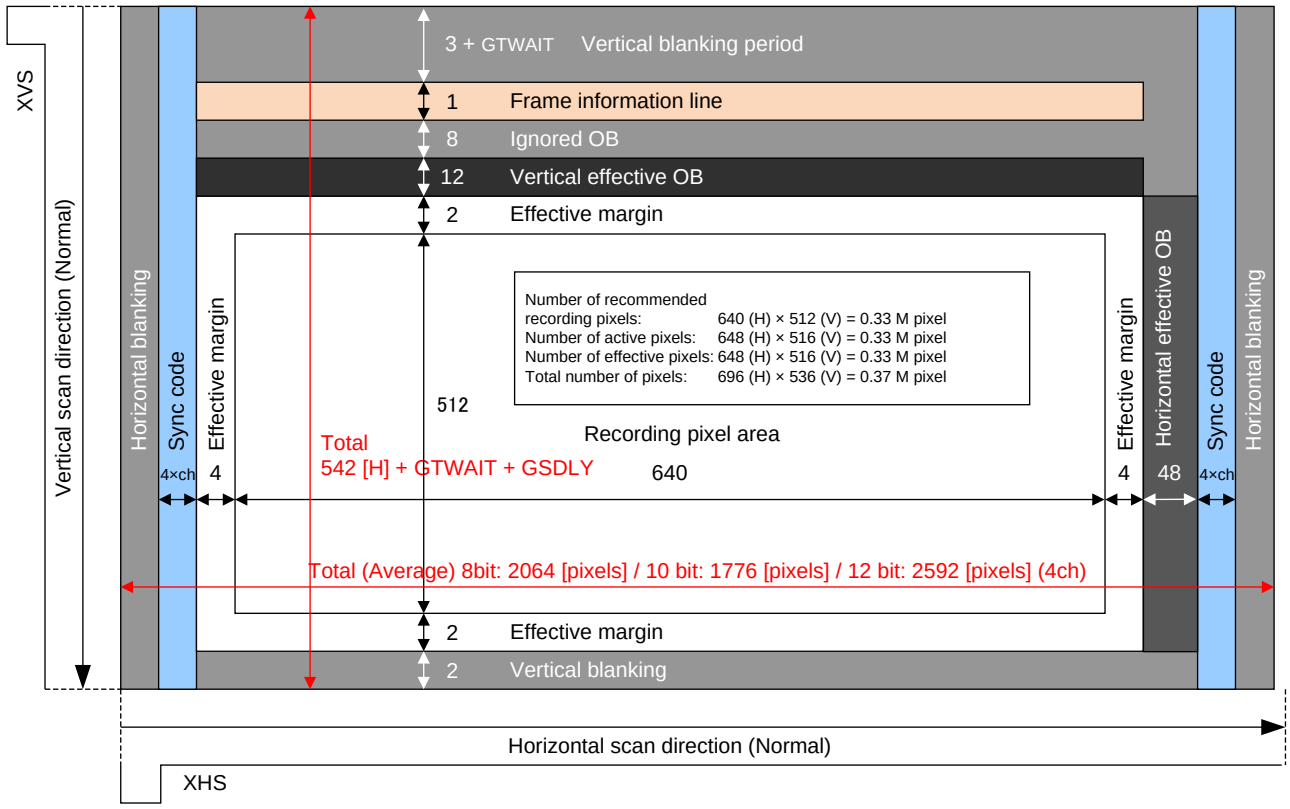
Vertical / Horizontal 1/2 Subsampling mode

V direction and H direction must be set in this mode. (WINMODE = 1h, HMODE = 1)

Register List of Vertical / Horizontal 1/2 subsampling mode

Please set All - pixel scan mode to the settings other than the following.

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 8 bit		AD = 10 bit		AD = 12 bit		
				SLVS 4 ch	SLVS 2 ch	SLVS 4 ch	SLVS 2 ch	SLVS 4 ch	SLVS 2 ch	
				260.68 [frame/s]	260.28 [frame/s]	242.36 [frame/s]	242.36 [frame/s]	138.39 [frame/s]	138.39 [frame/s]	FREQ = 0h
				260.68 [frame/s]	177.45 [frame/s]	242.36 [frame/s]	143.10 [frame/s]	138.39 [frame/s]	120.53 [frame/s]	FREQ = 1h
Chip ID = 02h										
3Ch	[0]	WINMODE	0	1						Subsampling mode
	[4]	HMODE	0	1						Subsampling
D4h	[7:0]	VMAX	436h	228h						
D5h	[7:0]									
D6h	[7:0]									
D8h	[7:0]	HMAX	235h	204h	204h	22Bh	22Bh	3CCh	3CCh	FREQ = 0h
D9h	[7:0]			204h	2F6h	22Bh	3ACh	3CCh	45Ch	FREQ = 1h
DCh	[1:0]	FREQ	0h	0h / 1h						
E2h	[7:0]	GTWAIT	6h	6h						
E3h	[7:0]	GSDLY	4h	4h						
Chip ID = 04h										
20h	[7:0]	INCKSEL0	52h	INCK = 37.125 MHz / 54 MHz: 50h INCK = 74.25 MHz: 52h						
21h	[7:0]	INCKSEL1	20h	INCK = 37.125 MHz / 74.25 MHz: 20h INCK = 54 MHz: 16h						
24h	[7:0]	INCKSEL2	52h	INCK = 37.125 MHz / 54 MHz: 50h INCK = 74.25 MHz: 52h						
25h	[7:0]	INCKSEL3	20h	INCK = 37.125 MHz / 74.25 MHz: 20h INCK = 54 MHz: 16h						
26h	[7:0]	FREQ_SYNC	93h	FREQ = 0: 93h FREQ = 1: A3h						
30h	[7:2]	LLBLANK	04h	04h						
31h	[1:0]									
Chip ID = 06h										
44h	[3:0]	STBSLVS	1h	2h	N/A	2h	N/A	2h	N/A	4 ch SLVS
				N/A	3h	N/A	3h	N/A	3h	2 ch SLVS
45h	[3:0]	OPORTSEL	1h	3h	N/A	3h	N/A	3h	N/A	4 ch SLVS
				N/A	4h	N/A	4h	N/A	4h	2 ch SLVS



Pixel Array Image Drawing in Vertical / Horizontal 1/2 subsampling mode

ROI mode

This Sensor has ROI function that signals are cut out and read out in multi arbitrary positions.
Cropping position can set maximum 64 areas that specified by horizontal 8 points and vertical 8 points, regarding effective pixel start position as origin (0, 0) in all pixel scan mode. Cropping is available from All - pixel scan mode and horizontal period are fixed to the value for this mode.
These cropped areas by horizontal cropping setting (ROI (1, y) to ROI (8, y)) are output with left justified and that extends the horizontal blanking period. In vertical cropping area (ROI (x, 1) to ROI (x, 8)), the number of image data is also output from cropping start line and the frame rate can be adjusted by changing the number of input XVS lines in slave mode or changing register VMAX in master mode.
One invalid frame is generated when the ROI area changing size or cropping address.
ROI image is shown in the figure below.
In case of Vertical / Horizontal 1/2 subsampling mode, this sensor doesn't support ROI mode.

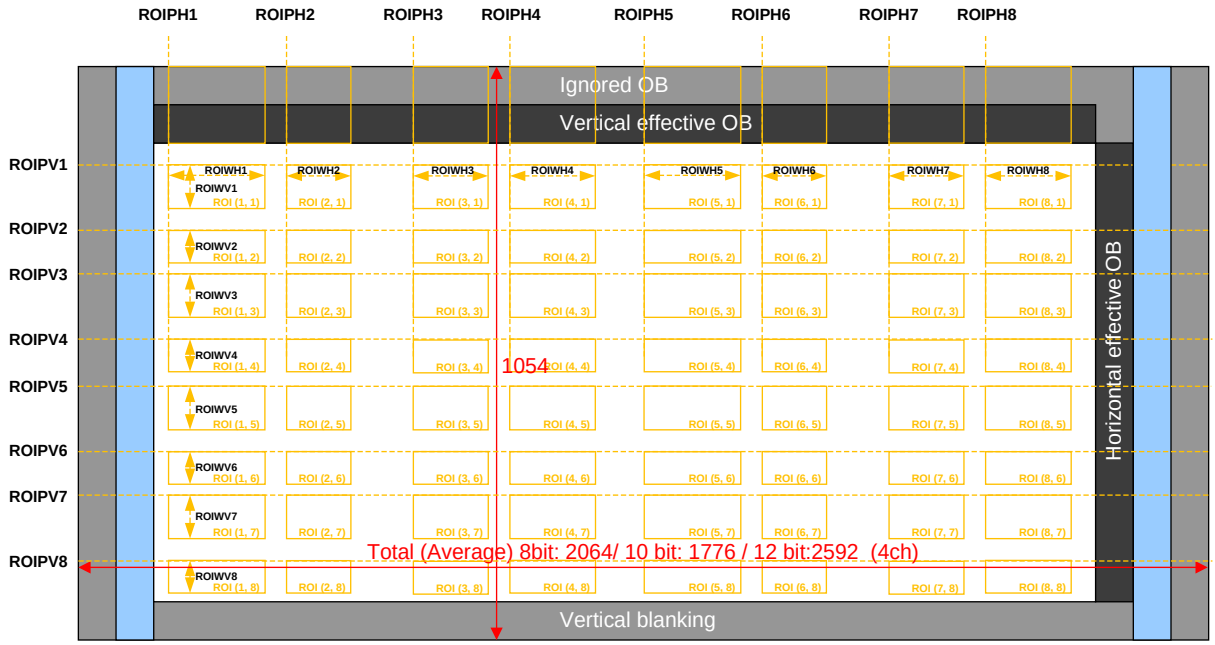
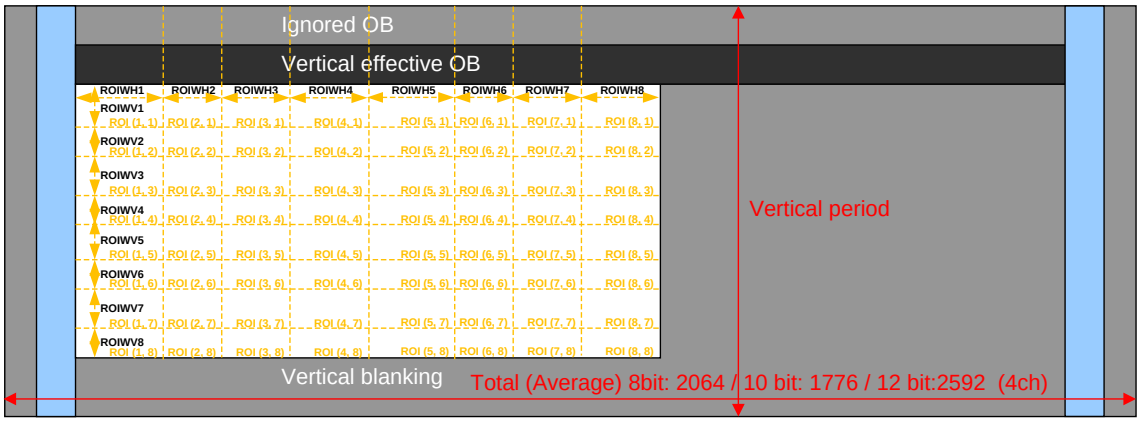


Image Drawing of Designated Areas in ROI Mode



Details of Image Drawing

Register List of ROI mode

Please set All - pixel scan mode to the settings other than the following.

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 8 bit		AD = 10 bit		AD = 12 bit		
				SLVS 4 ch	SLVS 2 ch	SLVS 4 ch	SLVS 2 ch	SLVS 4 ch	SLVS 2 ch	
				*1 [frame/s]	*2 [frame/s]	*3 [frame/s]	*4 [frame/s]	*5 [frame/s]	*6 [frame/s]	
Chip ID = 02h										
3Ch	[0]	WINMODE	0	0						All-pixel mode
	[4]	HMODE	0	0						All-pixel
D4h	[7:0]	VMAX	436h	*1	*2	*3	*4	*5	*6	
D5h	[7:0]									
D6h	[7:0]									
D8h	[7:0]	HMAX	235h	204h	2EEh	22Bh	3A2h	3CCh	450h	FREQ = 0h
D9h	[7:0]			2F6h	5AEh	3ABh	712h	45Ch	870h	FREQ = 1h
DCh	[1:0]	FREQ	0h	0h / 1h						
E2h	[7:0]	GTWAIT	6h	6h						
E3h	[7:0]	GSDLY	4h	4h						
Chip ID = 03h										
04h	[0]	FID0_ROIH1ON	0	The horizontal setting of FID0 ROI area (1, y) (y = 1 to 8) 0: Disable 1: Enable						
	[1]	FID0_ROIV1ON	0	The vertical setting of FID0 ROI area (x, 1) (x = 1 to 8) 0: Disable 1: Enable						
	[2]	FID0_ROIH2ON	0	The horizontal setting of FID0 ROI area (2, y) (y = 1 to 8) 0: Disable 1: Enable						
	[3]	FID0_ROIV2ON	0	The vertical setting of FID0 ROI area (x, 2) (x = 1 to 8) 0: Disable 1: Enable						
	[4]	FID0_ROIH3ON	0	The horizontal setting of FID0 ROI area (3, y) (y = 1 to 8) 0: Disable 1: Enable						
	[5]	FID0_ROIV3ON	0	The vertical setting of FID0 ROI area (x, 3) (x = 1 to 8) 0: Disable 1: Enable						
	[6]	FID0_ROIH4ON	0	The horizontal setting of FID0 ROI area (4, y) (y = 1 to 8) 0: Disable 1: Enable						
	[7]	FID0_ROIV4ON	0	The vertical setting of FID0 ROI area (x, 4) (x = 1 to 8) 0: Disable 1: Enable						
05h	[0]	FID0_ROIH5ON	0	The horizontal setting of FID0 ROI area (5, y) (y = 1 to 8) 0: Disable 1: Enable						
	[1]	FID0_ROIV5ON	0	The vertical setting of FID0 ROI area (x, 5) (x = 1 to 8) 0: Disable 1: Enable						
	[2]	FID0_ROIH6ON	0	The horizontal setting of FID0 ROI area (6, y) (y = 1 to 8) 0: Disable 1: Enable						
	[3]	FID0_ROIV6ON	0	The vertical setting of FID0 ROI area (x, 6) (x = 1 to 8) 0: Disable 1: Enable						
	[4]	FID0_ROIH7ON	0	The horizontal setting of FID0 ROI area (7, y) (y = 1 to 8) 0: Disable 1: Enable						
	[5]	FID0_ROIV7ON	0	The vertical setting of FID0 ROI area (x, 7) (x = 1 to 8) 0: Disable 1: Enable						
	[6]	FID0_ROIH8ON	0	The horizontal setting of FID0 ROI area (8, y) (y = 1 to 8) 0: Disable 1: Enable						
	[7]	FID0_ROIV8ON	0	The vertical setting of FID0 ROI area (x, 8) (x = 1 to 8) 0: Disable 1: Enable						
20h	[7:0]	FID0_ROIPH1	0000h	Designation of horizontal cropping position for FID0 on area (1, y) (y = 1 to 8) *Set the value of multiple of 8						
21h	[4:0]									
22h	[7:0]	FID0_ROIPV1	000h	Designation of vertical cropping position for FID0 on area (x, 1) (x = 1 to 8) *Set the value of multiple of 8						
23h	[3:0]									
24h	[7:0]	FID0_ROIWH1	0000h	Designation of horizontal cropping size for FID0 on area (1, y) (y = 1 to 8) *Set the value of multiple of 4						
25h	[4:0]									
26h	[7:0]	FID0_ROIWV1	000h	Designation of vertical cropping size for FID0 on area (x, 1) (x = 1 to 8) *Set the value of multiple of 8						
27h	[3:0]									
28h	[7:0]	FID0_ROIPH2	0000h	Designation of horizontal cropping position for FID0 on area (2, y) (y = 1 to 8) *Set the value of multiple of 8						
29h	[4:0]									
2Ah	[7:0]	FID0_ROIPV2	000h	Designation of vertical cropping position for FID0 on area (x, 2) (x = 1 to 8) *Set the value of multiple of 8						
2Bh	[3:0]									
2Ch	[7:0]	FID0_ROIWH2	0000h	Designation of horizontal cropping size for FID0 on area (2, y) (y = 1 to 8) *Set the value of multiple of 4						
2Dh	[4:0]									

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 8 bit		AD = 10 bit		AD = 12 bit		
				SLVS 4 ch	SLVS 2 ch	SLVS 4 ch	SLVS 2 ch	SLVS 4 ch	SLVS 2 ch	
				*1 [frame/s]	*2 [frame/s]	*3 [frame/s]	*4 [frame/s]	*5 [frame/s]	*6 [frame/s]	
2Eh	[7:0]	FID0_ROIWV2	000h	Designation of vertical cropping size for FID0 on area (x, 2) (x = 1 to 8) *Set the value of multiple of 8						
2Fh	[3:0]									
30h	[7:0]	FID0_ROIPH3	0000h	Designation of horizontal cropping position for FID0 on area (3, y) (y = 1 to 8) *Set the value of multiple of 8						
31h	[4:0]									
32h	[7:0]	FID0_ROIPV3	000h	Designation of vertical cropping position for FID0 on area (x, 3) (x = 1 to 8) *Set the value of multiple of 8						
33h	[3:0]									
34h	[7:0]	FID0_ROIWH3	0000h	Designation of horizontal cropping size for FID0 on area (3, y) (y = 1 to 8) *Set the value of multiple of 4						
35h	[4:0]									
36h	[7:0]	FID0_ROIWV3	000h	Designation of vertical cropping size for FID0 on area (x, 3) (x = 1 to 8) *Set the value of multiple of 8						
37h	[3:0]									
38h	[7:0]	FID0_ROIPH4	0000h	Designation of horizontal cropping position for FID0 on area (4, y) (y = 1 to 8) *Set the value of multiple of 8						
39h	[4:0]									
3Ah	[7:0]	FID0_ROIPV4	000h	Designation of vertical cropping position for FID0 on area (x, 4) (x = 1 to 8) *Set the value of multiple of 8						
3Bh	[3:0]									
3Ch	[7:0]	FID0_ROIWH4	0000h	Designation of horizontal cropping size for FID0 on area (4, y) (y = 1 to 8) *Set the value of multiple of 4						
3Dh	[4:0]									
3Eh	[7:0]	FID0_ROIWV4	000h	Designation of vertical cropping size for FID0 on area (x, 4) (x = 1 to 8) *Set the value of multiple of 8						
3Fh	[3:0]									
40h	[7:0]	FID0_ROIPH5	0000h	Designation of horizontal cropping position for FID0 on area (5, y) (y = 1 to 8) *Set the value of multiple of 8						
41h	[4:0]									
42h	[7:0]	FID0_ROIPV5	000h	Designation of vertical cropping position for FID0 on area (x, 5) (x = 1 to 8) *Set the value of multiple of 8						
43h	[3:0]									
44h	[7:0]	FID0_ROIWH5	0000h	Designation of horizontal cropping size for FID0 on area (5, y) (y = 1 to 8) *Set the value of multiple of 4						
45h	[4:0]									
46h	[7:0]	FID0_ROIWV5	000h	Designation of vertical cropping size for FID0 on area (x, 5) (x = 1 to 8) *Set the value of multiple of 8						
47h	[3:0]									
48h	[7:0]	FID0_ROIPH6	0000h	Designation of horizontal cropping position for FID0 on area (6, y) (y = 1 to 8) *Set the value of multiple of 8						
49h	[4:0]									
4Ah	[7:0]	FID0_ROIPV6	000h	Designation of vertical cropping position for FID0 on area (x, 6) (x = 1 to 8) *Set the value of multiple of 8						
4Bh	[3:0]									
4Ch	[7:0]	FID0_ROIWH6	0000h	Designation of horizontal cropping size for FID0 on area (6, y) (y = 1 to 8) *Set the value of multiple of 4						
4Dh	[4:0]									
4Eh	[7:0]	FID0_ROIWV6	000h	Designation of vertical cropping size for FID0 on area (x, 6) (x = 1 to 8) *Set the value of multiple of 8						
4Fh	[3:0]									
50h	[7:0]	FID0_ROIPH7	0000h	Designation of horizontal cropping position for FID0 on area (7, y) (y = 1 to 8) *Set the value of multiple of 8						
51h	[4:0]									
52h	[7:0]	FID0_ROIPV7	000h	Designation of vertical cropping position for FID0 on area (x, 7) (x = 1 to 8) *Set the value of multiple of 8						
53h	[3:0]									
54h	[7:0]	FID0_ROIWH7	0000h	Designation of horizontal cropping size for FID0 on area (7, y) (y = 1 to 8) *Set the value of multiple of 4						
55h	[4:0]									
56h	[7:0]	FID0_ROIWV7	000h	Designation of vertical cropping size for FID0 on area (x, 7) (x = 1 to 8) *Set the value of multiple of 8						
57h	[3:0]									
58h	[7:0]	FID0_ROIPH8	0000h	Designation of horizontal cropping position for FID0 on area (8, y) (y = 1 to 8) *Set the value of multiple of 8						
59h	[4:0]									
5Ah	[7:0]	FID0_ROIPV8	000h	Designation of vertical cropping position for FID0 on area (x, 8) (x = 1 to 8) *Set the value of multiple of 8						
5Bh	[3:0]									
5Ch	[7:0]	FID0_ROIWH8	0000h	Designation of horizontal cropping size for FID0 on area (8, y) (y = 1 to 8) *Set the value of multiple of 4						
5Dh	[4:0]									
5Eh	[7:0]	FID0_ROIWV8	000h	Designation of vertical cropping size for FID0 on area (x, 8) (x = 1 to 8) *Set the value of multiple of 8						
5Fh	[3:0]									

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 8 bit		AD = 10 bit		AD = 12 bit		
				SLVS 4 ch	SLVS 2 ch	SLVS 4 ch	SLVS 2 ch	SLVS 4 ch	SLVS 2 ch	
				*1 [frame/s]	*2 [frame/s]	*3 [frame/s]	*4 [frame/s]	*5 [frame/s]	*6 [frame/s]	
Chip ID = 04h										
00h	[6:5]	ADBIT	0h	2h		0h		1h		0: 10 bit 1: 12 bit 2: 8 bit
20h	[7:0]	INCKSEL0	52h	INCK = 37.125 MHz / 54 MHz: 50h INCK = 74.25 MHz: 52h						
21h	[7:0]	INCKSEL1	20h	INCK = 37.125 MHz / 74.25 MHz: 20h INCK = 54 MHz: 16h						
24h	[7:0]	INCKSEL2	52h	INCK = 37.125 MHz / 54 MHz: 50h INCK = 74.25 MHz: 52h						
25h	[7:0]	INCKSEL3	20h	INCK = 37.125 MHz / 74.25 MHz: 20h INCK = 54 MHz: 16h						
26h	[7:0]	FREQ_SYNC	93h	FREQ = 0: 93h FREQ = 1: A3h						
30h	[7:2]	LLBLANK	04h	04h						
31h	[1:0]									
Chip ID = 06h										
30h	[1:0]	ODBIT	0h	2h		0h		1h		0: 10 bit 1: 12 bit 2: 8 bit
44h	[3:0]	STBSLVS	1h	2h	N/A	2h	N/A	2h	N/A	4 ch SLVS
				N/A	3h	N/A	3h	N/A	3h	2 ch SLVS
45h	[3:0]	OPORTSEL	1h	3h	N/A	3h	N/A	3h	N/A	4 ch SLVS
				N/A	4h	N/A	4h	N/A	4h	2 ch SLVS
Chip ID = 07h										
C0h	[7:0]	BLKLEVEL	03Ch	00Fh		03Ch		0F0h		Recommended value
C1h	[3:0]									

Restrictions on ROI mode

The register settings should satisfy following conditions:

* Do not designate area like be overlap.
  ROIPH1 + ROIWH1 ≤ ROIPH2
  ROIPH2 + ROIWH2 ≤ ROIPH3
  ROIPH3 + ROIWH3 ≤ ROIPH4
…
  ROIPH8 + ROIWH8 ≤ 1392d

  ROIPV1 + ROIWV1 ≤ ROIPV2
  ROIPV2 + ROIWV2 ≤ ROIPV3
  ROIPV3 + ROIWV3 ≤ ROIPV4
…
  ROIPV8 + ROIWV8 ≤ 1032d

* Set the horizontal width in multiple of 4 and horizontal position, vertical width / position setting in multiple of 8.

* Minimum width of the window is as below.
  ROIWH1 + ROIWH2 + ROIWH3 + …. + ROIWH8 ≥ 8d

  ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 ≥ 8d

Frame rate on ROI mode

Frame rate [frame/s] = 1 / (("Number of lines per frame" or VMAX) × (1 H period))

* Number of lines per frame or VMAX
  V_{TR} = ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 + GTWAIT + GSDLY + 26
  Refer to the register list of each scan mode for GTWAIT and GSDLY.
* 1H period: Change according to the data rate settings and the number of SLVS channels.
  Calculate by number of INCK in 1 H and the period of INCK.

The example of ROI setting is shown below.
  ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 = 600
  ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 = 8 (minimum value)

Frame rate List of each setting

Register settings No. in register list	1 H period [µs]		Frame rate [frame/s]			
	FREQ 0h	FREQ 1h	Total number of ROI: 600 [line]		Total number of ROI: 8 [line]	
			FREQ = 0h	FREQ = 1h	FREQ = 0h	FREQ = 1h
*1	6.95	10.21	226.25	154.01	3270.34	2226.25
*2	10.1	19.58	155.66	80.29	2250.00	1160.59
*3	7.47	12.66	210.35	124.19	3040.54	1795.21
*4	12.53	24.38	125.53	64.50	1814.51	932.32
*5	13.09	15.03	120.10	104.61	1736.11	1512.09
*6	14.87	29.09	105.74	54.04	1528.53	781.25

Description of Various Function

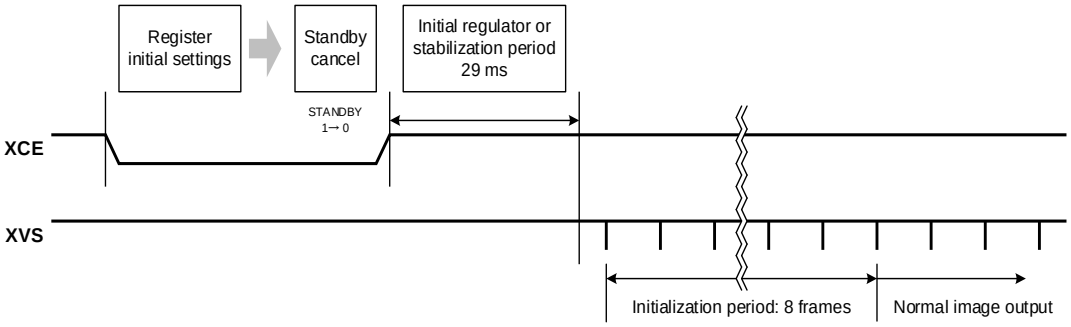
Standby mode

This sensor stops its operation and goes into standby mode which reduces the power consumption by writing “1” to the standby control register STANDBY. Standby mode is also established after power-on or other system reset operation.

Register List of Standby setting

Register	Register details			Initial value	Setting value	Remarks
	Chip ID	Address ( ): I^2C	bit			
STANDBY	02h	00h (3000h)	[0]	1h	1h: Standby 0h: Operating	Register communication is executed even in standby mode.

The serial communication registers hold the previous values. However, the address registers transmitted in standby mode are overwritten. The serial communication block operates even in standby mode, so standby mode can be canceled by setting the STANDBY register to “0”. Some time is required for sensor internal circuit stabilization after standby mode is canceled. For details on the sequence of setting and cancel of standby mode, see the sensor setting flow after power on.
After standby mode is canceled, a normal image is output from the 9 frames after internal regulator stabilization (29 ms or more).



Sequence from Standby Cancel to Stable Image Output

Slave Mode and Master Mode

The sensor can be switched between slave mode and master mode.
The switching is made by the XMASTER pin. Establish the XMASTER pin status before canceling the system reset. (Do not switch this pin status during operation.)
Input a vertical sync signal to XVS and input a horizontal sync signal to XHS when a sensor is in slave mode.
For sync signal interval, input data lines to output for vertical sync signal and 1H period designated in each operating mode for horizontal sync signal. See the section of "Readout Drive mode" for the number of output data line and 1H period.
Set the XMSTA register to “0” in order to start the operation after setting to master mode. In addition, set the count number of sync signal in vertical direction by the VMAX [23:0] register and the clock number in horizontal direction by the HMAX [15:0] register. See the description of operation mode for details of the section of “Readout Drive Modes”.

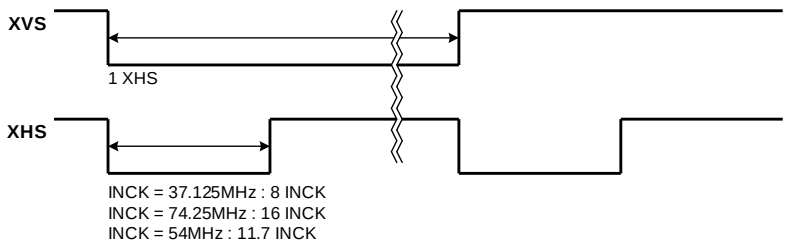
Pin Processing

Pin name	Pin processing	Operation mode	Remarks
XMASTER pin	Low fixed	Master mode	High: OV_{DD} Low: GND
	High fixed	Slave mode	

Register List of Slave Mode and Master Mode

Register	Register details			Initial value	Setting value	Remarks
	Chip ID	Address ( ): I^2C	Bit			
XMSTA	02h	0Ch (300Ch)	[0]	1h	1h: Master operation ready (Initial value) 0h: Master operation start	The master operation starts by setting 0.
VMAX [23:0]		D4h (30D4h)	[7:0]	000436h	See the item of each drive mode	Line number per frame designated (Master mode and Slave mode common setting.)
		D5h (30D5h)	[7:0]			
		D6h (30D6h)	[7:0]			
HMAX [15:0]		D8h (30D8h)	[7:0]	0235h	See the item of each drive mode	Clock number per line designated (Master mode and Slave mode common setting.)
		D9h (30D9h)	[7:0]			

XVS / XHS Output Waveform in Master Mode



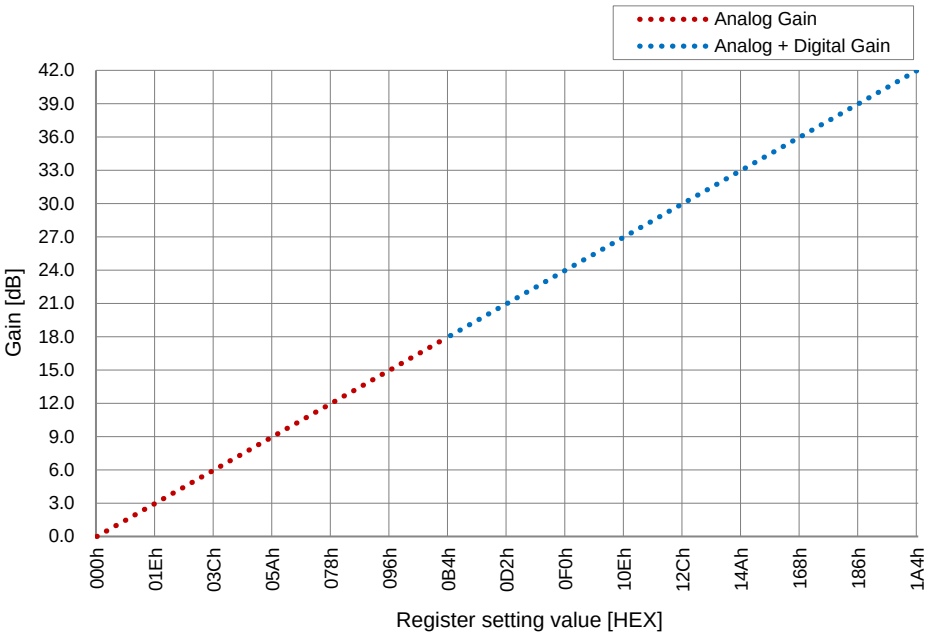
Gain Adjustment Function

PGC

The Programmable Gain Control (PGC) of this device consists of the analog block and digital block.
The total of analog gain and digital gain can be set up to 42 dB by the GAIN [8:0] register setting.
The value which is ten times the gain is set to register.

Example)
When set to 6 dB:

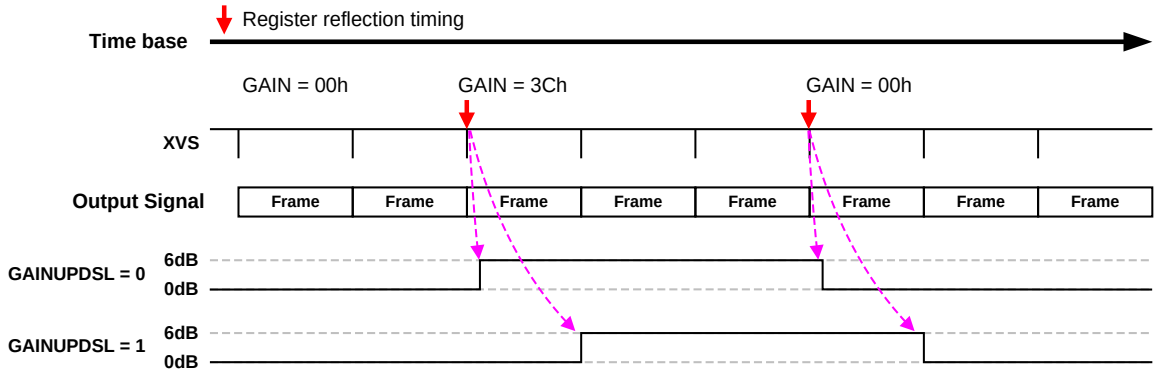
6 × 10 = 60d, GAIN = 03Ch



Register List of Gain setting

Register	Register details			Initial value	Setting value	Remarks
	Chip ID	Address ( ): I²C	bit		Setting range	
GAIN [8:0]	07h	14h (3514h)	[7:0]	000h	000h to 1A4h (0d to 420d)	Setting value: Gain [dB] × 10
		15h (3515h)	[0]			

Gain reflection timing in the normal mode is changed by the set value of GAINUPDSL as shown below. In the trigger mode, set 0 to the register GAINUPDSL.



Gain Reflection Timing

Black Level Adjustment Function

The black level offset (offset variable range: 000h to FFFh) can be added relative to the data in which the digital gain modulation was performed by the BLKLEVEL [11:0] register. When the BLKLEVEL [11:0] setting is increased by 1 LSB, the black level is increased by 1 LSB.

* Use with values shown below is recommended.
  8 bit output: 00Fh (15 d)
  10 bit output: 03Ch (60 d)
  12 bit output: 0F0h (240 d)

Register List of Black level adjustment

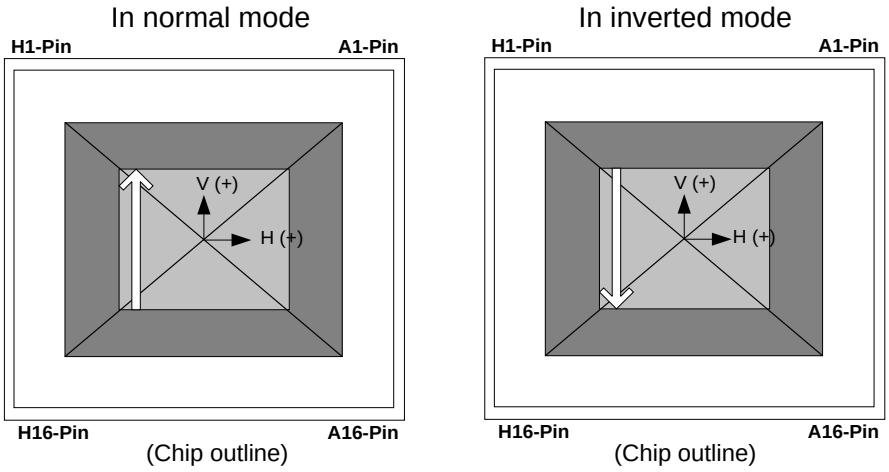
Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I^2C	bit		
BLKLEVEL [11:0]	07h	C0h (35C0h)	[7:0]	03Ch	000h to FFFh
		C1h (35C1h)	[3:0]		

Horizontal / Vertical Normal Operation and Inverted Operation

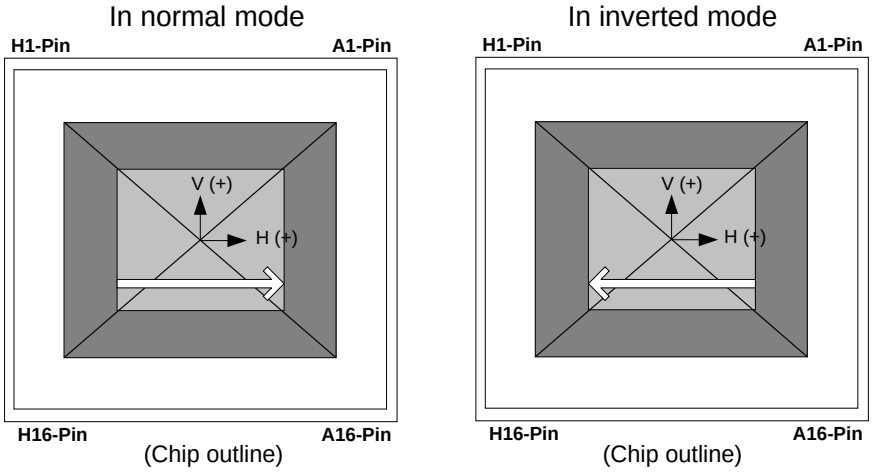
The sensor readout direction (normal / inverted) in vertical direction can be switched by the VREVERSE register setting and sensor readout direction (normal / inverted) in horizontal direction can be switched by the HREVERSE register setting. See the section of “Readout Drive Modes” for the order of readout lines in normal and inverted modes.

Register List of Readout Drive Direction setting

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I²C	bit		
VREVERSE	04h	04h (3204h)	[0]	0h	0h: Normal (Initial value) 1h: Inverted
HREVERSE			[1]	0h	0h: Normal (Initial value) 1h: Inverted



Normal and Inverted Drive Outline in Vertical Direction (TOP VIEW)



Normal and Inverted Drive Outline in Horizontal Direction (TOP VIEW)

Shutter and Integration Time Settings

This sensor has a global shutter function that integrates to all line collectively by using memory in each pixel.
This sensor has a variable electronic shutter function that can control the integration time in line units for adjust the exposure time. This sensor transferred signal to memory in pixel after the exposure (memory transfer), then this sensor performs output in which readout operation is performed sequentially for each line in sync with the XHS signal.
This sensor has trigger mode that can be controlled exposure start timing and memory transfer timing by trigger.

Note) For integration time control, an image which reflects the setting is output from the frame after the setting changes.

In this item, the shutter operation and storage time are shown as in the figure below with the time sequence on the horizontal axis and the vertical address on the vertical axis. For simplification, shutter and readout operation are noted in line units.

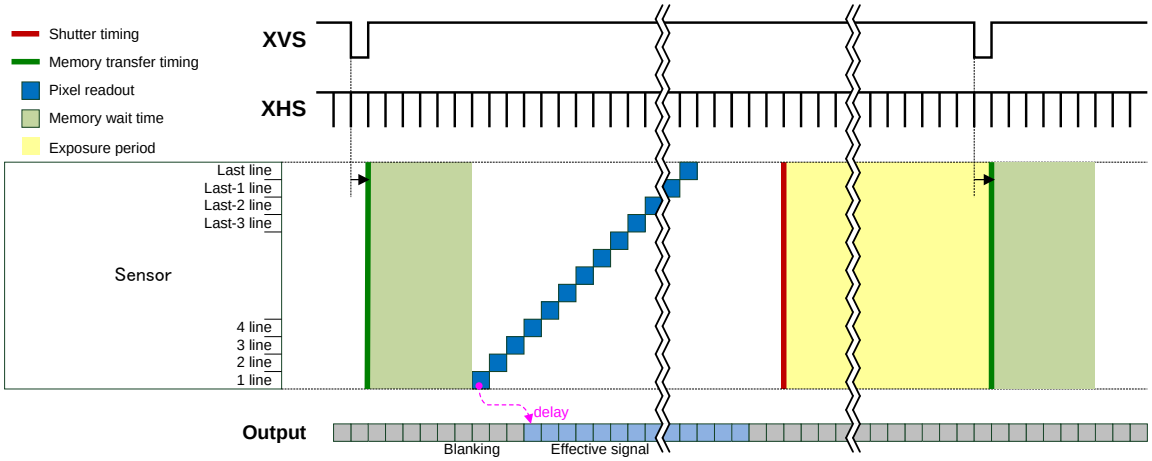


Image Drawing of Global Shutter (Normal mode) Operation

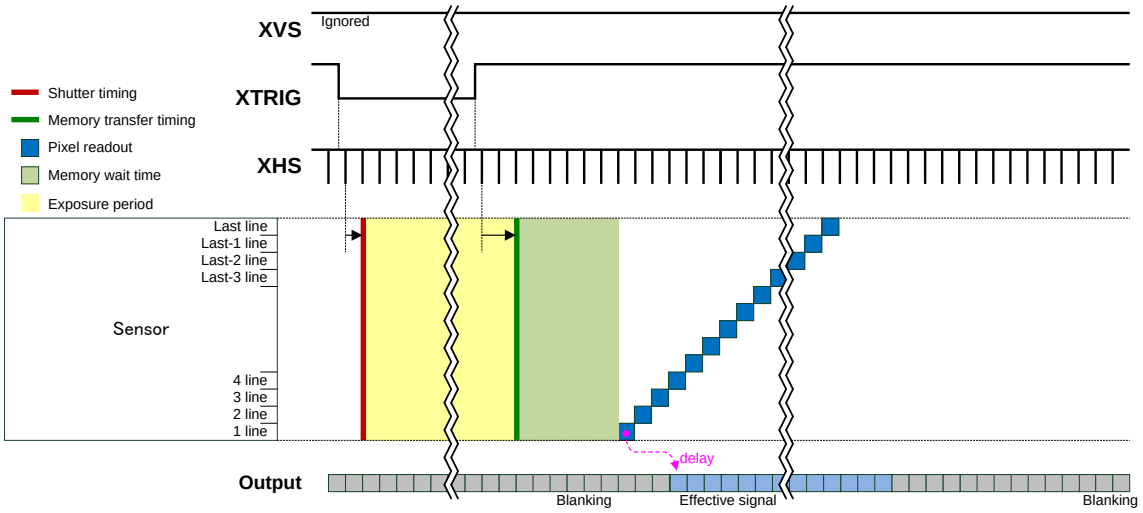


Image Drawing of Global Shutter (Sequential Trigger mode) Operation

Global Shutter (Normal Mode) Operation

The integration time can be controlled by varying the electronic shutter timing. In the electronic shutter settings, the integration time is controlled by the SHS [23:0] register. For setting value of SHS [23:0], see the table “List of Exposure Setting”. When the sensor is operating in slave mode, the number of lines per frame is determined by the XVS interval (number of lines), using the input XHS interval as the line unit. When the sensor is operating in master mode, the number of lines per frame is determined by the VMAX [23:0] register. The number of lines per frame differs according to the operating mode.

Calculation Formula of Exposure Time

Exposure time [s] = (1 H period) × (Number of lines per frame - SHS) + 7.372 [μs][*1]

[*1]: Exposure time error (t_{OFFSET})

Register List of Shutter setting

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I^2C	bit		
VMAX [23:0]	02h	D4h (30D4h)	[7:0]	000436h	Set the number of lines per frame (only in master mode)
		D5h (30D5h)	[7:0]		
		D6h (30D6h)	[7:0]		
GTWAIT [7:0]		E2h (30E2h)	[7:0]	6h	Refer to the register setting lists of each scan mode .
SHS [23:0]	04h	40h (3240h)	[7:0]	000018h	Set the shutter sweep time. (GTWAIT + 9) to (Number of lines per frame - 1)
		41h (3241h)	[7:0]		
		42h (3242h)	[7:0]		

List of Exposure Setting

Drive mode	memory wait time [H]	Number of lines per frame [DEC]	SHS Setting value [DEC]	Exposure Setting value [H]	AD 10bit, FREQ 0, 4 ch output	
					Frame rate [frame/s]	Actually exposure [ms]*3
All - pixel	6 (GTWAIT)	1068 (VMAX)	1067	1	125.27	0.015
			1066	2		0.022
			…	…		…
			16	1052		7.871
			15	1053		7.878
Vertical / Horizontal 1/2 Subsampling mode	6 (GTWAIT)	552 (VMAX)	551	1	242.36	0.015
			550	2		0.022
			…	…		…
			16	536		4.014
			15	537		4.021
ROI	6 (GTWAIT)	V_{TR}*1	V_{TR}-1	1	*2	0.015
			V_{TR}-2	2		0.022
			…	…		…
			16	VTR-16		*3
			15	VTR-15		

*1 V_{TR} and the frame rate, refer to the section “ROI mode” in “Readout Drive Mode”.
*2 INCK frequency is input by typical value, and t_{OFFSET} (7.372 [µs]) is included.
*3 Conform to the calculation formula of exposure time. (Number of lines per frame = V_{TR})

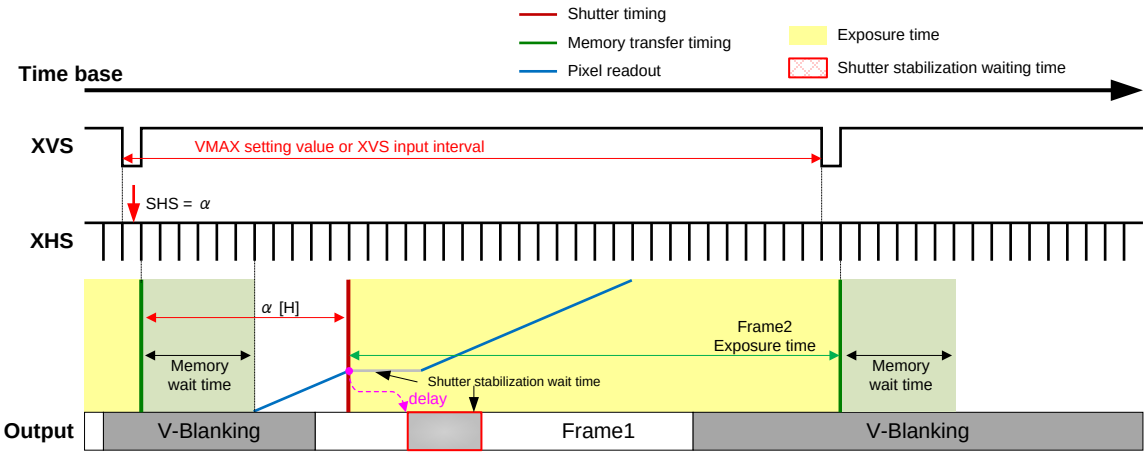


Image Drawing of Global Shutter (Normal Mode)

Global Shutter (Sequential Trigger Mode) Operation

The integration time can be controlled by varying the pulse width that is input to XTRIG pin. The pulse width designated in XHS unit [H]. For the transition from normal mode to trigger mode, set 1 to the register TRIGEN. The XVS input signal is ignored during trigger mode operating. In case of inputting trigger continuously, there are period which prohibit the trigger rise input (t_{TGPD}) and fall input (t_{TGES}) based on the previous trigger rise. When the trigger rise is input before the rise input prohibited period (t_{TGPD}), interrupt operation starts. This function is slave mode only. The number of lines per frame differs according to the operating mode.

Calculation Formula of Exposure Time

Exposure time [s] = (XTRIG low level pulse width [H][*2]) + 7.372 [µs][*1]

[*1]: Exposure time error (t_{OFFSET})

[*2]: Low level pulse width is counted by XHS pulse.

Register List of shutter setting

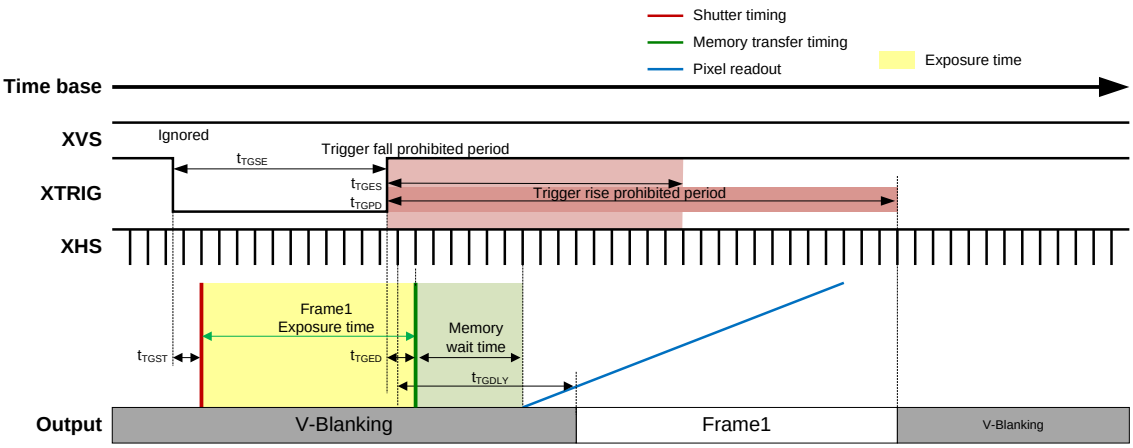
Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I²C	bit		
XMSTA	02h	0Ch (300Ch)	[0]	1	Setting of master mode operation 0: Master mode operation start 1: Master mode operation stop
VINT_EN	04h	32h (3232h)	[0]	1	Setting of Interrupt mode in Trigger Mode 0: V interrupt is disabled 1: V interrupt is enabled
TRIGEN	06h	00h (3400h)	[0]	0	Global shutter mode setting 0: Normal mode 1: Trigger mode

Parameter List of Global Shutter (Sequential Trigger Mode)

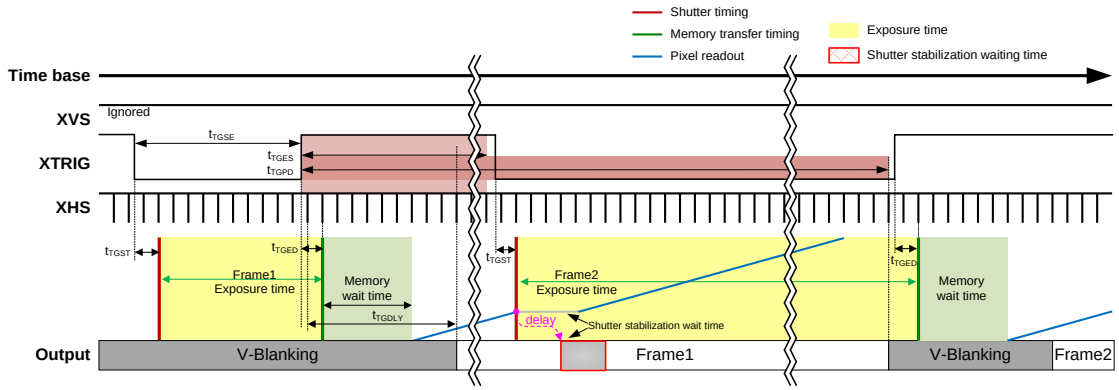
Item	Symbol	Min.	Typ.	Max.	Unit
Integration start delay	t_{TGST}	1	—	2	H
Integration end delay	t_{TGED}	1 + t_{OFFSET}	—	2 + t_{OFFSET}	H
Pulse width	t_{TGSE}	1	—	—	H
Next trigger fall prohibited period	t_{TGES}	10 + GTWAIT[*1]	—	—	H
Next trigger rise prohibited period (All - pixel / 1/2 Subsampling)	t_{TGPD}	VMAX	—	—	H
Next trigger rise prohibited period (ROI)		V_{TR}[*2]	—	—	
Data output delay	t_{TGDLY}	—	4 + GTWAIT[*1]	—	H

[*1] Refer to the register setting lists in each scan modes.

[*2] V_{TR} (See the section “ROI mode” in “Readout Drive Mode”)



Single shutter Image Drawing of Global Shutter (Sequential Trigger Mode)



Multi shutter image Drawing of Global Shutter (Sequential Trigger Mode)

Interrupt Operation

In case of VINT_EN = 1h, the image drawing when the interrupt operation is generated is shown below. When the trigger is raised again and the next frame is output during read of the frame for which read was started by a trigger rise (Frame 1 in the figure below), Frame 1 becomes an invalid frame. Trigger timing of interrupt generating corresponds to t_{TGPD} in Parameter List of Global Shutter (Trigger Mode)
In case of VINT_EN = 0h, both of the rising edge and the falling edge of the trigger signal are ignored in t_{TGPD} (Prohibit period).

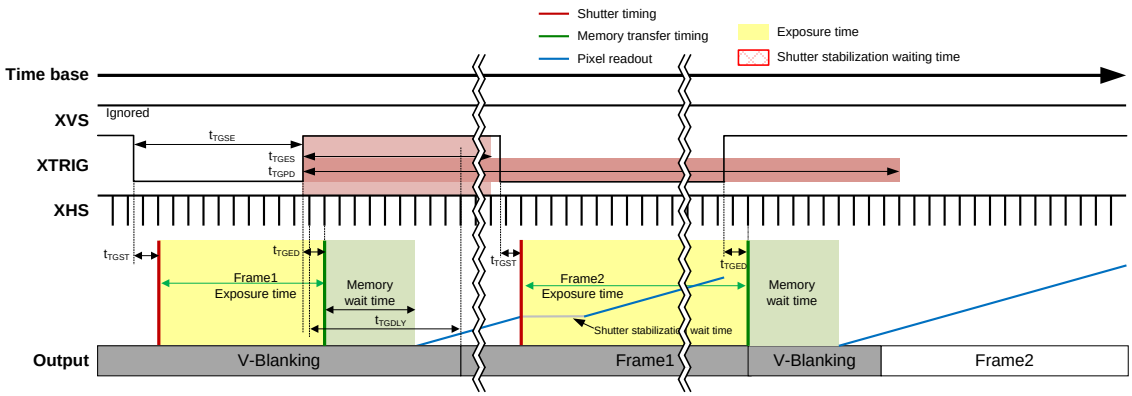


Image Drawing of Interrupt Operation in Global Shutter (Sequential Trigger Mode)

Global Shutter (Fast Trigger Mode) Operation

Fast trigger mode is the trigger mode that starts exposure at fall of XTRIG immediately.
This mode supports Master mode only.

Calculation Formula of Exposure Time

Exposure time [s] = (XTRIG low level pulse width [µs]) + 7.372 [µs][*1]
[*1]: Exposure time error (t_{OFFSET})

Register List of shutter setting

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I²C	bit		
XMSTA	02h	0Ch (300Ch)	[0]	1	Setting of master mode operation 0: Master mode operation start 1: Master mode operation stop
FASTTRIG	04h	30h (3230h)	[1]	0	Selection of trigger mode 0: Except for Fast trigger mode 1: Fast trigger mode
TRIGEN	06h	00h (3400h)	[0]	0	Global shutter mode setting 0: Normal mode 1: Trigger mode
SYNCSEL		3Ch (343Ch)	[5:4]	0h	XHS, XVS pin setting 0h: Normal Output 3h: Hi-Z

Parameter List of Global Shutter (Fast Trigger Mode)

Item	Symbol	Min.	Typ.	Max.	Unit
Integration start delay	t_{TGST}	—	—	0.13	µs
Integration end delay	t_{TGED}	—	—	0.13 + t_{OFFSET}	µs
Pulse width	t_{TGSE}	0.05	—	—	µs
Next trigger rise / fall prohibited period (All - pixel / 1 / 2 Subsampling)	t_{TGPD}	VMAX	—	—	H
Next trigger rise / fall prohibited period (ROI)		V_{TR}[*2]	—	—	
Data output delay	t_{TGDLY}	—	3 + GTWAIT[*1]	—	H

[*1] Refer to the register setting lists in each scan modes.
[*2] V_{TR} (See the section “ROI mode” in “Readout Drive Mode”)

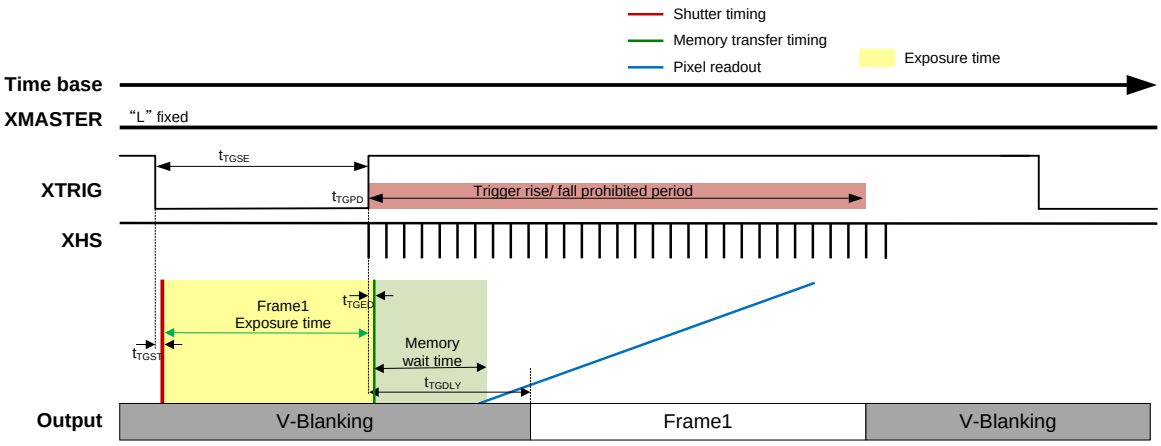


Image Drawing of Global Shutter (Fast Trigger Mode) (4-wire)

Mode Transitions of Global Shutter Operation

The sensor can be switched between normal mode and trigger mode in global shutter operation by setting the register TRIGEN. The sensor will transition to normal mode or trigger mode GTWAIT (H) after the register TRIGEN is set. TRIGEN register can be changed in V-blank period or in standby mode.
(The XVS and XTRIG input during transition are prohibited.)
In case of Fast Trigger mode, the mode transition must be done via sensor standby.

Transition from Normal Mode to Sequential Trigger Mode

The sensor will transition from normal mode to trigger mode after setting 1d to register TRIGEN. The XVS input is ignored after transition to trigger mode. Trigger input is prohibited for a GTWAIT (H) period after the register TRIGEN is set.

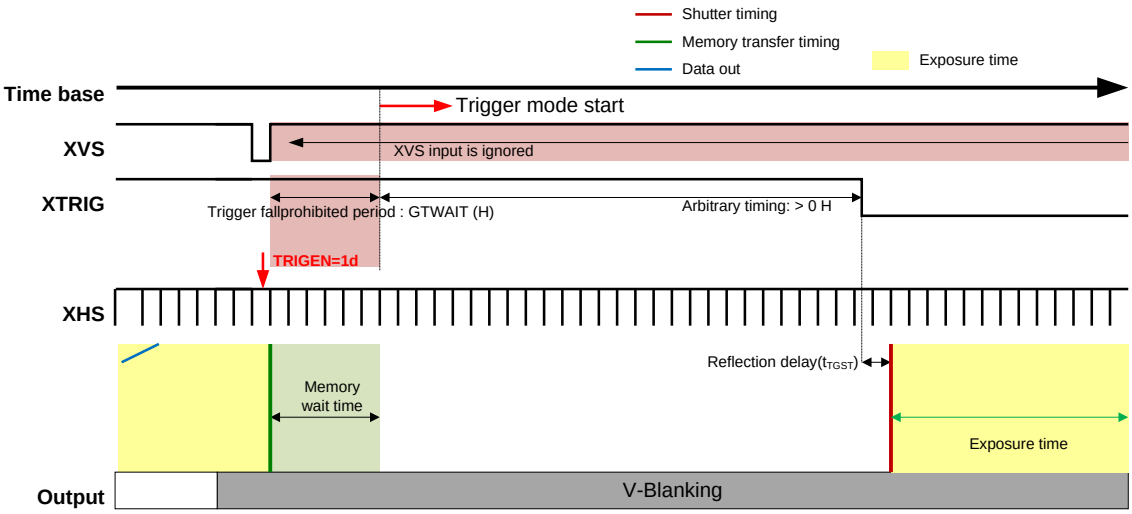


Image Drawing of Transition from Normal Mode to Sequential Trigger Mode

Transition from Sequential Trigger Mode to Normal Mode

The sensor will transition from trigger mode to normal mode after setting 0d to register TRIGEN. Start XVS input after transition to normal mode. Set TRIGEN after Next trigger rise prohibited period (t_{TGPD}) has passed.

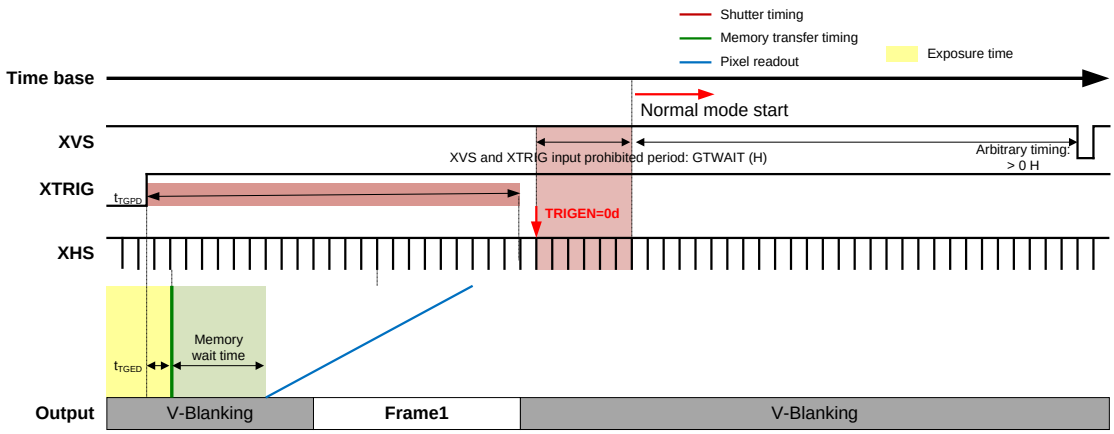


Image Drawing of Transition from Sequential Trigger Mode to Normal Mode

Pulse Output Function

This sensor has a pulse output function that indicates each state of shutter operation. The pulse output from TOUT1 pin and TOUT2 pin. The rise timing and fall timing of pulse are set by Register. For the reference point (The timing when register value set to 0) to be set, see the table “List of Reference point". The pulse is output asynchronously with other signals on the basis of the sensor internal timing shown in the “List of Reference point". This function doesn't support Fast Trigger mode.

Register List of Pulse Output Function

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I²C	bit		
TOUT1SEL [1:0]	06h	35h (3435h)	[1:0]	0h	TOUT1 pin setting 0h: Low fixed 3h: Pulse output
TOUT2SEL [1:0]			[3:2]	0h	TOUT2 pin setting 0h: Low fixed 3h: Pulse output
TRIG_TOUT1_SEL [3:0]		3Ah (343Ah)	[3:0]	0h	TOUT1 pin output selection 0h: Low fixed 1h: Pulse1 output
TRIG_TOUT2_SEL [3:0]			[7:4]	0h	TOUT2 pin output selection 0h: Low fixed 2h: Pulse2 output
PULSE1_EN_NOR		78h (3478h)	[0]	0	Pulse1 enable in normal mode 0: disable 1: enable
PULSE1_EN_TRIG			[1]	0	Pulse1 enable in trigger mode 0: disable 1: enable
PULSE1_POL			[2]	0	Pulse1 polarity selection 0: High active 1: Low active
PULSE1_UP [23:0]		79h (3479h)	[7:0]	000000h	Pulse1 active period start timing setting Designated in line units from reference point
		7Ah (347Ah)	[7:0]		
		7Bh (347Bh)	[7:0]		
PULSE1_DN [23:0]		7Ch (347Ch)	[7:0]	000000h	Pulse1 active period end timing setting Designated in line units from reference point
		7Dh (347Dh)	[7:0]		
		7Eh (347Eh)	[7:0]		
PULSE2_EN_NOR		80h (3480h)	[0]	0	Pulse2 enable in normal mode 0: disable 1: enable
PULSE2_EN_TRIG			[1]	0	Pulse2 enable in trigger mode 0: disable 1: enable
PULSE2_POL			[2]	0	Pulse2 polarity selection 0: High active 1: Low active
			[5]	0	Fixed to 1
PULSE2_UP [23:0]		81h (3481h)	[7:0]	000000h	Pulse2 active period start timing setting Designated in line units from reference point
		82h (3482h)	[7:0]		
		83h (3483h)	[7:0]		
PULSE2_DN [23:0]		84h (3484h)	[7:0]	000000h	Pulse2 active period end timing setting Designated in line units from reference point
		85h (3485h)	[7:0]		
		86h (3486h)	[7:0]		

List of Reference Point

	Normal mode	Trigger mode
Reference point of Pulse1	XVS fall edge in N frame	Fall edge of input trigger
Reference point of Pulse2	XVS fall edge in N +1 frame	Rise edge of input trigger

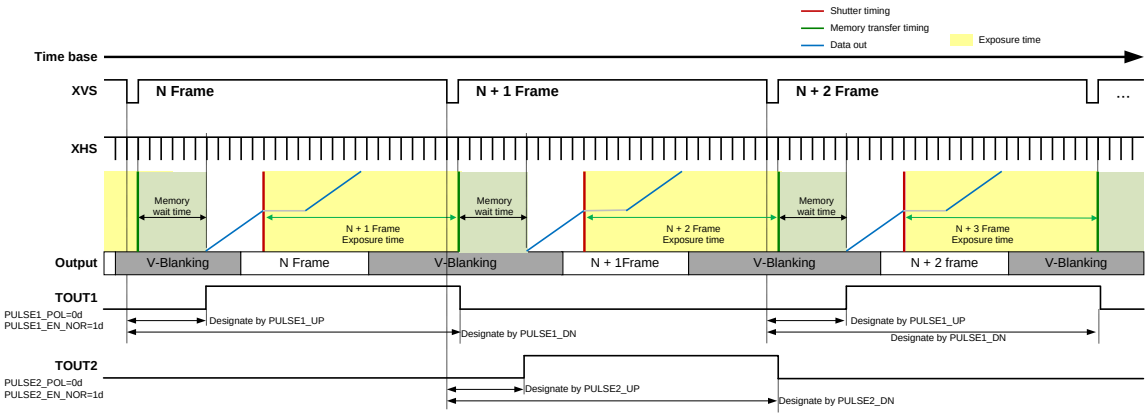


Image Drawing of Pulse Output Function in Global Shutter (Normal Mode)

In normal mode, TOUT1 and TOUT2 are output alternately each time inputting XVS.

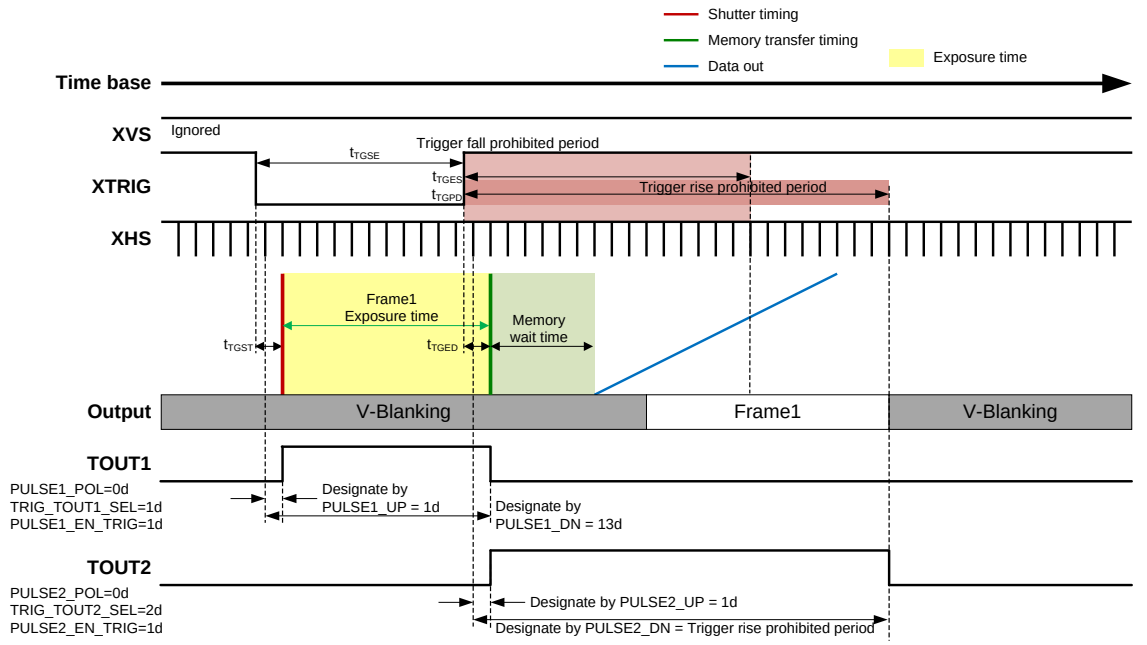


Image Drawing of Pulse Output Function in Global Shutter (Sequential Trigger Mode)

Signal Output

Output Pin Settings

This sensor supports SLVS (2 ch / 4 ch switching) output. In addition, the data rate per channel is adjustable. The table below shows the output format settings.

Register List of Output Settings

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I^2C	bit		
FREQ [1:0]	02h	DCh (30DCh)	[1:0]	0h	Frame rate adjust
FREQ_SYNC [7:0]	04h	26h (3226h)	[7:0]	93h	Refer to the register list in each Readout mode
STBSLVS [3:0]	06h	44h (3444h)	[3:0]	1h	The un-using SLVS channel go into standby
OPORTSEL [3:0]		45h (3445h)	[3:0]	1h	SLVS Output channel selection (Refer the list of output pins below)

Output Pins

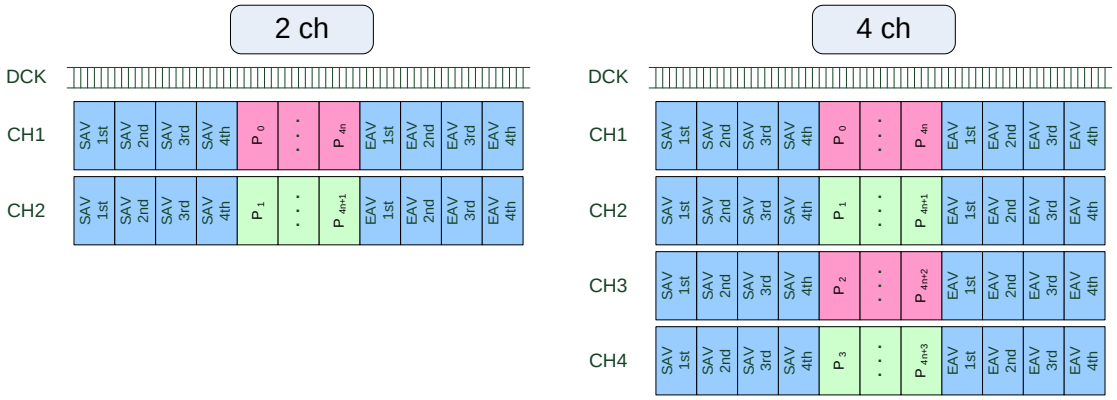
Output pins	SLVS output	
	2 ch	4 ch
DOP0 / DOM0	Hi-Z	Ch 3
DOP1 / DOM1	Ch 1	Ch 1
DOP2 / DOM2	Ch 2	Ch 2
DOP3 / DOM3	Hi-Z	Ch 4
DCKP / DCKM	DCK	DCK

SLVS 2 ch / 4 ch output format is shown in the figure below.

When setting 2 ch, after four data of SAV is output in the order of CH1 to CH2 pixel data is repeatedly output in the same order and then four data of EAV is output in the same order to CH1 to CH2 respectively.

When setting 4 ch, after four data of SAV is output in the order of CH1 to CH4 pixel data is repeatedly output in the same order and then four data of EAV is output in the same order to CH1 to CH4 respectively.

Data is sent MSB first. For details, see drive timing in each mode in the section of "Readout Drive Mode".



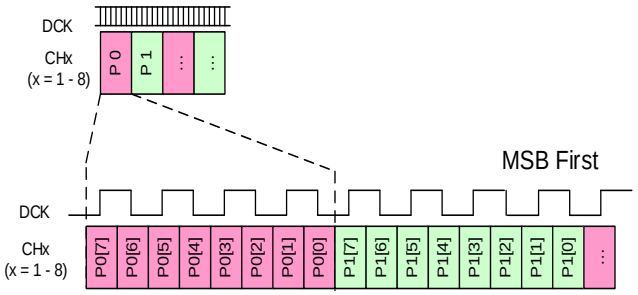
Output Format of SLVS 2 ch / 4 ch

Output Pin Bit Width Selection

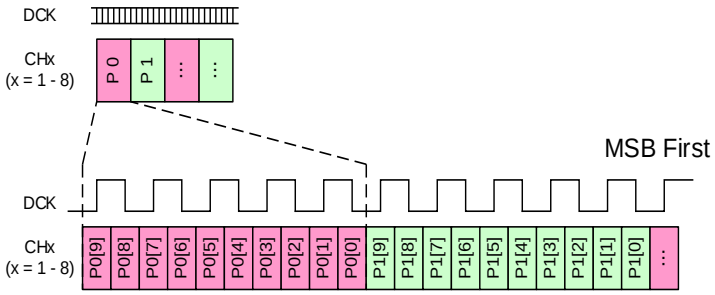
The output pin width can be selected from 8-bit, 10-bit or 12-bit output using register ADBIT, ODBIT. Sync code is output according to bit width setting of these registers.

Register List of Bit Width Selection

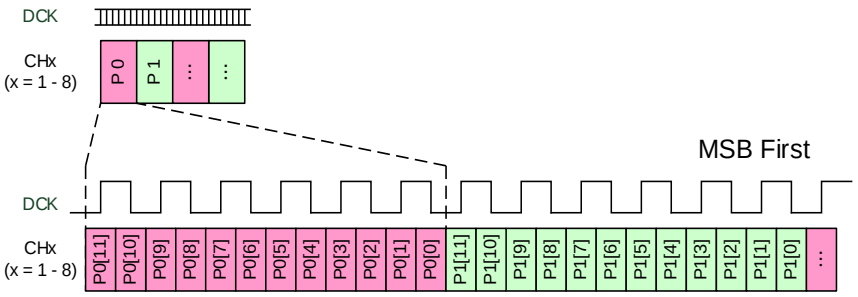
Register	Register details			Initial value	Setting value	Remarks
	Chip ID	Address ( ): I²C	bit			
ADBIT	04h	00h (3200h)	[6:5]	0h	0h: 10 bit 1h: 12 bit 2h: 8 bit	Set same value to both ADBIT and ODBIT
ODBIT	06h	30h (3430h)	[1:0]	0h	0h: 10 bit 1h: 12 bit 2h: 8 bit	



Example of Data format in SLVS 8-bit output



Example of Data format in SLVS 10-bit output



Example of Data format in SLVS 12-bit output

Output Signal Range

The sensor output has either a 8-bit or 10-bit or 12-bit gradation, but SLVS output is not performed over the full range, and the maximum output value is the “FFh – 1” (8-bit output), the “3FFh - 1” (10-bit output) and the “FFFh - 1” (12-bit output). The minimum value is 001h. The output range for each output gradation is shown in the table below. The maximum level and the minimum level are output only in the sync code. See the item of “Sync Codes” in the section of “Operating Modes” for the sync codes.

Output Gradation and Output Range

Output gradation	Output value	
	Min.	Max.
8 bit	01h	FEh
10 bit	001h	3FEh
12 bit	001h	FFEh

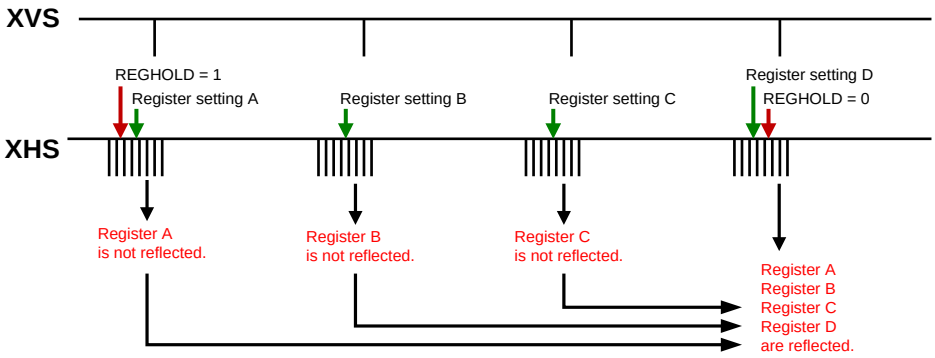
Register Hold Setting

For the registers marked "V" in the item of Reflection timing, register setting can be transmitted with divided to several frames and it can be reflected globally at a certain frame by the register REGHOLD. By setting REGHOLD = 1, the registers that are set thereafter aren't reflected at "frame reflection register reflection timing". The registers that are set during REGHOLD = 1 are reflected globally by setting REGHOLD = 0 by the "frame reflection register reflection timing" before the frame which you want to reflect the registers.

Refer to "Register Communication Timing (4-wire)" and "Register Communication Timing (I^2C)" for "frame reflection register reflection timing".

Register List of Register Hold

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I^2C	bit		
REGHOLD	02h	34h (3034h)	[0]	0h	0h: Invalid 1h: Valid (Register hold)



Register Hold Setting

Mode Transition

The Mode transition between operations is shown below. These examples shown in case that setting is completed within one communication timing.

List of Mode Transition

Transition			State
ROI	→	All - pixel	Via the Standby state is unnecessary
All - pixel	→	ROI	
- Transition between modes other than the above - Change the input frequency of INCK[*1] - Change the register setting noted “S” in the reflection timing column of the Register Map			Via the standby state is necessary

[*1] When changing input INCK frequency, care should be taken not to be input pulses whose width are shorter than the High / Low level width in front and behind of the INCK pulse at the frequency change. If the pulses above generate at the frequency change, change INCK frequency during system reset in the state of XCLR = Low, and then perform system clear in the state of XCLR = High following the item of "Power on sequence" in the section of "Power on / off sequence". Execute initial setting again because the register settings become default state after system clear.

Digital Thermometer

This sensor has a digital thermometer which indicates the junction temperature (Tj) of the sensor. The temperature can be known by reading TMP_OUT register. The way to calculate the temperature is as below.

Temperature [˚C] = (-256d * TMP_OUT[11]) + TMP_OUT[10:3]
+ (0.5 * TMP_OUT[2]) + (0.25 * TMP_OUT[1]) + (0.125 * TMP_OUT[0])

Example)
If TMP_OUT[11] = 1h, TMP_OUT[10:3] = F9h, TMP_OUT[2] = 0h, TMP_OUT[1] = 1h, and TMP_OUT[0] = 1h,
Temperature [˚C] = (-256d * 1) + 249d + (0.5 * 0) + (0.25 *1) + (0.125 * 1) = -6.625 [˚C].

If TMP_OUT[11] = 0h, TMP_OUT[10:3] = 0Fh, TMP_OUT[2] = 0h, TMP_OUT[1] = 0h, and TMP_OUT[0] = 0h,
Temperature [˚C] = (-256d * 0) + 15d + (0.5 * 0) + (0.25 * 0) + (0.125 * 0) = 15.000 [˚C].

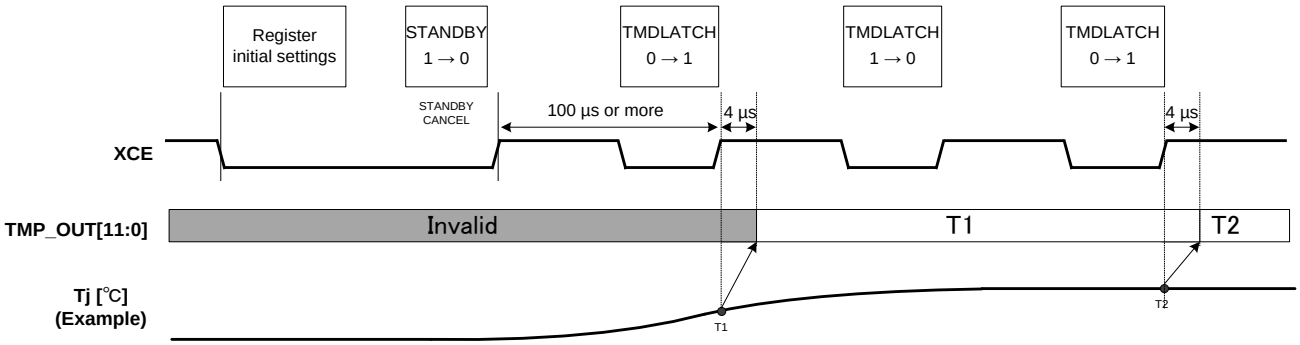
The resolution of the digital thermometer is about 0.3 ˚C.

Register List

Register	Register details			Initial value	value
	Chip ID	Address ( ): I²C	bit		
TMDLATCH	07h	88h (3588h)	0	0	Thermometer output is updated when this register is set from 0h to 1h.
TMP_OUT[11:0]	06h	90h	[7:0]	0	Output of the digital thermometer
		91h	[3:0]		

Thermometer update timing

TMP_OUT[11:0] is updated in 4 µs after TMDLATCH register is changed from “0” to “1”. TMP_OUT[11:0] is invalid value in standby mode. In case of updating the thermometer output after standby cancel, change TMDLATCH register from “0” to “1” after 100 µs or more from standby cancel.



Digital thermometer update timing

Other Function

This sensor has the function as below. About detail, refer to each application note.

- Multi Frame Set Output mode (2 / 4 frame)
- Multi Frame ROI mode
- Driving Low Power Consumption at longtime exposure
- Gradation Compression
- Pattern Generator (Refer to Support Package)

Extension Function

Use these functions after enough checks and evaluation.

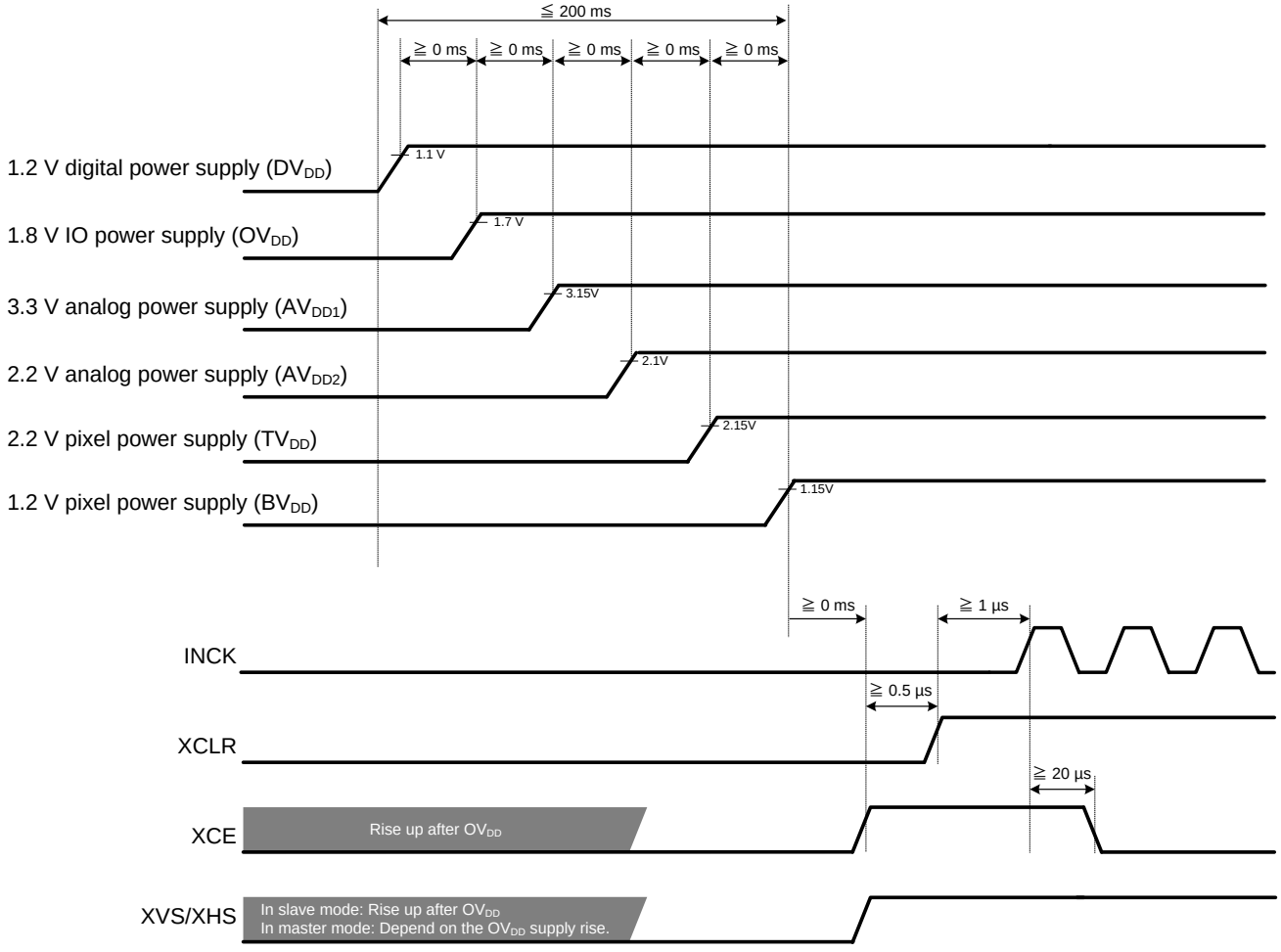
- Black Level Auto Adjust Off

Power-on and Power-off Sequence

Power-on sequence

Follow the sequence below to turn on the power supplies.

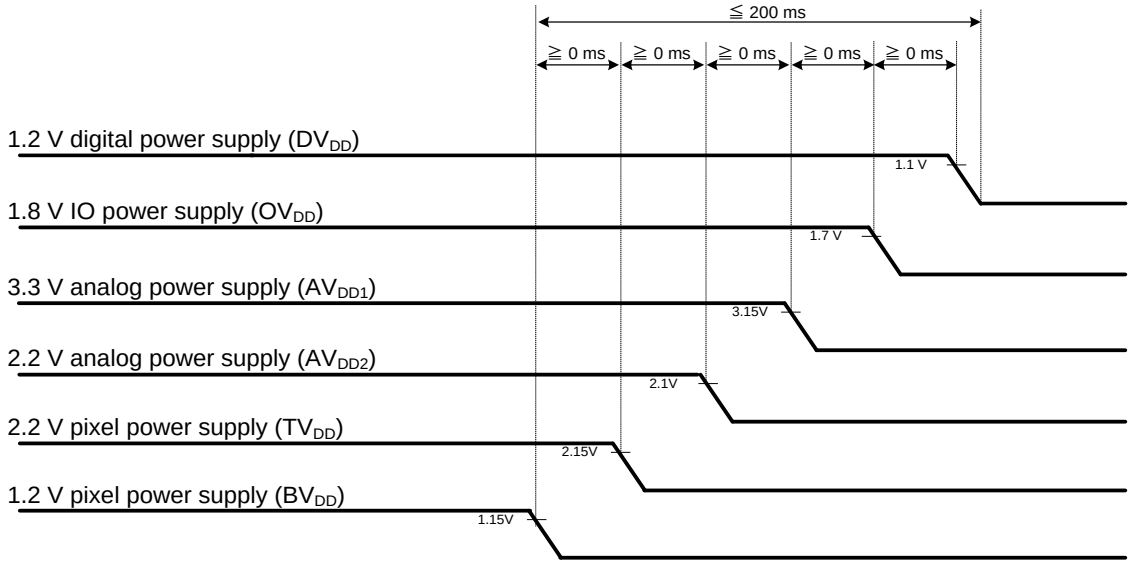
1. Turn On the power supplies so that the power supplies rise in order of 1.2 V digital power supply (DV_{DD}) →1.8 V IO power supply (OV_{DD}) → 3.3 V analog power supply (AV_{DD1}) → 2.2 V analog power supply (AV_{DD2}) → 2.2 V pixel power supply (TV_{DD}) → 1.2 V pixel power supply (BV_{DD}). In addition, all power supplies should finish rising within 200 ms.
   Each digital input terminal (INCK, XCE, SCK, SDI, XCLR, XMASTER, XTRIG, SLAMODE, XVS, and XHS) set 0V or Hi - Z.
2. The register values are undefined immediately after power-on, so the system must be cleared. Hold XCLR at Low level for 500 ns or more after all the power supplies have finished rising. (The register values after a system clear are the default values.)
   In addition, hold XCE to High level during this period. Rise XCE after 1.8 V power supply (OV_{DD}), so hold XCE at High level until INCK is input.
3. Start the input of INCK after turning the level of XCLR into the high.
4. Make the sensor setting by register communication after stabilizing the master clock (INCK).



Power-on Sequence

Power-off Sequence

Turn Off the power supplies so that the power supplies fall in order of 1.2 V pixel power supply (BV_{DD}) → 2.2 V pixel power supply (TV_{DD}) → 2.2 V analog power supply (AV_{DD2}) → 3.3 V analog power supply (AV_{DD1}) → 1.8 V IO power supply (OV_{DD}) → 1.2 V digital power supply (DV_{DD}) . In addition, all power supplies should finish falling within 200 ms.
Set each digital input pin (INCK, XCE, SCK, SDI, XCLR, XMASTER, XTRIG, SLAMODE, XVS, and XHS) to 0 V or high impedance before the 1.8 V power supply (OV_{DD}) falls.

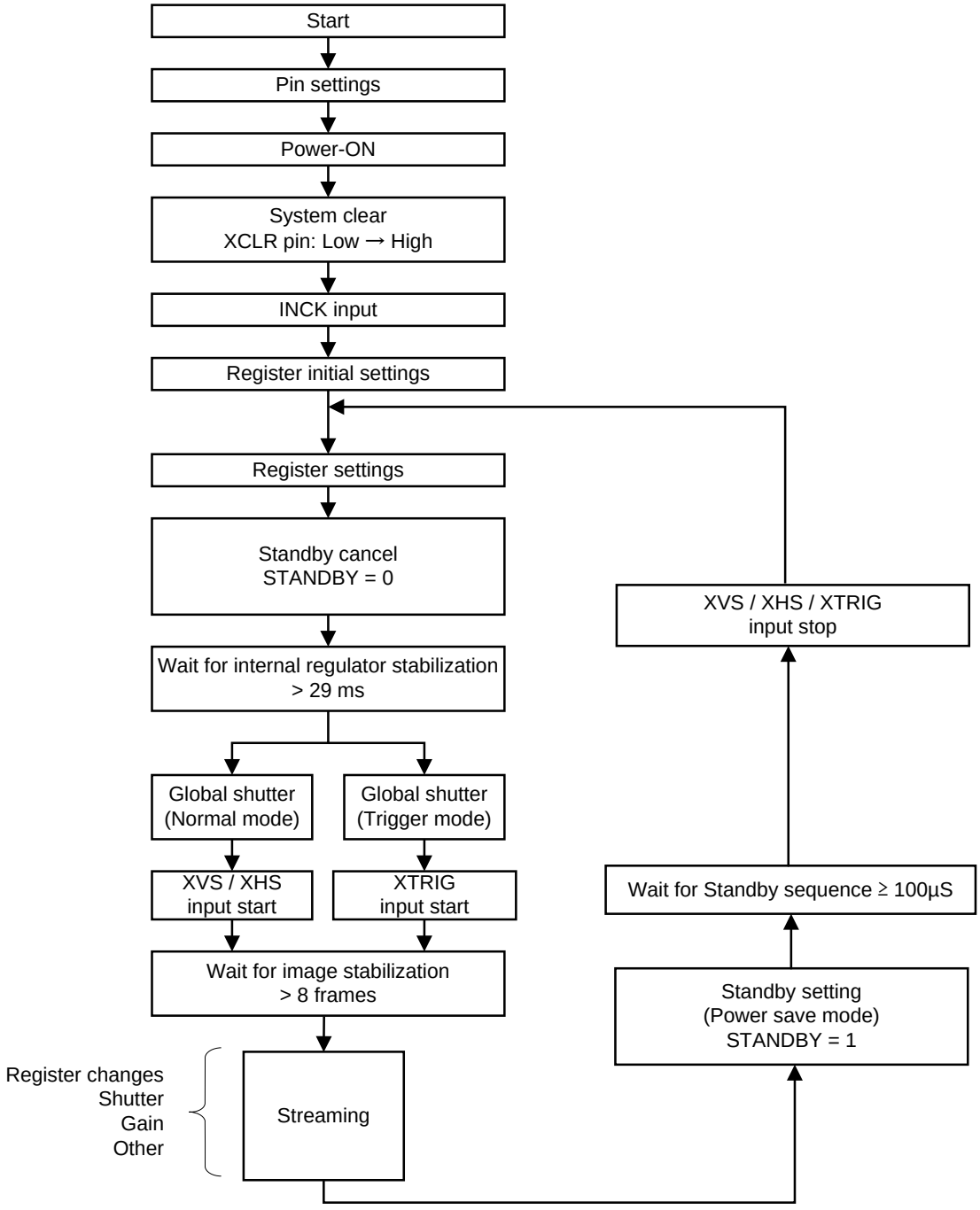


Power-off Sequence

Sensor Setting Flow

Setting Flow in Sensor Slave Mode

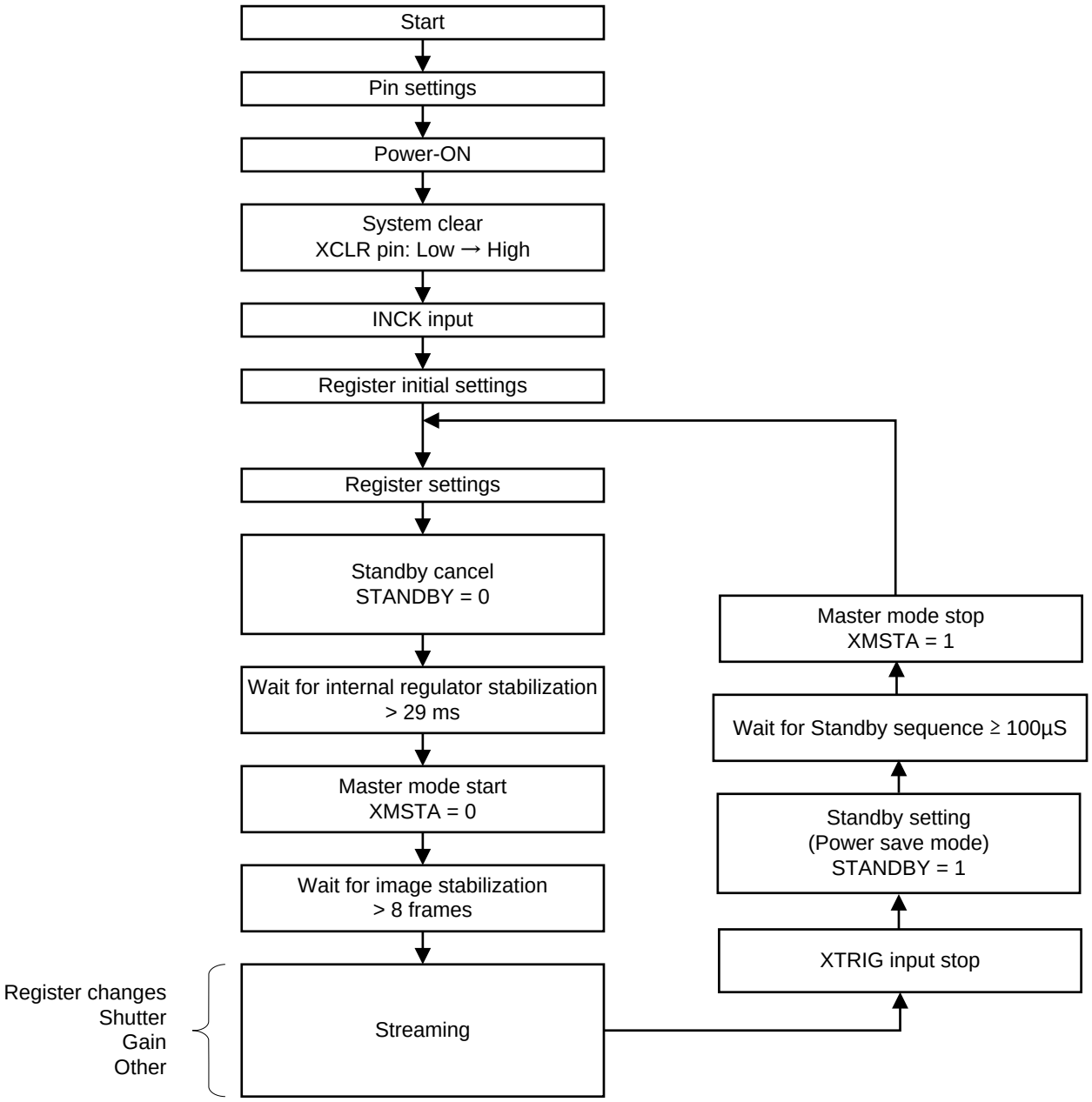
The figure below shows operating flow in sensor slave mode.
For details of "Power on" to "System clear", see the item of "Power on sequence" in this section. For details of "Standby cancel" to "Wait for image stabilization", see the item of "Standby mode". “Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”.



Sensor Setting Flow (Sensor Slave Mode)

Setting Flow in Sensor Master Mode

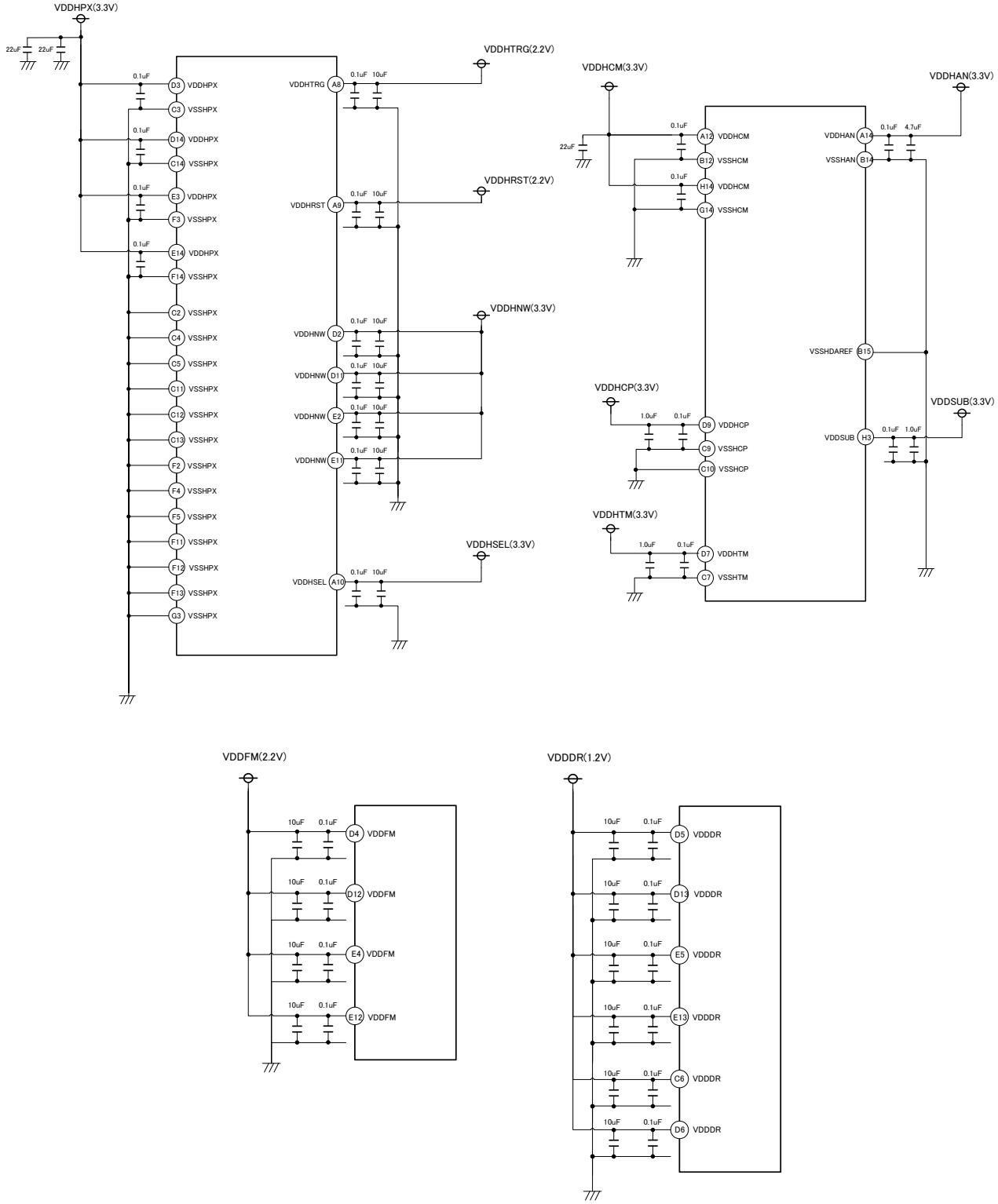
The figure below shows operating flow in sensor master mode.
For details of "Power on" to "System clear", see the item of "Power on sequence" in this section. For details of "Standby cancel" to "Wait for image stabilization", see the item of "Standby mode". In master mode, “Master mode start” by setting the master mode start register XMSTA to “0” after “Wait for internal regulator stabilization”.
“Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”. This time, set "master mode stop" by setting XMSTA to "1".



Sensor Setting Flow (Sensor Master Mode)

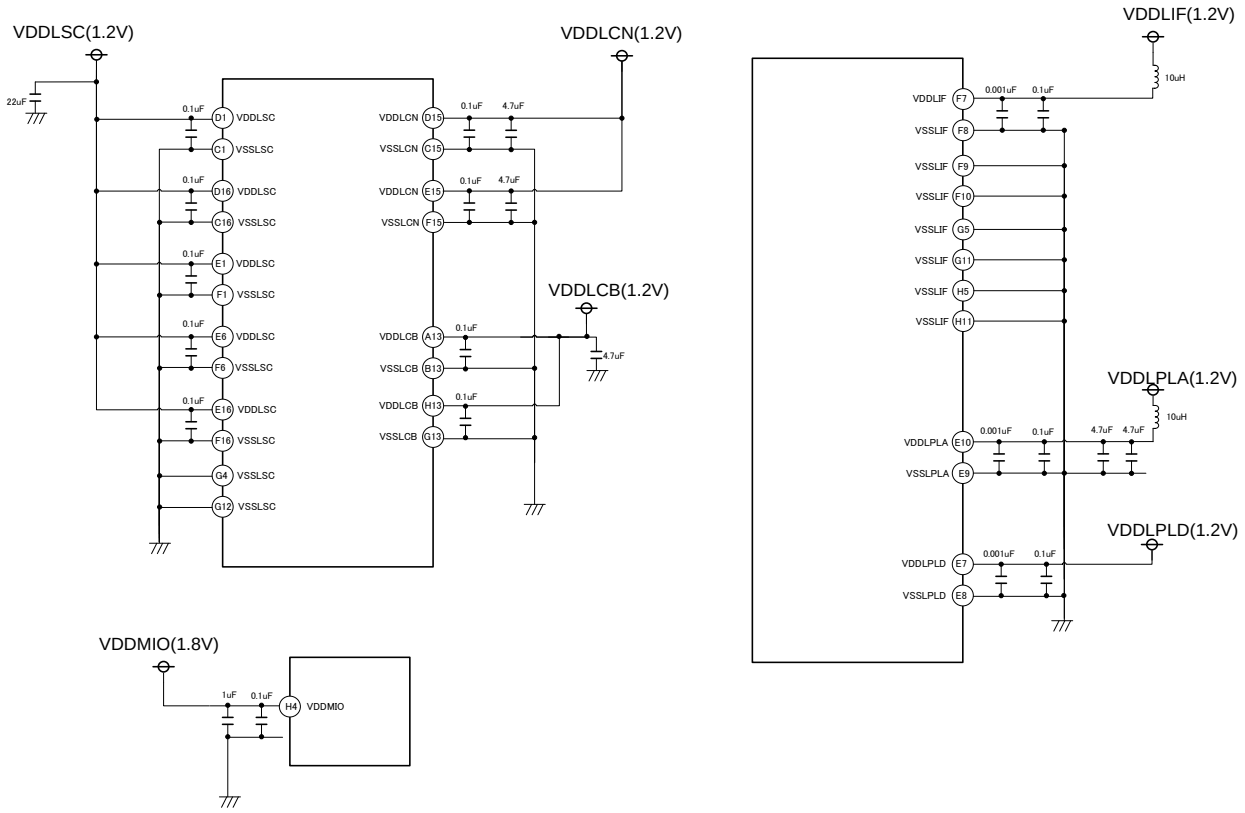
Peripheral Circuit

Analog and Pixel Power Pins



Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

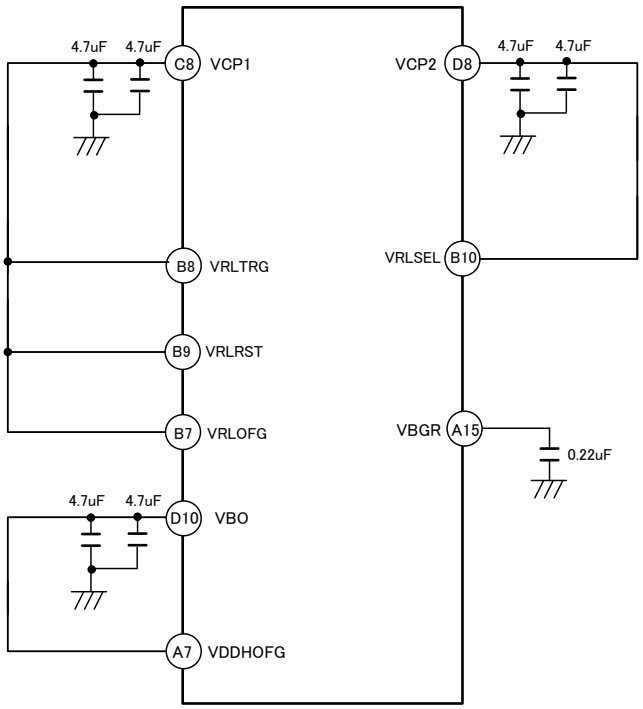
Digital Power Pins



J13 (VDDLCB) are analog power pins, but these pins can be connected to the digital power pins as shown above circuit. These pins can be separated from the digital power pins.

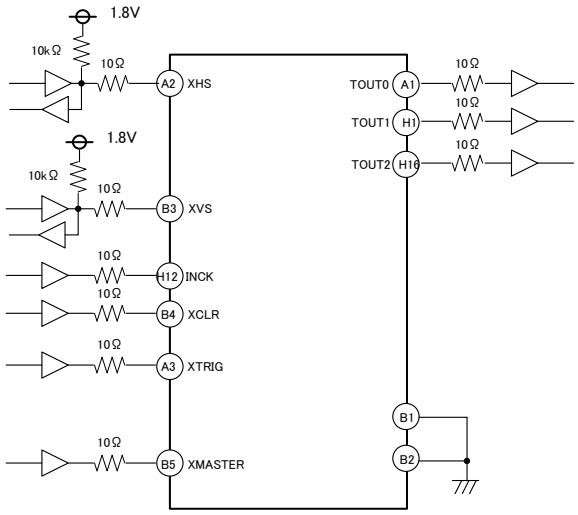
Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

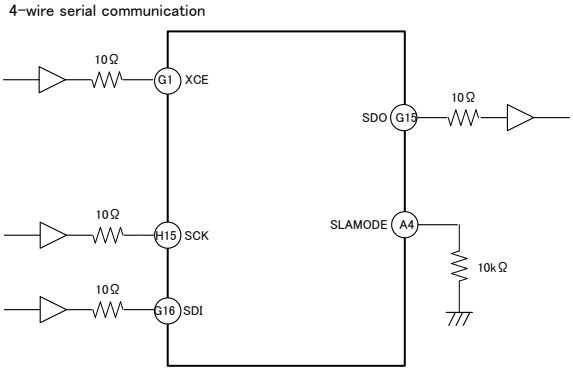
Analog Other Pins

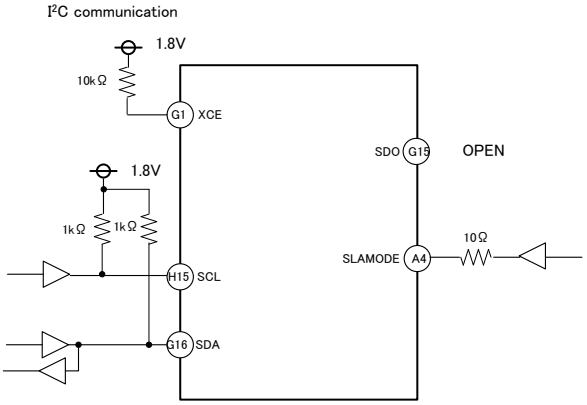


Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

Digital I/O Pins

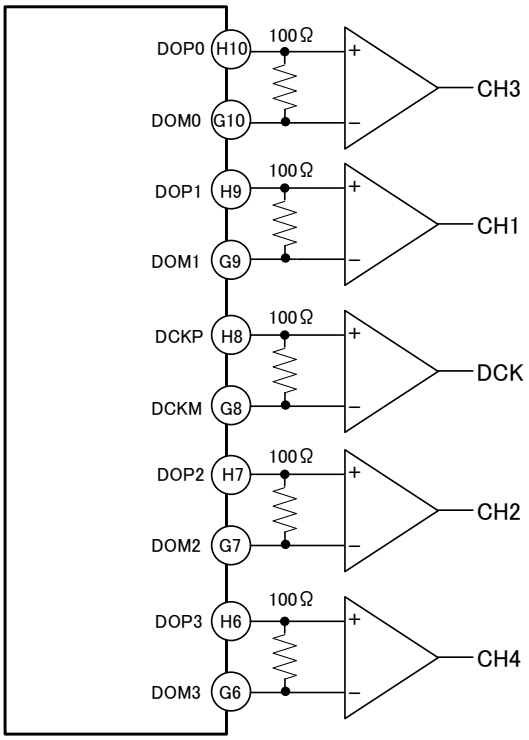






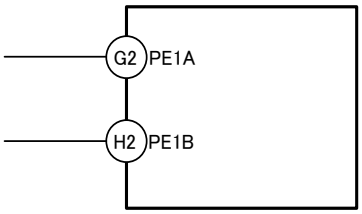
Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

Output pins



Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

Electricthermal cooler pins



Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

Spot Pixel Specifications

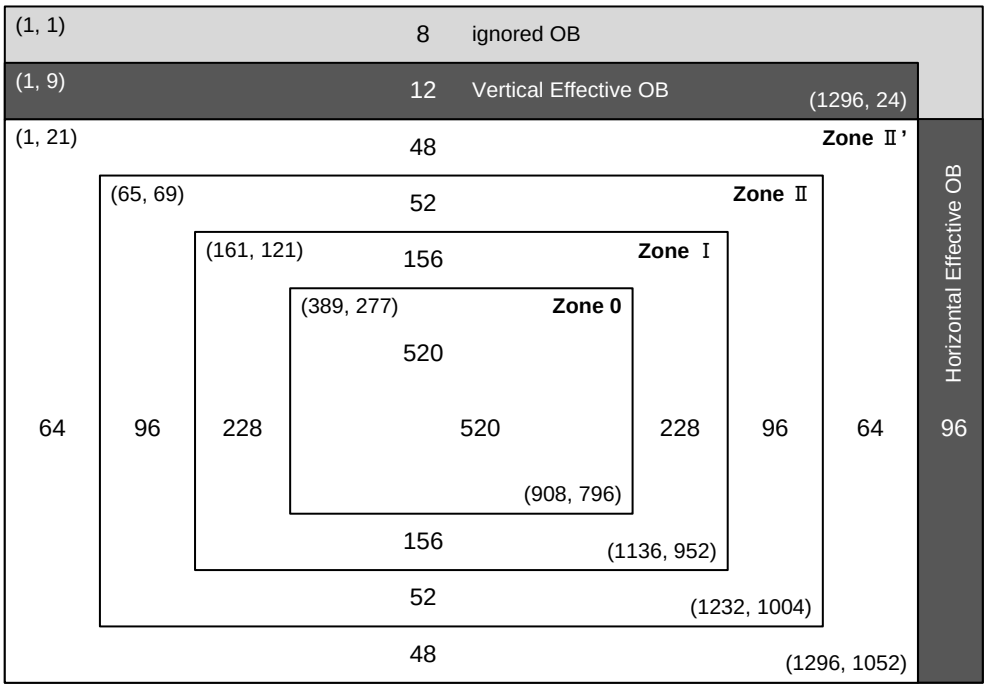
(Tj = 15 ˚C)

Type of distortion	Level	Maximum distorted pixels in each zone			Measurement method	Remarks
		0 to II'	Effective OB	Ineffective OB		
Black and white pixels at high light	30 % ≤ D	A	No evaluation criteria applied		1	
White pixels in the dark	23 mV ≤ D	B		No evaluation criteria applied	2	1/30 s storage
Black pixels at signal saturated	D ≤ 289 mV	C	No evaluation criteria applied		3	

The summation of A, B and C is 6687 or less.

Note) 1. Zone is specified based on all - pixel drive mode
2. D…Spot pixel level
3. See the Spot Pixel Pattern Specifications for the specifications in which pixel and black pixel are close.

Sport Pixel Zone Definition



Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, particle radiation etc. such as cosmic rays may distort pixels of SWIR image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".)
Unfortunately, it is not possible with current scientific technology for SWIR image sensors to prevent such White Pixels. It is recommended that when you use SWIR image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards. Neither Sony Semiconductor Solutions Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

Notice on Spot Pixels Specification

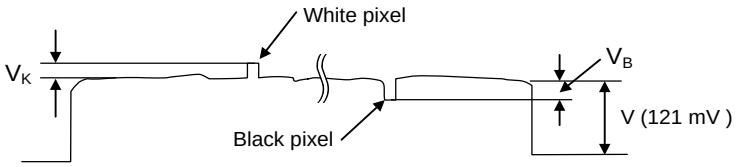
There are some pixels whose output value changes every readout frame under the same condition. It is recommended that you consider taking measures, such as adoption of compensation systems and establishment of quality assurance standards.

Measurement Method for Spot Pixels

The device driver should be set to meet bias and clock voltage conditions. Configure the drive circuit according to the example and measure.

1. Black or white pixels at high light
   Set the measurement condition to the standard imaging condition II. After adjusting the luminous intensity so that the average value V of the signal outputs is 121 mV, measure the local dip point (black pixel at high light, V_B) and peak point (white pixel at high light, V_K) in the signal output V, and substitute the value into the following formula.

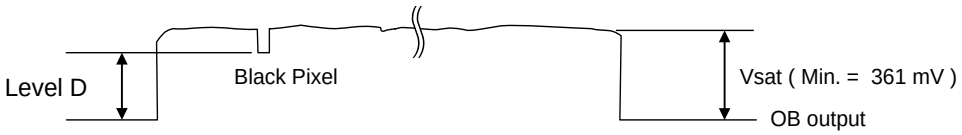
   Spot pixel level D = ((V_B or V_K) / Average value of V) × 100 [%]



Signal output waveform

2. White pixels in the dark
   Set the device to a dark setting and measure the local peak point of the signal output waveform, using the average value of the dark signal output as a reference.

3. Black pixels at signal saturated
   Set the measurement condition to the standard imaging condition II. Set the device to operate in saturation and measure the local dip point, using the OB output as a reference.



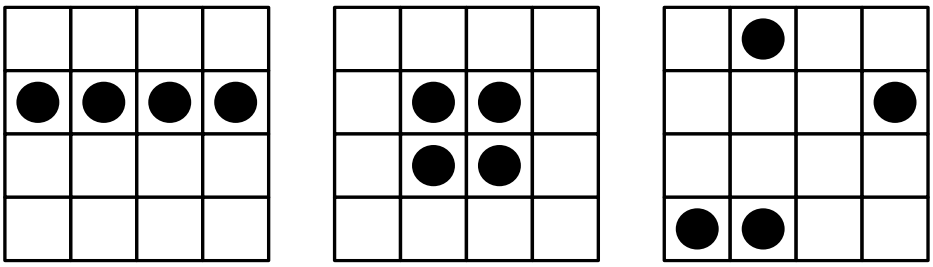
Signal output waveform

Spot Pixel Pattern Specification (Tentative)

The following pattern of White Pixel, Black Pixel and Bright Pixel is rejected.

■ 4 or more White Pixels, Black Pixels, Bright Pixels in a 4 × 4 pixel area

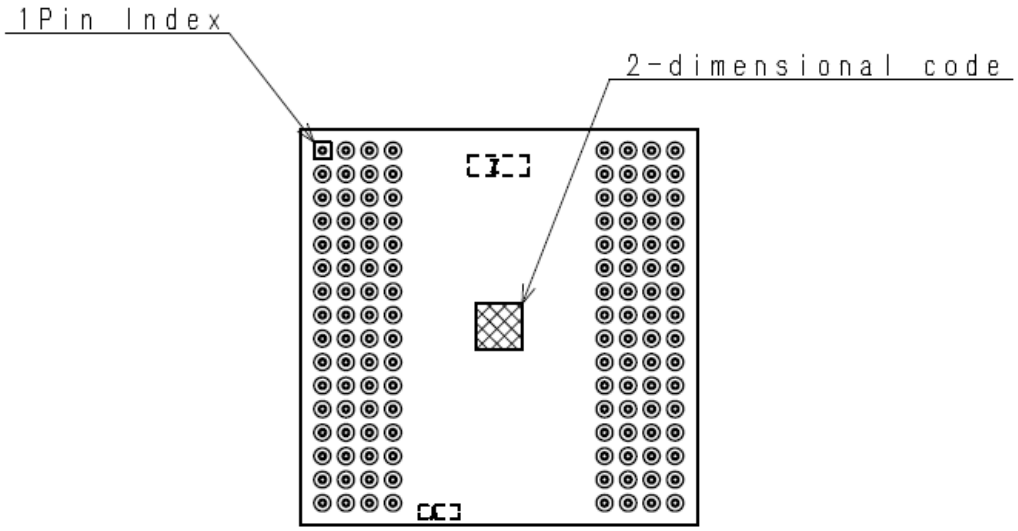
Example)



Note) "● " shows the position of white pixel, black pixel and bright pixel.
White pixel, black pixel and bright pixel are specified separately according the pattern.
(Example: If a black pixel and a white pixel is in the above pattern respectively, they are not judged to be rejected.)

Marking

TENTATIVE



Y part contains 2 alphanumeric characters(No Au coat)
Z part contains 4 alphanumeric characters

Notes On Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Soldering

4.1 Hand solder mounting conditions

(1) Use a 30 W soldering iron with a ground wire and solder each pin in 3 seconds or less.
For repairs and remount, cool sufficiently.
(2) Make sure the iron tip temperature of the solder does not exceed 350 °C.
(3) To dismount an image sensor, do not use solder suction equipment. When using a desoldering tool, use a zero-cross ON/OFF type for the temperature control system and ground the controller.
(4) Carry out evaluation for the solder joint reliability in your company.
(5) Note that condensation on glass or discoloration on resin interfaces may occur if the actual temperature and time exceed the conditions mentioned above or changes rapidly.

4.2 Flow solder mounting conditions

It is recommended to pay attention to the following matter when flow solder mounting. The optimum changes with the solder kind, so set it to usage.

(1) Flow solder work conditions

(a) Assume the solder mounting conditions follow.

Temperature : 245 to 260 °C

Time : 10 s or less

Perform the soldering at the place away from the bottom of the package more than1.0 mm.

(b) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 150 °C.

(c) Perform the flow soldering only one time.

(d) Finish flow soldering within 72 h after unsealing the degassed packing.
Store the products under the condition of temperature of 30 °C or less and humidity of 60 % RH or less after unsealing the package.

(e) Perform re-baking only one time under the condition at 125 °C for 24 h.

(2) Others

(a) Carry out evaluation for the solder joint reliability in your company.

(b) After flow, the paste residue of protective tape sometimes occurs around the seal glass.
(The paste residue of protective tape should be ignored except remarkable one.)

(c) Note that condensation on glass or discoloration on resin interfaces may occur if the actual temperature and time exceed the flow solder mounting conditions mentioned above.

5. Others

(1) Do not expose to strong light (sun rays) for long periods.

(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.

(3) This product is precision optical parts, so care should be taken not to applyexcessive mechanical shocks or force.

(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.

Material_No.26-0.0.1

Built-in thermoelectoric cooler

Please refer to the support package for cooling the image sensor using the built-in thermoelectric cooler.

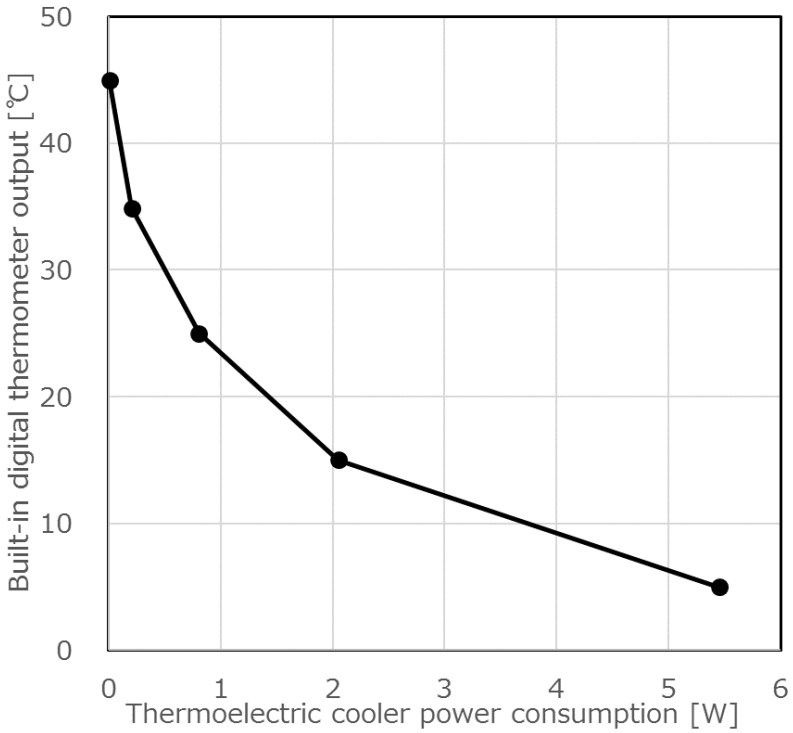
Thermoelectric cooler resistance

Symbol	Item	Min.	Typ.	Max.	Unit	Remarks
Rcooler	Resistance between PE1A - PE1B	3	4	5	Ω	Thermoelectric cooler temperature 25℃*1

[1] Ta=25℃, AC resintance measurement, sensor power off.

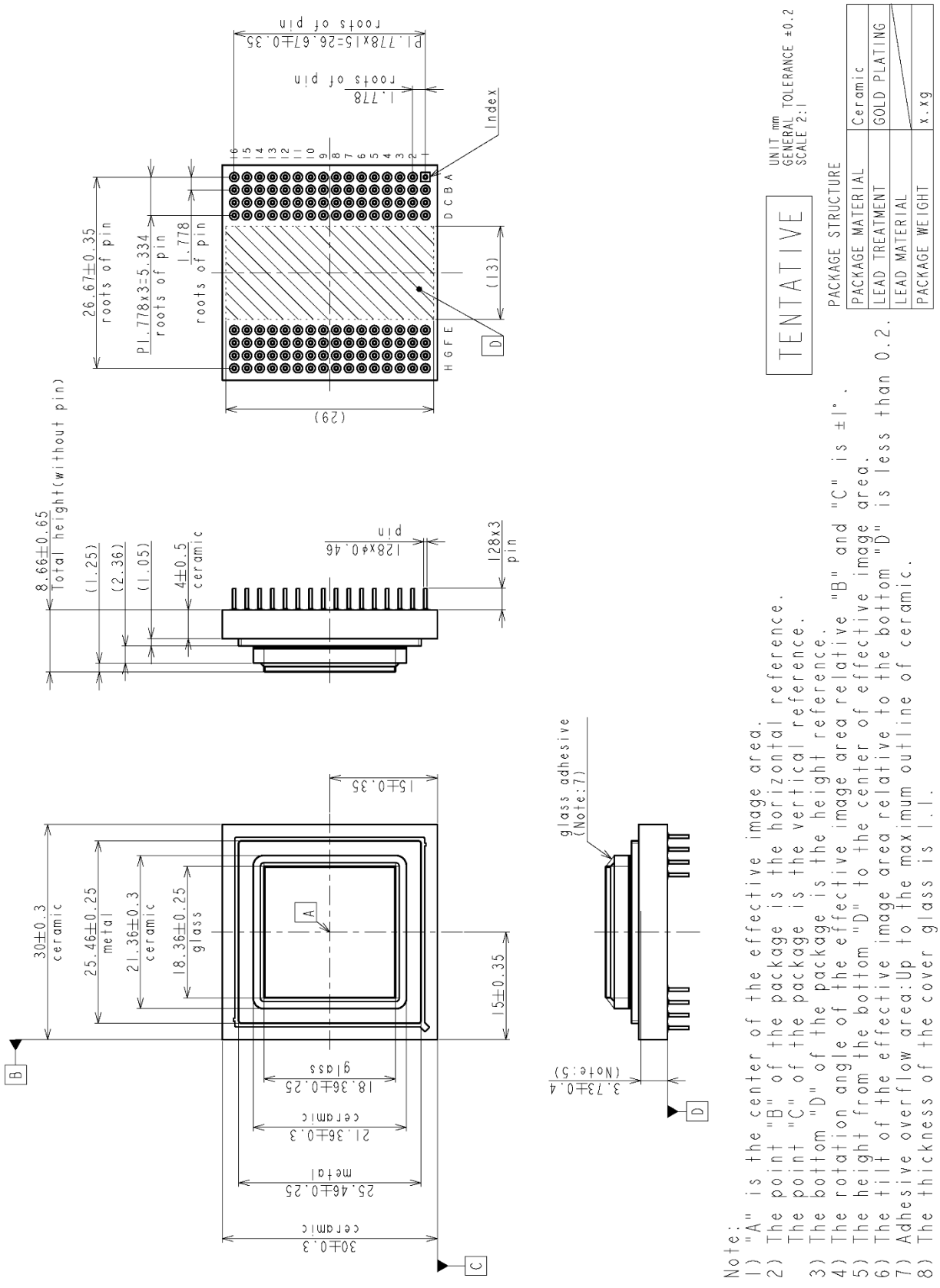
Example of thermoelectric cooler performance

(Typ. Ta = 45℃, Heatsink thermal resistance = 1℃/W)



Package Outline

(Unit: mm)



List of Trademark Logos and Definition Statements

SenSWIR

* SenSWIR is a trademark of Sony Corporation. SenSWIR is a wide-band and high-sensitivity SWIR image sensor technology implemented by the combination of compound semiconductor InGaAs photodiodes and Si readout circuits through Cu-Cu bonding.