Rémi Parrot

Post-doc

Education

2019–2022 **PhD**, *Centrale Nantes (ECN)*, Nantes, *Automatic Generation of VHDL Code for Electric Vehicle Chargers*

2015–2019 **Graduate Engineering School**, *Centrale Nantes (ECN)*, Nantes, *Computer Science and Research*

2013–2015 **Preparatory Classes**, *Lycée Bellevue*, Toulouse, *Physics and Engineering*
Intensive preparation for French Engineering School

2013 **High School Diploma**, *Lycée La Borde Basse*, Castres, *Major in Science*

Languages

French	Native language	
English	Fluent	*(level C1)*
Spanish	Fluent	*(level C1)*

Computing Tools

Languages	C, C++, Python, VHDL	Compilation	GCC, GDB, Xilinx Vivado
Model Checking	Roméo, Uppaal	Compiler	Flex, Bison, Galgas
Versioning	Git	Formatting	LaTeX

Hobbies

Climbing, handwork, juggling, art

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Experience

Nov. 2022– … **Post-doc**, *Uppsala Universitet*, CSD (Computer Science Division), Uppsala–Sweden
Research on stateful fuzzing for communication protocol.

Sep. 2019– Nov. 2022 **PhD Thesis**, *LS2N*, STR (Système Temps Réel), Nantes–France
- — Research on the construction of a pipeline with time and resource constraints, using an approach based on timed Petri Nets ;
- — Implementation of a compilation tool from Simulink to VHDL ;
- — Creation of a VHDL course for master M1 (master CORO at ECN) ;
- — Teaching and supervision of students projects at ECN (master and engineering students).

Apr.–Aug. 2019 **3rd year Internship**, *LS2N*, STR (Système Temps Réel), Nantes–France
Research on the control of formal models with time and cost.

Nov. 2017– Apr. 2018 **Gap year Internship**, *Valwin*, IT service, Nantes–France
Improvement of web site production tools for pharmacies.

Sep.–Oct. 2017 **Gap year formation**, *LS2N*, STR (Système Temps Réel), Nantes–France
Porting of Trampoline RTOS on microcontroller SAM3X8E based on processor ARM Cortex-M3.

Apr.–Aug. 2017 **2nd year Internship**, *Universidad Complutense*, GASS (Grupo de Análisis, Seguridad y Sistemas), Madrid–Spain
Research work of forensic analysis.

Jul.–Aug. 2016 **1st year Internship**, *CCL*, IT service, Castres–France
Web and Software development for a commercial company.

Research projects

Post-doc

title Stateful fuzzing of communication protocols

PI Kostis Sagonas and Bengt Jonsson

description Fuzzing is a testing technique which consists in providing random inputs to the system under test until a bug occurs. Communication protocols have the specificity to (generally) implement state machines. Such state machines can be learned using model learning techniques. Finally, one can guide the fuzzing in order to explore all the states, and thus as many behaviour of the system as possible.

PhD Thesis

title Timed Petri Nets for the synthesis of pipelined circuits

supervisors Olivier H. Roux, Mikaël Briday and Malek Ghanes

description This thesis was part of a collaboration with the automotive company Renault, with the objective of synthesizing resource and time constraint circuits on FPGA. We worked on the synthesis of optimal pipeline and on its usage for time-multiplexing, i.e., the merging of identical circuit portions by sequencing their access. To solve this problem, we reduce it to an optimal reachability problem in a new Timed Petri net model that we introduced, with *delayable* transitions that can miss their firing date and a specific action called *reset* that resets the clocks of all transitions. We studied the expressivity of this model and proposed a symbolic exploration algorithm.

Publications

[1] Rémi Parrot, Hanifa Boucheneb, Mikaël Briday, and Olivier H. Roux. Expressiveness and analysis of Delayable Timed Petri Net. In *16th International Workshop on Discrete Event Systems (WODES'22)*, Prague, Czechia, September 2022. IFAC.

[2] Rémi Parrot, Mikaël Briday, and Olivier H. Roux. Pipeline Optimization using a Cost Extension of Timed Petri Nets. In *The 28th IEEE International Symposium on Computer Arithmetic (ARITH 2021)*. IEEE, June 2021.

[3] Rémi Parrot, Mikaël Briday, and Olivier H Roux. Réseaux de Petri temporisés pour la conception et vérification de circuits pipelinés. In *Modélisation des Systèmes Réactifs (MSR'21)*, Paris, France, November 2021.

[4] Rémi Parrot, Mikaël Briday, and Olivier H. Roux. Timed Petri Nets with Reset for Pipelined Synchronous Circuit Design. In *The 42th International Conference on Application and Theory of Petri Nets and Concurrency (Petri Nets 2021)*, volume 12734 of *Lecture Notes in Computer Science*. Springer, June 2021.

[5] Rémi Parrot, Mikaël Briday, and Olivier H. Roux. Design and verification of pipelined circuits with timed petri nets. *Discrete Event Dynamic Systems*, 33(1) :1–24, dec 2022.

[6] Rémi Parrot and Didier Lime. Backward symbolic optimal reachability in weighted timed automata. In Nathalie Bertrand and Nils Jansen, editors, *18th International Conference on Formal Modeling and Analysis of Timed Systems (FORMATS 2020)*, Lecture Notes in Computer Science, pages 41–57, Vienna, Austria, September 2020. Springer.