Rémi Parrot

PhD student

Education

2013 **High School Diploma**, *Lycée La Borde Basse*, Castres, *Major in Science*

2013–2015 **Preparatory Classes**, *Lycée Bellevue*, Toulouse, *Physics and Engineering*
Intensive preparation for French Engineering School

2015–2019 **Graduate Engineering School**, *Centrale Nantes (ECN)*, Nantes, *Computer Science and Research*

PhD Thesis

title Automatic Generation of VHDL Code for Electric Vehicle Chargers

supervisors Olivier H. Roux, Mikaël Briday and Malek Ghanes

description The objective is to be able to automatically generate a circuit (described in VHDL) performing an algorithm described in Simulink, with an FPGA as target. This circuit must meet time (maximal critical path) and resource (maximal logical units) constraints. The thesis is part of a collaboration with the automotive company Renault.

date 2019–2022

Languages

French Native language

English Fluent *(level C1)*

Spanish Fluent *(level C1)*

Computing Tools

Languages C, C++, Python, VHDL

Model Checking Roméo, Uppaal

Versioning Git

Compilation GCC,GDB,Xilinx Vivado

Compiler Flex, Bison, Galgas

Formatting LaTeX

Hobbies

— Juggling
— Climbing
— Handwork
— Art

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Experience

Jul.–Aug. 2016 **1st year Internship**, *CCL*, IT service, Castres–France
Web and Software development for a commercial company.

Apr.–Aug. 2017 **2nd year Internship**, *Universidad Complutense*, GASS (Grupo de Análisis, Seguridad y Sistemas), Madrid–Spain
Research work of forensic analysis.

Sep.–Oct. 2017 **Gap year formation**, *LS2N*, STR (Système Temps Réel), Nantes–France
Porting of Trampoline RTOS on microcontroller SAM3X8E based on processor ARM Cortex-M3.

Nov. 2017–Apr. 2018 **Gap year Internship**, *Valwin*, IT service, Nantes–France
Improvement of web site production tools for pharmacies.

Apr.–Aug. 2019 **3rd year Internship**, *LS2N*, STR (Système Temps Réel), Nantes–France
Research work on the control of formal models with time and cost.

Sep.2019–... **PhD Thesis**, *LS2N*, STR (Système Temps Réel), Nantes–France
- Research work on the construction of a pipeline with time and resource constraints, using an approach based on timed Petri Nets ;
- Implementation of a compilation tool from Simulink to VHDL ;
- Creation of a VHDL course for master M1 (master CORO at ECN) ;
- Teaching and supervision of students projects at ECN (master and engineering students).

Publications

Rémi Parrot, Mikaël Briday, and Olivier H. Roux. Pipeline Optimization using a Cost Extension of Timed Petri Nets. In *The 28th IEEE International Symposium on Computer Arithmetic (ARITH 2021)*. IEEE, June 2021.

Rémi Parrot, Mikaël Briday, and Olivier H Roux. Réseaux de Petri temporisés pour la conception et vérification de circuits pipelinés. In *Modélisation des Systèmes Réactifs (MSR'21)*, Paris, France, November 2021.

Rémi Parrot, Mikaël Briday, and Olivier H. Roux. Timed Petri Nets with Reset for Pipelined Synchronous Circuit Design. In *The 42th International Conference on Application and Theory of Petri Nets and Concurrency (Petri Nets 2021)*, volume 12734 of *Lecture Notes in Computer Science*. Springer, June 2021.

Rémi Parrot and Didier Lime. Backward symbolic optimal reachability in weighted timed automata. In Nathalie Bertrand and Nils Jansen, editors, *18th International Conference on Formal Modeling and Analysis of Timed Systems (FORMATS 2020)*, Lecture Notes in Computer Science, pages 41–57, Vienna, Austria, September 2020. Springer.