ECE4700J Computer Architecture

Summer 2022

HW #1

Due: **2:59am (Beijing Time) June 6th, 2022**

*Please Submit a single **PDF** file on Canvas*

Q1 (10%): Please read the Turing lecture "A New Golden Age for Computer Architecture" offered by Prof. David Patterson and Prof. John Hennessy, and summarize **on your own words** at least **three** aspects about why it is "a golden age for computer architecture".

Q2 (5%): Please list at least **two** reasons why CISC can be better over RISC.

Q3 (20%): Assume the CPI of a processor is as follows:

- Loads = 6
- Stores = 5
- ALU operations = 4
- Conditional branches = 4
- Unconditional branches = 3

Architects are considering one of two enhancements. First, they are considering improving all ALU operations to be reduced to 3. Second, they are considering reducing all branches (conditional and unconditional) to 2. Using the **sjeng** benchmark from the table below, compute the average CPI before the enhancement and then with each enhancement and compute each enhancement's speedup over the original. The speedup is old CPI / new CPI. Redo this with the **mcf** benchmark. Compare the speedups between the two benchmarks and offer a suggestion of which speedup might be preferred.

Program	Loads	Stores	Branches	Jumps	ALU operations
astar	28%	6%	18%	2%	46%
bzip	20%	7%	11%	1%	54%
gcc	17%	23%	20%	4%	36%
gobmk	21%	12%	14%	2%	50%
h264ref	33%	14%	5%	2%	45%
hmmer	28%	9%	17%	0%	46%
libquantum	16%	6%	29%	0%	48%
mcf	35%	11%	24%	1%	29%
omnetpp	23%	15%	17%	7%	31%
perlbench	25%	14%	15%	7%	39%
sjeng	19%	7%	15%	3%	56%
xalancbmk	30%	8%	27%	3%	31%

Q4 (10%): Assume a new execution mode called "enhanced mode" provides a 2.5x speedup to the sections of programs where it applies. What percentage of a program (measured by original execution time) must run in enhanced mode for an overall speedup of 10%?

Q5 (15%): Suppose a processor uses 105W of power while operating at 2.7 GHz, of which 3/4 is dynamic power. Suppose we want to run the same processor at a higher frequency which requires increasing the operating voltage proportionally as well.

1) (10%) What is the Power delay product? What is the Energy delay product? What is the Energy-delay^2 product?
2) (10%) If a dynamic power consumption increase of up to 130W can be tolerated, by how much can the processor frequency be sped up?

Q6 (5%): Consider a 2.4 cm^2 die for a 64-bit processor manufactured from a 42 cm-diameter wafer costing $9,000. Assume a wafer yield of 99%. Use the defect model from the lecture notes with 0.016 defects per cm^2 and α=10. What is the expected cost per die (before testing)? Ignore edge effect correction.

Q7 (10%): Consider a single-cycle datapath as a one-stage pipeline which runs at a frequency of 700MHz, if you want to break it into a S-stage pipeline. Assume that the clock overhead is 500ps, the probability of break b due to code delay is 0.2. If we assume that 5% of the additional cycle is used to address the quantization errors and other non-ideal effects. What would be the optimal number of stages for this pipeline? What is the new clock frequency? What is the throughput under this condition?

Q8 (15%): Identify all data dependencies (potential data hazards) in the given code snippet. Assume the loop takes exactly one iteration to complete. Specify if the data dependence is RAW, WAW or WAR.

loop:

1. *ADDI R2, R2, #1*
2. *LD R4, 0(R3)*
3. *LD R5, 4(R3)*
4. *ADD R6, R4, R5*
5. *MUL R4, R6, R7*
6. *SUBI R3, R3, #8*
7. *BNEZ R2, loop*
8. *ADD R11, R12, R13*

Please answer in the following format.

Example:
1) 1 → 2 (RAW)

Q9 (10%): The design of RISC-V provides for 32 general-purpose registers and 32 floating-point registers. If registers are good, are more registers better? List and discuss as many trade-offs (**at least 3**) as you can that should be considered by instruction set architecture designers examining whether to, and how much to, increase the number of RISC-V registers.