VE470/ECE4700J Computer Architecture

Summer 2022

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Course website (Canvas): https://umjicanvas.com/courses/2578/
Course schedule: Lectures **MON**, **WED** 14:00-15:40 (**Beijing** Time); Labs TBD
Teaching mode (Lectures & Labs): Online (**Feishu ID: 613380151**); Labs (Feishu ID: TBD)
Office hours: TBD
TA: NA
Recitation: End of semester (last lecture)
Feishu group: https://applink.feishu.cn/client/chat/chatter/add_by_link?link_token=857iff06-f36d-4149-9ce7-04639fc6962f
Piazza group: piazza.com/sjtu.org/summer2022/ece4700j

Course Description:
This course serves as an alternative to VE450, and can be enrolled as a capstone (so-called MDE) course. Otherwise, it will be counted as an upper level elective course. The course is intended to offer students a solid and deep understanding of how modern computers are designed along with numerous tradeoffs in implementations, including the CPU, memory and their interactions, multi-threading and parallel computing. It will provide students opportunities to gain hands-on experiences of using popular computer architecture simulators (e.g. Gem5) and design frameworks (e.g. Chisel or HLS). Emerging architectures such as domain specific architectures (DSA), Process-in-Memory (PIM) or AI accelerators will also be introduced in the end.

Credits: 4
Prerequisite: VE370 & VE280
Textbooks:

- Computer Architecture: A Quantitative Approach, by John L. Hennessy and David A. Patterson, published by Morgan-Kaufmann publishers, November 2017. ISBN: 9780128119051.

References:

- John L K, Narayanan V. Microprocessor at 50: A Time to Celebrate and Energize for the Future[J]. IEEE Micro, 2021, 41(06): 10-12. (Available on Canvas)
- Reading material will also be available on the canvas course website time to time.

Course Objectives (what will be taught):

- To teach students fundamental design tradeoffs of the modern computer architectures;
- To teach advanced computer architecture concepts such as Multiprocessors, Superscalar, GPUs and advanced caches;
- To give students an exposure to state-of-the-art computer architecture simulators through hands-on assignments and/or a project that will help understand the tradeoffs;
- To offer student hands-on experiences of implementing or optimizing major portions of a substantial processor with either Verilog or High-level design approaches;

- To introduce students the most recent computer architecture advances such as Domain specific architectures (DSA) and AI accelerators;
- To provide experiences of executing a project as a team from concept to finish effectively and professionally, and to offer opportunities to present ideas to the public.

Course Outcomes (what students are expected to achieve):

- Understand fundamentals of designing a modern processor and the key metrics;
- Gain fundamental knowledge and understandings of advanced computer architectures such as multiprocessors, superscalars, advanced caches, and prefetching schemes;
- Learn about state-of-the-art computer architecture simulators or frameworks;
- Develop understandings about certain design tradeoffs in implementing the modern computer architectures;
- Learn about the concept of high-level design languages, AI accelerators or domain-specific architectures;
- Work as a team to implement and optimize a given functional description of a major portion of a substantial processor with learned knowledge and tools;
- Be able to present the results and conclusions of an experimental project in a clear, logical, succinct, and informative written format.

Course Outline: (Note: Tentative and subject to adjustment, please always go to canvas syllabus for the latest information.)

Week	Lec #	Date	Topics	Readings	Assignments
1	1	5/9	Course introduction, Intro. to Computer Architecture I	Syllabus, Slides, Reading Materials on Canvas	Course Survey
	2	5/11	Intro. to Computer Architecture, Fundamentals of Quantitative Analysis		
2	3	5/16	Fundamentals of Quantitative Analysis		
	4	5/18	Fundamental Processors I		
3	5	5/23	Fundamental Processors II		
	6	5/25	Fundamental Memories I		
4	7	5/30	Fundamental Memories II		
	8	6/1	Architectural Simulation and Implementation I		
5	9	6/6	Architectural Simulation and Implementation II		
	10	6/8	Advanced Processors I		
6	11	6/13	Advanced Processors II		
	12	6/15	Advanced Processors III		

7	13	6/20	Advanced Memories I		
	14	6/22	Advanced Memories II		
8	15	6/27	Advanced Memories III		
	16	6/29	Domain-Specific Architectures I		
9	17	7/4	Domain-Specific Architectures II		
	18	7/6	FPGAs and Reconfigurable Computing		
10	19	7/11	Warehouse-Scale Computing		
	20	7/13	Intro. to Process-in-Memory		
11	21	7/18	Intro. to AI Hardware		
	22	7/20	2017 Turing Award Lecture/Advanced Packaging		
12	23	7/25	Literature Review Presentation/Project Presentation		
	24	7/27	Course Review (RC)		
13	-	8/3	Capstone Defense & Design Expo		
	-	TBD	Final Exam		

Lab Schedule: (TBD)

Course Policies:

- Honor Code: All students in the class are bound by the Honor Code of the Joint Institute (https://www.ji.sjtu.edu.cn/academics/academic-integrity/honor-code/) ***as well as the Addendum to the Honor Code for Online Teaching***. You may not seek to gain an unfair advantage over your fellow students; you may not consult, look at, or possess the unpublished work of another without their permission; and you must appropriately acknowledge your use of another's work.
- Test: Test procedure will be announced prior to the tests. Anyone violating the test procedure will be given an 'F' for the test.
- Attendance: Attendance to the lectures is strongly encouraged, not only because difficult concepts are discussed during the lectures, but also because it is an effective way to get engaged in class activities.
- Participation: Active participation is highly expected for all students. This involves participation in interactive activities during the lecture time, proper assistance to other students in group studying, contributions to the Q&A on Piazza/Feishu, etc.
- Individual Assignments: Project 1, part of Project 2, paper review assignments, and homework assignments are individual assignments. Students are encouraged to discuss course topics and help each other understand the project/homework requirements better. However, all submissions must represent your own work. Duplicated submission is absolutely not allowed and will trigger an honor code violation investigation.
- Group Assignments: Part of Project 2 and Project 3 are team efforts. The work submitted must reflect the work of the team. The grade for a group assignment will be shared among the entire team equally, unless specified differently.

- Submission: All assignments should be submitted electronically on Canvas before the specific deadline. The instructor reserves the right to waive the penalty for emergencies (e.g. hospitalization) or arrangement made with the instructor **24 hours** prior to the due date.

Addendum to the Honor Code for Online Teaching

- **The Honor Code in the Context of Online Courses**

The JI Honor Code applies to courses taught in an online fashion in the same way that it does to all courses. It is worth repeating the central tenets here:

- Engineers must possess personal integrity as students and as professionals. They must honorably ensure safety, health, fairness, and the proper use of available resources in their undertakings.
- Members of JI are honorable and trustworthy persons.
- The students, faculty members, and staff members of JI trust each other to uphold the principles of the Honor Code. They are jointly responsible for precautions against violations of its policies.
- It is dishonorable for students to receive credit for work that is not the result of their own efforts.

In particular, the parts of the Honor Code regarding conduct during in-class examinations, for coursework, projects etc. apply correspondingly for such work conducted in courses taught online. Additional rules adapted to remote examinations, coursework etc. may be imposed as necessary.

In addition, students are required to abide by following rules specific to online teaching. These requirements are provisionally considered part of the Honor Code for the current teaching term.

Due to the new types of interaction and the new forms of learning activities there may be further issues that are not covered below. Students should not hesitate to contact their instructor, the Honor Council (jihonor@sjtu.edu.cn) or the FCD (jifcd@sjtu.edu.cn) if they have any questions.

- **Online Presence and Activities**

The Joint Institute imposes a “real name” policy for all online activities organized by JI instructors. This policy applies to groups or communication by E-Mail, Canvas, Piazza, Feishu, WeChat and all other platforms where groups are set up by JI or by individual instructors for students attending JI courses, events or other activities.

Students are required to use their actual name (in Pinyin) as part of their online presence for such groups and when communicating online. Individual instructors may also require students to add their name in Chinese characters (if applicable) and/or their Student ID.

Unless otherwise noted, such online activities are intended for the exclusive participation of JI students. Account names, meeting IDs, passwords and other information intended to protect the exclusivity of such activities may not be shared with anyone who is not part of the course or activity.

For example, it is not permissible to give a Feishu meeting ID of a given course to any person who is not enrolled in

that course, whether or not the person is a JI student.

- **Online Etiquette**

When communicating or otherwise using online groups, students should follow the regulations set down by instructors concerning the use of online tools. Vandalism, spam messages, verbal and other forms of abuse, violation of English-only policies (as detailed by instructors) and disturbance of the learning experience of other students are not permitted.

- **Teaching and Learning Materials**

Teaching and learning materials, such as lecture slides, assignments, quizzes, videos etc. are copyrighted and may not be passed on to others without the express permission of the course instructor. This applies in particular to recordings of Feishu lectures and other videos created by instructors.

In particular, it is not permissible to upload videos to sharing platforms (such as Youku or YouTube) or to post lecture slides, assignment questions, project descriptions etc. on public sites such as SlideShare.

Course Assessment Methods:

- **Homework:**

Homework problems are designed for students to revisit and practice the important concepts in computer organization and design. Homework assignments are also assigned for students to gain confidence in solving engineering problems in this class.

- **Literature search & review project:**

The ability to search and find literatures relevant to a specific topic is important for conducting research, resolving real-life engineering problems, and continuing one's intellectual growth in the life time. The project for literature search & review is designed for the students to get familiarized with the resources available in a college library physically and online virtually, and to learn tools that may facilitate the searching process. It is also designed to develop students' presentation skills and critical thinking process.

- **Examination:**

The examinations shall measure the ability to carry out analysis, design, and verification processes of digital circuits and systems. There will be two online or paper-based examinations. The typical types of exam problems include conceptual understanding, computation, procedural development, short answer, analysis and design, and etc.

- **Labs & Projects:**

The labs and projects are designed for students to practice the important concepts discussed in the lectures on a system level and to have a better understanding of the concepts and techniques with hands-on experience. The design

projects utilize contemporary software tools in aid of design. Documented design outcomes and/or demonstration of the labs/projects will be required.

- **Participation and Etiquette:**

Students are encouraged to actively participate in all kinds of classroom activities including, but not limited to, classroom interaction with the instructor and other students, effective contribution on Piazza/Feishu, active participation in team-based projects. In course related activities, students should follow the regulations set down by instructors concerning the use of online tools. *Vandalism, spam messages, verbal and other forms of abuse, violation of English-only policies and disturbance of the learning experience of other students are not permitted. Inappropriate behavior will result in deduction of points in this part of course evaluation.*

Grading Policy

Participation & Etiquette*	5%
Homework	10%
Labs	30%
Literature review/presentation assignment	5%
Final Project & Report	30%
Final Exam	20%
Total	**100%**

Notes:

- *This includes class/lab participation, piazza questions and answers, RC (2-hour requirement), etc.
- Creative ideas in projects or homework will get bonus.
- Final letter grades might be curved, but are not guaranteed.