ECE4700J Homework 2

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Q1

1. There is a RAW hazard on `x1`.

   7 cycles will be taken.

2. Still 7 cycles is needed, since it takes time to read memory and ALU cannot wait until memory access is done if they are executed at the same time. If such forwarding path is added, it will potentially lead to wrong ALU output since the signal is changed asynchronously.

Q2

1. $CPI = 1 + 25\% \times (1 - 45\%) \times 2 = 1.275$
2. $CPI = 1 + 25\% \times (1 - 55\%) \times 2 = 1.225$
3. $CPI = 1 + 25\% \times (1 - 85\%) \times 2 = 1.075$
4. $CPI = 1 + 12.5\% \times (1 - 85\%) \times 2 = 1.0375$

   Speedup by $1.1125/1.05625 = 1.036$.

5. Suppose the rest accuracy is x, then $(80\% + 20\%x)/100\% = 85\%$ yields $x = 25\%$.

Q3

Pipelining separates an instruction in several stages and execute one stage at a time, while superpipelining simply further divides each stage into sub-stages to reduce clock periods. Superscalar executes multiple instructions in a pipeline at the same time, which is instruction level parallelism.

Q4

```
addi x11, x12, 5
nop
nop
add  x13, x11, x12
addi x14, x11, 15
nop
add  x15, x13, x12
```

Q5

1. A structural hazard happens when instruction fetch and data memory access try to run at the same time. The above code will have to stall for two cycles at `beqz x17, label` when the first two instructions are using data memory.

```
sd   x29, 12(x16)   IF ID EX ME WB
ld   x29, 8(x16)       IF ID EX ME WB
sub  x17, x15, x14        IF ID EX ME WB
beqz x17, label              ** ** IF ID EX ME WB
add  x15, x11, x14                    IF ID EX ME WB
sub  x15, x30, x14                       IF ID EX ME WB
```

2. It is not possible to reduce stalls simply by reordering, since every line of code needs to fetch the instruction, then as long as there is a data memory access, the pipeline has to be stalled.