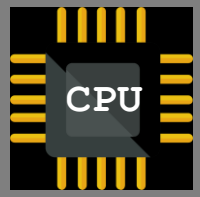


Topic 0

Course Introduction

Xinfei Guo
xinfei.guo@sjtu.edu.cn

May 9th, 2022

Greetings from Shanghai

Photo Credit: https://www.chinadaily.com.cn/a/201911/26/WS5ddc8d78a310cf3e3557a072.html

VE470 in one sentence…

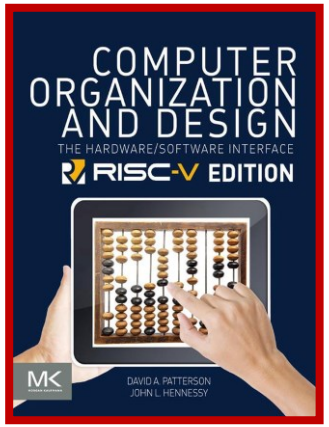
NEW COURSE

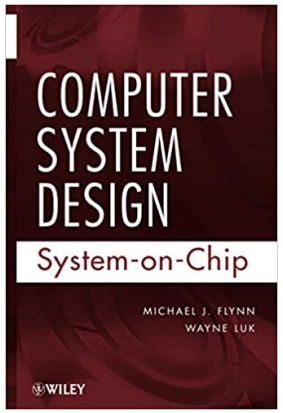
This is a newly offered four-level *Major Design Experience* (MDE) or *Upper Level Elective* Computer Engineering course, covering advanced concepts and practical approaches of architecting a computer (mainly processors).

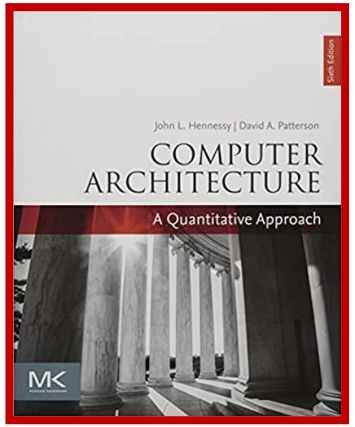
Image: https://nordicdairycongress.com/nyheder/welcome-nordicdairycongresscom#.YnEe5dpBxD8

Who I am?

- Assistant Professor @ JI since May 2021
- Computer Engineering Ph.D. (Virginia), M.S (Florida)
- Worked @ NVIDIA, IBM Research in US
- An enthusiastic computer hardware researcher
  - Circuit/Architecture/System
- Taught VE370 Intro. to Computer Organization (21SU), VE481 SoC Design (21FA) , VE470 Computer Architecture (22SU)
- Website: https://sites.ji.sjtu.edu.cn/xinfei-guo/



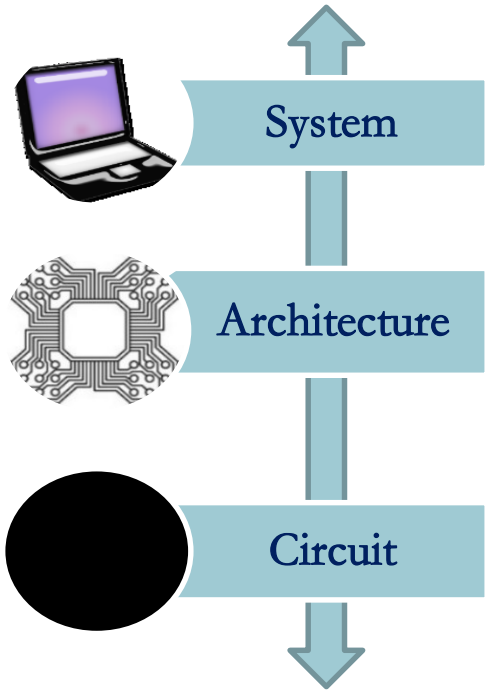




My research @ JI

Intelligent Circuits, Architectures, and Systems (iCAS)

上海交通大学密西根学院 智能电路、架构和系统实验室



EDA/Design Methodology

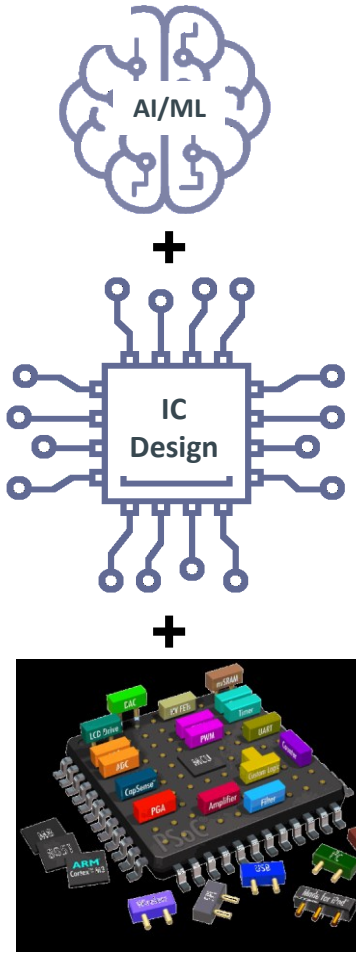
- AI/Machine learning-enabled chip design automation
- Open-source EDA
- Cross-layer Codesign

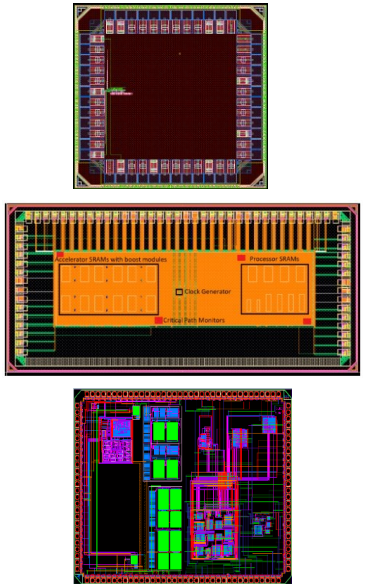
New Architectures/Platforms

- FPGA acceleration
- Crypto architecture
- RISC-V Extension

Chip Design

- Energy efficient & Reliable chip design
- Aging-aware Design
- Ultra low power IoT systems





https://sites.ji.sjtu.edu.cn/icas

Image: https://www.cleanpng.com/png-introduction-can-stock-photo-clip-art-cliparts-pro-924166/

Logistics

- Instructor: Xinfei Guo, Ph.D.
- Office: JI Building Rm 419
- Email: xinfei.guo@sjtu.edu.cn
- Phone: +86-21-3420-6045 Ext. 4191
- Course website: https://umjicanvas.com/courses/2347
- Course schedule: Lectures MON, WED **14:00-15:40 (Beijing Time)**; Labs TBD
- Teaching mode: Online (**Feishu ID: 613380151**); Labs Online (ID TBD)
- Office Hours: **TBD**
- RC: **4hrs (TBD)**
- Slides/handouts will be provided before the class most of the time (several might be not, this will be done **on purpose** or will be revised after the lecture)
- Reading materials will be assigned

Online Teaching

- Everything will be online (until further notification), including homework, labs, projects, presentations, OH and final exams.
- Please try to attend live lectures (if your time zone allows).
- The lectures will be recorded, and will be posted on canvas immediately after each lecture.
- There will be a 5-min break during the lecture (**14:45 – 14:50**).
- Please turn on your camera if condition allows.
- There can be internet issues, I will try my best to recover.
- Feel free to interrupt me anytime (you can also type in chat window).
- The best way to ask questions (either to the instructor or the TA) after lectures will be through **Piazza**, **Feishu course group** or **during OH**.

Who is TA?

- Mr. Haoyang Zhang (张浩洋)
- Senior Student (in CE) at UM & JI
- Incoming PhD student at UIUC
- Took 470 at UM
- Research Interests: Computer Architecture and System Software
- https://hieronzhang.github.io/
- Time zone: EDT (12hour difference)
- Email: zhy-sjtu-jc@sjtu.edu.cn
- TA Office Hours: TBD

Feishu Group

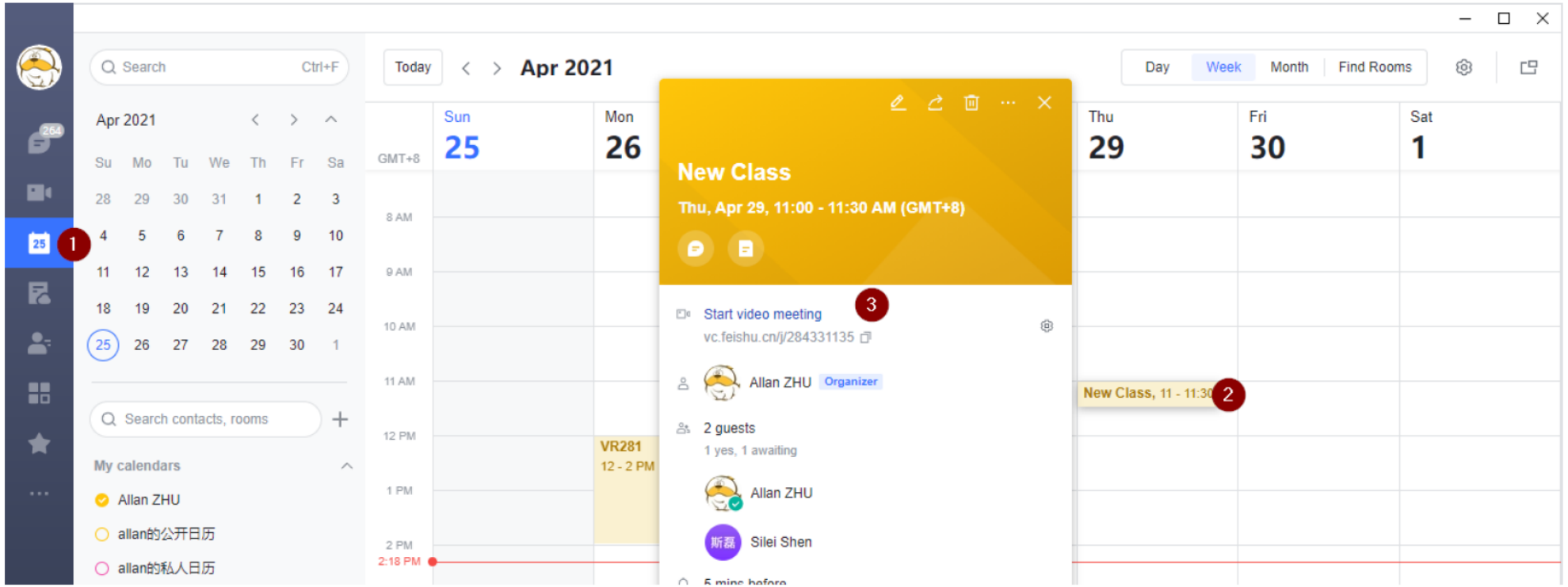
- For urgent matters, course announcements, logistics, etc. Please join asap!

Xinfei Guo invited you to a group on Feishu, click https://applink.feishu.cn/client/chat/chatter/add_by_link?link_token=857iff06-f36d-4149-9ce7-04639fc6962f to join！

Join class virtually (recordings available)

1.1 Join meeting from Calendar

(1) Switch calendar tab (2) Open meeting event (3) Click "Join video meeting"



s://sjtu.feishu.cn/docs/doccn9iBVyl6dFzpEU3WazFWtIg 12/1

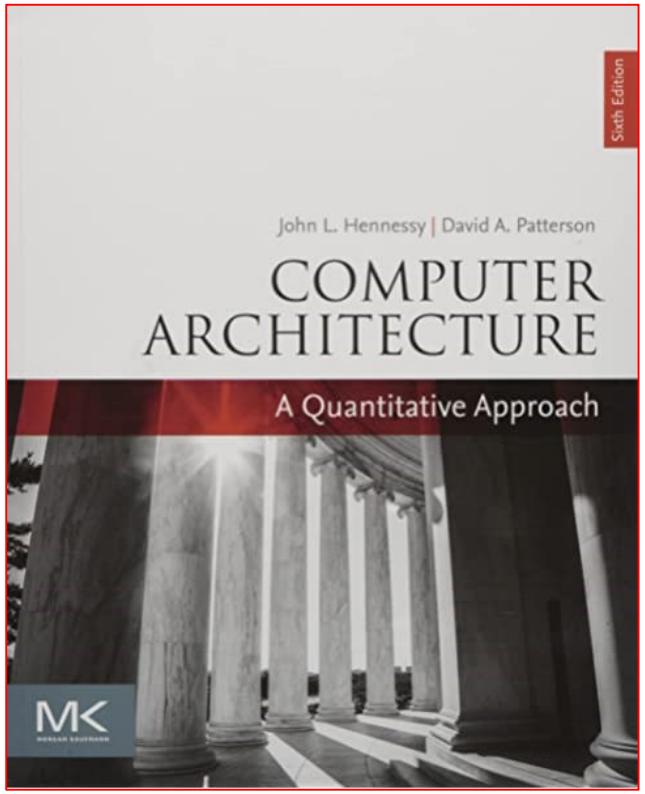
Piazza group

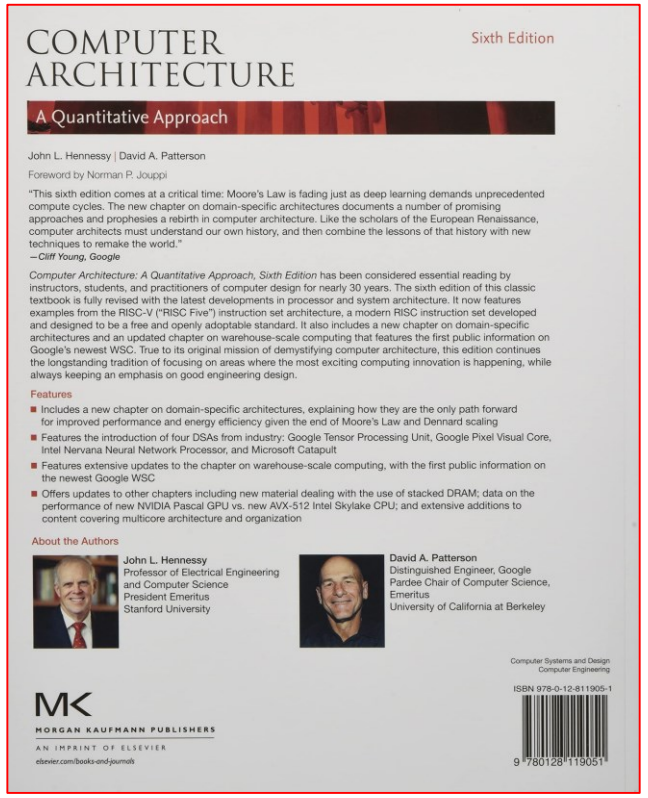
- For detailed discussions, questions about homework, projects, labs, clarifications, etc.
- Signup link

piazza.com/sjtu.org/summer2022/ece4700j

Textbook

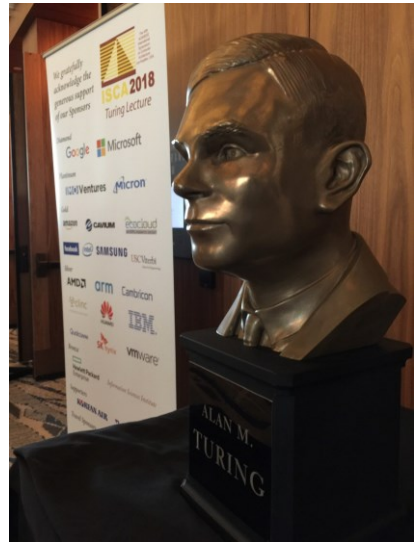
- Computer Architecture: A Quantitative Approach, by John L. Hennessy and David A. Patterson, published by Morgan-Kaufmann publishers, November 2017. ISBN: 9780128119051. (**Sixth** Edition)





About the Authors

- 2017 ACM “Turing Award” Winders (Lecture)
- Inventors of the reduced instruction set computer (RISC)
- Distinguished researchers, leaders and long-time educators
- Authors of groundbreaking computer architecture textbooks



About the Authors

- “simpler is more efficient”

— John Hennessy

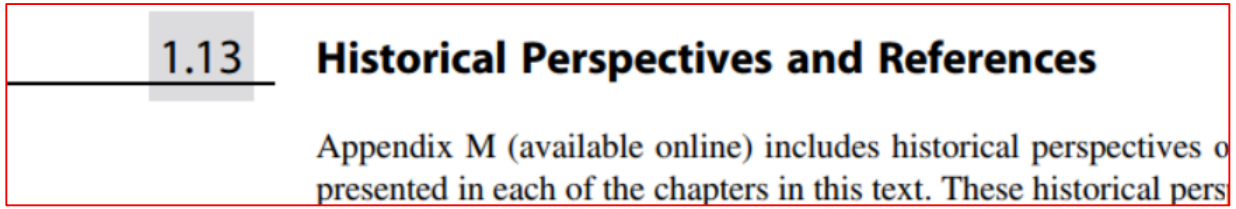
- “Instruction Sets want to be FREE!”

— David Patterson

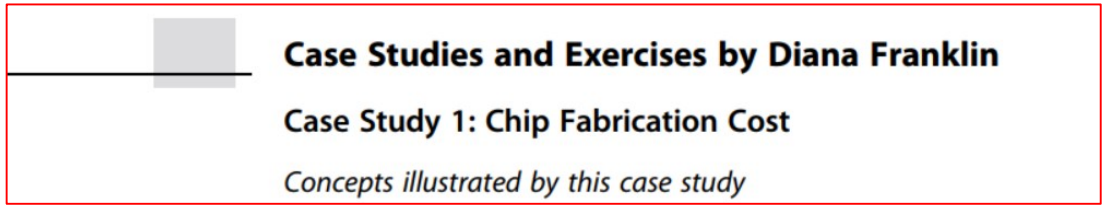
More about this book

Fallacies and Pitfalls

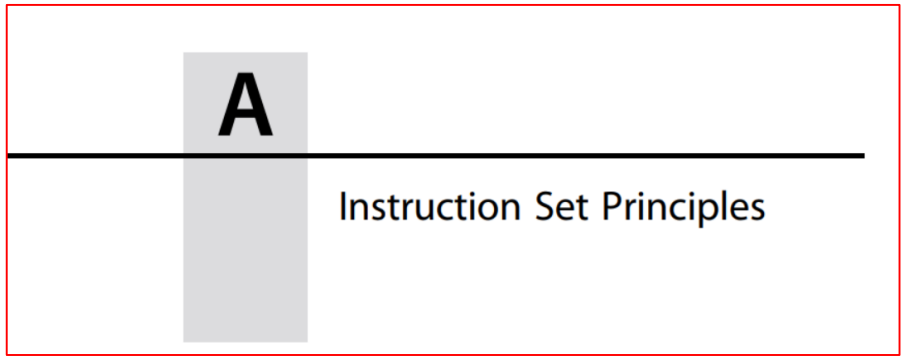
Historical Perspectives



Case Studies



Appendix



Course Survey

VE470 Course Survey #1

Open Feishu to scan code

Please finish by **May 11th, 23:00 Beijing Time,** make sure you answered **ALL** questions.
https://wenjuan.feishu.cn/m?t=ss2clUnTzaCi-kvff

Course Objectives (what will be taught)

- To teach students fundamental design tradeoffs of the modern computer architectures;
- To teach advanced computer architecture concepts such as Multiprocessors, Superscalar, GPUs and advanced caches;
- To give students an exposure to state-of-the-art computer architecture simulators through hands-on assignments and/or a project that will help understand the tradeoffs;
- To offer student hands-on experiences of implementing or optimizing major portions of a substantial processor with either Verilog or High-level design approaches;
- To introduce students the most recent computer architecture advances such as Domain specific architectures (DSA) and AI accelerators;
- To provide experiences of executing a project as a team from concept to finish effectively and professionally, and to offer opportunities to present ideas to the public.

Course Outcomes (what students are expected to achieve)

- Understand fundamentals of designing a modern processor and the key metrics;
- Gain fundamental knowledge and understandings of advanced computer architectures such as multiprocessors, superscalars, advanced caches, and prefetching schemes;
- Learn about state-of-the-art computer architecture simulators or frameworks;
- Develop understandings about certain design tradeoffs in implementing the modern computer architectures;
- Learn about the concept of high-level design languages, AI accelerators or domain-specific architectures;
- Work as a team to implement and optimize a given functional description of a major portion of a substantial processor with learned knowledge and tools;
- Be able to present the results and conclusions of an experimental project in a clear, logical, succinct, and informative written format.

My teaching philosophy

- Broadness and depth
- Practical with practice
- Industry oriented (Stay at the cutting edge)
- Research and teaching are closely coupled
- Teach unknowns
- Learn together

My expectations

- After taking this course (for many, the last course at JI)
  - Be able to understand fundamentals and tradeoffs of designing a modern microprocessor;
  - Be able to develop thinking logics from a hardware perspective;
  - Gain some exposures to real-world design problems;
  - Practice your research ability and critical thinking skills;
  - Be able to present confidently to a broader audience.

Course Topics (Tentative)

- Intro. to Computer Architecture
  - Quantitative Analysis
- The Processing Part (OoO)
  - Pipelining & Hazards
  - Scheduling
  - Interrupts
- Memory
  - Advanced Cache
  - Prefetching
  - Virtual Memory
- Architecture simulation
- Multiprocessors
  - GPUs

Course Topics (as a bonus)

- Domain-Specific Architectures (DSA)
- Processing in Memory (PIM)
- Reconfigurable Computing
- AI Accelerators
- High level synthesis (HLS)
- …

Labs (Tentative plan)

- 36 hours in total
  - Individual based
  - Verilog focused, with some Python/C components
  - Will have common parts and optional parts
  - Logistics need to be decided (complex due to large class size, multiple location/time zones, etc.)

Final Project (Tentative plan)

- Group based (4-5 students)
- Literature review will be part of it
- Implementing/optimizing an advanced architecture with the knowledge learned in this course.
- Will be given a pool to select your project (will be released at least 1 month before the deadline)
- You can also initiate or come up with your own ideas (by talking to the instructor/TA)

Course Outline & Recordings

- https://umjicanvas.com/courses/2578/assignments/syllabus

Course Outline: (Note: Tentative and subject to adjustment.) (All in **Beijing** Time)

Week	Lec #	Date	Topics	Readings	Assignments	Recordings
1	1	5/9	Course introduction, Intro. to Computer Architecture I	Syllabus, Slides, Reading Materials on Canvas	Course Survey Due on **May 11 (Wed), 23:00**	
	2	5/11	Intro. to Computer Architecture, Fundamentals of Quantitative Analysis			
2	3	5/16	Fundamentals of Quantitative Analysis			
	4	5/18	Fundamental Processors I			
3	5	5/23	Fundamental Processors II			
	6	5/25	Fundamental Memories I			
	7	5/30	Fundamental Memories II			

Course Policies

- **Honor Code:**
  - Honor Code of the Joint Institute
  - ***Addendum to the Honor Code for Online Teaching***.
- **Test:**
  - Test procedure will be announced prior to the tests. Anyone violating the test procedure will be given an 'F' for the test.
- **Attendance:**
  - Strongly encouraged for better understanding of difficult concepts and student engagement during class time
- **Participation:**
  - Active participation is highly expected for all students. This involves:
    - Participation in interactive activities during the lecture time
    - Active involvement in projects & labs
    - Proper assistance to other students in group studying
    - Contributions to the Q&A on Piazza, etc.

Course Policies

- **Labs**
  - This is a new course, so bugs/errors are expected.
  - The instructor or TA are not suppose to help with debug the code line by line (as debugging is part of the learning and practice).
  - But high level solutions and resources will be provided if you really get stuck.
  - Asking peers for help is allowed for certain labs, but you need to understand and translate into your own practices.
  - Your work will be measured by reports, demos, and more.

Course Policies

- **Individual Assignments**:
  - Homework and Labs
  - OK to discuss course topics and help each other understand the project/homework requirements better
  - NOT OK for duplicated submission
  - NOT OK to copy solutions from the Internet
- **Group Assignments**:
  - Final project
- **Submission:**
  - Electronic submission on Canvas before deadline
  - No extension will be allowed for homework assignment
  - Extensions need to be approved by the instructor for labs & project (reasons need to be justified)

Assessment Methods

- Labs (with reports)
- Final project (with presentation & report)
  - For those who enroll for capstone, corresponding rules need to be followed.
  - Creativity is strongly encouraged and will be credited.
- Homework
  - 4 – 5 homework
- Paper review & presentation
- Final exam
  - The typical types of exam problems include conceptual understanding, computation, procedural development, short answer, analysis and design, and etc.

Grading Policy

Participation & Etiquette*	5%
Homework	10%
Labs	30%
Literature review/presentation assignment	5%
Final Project & Report	30%
Final Exam	20%
Total	100%

- No attendance requirement for lectures.
- *This includes class/lab interactive discussions on Piazza/Feishu piazza questions and answers, etc.
- **Creative ideas in projects or homework will get bonus**
- Final letter grades may be curved, but not guaranteed

Hours (and hours) of work

- Attend lectures/Watch recordings
  - ~4 hrs/week
- Read book & handouts
  - ~2-3 hrs / week
- Homework
  - On average, 1 hr/week
- Labs/Project
  - 8 hrs/week
- Others
  - 1 hr/week

Concerns?

- The instructor – Who is he? is he good? I heard …
- New course, no history, what if …?
- Labs – are they difficult?
- Project – will it kill me?
- Exam – a lot of difficult questions?
- Class – will it be boring?
- Final grade – is it going to be bad?

How to ~~survive~~ this class?

- Have interests on computer hardware
- Attend/review lectures and participate
  - Involve in discussions
  - Ask questions any time
- No plagiarism (nor anything like it)
- Write your own code
- Understand what you submit
- Be creative in projects
- Read the materials (!)

How to enjoy this class?

- Have interests on computer hardware
- Attend/review lectures and participate
  - Involve in discussions
  - Ask questions
- No plagiarism (nor anything like it)
- Write your own code
- Understand what you submit
- Be creative in projects
- Read the materials (!)

Action Items

- Read syllabus and decide carefully
- Join Feishu group
- Sign up for Piazza
- Finish course survey (by **Wed 5/11 23:00** Beijing Time)

Q & A

- What if I am not in China?
- What if I am not taking it as MDE?
- What if we need to use hardware? How should we get them?
- What if the lectures are not convenient for my timezone?
- What if I miss the office hour?
- What if I miss the deadlines?
- What if I can’t find a teammate for my lab/project?
- Others?