

IO-LINK drivers

Sheet: IO_LINK_0

IO-LINK TRANSCEIVER 0

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IO-LINK TRANSCEIVER 1

File: IO_LINK_1.sch

Sheet: IO_LINK_2

IO-LINK TRANSCEIVER 2

File: IO_LINK_2.sch

Sheet: IO_LINK_3

IO-LINK TRANSCEIVER 3

File: IO_LINK_3.sch

Sheet: Power_Supply

POWER SUPPLY

File: Power_Supply.sch

Sheet: Microcontroller

MICROCONTROLLER

File: Microcontroller.sch



Sheet: /
File: IO_LINK.sch

Title: IO-LINK MASTER board

Size: A4 Date: 22.01.2021

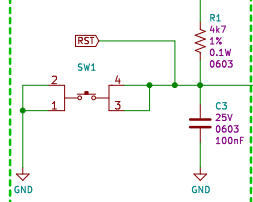
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Rev:
Id: 1/7

MICROCONTROLLER

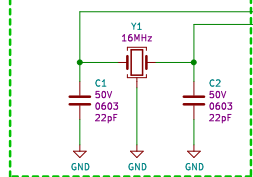
RESET SWITCH

PLACE CLOSE TO STM32F072RBT



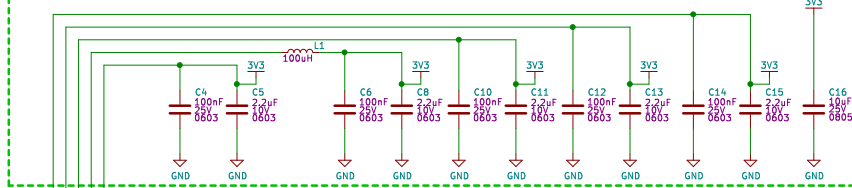
CRYSTAL

EPLACE CLOSE TO STM32F072RBT



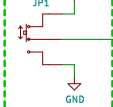
MCU DECOUPLING

PLACE CLOSE TO STM32F072RBT



BOOTLOADER MODE

PLACE CLOSE TO STM32F072RBT



UC-TS_ENCO

(UC-TS_RST)

(UC-TS_ENL+)

(TS_UC_IRQ)

(UC-T2_DATA)

(T2_UC_DATA)

(T0_UC_SIO)

(T0_UC_IRQ)

(UC-T0_ENCO)

(UC-T0_ENL+)

(RST_ETH)

(INT_ETH)

(TS_UC_SIO)

STM32F072RBTx

PA0

PA1

PA2

PA3

PA4

PA5

PA6

PA7

PA8

PA9

PA10

PA11

PA12

PA13

PA14

PA15

PF0

PF1

PD2

PC0

PC1

PC2

PC3

PC4

PC5

PC6

PC7

PC8

PC9

PC10

PC11

PC12

PC13

PC14

PC15

VDD

VSS

VSSA

VDDIO2

VDDIO1

VDDIO0

VDDIO3

VDDIO4

VDDIO5

VDDIO6

VDDIO7

VDDIO8

VDDIO9

VDDIO10

VDDIO11

VDDIO12

VDDIO13

VDDIO14

VDDIO15

VDDIO16

VDDIO17

VDDIO18

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VDDIO202

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VDDIO207

VDDIO208

VDDIO209

VDDIO210

VDDIO211

VDDIO212

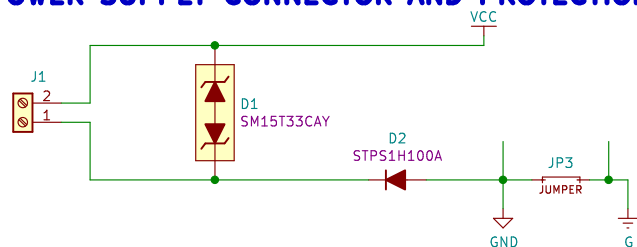
VDDIO213

VDDIO214

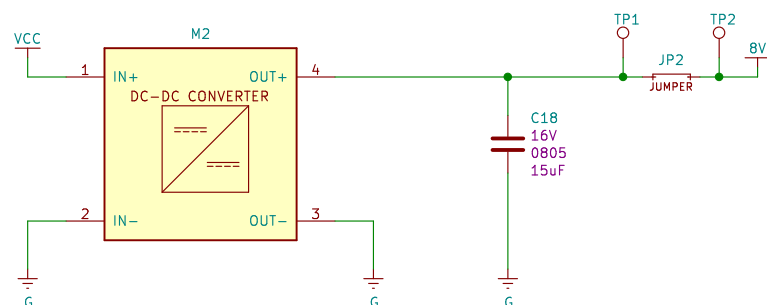
VDDIO215

VDDIO216

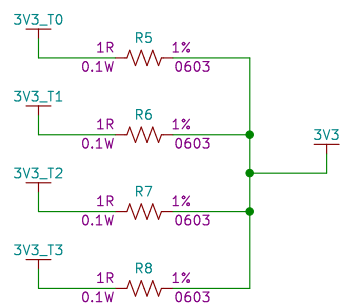
POWER SUPPLY CONNECTOR AND PROTECTION CIRCUIT



DC-DC SMPS POWER SUPPLY SECTION



Each IO_Link transceiver contain its own LDO and their outputs are parallelized:



Sheet: /Power_Supply/
File: Power_Supply.sch

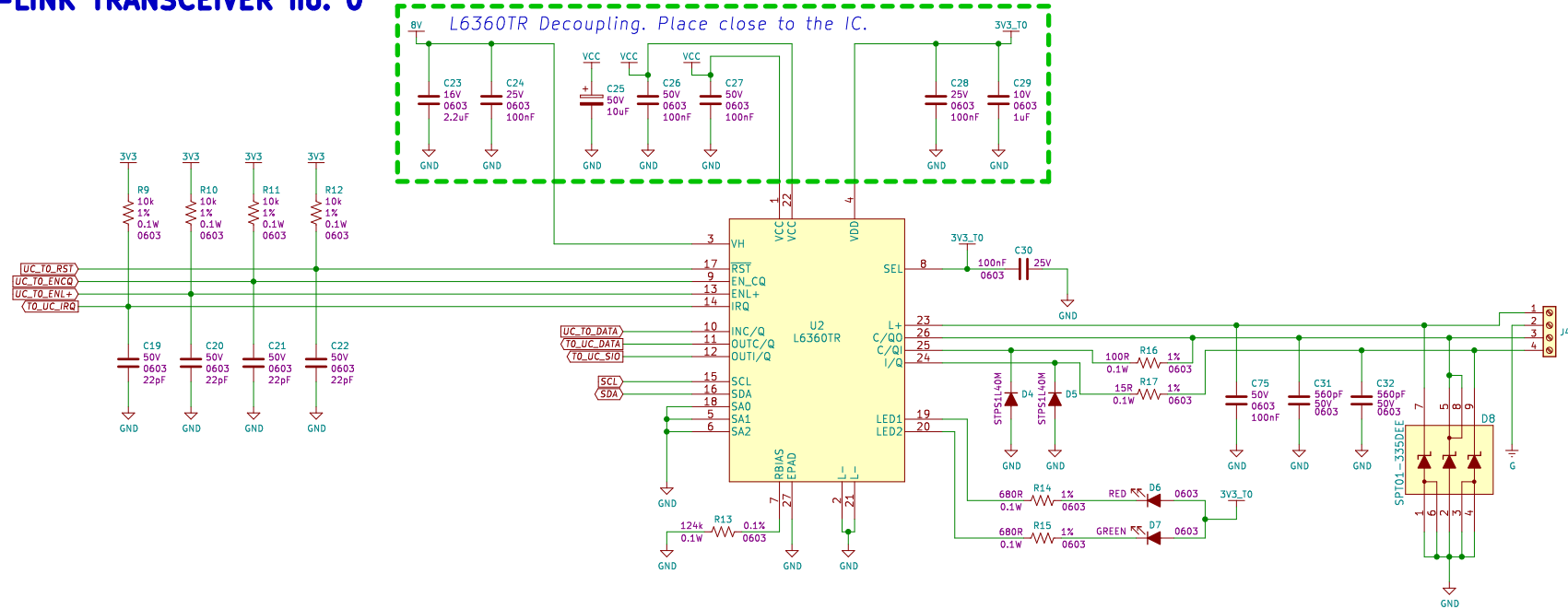
Title: IO-LINK MASTER board / power supply and protection circuit

Size: A4 Date:19.02.2021

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Rev:
Id: 3/7

IO-LINK TRANSCEIVER no. 0



Sheet: /IO_LINK_0/
File: IO_LINK_0.sch

Title: IO-LINK MASTER board / IO-Link driver no. 0

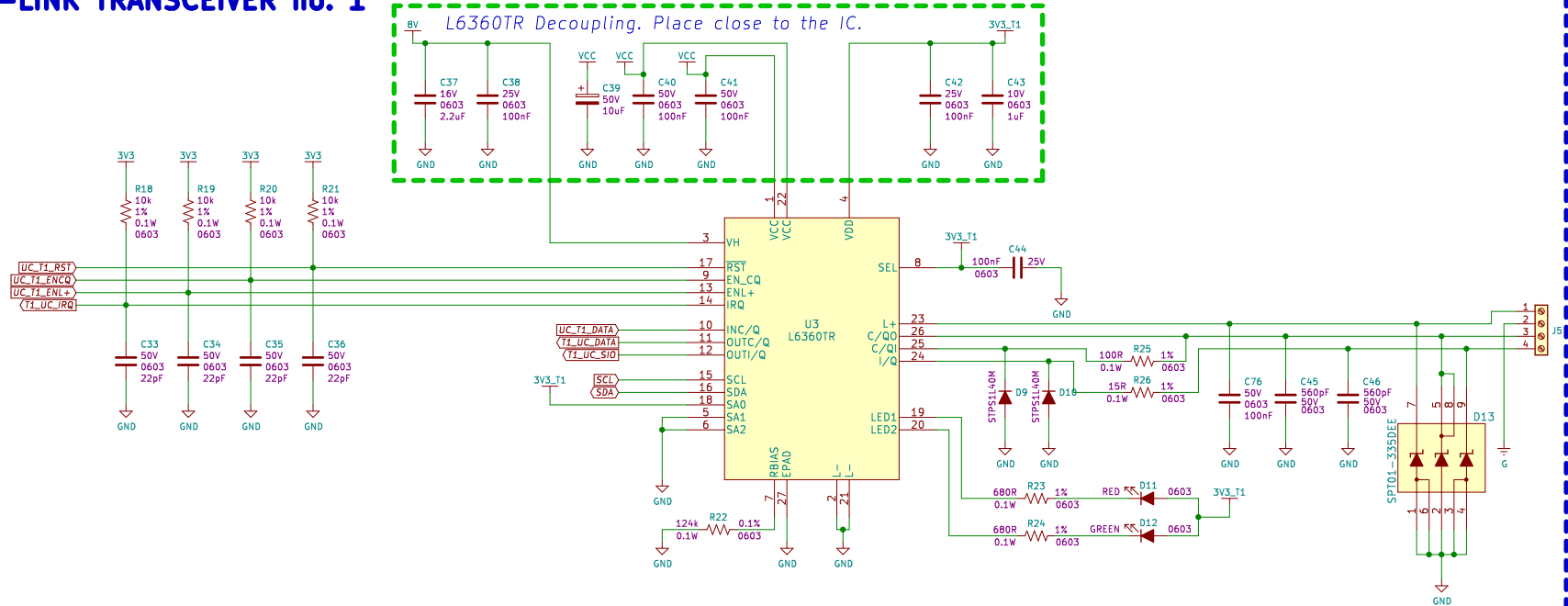
Size: User Date: 22.02.2021
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Rev:
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[illegible]

L6360TR Decoupling. Place close to the IC.

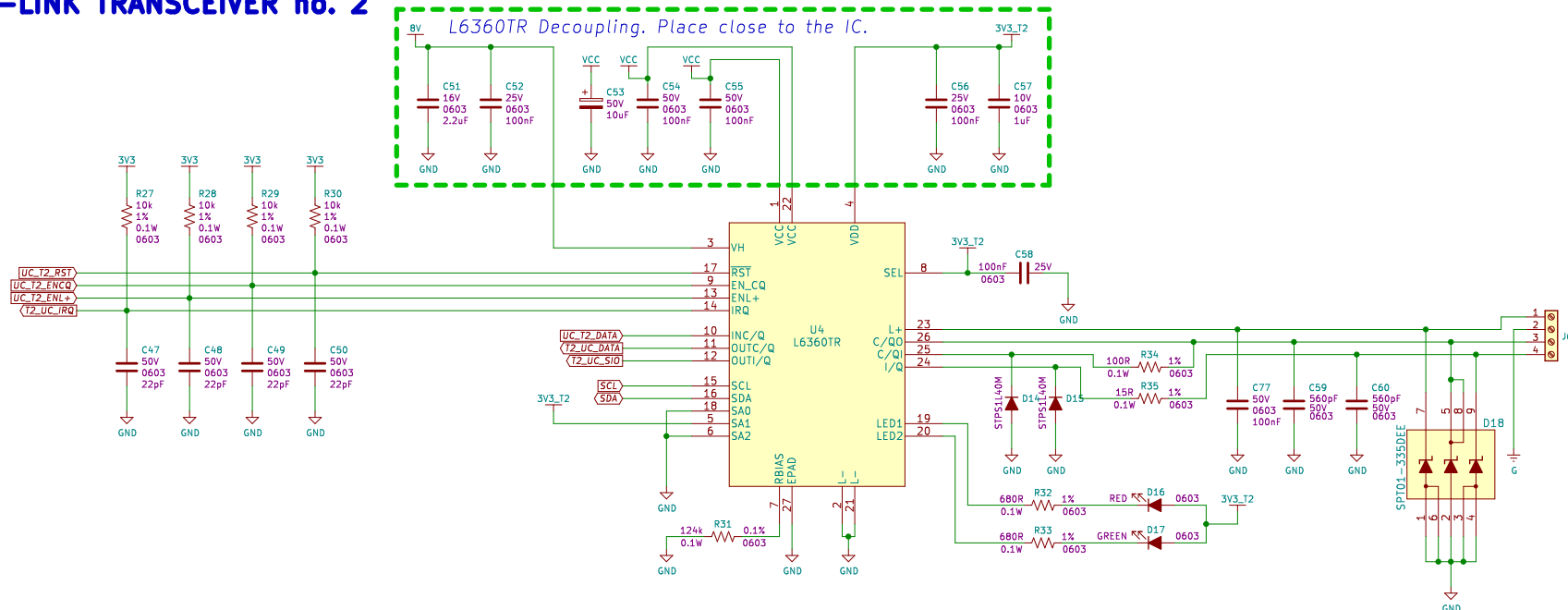
The diagram illustrates the decoupling capacitor placement for the L6360TR. It shows a 5V supply rail with capacitors C37 (16V 0603 2.2uF) and C38 (25V 0603 100nF). A 3V3 supply rail has capacitors C42 (25V 0603 100nF) and C43 (10V 0603 1uF). Intermediate capacitors C39 (50V 10uF), C40 (50V 0603 100nF), and C41 (50V 0603 100nF) are also shown connected to ground.



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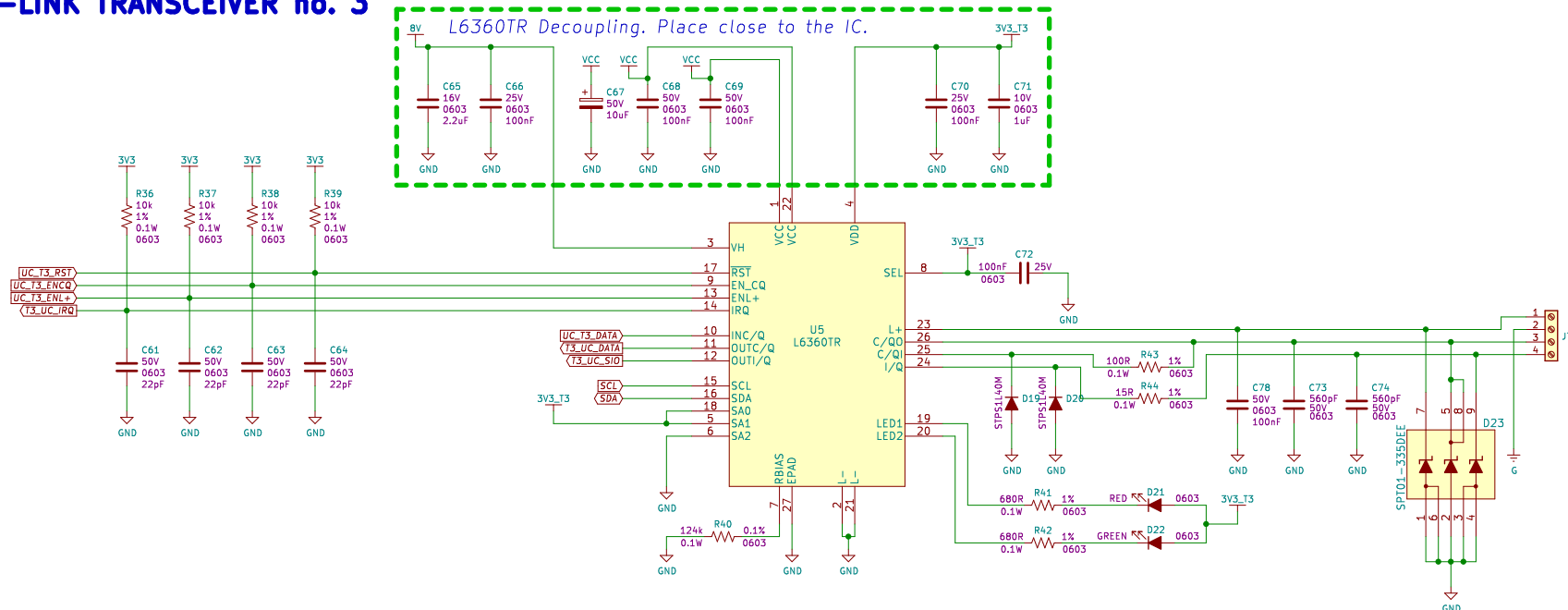
IO-LINK TRANSCEIVER no. 2



Sheet: /IO_LINK_2/
File: IO_LINK_2.sch
Title: IO-LINK MASTER board / IO-Link driver no. 2
Size: User Date: 22.02.2021
KiCad E.D.A. kicad (5.1.9)-1

Rev:
Id: 6/7

IO-LINK TRANSCEIVER no. 3



Sheet: /IO_LINK_3/
File: IO_LINK_3.sch
Title: IO-LINK MASTER board / IO-Link driver no. 3
Size: User Date: 22.02.2021
KiCad E.D.A. kicad (5.1.9)-1

Rev:
Id: 7/7