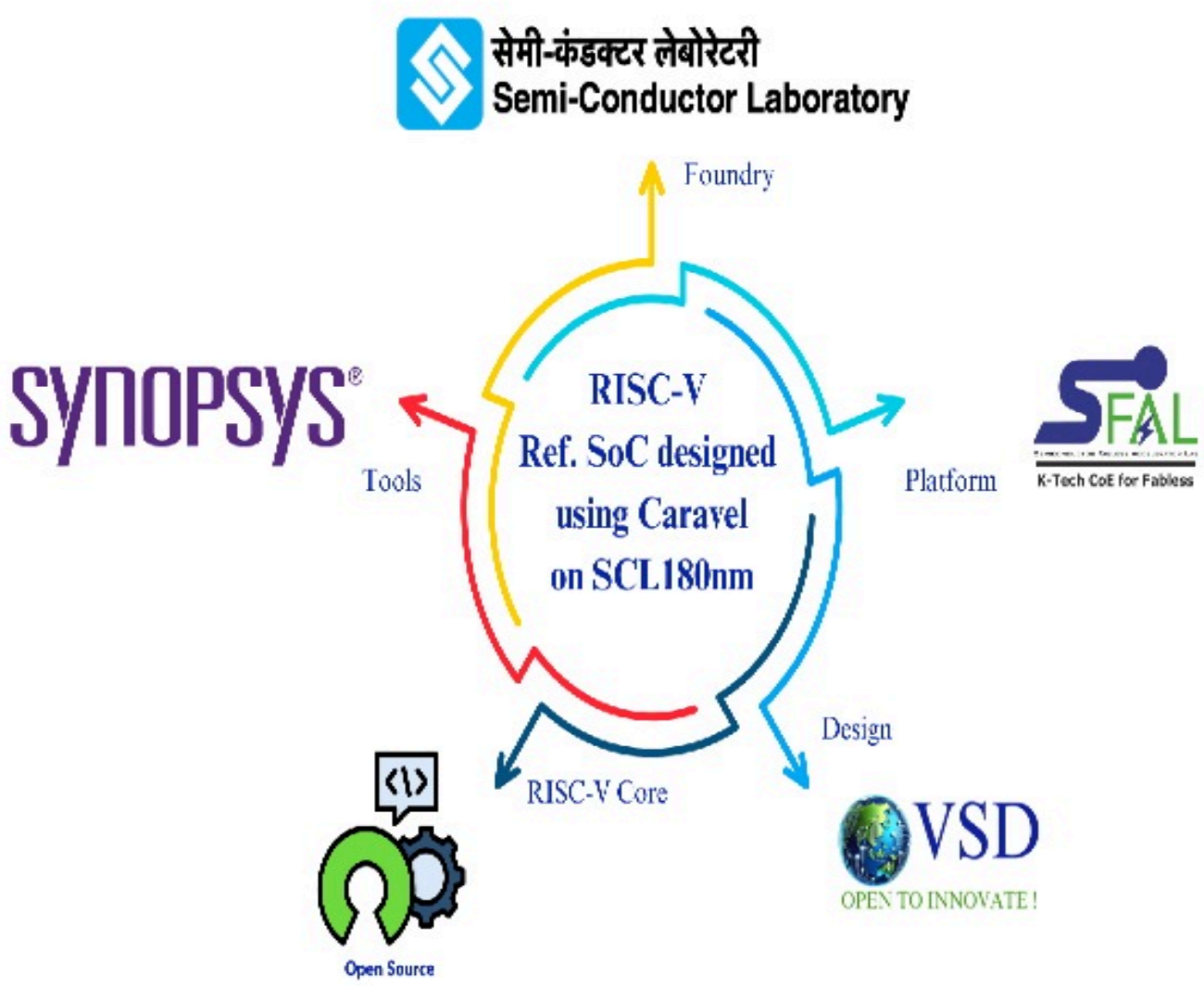
VSDBabySoC

Digital VLSI SoC Design and Planning



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Pre-synth sim is the RTL simulation of the design before synthesis to validate functional behavior with the original Verilog sources and the testbench that generates a VCD waveform. Post-synth sim is the gate-level simulation of the synthesized netlist to check that behavior matches the RTL and to observe effects introduced by synthesis, producing a separate VCD waveform

What pre-synth sim means

Pre-synth sim runs the testbench with the top-level RTL modules directly, using a define that enables dumping signals to a VCD file for waveform viewing in GTKWave. This produces pre_synth_sim.vcd under the pre_synth_sim output directory for inspecting clocks, resets, and data buses at the RTL level.

What post-synth sim means

Post-synth sim runs the same testbench against the synthesized netlist file vsdbabysoc.synth.v to validate logic after synthesis transforms. This produces post_synth_sim.vcd under the post_synth_sim output directory for analyzing gate-level behavior that corresponds to the RTL intent.

How they are run

The flow provides commands that compile and run pre-synth sim with the RTL sources and a macro for conditional dumping, followed by opening the generated VCD in GTKWave. The flow also provides commands that compile and run post-synth sim using the synthesized netlist after the synthesis step completes, followed by opening its VCD in GTKWave.

Aspect	Pre-synth sim	Post-synth sim
Design simulated	RTL sources with the top-level module and testbench [1]	Synthesized netlist vsdbabysoc.synth.v with the same testbench
Purpose	Fast functional verification before synthesis and quick debugging [1]	Functional checking after synthesis to confirm equivalence and observe changes from synthesis

Toolchain usage	Icarus Verilog for compile and run, VCD viewed in GTKWave, PRE_SYNTH_SIM define used in the testbench [1]	Synthesis produces the netlist, Icarus Verilog compiles the netlist with the testbench, VCD viewed in GTKWave
Output VCD	output/pre_synth_sim/pre_synth_sim.vcd [1]	output/post_synth_sim/post_synth_sim.vcd
Signals to inspect	Clock, reset, and data buses at RTL such as RV_TO_DAC and OUT as driven by the testbench [1]	The same logical signals as realized in the synthesized netlist to match RTL intent