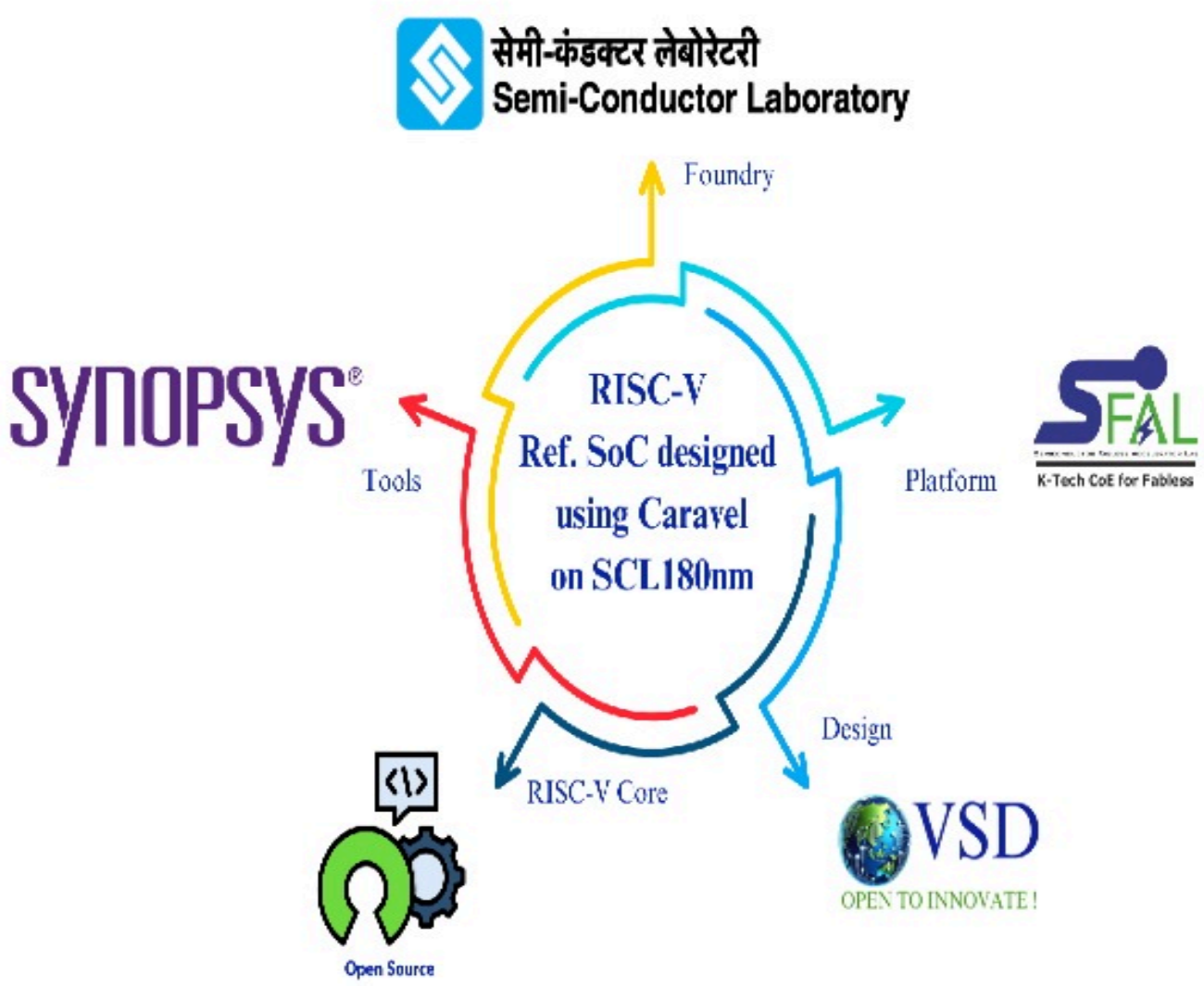
PROCESSOR DESIGN

Digital VLSI SoC Design and Planning



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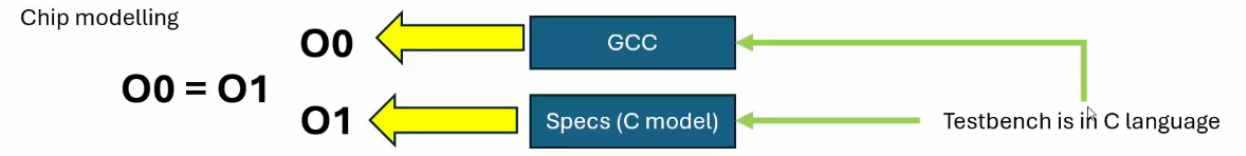
INTRODUCTION

Processors form the basic unit of microcontrollers and these microcontrollers are known as the brain of the electronics. In the era of automation the processor is arguably the most important part of any electronics, and to design it and put it to real world problems requires various steps. The end goal is to make a chip that can solve the problems.

PROCEDURE

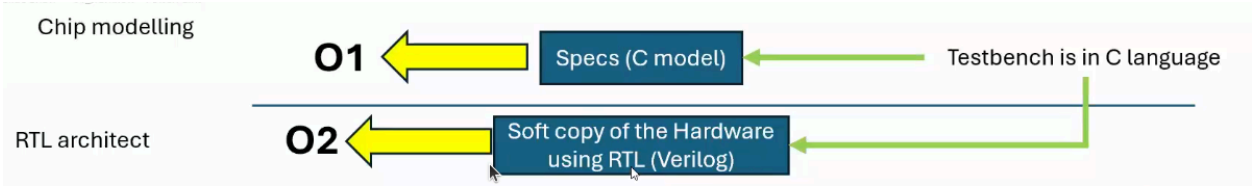
Before directly jumping into writing the hardware code we need chip modelling which is the first step.

- Firstly the application is coded in C language and compiled through a **GCC(compiler)** and an output is obtained namely **'O0'**.
- Now, we model the specification of the processor in the C environment and an output is measured '**O1**'.
- The crucial step is to verify if O0 = O1, once the output is true we can freeze the specification and we finish the first step of design i.e chip modelling.



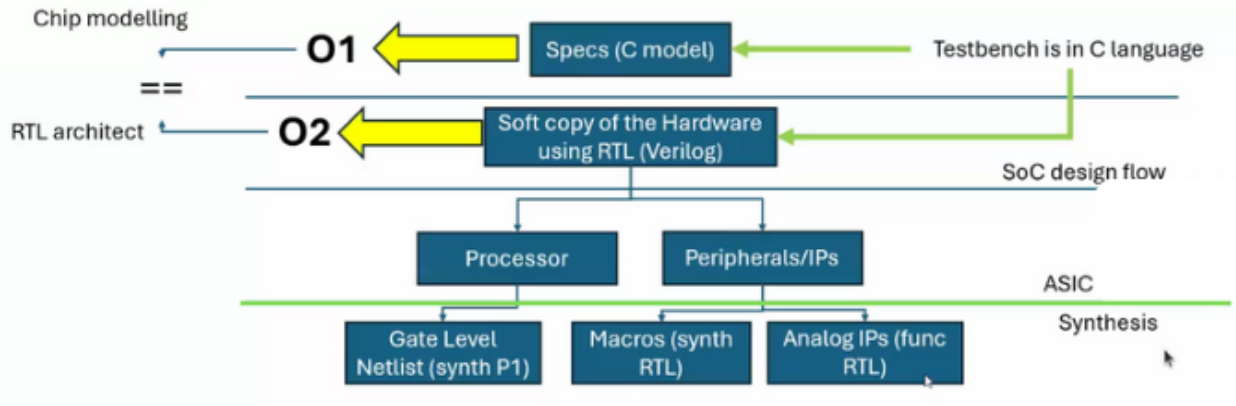
Now, we will move on to RTL Architecture after the chip modelling is complete.

- The code is now written using **RTL verilog** which is called the soft copy of the hardware and we then measure the output **O2**.
- The previous output O2 and output from chip modelling O1 are then compared and if returned true, we can conclude the second step i.e RTL Architecture



Moving to now one of the most crucial step of the design called **SoC Design Flow.**

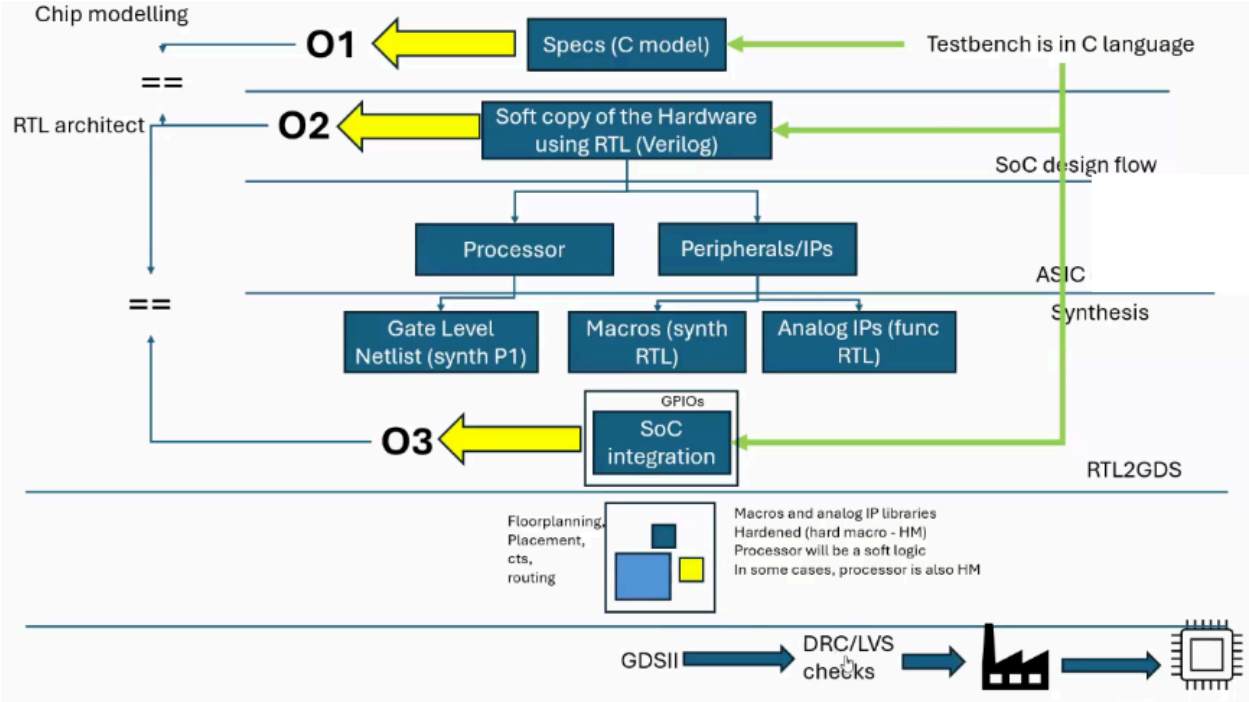
- The RTL architecture is divided into two parts namely **Processors** and **Peripheral/IPs .**
- **Processors** :- In processors we have to write synthesizable code in Verilog which is converted into gate constructs. Code should not include any construct or primitive which cannot be synthesized.
- **Peripheral/IPs** :- These are hardware blocks that support the main processor and perform certain functions. Can be further classified into two sub categories
    - **Macros** : It should also have a synthesizable RTL unlike the processor. These are building blocks of the design which are repeated multiple times.
    - **Analog IPs** : These should not need to have a synthesizable RTL rather the functional RTL is preferred. These handle real world analog signals, not just 0s and 1s.



The last part before tapeout is SoC Integration which is the inclusion of every above block into the way it was designed.

- **GPIOs** : General Purpose Input / Output pins are used for data transmission.
- The engineer collects all blocks integrating them with GPIOs and measures the output O3 which is then verified with O2, and if it's true a file is generated called GDSII.
- **GDSII (Graphical Data Stream Information Interchange)** is a file that needs a lot of computational power, as it contains all the details related to fabrication be it parts, material used etc so we run this file through

DRC/LVS checks before sending for tapeout and in 4-6 months we get our chip.



Finally after the tape-in, the chip is ready but the other components which are necessary for the completion are yet to be connected via the board

- When a chip is placed on the board with other blocks and forms a complete micro controller, we one last time measure the output **O4** and match with **O3,** if the results are positive we get a complete micro controller that has specification, look and functioning totally of our choice.
- We can replicate or even produce better micro controllers or boards at a much lower cost which can be scaled and used in various applications.