Static Timing Analysis (STA) – Summary Notes

1. Timing Path Basics

The course began with the concept of a timing path, which typically starts at a launch flip-flop goes through some combinational logic, and ends at a capture flip-flop.

2. Arrival Time and Required Time

- **Arrival Time (AAT):** This is the actual time when a signal reaches the capture point.
- **Required Arrival Time (RAT):** This is the time by which the data must arrive to meet timing constraints.

3. Slack (Max and Min)

- **Slack = RAT - AAT**
- If slack is **positive**, timing is met.
- If slack is **negative**, there is a violation.
- **Setup analysis** focuses on maximum delay paths (late data arrival).
- **Hold analysis** focuses on minimum delay paths (early data arrival).

4. Setup and Hold Checks

- **Setup Check:** Verifies that data arrives before the clock edge plus the setup time of the flip-flop.
- **Hold Check:** Verifies that data remains stable after the clock edge for at least the hold time.

5. Types of Setup/Hold Analysis

- **Path-based analysis:** Evaluates specific timing paths individually, often used for detailed checks or debugging.
- **Graph-based analysis:** Uses a timing graph to calculate slack across all paths simultaneously. It's faster and more scalable.

6. Clock Analysis

- Clock definitions are essential in STA. Clocks can be:
    - **Ideal clocks** with no delay or skew.
    - **Generated clocks** derived from PLLs or dividers.

- Important clock-related factors:
    - **Skew:** Difference in clock arrival time at different flip-flops.
    - **Jitter:** Random variation in clock period.

7. Skew, Transition, and Load Analysis

- **Clock Skew:** Can help or hurt timing depending on direction. Impacts both setup and hold.
- **Transition Time:** The time it takes for a signal to switch. Poor transitions can increase delay and power.
- **Load Analysis:** Affects cell delay based on the number of gates or wire capacitance being driven.

8. reg2reg Timing Path Example

In the reg-to-reg timing example, sir showed a flip-flop to flip-flop path. The circuit was converted into a Directed Acyclic Graph (DAG) for STA. Arrival time, required time, and slack were calculated to identify whether timing was met.