Flavor of GHDL Setup

I used GHDL by ssh-ing onto the Halligan servers. Bland, but no issues so far.

I definitely did not get mad after failing multiple times to create a gtkwave file [square brackets are funny].

A Refreshing Type of Model

For AND2, as it was a basic AND gate, I chose to model it with some nice and fresh combinational logic. That comes with the `dataflow` VHDL architecture bundle! As for the testbench, because it tests AND2 and requires it as a component, I chose `structural` VHDL architecture!

Waveforms from GTK

The green lines indicate the logic table. Initially, `in0` and `in1` are both 0. Then they alternate between having 1 or 0. Finally, both are 1. We see that the `output` waveform is 0 for all cases except when both inputs are 1. This is consistent with AND gate logic.

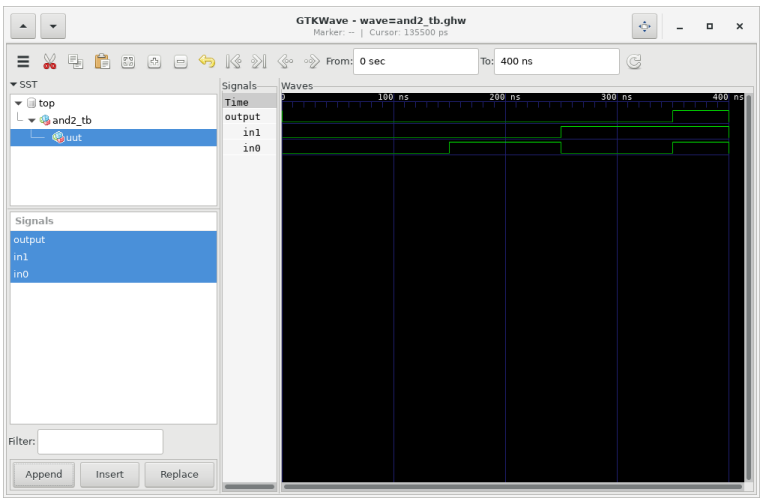

Figure 1: and2_tb Waveform