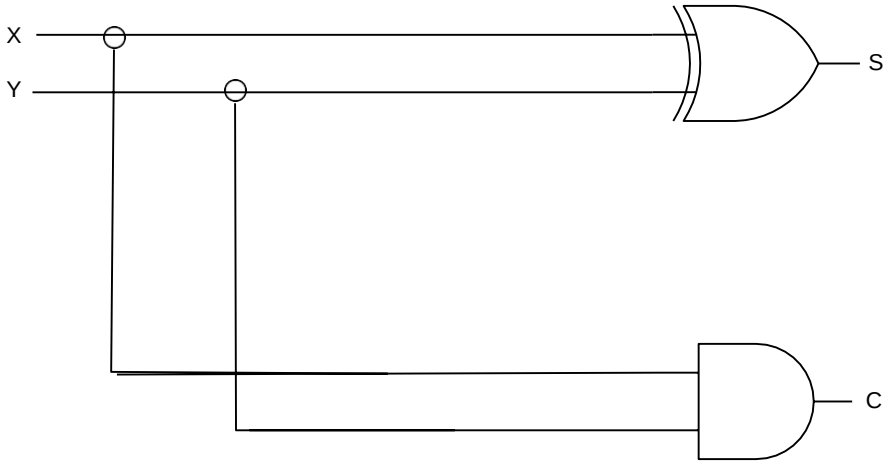
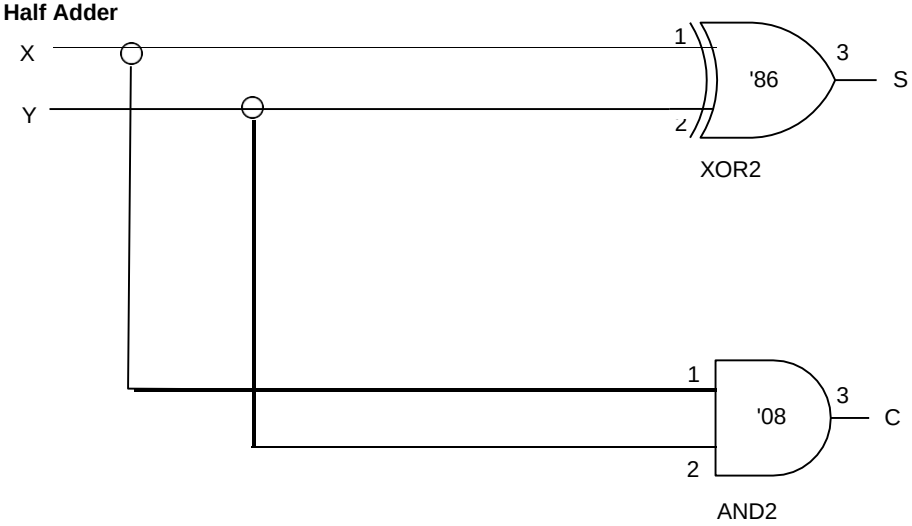
Logic Diagram of Half Adder



$S = X \oplus Y$
$C = X.Y$

Circuit Schematic of Half Adder



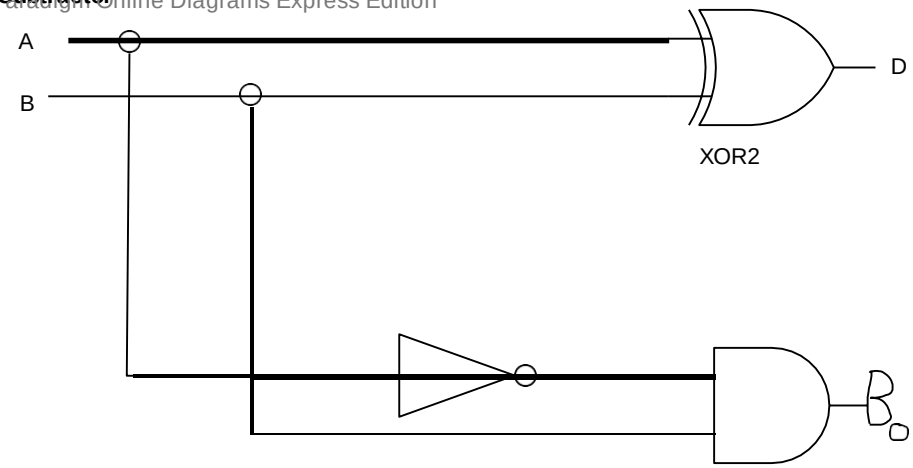
IC List of Half Adder

One 7408 Quad 2-Input AND Gate
One 7486 Quad 2-Input XOR Gate

74LS08:
GND- 7
+5- 14

74LS86:
GND- 7
+5- 14

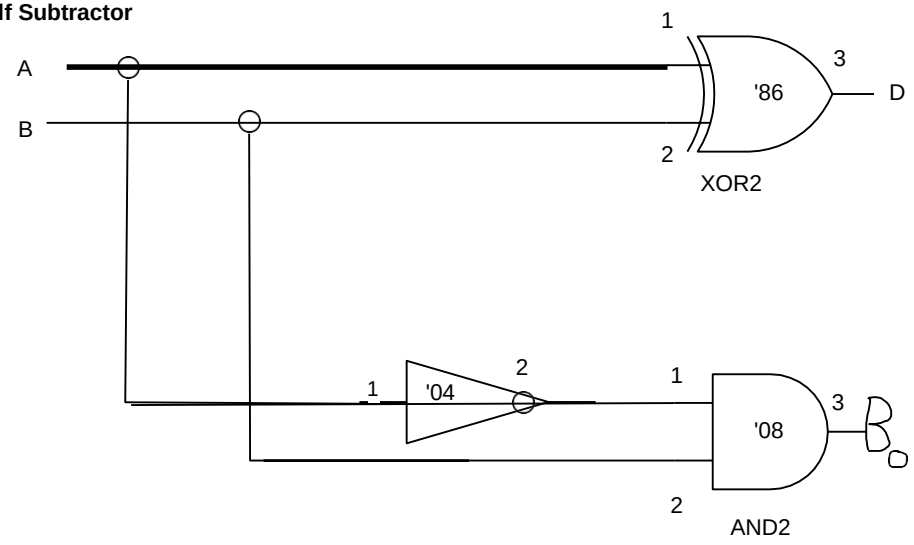
Subtractor



$D = A \oplus B$

Borrow out = $\overline{A}$ .B

Circuit Schematic of Half Subtractor



IC List of Half Subtractor

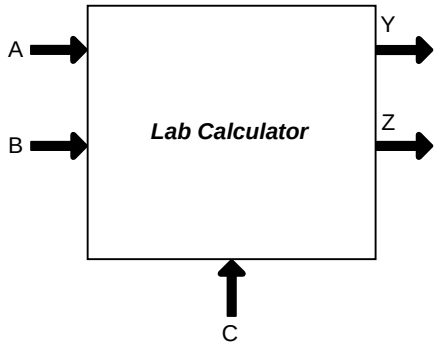
One 7408 Quad 2-Input AND Gate
One 7486 Quad 2-Input XOR Gate
One 7404 six INVERTER.

74LS08:
GND- 7
+5- 14

74LS86:
GND- 7
+5- 14

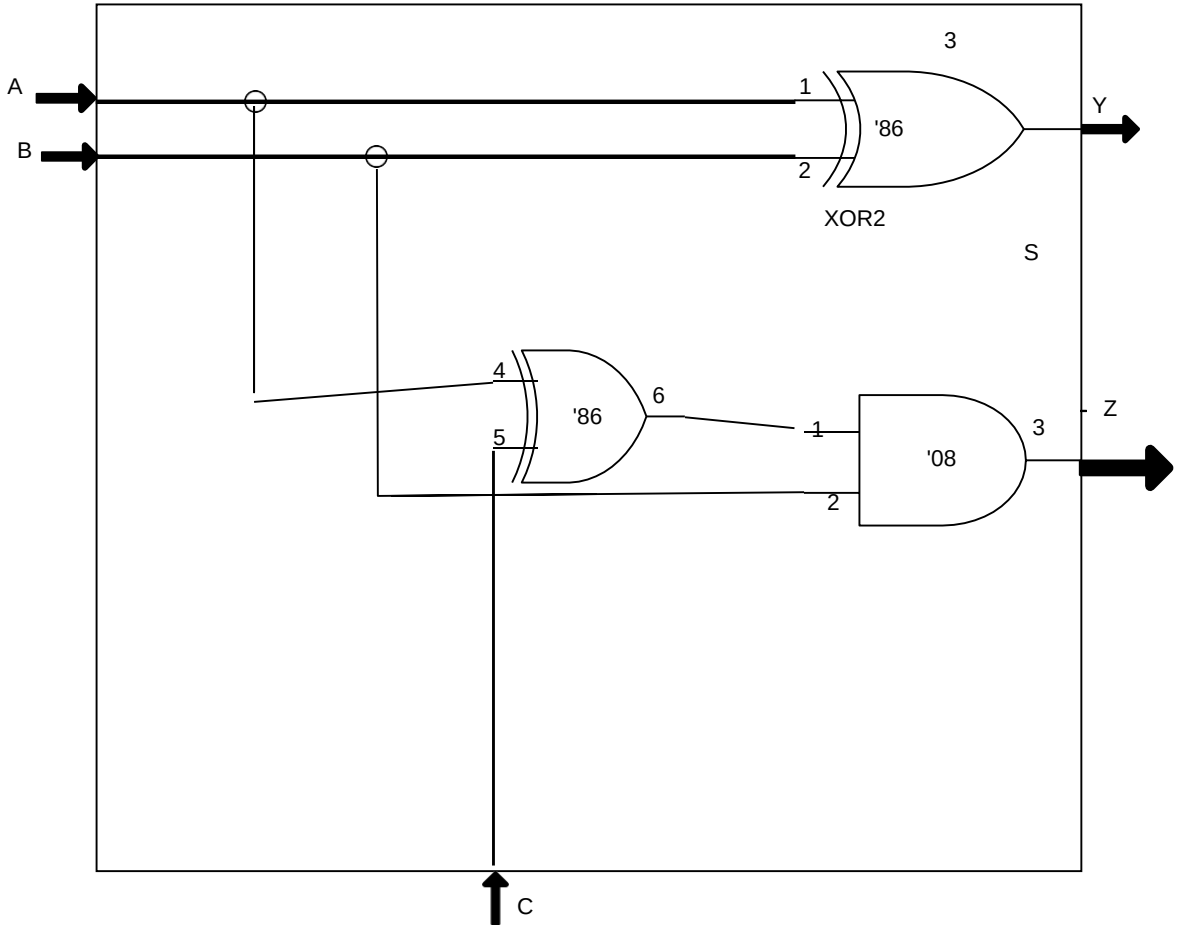
74LS04:
GND- 7
+5- 14

Logic Diagram of Lab Calculator



$Y = A \oplus B$
$Z = (A \oplus C).B$

Circuit Schematic of Lab Calculator



IC List of Lab Calculator
One 7408 Quad 2-Input AND Gate
One 7486 Quad 2-Input XOR Gate

74LS08:
GND- 7
+5- 14

74LS86:
GND- 7
+5-