

MUX com WITH SELECT — RTL

project_Aula2 - [C:/FPGA/FPGAAula2/project_Aula2/project_Aula2.xpr] - Vivado 2015.3

File Edit Flow Tools Window Layout View Help

Default Layout

Synthesis Complete

Flow Navigator

- Generate Block Design
- Simulation
 - Simulation Settings
 - Run Simulation
- RTL Analysis
 - Elaboration Settings
 - Elaborated Design
 - Report DRC
 - Report Noise
 - Schematic
- Synthesis
 - Synthesis Settings
 - Run Synthesis
 - Synthesized Design
 - Constraints Wizard
 - Edit Timing Constraint
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 - Report Timing Summary
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 - Report Clock Interactions
 - Report DRC
 - Report Noise
 - Report Utilization
 - Report Power
 - Schematic
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 - Implementation Settings
 - Run Implementation
 - Open Implemented Design
- Program and Debug

Elaborated Design - xc7a100tcsq324-1 (active)

RTL Netlist

- MUX
- Nets (7)
- Leaf Cells (2)

Sources

RTL Netlist

Properties

Select an object to see properties

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Strategy
synth_1	constrs_1	synth_design Complete!							1	0	0	0	0	11/22/15 9:25 PM	00:00:09	Vivado Synthesis Defaults (Vivado Synthesis 2014
impl_1	constrs_1	Not started														Vivado Implementation Defaults (Vivado Implemen

Td Console Messages Log Reports Design Runs

Schematic

in0 S=2'b00 I0

in1 S=2'b01 I1

in2 S=default I2

dout_i

addr[1:0]

RTL_MUX

dout_OBUF_inst

OBUF

dout

MUX com WITH SELECT — Síntese

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Synthesis Complete

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Synthesized Design - xc7a100tcsg324 1 (active)

Netlist

- MUX
- Nets (12)
- Leaf Cells (7)

Sources Netlist

Properties

Select an object to see properties

Project Summary Device MUX.vhd Schematic

7 Cells 6 I/O Ports 12 Nets

in0 in1 in2 addr[1:0]

in0_IBUF_inst IBUF

in1_IBUF_inst IBUF

in2_IBUF_inst IBUF

addr_IBUF[0]_inst IBUF

addr_IBUF[1]_inst IBUF

dout_OBUF_inst_i_1

LUT5

dout_OBUF_inst OBUF

dout

Tcl Console

```
INFO: [Netlist 29-17] Analyzing 5 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-479] Netlist was created with Vivado 2015.3
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
```

Type a Tcl command here

Tcl Console Messages Log Reports Design Runs

MUX com WHEN ELSE — RTL

project_Aula2 - [C:/FPGA/FPGAAula2/project_Aula2/project_Aula2.xpr] - Vivado 2015.3

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Elaborated Design - xc7a100tcs324-1 (active)

RTL Netlist

- MUX
- Nets (3)
- Leaf Cells (2)

Sources

RTL Netlist

Properties

Select an object to see properties

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Strategy
synth_1	constrs_1	synth_design Complete!							0	0	0	0	0	11/22/15 10:01 PM	00:00:07	Vivado Synthesis Defaults (Vivado Synthesis 2)
impl_1	constrs_1	Not started														Vivado Implementation Defaults (Vivado Impl

Td Console Messages Log Reports Design Runs

Schematic (3)

2 Cells 6 I/O Ports 3 Nets

```
graph LR
    in2[in2] --> in2_IBUF_inst[IBUF]
    in0[in0] --> in2_IBUF_inst
    in1[in1] --> in2_IBUF_inst
    in2_IBUF_inst --> dout_OBUF_inst[OBUF]
    dout_OBUF_inst --> dout[dout]
```

MUX com WHEN ELSE — Síntese

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Synthesized Design - xc7a100tcsq324-1 (active)

Netlist

- MUX
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Properties

Select an object to see properties

Project Summary | Device | MUX.vhd | Schematic (2)

2 Cells | 6 I/O Ports | 3 Nets

```
graph LR
    in2[in2] --> in2_IBUF_inst[in2_IBUF_inst]
    addr[addr[1:0]] --> in2_IBUF_inst
    in0[in0] --> in2_IBUF_inst
    in1[in1] --> in2_IBUF_inst
    in2_IBUF_inst --> dout_OBUF_inst[dout_OBUF_inst]
    dout_OBUF_inst --> dout[dout]
```

Tcl Console

```
launch_runs synth_1
[Sun Nov 22 22:01:00 2015] Launched synth_1...
Run output will be captured here: C:/FPGA/FPGAAula2/project_Aula2/project_Aula2.runs/synth_1/runme.log
refresh_design
INFO: [Netlist 29-17] Analyzing 1 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-479] Netlist was created with Vivado 2015.3
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
```

Type a Tcl command here

Tcl Console | Messages | Log | Reports | Design Runs

Qual a tecnologia escolhida pelo sintetizador para implementar a lógica ?

LUT