

## EDUCATION

B.S.E., **Electrical & Computer Engineering**, Princeton University GPA: 3.9

Sep 2022 - May 2026

- **Awards/Honors:** Tau Beta Pi (Engineering Honor Society), Machado de Assis Prize (Excellence in advanced Portuguese courses).
- **Minors:** Computer Science, Optimization & Quantitative Decision Science, Portuguese Language & Culture.
- **Relevant Graduate Coursework:** Advanced Computer Architecture, Domain-Specific Computer Systems Architecture (CPU, GPU, CGRA, FPGA, ASIC, TPU), VLSI Design. **Relevant Undergraduate Coursework:** Computer Architecture & Organization, Digital Logic Design, Algorithms & Data Structures, Systems Programming, Semiconductor Microfabrication, Power Electronics, Analog ICs, Robotics, Circuit Design, Signals & Systems, Stochastic Systems, Optimization, Machine Learning for Predictive Data Analytics.
- **Activities:** Science Olympiad Executive Board & Event Supervisor, WPRB 103.3 FM Radio DJ, Princeton Students in Quantum.

## SKILLS & LANGUAGES

- **Programming Languages:** Verilog, Java, Python, C/C++, ARMv8 Assembly, Tcl. Learning SystemVerilog (UVM), CUDA, CUDA-Q.
- **Tools:** Cadence (Virtuoso, Spectre, Genus, Innovus, Tempus, Xcelium, Flowtool), Synopsys (HSPICE, Nanosim), SPICE (LTSpice, QSPICE, PLECS), Linux/Unix, Emacs, GDB, Git, gem5.
- **Technical Skills:** Digital Design, RTL Design, CPU & Computer Architecture (ISA, High-Performance Processor Organization, Pipelining, Superscalars, Vector Processors, Branch Prediction, RISC-V, CISC, SIMD, MIMD, VLIW, x86, Arm), VLSI Design (Logic Synthesis, Place and Route (PnR), Layout, Schematic Design/Simulation, Physical Verification, Static Timing Analysis, DRC, LVS), Hardware Security, Quantum Computing, Silicon Design, Scripting, Soldering.
- **Languages:** Spanish (proficient), Mandarin Chinese (conversational), Portuguese (intermediate).

## RELEVANT WORK & PROJECT EXPERIENCE

**Incoming Core Design Verification Intern**, [Advanced Micro Devices \(AMD\), Inc.](#), Boxborough, MA May 2026 - Aug 2026

**ASIC Physical Design Engineering Intern**, [Cadence Design Systems](#), San Jose, CA May 2025 - Aug 2025

- Performed RTL-to-GDSII flow (Genus, Innovus, Tempus) to synthesize and place & route (PnR) Verilog/SystemVerilog designs, optimizing power, performance, and area (PPA) metrics on a SousVide controller and HiFi3 audio coprocessor.
- Evaluated 70+ design points (design attributes, aspect ratios, frequencies, optimization levels) for the HiFi3 chip, creating a final high-performance design (+13.6% frequency, +5% PPA) and a low power/area design (-10% area, -66% power, +22 to +37% PPA).

**Undergraduate Course Assistant**, [Princeton Engineering](#), Princeton, NJ Feb 2023 - Present

- Digital Logic Design (Fall 2024, Fall 2025), Circuit Design (Spring 2025), Signals & Systems (Spring 2025), Algorithms & Data Structures (Fall 2024), Engineering Physics: Electricity, Magnetism, & Photonics (Spring 2023).

**Hardware Security Research**, [Princeton ECE](#), Princeton, NJ Jan 2025 - May 2025

- Built framework using Verilog, Python, and C++ to apply taint-kill timing side-channel detection by extracting FSMs from HDL truth tables, automating VCD-to-JSON FSM graph conversion, with verified results on 3 designs using 2 automated testbenches.
- Scaled brute-force FSM extraction to 14-bit designs in ~50-110 mins, proposed graph pruning to reduce exponential growth.
- Advised by Professor Sharad Malik, presented in Princeton ECE Undergraduate Research poster session. [Poster](#), [Paper](#), [Code](#).

**gem5 Cache Replacement Policy Implementation & Comparison** Apr 2025 - May 2025

- Implemented 5 cache replacement policies in C++ in gem5 to analyze tradeoffs between frequency and recency based eviction.
- Benchmarked policies on STREAM benchmark and Bringup-Bench varying cache sizes and types of operation.
- Achieved lowest STREAM miss rates using WLRFU, minimized cache thrash misses using RRIP, and more results analyzed in report.

**Verilog RISC-V Processor Design** Jan 2025 - Apr 2025

- **Iterative Multiplier/Divider:** implemented a 32-bit iterative multiplier and divider in Verilog with FSM-based controllers, completed operations in 33 cycles using valid/ready handshaking, wrote 40+ custom tests (signed/unsigned mul, div, rem) and validated edge cases like overflow and negative operands.
- **Pipelined Processor with Bypassing & Mul/Div Unit:** updated 5-stage pipelined RISC-V processor to support bypassing and a 4-cycle pipelined mul/div unit by extending the pipeline to 7 stages, achieved 6x speedup on complex multiplication benchmark (16.8k to 2.55k cycles) and 2.5x on masked-filter benchmark (15.8k to 4.9k cycles) compared to stall-only baseline.
- **Superscalar Processor:** designed a 2-issue in-order superscalar RISC-V processor, verified correctness with custom test suites (non-ALU dual issue, WAW hazards, SW-LW bypass), achieved IPC up to 0.96.
- **Out-of-Order (OOO) Execution with Reorder Buffer:** equipped an OOO core with in-order commit by designing and integrating a Reorder Buffer (ROB) with bypass support, created custom OOO test programs (ROB ordering, bypassing, WAW hazards).

## ADDITIONAL TECHNICAL WORK EXPERIENCE

• **Power Electronics Intern**, [Princeton Satellite Systems](#), Plainsboro, NJ

Jan 2025

• **Electrical Engineering Intern**, [Lutron Electronics](#), Boynton Beach, FL

May 2024 - Aug 2024

• **Energy Management Intern**, [NextEra Analytics \(NextEra Energy\)](#), St. Paul, MN

Jun 2023 - Aug 2023

• **Research Assistant**, [Princeton Center on Science and Technology \(CST\)](#), Princeton, NJ

Oct 2022 - May 2023