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EDUCATION

B.S.E., ***Electrical & Computer Engineering***, **Princeton University** **GPA:** 3.9/4.0 Sep 2022 - May 2026

- **Awards/Honors:** **Tau Beta Pi Engineering Honor Society** (Top 1/5), **Machado de Assis Prize** (Excellence in Portuguese courses).
- **Minors:** *Computer Science*, *Optimization & Quantitative Decision Science*, *Portuguese Language & Culture*.
- **Activities:** **Science Olympiad** (Exec. Board & Event Supervisor), **WPRB 103.3 FM** (Radio DJ), **Students in Quantum**, **Rocketry** (Prev. Social Officer), **Center for InfoTech Policy Digital Witness Lab** (Prev. Research Assistant), **Campus Dining** (Prev. Student Worker).
- **Selected as 1 out of 10 students to complete Princeton in Portugal: four week study abroad program in Portugal and Cape Verde**

RELEVANT WORK, RESEARCH, & PROJECT EXPERIENCE

Incoming Core Design Verification Intern, **Advanced Micro Devices (AMD), Inc.**, Boxborough, MA May 2026 - Aug 2026

- Accepted an offer to intern at AMD during the summer between my Bachelor's graduation and starting my PhD.

Quantum Computing Senior Thesis, **Princeton ECE**, Princeton, NJ Aug 2025 - May 2026

- Working with ***Professor Margaret Martonosi*** and received $420 in funding for the fall semester from Princeton ECE and SEAS.
- Implementing SupermarQ benchmarks in CUDA-Q for integration with NVIDIA's quantum ecosystem.
- Adapting SupermarQ to benchmark Duke University's STAQ machines and comparing performance with prior technologies.
- Systematically studying the effects of scaling SupermarQ benchmark sizes to reveal potential trends in both the benchmarking methodology and quantum hardware performance.

Genomics GPU: A Hybrid SIMD-Systolic Architecture for Filtering & Alignment (ECE 580 Project) Oct 2025 - Dec 2025

- Coding GPU in Verilog to exploit both SIMD and wavefront parallelism, incorporating special genomics processing systolic arrays to accelerate D-SOFT and GACT algorithms from **Darwin** paper.
- Making algorithmic changes to D-SOFT for better SIMD parallelism and memory access patterns, testing threading schemes using OpenMP and GPUs. Achieved a 2x speedup running D-SOFT in parallel instead of serially. **Poster** in progress.

ASIC Physical Design Intern, **Cadence Design Systems**, San Jose, CA May 2025 - Aug 2025

- Performed RTL-to-GDSII flow (Genus, Innovus, Tempus) to synthesize and place & route (PnR) Verilog/SystemVerilog designs, optimizing power, performance, and area (PPA) metrics on a SousVide controller and HiFi3 audio coprocessor.
- Evaluated 70+ design points (design attributes, aspect ratios, frequencies, optimization levels) for the HiFi3 chip, creating a final high-performance design (+13.6% frequency, +5% PPA) and a low power/area design (-10% area, -66% power, +22 to +37% PPA).
- Presented 2 design reviews to senior engineers/managers and 1 intern showcase poster to the company. **Received options to return**.

Hardware Security Junior Independent Research, **Princeton ECE**, Princeton, NJ Jan 2025 - May 2025

- Built framework using Verilog, Python, and C++ to apply taint-kill timing side-channel detection by extracting FSMs from HDL truth tables, automating VCD-to-JSON FSM graph conversion, with verified results on 3 designs using 2 automated testbenches.
- Scaled brute-force FSM extraction to 14-bit designs in ~50-110 mins, proposed graph pruning to reduce exponential growth.
- Advised by ***Professor Sharad Malik***, presented at Princeton ECE Undergraduate Research poster session. **Poster**, **Paper**, **Code**.

gem5 Cache Replacement Policy Implementation & Comparison (ECE 475/575 Project) Apr 2025 - May 2025

- Implemented 5 cache replacement policies in C++ in gem5 to analyze tradeoffs between frequency and recency based eviction.
- Benchmarked policies on STREAM benchmark and Bringup-Bench varying cache sizes and types of operation.
- Achieved lowest STREAM miss rates using WLRFU, minimized cache thrash misses using RRIP, and more results analyzed in report.

Arduino Ethernet Model (ECE 583 Project) Apr 2025 - May 2025

- Created a model of Metcalfe and Bogg's early ethernet using 3 communicating Arduinos Unos, circuit elements, and an original FSM.
- Incorporated bus based communication, carrier detection, interference detection, and collision consensus enforcement with random binary exponential backoff. **Code & Pictures**.

Verilog RISC-V Processor Design (ECE 475/575 Project) Jan 2025 - Apr 2025

- **Iterative Multiplier/Divider:** implemented a 32-bit iterative multiplier and divider in Verilog with FSM-based controllers, completed operations in 33 cycles using valid/ready handshaking, wrote 40+ custom tests to validated edge cases.
- **Pipelined Processor with Bypassing & Mul/Div Unit:** updated 5-stage pipelined RISC-V processor to support bypassing and a 4-cycle pipelined mul/div unit by extending the pipeline to 7 stages, achieved 6x speedup on complex multiplication benchmark (16.8k to 2.55k cycles) and 2.5x on masked-filter benchmark (15.8k to 4.9k cycles) compared to stall-only baseline.
- **Superscalar Processor:** designed a 2-issue in-order superscalar RISC-V processor, verified correctness with custom test suites (non-ALU dual issue, WAW hazards, SW-LW bypass), achieved IPC up to 0.96.
- **Out-of-Order (OOO) Execution with Reorder Buffer:** equipped an OOO core with in-order commit by designing and integrating a Reorder Buffer (ROB) with bypass support, created custom OOO test programs (ROB ordering, bypassing, WAW hazards).

TEACHING EXPERIENCE

Undergraduate Course Assistant, **Princeton Engineering**, Princeton, NJ Feb 2024 - Present

- **ECE 206**: Digital Logic Design (Fall 2024, Fall 2025), **ECE 203**: Circuit Design (Spring 2025), **ECE 201**: Signals & Systems (Spring 2025), **COS 226**: Algorithms & Data Structures (Fall 2024), **EGR 153**: Engineering Physics: Electricity, Magnetism, & Photonics (Spring 2024).

ADDITIONAL TECHNICAL WORK & PROJECT EXPERIENCE

Power Electronics Intern, **Princeton Satellite Systems**, Plainsboro, NJ — Jan 2025

- Assembled and tested 5 PCBs of Class E Power Amplifiers for RF plasma heating and nuclear fusion (funded by DOE, ARPA-E).
- Simulated amplifiers in QSPICE, using MATLAB functions for component sizing, and tested 9 component combinations per board (including several hand-wound inductors) to improve efficiencies at different voltages by ~6 to 12%.
- Adapted Python code to interface Raspberry Pi with clock generator board to feed 4+ PWM signals into Class E boards. **Internship Summary Blog Post**. **Received option to return.**

Electrical Engineering Intern, **Lutron Electronics**, Boynton Beach, FL — May 2024 - Aug 2024

- Wrote Python scripts to generate 500+ distinct 240 V line voltage waveforms and conducted 500+ experimental trials measuring LED light output using a hand-built flicker meter.
- Designed an analog circuit to convert high-voltage waveforms into low-voltage microprocessor inputs without data loss for integration into a new dimmer. Presented 3 design reviews to senior engineers/managers with prompt follow-up analysis. **Received return offer.**

Energy Management Intern, **NextEra Analytics (NextEra Energy)**, St. Paul, MN — Jun 2023 - Aug 2023

- Used predictive backcasting models on electricity price data to analyze/visualize optimal battery storage (BESS) siting and operation in untapped grid regions, built a dashboard comparing market values across northeastern US hubs.
- Streamlined the data analysis workflow by consolidating scripts, saving 2+ hours per electricity hub.
- Presented 3 design reviews to senior engineers, managers, VPs, and NextEra Analytics President. **Received return offer.**

Research Assistant, **Princeton Center on Science and Technology (CST)**, Princeton, NJ — Oct 2022 - May 2023

- Assisted ***Professor Vivian Feng*** (unrelated) to design and test spectroscopy instruments using LEGOs and microcontrollers, varying automation (servo-driven, manual tuning) and accessibility (iPhone camera, photodetector sensors) for a future course offering.

LANGUAGE RELATED SERVICES & LEADERSHIP

Volunteer Freelance Translator, **Various Nonprofits/NGOs**, Remote — Jan 2023 - Present

- **Caminos de Agua** (Mexico): Proofread and revise translations of outreach materials (Spanish to English). — Nov 2023 - Present
- **Community Bots** (US & Latin America): Translated 332 slides of Python and robotics curriculum (English to Spanish). — Jan 2024
- **Disability Rights Maryland** (US): Translated pamphlet about parents' rights at psychiatric centers (English to Spanish). — Aug 2023
- **Pilares** (Argentina): Translated volunteer manual (Spanish to English). — Jan 2023 - Feb 2023

Co-President, **Princeton University Language Project** — Jan 2023 - May 2024

- Restarted the previously dormant club, recruited ~35 members, and secured $575 in funding to host two social/recruitment events.
- Oversaw 6 translation teams, communicated with nonprofits to coordinate translation projects.
- Updated website, designed and published Instagram posts and promotional materials for the club.
- Partnered with Princeton Translator in Residence to create a translation discussion event for students.
- Led the Spanish team in the translation of a wildlife book purchasable on Amazon: **Seres Silvestres**.

Independent Translation of *El sueño y otros relatos* by Donato Ndongo — Jun 2023 - Sep 2023

- Awarded $2000 in funding from **Princeton Translation Department** to translate a book from Spanish to English.

VOLUNTEER ACTIVITIES, OUTREACH, & HOBBIES

Radio DJ, **WPRB 103.3 FM**, Princeton, NJ — Jan 2023 - Present

- Curate music for and host weekly 3 hour rock and metal radio show with an FM broadcast range spanning four states.
- Interact with online listeners keeping the spirit of freeform independent radio programming alive!
- Current show: “Pit Stop”. Previous shows: “Shock Wave” (Summer 2024, Fall 2024, Spring 2025), “Lost in Orbit” (Spring 2023).

Executive Board & Event Supervisor, **Princeton University Science Olympiad**, Princeton, NJ — Oct 2022 - Present

- Communications and outreach team member for annual competition (750+ high school competitors). Previously organized all event logistics, testwriting, and materials sourcing for 23 science and technology related events for 2 years as Content Director.
- Event Supervisor (test writer, grader, lab setup, event planner and director) for Robot Tour. Previous Event Supervisor for Bridge and Detector Building. Totaling **11 years** with Science Olympiad, first as a competitor and captain (7 years) and now organizer (4 years).

Event Supervisor, **New Jersey Science Olympiad State Tournament**, Edison, NJ — Mar 2023

- Ran Detector Building competition event for ~25 high school teams (50 competitors): wrote, proctored, and graded a test about force sensors and electronics. Evaluated and graded student-created sensors/detectors (weight scales).

SKILLS & LANGUAGES

- **Programming Languages:** Verilog, Java, Python, C/C++, ARMv8 Assembly, Tcl. Learning SystemVerilog (UVM), CUDA, CUDA-Q.
- **Tools:** Cadence (Virtuoso, Spectre, Genus, Innovus, Tempus, Xcelium, Flowtool), Synopsys (HSPICE, Nanosim), SPICE (LTSpice, QSPICE, PLECS), Linux/Unix, Emacs, GDB, Git, gem5.
- **Technical Skills:** Digital Design, RTL Design, CPU & Computer Architecture (ISA, High-Performance Processor Organization, Pipelining, Superscalars, Vector Processors, Branch Prediction, RISC-V, CISC, SIMD, MIMD, VLIW, x86, Arm), VLSI Design (Synthesis, Place and Route, Layout, Schematic Design/Simulation, STA, DRC, LVS), Hardware Security, Quantum Computing, Scripting, Soldering.
- **Foreign Languages:** Spanish (advanced), Portuguese (proficient), Mandarin Chinese (conversational).