cadence™

Autorouting with Allegro® PCB Editor Tutorial

Series L and XL

Product Version 16.01
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Contents

Introduction

This chapter discusses the following:

Purpose of This Tutorial

This tutorial provides lessons and sample design files to help new users learn how to autoroute a design in the Allegro PCB Editor. The goal of this tutorial is to plan, prepare, and route a design. You also learn to analyze the routing results and perform basic post-routing operations.

This tutorial was created in Release 15.1 and has been regularly updated to be in synch with the most current release. You should expect to spend approximately sixteen hours to complete the lessons in this tutorial.

The tutorial contains these modules:

Audience

This tutorial can help train new users who need to autoroute a design, or can serve as a “refresher” course for infrequent users.

To successfully route boards, you need a basic knowledge of electronic design and printed circuit board layout in the Allegro PCB Editor.

Routing a board is both a science and an art. If you are not experienced in routing designs, you may use the garroting feature to route the design. You will achieve quick results without having to learn complicated tasks such as managing do files or iterative rounds of cleansing, etching, and ripping. As you gain experience in routing designs, you will realize the power of the PCB Router and start performing routing like a proficient user.

You will find this tutorial useful to:

- prepare a design for routing
- use different ways to route a design
- perform basic post-routing follow-up steps

To perform all exercises in this tutorial, you need the following Cadence tools:

- PCB Editor
- PCB Router
- Allegro Constraint Manager

Note: It is recommended that you use the Allegro PCB Design HDL XL product suite to run this tutorial.

What is not within the scope of this tutorial?

This tutorial does not cover using the PCB Router graphic user interface (GUI) or routing capabilities of the PCB Editor, such as interactive etch editing.

Note: For more information about using the PCB Router GUI, see the Cadence document *Allegro PCB Router Tutorial*.

How to Use This Tutorial

The training is offered in three learning modes:

- Written lessons provide detailed procedures for performing basic operations.
- Sample design files offer a starting point for practicing with the tools.

You can begin by reading through the written tutorial lessons. After completing each lesson. Then, work through the procedures yourself using the sample design files with the PCB Editor.

> **Note:** The exercises in this tutorial are built on a sample design and are progressive in nature. Follow the lessons in the sequence used in this tutorial. Skipping lessons might unsynchronize the design with the snapshots in the tutorial.

The written lessons and sample designs all work together to reinforce your learning experience. Use them in a way you find most conducive to learning.

Understanding the Sample Design Files

You can load the sample design files into PCB Editor and begin working with them immediately. The lessons use these same design files to illustrate the procedures. You can work with the design files as you progress through the lessons.

To use the design files, copy them to your system using the following instructions:

Windows 2000

Unzip the `aleg_spec_tut_db.zip` file located in the directory:

`<your_inst_dir>/doc/aleg_spec_tut/examples`

and extract it to an empty directory, for example `user_name`. On extracting the `aleg_spec_tut_db.zip` file, you will find a directory named `allegro`, which has 3 sub-directories–`project`, `solutions`, and `symbols`.

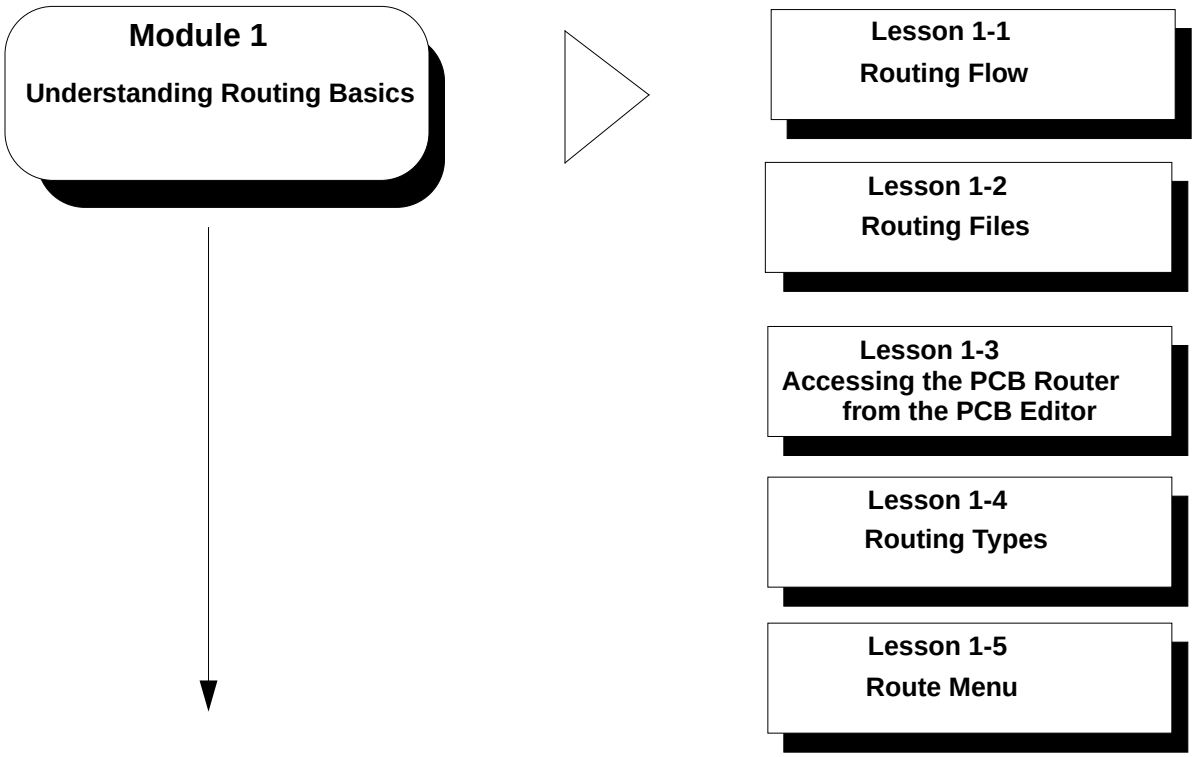
Note: For more information about the tutorial files, see **List of Sample Design Files**.

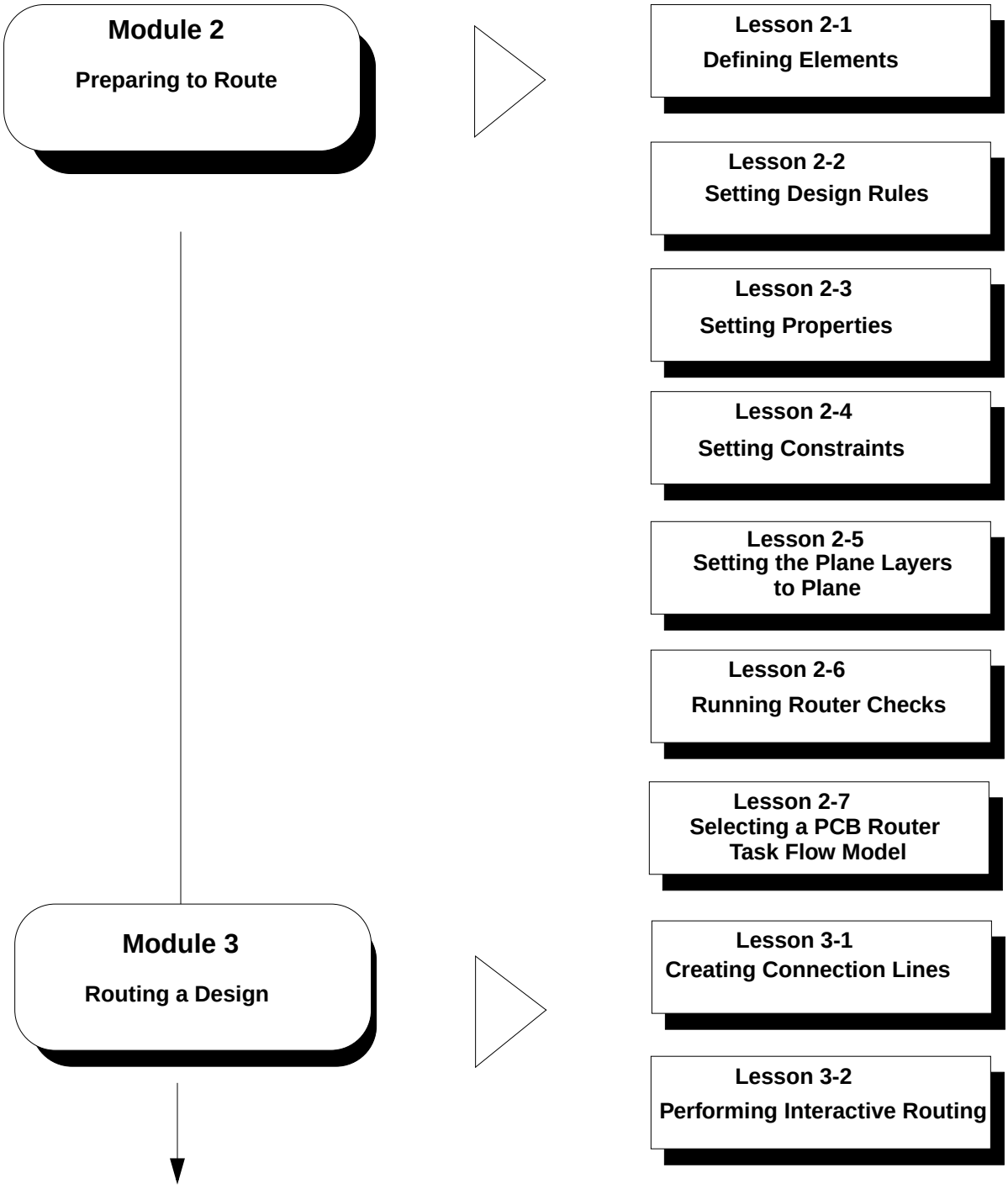
UNIX

Uncompress and untar the file `aleg_spec_tut_db.t.Z`, and extract the information to an empty directory, for example `user_name`. This directory serves as the demo directory for this tutorial.

Tutorial Flow

This tutorial consists of the modules and lessons shown in the following figure:




Module 2
Preparing to Route
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Defining Elements
Lesson 2-2
Setting Design Rules
Lesson 2-3
Setting Properties
Lesson 2-4
Setting Constraints
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Lesson 2-7
Selecting a PCB Router Task Flow Model
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Lesson 3-1
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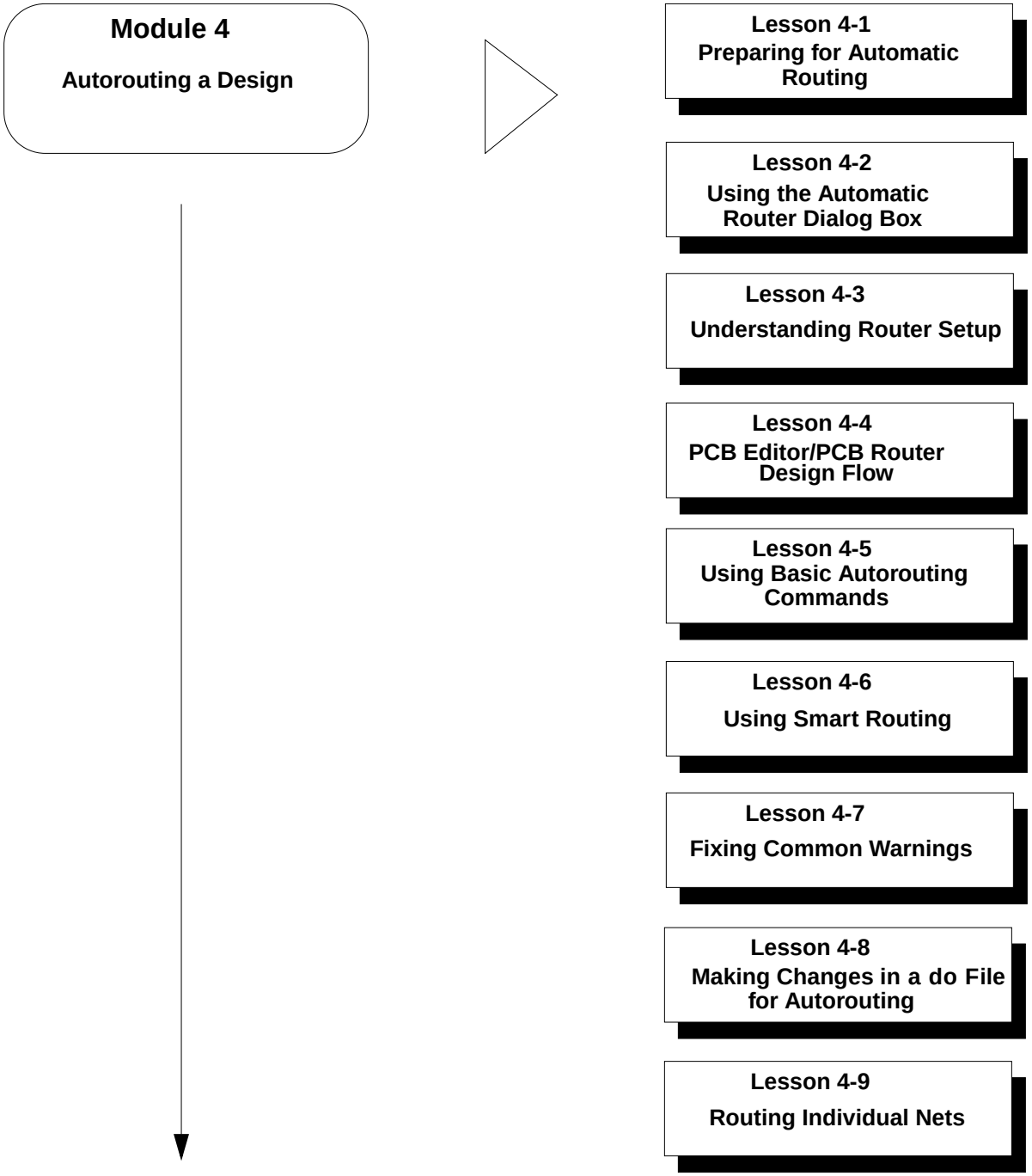
Performing Interactive Routing


Module 4
Autorouting a Design
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Preparing for Automatic Routing
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Lesson 4-3
Understanding Router Setup
Lesson 4-4
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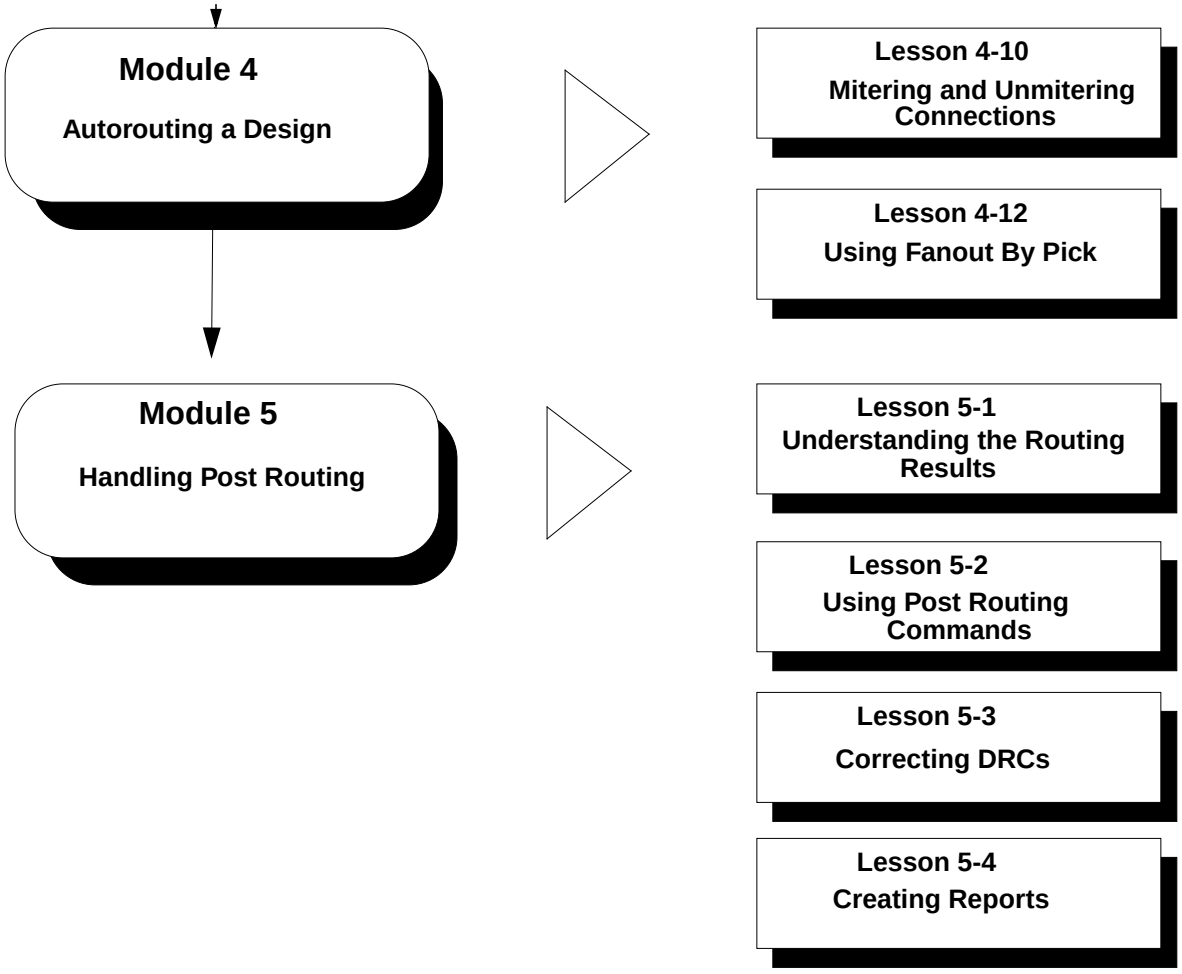
Using Basic Autorouting Commands
Lesson 4-6
Using Smart Routing
Lesson 4-7
Fixing Common Warnings
Lesson 4-8
Making Changes in a do File for Autorouting
Lesson 4-9
Routing Individual Nets



Related Information

You can obtain additional information about how to use PCB Design HDL from the following online manuals. You can access these manuals from the Help Systems page of the individual tools.

- *Getting Started with Allegro PCB Design HDL L*
- *Allegro Front-to-Back User Guide*
- *Allegro Design Entry HDL Tutorial*
- *Allegro Design Entry HDL User Guide*
- *Allegro Design Entry HDL Libraries Reference*

- *Allegro PCB Editor Tutorial*
- *Allegro PCB and Package User Guide*
- *Allegro PCB Router Command Reference*
- *Allegro PCB Router User Guide*
- *Allegro PCB Router Tutorial*
- *Allegro PCB Router Design Language Reference*

Note: At the end of each lesson, you will find hyperlinks to related sections of the *Allegro PCB and Package User Guides* and the *Allegro PCB and Package Physical Layout Command Reference*. You can also access these manuals from the PCB Editor Help Systems page.

Syntax Conventions

This list describes the syntax conventions used in this tutorial.

`literal`	Key words that you must enter literally. These keywords represent commands (functions, routines) or option names.
Courier font	Command line examples.
UI	Menus, labels, fields, or tabs in the user interface.
`variable`	Arguments for which you must substitute a value.

1

Module 1: Understanding Routing Basics

This module consists of the following lessons:

Completion Time

1 hour

Lesson 1-1: Routing Flow

Overview

In this lesson, you will learn the main steps in routing a design. Assuming that a netlist is available, the routing flow consists of 3 primary steps:

1. **Pre-routing**—Define different design objects and assign properties and constraints.
2. **Routing**—Perform a combination of manual and automatic routing. You need to understand different options and methodologies for routing a design and how different routing parameters impact autorouting.

3. **Post-routing**—Review routing results and make iterative changes to optimize results.

Concept

The steps that you use while routing a design change based on:

- the nature of your design
- your experience (and thereby preferences)

As a new user learning to route a design, you may get best results using the Autorouter from within the PCB Editor. The following basic routing flow is recommended:

1. Prepare for routing
   - Check layers to see that layer types and photo film types are correct.
   - Create internal shapes on planes.
   - Create blind and buried vias.
   - Set routing rules (such as routing areas, constraints and properties, grids, and nets).
2. Manually route critical nets.
3. Define routing parameters in the PCB Router to control how automatic routing functions.
4. Perform routing in the PCB Router.
5. Review routing results.
6. Interactively finish or correct etch.
7. Gloss the design.
8. (Optional) Analyze the design for signal integrity or EMI.

Summary

You can route a design any time after placement is completed. Quality routing involves proper preparation, selecting relevant routing parameters, and effective post-routing clean-up and glossing.

For More Information

See Cadence document Allegro PCB and Package User Guide: Routing the Design.

Lesson 1-2: Routing Files

Overview

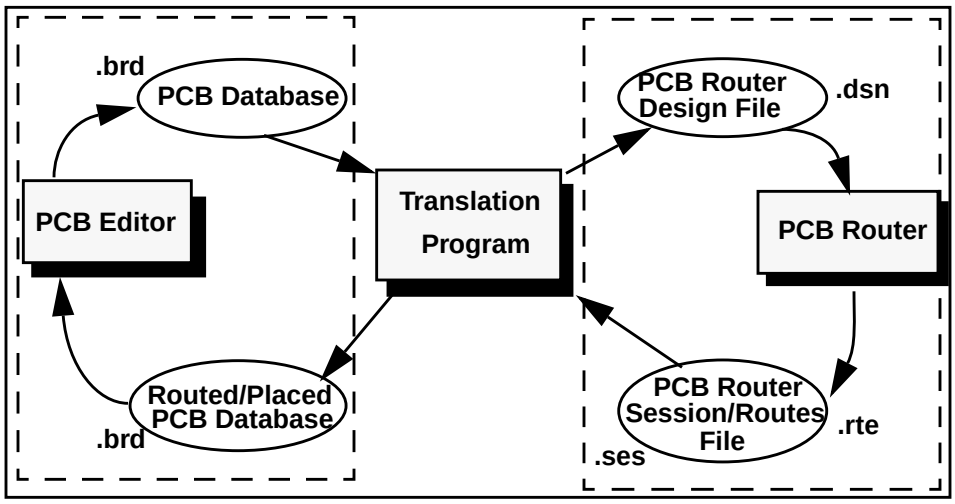
In this lesson, you will learn the functions of different files required or generated in the routing process. You will analyze how data flows between these files.

Role of Autorouter in the PCB Design Process

The PCB Router extends your PCB CAD system by adding automatic and interactive placement and routing tools. You use the PCB Router to place components and route your printed circuit board design.

After you create a PCB database in your layout system, you translate the design data to a PCB Router Design file. You place and route the design in the PCB Router, save the results, and then merge the placement and routing data with your original PCB database.

Figure 1-1 The Autorouter in the PCB Design Process



You transfer your printed circuit board design between the PCB Router and the PCB Editor by translating the design data from one format to the other. All files that are read and written by the PCB Router are text files.

Key Routing Files

The following files play an important role in the routing process:

- Design file
- Do file
- Session file
- Wires file
- Placement file
- Routes file

Design File

A design file (`.dsn`) contains design data generated by the PCB Editor. It includes complete information about components, connectivity (netlist) and design constraints. This file serves as the starting point for all work in the PCB Router.

Do File

A `do` file is a text file that contains a list of Autorouter commands. It is a script that controls the Autorouter. Efficient use of `do` files:

- Simplifies your work life
- Fosters productivity
- Avoids redundant activities

Following is an example of a `do` file.

```
# Lines beginning with '#' are comments
# Initial Commands
status file route.sts
# This is where you place prerouting commands:
```

```
unit mil
rule pcb (clearance 10)
# Standard Routing Commands
smart_route
```

The order of commands in a `do` file is important because the Autorouter executes each command *sequentially*. For example, you may not route the design before you set rules, such as clearance and width rules, that you need the Autorouter to follow.

Session File

A session file (`.ses`) contains design data generated by the PCB Router. It includes a nearly complete record of all commands and activities that were executed during a design session.

Wires File

A wires file (`.w`) includes wire and via information that you saved from a previous PCB Router session.

Placement File

A placement file (`.plc`) contains design data generated by the PCB Router. It includes information about component placement, such as x,y coordinate location, rotation, and layer association. To create placement data in the PCB Router, first read in a design file generated from the PCB Editor.

Routes File

A routes file (`.rte`) contains design data generated by the PCB Router. It includes information about wiring that has been routed in the PCB Router. To create routing data in the PCB Router, first read in a design file generated from the PCB Editor.

Did File

A `did` file captures all the commands you enter at the command line, read in from a `do` file, or execute from the text menu and icons. When

you invoke the PCB Router, it automatically starts recording all your commands in a did file named `MMddhhmm.did` where `MM` is the number of the current month, `dd` is the date of the current month, `hh` is the hour and `mm` is the minute that the PCB Router session was invoked.

Summary

The PCB Router is tightly integrated with the PCB Editor. The board file from the PCB Editor is converted to a PCB Router Design file by a translator. The PCB Router may also use `do`, `did`, `routes`, and `session` files in conjunction with the design file to complete autorouting. The PCB Editor captures routing commands entered at the command line in a did file. You can create your own routing command-line script in a `do` file and use it to run the PCB Router in a batch mode.

Lesson 1-3: Accessing the PCB Router from the PCB Editor

Overview

In this lesson, you will learn to use the PCB Router from the PCB Editor.

Launching the PCB Router from the PCB Editor

You can use the PCB Router from the PCB Editor by:

- Creating a `dsn` file and using it in the PCB Router
- Using the Automatic Router dialog box
- Using the PCB Router Editor

Procedure

Creating a .dsn file

1. Open the `placed.brd` file in the PCB Editor.

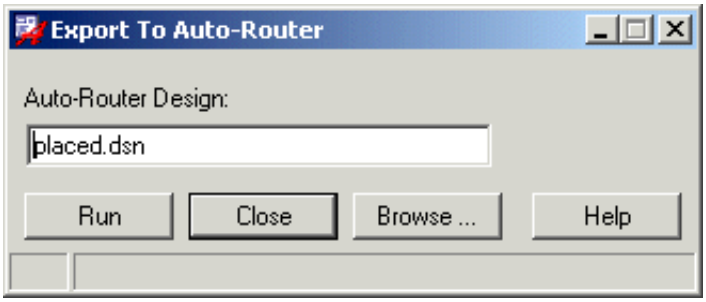
   Note: The `placed.brd` file is available in the `physical` folder under the `root` design. For more information about copying the source files in your computer, see `List of Sample Design Files` on page 180.

2. Choose *File – Export – Router.*

   Or

   Type `specctra_out` in the Console Window and press `Enter`.

   The Export to Auto-Router dialog box appears.



   Notice that the default name of the dsn file is the same as the name of the board file. The dsn file is saved in the `physical` folder (just as the PCB Editor board file). To change the folder location, click *Browse* and specify the alternate location.

3. Click *Run* to generate the design file for the PCB Router.

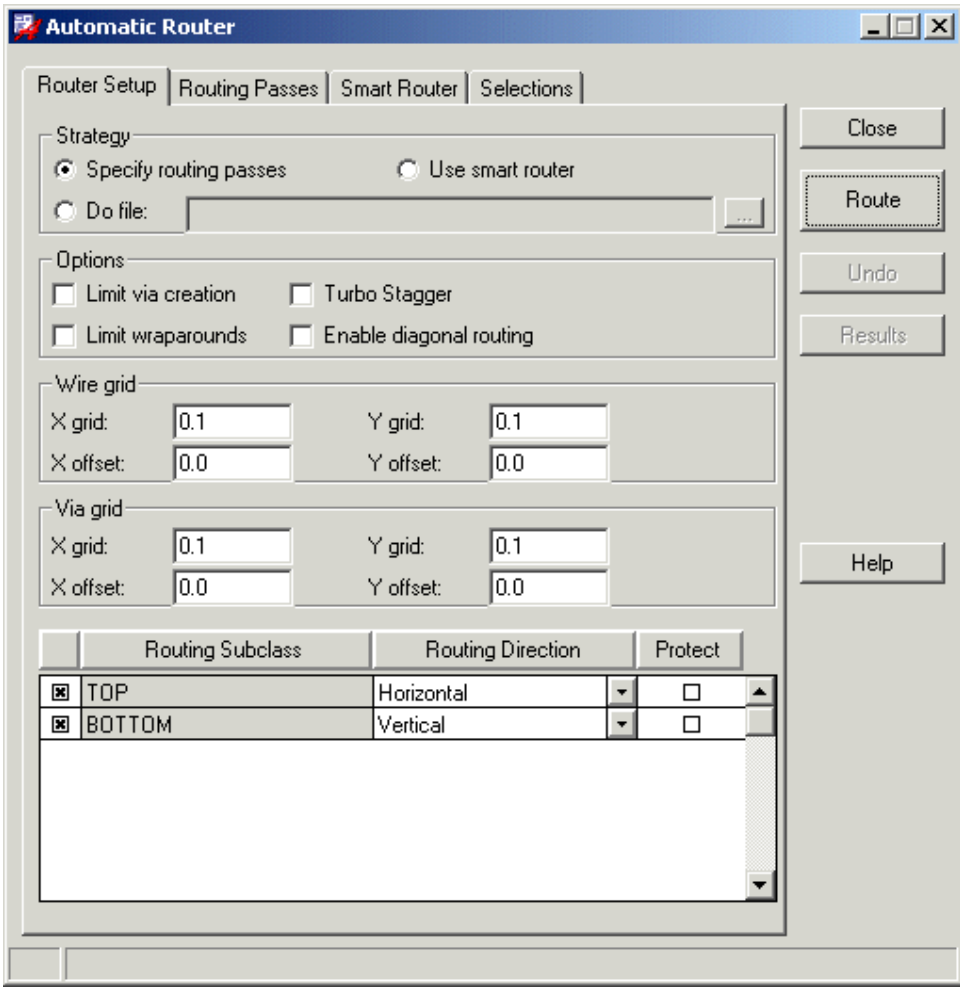
4. Click *Close* to close the Export to Auto-Router dialog box.

   The design file is created for the PCB Router. You can now open the PCB Router and load the `placed.dsn` file.

Using the Automatic Router dialog box

1. Choose *Route – Route Automatic.*

The Automatic Router dialog box appears.



You can use the Automatic Router dialog box to automatically route all or parts of your board file. Before using this dialog box, ensure that you have performed all pre-routing procedures, such as placement of the design. Module 2: Preparing to Route on page 35 covers some of these procedures. For more information about using the Automatic Router dialog box, see Lesson 4-2: Using the Automatic Router Dialog Box on page 96.

2. Click *Close* to close the Automatic Router dialog box.

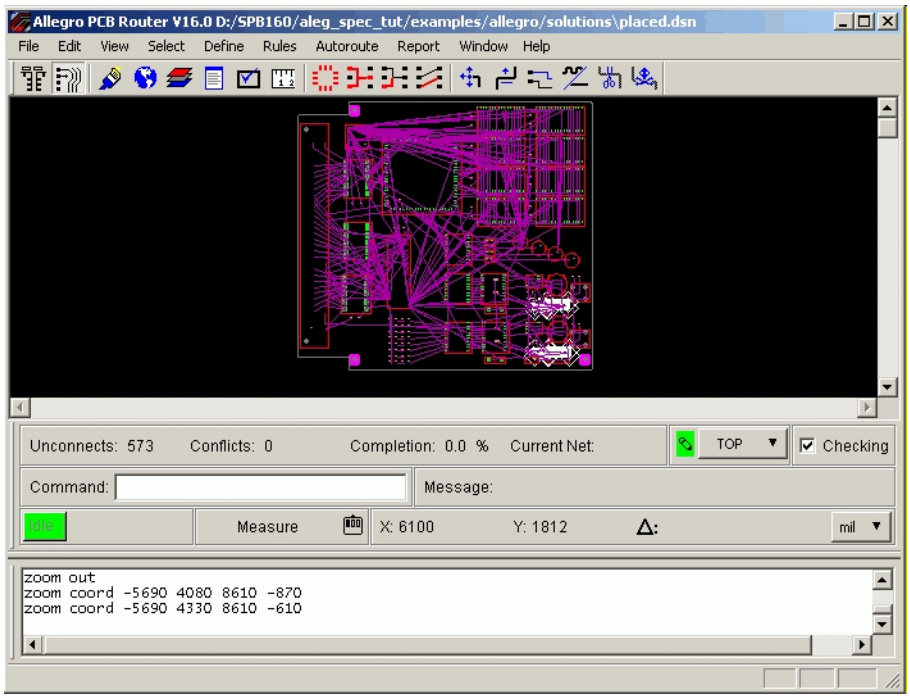
Note: For more information about how to use the Automatic Router dialog box to autoroute a design, click this link:

Using the PCB Router

1. Choose *Route – Route Editor.*

   The PCB Editor opens the dsn file corresponding to the board file in the PCB Router.

   The Allegro PCB Router GUI.



   Note: The remaining lessons in this tutorial will focus on using the PCB Router from the PCB Editor and will not use the PCB Router GUI. For more information about the PCB Editor GUI, see cadence document *Allegro PCB Router Tutorial.*

2. Click *File – Quit* to close the PCB Router.

   The Quit dialog box appears. You can choose to delete the `Did` file created for the current PCB Router session.

3. Click *Quit.*

Summary

You can use the PCB Router from the PCB Editor in multiple ways. To automatically route a complete design, use the Automatic Router dialog box. For interactive routing, you can use the PCB Editor GUI.

Lesson 1-4: Routing Types

Overview

In this lesson, you will identify the differences between automatic routing and interactive or manual routing.

Autorouting

The power of the PCB Router lies in automatically routing a design by specifying varying parameters. You can route all parts of a board or parts of the board. The following situations describe the commands you should use:

To do this...	... run this command
Automatically route the whole design	*Route – Route Automatic* See Lesson 4-2: Using the Automatic Router Dialog Box on page 96.
Route specific nets and/or components in the design rather than the entire database.	*Route – Net(s) By Pick* See Lesson 4-9: Routing Individual Nets on page 137.

When you run an automatic routing command, the following file types are generated from the design you are routing:

- Design file (`<filename>.dsn`) – Created from a `.brd` file and acts as a placeholder for the PCB Router.
- Rules file (`<filename>_rules.do`) – Contains design rules such as clearance, wiring, timing, cross-talk, and so on.

- Forget file (`<filename>_forget.do`) – Contains commands that let you forget specific rules defined in the rules file.

Interactive Routing

If you choose not to use the automatic routing feature, you can manually (or interactively) route the design.

Interactive routing lets you do the following:

- Connect two points, with or without vias
- Start a connection from a Rat T point
- Edit vertex
- Insert blind, buried, and through-hole vias
- Shove vias when adding clines
- Add, slide, or delete connections and vias
- Begin a connection and then run automatic routing to finish the etch/conductor for the pin-pair
- Route timing-sensitive circuits

Interactive routing features complement automatic routing features. You can use interactive routing to:

- Complete critical nets before automatic routing.
- Finish disconnects left after automatic routing.

Note: For more information about interactive routing, see Lesson 3-2: Performing Interactive Routing on page 82.

Summary

The choice between manual and automatic routing is often personal and dependent on the comfort level of a user. The PCB Router returns high quality autorouting results. You can optimize the results by modifying different routing parameters. You can perform interactive routing for specific cases, such as routing critical nets and finishing disconnects left after autorouting.

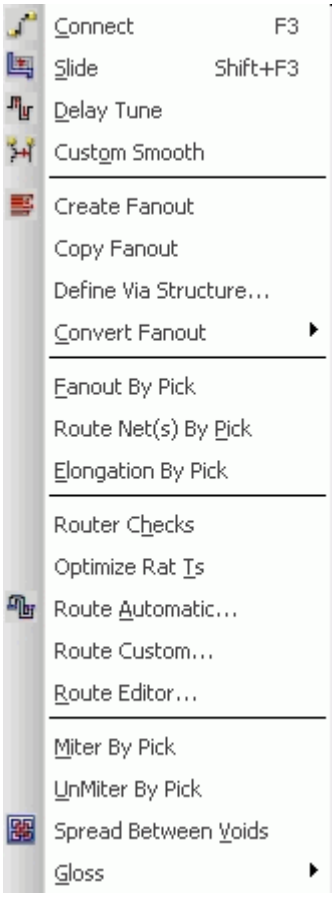
Lesson 1-5: Route Menu

Overview

In this lesson, you will identify the functions of different commands in the Route menu of the PCB Editor.

Route Menu

The PCB Editor has the following *Route* menu. Most of these commands a corresponding Toolbar icon. The *Route* menu commands also have a corresponding console command.



Connect `(add connect)`

The *Route – Connect* command lets you add connections to a design interactively. You can add etch/conductor interactively, before or after automatic routing.

Note: To learn different ways to add etch using the *Route - Connect* command, see Lesson 3-1: Creating Connection Lines on page 69.

Slide `(slide)`

The *Route – Slide* command lets you move or edit connect lines or vias interactively while maintaining their connectivity. When you use this command, you choose the element to move and then its destination. This command can be useful in post-autorouting cleaning and adjustment of connect lines.

Note: For more information about the `slide` command, see Lesson 3-2: Performing Interactive Routing on page 82.

Delay Tune `(delay tune)`

The *Route – Delay Tune* command helps you add or remove etch when fully connected nets violate delay constraints.

Note: This command is not available in PCB Design L.

Note: For more information about the `delay tune` command, see Lesson 3-2: Performing Interactive Routing on page 82.

Custom Smooth `(custom smooth)`

The *Route – Custom Smooth* command optimizes selected clines or cline segments according to parameters set in the *Options* tab. Smoothing the angles of clines or cline segments can minimize the distance to pad connections. Use this command when you manually edit etch.

Note: For more information about the `custom smooth` command, see Lesson 5-2: Using Post Routing Commands on page 153.

Router Checks `(specctra_checks)`

The *Route – Router Checks* command lets you run router and alignment checks on the current design to identify routing problems prior to running the PCB Router. A window displays a log file with items that may not have a corresponding constraint in the PCB Router or that may otherwise cause the router to fail.

Note: For more information about performing router checks, see Lesson 2-6: Running Router Checks on page 60.

Fanout by Pick `(fanout_by_pick)`

The *Route – Fanout by Pick* command routes short pin escape wires from pins to vias. It lets you control pin and via sharing, set the layer depth, control the escape direction, and set a temporary via grid for this command to use.

Note: For more information about the `fanout_by_pick` command, see Lesson 4-11: Using Fanout By Pick on page 145.

Route Net(s) by Pick `(route_by_pick)`

The *Route – Net(s) by Pick* command lets you route specific nets and components in your design rather than the entire database. When you choose this command, the PCB Router is invoked in the background and a design (.dsn) file is created.

Note: For more information about the `route_by_pick` command, see Lesson 4-9: Routing Individual Nets on page 137.

Elongation by Pick `(elong_by_pick)`

The *Route – Elongation by Pick* command increases etch length. You may need this command to adhere to timing rules.

Note: For more information about the `elong_by_pick` command, see Lesson 4-3: Understanding Router Setup on page 106.

Route Automatic `(auto_route)`

The *Route – Route Automatic* command lets you automatically route all or parts of your .`brd` or .`mcm` file through the Automatic Router dialog box.

Note: For more information about the `auto_route` command, see Lesson 4-5: Using Basic Autorouting Commands on page 115.

Route Editor `(specctra)`

The *Route – Route Editor* command launches the PCB Router Editor.

Note: For more information about using the PCB Router interface, see the Cadence tutorial *Allegro PCB Router Tutorial.*

Miter by Pick `(miter_by_pick)`

The *Route – Miter by Pick* command lets you change 90-degree wire corners to 45 degrees for wires exiting pins and vias.

Note: For more information about the `miter_by_pick` command, see Lesson 4-10: Mitering and Unmitering Connections on page 142.

Unmiter By Pick `(unmiter_by_pick)`

The *Route – Unmiter by Pick* command lets you remove 45-degree wire corners and change them to 90-degree corners.

Note: For more information about the `unmiter_by_pick` commands, see Lesson 4-10: Mitering and Unmitering Connections on page 142.

Gloss `(gloss param)`

The *Route – Gloss* command lets you eliminate vias and straighten lines. This command opens the Glossing Controller dialog box from where you can start different glossing applications. You can also run glossing from this dialog box.

Note: For more information about the `gloss param` command, see Lesson 5-2: Using Post Routing Commands on page 153.

Summary

The Route menu lists all commonly used routing commands. These commands can let you perform interactive and automatic routing. Using these commands, you can have connection lines for all nets and change desired length, vertices, elongation or contraction to adhere to timing and design rules.

2

Module 2: Preparing to Route

This module consists of the following lessons:

Completion Time

- 2 hour for written lessons

Lesson 2-1: Placing Elements

Overview

In this lesson, you will learn the important steps involved in placing different elements in a design. You will learn to do the following:

- **Define route keepin**—A route keepin is an unfilled polygon that defines the area where etch/conductor is permitted. You can have only one route keepin in the PCB Editor. Etches and conductors are placed within DRC limits of the keepin. The PCB

Router ignores any connect points outside the route keepin. Connections may touch, but not cross, the route keepin.

- **Define placement keepout area**—Route keepouts are filled shapes (closed polygons) that you create to indicate areas of a design that may not contain etch/conductor objects. Etches and conductors may touch, but not enter a keepout area. The automatic router does not add etches or conductors inside a route keepout. You may like to add route keepout around the mechanical parts, such as connectors or heat sinks in a layout.

Concept

Component placement using the PCB Editor typically involves the following activities:

- Determining design requirements
- Creating the items required for placement processing (such as grids or package or part keepin areas)
- Setting basic placement controls, such as package/part keepin and keepout areas, placement properties, and automatic placement parameters
- Running manual placement alternately with automatic placement. You can run different iterations of automatic placement and view the placement results.
- Reviewing placement status and automatic placement results
- Swapping pins, gates, and parts as necessary

Note: Element placement is a comprehensive subject and outside the scope of this tutorial. For more information about placing design elements, see the Cadence document *Allegro® PCB and Package User Guide: Placing the Elements*.

You will learn to create route keepin and couplets in this lesson. These exercises emphasize the important placement requirements for successful routing of a design. You create keepin and keepout areas while creating mechanical board symbol.

Important

While you have option to include keepin areas for wires, vise, and packages, the route keepin are a MUST for the design.

Procedure

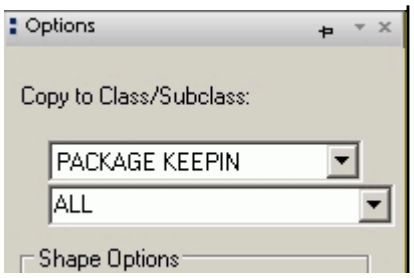
Defining Package and Route Keepin

1. Open the `unplaced.brd` file in the PCB Editor.
2. Click the *Zoom Fit* icon  to view the entire board.
3. Choose *Edit – Z-Copy*.

   The following message prompts in the command window:

   ```
   Enter Selection Point
   ```

4. Choose the *Options* tab and set the *Active Class* and *Subclass* to `PACKAGE KEEPIN` and `ALL`.



5. In the *Shape Options* box, set *Offset* as `60` and size to *Contract*.
6. Select any point on the board outline.

   The message window prompts:

   ```
   Copied to: ("Package Keepin/All"), 1 copies made
   ```

   A package keepin is drawn 60 mils inside the boundary of the board outline. All components are placed within this area.

7. Set the *Active Class* and *Subclass* to `ROUTE KEEPIN` and `ALL`.

8. In the *Shape Options* box, set *Offset* as `50` and size to *Contract*.
9. Select any point on the board outline.

   The message window prompts:

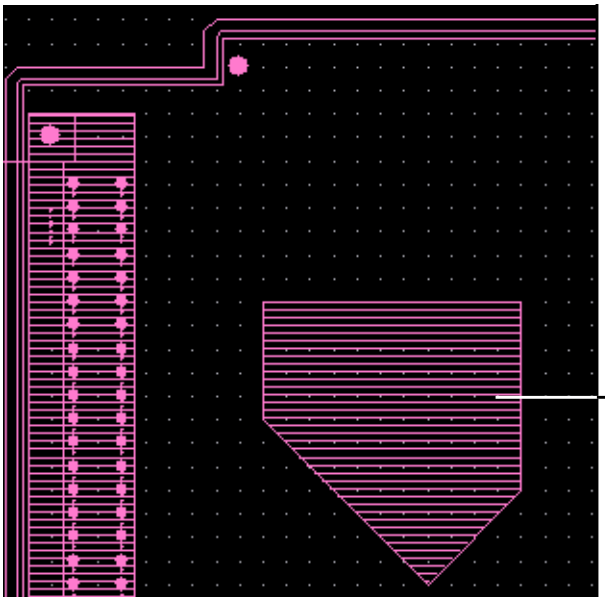
   ```
   Copied to: ("Route Keepin/All"), 1 copies made
   ```

   A route keepin is drawn 60 mils inside the boundary of the board outline. All routing is done within this area.
10. Choose *File – Save As*.
11. Type `keepin.brd` as the file name and press `Enter`.

Defining Placement Keepout Areas

Note: This exercise is for demonstration only. You will create a route keepout and package keepout in the board file you used in last exercise and then delete them.

1. Choose *Setup – Areas – Package Keepout*.
2. Set *Segment Type* in the *Options* tab to *Line.*
3. Click anywhere inside the board to define the polygon. Start from the first corner and draw a line. Click at each corner to define a vertex. To close the polygon, connect the last corner to the first corner.



When the polygon is closed, it is automatically filled.

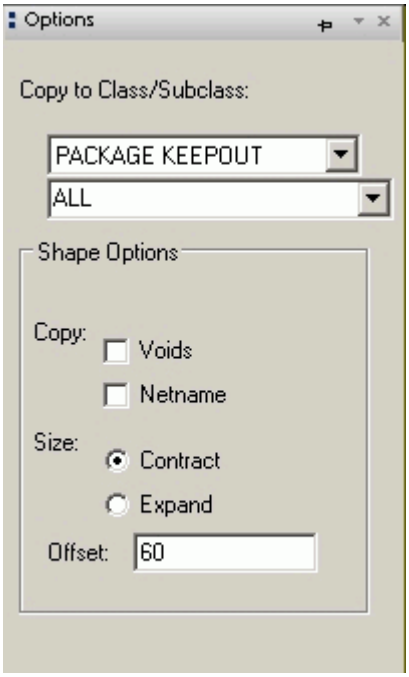
4. Right-click and select *Done* from the pop-up menu to finish making changes to the package keepout. You will now create a route keepout area.

5. Zoom into the area around the mounting hole at the upper left corner of the board.

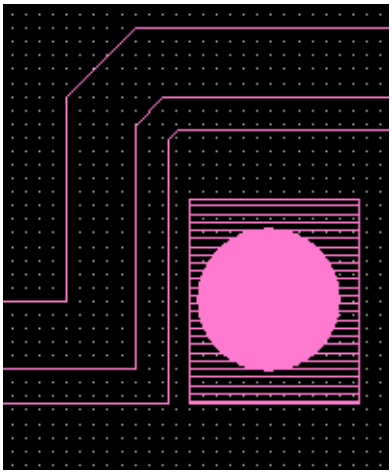
6. Choose *Setup – Areas – Route Keepout*.

   Notice that the active class and subclass change to *Route Keepout* and *All*.

   Ensure that the *Options* tab has the following settings:



Click towards the north-edge of the mounting hole and draw a rectangle as shown below:



7. Right-click and select *Done* from the pop-up menu to finish making changes to the route keepout.

   The route keepout is visible. No routing will be permitted within this area.

8. Close the PCB Editor without saving the file.

Summary

You learned to define keepin and keepout areas in a layout. These areas ensure that the Autorouter does not step outside the defined limits or inside the restricted limits while placing etches or conductors.

Note: If you have not defined a route keepin or a package keepin for a layout, the *Route - Router Checks* command displays a warning.

For more information about fixing different warnings generated by the the *Route - Router Checks* command, see Lesson 4-7: Fixing Common Warnings on page 123.

Lesson 2-2: Setting Design Rules

Overview

In this lesson, you will learn to set design rules for a design.

Concept

As part of preparation for layout, you should set up design rules. The PCB Editor performs Design Rule Checking (DRC) to ensure that the design conforms to specified properties and constraints you attach to individual design elements or assign globally to the entire design.

The PCB Editor has a set of predefined rules, such as Line-to-Pin Spacing or Minimum Line Width. You can define values for each rule within the context of a rule set. A rule set is a group of rules that have been bundled together to make value assignments easier for the user.

There are four types of design rules:

- **Spacing Rule Set**—These constraints govern the spacing between objects on different nets (for example, line-to-thru-pin spacing).
- **Physical Rule Set**—These constraints govern physical construction of a net (for example, minimum line width and allowed etch layers).
- **Design Constraints**—These constraints govern setting or clearing of package DRC checking. Negative Plane Islands constraints and solder mask constraints also fall in this category.
- **Electrical Constraint Sets**—These constraints govern electrical behavior and performance of an entire net (for example, maximum propagation delay).

Design rules can be specified at different levels and consequently form a hierarchy. Rules at higher levels in the hierarchy override rules at lower levels that are set for the same physical objects. For example, consider what happens if you set a global (PCB) spacing rule of .25 inches for all components and a spacing rule of .8 inches for a specific connector. The PCB Router follows the .8 spacing rule

only in the area surrounding the connector. The PCB Router follows the .25 spacing rule in the areas surrounding other components.

➤ Choose *Setup – Constraints – Constraint Manager*.

or

Select the *Cmgr* icon  .

Procedure

Defining Constraints

You define Electrical, Spacing, and Physical constraints in Constraint Manager.

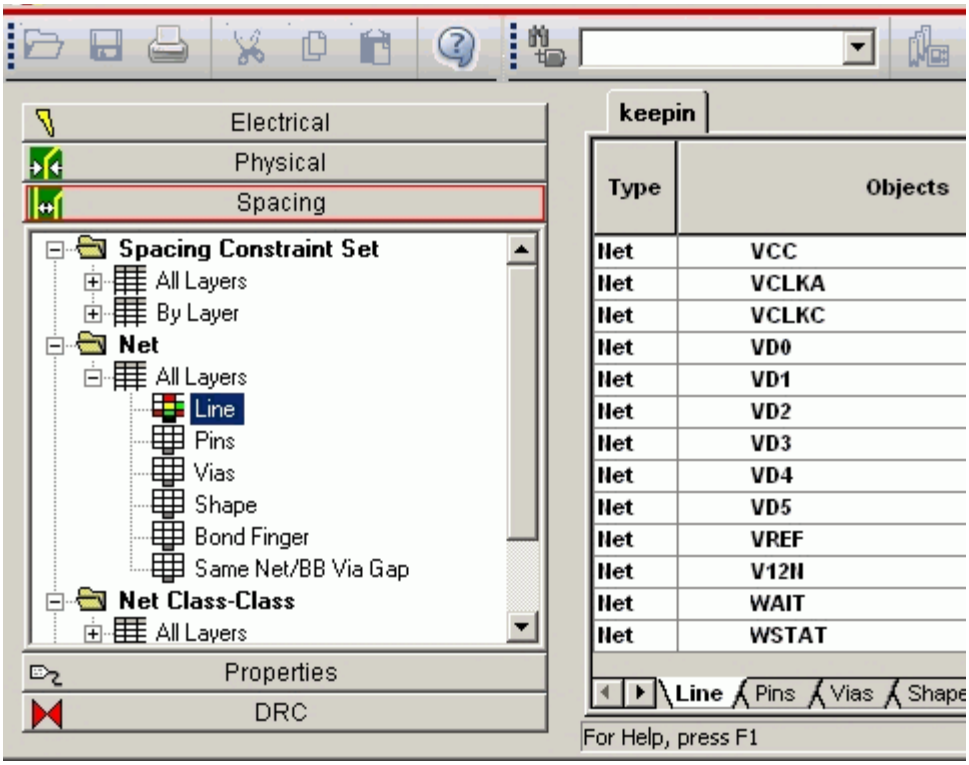
To launch Constraint Manager:

1. Open the `keepin.brd` file in the PCB Editor.
2. Choose *Setup – Constraints – Constraint Manager*.

Creating a Spacing Net Class

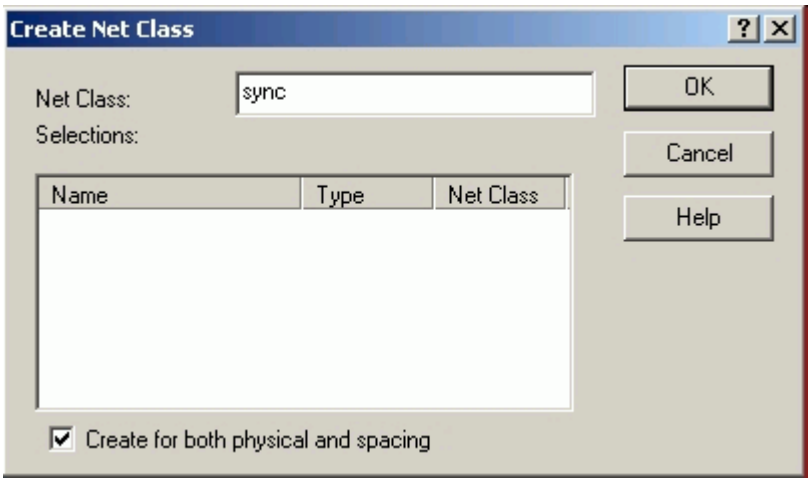
In this exercise, you will set design rules on a net-by-net or layer-by-layer basis for two nets `wait` and `wstat` in the *Spacing* tab of Constraints Manager.

1. Select the *Cmgr* icon  .



2. Choose *Objects – Create – Net Class*.

3. Type sync as the name for the Net Spacing class in the *Net Class* field.

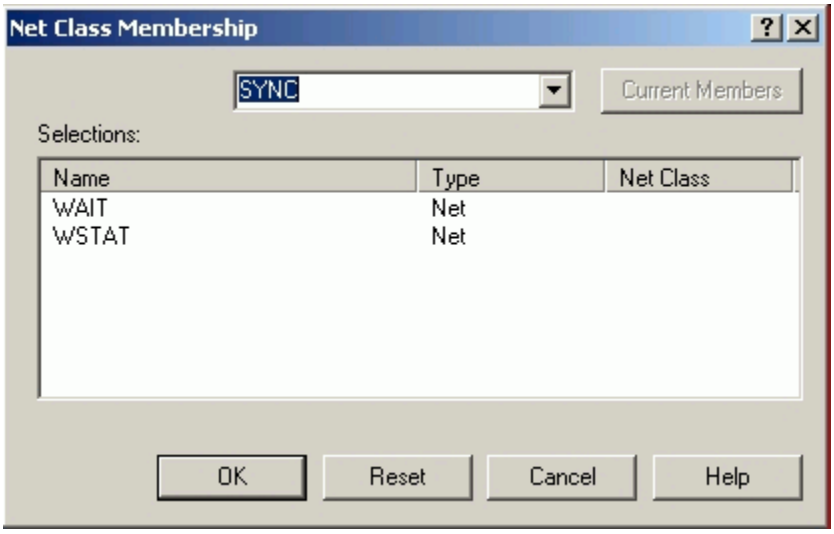


4. Click *OK*.

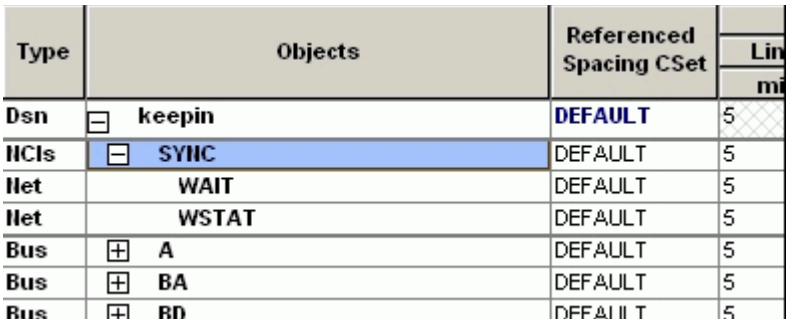
The Net Spacing class, *SYNC*, is created.

Type	Objects	Referenced Spacing CSet	Lin mi
Dsn	⊟ keepin	DEFAULT	5
NCls	SYNC	DEFAULT	5
Bus	⊞ A	DEFAULT	5
Bus	⊞ BA	DEFAULT	5
Bus	⊞ BD	DEFAULT	5
Bus	⊞ D	DEFAULT	5
Bus	⊞ RA	DEFAULT	5
Bus	⊞ RD	DEFAULT	5
DPr	⊞ DP1	DEFAULT	5
Net	AEN	DEFAULT	5
Net	AGND	DEFAULT	5

5. Click the *Line* worksheet under *Net—Layers*.
6. Browse to and select nets *WAIT* and *WSTAT*.
7. Right-click and choose *Membership – Net Class* from the pop-up menu.
8. Select *SYNC* in the Net Class membership dialog box.



9. Click *OK*.

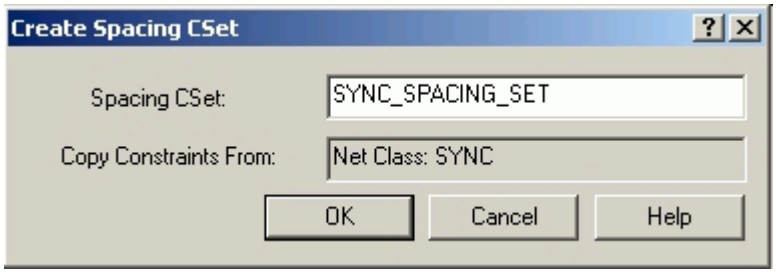


You have created a Spacing Net class called `sync`. Both the nets `wait` and `wstat` are members of this class. If you need to assign special clearance to more nets later on, add them to this net class.

Creating a Spacing CSet

You can create a Spacing CSet (Spacing rules) in the *Spacing* tab of Constraint Manager.

1. Click the *Line* worksheet under *Net—Layers*.
2. Right-click the Net class *SYNC* and choose *Create – Spacing CSet* from the pop-up menu.
3. Type *SYNC_SPACING_SET* in the Spacing CSet field.



4. Click *OK*.

5. Click *Line* under *Spacing Constraint Set—All Layers*.

Type	Objects	Line	Thru Pin	SMD Pi
		mil	mil	mil
Dsn	⊟ keepin	5	5	5
SCS	⊟ DEFAULT	5	5	5
Lyr	TOP	5	5	5
Lyr	GND	5	5	5
Lyr	VCC	5	5	5
Lyr	BOTTOM	5	5	5
SCS	⊞ SYNC_SPACING_SET	5	5	5

   The Spacing CSet is created.

6. Change the value of Line to `6 mil`.
7. Click the *Line* worksheet under *Net—Layers*.
8. Click in the *Referenced Spacing CSet* column next to the Net class *SYNC*.
9. Select *SYNC_SPACING_SET*.
10. Notice the value of Line is changed from the default value of `5 mil` to `6 mil` as specified in the CSet.

Type	Objects	Referenced Spacing CSet	Line	Thr
			mil	n
Dsn	⊟ keepin	DEFAULT	5	5
NCls	⊟ SYNC	SYNC_SPACING_SET	6	5
Net	WAIT	SYNC_SPACING_SET	6	5
Net	WSTAT	SYNC_SPACING_SET	6	5
Bus	⊞ A	DEFAULT	5	5
Bus	⊞ BA	DEFAULT	5	6
Bus	⊞ BD	DEFAULT	5	5
Bus	⊞ D	DEFAULT	5	5
Bus	⊞ BA	DEFAULT	5	5

For more details, see the *Constraint Manager Reference* guide.

Summary

To set a Spacing rule, first create a Net class in Constraint Manager and then assign objects to the class. You can then create a Spacing CSet and assign the CSet to the Net class.

Exercise

The procedure for creating a physical rule set is the same as the procedure for creating a spacing rule set. Using the information presented in this lesson:

1. Create a physical net class `sync` in the Physical tab of Constraint Manager. Then, add the nets `wait` and `wstat` in the `rule_set.brd` file you created in the last exercise.
2. Define a Physical CSet named `16_mil_space` that has a minimum line width and minimum neck width of 16 mil each.
3. Assign the `16_mil_space` Cset set to the net class `sync`.
4. Save the board file.

Note: In Lesson 4-5: Using Basic Autorouting Commands on page 115, you will see how the physical rule set you have defined influences routing results.

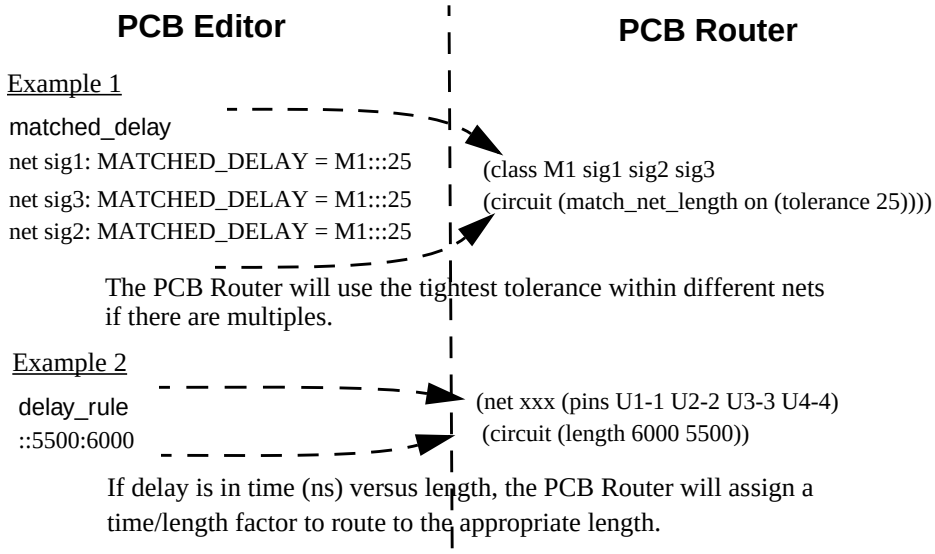
Lesson 2-3: Setting Properties

Overview

In this lesson, you will learn to set properties for a design.

You should add properties to components or nets that require any Autorouter processing. Most PCB Editor properties are translated into the PCB Router. However, some properties or rules may not get translated.

The following diagram shows examples of how properties are translated between the PCB Editor and the PCB Router:



In this lesson, you will learn to add the following properties on a net:

1. **FIXED**—This property prevents all automatic routines from changing a net. Once applied on a net, you cannot perform autorouting on the net.
2. **Differential pair**—This property represents a pair of nets or Xnets that will be routed in a way that the signals passing through them are opposite in sign with respect to the same reference. This ensures that any electromagnetic noise in the circuit is canceled out.

Note: You will learn how the above properties impact routing results later in this tutorial.

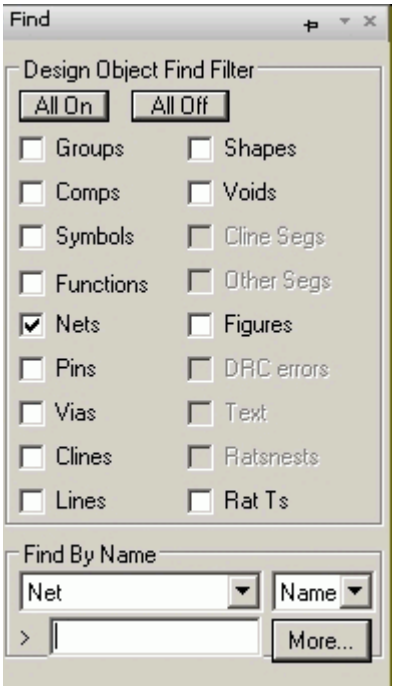
You can add properties to a net using the Edit Property dialog box. If you are adding an electrical property (for example, Differential Pair), you can add it by using Allegro Constraint Manager.

Procedure

Adding a Property Using the Edit Property Dialog Box

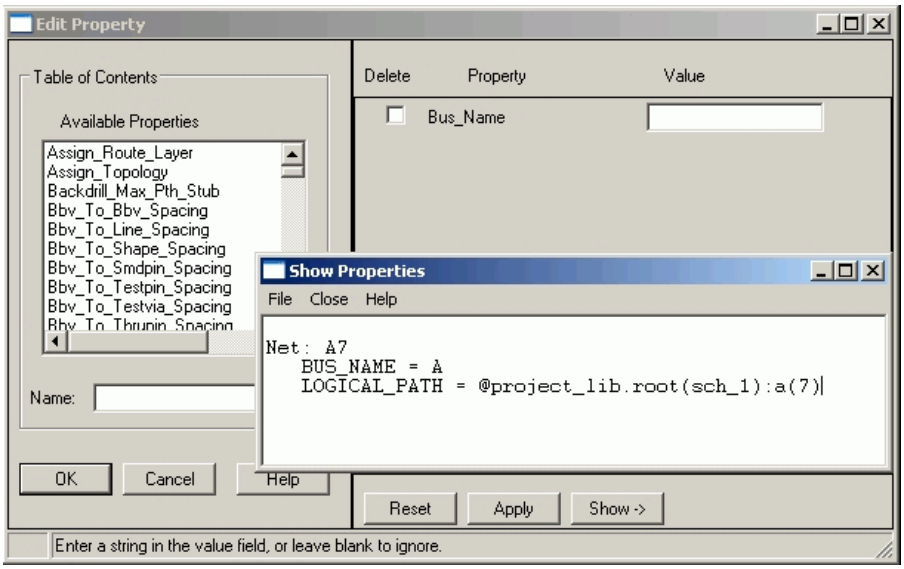
1. Open the `rule_set.brd` file in the PCB Editor.

2. Choose *Edit – Properties*.
3. Change the *Find* filter. First, choose *All Off*. Next, choose the *Nets* option.
4. In the *Find By Name* field, choose *Net*.



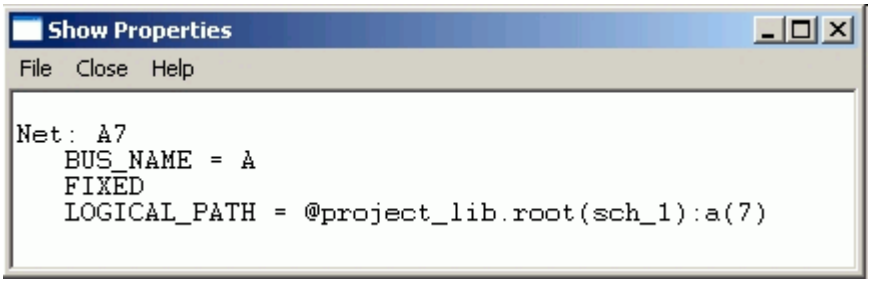
5. Type in the net name A7 and then click *More.*

The Edit Property dialog box appears.



6. Choose `FIXED` in the *Available Properties* list.
7. Set the value of `FIXED` property to `True`.
8. Click *Apply*.

   Notice that the Show Properties dialog box shows you that the `A7` net now has the `FIXED` property associated with it.



9. Click *OK* to close the Edit Properties dialog box.
10. Right-click and choose *Done* to complete the operation.

Creating a Differential Pair Using Constraint Manager

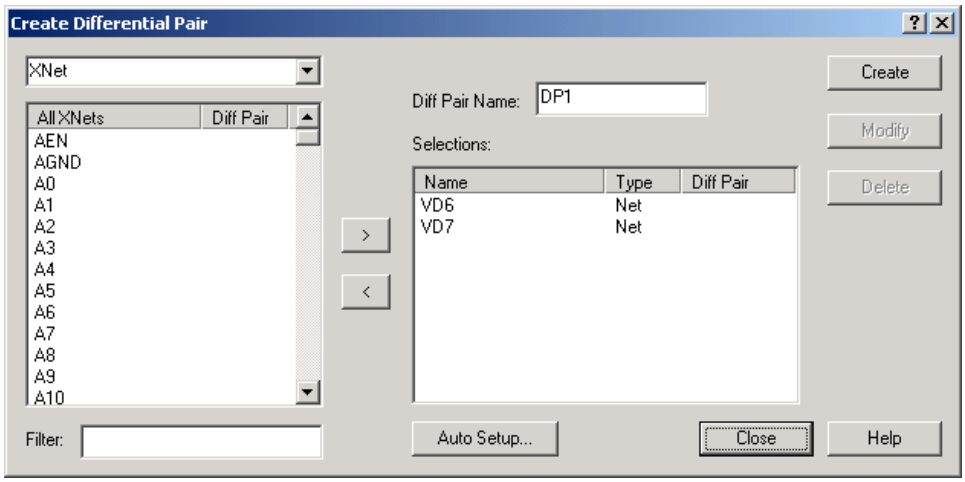
You will create a differential pair for two nets. In Lesson 4-9: Routing Individual Nets on page 137, you will learn to route the two nets, `vd6` and `vd7`, together by selecting one net only.

Note: Electrical constraints are not passed from the PCB Editor to the PCB Router if you set DRC mode to Never in the Constraints System Master dialog box, accessed when you choose *Setup - Constraints* (cns command). You need to set the DRC mode to *Always* or *Batch* to pass electrical constraints.

1. Click  to open Constraint Manager.
2. In the *Routing* workbook, click Differential Pair.

   The Differential Pair worksheet appears to the right in the Constraint Manager window.
3. Choose the vd6 and vd7 nets.
4. Right-click and choose *Create – Differential Pair* from the pop-up menu.

   The Create Differential Pair dialog box appears.



   Notice that the nets vd6 and vd7 appear in the *Selections* box indicating that these nets are members of the differential pair. The name of the differential pair appears automatically as DP1 in the *Diff Pair Name* field.

   Note: If the nets forming a differential pair are of the type DP+ and DP-, the name of the differential pair is set to DP. For other pairs of nets, the name of the differential pair is of the type DP*n*.
5. Click *Create*.

   A new differential pair DP1 is created.
6. Click *Close*.

The Create Differential Pair dialog box closes.

7. Scroll up the list of nets in the worksheet to see the entry for differential pair *DP1* with `vd6` and `vd7` as its members.
8. Close the Constraint Manager to return to the PCB Editor.

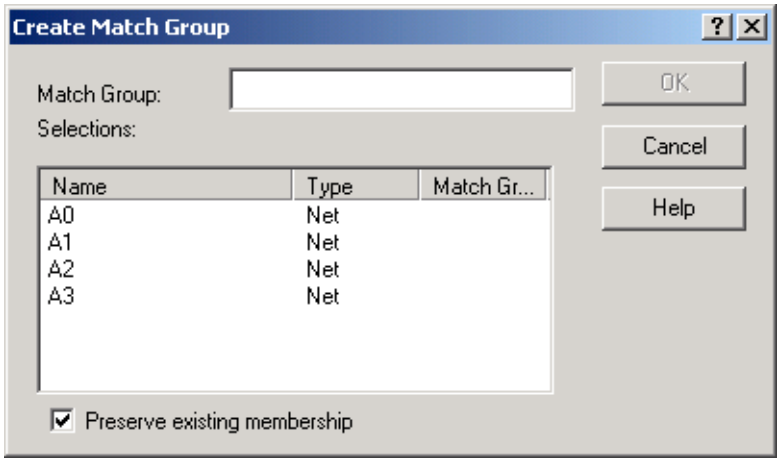
   You have created a differential pair.

Creating a Match Group Using Constraint Manager

You can use the Relative Propagation Delay property in Constraint Manager to route multiple nets relative to one net. For example, you will now set Relative Propagation Delay properties for nets `A0`, `A1`, `A2`, and `A3` by declaring `A1` as the target net and allowing relative delta for other nets.

1. Click  to open Constraint Manager.
2. In the Routing workbook, click *Relative Propagation Delay*.
3. Choose the `A0`, `A1`, `A2`, and `A3` nets.
4. Right-click and choose *Create – Match Group* from the pop-up menu.

   The Create Match Group dialog box appears.



5. Type `M1` as the name in the *Match Group* field and click *OK*.
6. Scroll up the list of nets in the worksheet to see the entry for the match group `M1` with nets `A0`, `A1`, `A2`, and `A3` as its members.

7. Right-click in the *Delta Tolerance* field for the A1 net and choose *Set as Target*.
8. For the remaining nets A0, A2, and A3, enter the following values 200 Mil:10%, 100 Mil:5%, and 50 Mil:8%, respectively.
9. Close the Constraint Manager to return to the PCB Editor.

   You have created a match group. In Lesson 4-9: Routing Individual Nets on page 137, you will learn how this match group influences the routing of A0, A1, A2, and A3 nets.
10. Leave the PCB Editor open. You will set more constraints in the open board file in next exercise.

Summary

You learned to assign properties to nets. By assigning properties that may impact routing behavior early in the design cycle, you can control the routing output better. For example, you can define a differential pair and pick one net for routing, and the Autorouter routes both nets simultaneously. You can set the Relative Propagation Delay constraint to route nets relative to each other.

Lesson 2-4: Setting Constraints

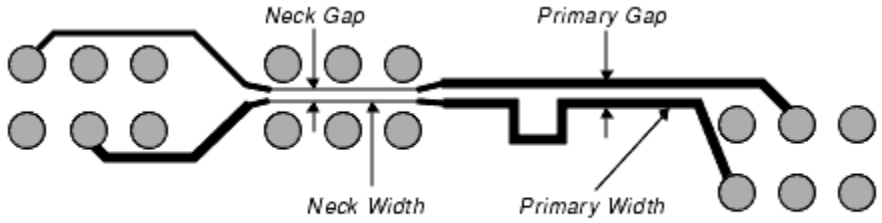
Overview

In this lesson, you will learn to set constraints on nets.

You will learn to set constraints on the differential pair DP1 you created in Lesson 2-3: Setting Properties on page 47. These constraints will be inherited by the member nets vd6+ and vd7-

automatically. When these nets are routed, the constraints will control the routing behavior as shown below.

Controlling a Differential Pair



+Tolerance and *-Tolerance* determine when lines are uncoupled

Procedure

1. Click  to open Constraint Manager.
2. In the Routing workbook, click *Differential Pair* and choose `DP1`.
3. In the *Uncoupled Length* column, set *Gather Control* as *Ignore*.

   The *Gather Control* value determines whether to *Ignore* or to *Include* the uncoupled length that occurs before the etch gathers at the pins.
4. In the *Phase Tolerance* column, set the value of *Tolerance* as `0.2 ns`.

   The *Phase Tolerance* value matches the travel time for each signal of the differential pair to within the specified *Tolerance*.
5. In the *Line Spacing* column, set the value of *Min* as `6 mil`.

   This sets the minimum etch-to-etch spacing for the differential pair to 5 mil. If this value is not set, the default net spacing rule is used.
6. In the *Coupling* column:

   a. Set the value of *Primary Gap* to `8 mil`.

   The *Primary Gap* value sets the optimal distance between the pair of nets in the differential pair to 8 mil.

b. Set the value of *Primary Width* as `6 mil`.

The *Primary Width* value sets the line width for the differential pair to 6 mil.

c. Set the value of *Neck Gap* as `6 mil`.

The *Neck Gap* value sets the allowed distance between the two nets of the differential pair if the etch needs to neck-down to get through the pins.

d. Set the value of *Neck Width* as 6 `mil`.

The *Neck Width* value sets the allowed line width for the differential pair if the etch needs to neck-down to get through the pins.

e. Set the value of *(+) Tolerance* as `2 mil`.

This sets the positive tolerance when the optimal *Primary Gap* cannot be met.

f. Set the value of *(-) Tolerance* as `0 mil`.

This sets the negative tolerance when the optimal *Primary Gap* cannot be met.

Objects	Ref	Uncoupled Lengt			Phase Tolerance			Line Spacing		Coupling					
		Gather Contro	L m	Max mil	Tolera ns	Actual	Margin	Mi mi	Actual mil	Primary Gap mil	Primary Width mil	Neck Gap mil	Neck Widt mil	(+)Toler mil	(-)Tolera mil
DP1		Ignore			.2 ns			6		8	6	6	6	2	0
VD6		Ignore			.2 ns			6		8	6	6	6	2	0
VD7		Ignore			.2 ns			6		8	6	6	6	2	0

7. Close Constraint Manager to return to the PCB Editor.

8. Choose File – *Save As*.

9. Type `constraints.brd` and press `Enter`.

You have set the constraints for the differential pair `DP1`.

Summary

You learned to set constraints for a differential pair. Before you route a design, ensure that you have set the necessary constraints.

Lesson 2-5: Setting the Plane Layers to Plane

Overview

In this lesson, you will learn how to set the plane layer to negative in the layer stackup.

A plane layer is a conductive layer in the cross-section editor designated as the layer type "plane". These layers are typically used to create shapes for the purpose of Power and GND distribution.

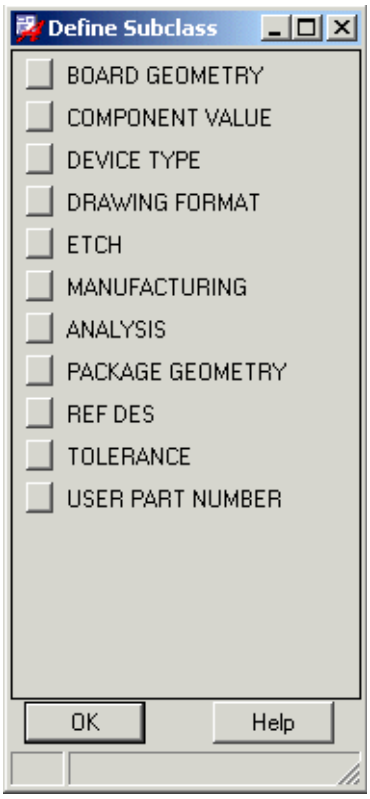
Internal plane layers need to be defined as negative. The Autorouter translator and the router take a long time to process the plane if you treat internal plane layers as positive.

Procedure

Checking Whether Plane Layers Are Negative

1. Open the `constraints.brd` file in the PCB Editor.
2. Choose *Setup – Subclasses*.

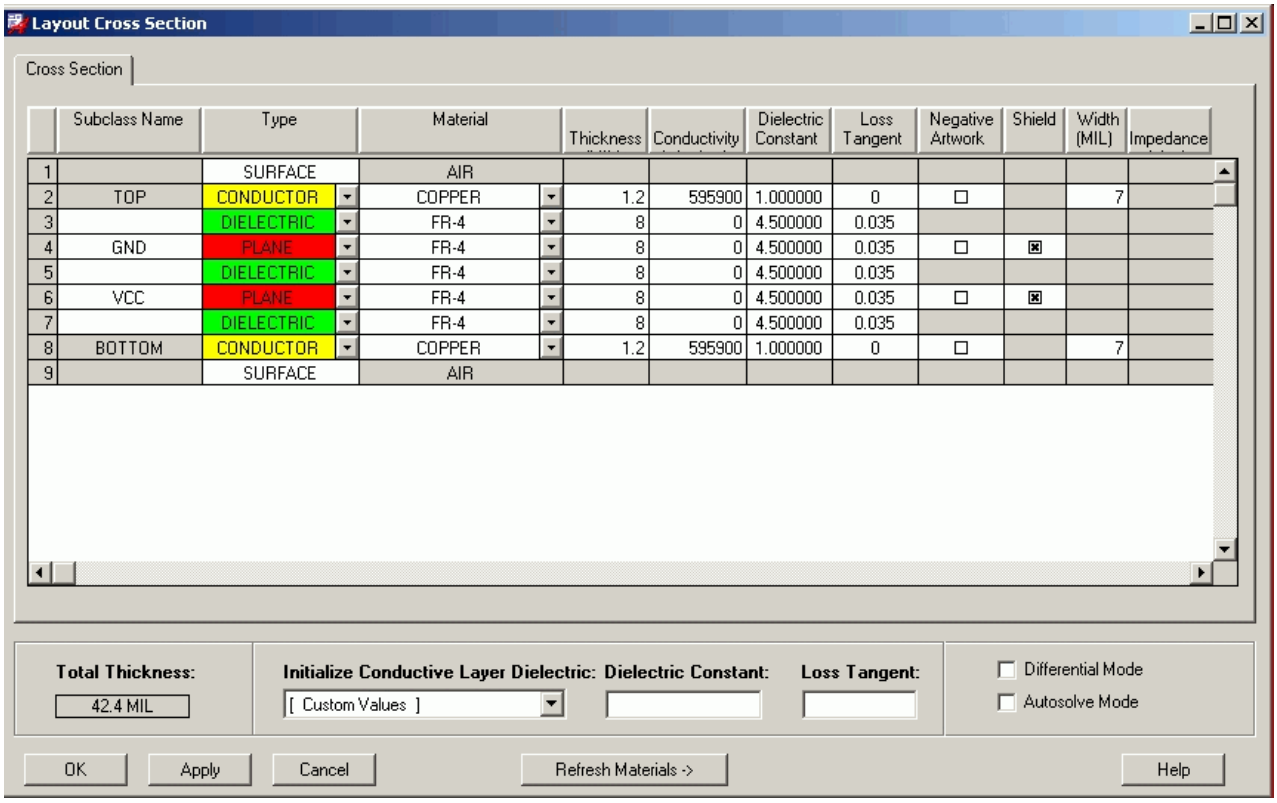
The Define Subclass dialog box appears.



3. Choose *Etch.*

The Layout Cross Section dialog box appears.

4. If the GND and VCC are plane layers and are set to *Positive,* then change them to *Negative*.



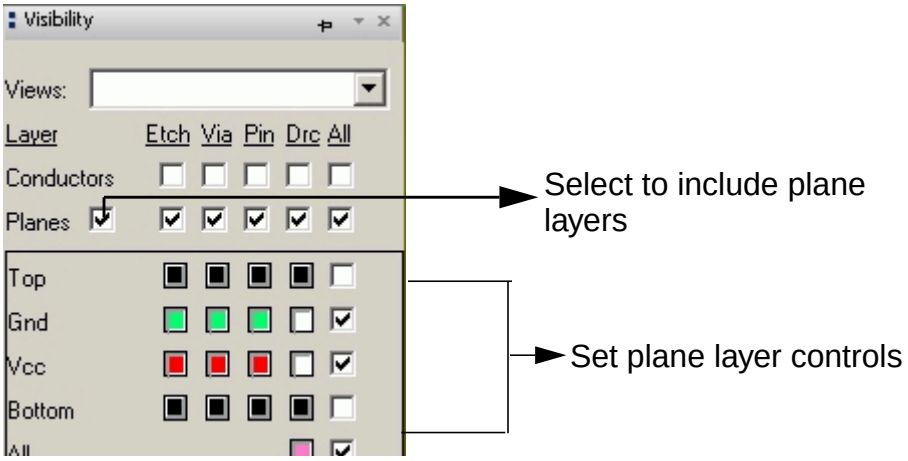
If you have any other split plane layers, ensure that they are set to *Negative*.

5. Click *OK* to close the Layout Cross Section dialog box.
6. Click *OK* to close the Define Subclass Dialog box.

Making Plane Layers Visible

1. In the Control Panel, choose the *Visibility* tab.

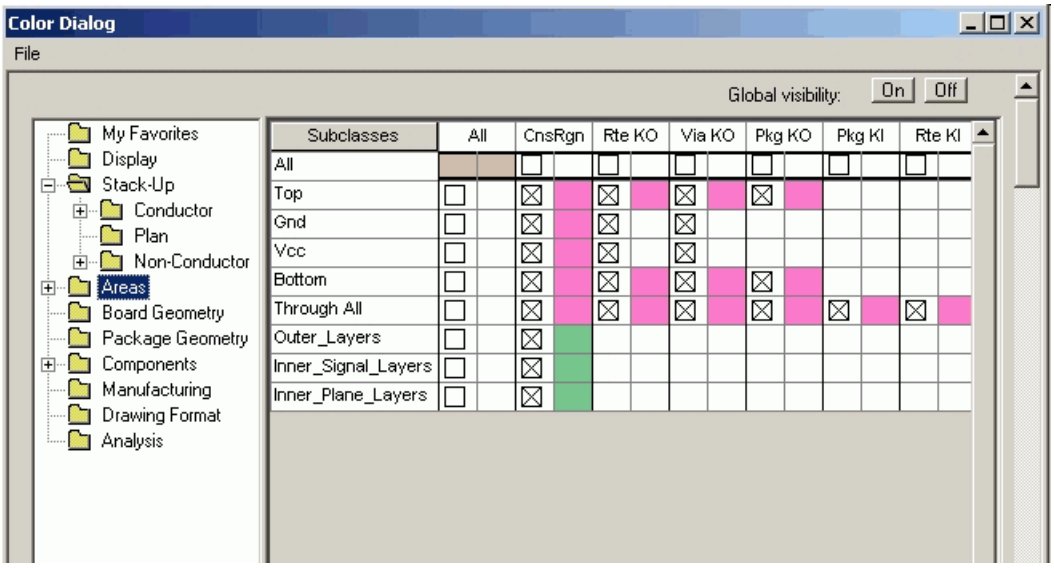
To make the plane layers visible and allow the Autorouter to add VCC and GND connections, choose the following options:



2. Click the *Color* icon  .

   The Color and Visibility dialog box appears.

3. Set the color for etch, pin and via to green for the GND subclass and to red for the VCC subclass as shown in following figure:



4. Choose *Areas* in the *Group* drop-down list.
5. Toggle the *Route Ki* (Route Keepin) class to ON.
6. Click *OK* to confirm the changed settings.

7. Choose *File – Save As*.
8. Type `plane_checked.brd` and press `Enter`.
9. Do not close the board file. You will use the open board file in next exercise.

Summary

You learned to make the plane layers negative and make them visible.

Lesson 2-6: Running Router Checks

Overview

In this lesson, you will learn to perform basic router checks before routing a layout.

The *Router Checks* command lets you run router and alignment checks on the current design to identify routing problems prior to running the PCB Router. A window displays the items that may not have a corresponding constraint in the PCB Router or that may otherwise cause the router to fail.

Listing of Pre-Route Design Checks

The following design checks are performed for the PCB Router when you run the pre-route program.

Design check...	verifies whether ...
checkKeepin	Route_keepins are defined
checkFiguresOnEtch	Figures exist on ETCH subclass
checkVias	Vias are available for routing. Checks for default vias only.
check0LineWidth	One or more nets have a default line of zero units.

checkConsOutsideKeepin	One or more connection points of a route is outside the route_keepin area. Connections are checked for placed components only.
checkPositiveShapes	One or more routing layers have more than 50% of their areas covered with positive shapes.
checkPinsUnderKeepout	A through pin is blocked by `ROUTE_KEEPOUT ALL`, or a surface-mount pin is blocked by `KEEPOUT` on its layer.

Tips for Design Translation Between the PCB Editor and the PCB Router

The following information will help you in preparing the PCB Editor designs going to the PCB Router.

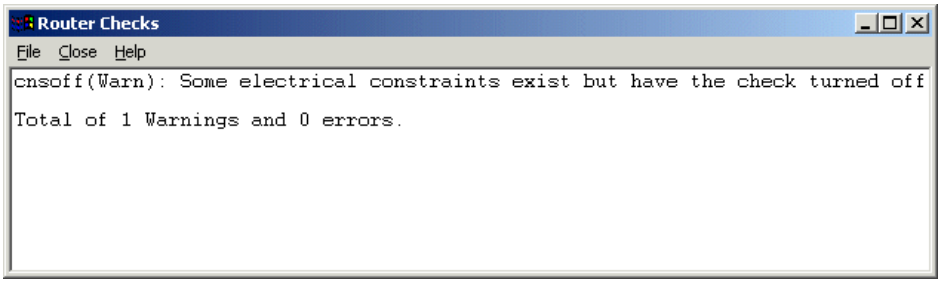
- The `FIXED` property in the PCB Editor translates to a net of `TYPE FIX` in the PCB Router. The net cannot be changed in PCB Router.
- The translator “protects” pre-existing routed etch in the PCB Editor. Etch that is carried over to the PCB Router can be unprotected, then removed/modified there.
- The translated board file should not be changed between the time the PCB Router design file is written and the session file is read back into the PCB Editor.
- Only place and route results (not rules) created in the PCB Router translate back to the PCB Editor.
- Electrical constraints are not passed from the PCB Editor to the PCB Router if DRC mode is set to *Never* in the constraints set-up dialogs (when you only define constraints). You need to set the DRC mode to *Always* or *Batch* to pass electrical constraints.

You will now run router checks to identify common routing problems for a design.

Procedure

1. Open the `plane_checked.brd` file in the PCB Editor.
2. Choose *Router – Router Checks*.

The Router Checks window appears displaying any warnings or errors in the design.



Notice that the Autorouter has displayed a warning that the check for electrical constraints is turned off. These constraints were created in Lesson 2-4: Setting Constraints on page 53. To turn 0n the electrical constrains check:

a. Click  to open Constraint Manager.

b. Choose *Analyze – Analyze Modes*.

c. Ensure that the *On-line DRC* check box is selected.

d. Choose the *All On* button in the DRC mode tab of the Analyze Mode dialog box.

e. Click *OK* to close the Analyze Mode dialog box.

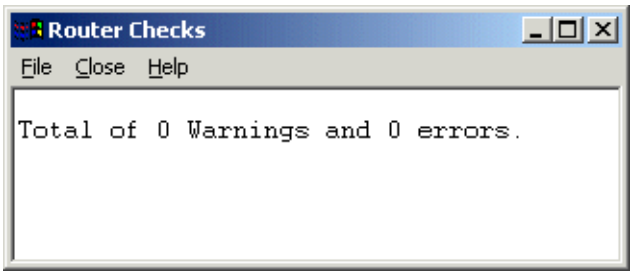
f. Close Constraint Manager to return to the PCB Editor.

You have enabled the check for electrical constraints. You can now again run Router Checks to see if any errors exist.

3. Close the Router Checks window.

4. Choose *Route – Router Checks*.

The Router Checks window appears displaying zero warnings or errors in the design.



5. Close the Router Checks window.
6. Choose *File – Save As*.
7. Type `placement_ready.brd` and press `Enter`.

Summary

You learned to perform router checks to find routing or alignment errors. It is a good practice to perform router checks before routing a design. Fix the issues you find during a router check before running any routing command.

Lesson 2-7: Selecting a PCB Router Task Flow Model

Overview

In this lesson, you will identify the differences in different router task flow models. This information will help you decide the type of routing that best suits a design.

Concept

Depending upon your design requirement, you can use one of the following three task flow models to plan routing for a design.

To do this...	... select this model
Wholly automatic routing of designs that do not require interactive routing	Mainstream Model
Routing of designs that require a degree of interactive routing and possible editing of the various .do files created for the PCB Router	Highspeed Model
Routing of designs that require significant interactivity in the PCB Router and through the editing of the various .do files created for the PCB Router	Highspeed Power User Model

Mainstream Model

This task flow is appropriate if you need to perform an automatic routing of the design using the PCB Router. This method is not designed for manual editing of routing files.

To automatically route the whole design, choose *Route – Route Automatic*. If you do not want to route the entire design, choose *Route – Net(s) By Pick*.

The *Route – Route Automatic* command reads the design file that is open in the PCB Editor, translates the design to the PCB Router and runs the router in the background, and writes out the following files:

- <*board_name*>.dsn
- <*board_name*>_rules.do
- <*board_name*>_forget.do

Following files are generated in the routing process:

- <*board_name*>.dsn—the binary file that is used by the PCB Router to route the design.
- <*board_name*>_rules.do—contains all the rules for the design. You can use it to add or modify some of the rules.
- <*board_name*>_forget.do—contains list of rules that you can choose to have removed from the board.

Note: For more information about automatic routing commands, see Lesson 4-5: Using Basic Autorouting Commands on page 115 and Lesson 4-9: Routing Individual Nets on page 137.

Setting Parameters

When routing the entire design or routing nets by pick, or before doing any automatic routing, you can set parameters in the Automatic Router Parameters dialog box. You can set parameters for:

- **Fanout**—Routes short pin escape wires from pins to vias
- **Bus routing**—Routes component pins that share the same, or nearly the same, X or Y coordinate

- **Seed vias**—Breaks a single connection into two shorter connections by adding a via
- **Testpoint**—Assigns test points to signal nets
- **Miter corners**—Changes 90-degree wires to 45-degrees for wires exiting pins and vias
- **Spread wires**—Adds an extra space between wires, and between wires and pins
- **Elongate**—Increases etch length to adhere to timing rules

Note: For more information about setting routing parameters, see

- Lesson 4-3: Understanding Router Setup on page 106.
- Lesson 4-9: Routing Individual Nets on page 137
- Lesson 4-10: Mitering and Unmitering Connections on page 142
- Lesson 4-11: Using Fanout By Pick on page 145

Highspeed Model

The Highspeed task flow is appropriate if you need to review and possibly modify the generated .do files, and then route the design with the PCB Router.

Important

Be aware that the original .do files generated and modified using this model are automatically deleted when you terminate the current session of the PCB Editor. Renamed .do files are retained after termination.

If you use only the original generated .do files, ignore steps 2a, 2b, and 3 in the following procedure.

1. Choose *Route – Route Editor* (`specctra` command).

   When you run this command, the following actions occur:

   - The PCB Editor writes the design, rules, and forget files from the current database.
   - The PCB Router user interface opens.

- ❑ The generated design and rules file are read into the PCB Router.

2. Open a text editor to review and edit the `rules.do` file. Cadence recommends that you do the following when editing any `.do` files:

   a. Copy the generated `rules.do` file to a different file name.

   b. Edit the renamed file.

   Note: Only place and route results (not rules) created in the PCB Router translate back to the PCB Editor.

   Note: For more information about automatic routing commands, see Lesson 4-8: Making Changes in a do File for Autorouting on page 130.

3. Load the forget file and the renamed `.do` file(s) into the PCB Router and perform an initial route of the design.
4. If the initial route is completed to satisfaction, load the forget file and the original `.do` file(s).
5. Run the `check` command to verify any design rule violations.
6. If you are satisfied with the results, load the original files back into the PCB Editor.

Note: For more information about the data flow between the PCB Editor and the PCB Router, see Lesson 4-4: PCB Editor/PCB Router Design Flow on page 111.

Highspeed Power User Model

The Highspeed power user task flow is appropriate if you need to actively edit the generated `.do` files before loading and routing them with the PCB Router.

1. Choose *File* – Export – *Router.*

   When you run this command, the following actions occur:

   - ❑ The PCB Editor writes a design, rules, and forget file from the current database.
   - ❑ The Export to Auto-Router dialog box opens.

2. Click *Run* to export the design file to the PCB Router.
3. When translation of the design file is complete, close the dialog box.
4. Open a text editor to review and edit the `rules.do` file. Cadence recommends that you make a copy the generated `rules.do` file and edit the copy.

   Note: Only place and route results (not rules) created in the PCB Router translate back to the PCB Editor.
5. Open the PCB Router interface by selecting *Route – Route Editor*.
6. Load the forget file and the renamed .do files into the PCB Router and perform an initial route of the design.
7. If the initial route is completed to your satisfaction, load the forget file and the original .do file(s).
8. Run the check command to verify any design rule violations.
9. If you are satisfied with the results, write out a session file and load the original files back into the PCB Editor.

   a. Choose *File – Import – Router* (`specctra_in` command).

   The Import from Auto-Router dialog box opens.

   b. Enter the name of the session file.

   c. Click *Run* to import the file into the PCB Editor.

The .do files generated and modified using this model are saved when you terminate the current session of the PCB Editor. If you use only the original generated .do files, ignore steps 4a, 4b, and 6 in the above procedure.

Note: The exercises in this tutorial are based on the mainstream task flow model.

Summary

In this lesson, you learned the differences in different router task flow models.

3

Module 3: Routing a Design

This module consists of the following lessons:

Completion Time

- 1.5 hours for written lessons

Lesson 3-1: Creating Connection Lines

Overview

In this lesson, you will learn how to connect pins by creating a pin-net connection (also called etch or connection line (cline) or trace). You will also learn about the Route toolbar and use common operations that help in creating pin-net connections.

Concept

The Route toolbar lists commonly accessed routing operations.

Note: By default, the *Specctra* icon is NOT part of the route toolbar. You can add this icon manually by customizing the toolbar (*View – Customization – Toolbars)*.

All routing commands are listed in the *Route* menu or the *Route* toolbar. For more information, see Lesson 1-5: Route Menu on page 30.

You perform the following basic steps to create connection lines:

1. **Define an etch grid**—An etch grid is a grid used by the PCB Editor for adding any etches.
2. **Control ratsnest display**—Rats are imaginary lines drawn between the unconnected pins of a net. You can turn the rats display `ON` or `OFF` using the Route toolbar or *Display* command. You may often need to switch off the display of all ratsnests and then display specific ratsnests.
3. **Create an etch**—Use the *Add Connect* command to create etches. You will use different command options to change line width, draw lines as arcs or straight lines, change mitering setup, and rip etches to create space for all etches.
4. **Delete etches**—Use the *Delete* icon  to delete etches.

Procedure

Defining an Etch Grid

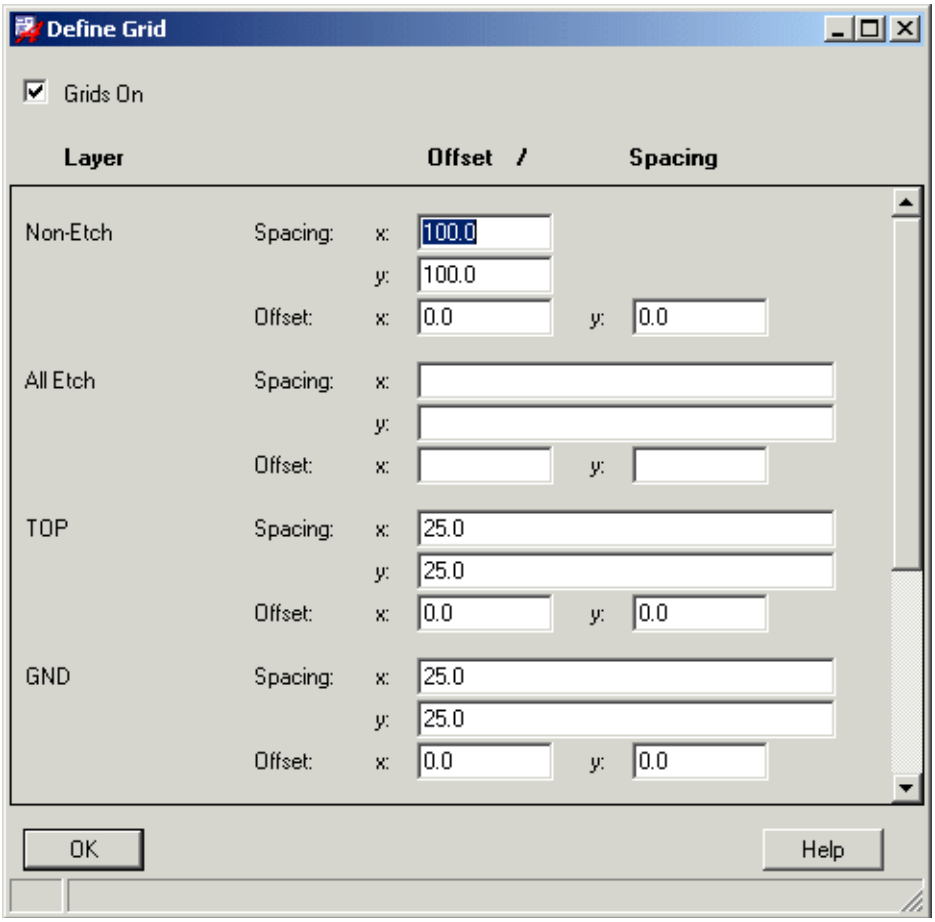
1. Open the `routing_ready.brd` file in the PCB Editor.

Note: The `routing_ready` board includes all constraints and properties you attached in the `placement_ready.brd` file in Module 2: Preparing to Route on page 35 and has all components placed on it. Component placement is not within the scope of this tutorial. For more information about component placement, see the Cadence document *Allegro PCB and Packaging User Guide: Placing the Elements.*

2. Click the *Zoom Fit* icon  to view the entire board.

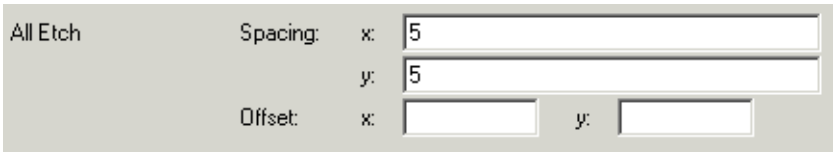
3. Choose *Setup – Grids*.

The Define Grid dialog box appears.



4. Ensure that the *Grids On* option in the upper left corner of the dialog box is selected.

   In the *All Etch* section, make the entries shown in the following figure:



Note: The settings will automatically change for all other etches to 5.

5. Click *OK* to close the Define Grid dialog box.

   Depending on your last active command, the PCB Editor Design window may or may not display the 5-Mil grid pattern.

6. If the etch grid is not displayed, then choose any routing command, for example choose *Route – Connect*.

   An etch grid appears. For enhanced viewability, the grid may show a wider grid pattern, such as 80.0 by 80.0, like the one shown below.

```
Grids are drawn 80.0, 80.0 apart for enhanced viewability.
Command >
```

7. To decrease the grid size, click the *Zoom In* icon  .

   The grid size reduces to 20 by 20. Additional zooming in might not reduce the displayed grid size.

8. Right-click and choose *Cancel* from the pop-up menu to cancel the *Connect* command.

Controlling Ratsnest Display

1. Click the *Zoom Fit* icon  to view the entire board.
2. Using the *Visibility* tab, make visible only the `TOP` and `BOTTOM` layers.
3. Click the *Unrats All* icon  to switch off the display of ratsnests.

   The PCB Editor shows only components and the board outline. No ratsnests are displayed.

 *Tip*

If you want only a specific net to be displayed on the board, then click the Unrats All icon and then select the net.

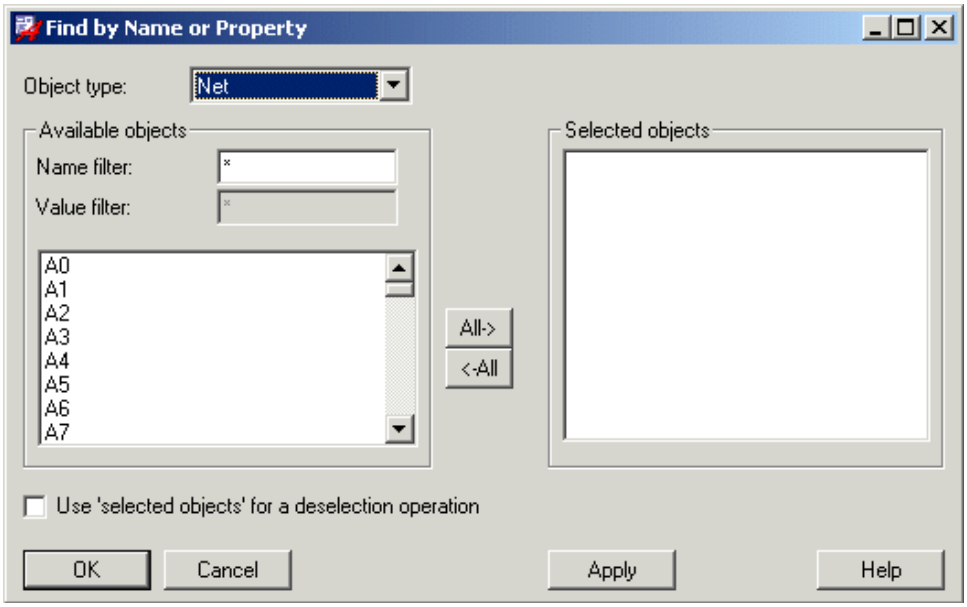
4. Click the *Rats All* icon  to switch on the display of ratsnests.

   All ratsnest appear in the PCB Editor. You can even display the ratsnests for a few nets, for example the ratsnest for nets `A6` and `A5`.

5. Click the *Unrats All* icon  to switch off the display of ratsnests.
6. Choose *Display – Show Rats – Net*.

7. Select the *Find* tab and in the *Find By Name* field, first choose the *All Off* button, and then choose the *Nets* check box.
8. In the *Find By Name* field, change the value to *Net*.
9. Click *More* in the *Find By Name* section of the *Find* tab.

   The Find by Name or Property dialog box appears.



10. Choose the A5 and A6 nets in the *Available objects* list.

    The selected nets appear in the *Selected objects* list.
11. Click *OK* to close the Find By Name or Property dialog box.

    The ratsnests for the A5 and A6 nets are selected.

Creating an Etch

You will create an etch for the A6 net.

1. Click the *Zoom Fit* icon  to view the entire board.
2. Choose *Display – Blank Rats – All*.
3. Choose *Display – Show Rats – Net*.
4. In the *Find By Name* field, change the field to *Net*.
5. Type A6 and press `Enter`.

The A6 net is selected in the PCB Editor. You can see a ratsnest in the Design Window.

6. If the focus is not on the A6 net, click the *Zoom In* icon  .
7. Click the *Show Element* icon  and then do the following:
   a. Click the pin connecting the ratsnest on its left side.

      The Show Element window appears stating that the element displayed is a connector with REFDES J1, and its pin number 60 is connected to the A6 net.

      Note: To ensure that properties of all elements are displayed, set the *Design Object Find Filter* in the *Find* tab to *All On*.

   b. Click the pin at the right side of the ratsnest.

      The Show Element window refreshes its display. Notice that the connecting component is U4, its package symbol is SOIC48, and its pin 38 is connected to the A6 net.

   c. Click the ratsnest connecting the two nets.

      The Show Element window refreshes its display. Notice that the element is a net named A6 and it connects pin J1:60 with pin U4:38.

   d. Right-click and choose *Done.*
8. Choose *Route – Connect*.

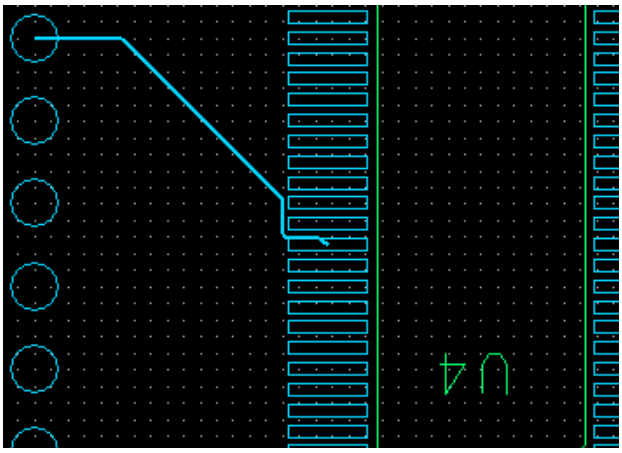
   The values in the *Options* tab change.
9. Click the J1:60 pin.

   After you select the start point, you see a ratsnest line stretching from the cursor to the nearest destination pin. As you move the cursor, the route appears.

   Note: As the TOP layer is active and the pin is a through-hole pin, you need to add a connection on the top layer of the board. If this were a surface-mount pin, the connection would be added to the layer on which the SMD pin was defined.

   The net name and the correct line width for the A6 net appear in the *Options* tab.

10. Continue to click points for the line until you reach the destination pin. You can make your trace look similar to the figure shown below:



When you reach the destination pin, the ratsnests line disappears, showing that the connection has been made.

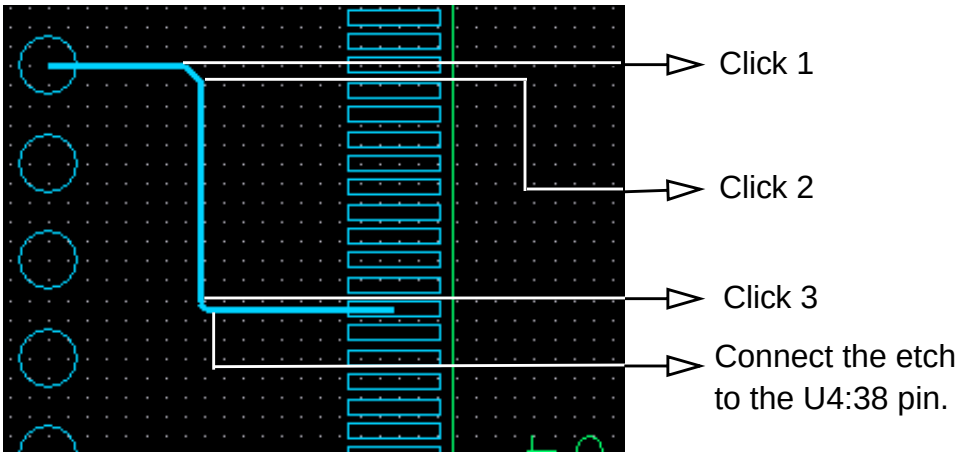
You have a connection between pins `J1:60` and `U4:38`.

If you make a mistake while picking points, you can retrace your steps by right-clicking and choosing the *Oops* option.

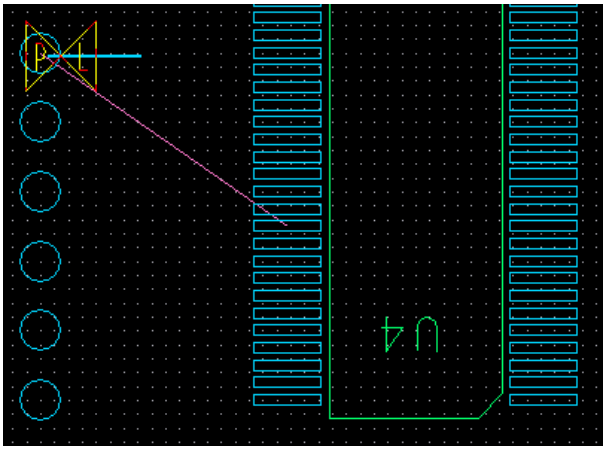
11. Try it out now. Right-click and choose the *Oops* option.

You can now again draw an etch between pins `J1:60` and `U4:38`. To have a corner for a line (also called vertex), click at the point where you need the corner.

12. Try making a connection like the figure shown below:



Note: If the connection you are making causes a DRC violation, the PCB Editor flags a DRC error as shown below:



If a DRC error is generated, right-click and choose the *Oops* option and start again.

13. After you have made the connection between the pins `J1:60` and `U4:38`, right-click and choose *Done.*

You have created a pin-net connection.

Deleting Etches

1. Click the *Delete* icon  to delete an etch.

   Note: The default settings in the Find Filter may show all items Ideally, you should switch all items `OFF`, and then choose only the items you want to delete.

2. Click the *Find* tab to bring the *Find* tab to the front if it is not visible.

3. Click the *All Off* button in the *Find* tab.

   You can now delete connection line (all segments from pin to pin) or individual segments. Using *Clines* in the Find Filter lets you delete the entire connect line (all segments from pin to pin), while using *Cline Segs* in the Find Filter lets you delete individual line segments.

4. Choose the *Clines* (connect lines) box.

5. Click the A6 net.

The connection becomes highlighted.

6. Click anywhere on the board.

   The previous etch you added disappears.

   You now learn to delete individual line segments.

7. Right-click and choose *Oops* from the pop-up menu to cancel the last operation.

8. In the Find Filter, set the check box options as follows:

   a. Clear the *Clines* check box.

   b. Choose the *Cline Segs* (connect line segments) check box.

9. Click the A6 net.

   A segment becomes highlighted.

   You can delete individual segments of a connect line by using *Cline Segs* in the Find Filter.

10. Click another segment.

    The first segment disappears. The ratsnest line reappears because the pin-to-pin connection has been broken.

11. Right-click and choose *Done* from the pop-up menu.

You have deleted connections by deleting clines or individual line segments.

Modifying the Connect Command Options

1. Choose *Route – Connect*.

The values in the *Options* tab change.

Act—Specifies *Top* as the active subclass. The pin-net connection is made on this layer, unless you define a via or swap layer. If required, you can change the active subclass.

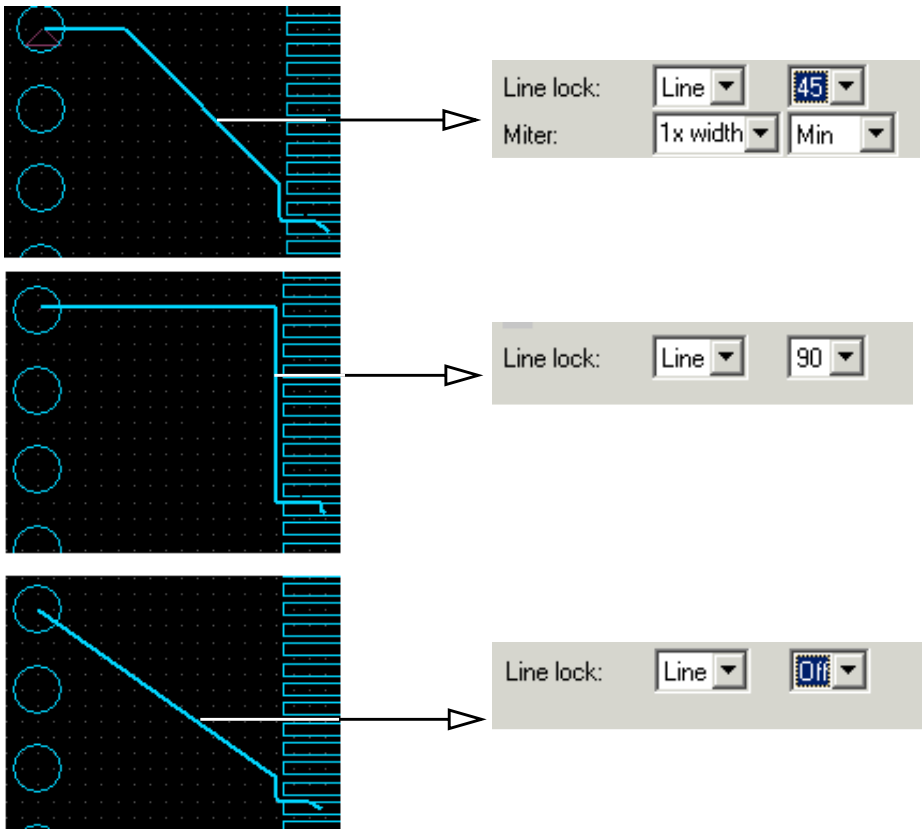
Alt—Specifies *Bottom* as the alternate subclass. The alternate layer becomes the active layer when you right-click within the design and choose *Swap Layers* or *Add Via* from the pop-up menu when an element is active. If no element is active or the active element also exists on an alternate subclass, *Swap Layers* lets you change active layer to alternate layer and vice versa.

Via—Lists the available via padstacks between the active and alternate subclasses.

Line Lock—Controls the type of line, either Line or Arc, and the angles allowed for turns. `Off` implies that “any-angle routing” is allowed. You can set angle of turns to 45 or 90 degrees. The default setting is Line 45 degrees.

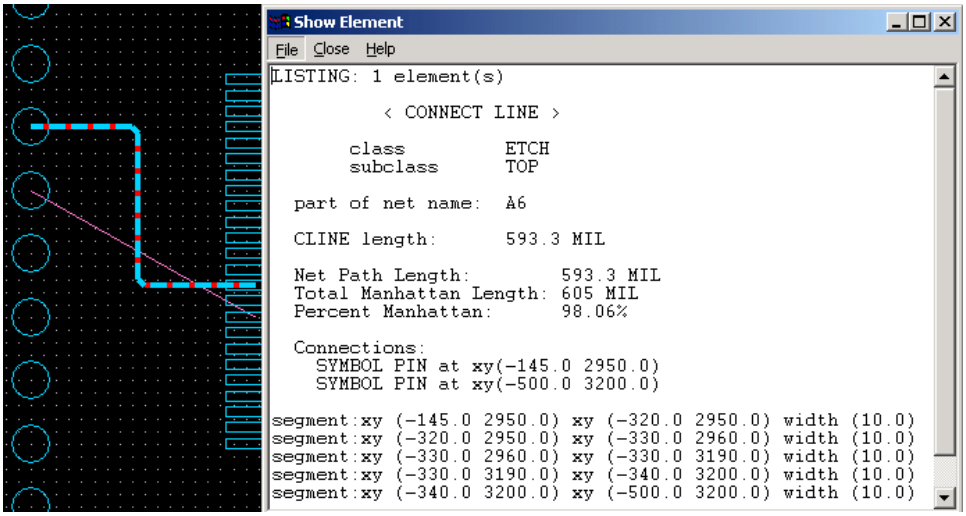
Miter controls—Specifies to cut corners at 45-degree angle in these settings. These controls are available only when the *Line Lock* is set to 45.

2. Try recreating the A6 net using different *Line Lock* settings as shown below:



3. Delete the A6 net and recreate it using *Line width* 10 and *Line Lock* 45.
4. Ensure that only the *Clines* check box is selected in the *Find* tab.
5. Click  and click the A6 net.

The Show Element window appears displaying the A6 net with 5 segments, each 10 mil wide.



6. Click the *Add Connect* icon  .

   The Show Element window disappears. The *Options* tab shows settings for the `Add Connect` command. Notice that the *Bubble* option is set to *Off.* The *Bubble* field provides three choices:

   - **Off**—The new route follows your cursor picks in the x and y direction absolutely. Line connections are created regardless of potential DRC errors.
   - **Hug Preferred**—The new route hugs around existing etch objects. The existing objects are not modified.
   - **Shove Preferred**—The new route shoves or moves away other etch objects to correct for spacing violations.

   When you set the *Bubble* field to *Hug Preferred* or *Shove Preferred*, the *Gridless* option appears. This option offers two choices:

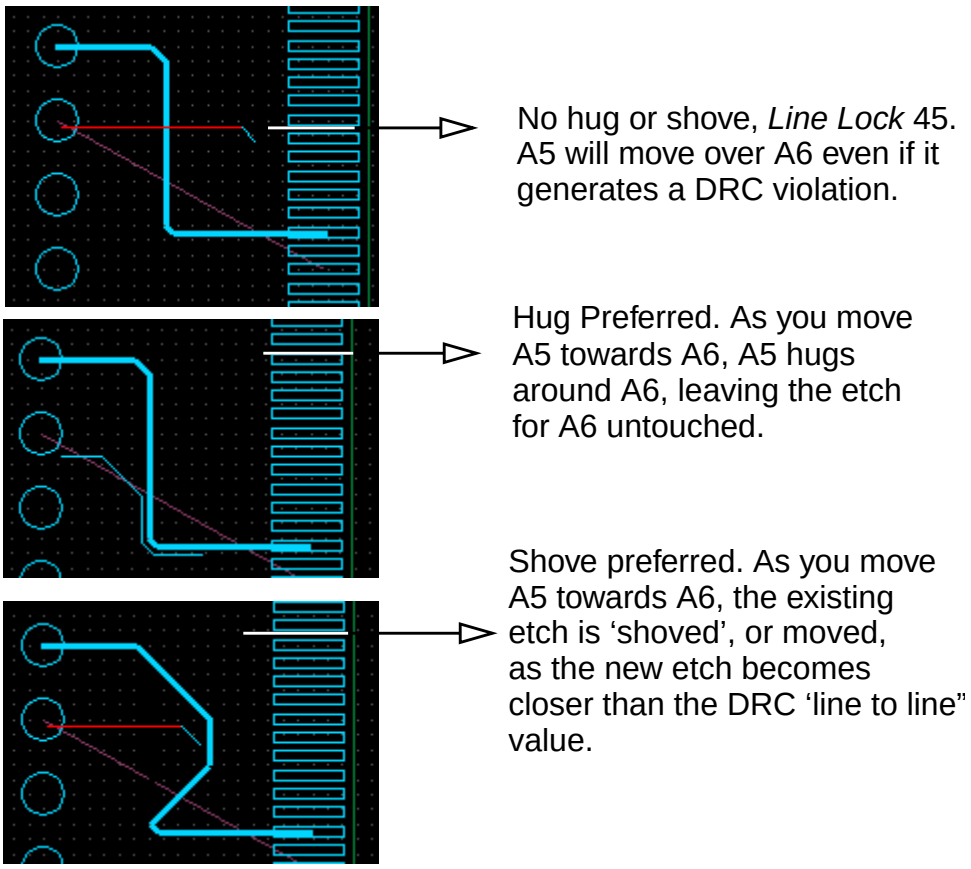
   - **Off**—Pushes etch to the next available free grid.
   - **On**—Pushes etch away from pads and vias just enough to reach a legal minimum DRC clearance.

7. Create a connection for the A5 net by following different settings as shown below.

Tip

You may display the ratsnest for the A5 net first. (See Controlling Ratsnest Display on page 72)

.



8. Right-click and choose *Cancel* from the pop-up menu to cancel the connection for the A5 net.

   Note: In Lesson 3-2: Performing Interactive Routing on page 82, you use vias to create a connection for the A5 net

9. Do not close PCB Editor. You will use this board file in the next lesson.

Summary

In this lesson, you learned to create connections using the *Route - Connect* command. This command allows you to create new

connections and control the line width and line lock angle. Further, you can set how a new connection moves existing connections.

Lesson 3-2: Performing Interactive Routing

Overview

In this lesson, you will learn to perform interactive routing (or manual routing).

Concept

You can perform interactive routing to:

- Connect two points, with or without vias
- Start a connection from a Rat T point

Note: You learned how to connect two points without making vias in Lesson 3-1: Creating Connection Lines on page 69.

Interactive routing also involves:

- Insert blind, buried, and through-hole vias—A through-hole via penetrates all layers and allows a connection to travel between the top/surface and bottom/base etch/conductor layers.
- Edit vertices (etch segment corners)
- Shove vias when adding clines
- Add or delete connections and vias
- Slide connections and vias
- Begin a connection, then run automatic routing to finish the etch/conductor for that pin-pair

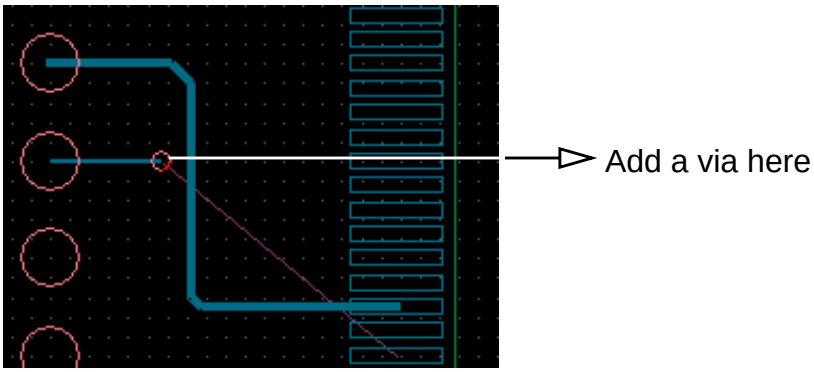
  Note: For more information about automatic routing, see Lesson 4-5: Using Basic Autorouting Commands on page 115.

- Route timing-sensitive circuits

Procedure

Inserting Vias

1. Click the *Add Connect* icon  .
2. If necessary, click the tab for the *Options* tab to bring it forward.
3. In the *Options* tab, set the active and alternate layers to `Top` and `Bottom` . Also, set the *Bubble* option to `Off`.
4. Click the pin of the `A5` net in the `J1` connector, the pin connected to one end of the ratsnest. (Hint: This is `J1:59` pin.)
5. Begin adding segments from the pin toward its destination.
6. When you have reached a point where you need to add a via, double-click the left mouse button.

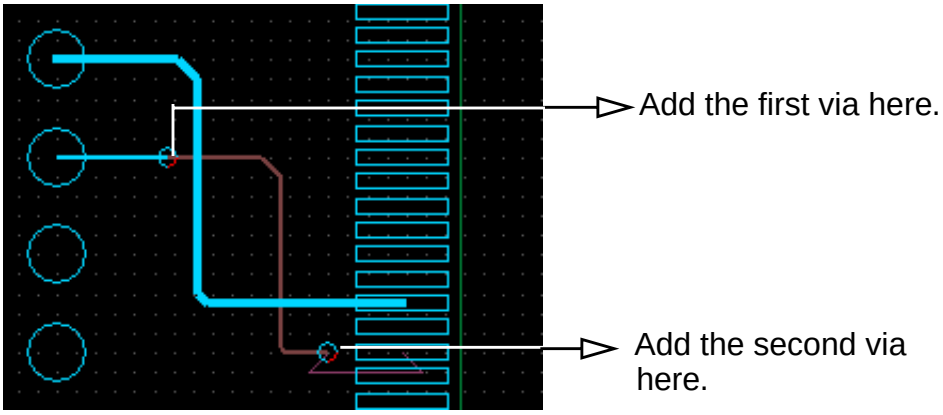


You have just added a via, and the Active and Alternate layers in the *Options* tab are swapped. You are now routing on the `Bottom` layer.

7. Finish the connection all the way to the pin of the selected component (`U4.40`).

   Because the destination pin is on a surface-mount device at the top side of the design, you need to add another via to finish the route on the `Top` layer. However, you cannot add the via where

the pad is. So you have to put it slightly to the left of the pad as shown in the figure below.



Notice that the connection in the `Bottom` layer is in pink and connection in the `Top` layer is in blue. You can change the colors by setting them in the Colors and Visibility dialog box.

8. Right-click and choose *Done* from the pop-up menu.
9. Save the board file with the name `a6_5.brd`.

Editing Vertices

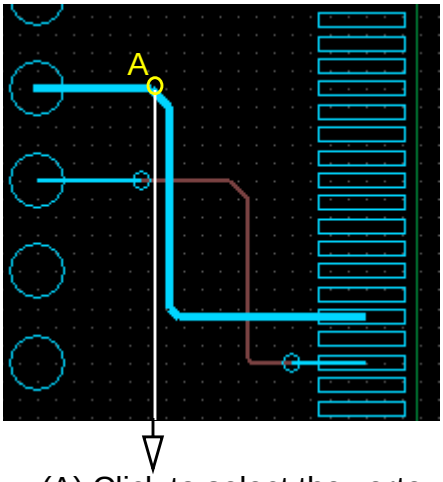
1. Choose *Edit* – *Vertex*.

   Or

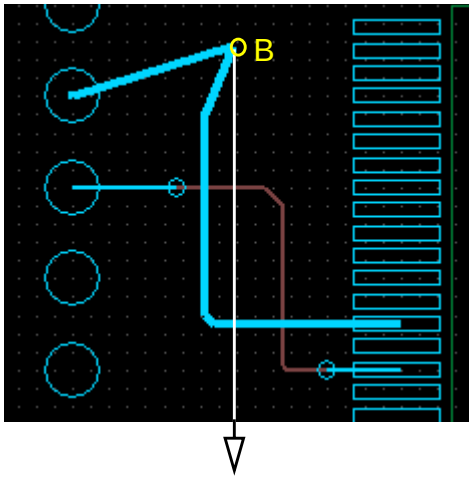
   Click the *Vertex* icon  .

2. Click a corner (Point A) or vertex on an etch line as shown below.

The corner of the etch line is now attached to the cursor, and can be moved to a new location.



(A) Click to select the vertex.



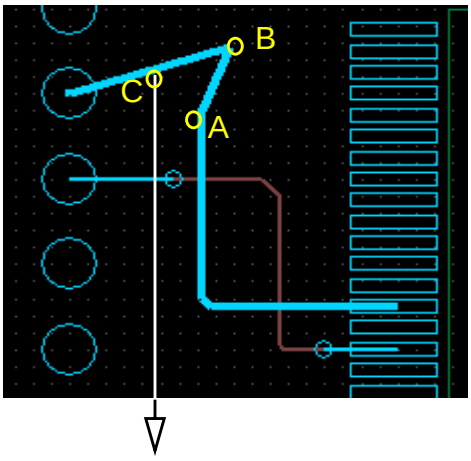
(B) Drag to change the vertex.

3. Choose a new location and click at that point (point B) as shown above.

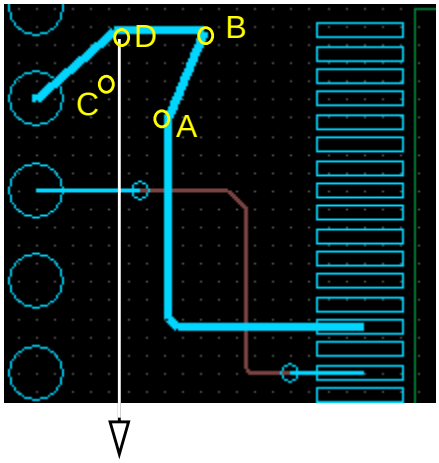
The vertex has moved to the new location. You will now add another vertex (C) to an etch segment.

4. Click a point (C) anywhere between the ends of an etch segment as shown below.

This adds a new vertex point.



(C) Click to select the vertex.



(D) Drag to change the vertex.

5. Click a new location (D) for the vertices shown above.

You have created vertices. You will now learn to remove them.

6. Click a corner (D) of an etch line.
7. Right-click and choose *Delete Vertex*.

   The vertex D is deleted and the etch shape returns to the one before adding this vertex.
8. Click a corner (B) of an etch line.
9. Right-click and choose *Delete Vertex*.

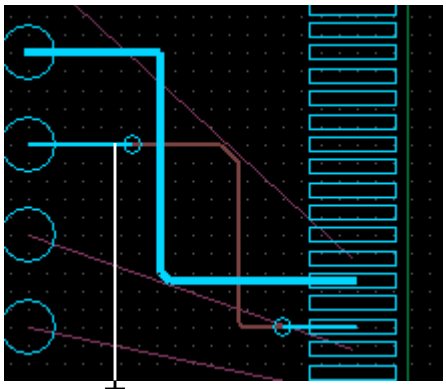
   Both vertices (B and D) are deleted.
10. Close the PCB Editor without saving the open board file.

Sliding Connections and Vias

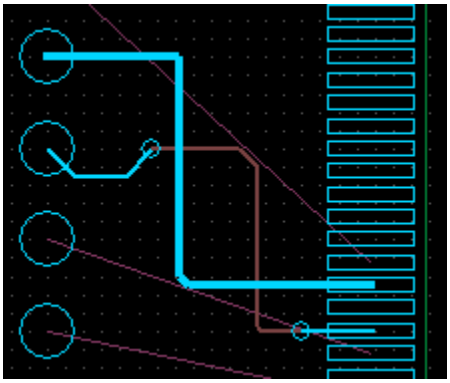
1. Open the `a6_5.brd` file in the PCB Editor.
2. If the focus is not on the A5 net, click the *Zoom In* icon  .
3. Click the *Slide* icon  .
4. Select *Cline Segs*, *Vias*, and *Rat Ts* in the *Find* tab
5. In the *Visibility* tab, for Conductors select *Etch, Pin, Via, Drc*, and *All*. Also, select the *Planes* check box. Finally, select the *Top* and *Bottom* check boxes.
6. In the *Options* tab, set the *Max 45 len* field to `20`.

   The *Max 45 len* determines the length of the 45-degree corner added while sliding connect lines.
7. Click a segment of etch in your display as shown below.

The segment you picked travels with the cursor.

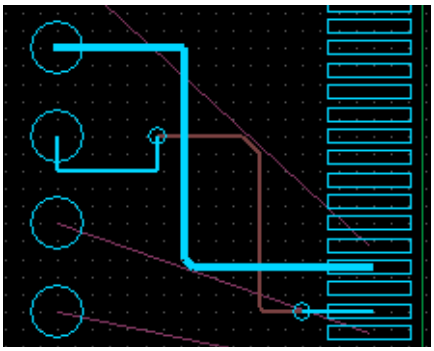


Click here.
(Before slide)



(After slide)

8. Choose a location for the movable etch and click to define the new location as shown in figure above.
9. The *Options* tab controls the corners that you create using Slide. You can try modifying different options, such as:
   - ❑ Set shove to on or off
   - ❑ Set Allow DRCs check to on or off
   - ❑ Set Gridless check to on and off
10. Set *Corners* to 90 and then slide A6 like shown below:

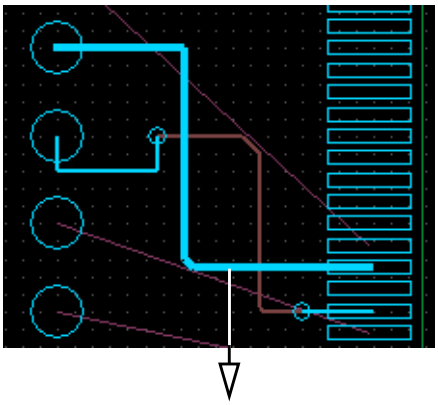


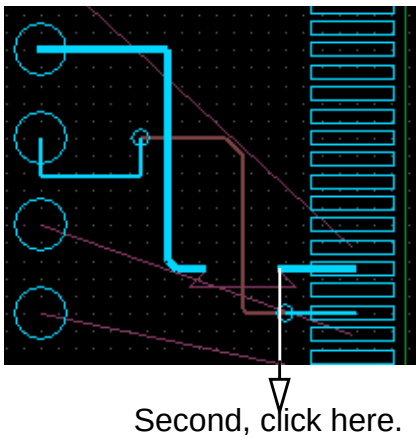
11. Right-click and choose *Done* from the pop-up menu.

You learned how to slide nets. In Lesson 5-2: Using Post Routing Commands on page 153, you will practice sliding nets and vias.

Cutting Connections

1. If the focus is not on the A6 net, click the *Zoom In* icon  .
2. Choose *Edit – Delete.*
3. In the *Find By Name* field, first click the *All Off* button, then choose the *Cline Segs* check box.
4. Right-click and choose *Cut* from the pop-up menu.
5. Click two points on a single segment, where you want the cut to occur as shown below.





   The highlighted portion is deleted. Notice that a ratsnest appear for the deleted segment.

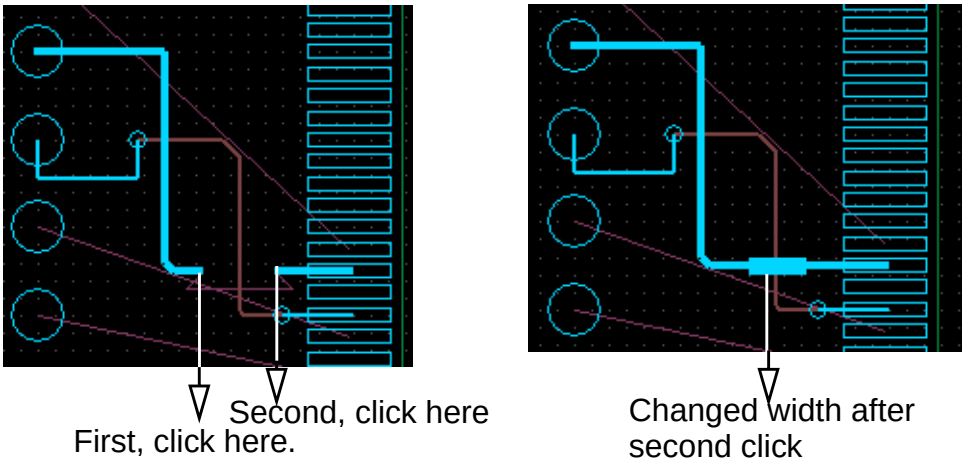
6. Click  and redraw the deleted etch.

Changing the Width Using Cut

You can also change the width of a line using the Cut feature. To change the width for a segment of the A6 net, perform the following:

1. Choose *Edit – Change.*
2. In the *Find By Name* field, first click the *All Off* button, then choose the *Cline Segs* check box.
3. Right-click and choose *Cut* from the pop-up menu.
4. In the *Options* tab, set class to *Etch* and *Line Width* to 20.
5. Right-click and choose *Cut* from the pop-up menu.

6. Click two points in a single segment where you want the cut to change width as shown below.



   Notice the segment displays the new width.

7. Right-click and choose *Done* from the pop-up menu.
8. Choose *File – Save As* and save the board file with the name `a6_5.brd`.

Adding a Delay Tune

1. Open the `a6_5.brd` file in the PCB Editor.
2. If the focus is not on the A6 net, click the *Zoom In* icon  .
3. Click the *Delay Tune* icon  .

   Note: This command is not available in PCB Design L.

   The Command window displays the message:

   ```
   Pick start of tuning.
   ```

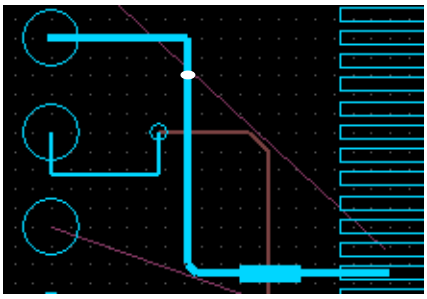
4. Click a point on the A6 net as shown in diagram in step 5.

   The Command window displays the message:

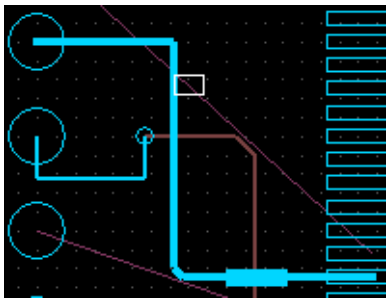
   ```
   Pick tuning end corner.
   ```

   Notice that a white rectangle appears. You can increase the width of this rectangle to increase the tune size.

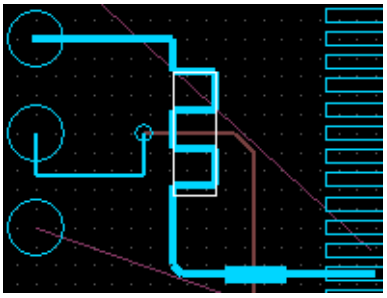
5. Click at another point in the A6 net to define the delay tune.



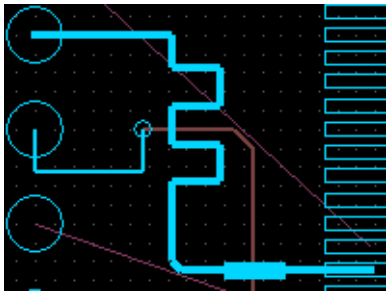
A. Click at the white point.



B. A white rectangle appears.



C. Move down to select the second point.



D. Click to set the delay tune.

The delay tune is set.

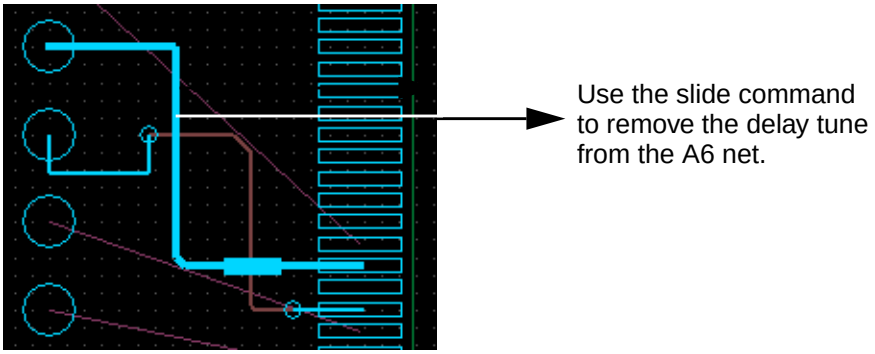
6. Save the board file with the name `a6_5.brd`.

Summary

You learned to interactively route nets. While routing nets, you may need to change width, cut segments, swap layers, create vias, and slide or shove other etches. You may want to interactively route critical nets that are assigned timing-sensitive properties before you automatically route the entire design.

Exercise

Use the `slide` command to remove the delay tune for the A6 net, and save the board file with the name `A6_5.brd`



4

Module 4: Autorouting a Design

This module consists of the following lessons:

Completion Time

- 4 hours for written lessons

Lesson 4-1: Preparing for Automatic Routing

Overview

In this lesson, you will identify the basic preparation for automatic routing of design.

Concept

Before you autoroute any design, ensure that your design is ready for routing. The following steps are recommended before you autoroute any design:

- Define etch grids—This is especially important if you want to use grided routing.

  Note: For more information, see Defining an Etch Grid on page 70.

- Define Cross Section (layer stackup)—You might want to add routing layers prior to automatic routing. You can define the positive and negative layers and set visibility for plane layers, such as `VCC` and `GND`. Ensure that you have set internal plane layers to negative. If you have a split plane on a layer, set it to negative.

  Note: For more information, see Lesson 2-5: Setting the Plane Layers to Plane on page 56.

- Define appropriate constraints and properties—Check constraint rules and routing related properties. You can define the following:

  - Properties—Lesson 2-3: Setting Properties on page 47
  - Constraints—Lesson 2-4: Setting Constraints on page 53
  - Design Rules—Lesson 2-2: Setting Design Rules on page 41

- Manually route critical nets—You can manually route critical nets using the `add connect` command.

  Note: For more information, see Lesson 3-1: Creating Connection Lines on page 69.

- Check existing etch for `NO_RIPUP`, `NOROUTE`, `FIXED`, and `NO_GLOSS` properties, and add these properties if needed. Ensure that you set the value to `TRUE` for the PCB Router to process these properties.

Property	Function

NO_RIPUP	Prevents the PCB Router from removing any etch from the specified net. However, if you add any connections to a net after you assign this property, the router removes the etch from these new connections.
NO_ROUTE	Prevents the PCB Router from routing any missing connections on the specified net.
FIXED	Prevents the PCB Router from moving or deleting objects. This property also prevents the PCB Router from ripping connections in nets and glossing nets. You can attach this property on components, symbols, nets, pins, vias, clines, lines, filled rectangles (frectangles), rectangles, shapes, and groups.
NO_GLOSS	Prevents the PCB Router from glossing nets.

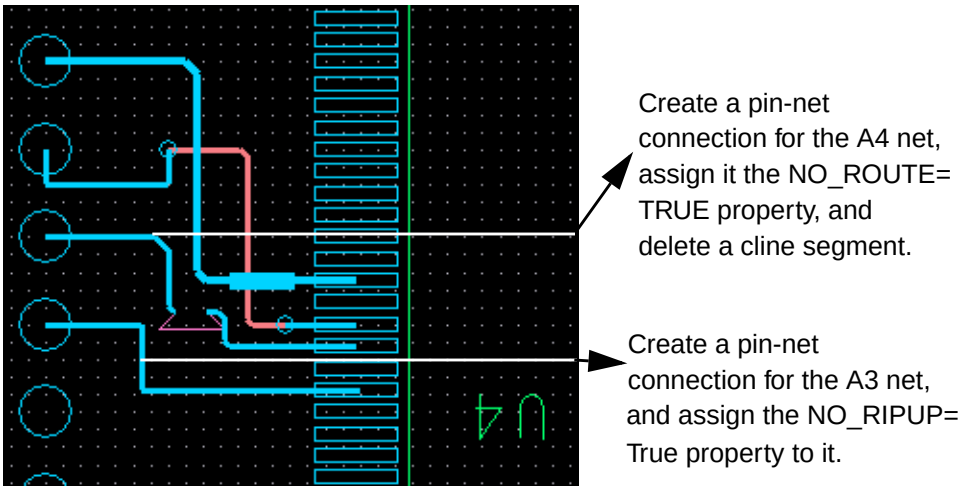
- Run router checks—For more information, see Lesson 2-6: Running Router Checks on page 60.
- Save your work—It is important to save your work to prevent any loss of settings that you have added thus far.

Summary

In this lesson, you learned the different steps you need to run before you autoroute a design.

Exercise

Assign the following properties to different nets in the `a6_5.brd` file as shown in following figure, and save the board file with the name `auto_routing_ready.brd`.



1. Assign the `NO_ROUTE=TRUE` property to the A4 net.

   (Hint: See Lesson 3-1: Creating Connection Lines on page 69 on how to create a connection and delete connection segments.)

2. Assign the `NO_RIPUP=TRUE` property to the A3 net. After assigning the property, create a pin-net connection as shown in the figure.

3. Save the board file as `auto_routing_ready.brd`.

You will see how these properties are handled by the PCB Router in Lesson 4-2: Using the Automatic Router Dialog Box on page 96.

Lesson 4-2: Using the Automatic Router Dialog Box

Overview

In this lesson, you will learn how the Automatic Router works.

Concept

You define parameters for automatic routing through the Automatic Router dialog box.

You can access this dialog box by:

➤ Close *Route – Route Automatic*.

or

➤ Type `auto_route` and press `Enter` in the command window.

The Automatic Router dialog box is a tabbed dialog box with four tabs. The default tab in the Automatic Router dialog box is *Router Setup*. Each tab in the Automatic Router dialog box lets you configure specific routing parameters. You can choose any tab by clicking it.

Router Setup Tab

Use this tab to define a high-level strategy by selecting which set of parameters to follow when routing.

- **Strategy**—You can choose one of three modes by selecting the appropriate option in the Strategy box.:
  - Routing passes mode
  - Smart router mode
  - Do file mode

  Based on your Strategy selection, parameters in remaining strategies will become unavailable. For example, if you select the Routing Passes mode, the options in Smart Router tab will become unavailable.

  Note: For more information about do files or using them in autorouting, see Lesson 4-8: Making Changes in a do File for Autorouting on page 130.

- **Options**—This section defines how the autorouter routes across layers. You can restrict via creation; set diagonal routing or limit wraparounds.

- **Wire grid**—Lets you set the X, Y wire grid spacing and the offset from where the grid originates. Values are in user-defined units.
- **Via grid**—Lets you set the X, Y via grid spacing and the offset from where the grid originates. Values are in user-defined units.
- **Routing Subclass/ Routing Direction**—Displays a list of etch subclasses of Etch/Conductor type on which you can perform routing. Each etch layer can be enabled or disabled for routing. When enabled, Routing Direction for that layer can be set to horizontal, vertical, or both (orthogonal). If orthogonal routing is enabled, you can also choose either positive or negative diagonal routing or both.
- **Protect**—Causes all clines on the specified layer to be fixed so they cannot be ripped up during routing.

Routing Passes Tab

Parameters in this tab are active only when *Specify routing passes* in the *Router Setup* tab is checked.

- **Preroute and route**—Lets you set the routing actions that you want to perform in a specific sequence. You can use the arrow buttons to the left of each row to set the order of routing passes. You can modify the sequence. You can set the routing actions that you want to perform and set the number of passes for each valid action (fanout, route, and clean).
- **Params**—Lets you set additional parameters for various action types in the Automatic Router Parameter Dialog Box. The dialog box opens to the tab that corresponds to the item you have highlighted in the Preroute and route section--for example, the Bus Routing tab.

  Note: For more information about SPECCTRA Automatic Router Parameters dialog box, see Lesson 4-3: Understanding Router Setup on page 106.
- **Clear**—Removes all Preroute and route entries.
- **Post Route**—This section contains a set of items for controlling post-route actions. The items are active only if you selected the *Specify routing passes* strategy in the Router Setup tab. The commands you select are run from top to bottom. You can set

additional parameters for *Spread wires* and *Miter corners* commands.

Note: For more information about post route commands, see Lesson 5-2: Using Post Routing Commands on page 153.

Smart Router Tab

The items in this tab are active only when you choose the *Use smart router strategy* in the Router Setup tab.

- **Grid**—Allows you to set minimum via grid and minimum wire grid values/ The default value is 1.
- **Fanout**—Sets fanout routing. When you select fanout routing, you can set fanouts to share vias on the same net. You can also set fanouts to escape to through-pins on the same net.
- **Generate testpoints**—You can set the locations where you want to generate testpoints. This could be at top, bottom or at both top and bottom. You may define a grid for testpoints too.
- **Miter after route**—Allows mitering after routing.

  Note: For more information about smart routing, see Lesson 4-6: Using Smart Routing on page 120.

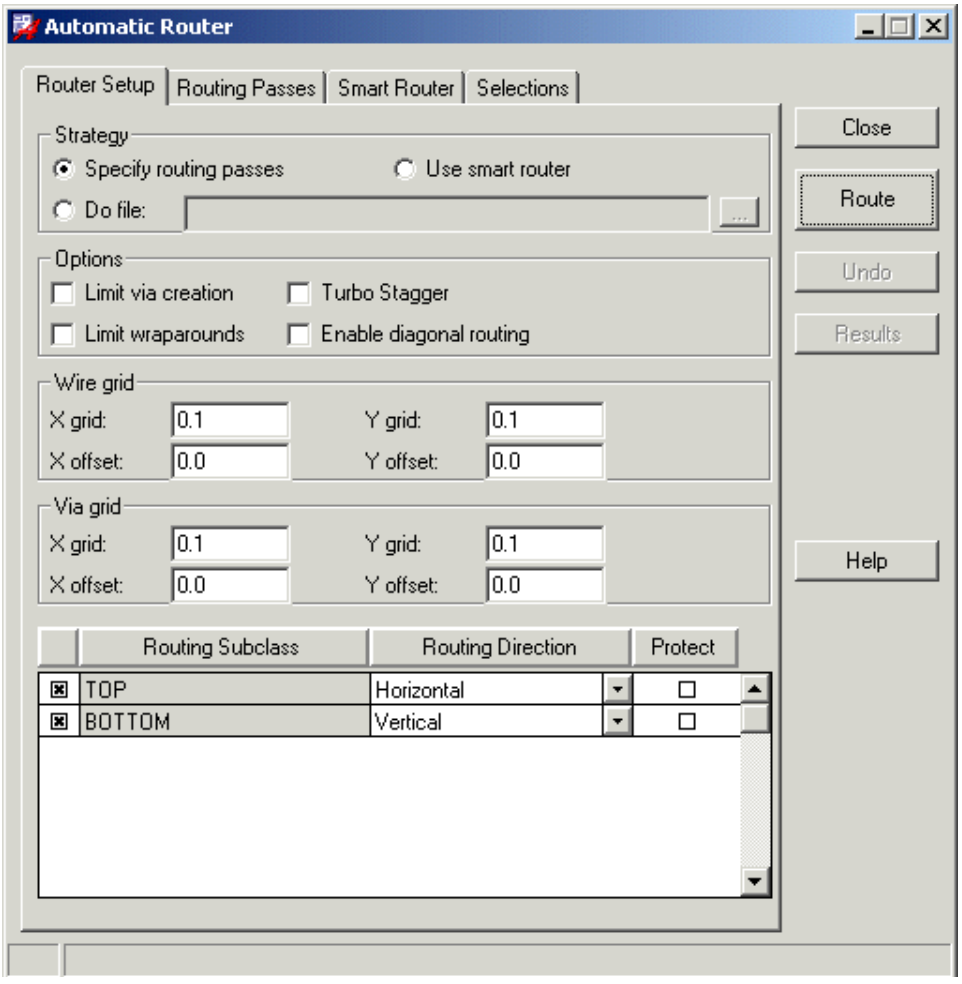
Selections Tab

- **Objects to route**—Define whether you want to route the entire design or specific nets and components. You may choose specific nets and route them or route all nets, while leaving a few selected nets untouched.
- **Available objects**—Lets you select, by way of the *Object type* field, nets and/or components to route or to keep from being routed. The Filter field lets you limit the objects in the list by displaying only objects of the selected type.
- **Select all in list**—Moves all the listed objects to the *Selected Objects* section.
- **Selected Objects**—Displays objects selected from the Available objects list.
- **Deselect all**—Removes all items from this list.

Note: This tab is not available through the `route_by_pick` command.

Procedure

1. Open the `auto_routing_ready.brd` file in the PCB Editor.
2. Ensure that only `Top` and `Bottom` layers are selected in the *Visibility* tab.
3. Chose *Route – Route Automatic*.



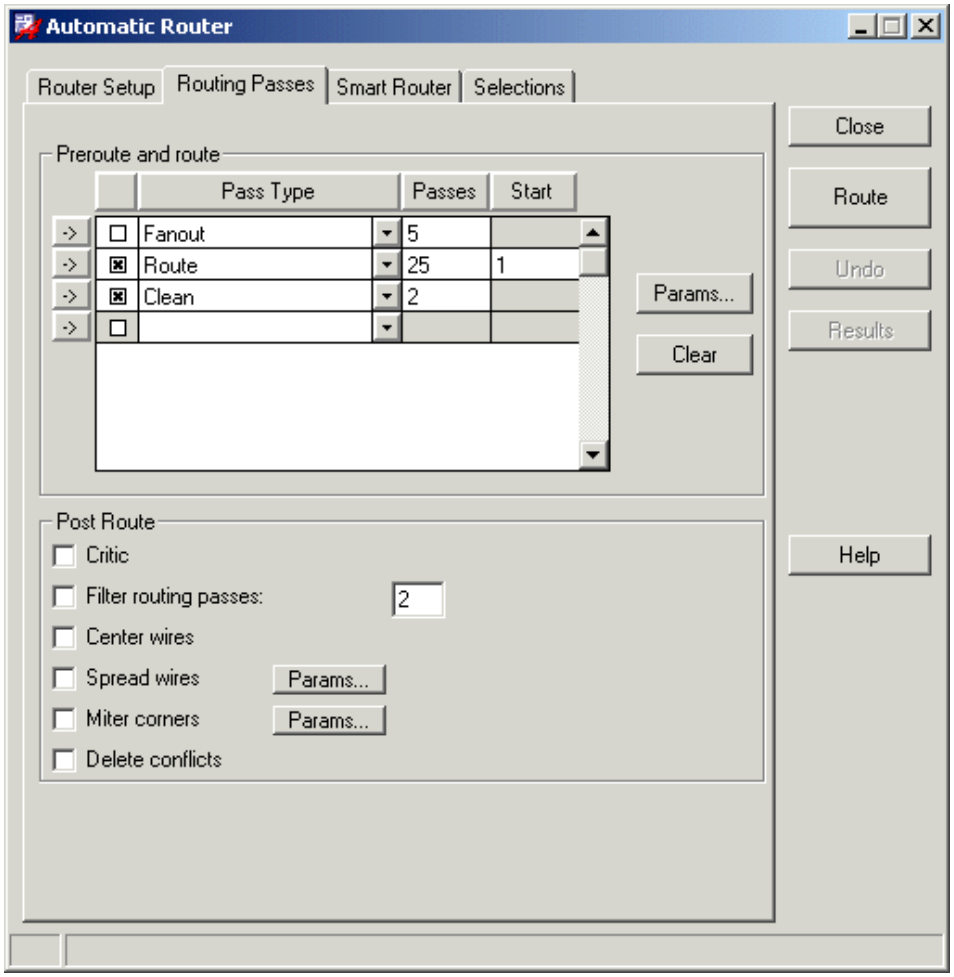
The Automatic Router dialog box appears with the *Router Setup* tab selected. Notice that the selected routing strategy is *Specify routing passes*.

4. Click different tabs and notice grayed options.

Options in the Routing Passes tab are available for selection while the options in the Smart router tab are not available for selection.

5. Click the *Routing Passes* tab.

   The *Routing Passes* tab is selected.



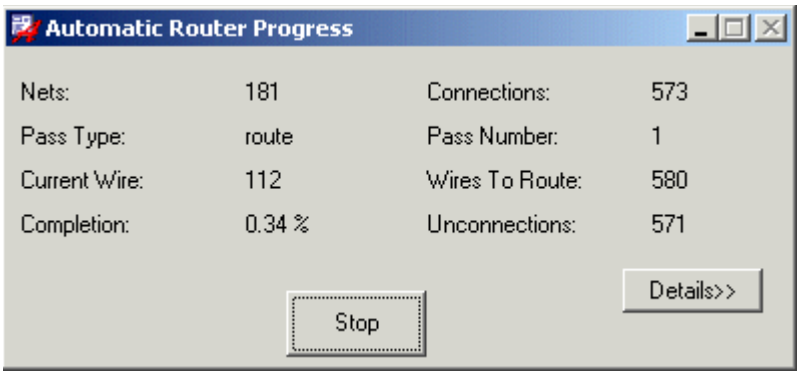
Notice that 25 routing passes and 2 clean passes are selected. For different designs, you may like to change these passes and select or delete more commands for routing. Changing these options is covered in later exercises. As of now, leave them unchanged.

6. Switch to the *Router Setup* tab.

   The wire grid and via grid are set at .1 mils. Do not make any changes to the parameters.

7. Click *Route* to begin routing.

   The PCB Router begins routing the design. The `auto_routing_ready.brd` file is being converted to `auto_routing_ready.dsn` file. The Automatic Router Progress window appears detailing the progress.



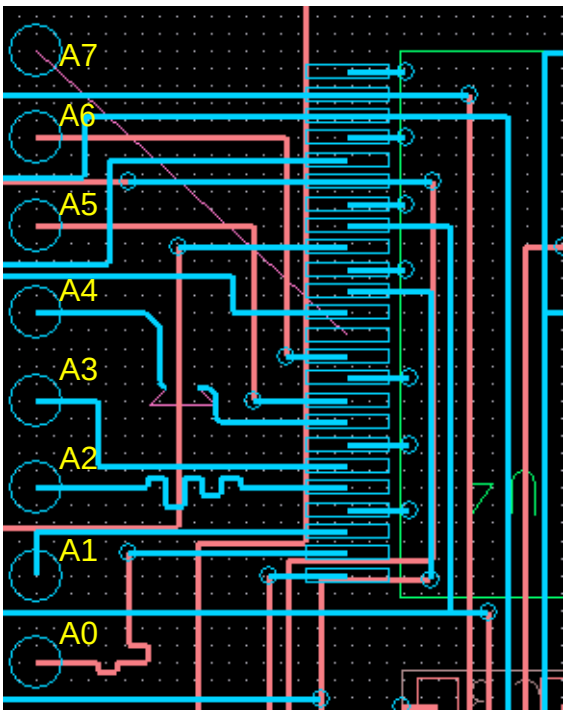
   You can click *Details* button to see a consolidated report that details the result of each routing pass.

   Note: For more information about routing progress report, see Lesson 5-1: Understanding Routing Results on page 149.

   When routing is completed, the Automatic Router Progress window disappears and the Automatic Router dialog box appears with *Undo* button available. If you are satisfied with routing results, click *Close* else click *Undo* and start again.

8. Click  to minimize the Automatic Router dialog box.

Zoom in to view routing for the A0, A1, A2, A3, A4, A5, A6, and A7 nets.



Notice that the routing for the net A3 has got changed. This net had a NO_RIPUP property assigned to it. An etch for the A3 net was created after the property assignment. An etch created after assigning of the NO_RIPUP property is routed by the autorouter.

The A0, A1, A2, and A3 nets had a match group defined in Lesson 2-3: Setting Properties on page 47. This match group results the A0, A2, and A3 nets to share a relative propagation delay with the A1 net defined as the target net.

The A4 net is assigned the NO_ROUTE property. This prevents any routing for any cline segment on the net. Notice that the etch that was deleted previously is left untouched.

The A5 and A6 nets did not have any routing-impacting property attached. These nets had an etch created. These etches are ripped off and new optimized etches are created.

The A7 net is assigned the FIXED property. The autorouter leaves this net untouched. No connection is drawn for it.

Note: Based on the etches you created in the

`auto_routing_ready.brd` file, minor differences in routing may appear in your board.

9. Maximize the Automatic Router dialog box and click *Undo* to remove all nets.

   You will route the connections again for the selected nets. You will route all nets except nets A5 and A6.

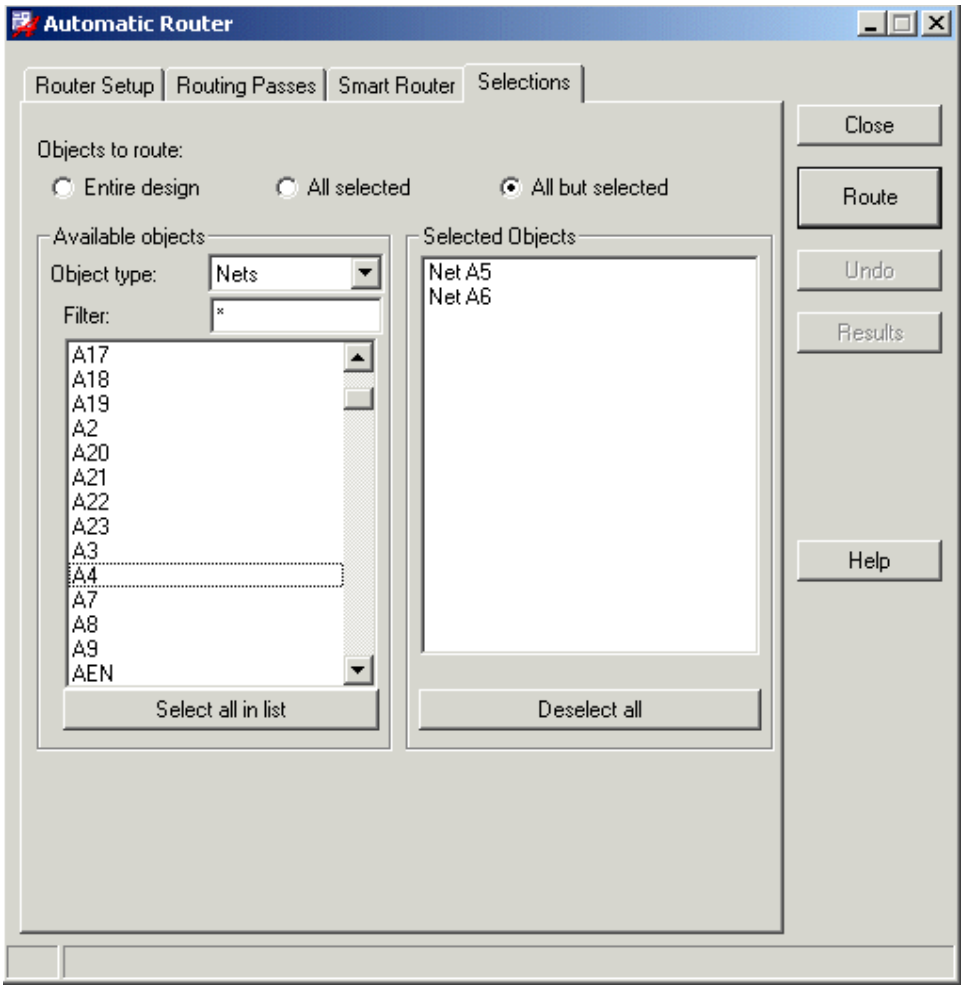
10. Click the *Selections* tab.

11. Click *All but selected* radio button.

12. Set the *Object type* in the *Available Objects* box to *Nets.*

13. Click *A5 and A6* in the *Filter* list.

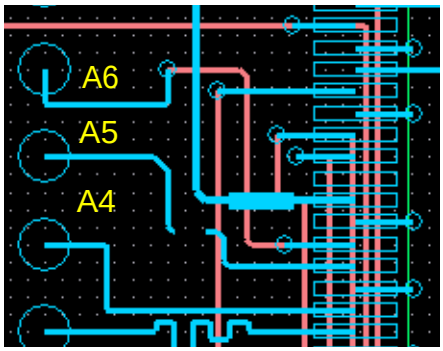
    Ensure that the Automatic Router dialog box shows the following settings:



14. Click *Route.*

Routing results appear on the screen.

15. Zoom in around nets `A5` *and* `A6`.



The connections for the nets `A5` *and* `A6` remain untouched and other nets are routed.

16. Click *Close* to finish routing.

17. Choose *File – Save As*.

18. Save the file with name `auto_routed.brd`.

Summary

You learned the functions of different options in the Automatic Router dialog box. By controlling these options, you can determine how to autoroute a design. You can choose a routing strategy and then optimize it. You can choose specific nets for routing.

Note: For more information about routing specific nets, see Lesson 4-9: Routing Individual Nets on page 137.

Note: For more information about understanding routing results, see Lesson 5-1: Understanding Routing Results on page 149.

Lesson 4-3: Understanding Router Setup

Overview

In this lesson, you will learn the functions of different options in the Automatic Router Parameters dialog box and use the information to route a design.

Concept

You can access the Automatic Routers Parameters dialog box in multiple ways:

- Click the *Params* button for any post route command in the Automatic Router dialog box.
- Choose the setup option for the following commands:
  - *Route – Fanout By Pick*
  - *Route – Net(s) By Pick*
  - *Route – Elongation By Pick*
  - *Route – Miter By Pick*
  - *Route – UnMiter By Pick*

The Automatic Routers Parameters dialog box has the following tabs:

Fanout Tab

Routes short pin escape wires from pins to vias. Lets you control pin and via sharing, set the layer depth, control the escape direction, and set a temporary grid.

Note: For more information on setting options in the Fanout tab, see Lesson 4-11: Using Fanout By Pick on page 145.

Fanout Grid

Allows the autorouter to automatically calculate initial via grids that permit one wire or two wires between adjacent vias. This depends on the grid choice specified in this section.

Bus Routing Tab

Routes component pins that share the same, or nearly the same, X or Y coordinate.

Seed Vias Tab

Breaks a single connection into two shorter connections by adding a via.

Testpoint Tab

Assigns test points to signal nets.

Spread Wires Tab

Adds extra space between wires, and between wires and pins. The PCB Editor adds extra wire-to-wire, wire-to-SMD pad, and wire-to-pin clearances to improve PCB manufacturability. Extra clearances are created by moving wires without moving or adding vias.

Miter Corners Tab

Lets you change 90-degree wire corners to 45 degrees for wires exiting pins and vias.

Note: For more information on setting options in the Miter Corners tab, see Lesson 4-10: Mitering and Unmitering Connections on page 142.

Elongate Tab

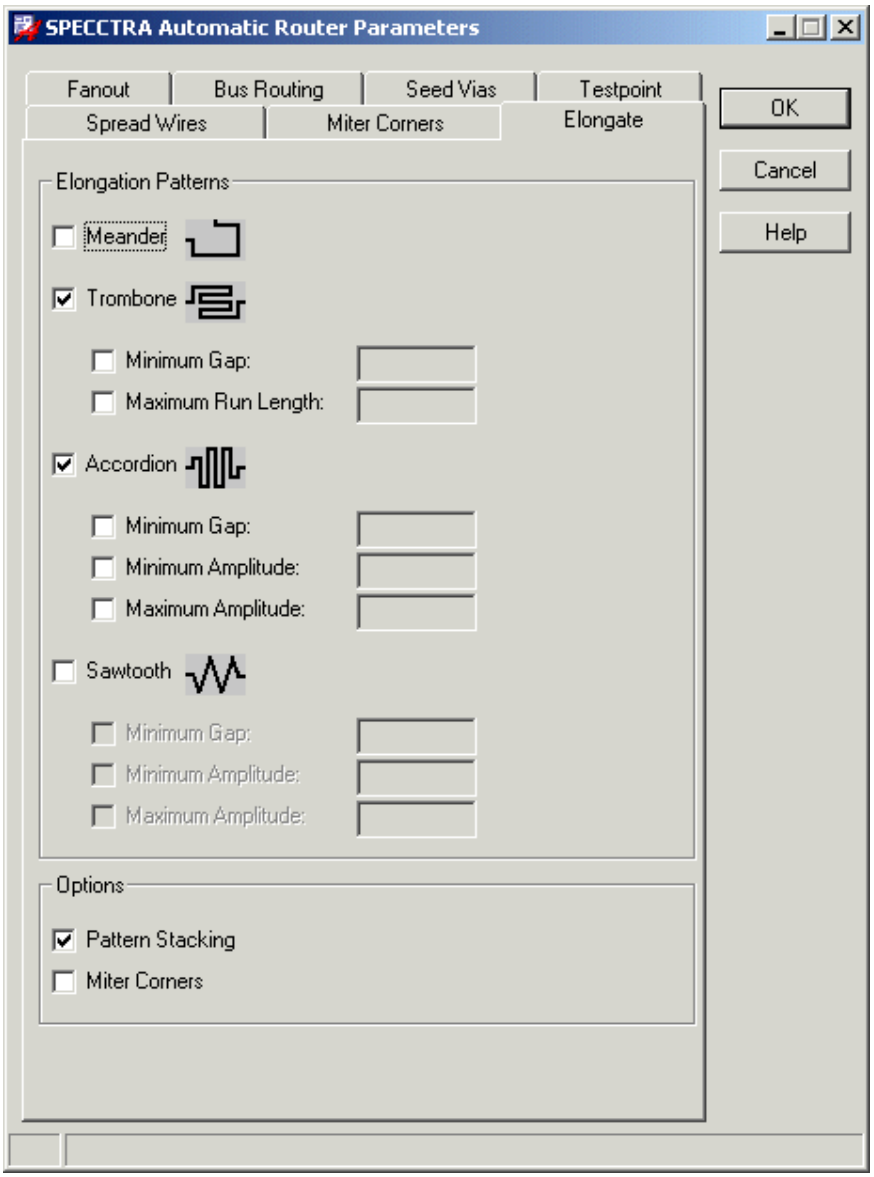
Increases etch length to adhere to timing rules.

You will learn to use the Elongate tab in this lesson. The `timing_error.brd` file has a net `mclk` that has the PROPAGATION_DELAY property assigned. This net has a connection that does not conform to the timing property. Use *Route - Elongation by Pick* command to increase the etch length to conform the timing property.

Procedure

1. Open the `timing_error.brd` file in the PCB Editor.
2. Focus on the `mclk` net. This net has a DRC.
3. Choose *Route – Elongation by Pick*.
4. Right-click and choose *Setup* from the pop-up menu.

The Automatic Router Parameters dialog box appears with the Elongate tab selected.



Notice that the *Trombone* and *Accordion* check boxes are selected indicating that the PCB Router can use a trombone or accordion shape (as shown in the dialog box) to add length to the selected net.

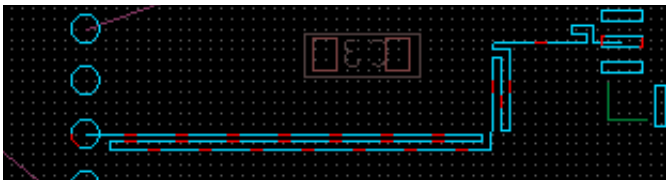
Minimum Gap—Specifies the spacing between etch when the autorouter uses accordion, sawtooth or trombone elongation patterns.

Maximum Run Length—Specifies the maximum length of a routed connection when the autorouter uses the trombone elongation pattern.

5. Do not change any options in the Automatic Router Parameters, and click *OK*.
6. Choose the `mclk` net.

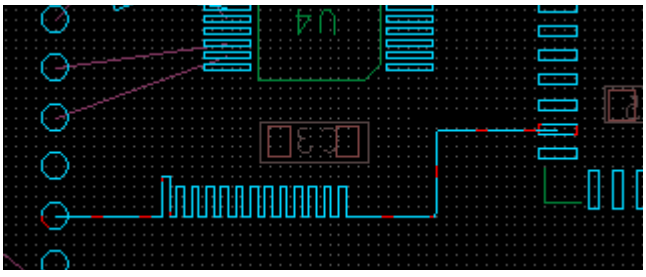
   The Automatic Router progress box appears detailing the routing progress status.

   The net is routed as shown below. Notice that the DRC is fixed.



7. Right-click and select *Oops* from the pop-up menu.
8. Right-click and select *Setup* from the pop-up menu.
9. Set the *Trombone* check box to `OFF`.
10. Click *OK*, and select the `mclk` net.

    The net is routed differently as shown below.



11. You can modify more options.
12. Close the `timing_error.brd` file without saving it.

Summary

You learned the functions of different options in the Automatic Router Parameters dialog box and used the *Route – Elongation by Pick* command to add length to a net requiring timing delay.

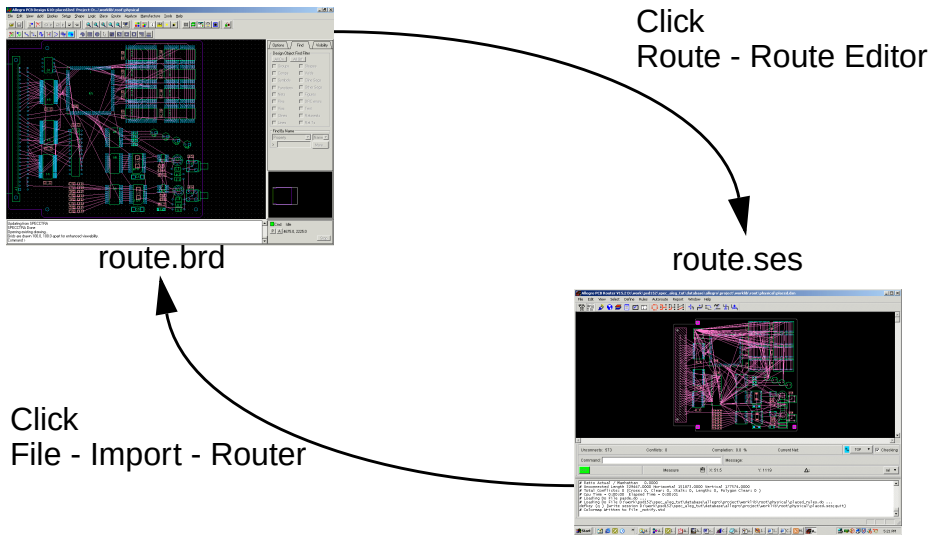
Lesson 4-4: PCB Editor/PCB Router Design Flow

Overview

In this lesson, you will learn how data flows between the PCB Editor and the PCB Router.

Concept

The data flow between the PCB Editor and the PCB Router can be shown by the following diagram:



When you launch the PCB Router from the PCB Editor (using *Route - Route Editor* command), the PCB Editor writes a `filename.dsn` (design file) that is used as an input by the PCB Router. The PCB Router window then starts automatically.

After selecting parameters or importing custom parameters (for example, `.do` files), you can start routing from the PCB Router.

When routing is complete, you are prompted to write a `filename.ses` (session file) that can be imported into the PCB Editor. The PCB Editor will expect to import a file with a similar name. For example, if you start with a PCB Editor file named `route.brd`,

the PCB Router creates a `route.dsn` file and expects to read back a `route.ses` file after routing.

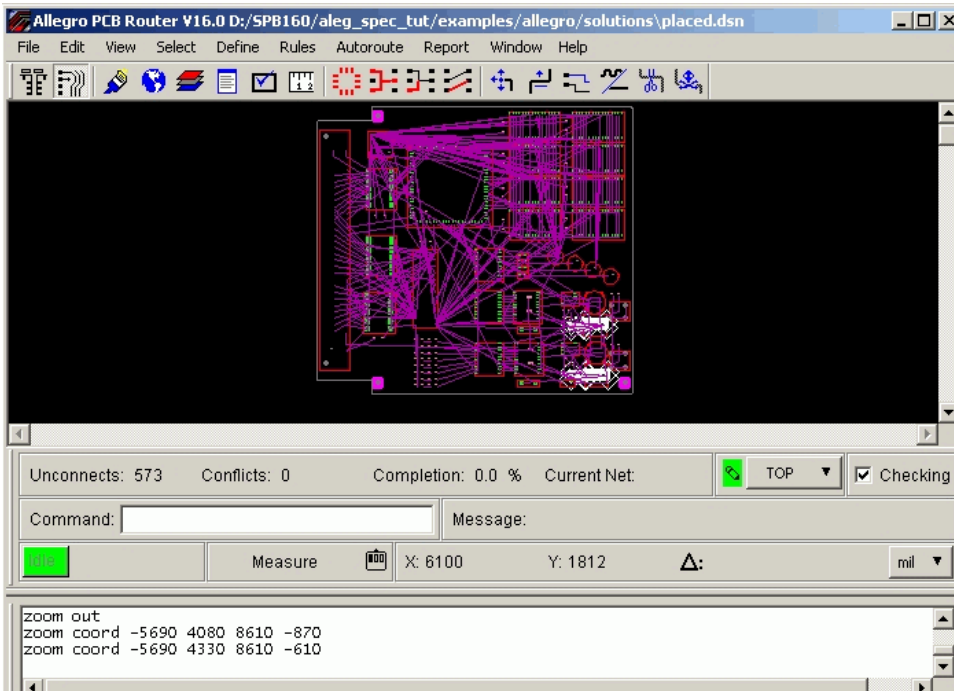
Upon quitting from the PCB Router window, you are returned to the PCB Editor, and connections are updated automatically.

Procedure

Note: The PCB Router user interface section covered in this exercise is for demonstration purpose only. For more information about using the PCB Router user interface, see the Cadence documents *Allegro PCB Router Tutorial* and *Allegro PCB Router User Guide*.

1. Open the `flow_demo.brd` file in the PCB Editor.
2. Choose *Route – Route Editor.*

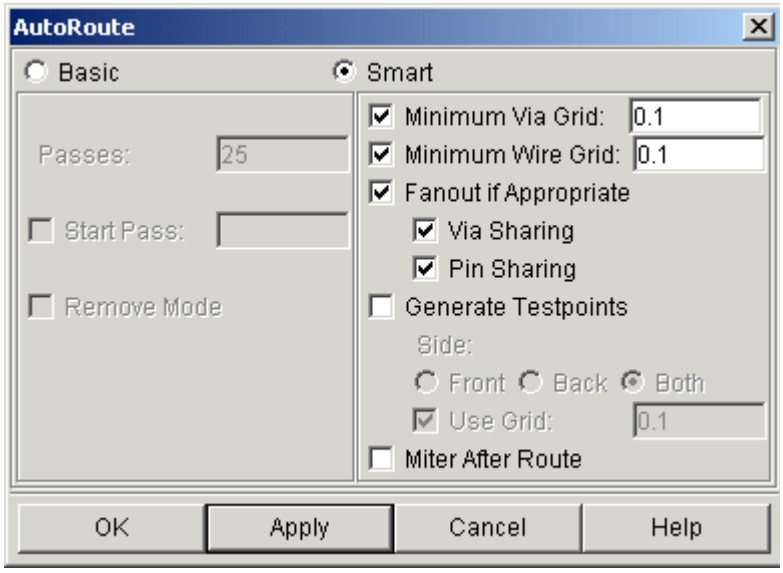
   The PCB Router opens.



   Read the history in the command window. The design name file is `flow_demo.dsn` and the `did` file is `specctra.did`.

3. Choose *Autoroute – Route*.

The Autoroute dialog box appears.

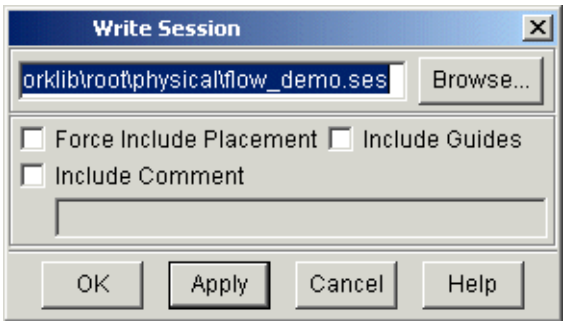


4. Click *OK* to autoroute in the smart mode.

   The PCB Router routes connections and displays a message `Smart_route completed` in the console window.

5. Choose *File – Write – Session.*

   The Write Session dialog box appears.



6. Click *OK* to save the session file in the same folder as the board file.

   The session file is saved. Notice the console window displays the path of the saved session file.

7. Choose *File – Quit.*

The Quit window appears displaying the *Delete Did File* check box. The PCB Router creates a did file, which records all the commands you entered while in the PCB Router.

8. Click *Quit*.

   The PCB Router closes and you are back in the PCB Editor. Note that the PCB Editor quickly updates the routing as it was done in the PCB Router.

   You will now close the `flow_demo.brd` file without saving it, then reopen it using the `flow_demo.ses` file to import the routing.

9. Choose *File – Open*.

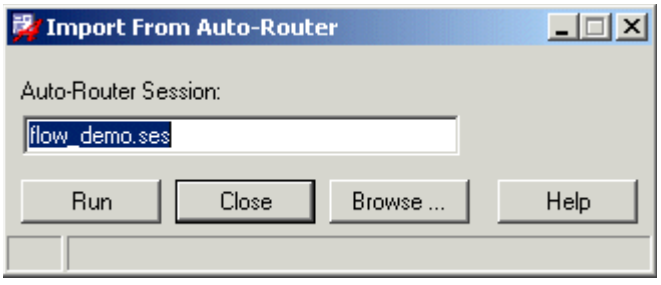
   You are asked whether you want to save changes in the `flow_demo.brd` file.

10. Click *No.*

11. Choose the `Flow_demo.brd` file in the browser to open it.

12. Choose *File – Import – Router.*

    The Import From Auto-Router dialog box appears with `flow_demo.ses` file selected for import.



13. Click *Run.*

    The PCB Editor uses the `flow_demo.ses` file to update the routing done in the PCB Router.

14. Click *Close*.

15. Close the `flow_demo.brd` file without saving it.

Summary

You learned to exchange data within the PCB Router and the PCB Editor. You will find this data flow useful in implementing Highspeed Model or Highspeed Power User Model as a task flow for routing designs (as covered in Lesson 2-7: Selecting a PCB Router Task Flow Model on page 63).

Lesson 4-5: Using Basic Autorouting Commands

Overview

In this lesson, you will learn to perform basic autorouting commands:

- Bus
- Fanout
- Route
- Clean

Concept

You can use the Automatic Router dialog box to set basic routing commands. These commands can be set in the Automatic Router dialog box - Routing Passes tab. The following table lists the functions of basic routing commands.

Command	Description
Bus	Routes component pins that share the same, or nearly the same, X or Y coordinate. This command is useful for rerouting memory arrays, backplanes, and other pins that share a common X or Y coordinate.
Fanout	Routes short pin escape wires (SMD pads and through-pins) from pins to vias.
Route	Routes with conflicts, and after the first five passes, reroutes only connections involved in conflicts. Escapes SMD pads to vias as needed.

Command	Description
Clean	Rips up and reroutes all connections. Adding new conflicts is prohibited.

An important part of autorouting strategy involves choosing which routing commands to use and when to use them. Each routing command can have multiple passes.

During the first routing pass, the autorouter allows conflicts to route every connection. After the first routing pass, the cost for creating these conflicts increases with each pass.

During the first five routing passes, all connections are ripped up and rerouted. After the first five routing passes, the strategy changes, and only wires involved in conflicts are ripped up and rerouted. Wires that are not involved in conflicts are ignored during this phase. By changing the number of passes and order of routing commands, you can achieve better results. In this lesson, you will learn some of these techniques.

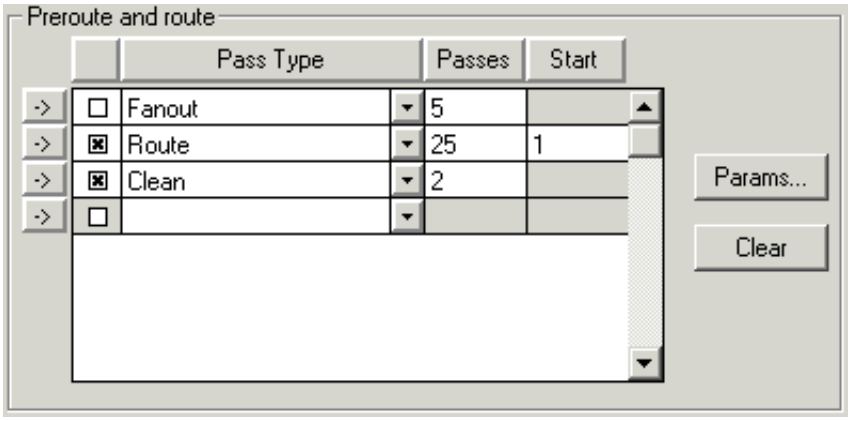
Procedure

1. Open the `auto_routing_ready.brd` file in the PCB Editor.
2. Choose *Route – Route Automatic*.
3. Ensure that the *Specify routing passes* radio button is selected in the *Strategy* box of the Router Setup tab.
4. Choose the Routing Passes tab.

   The Routing Passes tabbed page appears.

   The preroute and route section is the place where you define basic autorouting commands. You can define a new command,

delete a command, change command order and define the number of passes for each command.



To change a bus command, click the arrow next to an existing command and select the new command.

5. Click the arrow next to *Fanout* and choose *Bus*.

   Notice that the *Bus* command is added to the list and the check box against it is automatically selected. This check box denotes that autorouter will perform this command.

   Note: If you click the *Params* button, the Automatic Router Parameter dialog box appears where you can set routing parameters. For more information, see *Lesson 4-3: Understanding Router Setup* on page 106.

6. To add a new command for *Fanout*, click the arrow next to the vacant *Pass Type* (below *Clean*) and choose *Fanout.*

7. To delete the *Clean* command from the list, right-click the arrow to the left of *Clean* command and choose *Delete.*

   To add a new command in the middle of list, right-click the Arrow button to the left of an existing command, and choose *Insert.* Next, select the new command from the *Pass type* drop-down list.

8. Right-click the Arrow button to the left of *Fanout* command and choose *Insert.*

   A blank row appears between the *Route* and *Fanout* commands.

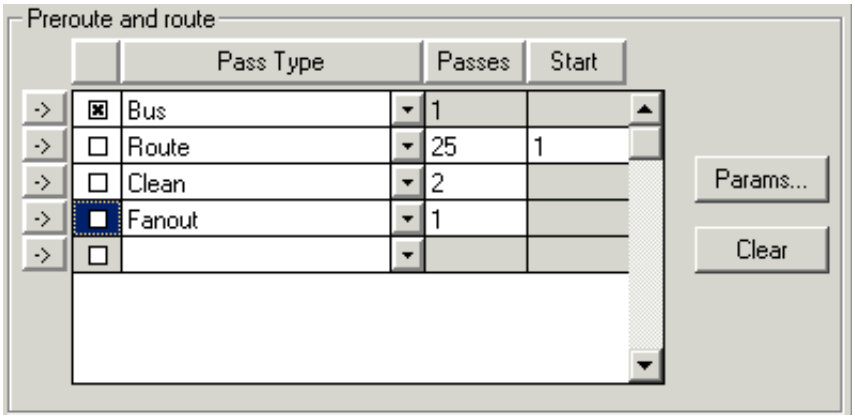
9. Choose *Clean* from the *Pass Type* drop-down list.

10. To change the number of passes for the *Clean* command, type 2 in the *Passes* field for the *Clean* command.

You can have a command in the *Pass Type* list and yet not run it. For this, clear the check box against it.

11. Clear the check box next to the *Route, Clean and Fanout* commands.

You should have the following setup.

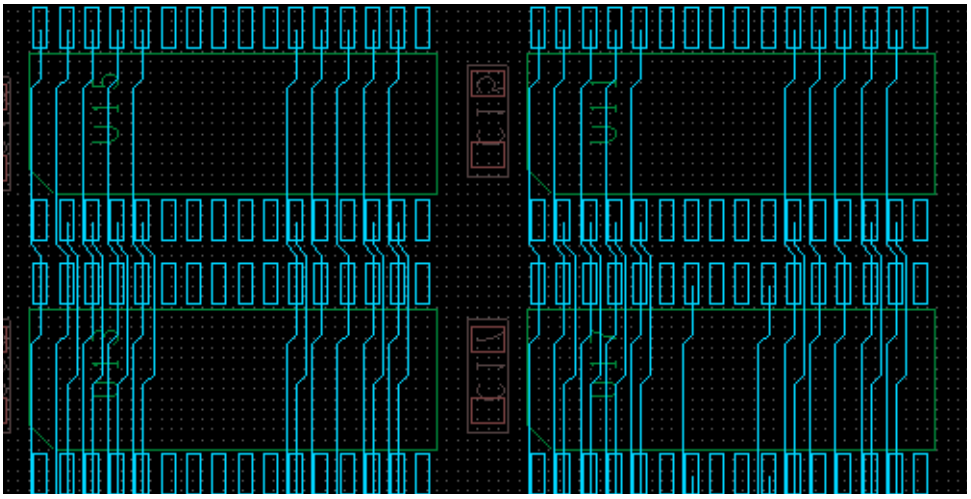


Notice that four basic autorouting commands are available and only one (the *Bus* command) is selected for routing.

12. Click *Route*.

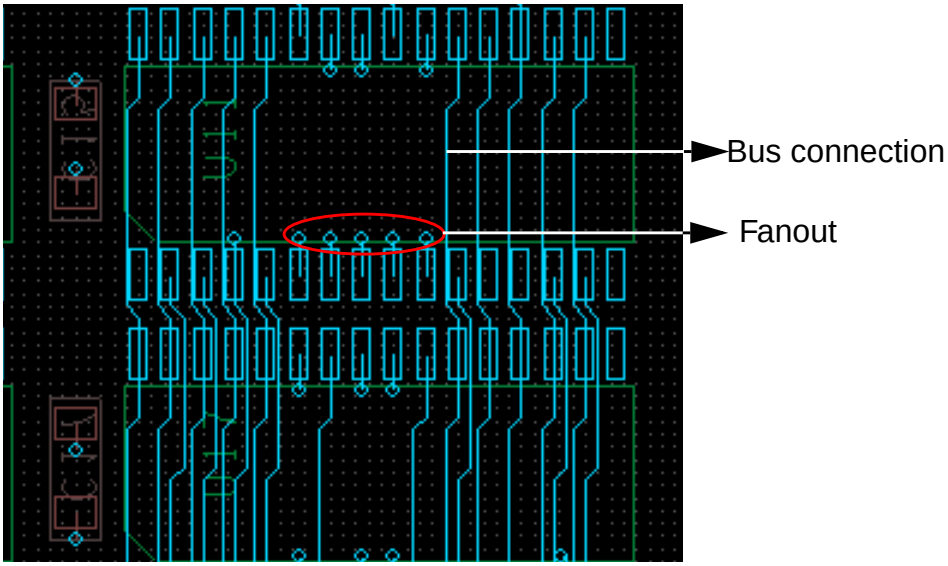
The autorouter routes the design. Focus on the components U10 to U17. These components have pins that share the same, or

nearly the same, X or Y coordinate. These have a bus routing. The other components are not routed.



13. Choose the check box corresponding to the *Fanout* command and then choose *Route*.

The autorouter routes the design. Besides the *Bus* command routing, the autorouter now creates escape wires from SMD pads and through-pins to vias.



Notice that most pins are still not routed.

14. Choose the check box corresponding to the *Route and Clean* commands.

15. Choose *Route*.

    The autorouter routes the entire board. All pin-net connections are created and no DRC is reported.

16. Click *Close* to exit the Automatic Router dialog box.

17. Choose *File – Save As*.

18. Save the file with name `bus_route_clean_fanout.brd`.

Summary

You learned to perform basic autoroute commands. By selecting the order of these commands and number of passes, you can control routing results.

Note: For more information about understanding routing results and causing convergence, see Lesson 5-1: Understanding Routing Results on page 149.

Lesson 4-6: Using Smart Routing

Overview

In this lesson, you will learn to use smart router to route a design.

Concept

The smart router sets wire and via grids, performs bus and fanout operations, and runs a series of route and clean passes until routing completes.

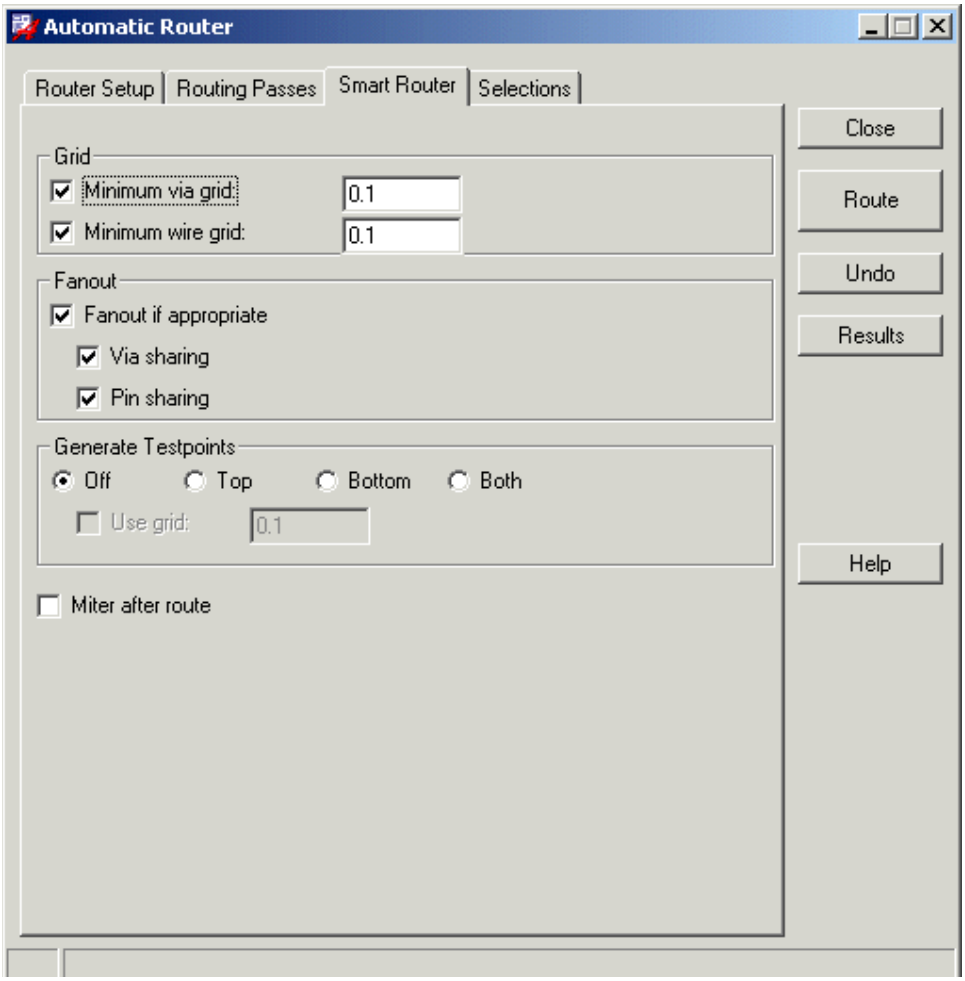
While the smart router is running, the autorouter monitors and analyzes routing progress. If it detects design problems, warning or error messages appear. If the autorouter reaches a point where further improvement is unlikely, it switches to a different method and completes as many connections as possible with zero conflicts.

Procedure

1. Open the `auto_routing_ready.brd` file in the PCB Editor.
2. Ensure that only the `Top` and `Bottom` layers are selected in the *Visibility* tab.
3. Choose *Route – Route Automatic*.

   The Automatic Router dialog box appears.
4. Choose the *Use smart router* radio button in the *Strategy box.*
5. Choose the *Smart Route*r tab.
6. Select the *Minimum via grid* and *Minimum wire grid* check boxes and set their value to `0.1`.
7. Select the *Fanout if appropriate* check box.
8. Choose the *Via sharing* and *Pin sharing* check boxes.

The Automatic Router dialog box should display the following values:



9. Click *Route*.

   The design is routed.

10. Click *Close* to exit from the Automatic Router dialog box.

11. Save the board file with the name `smart_routed_gui.brd`.

Summary

You learned to smart route a design. When you use the Smart routing option, the PCB Router adjusts the autorouting strategy based on the conflict reduction rate, the routing completion rate, the failure rate,

and the number of layers. It applies bus routing, if necessary, and runs clean passes after all connections are completed.

Lesson 4-7: Fixing Common Warnings

Overview

In this exercise, you will learn to identify and resolve common warnings that occur during routing a design

Concept

Before you route a design, it is recommended that you run a router check and resolve the warnings and errors.

Lesson 2-6: Running Router Checks on page 60 explains how you can quickly perform standard routing checks. This lesson explains how to resolve the following warnings:

1. keepin(Warn): Route keepin not defined.
2. vias(Warn): There are no vias available for routing
3. linewidth0(Warn): 1 nets have minimum line width of Zero
4. cnsoff(Warn): Some electrical constraints exist but have the check turned off

   Note: The above warning is detected in the Allegro PCB Design HDL XL product suite.
5. packagekeepin(Warn): Package keepin not defined.
6. packagekeepin(Warn): Package keepin is not within route keepin.
7. spacingvalues(Warn): Some of the clearance rules defined in Cset <*name_of_CSet*> will be different in the PCB Router.

Procedure

Understanding Bad Results

1. Open the `error_warnings.brd` file in the PCB Editor.
2. Choose *Route – Route Automatic.*

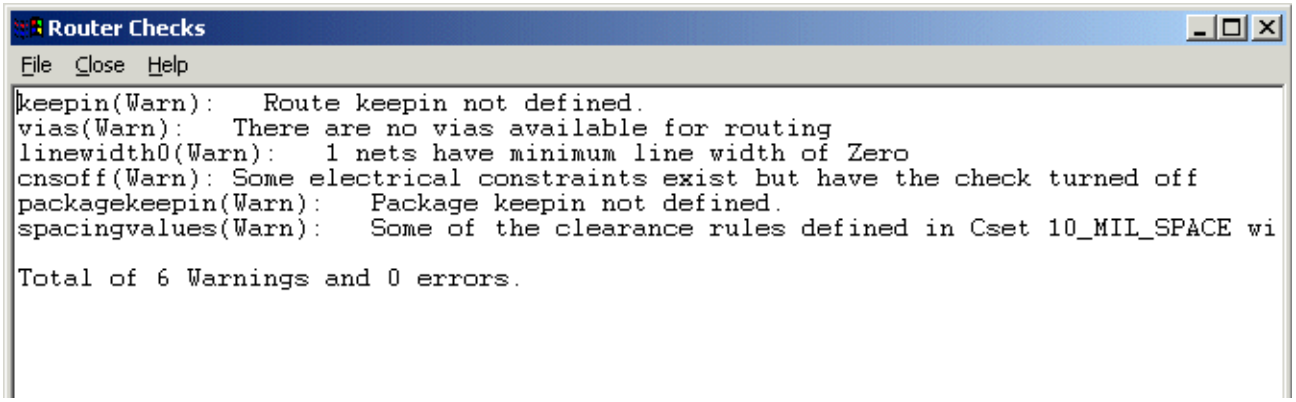
   Do not change any parameters in the Automatic Router dialog box.
3. Click *Route.*

   Notice that the routing progress is rather long one and numerous DRCs are generated after routing completion.
4. Click *Undo*.
5. Click *Close*.

Identifying Warnings

1. Choose *Route – Router Checks*.

   The Router Checks window appears displaying following warnings:



Fixing keepin(Warn): Route keepin not defined

You learned to define a route keepin in Defining Package and Route Keepin on page 37. Using your skills, create a route keepin that is of

same shape as the board outline and is offset 50 mils inside the board outline. After defining a route keepin, run Router Checks.

1. Choose *Edit – Z-Copy*.
2. In the *Options* tab, set class to `Route Keepin`, subclass to `All`, *Size* to *Contract* and *Offset* to `50`.
3. Click anywhere on the board outline.

   A route keepin is created.
4. Choose *Route – Router Checks*.

   The Router Checks window appears and it has 5 warnings. The warning on route keepin not defined is removed.

Fixing packagekeepin(Warn): Package keepin not defined.

You learned to define a package keepin in Defining Package and Route Keepin on page 37. Using your skills, create a package keepin that is of same shape as the board outline and is offset 20 mils inside the board outline. After defining a package keepin, run Router Checks.

1. Choose *Edit – Z-Copy*.
2. In the *Options* tab, set class to `Package Keepin`, subclass to `All`, *Size* to *Contract* and *Offset* to `20`.
3. Click anywhere on the board outline.

   A package keepin is created.
4. Choose *Route – Router Checks*.

   The Router Checks window appears and it has 5 warnings. The warning for package keepin not defined is removed.

   However, a new warning stating the package keepin is not within the route keepin appears.

Fixing packagekeepin(Warn): Package keepin is not within route keepin

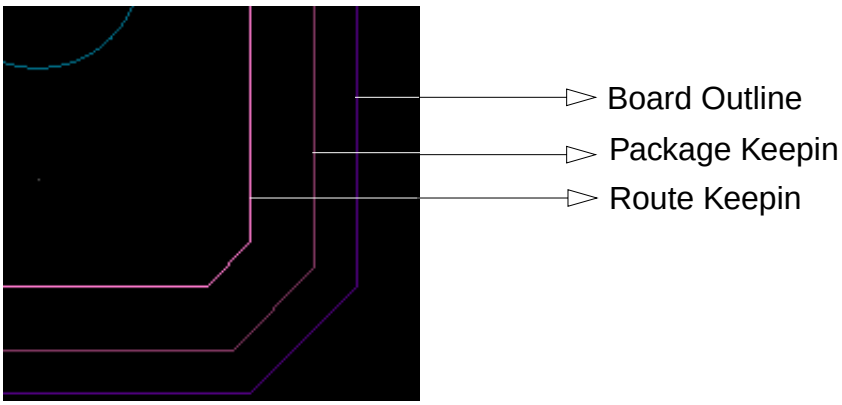
You will see this warning if the outline of the package keepin that sets the limits for where the components are placed extends past the route keepin area, where the routes are contained.

To fix the warning, delete the existing package keepin and recreate it so that it comes within the route keepin area:

1. Click the *Color* icon  .

   The Color and Visibility dialog box appears.

2. Choose *Areas* from the list.
3. Toggle ON the *Package Ki* and *Route Ki options* to make them visible.
4. Choose *Stackup* from the list.
5. Toggle the entire *ETCH* column to OFF.
6. Click *OK* to exit the dialog box.
7. Zoom in to look closer at any edge of the board.



   You will also see the borders of the shapes that define the package and route keepins.

8. Choose *Edit – Delete*.
9. In the Find Filter turn all objects OFF and toggle Shapes ON.
10. Click the outer Package Keepin line.
11. Right-click and choose *Done* from the pop-up menu.

12. Choose *Edit – Z-Copy*.
13. In the *Options* tab, set class to `Package Keepin`, subclass to `All`, *Size* to *Contract* and *Offset* to `70`.
14. Click anywhere on the board outline.

    A package keepin is created.
15. Choose *Route – Router Checks*.

    The Router Checks window appears and it has 4 warnings. The warning for package keepin is not within route keepin is removed.

Fixing vias(Warn): There are no vias available for routing

To fix the above warning assign a padstack to the Current via list in the Physical Rule Set of the board.

1. Choose the *Cns* icon  .

   The Constraints System Master dialog box appears.
2. Choose *Set Values* in the *Physical Rules Set* area.
3. Set the Constraint Set Name as *Default.*
4. Scroll down to the bottom of the list of *Available Padstacks*.

   This shows us a list of all the current board padstack names available in this design.
5. Click *VIA*, the last name in that list.
6. Click OK to exit the dialog boxes.
7. Choose *Route – Router Checks*.

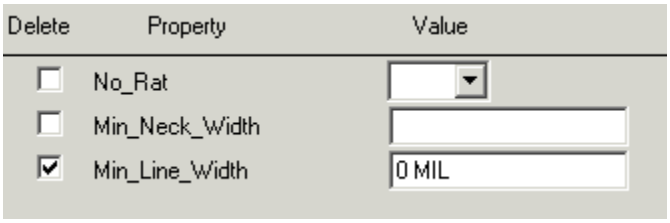
   The Router Checks window appears and it has 3 warnings. The warning for no vias being available for routing is removed.

Fixing linewidth0(Warn): 1 nets have minimum line width of Zero

The above warning occurs when one net is accidentally assigned a line width of 0. Search the property and change its value or remove it.

1. Choose *Edit – Properties*.
2. Set all objects `OFF`, then toggle *Nets* `ON`, in the Find Filter.
3. Choose *Property* in the *Find by Name* area of the Find Filter.
4. Type `m*` and press `Enter`.

   The Edit Property dialog box and the Show Properties window appear. Notice that net `A23` has `MIN_LINE_WIDTH=0` property.
5. In the Edit Property dialog box, set the following values and click *Apply*.



   Notice that the `MIN_LINE_WIDTH=0` property is removed from the `A23` net.
6. Click *OK* to close the Edit Property dialog box.
7. Choose *Route – Router Checks*.

   The Router Checks window appears and it has 2 warnings. The warning for nets having minimum line width of 0 is removed.

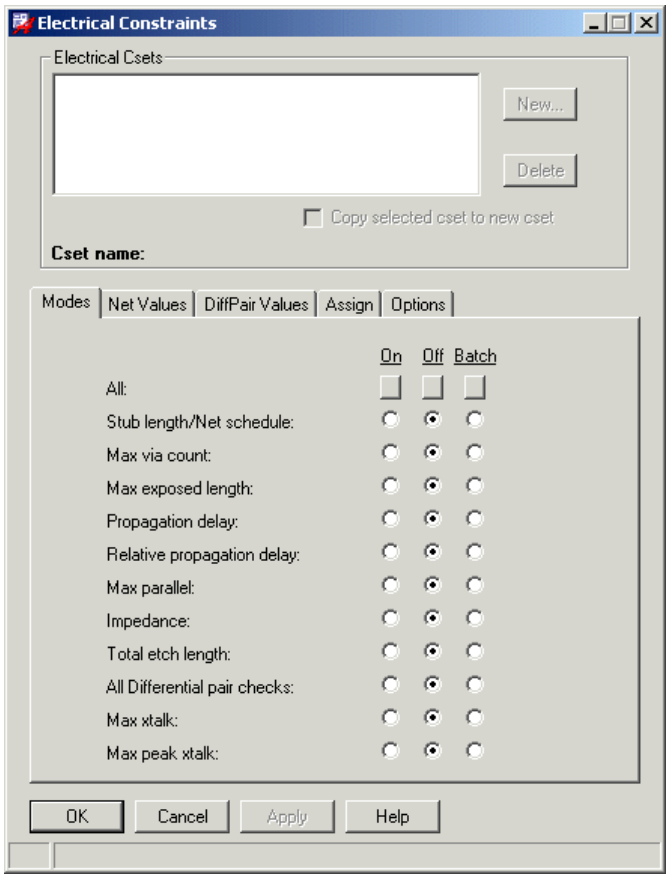
Fixing cnsoff(Warn): Some electrical constraints exist but have the check turned off

The above warning appears when electrical rules have been defined for a design, although they haven't been turned on to be checked. To fix the warning, turn on electrical checks.

1. Select the *Cns* icon  .

   The Constraints System Master dialog box appears.
2. Choose *Electrical Constraint Sets*.

The Electrical Constraints dialog box appears.



Notice that all checks in the *Modes* tab are turned off.

3. Click the ON radio button for *Propagation Delay* and *Relative Propagation Delay* to set the rules to be routed.
4. Click *OK* to exit all the forms.
5. Choose *Route – Router Checks*.

   The Router Checks window appears and it has 1 warnings. The warning for electrical constraints check not turned on is removed.

Fixing spacingvalues(Warn): Some of the clearance rules defined in Cset <name_of_CSet> will be different in the PCB Router

The above warning appears when you have set certain constraints in a spacing set that may not apply as is in the PCB Router. Typically, you can remove this warning by setting a consistent value to all fields in the Spacing worksheet of Constraint Manager.

1. Choose the *Cns Show*icon  .

   Constraints Manager appears.

2. Specify consistent values.
3. Choose *Route – Router Checks*.

   All warnings are removed.

4. Close the PCB Editor without saving the board file.

Summary

You learned to fix the most common warnings that occur when autorouting a design.

Exercise

Perform an autorouting of the board file. You will notice that the PCB Router generates fewer DRCs and takes far less time to route the design as compared to what it took before all warnings were fixed.

Lesson 4-8: Making Changes in a do File for Autorouting

Overview

In this lesson, you will learn to use do files for autorouting.

Concept

A do file is a text file that has the PCB Router commands. These commands are run sequentially. You can use do files to automate activities such as putting nets in classes and applying design rules. The use of do files simplifies routing work and increases productivity.

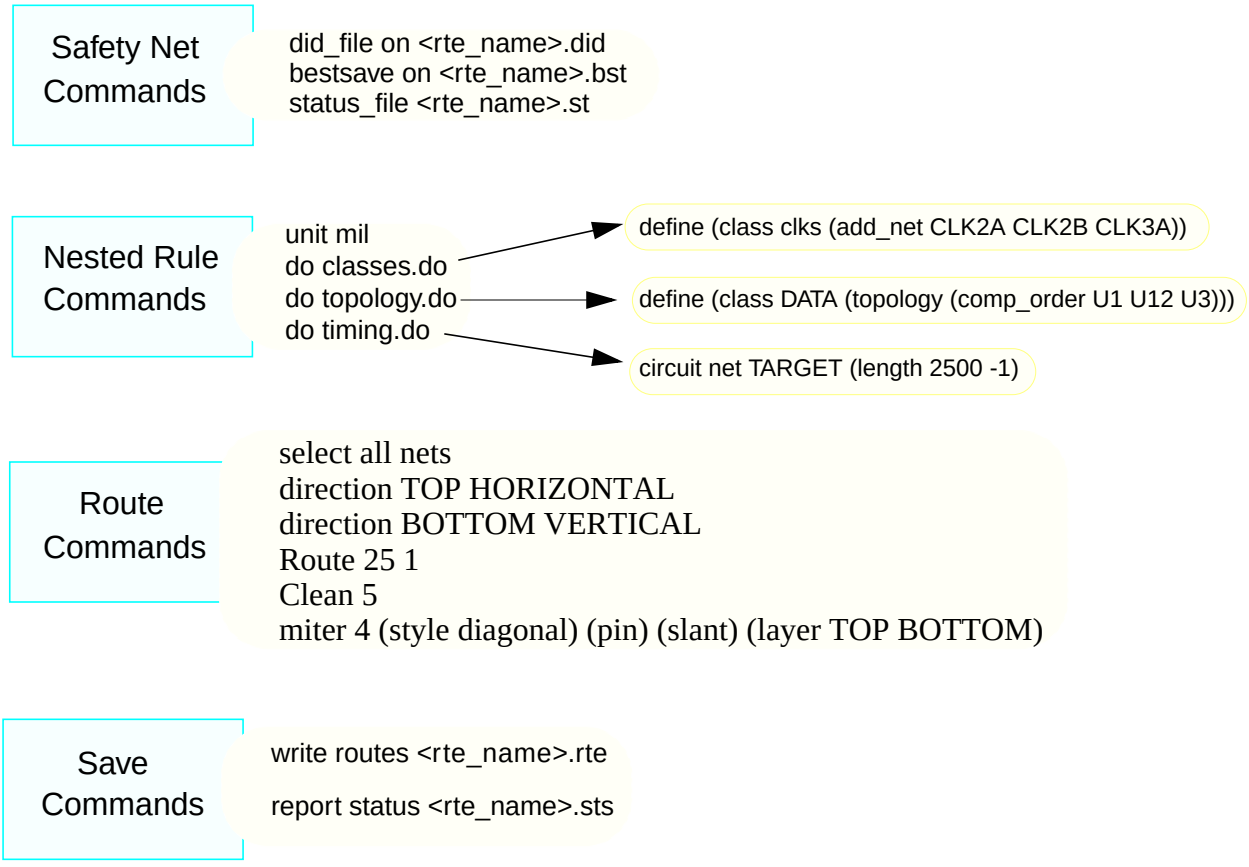
If you have one large do file, it is recommended you break it into several special purpose do files to accomplish different autorouting tasks such as:

- setting up the routing environment.
- setting up the design rules for a specific design.
- setting up fences and keepout areas.

You can then use and reuse these do files for similar designs that meet the same type of constraints. You can also call one or more of these files from a single master do file to accomplish a specific autorouting task.

The number of nested do file levels is unlimited. For example, your master do file may call a rules do file named `rules.do`, that in turn may call other do files such as `classes.do`, `topology.do`, and `timing.do` and so on.

Parts of a Basic Route do File



Note: For more information about do files, see the Cadence document *Allegro PCB Router User Guide*.

Using Do Files

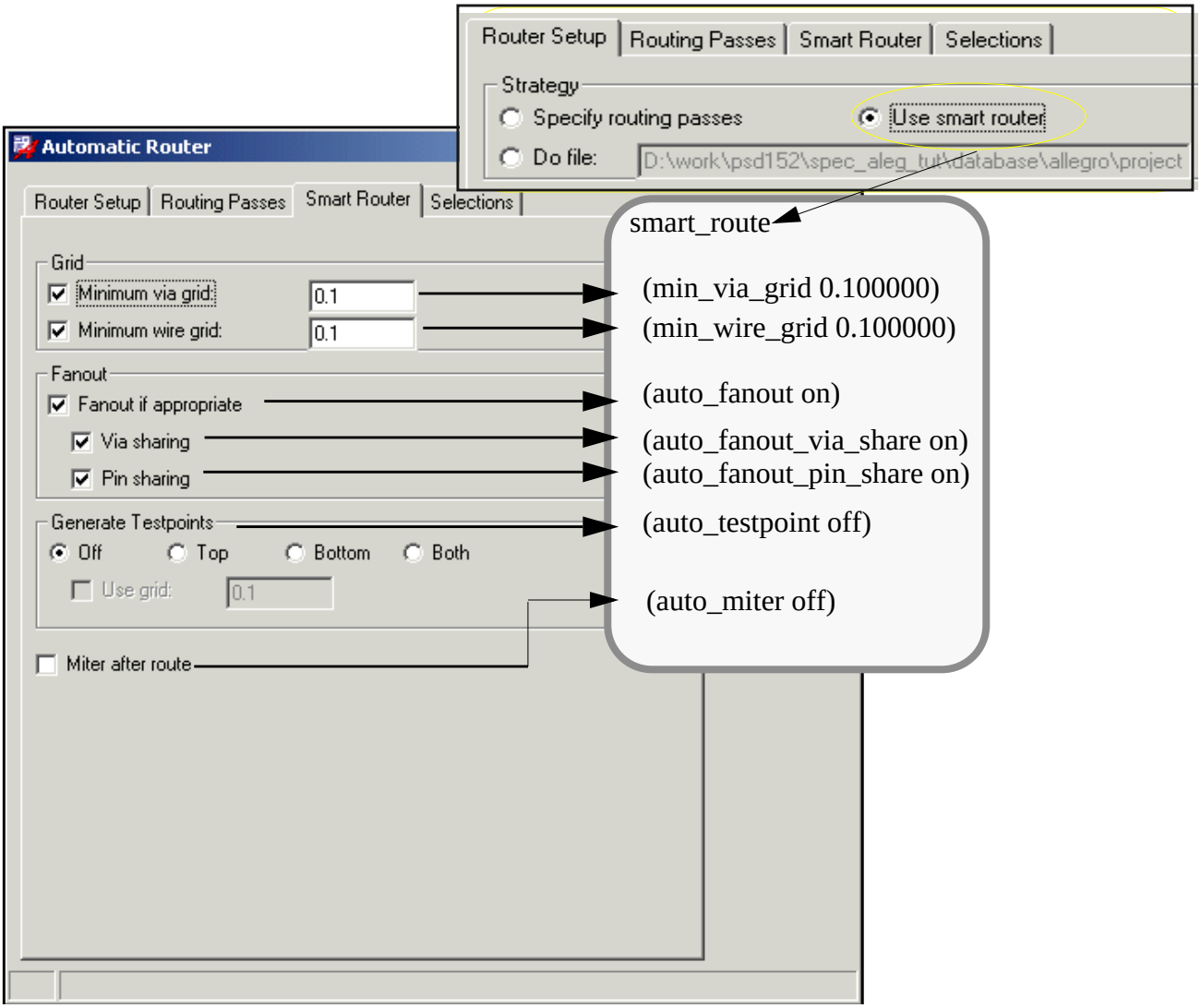
You can use a do file for autorouting from:

- PCB Editor—Use the *Do file mode* as routing strategy in Autorouter dialog box.
- PCB Router—Choose *File – Execute Do File* and then select the do file.

Note: In this tutorial, you will learn to use do files using the PCB Editor. For more information about using do files using the PCB Router, see the Cadence document *Allegro PCB Router Tutorial*.

Understanding the Content of a Do File

Each command in a `do` file corresponds to an action that you performed in the PCB Editor or the PCB Router. To understand the content of a `do` file, use the example exercise in Appendix 4, "Lesson 4-6: Using Smart Routing". In that exercise, you used the Automatic Router dialog box to perform smart routing. The following figure shows how the `smart_route.do` file command is created for your selections in the Automatic Router dialog box.

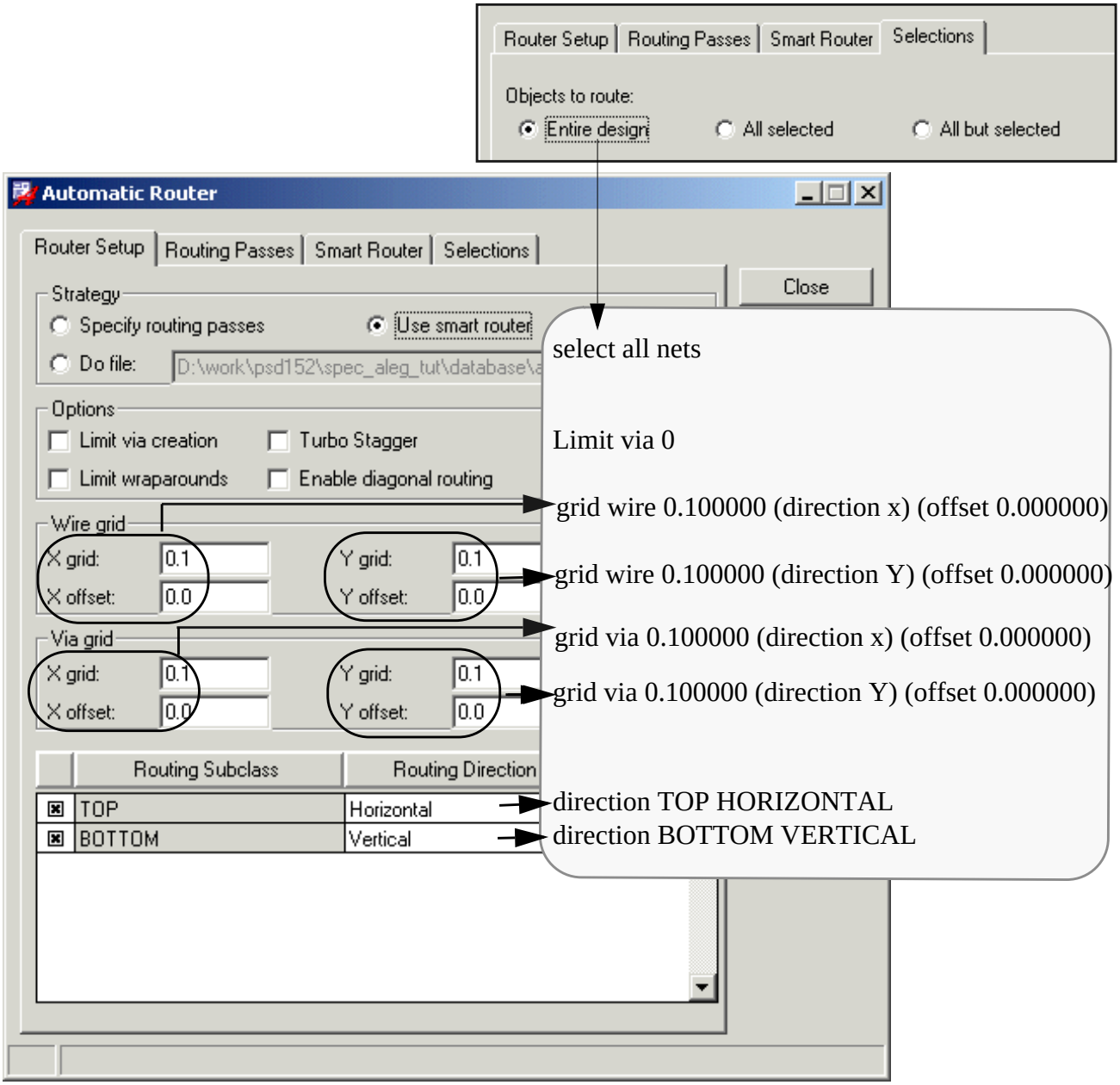


Besides the `smart_route` command, you need to define:

- Routing classes, direction and grid

- Nets that you want to route

The following figure shows the how do file commands are created based on your selections in the Automatic Router dialog box.



To specify a route file, which contains the design data generated by the PCB Router, use the following command.

```
write routes $/example_smart_route.rte
```

The route file includes information about wiring that has been routed in the PCB Router.

Finally, to specify that the PCB Router exit after running the last command in the do file, use the command:

```
quit -c
```

The `smart_route.do` file contains the following commands:

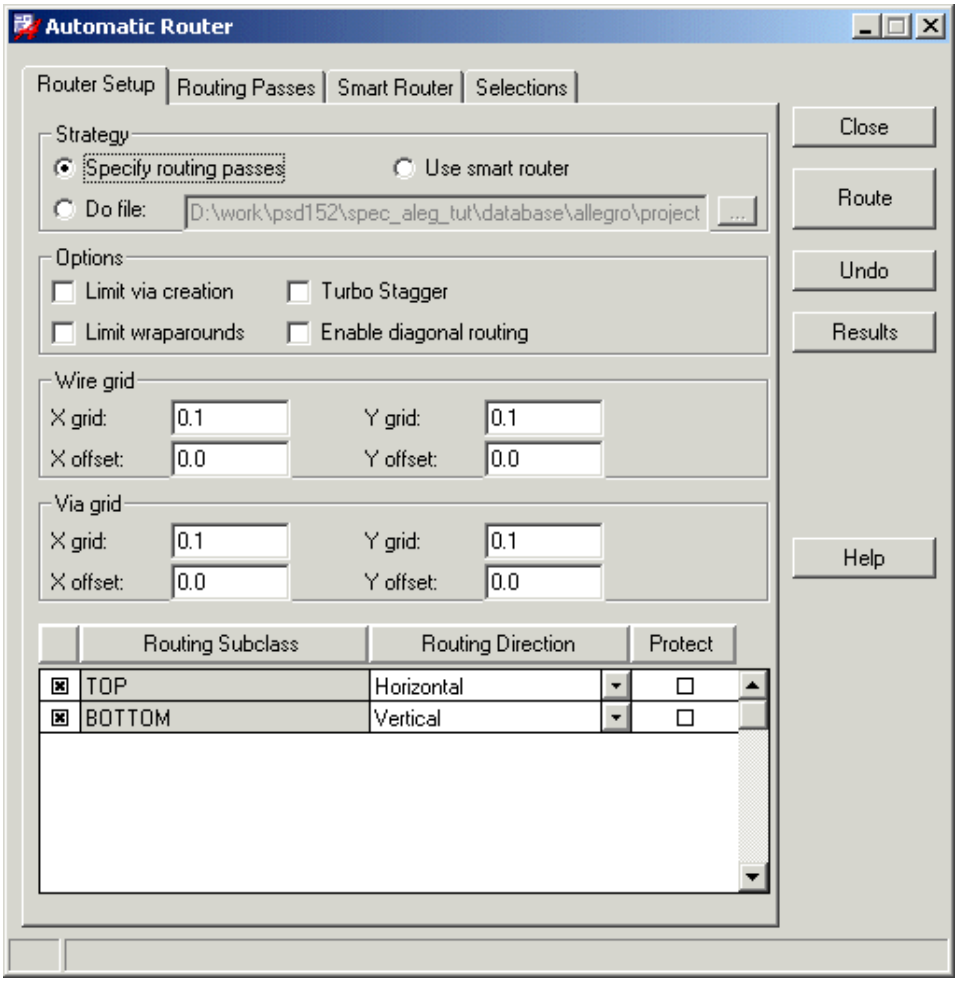
```
select all nets

grid wire 0.100000 (direction x) (offset 0.000000)
grid wire 0.100000 (direction Y) (offset 0.000000)
grid via 0.100000 (direction x) (offset 0.000000)
grid via 0.100000 (direction Y) (offset 0.000000)
Limit via 0
direction TOP HORIZONTAL
direction BOTTOM VERTICAL
smart_route
 (min_via_grid 0.100000)
 (min_wire_grid 0.100000)
 (auto_fanout on)
 (auto_fanout_via_share on)
 (auto_fanout_pin_share on)
 (auto_testpoint off)
 (auto_miter off)
write routes $/example_smart_route.rte
quit -c
```

Procedure

1. Open the `auto_routing_ready.brd` file in the PCB Editor.
2. Ensure that only the `Top` and `Bottom` layers are selected in the *Visibility* tab and all ratsnest are switched off.
3. Choose *Route – Route Automatic*.

The Automatic Router dialog box appears.



Ensure that the settings in the Router Setup tab reflect the above figure.

4. Click the *Do file* radio button in the *Strategy* box.
5. Click  and choose the *smart_route.do* file in the `physical` folder under the root design.
6. Click *Route*.

   The Automatic Router Progress window appears detailing the progress. You can click *Details* to view routing progress.

   When routing is completed, the Automatic Router Progress window disappears.
7. Click *Close* to close the Automatic Router dialog box.

8. Save the board file with the name `smart_routed.brd`.

Summary

In this lesson, you learned about the basic commands in a `do` file. You used a `do` file to route a design from the Automatic Router dialog box in the PCB Editor.

Lesson 4-9: Routing Individual Nets

Overview

In this lesson, you will learn to route individual nets using the *Route – Route By Pick* command.

Concept

The *Route – Route By Pick* command allows you to route specific nets and/or components in the design rather than the entire database. When you choose this command, the PCB Router is invoked in the background and a design (`.dsn`) file is created. Cross-probing is also allowed. You select components or nets or both in the Find filter, use the mouse pick, or choose the *Temp Group* option.

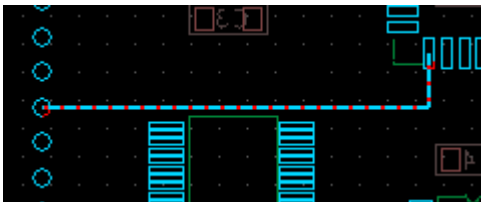
Procedure

1. Open the `auto_routing_ready.brd` file in the PCB Editor.
2. Using the *Visibility* tab, make visible only the `TOP` and `BOTTOM` layers.
3. Click the *Unrats All* icon  to switch off the display of ratsnests.

   The PCB Editor shows only components and board outline. No ratsnests are displayed.
4. Choose *Display – Show Rats – Nets.*
5. Display the ratsnest for the `wait` net. (For details, see `Controlling Ratsnest Display` on page 72.)

6. Choose *Route – Route Net(s) By Pick.*
7. Ensure that only *Nets* is selected in the *Options* tab.
8. Type `wait` in the *Find By Name* field as shown below and press `Enter`.

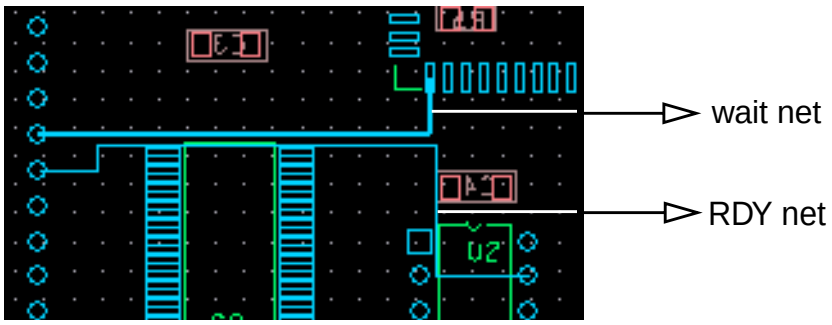
The Automatic Router Progress window appears detailing routing progress. A route for the `wait` net is created.



Compare the width of the route for the `wait` net with other nets, such as `A6`. The width is greater as the `wait` net is assigned a *NET_PHYSICAL_TYPE* rule with value `SYNC`. The rule specifies `MINIMUM_LINE_WIDTH=16` for all nets. (For information about defining design rules, see Lesson 2-2: Setting Design Rules on page 41.)

9. Type `RDY` in the *Find By Name* field as shown below and press `Enter`.

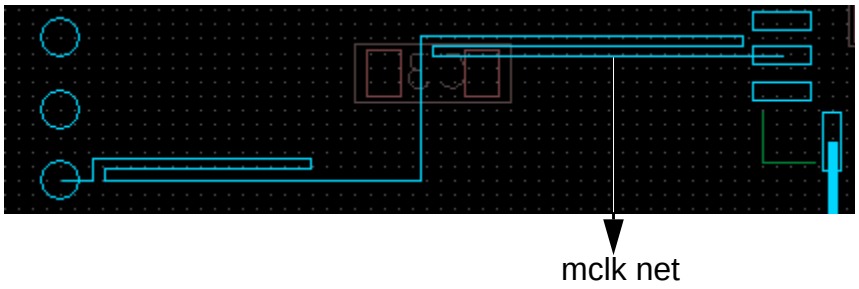
   The Automatic Router Progress window appears detailing routing progress. A route for `RDY` net is created. Notice that this net has a lesser width as it does not have a *NET_PHYSICAL_TYPE* rule defined.



10. Type `mclk` in the *Find By Name* field as shown below and press `Enter`.

The Automatic Router Progress window appears detailing the routing progress. However, after completion you will see no route is created for the `mclk` net.

A route for the `mclk` net is created. Notice that the autorouter uses trombone patterns to add length to the net.



The `mclk` net has the following property assigned to it:

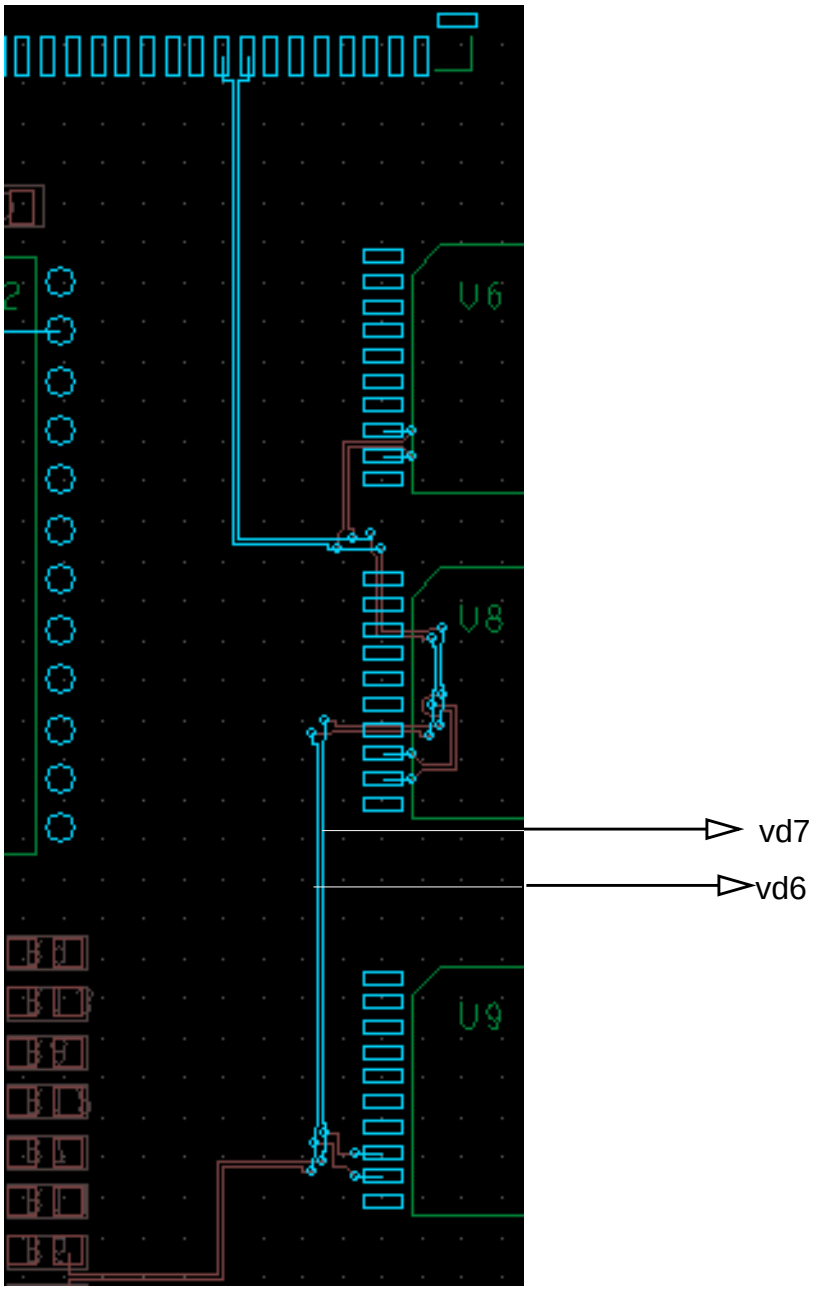
```
PROPAGATION_DELAY = L:S:2800 MIL:3500 MIL
```

This property requires a delay, which in turn calls for an increased length.

11. Type `VD7` in the *Find By Name* field as shown below and press Enter.

Notice that a route for two nets `VD6` and `VD7` is created. In Lesson 2-4: Setting Constraints on page 53, a differential pair was created for these nets and constraints were defined. The

Route – Route By Net command routes both these nets taking care of the constraints set for them.



You will now select the nets A0, A1, and A2 together and route them.

12. Click the *More* button in the *Find By Name* section of the *Find* tab.

The Find By name or Property dialog box appears.

13. Click A0, A1, and A2 in the *Available objects* field.

These nets appear in the *Selected objects* box.

14. Click *Ok* to accept the settings and close the dialog box.

The Automatic Router Progress window appears detailing routing progress. Routes for the A0, A1, and A2 nets are created.

These nets form a match group and have RELATIVE PROPAGATION DELAY property assigned. The autorouter adheres to the constraints defined for the selected nets while routing them.

You will now route all pin-net connections for a component.

15. Ensure that only *Comps* is selected in the *Options* tab.

16. Type U5 in the *Find By Name* field, set the search to *Comp* as shown below and press Enter.

The Automatic Router Progress window appears detailing routing progress. All pin-net for the U5 component are made.

You can also route component or nets by clicking them.

17. Click the U2 component to route it.

The U2 component is routed.

18. Right-click and choose *Done* in the pop-up menu.

19. Save the board file with the name pick_by_net_routed.brd.

Summary

You learned to route nets and components by using the *Route – Route By Pick* command.

Lesson 4-10: Mitering and Unmitering Connections

Overview

In this lesson, you will learn to miter and unmiter connections. Mitering and unmitering involve changing 90-degree wire corners to 45 degrees and vice versa.

Procedure

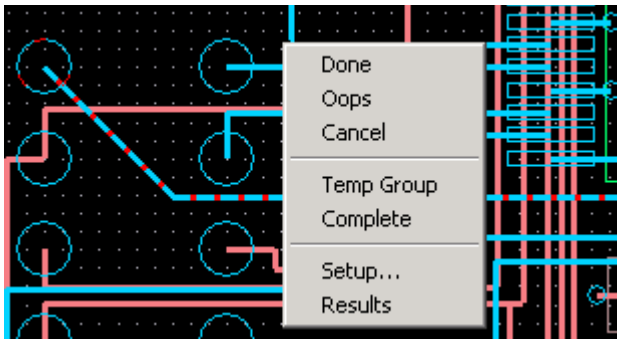
1. Open the `auto_routed.brd` file in the PCB Editor.
2. Zoom in around `D1`, `D2`, `D3`, and `D4` nets.

   Notice that the `D1`, `D2`, `D3`, and `D4` nets have 90-degree corners.
3. Choose *Route – Miter by Pick*.

   The Command window prompts:

   ```
   Enter selection point
   ```
4. Choose the `D4` net.

   The Automatic Router Progress window appears detailing routing progress. The net is routed and has a 45-degree corner.
5. Right-click and see the available command options.



Done—Saves any routing performed while the command was active and terminates the command.

Oops—Removes the result of the last route. The command is still active.

Cancel—Terminates the command without saving any routing.

Temp Group—Enables you to route groups of connections. For example, you can miter D1, D2, and D3 nets together.

Complete—Completes the selection of the items to group. First, you select *Temp Group*, then select individual elements, and finally *Complete* to signify the selection of a temporary group.

Setup—Opens the Miter Corners tab of Automatic Router Parameter dialog box.

Results—Displays the results of the current routing session.

You will now create a temporary group of D1, D2, and D3 nets and miter them.

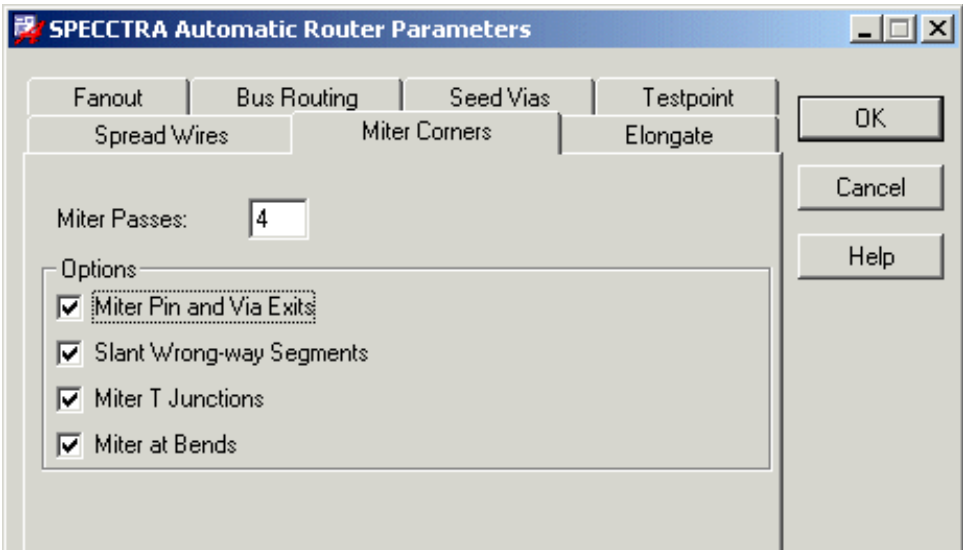
6. Click *Temp Group* in the pop-up menu, and select D1, D2, and D3 nets.
7. Right-click and choose *Complete* in the pop-up menu.

   The Automatic Router Progress window appears detailing routing progress. The D1, D2, and D3 nets are routed and have 45-degree corners.
8. Right-click and choose *Done* in the pop-up menu to save routing.
9. Choose *Route – UnMiter by Pick.*
10. Create a temporary group of D1, D2, D3, and D4 nets and unmiter them. (See steps 5 and 6)

    The D1, D2, D3, and D4 nets are routed and all 45-degree corners are converted to 90-degree corners.

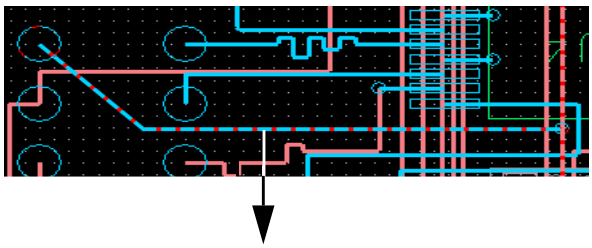
    You will now learn to display the setup options and see how changing them causes different routing results.
11. Choose *Route – Miter by Pick.*
12. Right-click and choose *Setup* in the pop-up menu.

The Automatic Router Parameter dialog box appears with the Miter Corners tab selected.

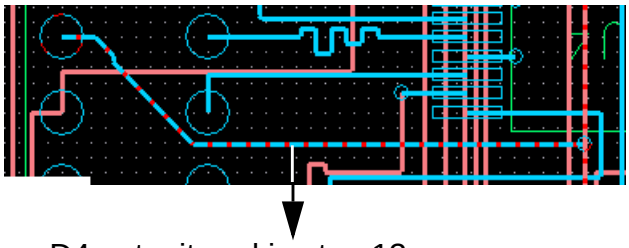


13. Remove the selection for *Miter Pins and Via Exits* check box.
14. Click *OK* to save the changes and close the dialog box.
15. Choose the `D4` net.

    The net is routed and has a 45-degree corner. Notice that the 45 degree-corner is in the middle of cline and not at a pin or via.



D4 net mitered in step 4
with the Miter Pins and Via Exits
option selected



D4 net mitered in step 13
with the Miter Pins and Via Exits
option not selected

16. Right-click and choose *Done* in the pop-up menu.
17. Close the `auto_routed.brd` file in the PCB Editor without saving it.

Summary

You learned to change 90-degree wire corners to 45 degrees and vice versa.

Lesson 4-11: Using Fanout By Pick

Overview

In this lesson, you will learn to fanout a component using the `Fanout_by_pick` command.

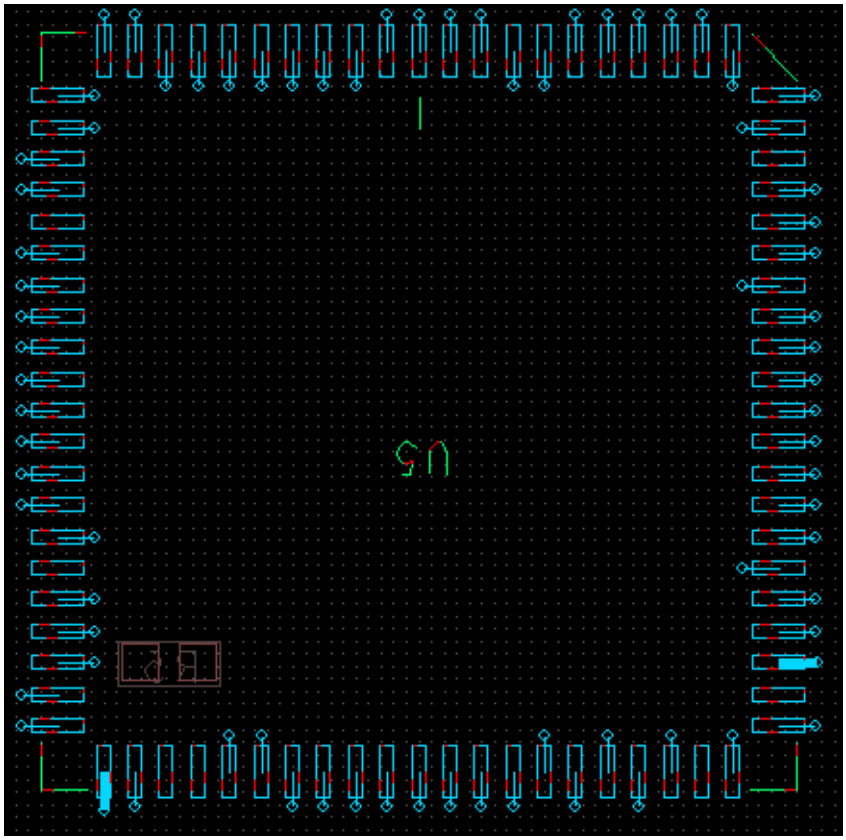
The `Fanout_by_pick` command routes short escape wires from SMD pads to vias.

Procedure

1. Open the `auto_routing_ready.brd` file in the PCB Editor.
2. Zoom in around the `U5` component.
3. Choose *Route – Fanout By Pick.*
4. Ensure that only *Comps* is selected in the Find Filter.
5. Choose the `U5` component.

   The Automatic Router Progress window appears detailing routing progress. The component has a fanout.

Notice that routes for short escape wires from SMD pads to vias are created.



6. Right-click and choose *Oops* in the pop-up menu.

   The fanouts are removed.

7. Right-click and choose *Setup* in the pop-up menu.

   The Automatic Router Parameter dialog box appears with the Fanout tab selected. You can use this tab to control pin and via sharing, set the layer depth, control the escape direction, and set a temporary grid.

   Direction—Specifies the fanout routing direction from the pins. Directs the autorouter to escape wires and vias inward from the component pins (*In*), outward from the component pins (*Out*), or either way (*Either*).

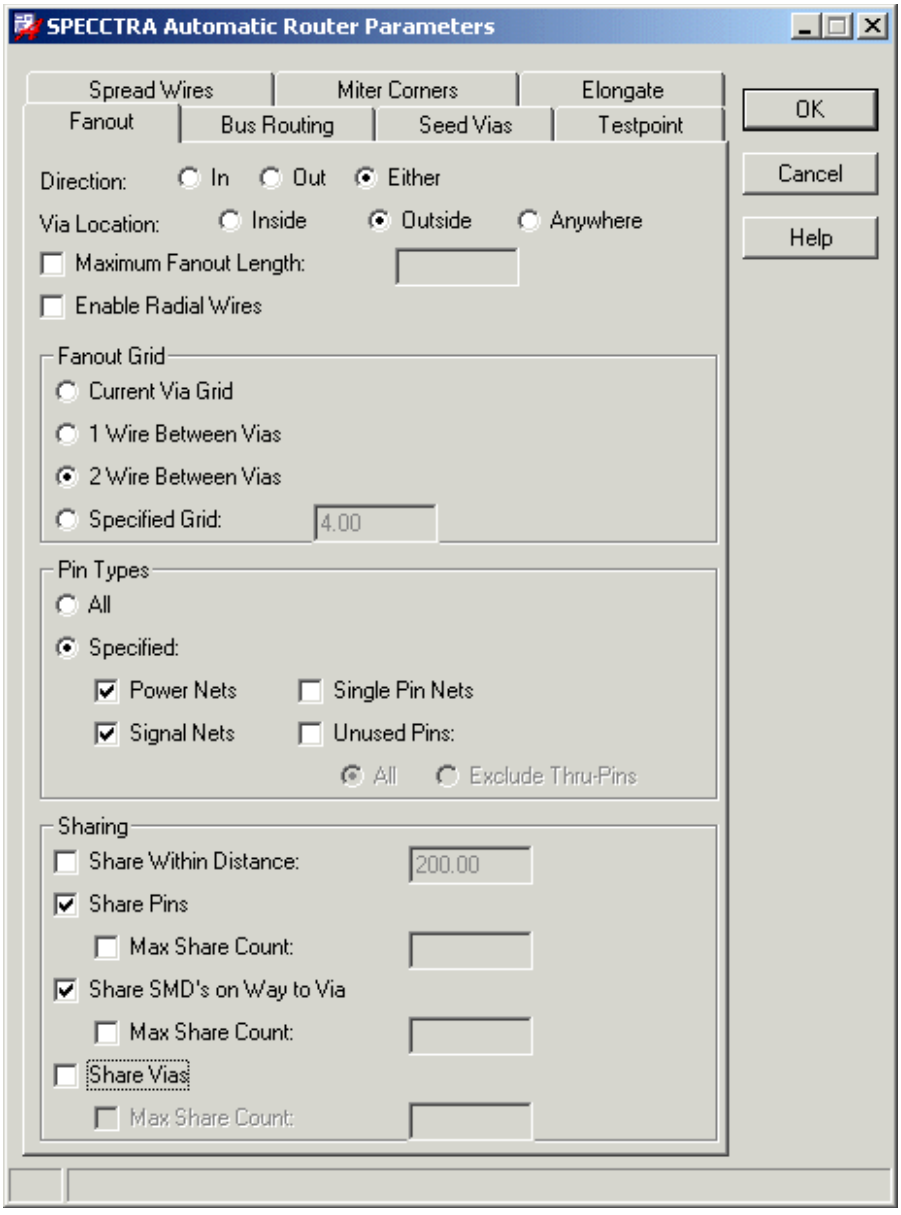
   Via Location—Directs fanout to escape wires and vias inside the component outline, outside the component outline, or relative to the component outline.

Fanout Grid—Allows the autorouter to automatically calculate initial via grids that permit one wire or two wires between adjacent vias.

Pin Types—Selects all or specific pins such as power nets, signal nets or single pin nets.

Sharing—Specifies whether you want to share thorough pins or SMD pins or vias.

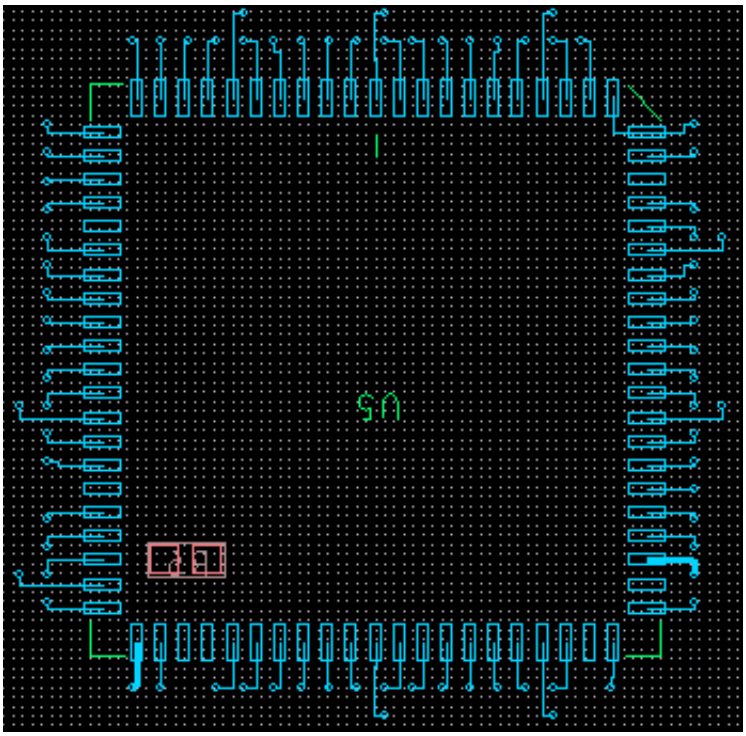
8. Set the parameters as shown below.



9. Click *OK* to save the changes and close the dialog box.

10. Choose the U5 component.

    Notice that the routes for the short escape wires from SMD pads to vias are created. All vias are located outside the component outline.



11. Close the `auto_routing_ready.brd` file in the PCB Editor without saving it.

Summary

You learned to fanout a component using the *Route – Fanout By Pick* command.

5

Module 5: Handling Post-Routing

This module consists of the following lessons:

Completion Time

- 2 hours for written lessons

Lesson 5-1: Understanding Routing Results

Overview

In this topic, you will learn to analyze the routing results by reading the routing progress report.

Concept

Automatic Router Results

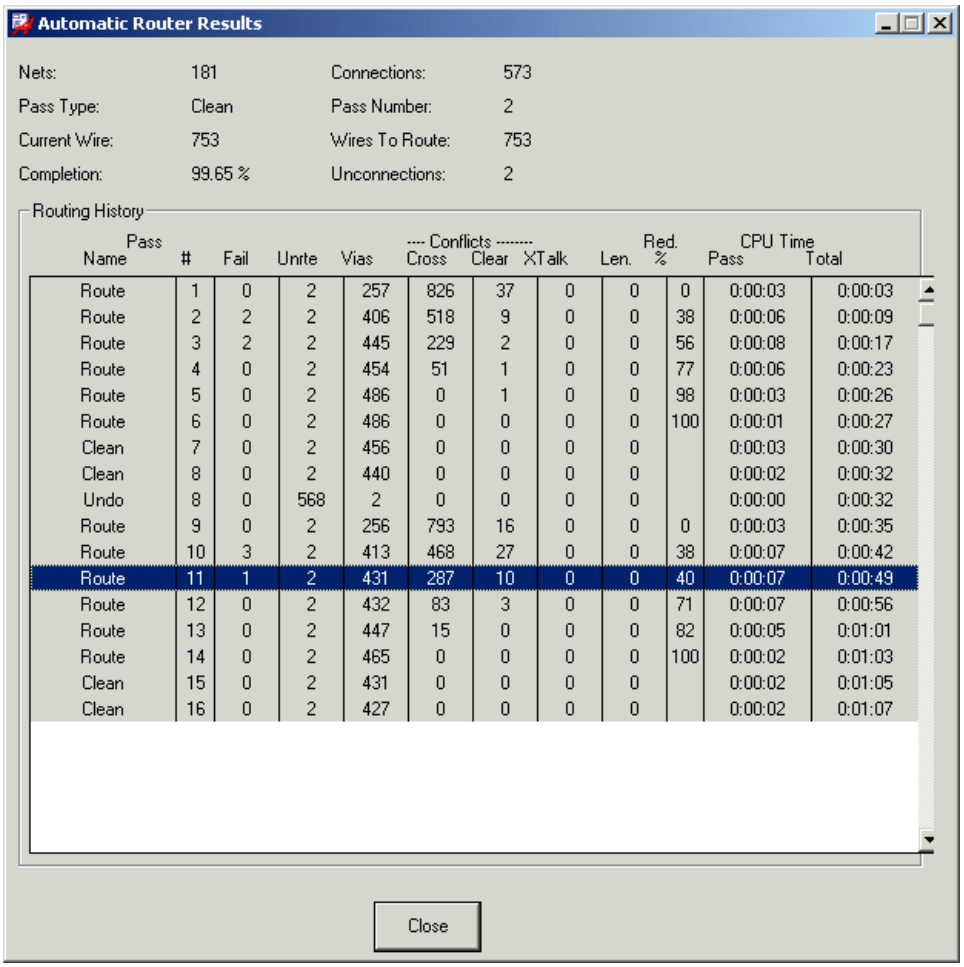
To identify the detailed routing status while auto routing a design, choose the *Results* button in the Automatic Router dialog box. This displays the Automatic Router Results dialog box, which shows the following information:

- **General information**—Information about the number of nets and connections in the design. This section also lists routing progress in terms of pass type, pass number, current wire, and completion percentage.
- **Routing history**—This section contains the route history for the current session. Careful reading of this section helps determine if the autorouter is making progress on routing to completion, and how you can use different influencing techniques when the autorouter is not converging.

  The first two columns of the route history list the pass number and pass type for each routing pass. The third column lists the number of failures during the routing pass. Failures are determined by the connections the router could not rip up and reroute with a new path during the routing pass.

  The next two columns list the unroute and via information. The remaining columns list information about the length rule

violation, reduction percentage, CPU time per pass, and the total CPU time.

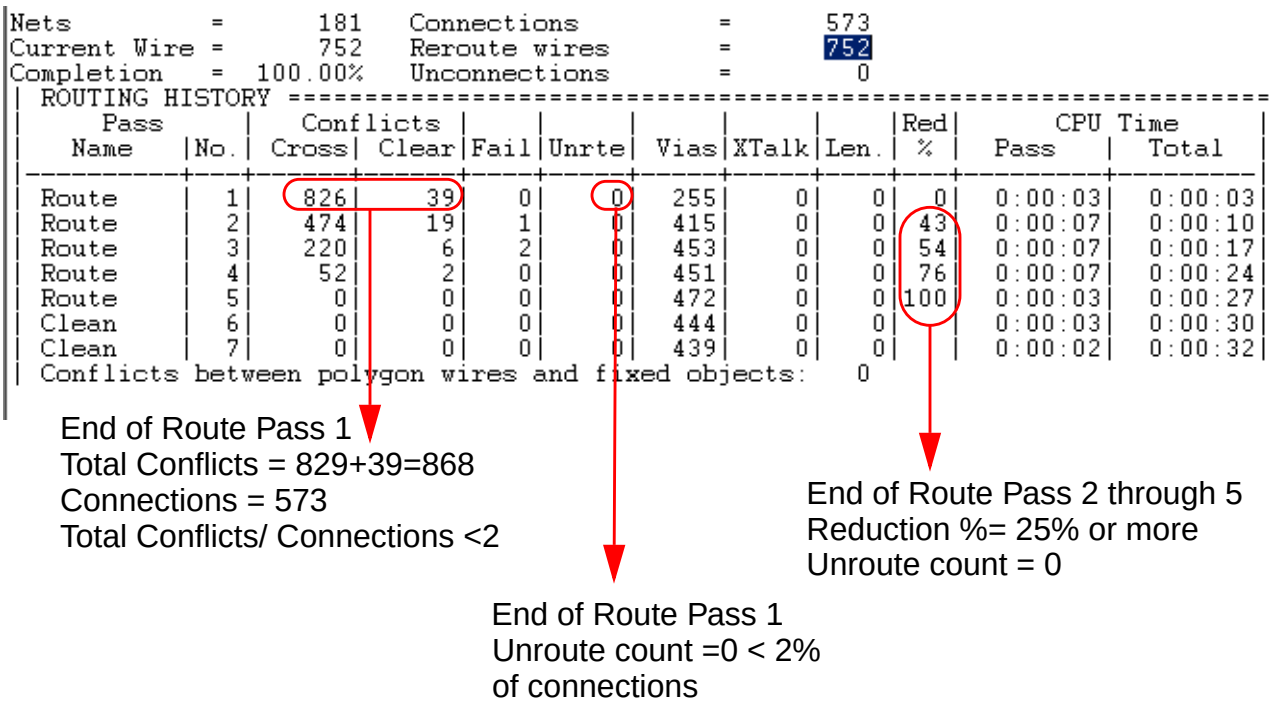


Pass Name	#	Fail	Unrte	Vias	Conflicts Cross	Conflicts Clear	Conflicts XTalk	Red. Len.	Red. %	CPU Time Pass	CPU Time Total
Route	1	0	2	257	826	37	0	0	0	0:00:03	0:00:03
Route	2	2	2	406	518	9	0	0	38	0:00:06	0:00:09
Route	3	2	2	445	229	2	0	0	56	0:00:08	0:00:17
Route	4	0	2	454	51	1	0	0	77	0:00:06	0:00:23
Route	5	0	2	486	0	1	0	0	98	0:00:03	0:00:26
Route	6	0	2	486	0	0	0	0	100	0:00:01	0:00:27
Clean	7	0	2	456	0	0	0	0		0:00:03	0:00:30
Clean	8	0	2	440	0	0	0	0		0:00:02	0:00:32
Undo	8	0	568	2	0	0	0	0		0:00:00	0:00:32
Route	9	0	2	256	793	16	0	0	0	0:00:03	0:00:35
Route	10	3	2	413	468	27	0	0	38	0:00:07	0:00:42
Route	11	1	2	431	287	10	0	0	40	0:00:07	0:00:49
Route	12	0	2	432	83	3	0	0	71	0:00:07	0:00:56
Route	13	0	2	447	15	0	0	0	82	0:00:05	0:01:01
Route	14	0	2	465	0	0	0	0	100	0:00:02	0:01:03
Clean	15	0	2	431	0	0	0	0		0:00:02	0:01:05
Clean	16	0	2	427	0	0	0	0		0:00:02	0:01:07

Analyzing Routing History

You can identify the final success of the autorouter by a quick analysis of the first five routing passes. After the first pass, the total number of conflicts should be less than 5 times the number of connections in the design. Add the number of crossing violations to the number of clearance violations after the first routing pass and divide this number by the number of connections in the design. If this number is much above 5, there is a very good chance that the

autorouter will not be able to reduce the number of conflicts to a reasonable amount.



```
Nets          =      181   Connections          =      573
Current Wire  =      752   Reroute wires        =      752
Completion    =  100.00%   Unconnections        =        0
| ROUTING HISTORY ================================================================
|     Pass      |   Conflicts |     |      |      |      |     |Red|       CPU Time      |
|   Name   |No.| Cross| Clear|Fail|Unrte| Vias|XTalk|Len. | % |  Pass    |  Total   |
|----------+---+------+------+----+-----+-----+-----+-----+---+----------+----------|
| Route    |  1|   826|    39|   0|    0|  255|    0|    0|  0|  0:00:03|  0:00:03|
| Route    |  2|   474|    19|   1|    0|  415|    0|    0| 43|  0:00:07|  0:00:10|
| Route    |  3|   220|     6|   2|    0|  453|    0|    0| 54|  0:00:07|  0:00:17|
| Route    |  4|    52|     2|   0|    0|  451|    0|    0| 76|  0:00:07|  0:00:24|
| Route    |  5|     0|     0|   0|    0|  472|    0|    0|100|  0:00:03|  0:00:27|
| Clean    |  6|     0|     0|   0|    0|  444|    0|    0|   |  0:00:03|  0:00:30|
| Clean    |  7|     0|     0|   0|    0|  439|    0|    0|   |  0:00:02|  0:00:32|
| Conflicts between polygon wires and fixed objects:   0
```

End of Route Pass 1
Total Conflicts = 829+39=868
Connections = 573
Total Conflicts/ Connections <2

End of Route Pass 2 through 5
Reduction %= 25% or more
Unroute count = 0

End of Route Pass 1
Unroute count =0 < 2%
of connections

The number of unroutes at the end of the first route pass should be less than two percent of the number of connections. Divide the number of unroutes after the first route pass by the total number of connections. If this number is greater than .02, then the autorouter will probably not be able to reduce the number of unroutes to a reasonable amount. The autorouter first tries to make every connection in the design, giving little regard to creating crossing and clearance violations. The autorouter then tries to resolve the clearance and crossing violations to converge on a solution. If unroutes remain after the fifth router pass, it is unlikely that the autorouter will ever make these connections.

During route passes two through five, you should see reduction ratios of at least 20 or 25 percent. If the reduction ratios are less than this, there is a good chance that the PCB Router will not be able to converge on a reasonable solution.

Convergence Success Criteria

After the fifth pass, the autorouter begins its convergence phase and is continually trying to reduce the number of crossing and clearance violations. It is common for the autorouter to actually increase the number of crossing and clearance violations over a single pass. In the convergence phase, you want to make sure that there is a downward trend in the number of clearance and crossing violations over any ten route passes. If there is no downward trend in the number of clearance and crossing violations over ten or more routing passes, then the router is stalled. At this point, you should stop the autorouter, change the influences on it, and restart the autorouter.

Other Useful reports

You can use the following reports to evaluate the current routing status:

- **Summary Drawing Report**—This report provides an executive summary of the drawing, connection and layout statistics.
- **Unconnected Pins Report**—This report helps you to locate missing connections by providing the x, y coordinate information of all pins requiring connection.

Note: For more information about generating the above reports, see Lesson 5-4: Creating Reports on page 171.

Summary

You learned to analyze the routing results by reading the routing progress report. This report can provide information about whether or not you are approaching optimum results. Based on this report, you can change routing parameters to achieve optimum results.

Lesson 5-2: Using Post Routing Commands

Overview

In this lesson, you will learn to perform basic post routing commands from the Automatic Router dialog box.

Concept

The function of basic post-routing commands are:

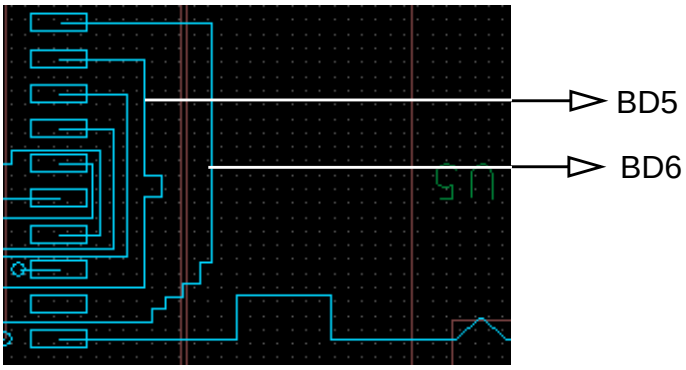
Command	Description
Slide	Moves or edits connect lines or vias interactively while maintaining their connectivity. When you use this command, you choose the element to move, then its destination.
Gloss	Starts the glossing process, which can be used to: ■ Clean up lines and vias ■ Eliminate vias ■ Smooth lines ■ Center lines between pads ■ Improve line entry into pads ■ Widen connect lines ■ Convert corners to arcs ■ Generate dielectric patches ■ Fillet pad and T connection You can attach either the `NO_GLOSS` property or the `FIXED` property to the nets so that gloss does not modify the routing of these nets.
Custom Smooth	Optimizes selected clines or cline segments according to the parameters set in the Options tab. Smoothing the angles of clines or cline segments can minimize the distance to pad connections. Use this command as you manually edit etch. This feature does not operate on clines with DRC errors, so you may need to update DRCs and clean up your design before using this command.

Command	Description
Clean	Rips up and reroutes all connections to improve routing and manufacturability. This command removes unnecessary vias and bend points and improves SMD entries and exits. All connections are ripped up and rerouted with higher costs for via use, off-center SMD pad entry, and SMD pad side exit. Four clean passes are suggested after completing all routing passes.
Critic	Helps improve manufacturability without performing a rip-up and reroute operation. This command eliminates notches and removes extra bends from existing etches. The `critic` command is similar to the `clean` command but different in one important respect. Where `clean` completely reroutes each wire and can drastically change a connection's wiring, `critic` attempts to make local adjustments to the existing wires without rip-up and rerouting. The critic operation executes much faster than clean.
Miter Corners	Changes 90-degree corners to 45-degree diagonals.

Procedure

Running the Critic Command

1. Open the `post_route_practice.brd` file in the PCB Editor.
2. Use the *Zoom In* icon  and pan your design to set the focus on the BD6 and BD5 nets as shown below:



Notice that the BD5 net has a notch point or bend and the BD6 net has a staircase-like structure. The `critic` command eliminates these notches or extra bends.

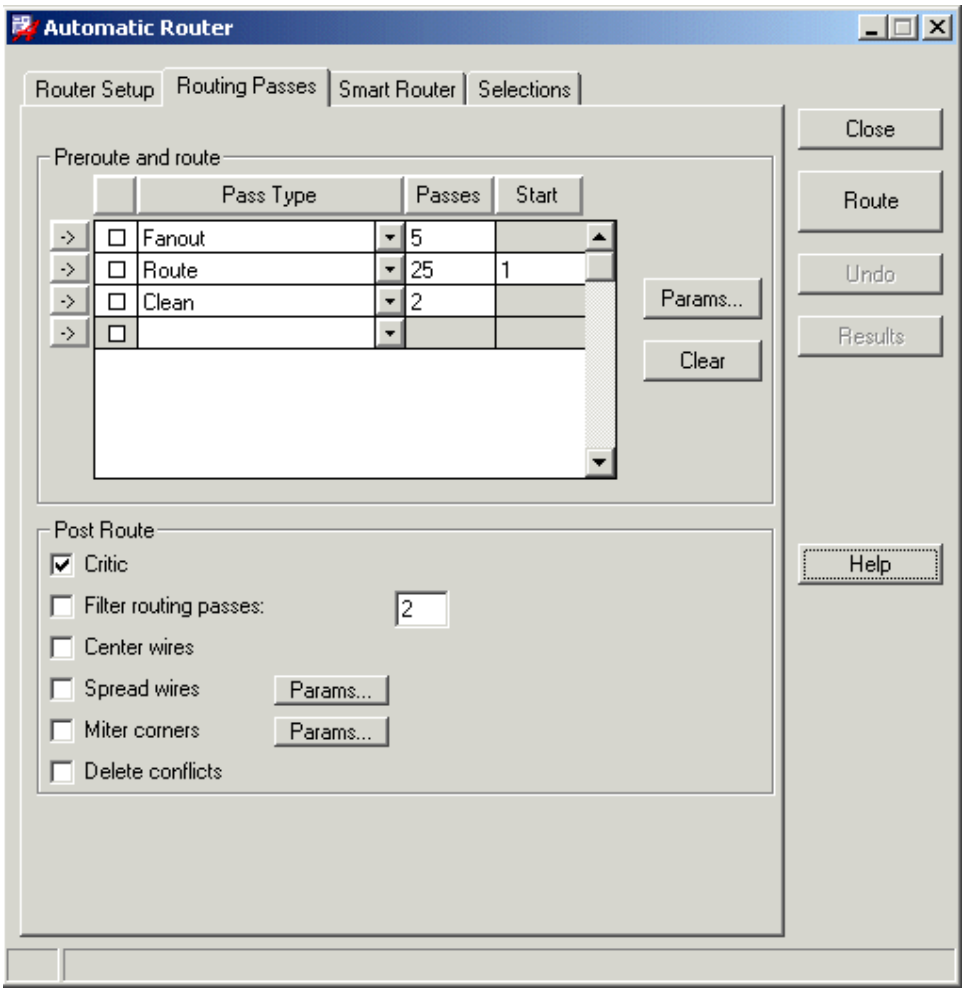
3. Choose *Route – Route Automatic*.

   The Automatic Router dialog box appears.

4. Ensure that the selected routing strategy is *Specify routing passes*.

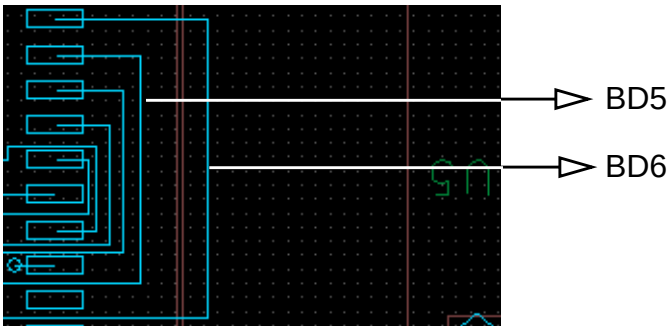
5. Click the *Routing Passes* tab.

6. Clear all check boxes in the *Preroute and route* section and select the *Critic* check box in the *Post Route* section.



7. Click *Route*.

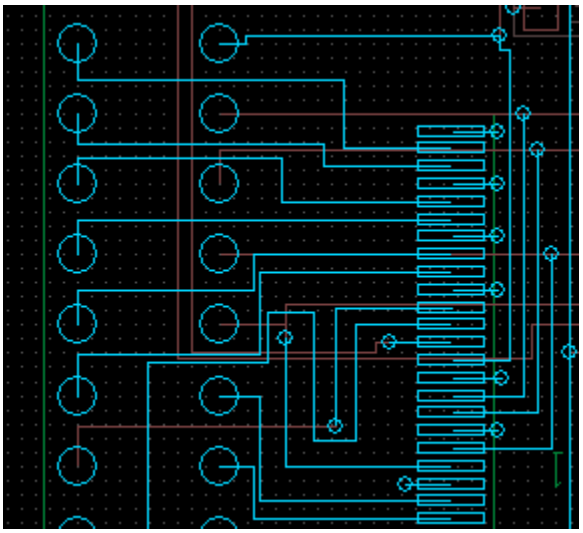
The Automatic Router Progress window appears detailing the routing progress. Notice that the BD5 and BD6 nets have a cleaner route with straight-edges. The notches and bends are removed.



8. Click *Close*.

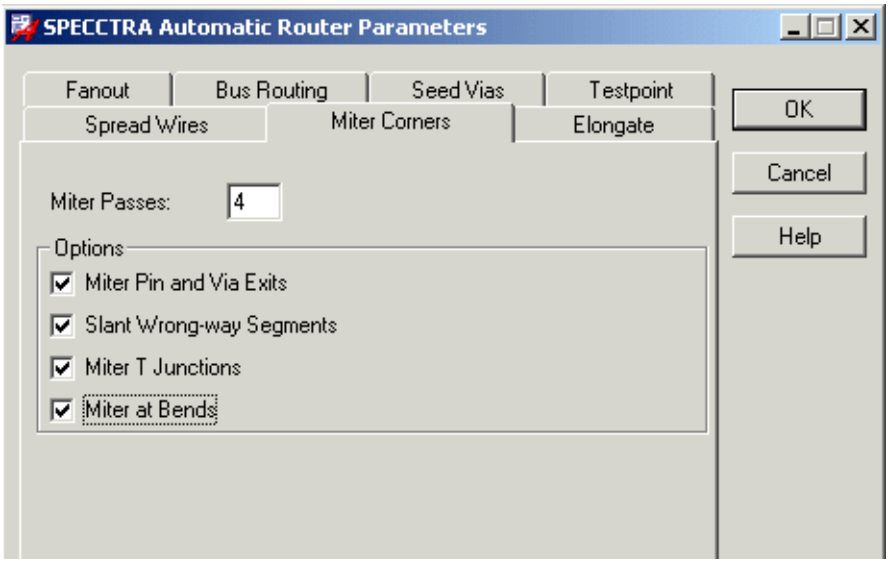
Mitering Corners

1. Zoom in around the nets between the J1 and U1 components.



2. Open the Automatic Router dialog box and ensure that only the *Miter corners* check box is selected in the *Post Route* section. (Hint: See last exercise for details)
3. Click the *Params* button to the right of the *Miter corners* check box.

The Automatic Router Parameters dialog box appears with the *Miter Corners* tab selected.



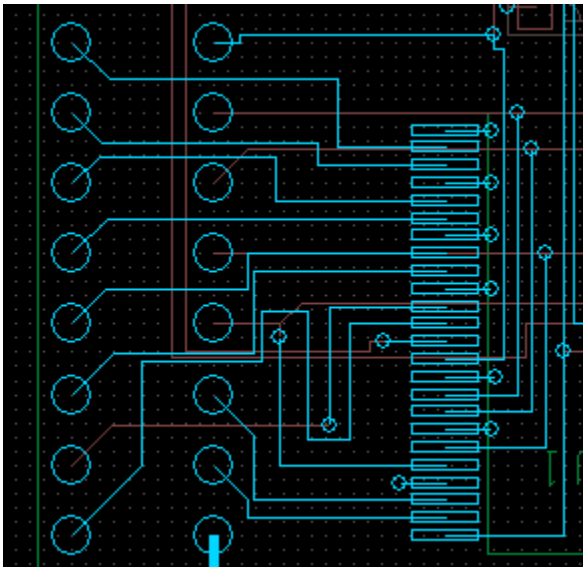
4. Ensure that only the *Miter Pins and Via Exits* check box is selected while the other options are cleared like shown below.

The above selection sets the PCB Router to change 90-degree wire corners to 45 degrees for wires exiting pins and vias.

5. Click *OK* to accept the changed settings.

6. Click *Route.*

7. The Automatic Router Progress window appears detailing the routing progress.



Notice that the 90-degree wire corners are changed to 45 degrees for wires exiting pins and vias.

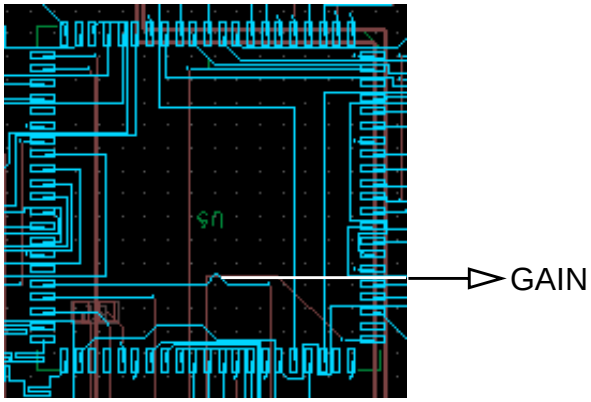
8. Click *Close* to close the Automatic Router dialog box.

Using Slide

You learned to slide connections and vias in the section Sliding Connections and Vias on page 86. In this exercise, you will slide connections using the `Cut` feature.

1. Choose *Route – Slide*.
2. Set the *Find* tab so that only the *Cline Segs* check box is selected.
3. In the *Options* tab, set the value of *Corners* to 90.

4. Zoom in around the U5 component.

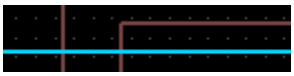


Notice that the GAIN net has a triangular bend.

5. Click the end of the triangular bend and slide it towards the main etch and click when the bend merges with the main etch.

Click the edge.

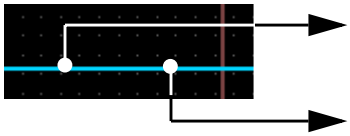
Set the corner selection to 90 and slide down.



Click when the corner disappears.

6. Right-click and choose *Cut* from the pop-up menu.

7. To define a section, choose two points, within a single segment as shown below.



First, click here.

Next, click here and slide.

Click here to complete the segment.

As soon as you make the second click, the section becomes moveable.

8. Complete the segment as shown above.

9. Right-click and choose *Done* from the pop-up menu.

You used the `slide` command to remove segments from etches or add segments to etches.

Using Custom Smooth

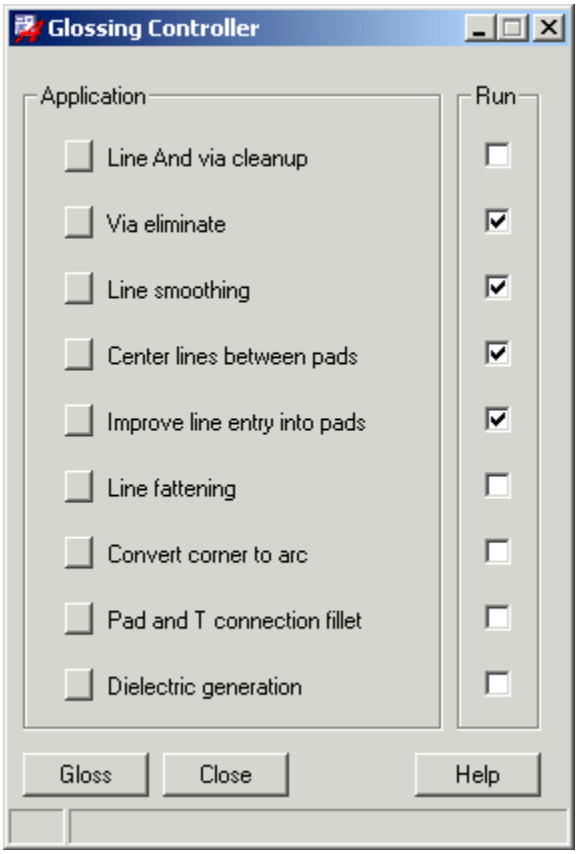
1. Choose *Route – Custom Smooth.*
2. Click the `GAIN` net.

   The section created in the last exercise is removed and the `GAIN` net attains a straight connection line.
3. Right-click and choose *Done* from the pop-up menu.

Glossing a Design

1. Choose *Route – Gloss – Parameters.*

   The Glossing Controller dialog box appears.



You can select any available applications, such as line and via cleanup and via elimination.

To set the parameters for an application, click the rectangle to the left of the application name.

2. Click *Gloss*.

   The Glossing routine is run. You can see the traces being moved, and corners being changed from orthogonal to diagonal.

3. To view the gloss log file, choose *File – File Viewer*.

   The Select File to View dialog box appears.

4. Double-click `gloss`.

   The `gloss.log` file appears listing the results of last gloss operation.

5. Close the `gloss.log` file.

   You will now set the line and via cleanup glossing application.

   Note: This is the only glossing application whose parameter settings are used by the autorouter when it runs the Cleanup Router. Therefore, you should establish these parameters before you run the autorouter.

   The autorouter looks at this dialog box when it is organizing to route, and any parameters it does not find here, it takes from the Automatic Router dialog box.

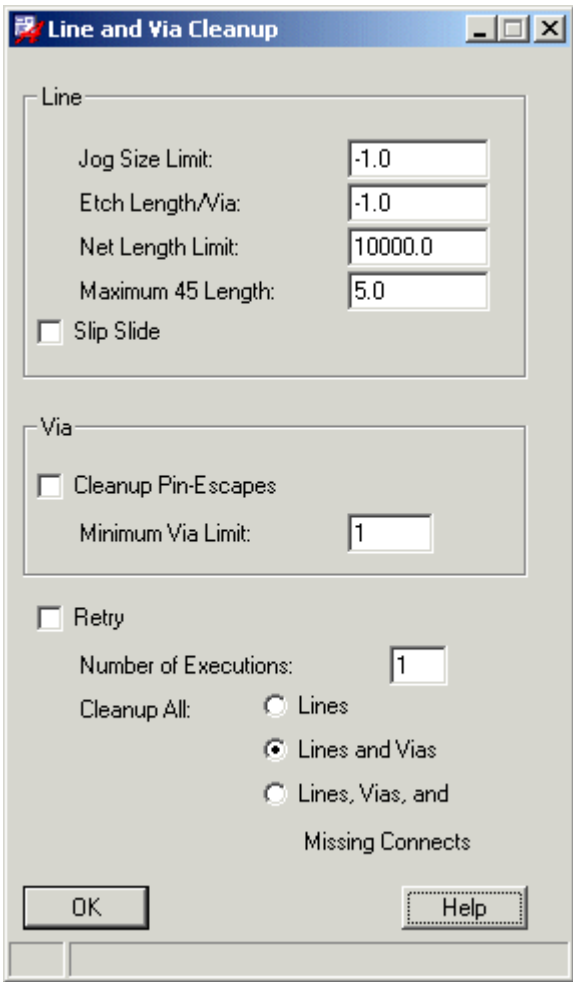
6. Choose *Route – Gloss – Parameters.*

7. Select the *Run* check box for the *Line and via cleanup* application.

   The above selection processes one net at a time, ripping up every connect line and via and rerouting it using a high via cost. If the rerouted path is an improvement, the new path replaces the existing one.

8. Click the application button to the left of *Line and via cleanup* application.

The Line and Via Cleanup dialog box appears.



You can make changes in this dialog box. The `-1` limit in the *Jog Size Limit* and *Etch Length/Via* fields indicate that these fields are not used.

9. Select the *Cleanup Pin-Escapes* check box to specify that the pin escape lines and vias connected to the SMD pins should be ripped up and rerouted as required.
10. Click *OK* to accept the settings.
11. Click *Gloss*.

    Notice that the PCB Router processes one net at a time, ripping up every connect line and via and reroutes it. The only nets untouched are the ones that have the `FIXED` or `NO_GLOSS` property assigned.

Summary

You learned to run post-routing commands such as `critic`, `miter`, `slide` and `gloss`. Post-routing commands refine the wiring after routing is complete.

Exercise

Click the application button to the left of all glossing applications in the Glossing Controller dialog box and view the available parameters.

Lesson 5-3: Correcting DRC Violations

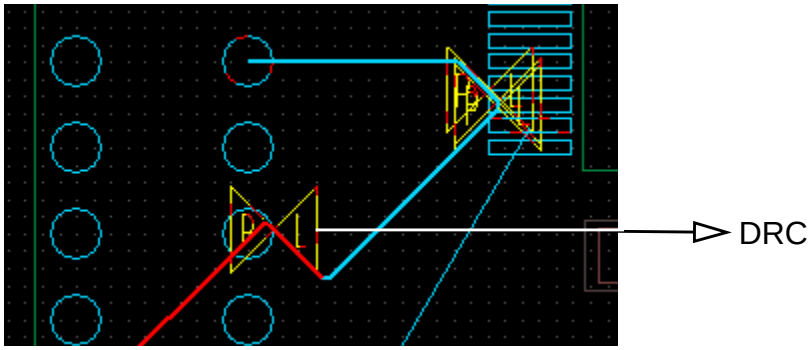
Overview

In this lesson, you will learn to correct DRC violations.

The PCB Editor performs to ensure that the design conforms to the specified properties and constraints you attach to individual design elements or assign globally to the entire design. DRC identifies violations of physical design rules whenever you add an element or make any change to the design.

You can check for violations in real-time as you design (called online DRC), or in batch mode (called batch DRC). You may prefer the instant feedback of an online DRC, at the expense of system performance, or you may prefer to use batch mode to improve system performance and decide to resolve violations later in the design process.

When the PCB Editor detects a design rule violation, the offending design element is flagged with an appropriate DRC marker (bow tie) as shown below.



Displaying Information About DRC Violations

DRC markers store the following information about a DRC:

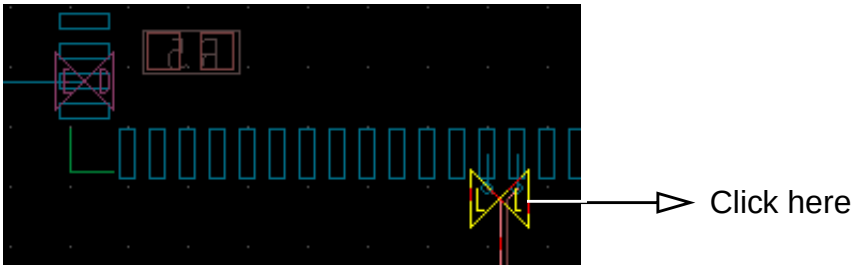
- DRC class, subclass, and location
- Type of constraint set (spacing, physical, or electrical)
- Name of the constraint set
- Constraint type being violated (for example, Line to Thru Pin Spacing)
- Data concerning the first element in the violation (type of element, location, Refdes, if a package, and so on)
- Data concerning any second element in the violation (type of element, location, Refdes, if a package, and so on)

Procedure

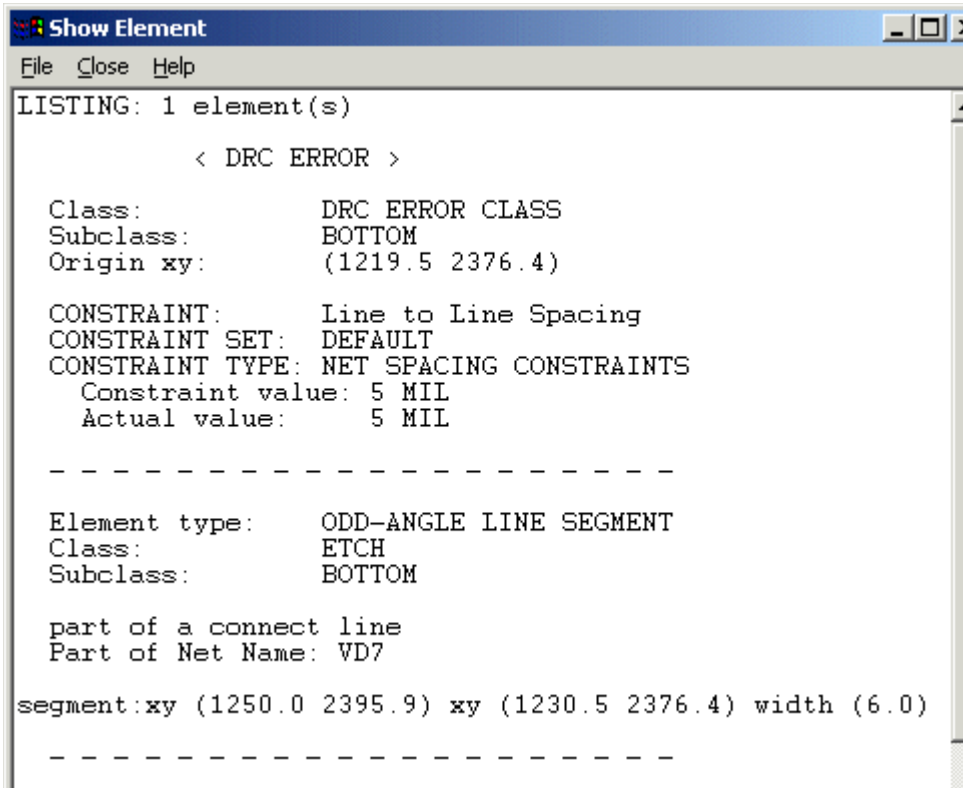
Displaying Details About a DRC

1. Open the `drc.brd` file in the PCB Editor.
2. Choose *Display – Element*.
3. Click the *All Off* button in the *Design Object Find Filter* section of the *Find* tab, and then choose *DRC errors*.

4. Zoom in around the U5 component, and click the DRC marker as shown below:



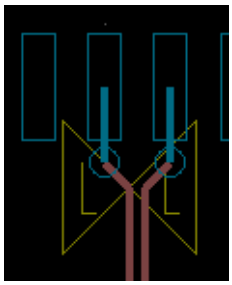
The Show Elements window appears detailing information about the DRC. Notice that the error is caused on the BOTTOM subclass and the reason of the error is related to the value of line to line spacing. Notice that the actual value is exceeding the constraint value.



5. Right-click and choose *Done* from the pop-up menu.

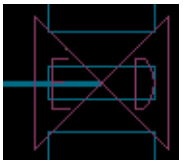
Understanding DRC Marker Code Characteristics

1. Zoom in to see the graphical details of the DRC marker you checked in the last exercise.
2. Notice that the DRC marker has two characters (L), one in each side of the "bow-tie," that identify the type of constraint violation being marked.



The letter “L” refers to line related violations. This includes clines, c-arcs, lines, arcs, and text on etch layers. The PCB Editor treats the text on etch layers as lines for DRC purposes.

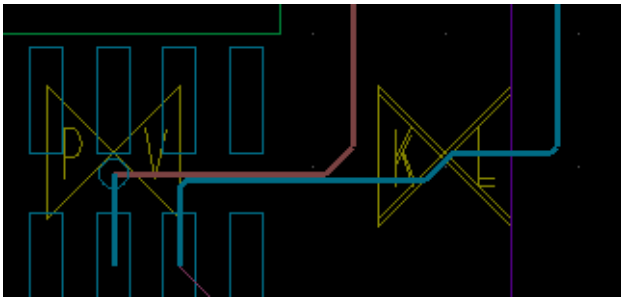
3. Zoom in to see the graphical details of the DRC marker attached to the `mclk` net.



The DRC marker lists two letters, E and D.

The letter E refers to electrical constraint related violations. If you check the properties attached to this net, you find a `PROPAGATION_DELAY` property attached. The constraints specified by this property are not being met, therefore a DRC is generated.

4. Zoom in to see the graphical details of the DRC markers attached to the U11 component.



Notice that there are multiple DRC markers and these have different letters.

The letter P refers to pin related violations, except when preceded by the letter D for phase tolerance violations or letter E for parallelism violations.

The letter V refers to via-related violations.

The letter K refers to keepin/keepout-related violations.

Fixing DRC Violations

This procedure is for demonstration only. You may get a variety of DRC violations and have different design situations causing them. To fix DRC violations, you may need to understand the properties and constraints assigned to the erroneous etch and study it in the context of its route.

1. Using the procedure in Exercise 5.3.1, show the element details for the DRC check with the K/L letter mark for the RA13 net.

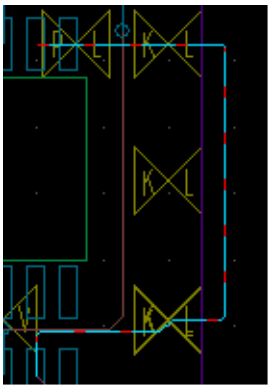
   The Show Element window appears with a Line to route keepin spacing violation. A quick look at the RA13 net shows it is etching past the route keepin area.

2. Delete the etch for the RA13 net.

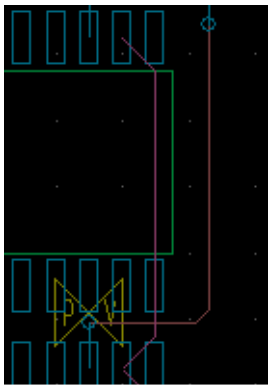
   Notice that few DRCs are removed.

3. Using *Route – Route Net(s) By Pick* command, create an etch for the RA13 net.

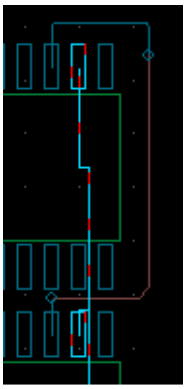
The etch is recreated and DRCs are removed as shown below.



Step 2



Step 3



Step 4

4. Right-click and choose *Done* from the pop-up menu.
5. Zoom in around the U5 component, and show the element details for the DRC marker with the L/L text.

   The Show Elements window displays that the marker has a Line to Line spacing violation. This violation is caused by net spacing constraints.
6. Right-click and choose *Done* from the pop-up menu.
7. Click  to open Constraint Manager.
8. In the Routing workbook, click *Differential Pair*.

   The Routing workbook lists the constraint information for the DP1 differential pair, which includes the nets VD6 and VD7.

   Notice that the minimum line spacing value is 6 mil. The minimum line spacing value in the board is 5 mil.
9. Change the *Min Line Spacing* value to 5 mil.
10. Close Constraint Manager to return to the PCB Editor.
11. Using the *Route – Route Net(s) By Pick* command, create an etch for the vd6 net.

    A route is created for both Vd6 and Vd7 nets. All DRCs on these two nets are resolved.
12. Right-click and choose *Done* from the pop-up menu.

13. Zoom in around the U5 component, and show the element details for the DRC marker attached to the mclk net.

    You get the following details:

```
CONSTRAINT SET:  PROPAGATION_DELAY
  CONSTRAINT TYPE: ATTRIBUTE
    Constraint value: L:S:2800 MIL:3500 MIL
    Actual value:     1197.1 MIL
```

14. Right-click and choose *Done* from the pop-up menu.

15. Delete the mclk net.

16. Click the *Add Connect* icon  .

17. Click the pin of the mclk net in the J1 connector, the pin connected to one end of the ratsnest. (HINT: This is J1:51 pin.)

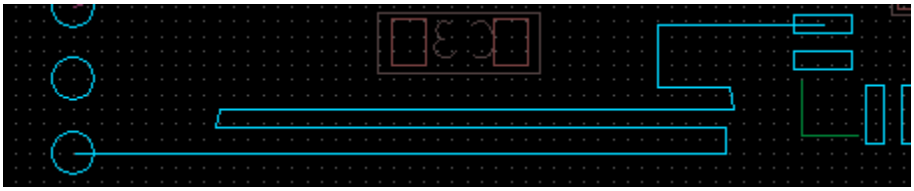
18. Start adding an etch towards the U5.31 pin.

    Notice that an online delay constraint report appears in the *Options* tab warning you that the net has a timing delay and you need certain etch length to accommodate this delay.

    As you create the etch, the delay value adjusts itself. You can use this information to add the desired etch length. When the delay is still negative, the data appears in red.

    If the etch length satisfies the required delay, the value appears in green.

19. Complete the etch for the mclk net as shown below.



    You have fixed the DRC violations in the board.

20. Close the PCB Editor without saving the drc.brd file. (This file will be used in next exercise.)

Summary

The PCB Editor performs comprehensive DRC violation checking. You can use the available DRC checking features to fix DRCs. You can also generate a comprehensive DRC violation report. You will learn generating this report in Lesson 5-4: Creating Reports on page 171.

Lesson 5-4: Creating Reports

Overview

In this lesson, you will learn to create different reports that you can use to analyze routing results.

Concept

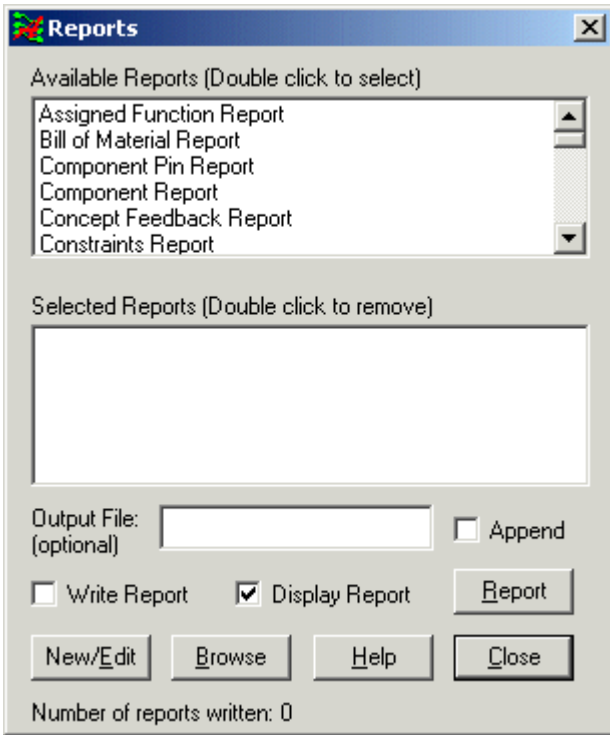
You will find the following reports useful in analyzing routing results:

- **Design Rules Check Report**—This report lists all DRC violations in the current design. For each DRC violation, the PCB Editor identifies the element causing the DRC along with its location and name details. The report also provides a quick summary of total DRCs in the design.
- **Summary Drawing Report**—This report provides an executive summary of the drawing, connection and layout statistics.
- **Unconnected Pins Report**—This report helps you to locate missing connections by providing the x, y coordinate information of all pins requiring connection.

Procedure

1. Open the `drc.brd` file in the PCB Editor.
2. Choose *Tools – Reports*.

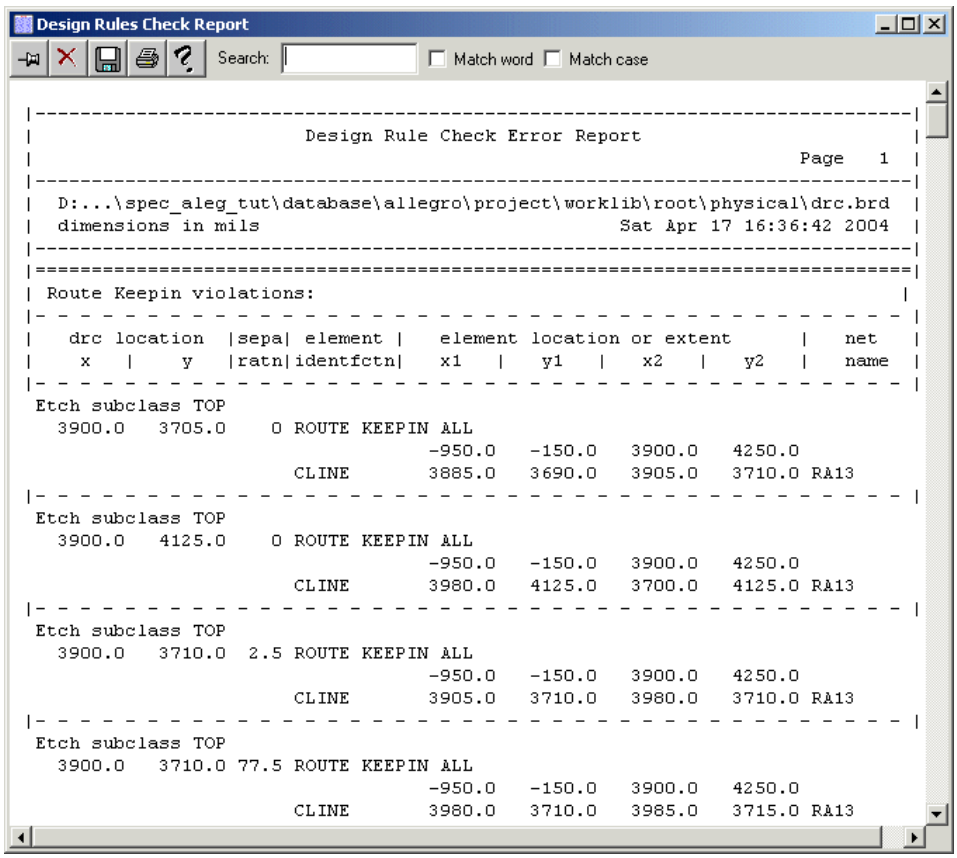
The Reports dialog box appears.



3. Scroll through the list of reports and double-click the *Design Rules Check Report.*

4. Click *Report*.

A window appears titled Design Rules Check Report.



Notice that the report lists the name of the board file and has a timestamp detailing its creation details. Each DRC is detailed and is categorized. If you scroll down the report, you will see the following high-level data:

```
Route Keepin 6
Pad-to-pad -- different net 1
Etch-to-pad -- different net 1
Etch-to-etch -- different net 57
Net Electrical Constraints 1
```

Depending on the DRC violation, you will get the necessary details to correct it. For example, a Route Keepin violation lists the associated subclass, route keepin area details, and the information about all faulting clines.

You can perform quick operations using the Toolbar.

You can save the results to a text file or print results. You can also search for text within the document.

5. Type `mclk` in the *Search* field and press `Enter`.

   The `mclk` net is selected in the report.

   ```
   Propagation Delay
   Required value L:S:2800 MIL:3500 MIL
   Constraint set name PROPAGATION_DELAY
   Netname MCLK
   ```

   Notice that the DRC is caused because the length of the `mclk` connection is not meeting the assigned propagation delay constraint.

   Note: For more information about fixing DRC violations, see Lesson 5-3: Correcting DRC Violations on page 164.

6. Close the Design Rules Check Report.

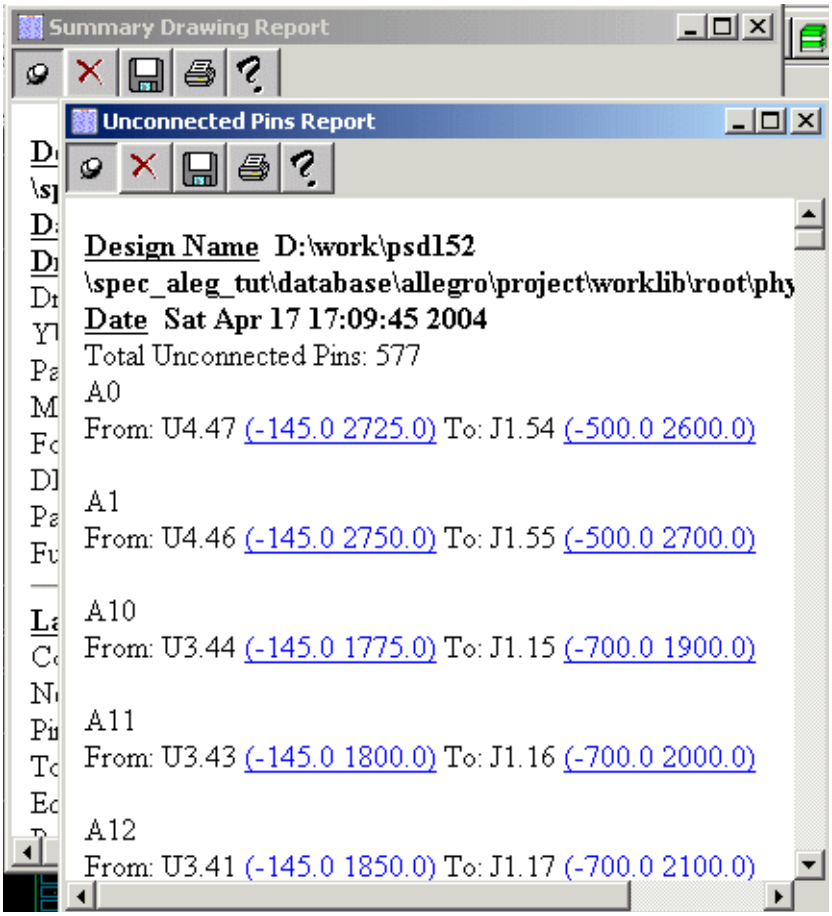
7. Double-click the *Design Rules Check Report* in *Selected Reports* section of the Reports dialog box.

   The *Design Rules Check Report* entry is removed from the *Selected Reports* section of the Reports dialog box.

8. Scroll through the list of reports and double-click the *Summary Drawing Report* and *Unconnected Pins Report*.

9. Click *Report*.

Two report window appear with a list of all unconnected pins and the top-level summary of all elements in the routed board.



You can read the information in these reports.

10. Click *Close* to close the *Summary Drawing Report* and the *Unconnected Pins Report*.

11. Click *Close* to close the Reports dialog box.

Summary

You learned to create different reports that you can use to analyze routing results. You can complete missing connections by finding information about them in the Unconnected Pin report. You can fix DRC violations by analyzing the DRCs in the Design Rules Check report.

A

PCB Router Reference Tables

This appendix discusses the following:

Mapping PCB Editor and PCB Router Names

Some key terms in the PCB Editor are named differently in the PCB Router. The following table lists the mapping of names in the PCB Editor and the PCB Router.

PCB Editor	PCB Router
pin-pair	fromto
pin escapes	fanout
etch or cline	wire
ratsnests	unconnect/guides
shape	area (in rules)
shape	image (for components)
Line lock 45	mitre
DRC	conflict
schedule	pin ordering
symbol	image
constraint area	region

PCB Router Rule Hierarchy

The PCB Router uses the following precedence order while processing rules:

HIGHEST PRECEDENCE

LOWEST PRECEDENCE

- region
- padstack
- class_class_layer
- class_class
- fromto_layer
- fromto
- group_layer
- group
- net_layer
- net
- group_set_layer
- group_set
- class_layer
- class
- layer
- pcb

B

Conclusion

This appendix discusses the following:

- Learning More About the Allegro PCB Editor and Allegro PCB Router
- List of Sample Design Files

Learning More About the Allegro PCB Editor and Allegro PCB Router

Internet Learning Series (ILS) courses

Cadence offers Internet-based training courses for the Allegro PCB Editor and Allegro PCB Router. These are self-paced instruction modules that you run from the Internet. The Internet Learning Series courses offer comprehensive training in how to use the PCB Editor and the PCB Router.

For the most current information about the Internet Learning Series, go to:

http://www.cadence.com/support/education/ils.aspx

Instructor-led courses

Cadence offers in-depth training courses for the PCB Editor and the PCB Router. These are led by highly qualified instructors who are experienced users of the tools. The courses give you thorough and complete training in how to be most productive using the PCB Editor and the PCB Router. Cadence encourages you to gain more advanced knowledge about the tools by taking these instructor-led courses.

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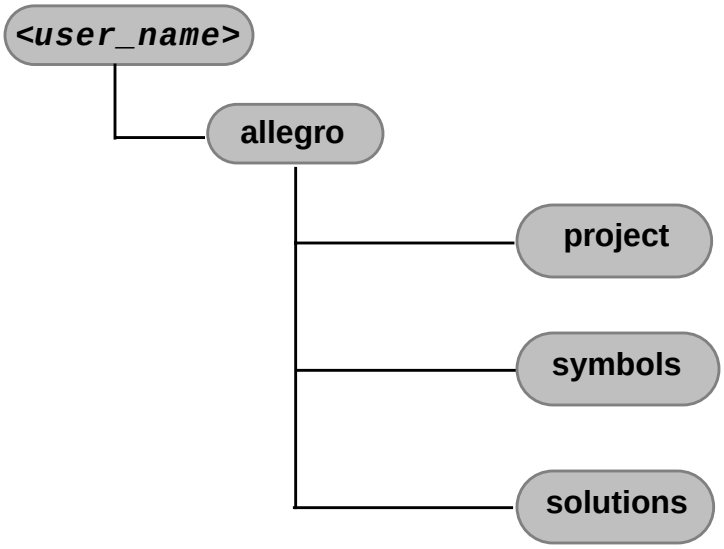
List of Sample Design Files

The zipped or tarred copy of the tutorial database is located in the directory:

```
<your_inst_dir>/doc/aleg_spec_tut/examples/
```

After you have unzipped the `aleg_spec_tut_db.zip` file or untarred the `aleg_spec_tut_db.t.Z` file, you will get the following directory structure.



The `project` directory contains a complete project with a `cpm` file, associated schematic and board data. You can access the board data by navigating to the `physical` folder under the `root` design.

The `symbol` directory contains all the symbols you need to create different boards in this tutorial.

The `solutions` directory contains different board files that are created in various exercises in this tutorial. You can access these board files in case you are struck completing some exercise or if you want to see the results of any operation. This directory also contains a do file that is used as an example for completing an exercise in the tutorial.