

# MOS FIELD EFFECT POWER TRANSISTOR

# 2SJ303

## SWITCHING

## P-CHANNEL MOS FET

## INDUSTRIAL USE

### DESCRIPTION

The 2SJ303 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

### FEATURES

- Low On-state Resistance.  
 $R_{DS(on)} \leq 0.1 \Omega$  ( $V_{GS} = -10 \text{ V}$ ,  $I_D = -7 \text{ A}$ )  
 $R_{DS(on)} \leq 0.24 \Omega$  ( $V_{GS} = -4 \text{ V}$ ,  $I_D = -6 \text{ A}$ )
- Low  $C_{iss}$   $C_{iss} = 1200 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diode
- Isolated TO-220 Package

### QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

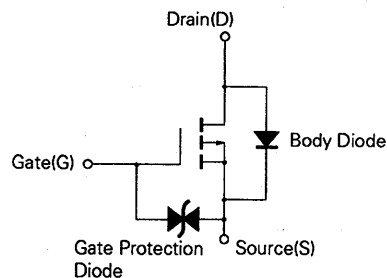
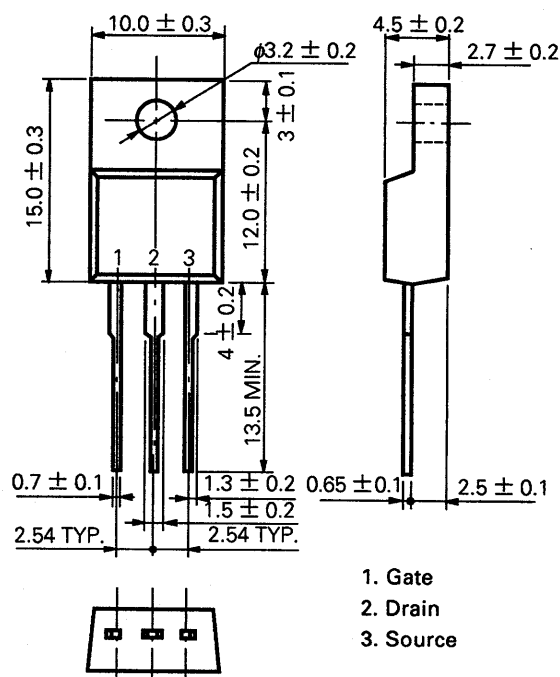
### ABSOLUTE MAXIMUM RATINGS ( $T_a = 25^\circ\text{C}$ )

Drain to Source Voltage	$V_{DSS}$	-60	V
Gate to Source Voltage	$V_{GSS}$	-20, +10	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 14$	A
Drain Current (pulse)	$I_{D(pulse)^*}$	$\pm 56$	A
Total Power Dissipation ( $T_c = 25^\circ\text{C}$ )	$P_{T1}$	35	W
Total Power Dissipation ( $T_a = 25^\circ\text{C}$ )	$P_{T2}$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

\*  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

### PACKAGE DIMENSIONS

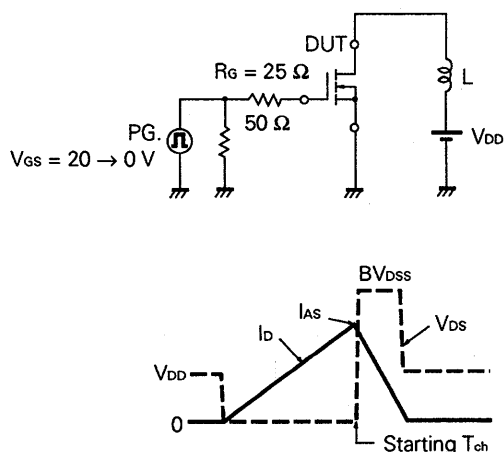
in millimeters



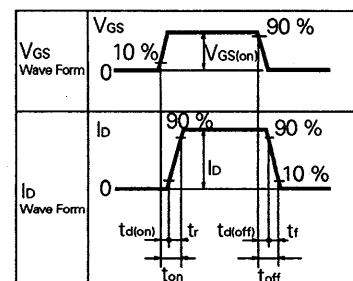
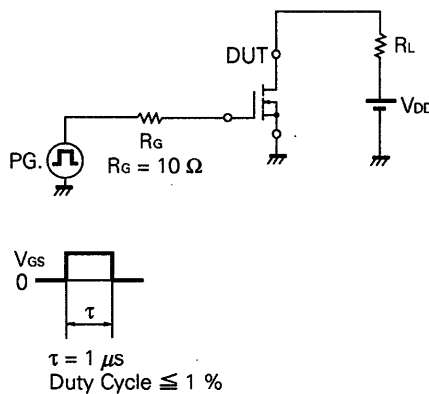
ELECTRICAL CHARACTERISTICS ( $T_a = 25^\circ\text{C}$ )

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		75	100	$\text{m}\Omega$	$V_{GS} = -10\text{ V}$ , $I_D = -7\text{ A}$
Drain to Source On-state Resistance	$R_{DS(on)}$		130	240	$\text{m}\Omega$	$V_{GS} = -4.0\text{ V}$ , $I_D = -6\text{ A}$
Gate to Source Cutoff Voltage	$V_{GS(off)}$	-1.0		-2.0	V	$V_{DS} = -10\text{ V}$ , $I_D = -1\text{ mA}$
Forward Transfer Admittance	$ y_{fs} $	5.0			S	$V_{DS} = -10\text{ V}$ , $I_D = -7\text{ A}$
Drain Leakage Current	$I_{DSS}$			-10	$\mu\text{A}$	$V_{DS} = -60\text{ V}$ , $V_{GS} = 0$
Gate to Source Leakage Current	$I_{GSS}$			$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 16\text{ V}$ , $V_{DS} = 0$
Input Capacitance	$C_{iss}$		1200		pF	$V_{DS} = -10\text{ V}$ $V_{GS} = 0$ $f = 1\text{ MHz}$
Output Capacitance	$C_{oss}$		670		pF	
Reverse Transfer Capacitance	$C_{rss}$		290		pF	
Turn-On Delay Time	$t_{d(on)}$		30		ns	$V_{GS(on)} = -10\text{ V}$ $V_{DD} = -30\text{ V}$ $I_D = -7\text{ A}$ , $R_G = 10\ \Omega$ $R_L = 4.3\ \Omega$
Rise Time	$t_r$		110		ns	
Turn-Off Delay Time	$t_{d(off)}$		160		ns	
Fall Time	$t_f$		120		ns	
Total Gate Charge	$Q_G$		42		nC	$V_{GS} = -10\text{ V}$ $I_D = -16\text{ A}$ $V_{DD} = -48\text{ V}$
Gate to Source Charge	$Q_{GS}$		3		nC	
Gate to Drain Charge	$Q_{GD}$		17		nC	
Diode Forward Voltage	$V_{SD}$		1.0		V	$I_F = -14\text{ A}$ , $V_{GS} = 0$
Reverse Recovery Time	$t_{rr}$		120		ns	$I_F = -14\text{ A}$ , $V_{GS} = 0$ $di/dt = 50\text{ A}/\mu\text{s}$
Reverse Recovery Charge	$Q_{rr}$		230		nC	

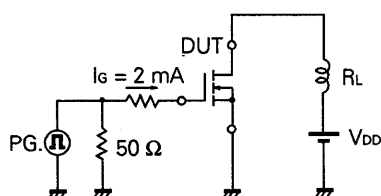
## Test Circuit 1 : Avalanche Capability



## Test Circuit 2 : Switching Time

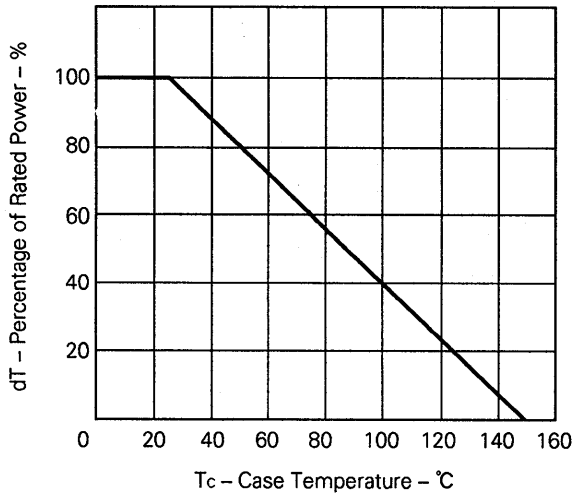


## Test Circuit 3 : Gate Charge

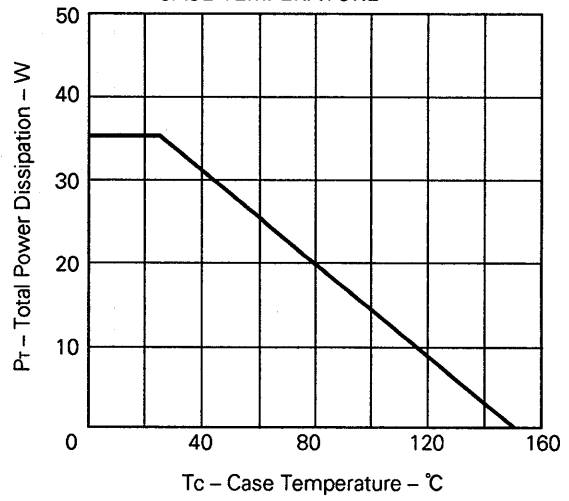


TYPICAL CHARACTERISTICS ( $T_a = 25^\circ\text{C}$ )

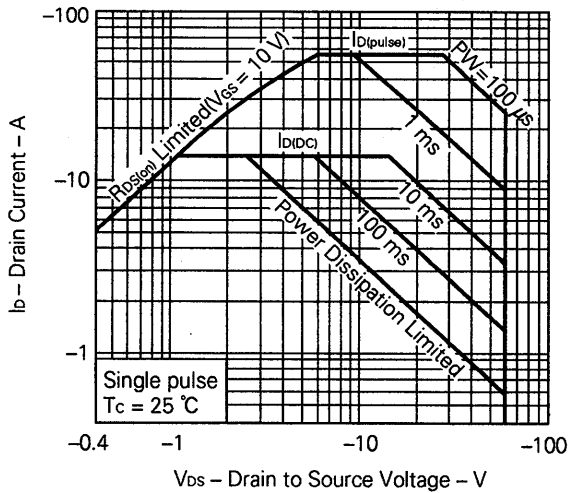
DERATING FACTOR OF FORWARD BIAS  
SAFE OPERATING AREA



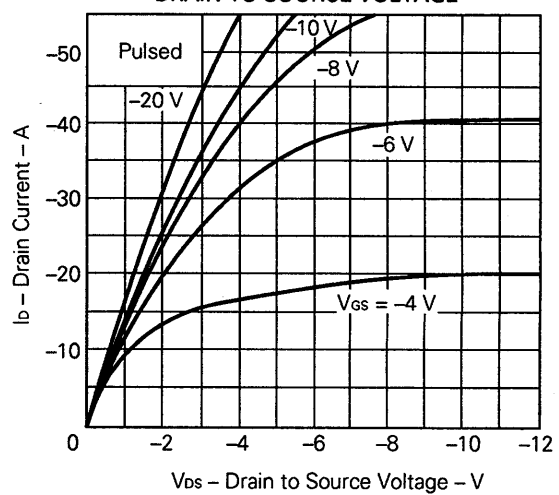
TOTAL POWER DISSIPATION vs.  
CASE TEMPERATURE



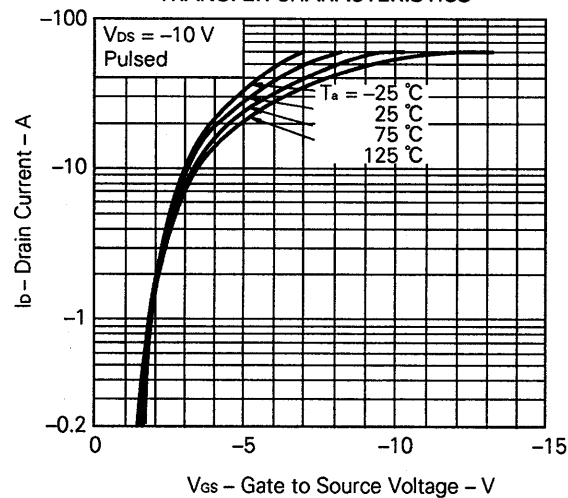
FORWARD BIAS SAFE OPERATING AREA

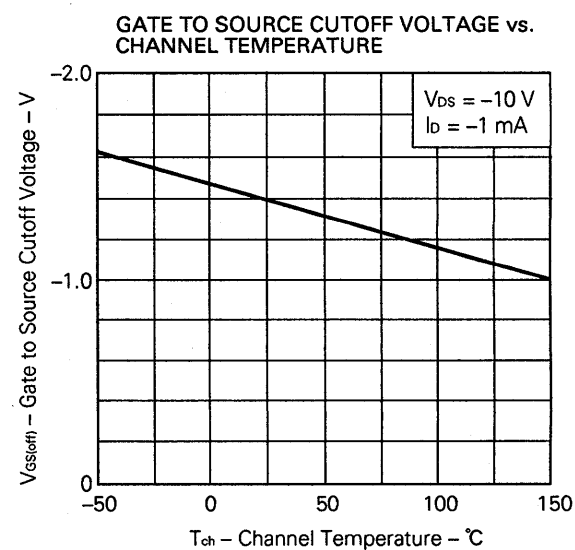
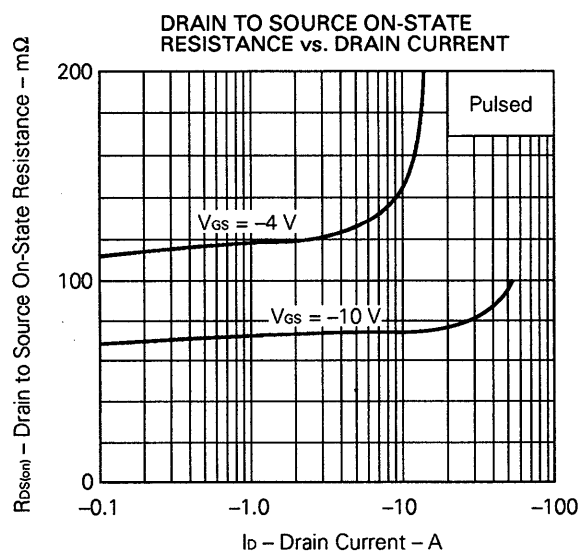
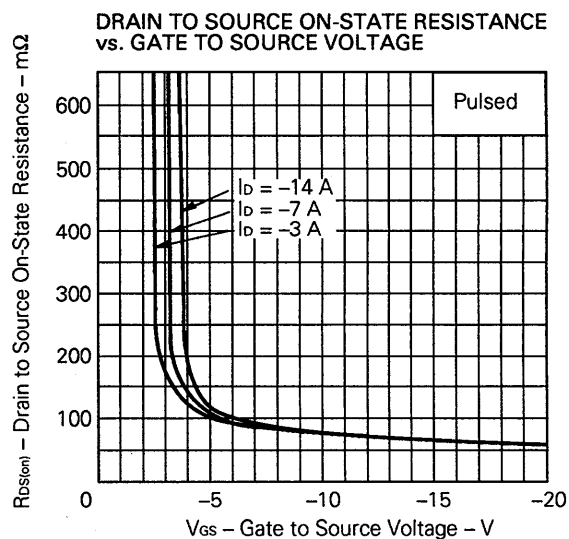
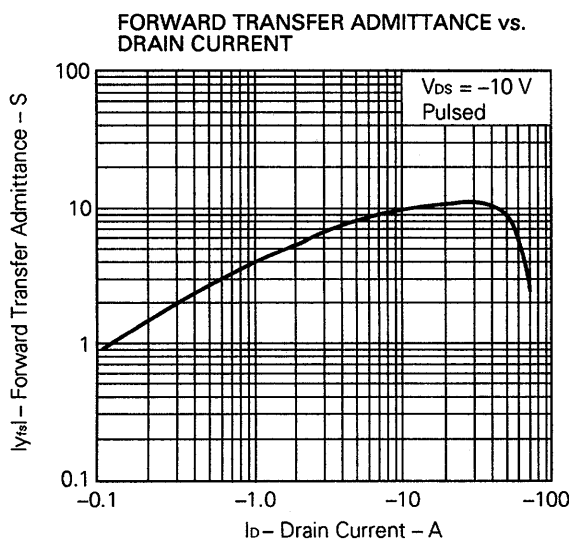
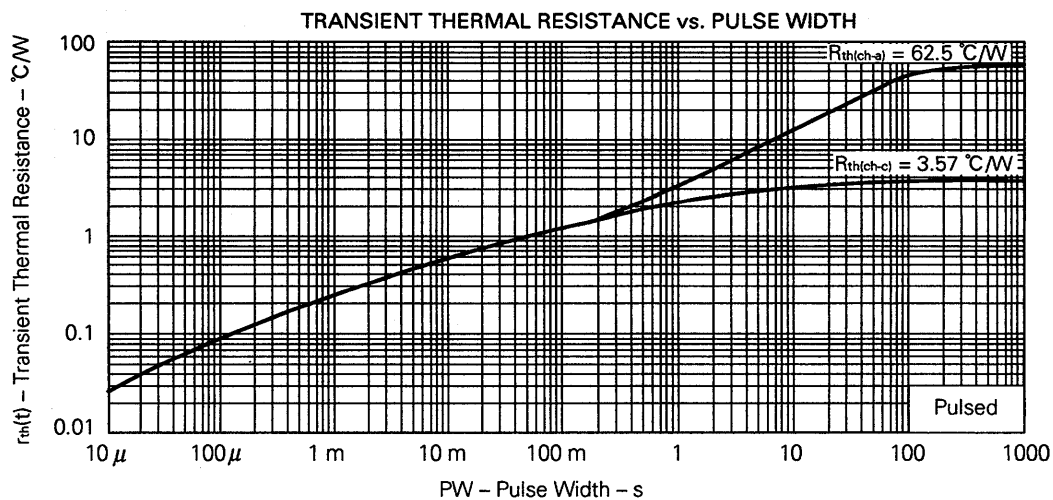


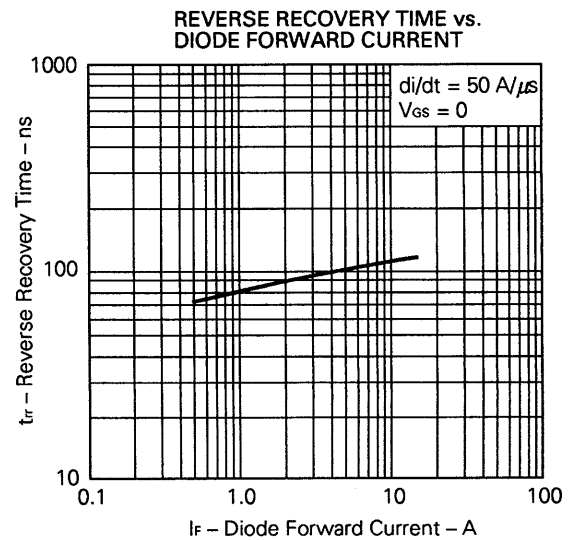
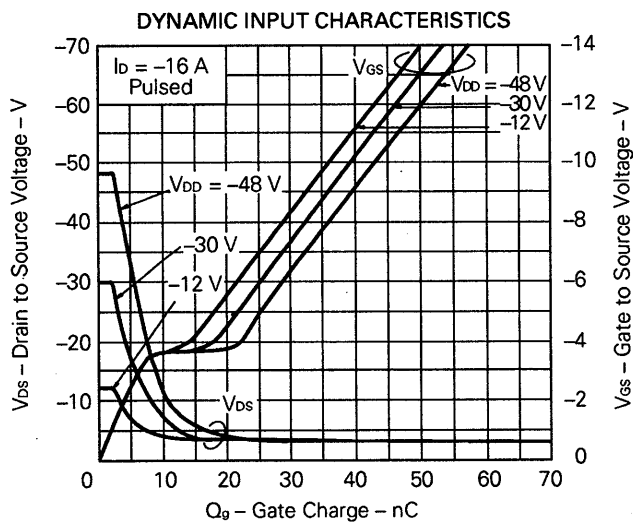
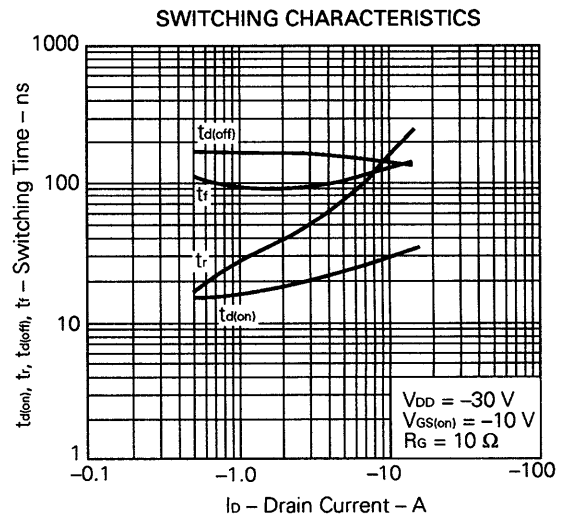
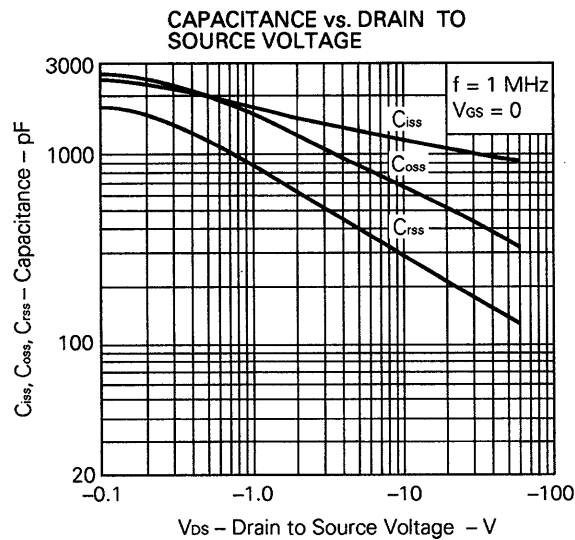
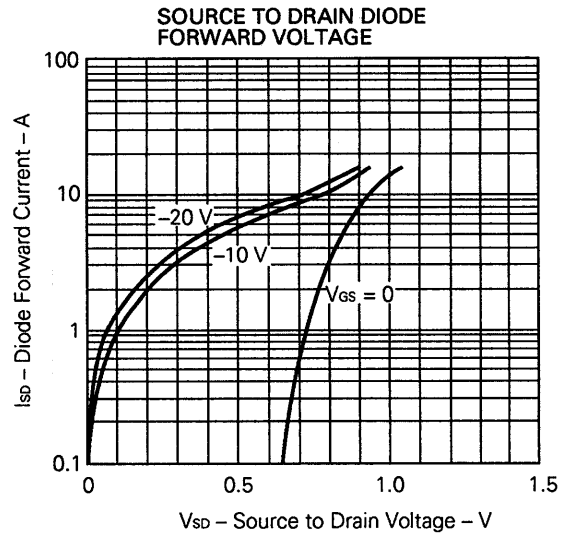
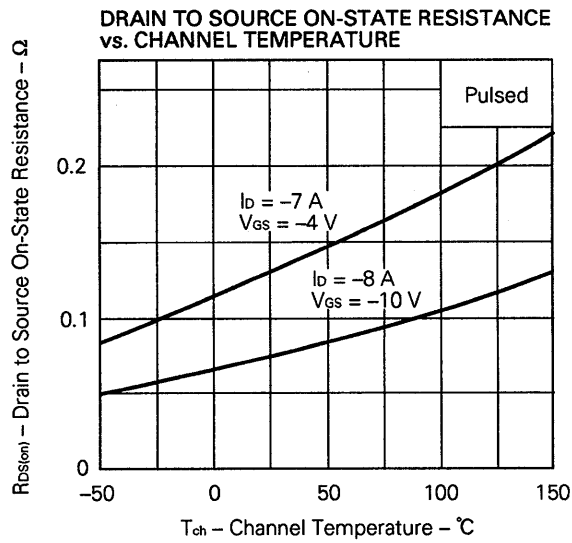
DRAIN CURRENT vs.  
DRAIN TO SOURCE VOLTAGE

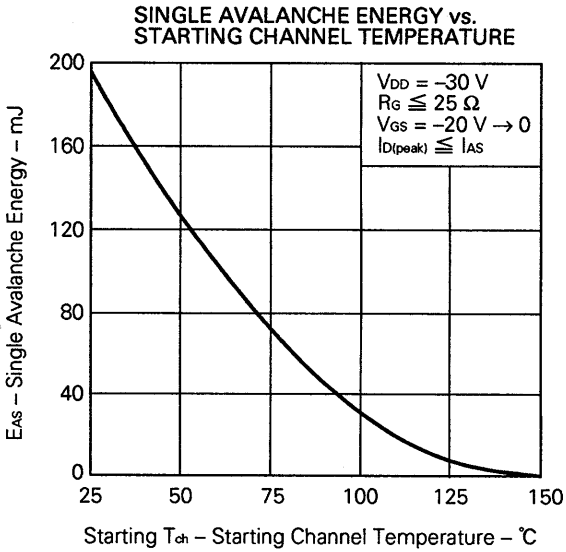
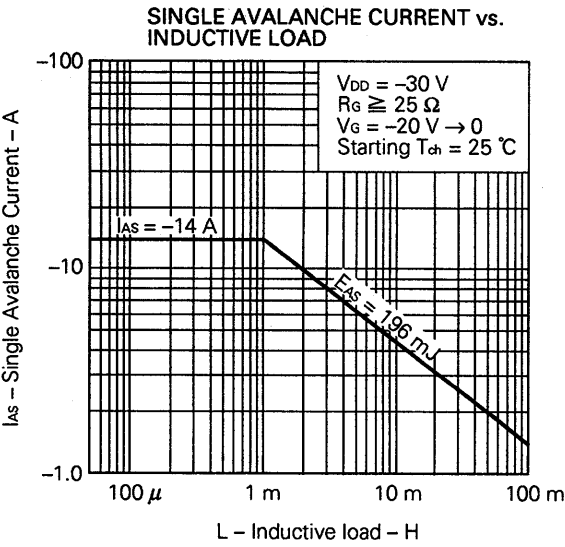


TRANSFER CHARACTERISTICS









**Reference**

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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