

# Integration Manual

for S32K1\_S32M24X MCL Driver

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## Chapter 1

### Revision History

Revision	Date	Author	Description
1.0	04.08.2023	NXP RTD Team	S32K1_S32M24X Real-Time Drivers AUTOSAR 4.4 & R21-11 Version 2.0.0

## Chapter 2

### Introduction

- [Supported Derivatives](#)
- [Overview](#)
- [About This Manual](#)
- [Acronyms and Definitions](#)
- [Reference List](#)

This Integration Manual describes the integration requirements for NXP Mcl Driver for S32K1\_S32M24X.

### 2.1 Supported Derivatives

The software described in this document is intended to be used with the following microcontroller devices of NXP Semiconductors:

- s32k116\_qfn32
- s32k116\_lqfp48
- s32k118\_lqfp48
- s32k118\_lqfp64
- s32k142\_lqfp48
- s32k142\_lqfp64
- s32k142\_lqfp100
- s32k142w\_lqfp48
- s32k142w\_lqfp64
- s32k144\_lqfp48
- s32k144\_lqfp64 / MWCT1014S\_lqfp64
- s32k144\_lqfp100 / MWCT1014S\_lqfp100

- s32k144\_mapbga100
- s32k144w\_lqfp48
- s32k144w\_lqfp64
- s32k146\_lqfp64
- s32k146\_lqfp100 / MWCT1015S\_lqfp100
- s32k146\_mapbga100 / MWCT1015S\_mapbga100
- s32k146\_lqfp144
- s32k148\_lqfp100
- s32k148\_mapbga100 / MWCT1016S\_mapbga100
- s32k148\_lqfp144
- s32k148\_lqfp176
- s32m241\_lqfp64
- s32m242\_lqfp64
- s32m243\_lqfp64
- s32m244\_lqfp64

All of the above microcontroller devices are collectively named as S32K1\_S32M24X. Note: MWCT part numbers contain NXP confidential IP for Qi Wireless Power

## 2.2 Overview

**AUTOSAR (AUTomotive Open System ARchitecture)** is an industry partnership working to establish standards for software interfaces and software modules for automobile electronic control systems.

AUTOSAR:

- paves the way for innovative electronic systems that further improve performance, safety and environmental friendliness.
- is a strong global partnership that creates one common standard: "Cooperate on standards, compete on implementation".
- is a key enabling technology to manage the growing electrics/electronics complexity. It aims to be prepared for the upcoming technologies and to improve cost-efficiency without making any compromise with respect to quality.
- facilitates the exchange and update of software and hardware over the service life of the vehicle.

## 2.3 About This Manual

This Technical Reference employs the following typographical conventions:

- **Boldface** style: Used for important terms, notes and warnings.
- *Italic* style: Used for code snippets in the text. Note that C language modifiers such "const" or "volatile" are sometimes omitted to improve readability of the presented code.

Notes and warnings are shown as below:

Note

This is a note.

Warning

This is a warning

## 2.4 Acronyms and Definitions

Term	Definition
API	Application Programming Interface
ASM	Assembler
BSMI	Basic Software Make file Interface
CAN	Controller Area Network
C/CPP	C and C++ Source Code
CS	Chip Select
CTU	Cross Trigger Unit
DEM	Diagnostic Event Manager
DET	Development Error Tracer
DMA	Direct Memory Access
ECU	Electronic Control Unit
FIFO	First In First Out
LSB	Least Significant Bit
MCU	Micro Controller Unit
MIDE	Multi Integrated Development Environment
MSB	Most Significant Bit
N/A	Not Applicable
RAM	Random Access Memory
SIU	Systems Integration Unit
SWS	Software Specification
VLE	Variable Length Encoding
XML	Extensible Markup Language

## 2.5 Reference List

#	Title	Version
1	S32K1xx Series Reference Manual	Rev. 14, 09/2021
2	Errata S32K116_0N96V	Rev. 22/OCT/2021
3	Errata S32K118_0N97V	Rev. 22/OCT/2021
4	Errata S32K142_0N33V	Rev. 22/OCT/2021
5	Errata S32K144_0N57U	Rev. 22/OCT/2021
6	Errata S32K144W_0P64A	Rev. 22/OCT/2021
7	Errata S32K146_0N73V	Rev. 22/OCT/2021
8	Errata S32K148_0N20V	Rev. 22/OCT/2021
9	S32K1xx Data Sheet	Rev. 14, 08/2021
10	S32M24x Reference Manual	Rev. 2 Draft A, 05/2023
11	Errata S32M244_P64A+P73G	Rev. 0
12	Errata S32M242_N33V+P73G	Rev. 0, 06/2023
13	S32M2xx Data Sheet	Rev. 3 DraftA, 05/2023



## Chapter 3

### Building the driver

- [Build Options](#)
- [Files required for compilation](#)
- [Setting up the plugins](#)

This section describes the source files and various compilers, linker options used for building the driver. It also explains the EB Tresos Studio plugin setup procedure.

#### 3.1 Build Options

- [GCC Compiler/Assembler/Linker Options](#)
- [IAR Compiler/Assembler/Linker Options](#)
- [GHS Compiler/Assembler/Linker Options](#)

The RTD driver files are compiled using:

- NXP GCC 10.2.0 20200723 (Build 1728 Revision g5963bc8)
- IAR ANSI C/C++ Compiler V8.40.3.228/W32 for ARM Functional Safety
- Green Hills Multi 7.1.6d / Compiler 2020.1.4

The compiler, assembler, and linker flags used for building the driver are explained below.

The TS\_T40D2M20I0R0 part of the plugin name is composed as follows:

- T = Target\_Id (e.g. T40 identifies Cortex-M architecture)
- D = Derivative\_Id (e.g. D2 identifies S32K1 platform)
- M = SW\_Version\_Major and SW\_Version\_Minor
- I = SW\_Version\_Patch
- R = Reserved

##### 3.1.1 GCC Compiler/Assembler/Linker Options

###### 3.1.1.1 GCC Compiler Options

Compiler Option	Description
-mcpu=cortex-m4	Targeted ARM processor for which GCC should tune the performance of the code (for S32K14x or S32M24x devices)
-mcpu=cortex-m0plus	Targeted ARM processor for which GCC should tune the performance of the code (for S32K11x devices)
-mthumb	Generates code that executes in Thumb state
-mlittle-endian	Generate code for a processor running in little-endian mode
-mfpv4-sp-d16	Specifies the floating-point hardware available on the target (for S32K14x or S32M24x devices)
-mfloat-abi=hard	Specifies the floating-point ABI to use. "hard" allows generation of floating-point instructions and uses FPU-specific calling conventions (for S32K14x or S32M24x devices)
-mfpv4-sp-d16	Specifies the floating-point hardware available on the target (for S32K11x devices)
-mfloat-abi=soft	Specifies the floating-point ABI to use. Specifying "soft" causes GCC to generate output containing library calls for floating-point operations (for S32K11x devices)
-std=c99	Specifies the ISO C99 base standard
-Os	Optimize for size. Enables all -O2 optimizations except those that often increase code size
-ggdb3	Produce debugging information for use by GDB using the most expressive format available, including GDB extensions if at all possible. Level 3 includes extra information, such as all the macro definitions present in the program
-Wall	Enables all the warnings about constructions that some users consider questionable, and that are easy to avoid (or modify to prevent the warning), even in conjunction with macros
-Wextra	This enables some extra warning flags that are not enabled by -Wall
-pedantic	Issue all the warnings demanded by strict ISO C. Reject all programs that use forbidden extensions. Follows the version of the ISO C standard specified by the aforementioned -std option
-Wstrict-prototypes	Warn if a function is declared or defined without specifying the argument types
-Wundef	Warn if an undefined identifier is evaluated in an #if directive. Such identifiers are replaced with zero
-Wunused	Warn whenever a function, variable, label, value, macro is unused
-Werror=implicit-function-declaration	Make the specified warning into an error. This option throws an error when a function is used before being declared
-Wsign-compare	Warn when a comparison between signed and unsigned values could produce an incorrect result when the signed value is converted to unsigned.
-Wdouble-promotion	Give a warning when a value of type float is implicitly promoted to double
-fno-short-enums	Specifies that the size of an enumeration type is at least 32 bits regardless of the size of the enumerator values.

Compiler Option	Description
-funsigned-char	Let the type char be unsigned by default, when the declaration does not use either signed or unsigned
-funsigned-bitfields	Let a bit-field be unsigned by default, when the declaration does not use either signed or unsigned
-fomit-frame-pointer	Omit the frame pointer in functions that don't need one. This avoids the instructions to save, set up and restore the frame pointer; on many targets it also makes an extra register available.
-fno-common	Makes the compiler place uninitialized global variables in the BSS section of the object file. This inhibits the merging of tentative definitions by the linker so you get a multiple-definition error if the same variable is accidentally defined in more than one compilation unit
-fstack-usage	This option is only used to build test for generation Ram/↔ Stack size report. Makes the compiler output stack usage information for the program, on a per-function basis
-fdump-ipa-all	This option is only used to build test for generation Ram/↔ Stack size report. Enables all inter-procedural analysis dumps
-c	Stop after assembly and produce an object file for each source file
-DS32K1XX	Predefine S32K1XX as a macro, with definition 1
-DS32K148	Predefine S32K148 as a macro, with definition 1. S32↔K148 can be replaced according to derivatives name S32K116,S32K118,S32K142,S32K142W,S32K144,S32↔K144W,S32K146,S32K148,S32M244,S32M242.
-DGCC	Predefine GCC as a macro, with definition 1
-DUSE_SW_VECTOR_MODE	Predefine USE_SW_VECTOR_MODE as a macro, with definition 1. By default, the drivers are compiled to handle interrupts in Software Vector Mode
-DI_CACHE_ENABLE	Predefine I_CACHE_ENABLE as a macro, with definition 1. Enables instruction cache initialization in source file system.c under the Platform driver (for S32K14x or S32↔M24x devices)
-DENABLE_FPU	Predefine ENABLE_FPU as a macro, with definition 1. Enables FPU initialization in source file system.c under the Platform driver (for S32K14x or S32M24x devices)
-DMCAL_ENABLE_USER_MODE_SUPPORT	Predefine MCAL_ENABLE_USER_MODE_SUPPO↔RT as a macro, with definition 1. Allows drivers to be configured in user mode.
-sysroot=	Specifies the path to the sysroot, for Cortex-M7 it is /arm-none-eabi/newlib
-specs=nano.specs	Use Newlib nano specs
-specs=nosys.specs	Do not use printf/scanf

### 3.1.1.2 GCC Assembler Options

Assembler Option	Description
-Xassembler-with-cpp	Specifies the language for the following input files (rather than letting the compiler choose a default based on the file name suffix)
-mcpu=cortex-m4	Targeted ARM processor for which GCC should tune the performance of the code (for S32K14x or S32M24x devices)
-mcpu=cortex-m0plus	Targeted ARM processor for which GCC should tune the performance of the code (for S32K11x devices)
-mfpu=fpv4-sp-d16	Specifies the floating-point hardware available on the target (for S32K14x devices)
-mfloat-abi=hard	Specifies the floating-point ABI to use. "hard" allows generation of floating-point instructions and uses FPU-specific calling conventions (for S32K14x devices)
-mfpu=auto	Specifies the floating-point hardware available on the target (for S32K11x devices)
-mfloat-abi=soft	Specifies the floating-point ABI to use. Specifying "soft" causes GCC to generate output containing library calls for floating-point operations (for S32K11x devices)
-mthumb	Generates code that executes in Thumb state
-c	Stop after assembly and produce an object file for each source file

### 3.1.1.3 GCC Linker Options

Linker Option	Description
-Wl,-Map,filename	Produces a map file
-T linkerfile	Use linkerfile as the linker script. This script replaces the default linker script (rather than adding to it)
-entry=Reset_Handler	Specifies that the program entry point is Reset_Handler
-nostartfiles	Do not use the standard system startup files when linking
-mcpu=cortex-m4	Targeted ARM processor for which GCC should tune the performance of the code (for S32K14x or S32M24x devices)
-mcpu=cortex-m0plus	Targeted ARM processor for which GCC should tune the performance of the code (for S32K11x devices)
-mthumb	Generates code that executes in Thumb state
-mfpu=fpv4-sp-d16	Specifies the floating-point hardware available on the target (for S32K14x or S32M24x devices)
-mfloat-abi=hard	Specifies the floating-point ABI to use. "hard" allows generation of floating-point instructions and uses FPU-specific calling conventions (for S32K14x or S32M24x devices)
-mfpu=auto	Specifies the floating-point hardware available on the target (for S32K11x devices)
-mfloat-abi=soft	Specifies the floating-point ABI to use. Specifying "soft" causes GCC to generate output containing library calls for floating-point operations (for S32K11x devices)
-mlittle-endian	Generate code for a processor running in little-endian mode
-ggdb3	Produce debugging information for use by GDB using the most expressive format available, including GDB extensions if at all possible. Level 3 includes extra information, such as all the macro definitions present in the program
-lc	Link with the C library
-lm	Link with the Math library
-lgcc	Link with the GCC library
-n	Turn off page alignment of sections, and disable linking against shared libraries
-sysroot=	Specifies the path to the sysroot, for Cortex-M7 it is /arm-none-eabi/newlib

Linker Option	Description
-specs=nano.specs	Use Newlib nano specs
-specs=nosys.specs	Do not use printf/scanf

### 3.1.2 IAR Compiler/Assembler/Linker Options

#### 3.1.2.1 IAR Compiler Options

Compiler Option	Description
-cpu=Cortex-M4	Targeted ARM processor for which IAR should tune the performance of the code (for S32K14x or S32M24x devices)
-cpu=Cortex-M0+	Targeted ARM processor for which IAR should tune the performance of the code (for S32K11x devices)
-cpu_mode=thumb	Generates code that executes in Thumb state
-endian=little	Generate code for a processor running in little-endian mode
-fpu=FPv4-SP	Use this option to generate code that performs floating-point operations using a Floating Point Unit (FPU). Single-precision variant. (for S32K14x or S32M24x devices)
-fpu=none	Use this option to generate code that performs floating-point operations using a Floating Point Unit (FPU). No FPU. (for S32K11x devices)
-e	Enables all IAR C language extensions
-Ohz	Optimize for size. The compiler will emit AEABI attributes indicating the requested optimization goal. This information can be used by the linker to select smaller or faster variants of DLIB library functions
-debug	Makes the compiler include debugging information in the object modules. Including debug information will make the object files larger
-no_clustering	Disables static clustering optimizations. Static and global variables defined within the same module will not be arranged so that variables that are accessed in the same function are close to each other
-no_mem_idioms	Makes the compiler not optimize certain memory access patterns
-no_explicit_zero_opt	Do not treat explicit initializations to zero of static variables as zero initializations
-require_prototypes	Force the compiler to verify that all functions have proper prototypes. Generates an error otherwise
-no_wrap_diagnostics	Does not wrap long lines in diagnostic messages
-diag_suppress=Pa050	Suppresses diagnostic message Pa050
-DS32K1XX	Predefine S32K1XX as a macro, with definition 1
-DS32K148	Predefine S32K148 as a macro, with definition 1. S32K148 can be replaced according to derivatives name S32K116,S32K118,S32K142,S32K142W,S32K144,S32K144W,S32K146,S32K148,S32M244,S32M242.
-DIAR	Predefine IAR as a macro, with definition 1

Compiler Option	Description
-DUSE_SW_VECTOR_MODE	Predefine USE_SW_VECTOR_MODE as a macro, with definition 1. By default, the drivers are compiled to handle interrupts in Software Vector Mode.
-DI_CACHE_ENABLE	Predefine I_CACHE_ENABLE as a macro, with definition 1. Enables instruction cache initialization in source file system.c under the Platform driver (for S32K14x or S32M24x devices)
-DENABLE_FPU	Predefine ENABLE_FPU as a macro, with definition 1. Enables FPU initialization in source file system.c under the Platform driver (for S32K14x or S32M24x devices)
-DMCAL_ENABLE_USER_MODE_SUPPORT	Predefine MCAL_ENABLE_USER_MODE_SUPPORT as a macro, with definition 1. Allows drivers to be configured in user mode.

### 3.1.2.2 IAR Assembler Options

Assembler Option	Description
-cpu=Cortex-M4	Targeted ARM processor for which IAR should tune the performance of the code (for S32K14x or S32M24x devices)
-cpu=Cortex-M0+	Targeted ARM processor for which IAR should tune the performance of the code (for S32K11x devices)
-fpu=FPv4-SP	Use this option to generate code that performs floating-point operations using a Floating Point Unit (FPU). Single-precision variant. (for S32K14x devices)
-fpu=none	Use this option to generate code that performs floating-point operations using a Floating Point Unit (FPU). No FPU. (for S32K11x devices)
-cpu_mode thumb	Selects the thumb mode for the assembler directive CODE
-g	Disables the automatic search for system include files
-r	Generates debug information

### 3.1.2.3 IAR Linker Options

Linker Option	Description
-map filename	Produces a map file
-config linkerfile	Use linkerfile as the linker script. This script replaces the default linker script (rather than adding to it)
-cpu=Cortex-M4	Targeted ARM processor for which IAR should tune the performance of the code (for S32K14x or S32M24x devices)
-cpu=Cortex-M0+	Targeted ARM processor for which IAR should tune the performance of the code (for S32K11x devices)
-fpu=FPv4-SP	Use this option to generate code that performs floating-point operations using a Floating Point Unit (FPU). Single-precision variant. (for S32K14x or S32M24x devices)
-fpu=none	Use this option to generate code that performs floating-point operations using a Floating Point Unit (FPU). No FPU. (for S32K11x devices)

Linker Option	Description
-entry _start	Treats _start as a root symbol and start label
-enable_stack_usage	Enables stack usage analysis. If a linker map file is produced, a stack usage chapter is included in the map file
-skip_dynamic_initialization	Dynamic initialization (typically initialization of C++ objects with static storage duration) will not be performed automatically during application startup
-no_wrap_diagnostics	Does not wrap long lines in diagnostic messages

### 3.1.3 GHS Compiler/Assembler/Linker Options

#### 3.1.3.1 GHS Compiler Options

Compiler Option	Description
-cpu=cortexm4	Selects target processor: Arm Cortex M4 (for S32K14x or S32M24x devices)
-cpu=cortexm0plus	Selects target processor: Arm Cortex M0+ (for S32K11x devices)
-thumb	Selects generating code that executes in Thumb state
-fpu=vfpv4_d16	Specifies hardware floating-point using the v4 version of the VFP instruction set, with 16 double-precision floating-point registers (for S32K14x or S32M24x devices)
-fsingle	Use hardware single-precision, software double-precision FP instructions (for S32K14x or S32M24x devices)
-fsoft	Specifies software floating-point (SFP) mode. This setting causes your target to use integer registers to hold floating-point data and use library subroutine calls to emulate floating-point operations (for S32K11x devices)
-C99	Use (strict ISO) C99 standard (without extensions)
-ghstd=last	Use the most recent version of Green Hills Standard mode (which enables warnings and errors that enforce a stricter coding standard than regular C and C++)
-Osize	Optimize for size
-gnu_asm	Enables GNU extended asm syntax support
-dual_debug	Generate DWARF 2.0 debug information
-G	Generate debug information
-keeptempfiles	Prevents the deletion of temporary files after they are used. If an assembly language file is created by the compiler, this option will place it in the current directory instead of the temporary directory
-Wimplicit-int	Produce warnings if functions are assumed to return int
-Wshadow	Produce warnings if variables are shadowed
-Wtrigraphs	Produce warnings if trigraphs are detected
-Wundef	Produce a warning if undefined identifiers are used in #if preprocessor statements
-unsigned_chars	Let the type char be unsigned, like unsigned char

Compiler Option	Description
-unsigned_fields	Bitfields declared with an integer type are unsigned
-no_commons	Allocates uninitialized global variables to a section and initializes them to zero at program startup
-no_exceptions	Disables C++ support for exception handling
-no_slash_comment	C++ style // comments are not accepted and generate errors
-prototype_errors	Controls the treatment of functions referenced or called when no prototype has been provided
-incorrect_pragma_warnings	Controls the treatment of valid #pragma directives that use the wrong syntax
-c	Stop after assembly and produce an object file for each source file
-DS32K1XX	Predefine S32K1XX as a macro, with definition 1
-DS32K148	Predefine S32K148 as a macro, with definition 1. S32K148 can be replaced according to derivatives name S32K116,S32K118,S32K142,S32K142W,S32K144,S32K144W,S32K146,S32K148,S32M244,S32M242.
-DGHS	Predefine GHS as a macro, with definition 1
-DUSE_SW_VECTOR_MODE	Predefine USE_SW_VECTOR_MODE as a macro, with definition 1. By default, the drivers are compiled to handle interrupts in Software Vector Mode
-DI_CACHE_ENABLE	Predefine I_CACHE_ENABLE as a macro, with definition 1. Enables instruction cache initialization in source file system.c under the Platform driver (for S32K14x or S32M24x devices)
-DENABLE_FPU	Predefine ENABLE_FPU as a macro, with definition 1. Enables FPU initialization in source file system.c under the Platform driver (for S32K14x or S32M24x devices)
-DMCAL_ENABLE_USER_MODE_SUPPORT	Predefine MCAL_ENABLE_USER_MODE_SUPPORT as a macro, with definition 1. Allows drivers to be configured in user mode

### 3.1.3.2 GHS Assembler Options

Assembler Option	Description
-cpu=cortexm4	Selects target processor: Arm Cortex M4 (for S32K14x or S32M24x devices)
-cpu=cortexm0plus	Selects target processor: Arm Cortex M0+ (for S32K11x devices)
-fpu=vfpv4_d16	Specifies hardware floating-point using the v4 version of the VFP instruction set, with 16 double-precision floating-point registers (for S32K14x devices)
-fsingle	Use hardware single-precision, software double-precision FP instructions (for S32K14x devices)
-fsoft	Specifies software floating-point (SFP) mode. This setting causes your target to use integer registers to hold floating-point data and use library subroutine calls to emulate floating-point operations (for S32K11x devices)
-preprocess_assembly_files	Controls whether assembly files with standard extensions such as .s and .asm are preprocessed
-list	Creates a listing by using the name and directory of the object file with the .lst extension



Assembler Option	Description
-c	Stop after assembly and produce an object file for each source file

### 3.1.3.3 GHS Linker Options

Linker Option	Description
-e Reset_Handler	Make the symbol Reset_Handler be treated as a root symbol and the start label of the application
-T linker_script_file.ld	Use linker_script_file.ld as the linker script. This script replaces the default linker script (rather than adding to it)
-map	Produce a map file
-keepmap	Controls the retention of the map file in the event of a link error
-Mn	Generates a listing of symbols sorted alphabetically/numerically by address
-delete	Instructs the linker to remove functions that are not referenced in the final executable. The linker iterates to find functions that do not have relocations pointing to them and eliminates them
-ignore_debug_references	Ignores relocations from DWARF debug sections when using -delete. DWARF debug information will contain references to deleted functions that may break some third-party debuggers
-Llibrary_path	Points to library_path (the libraries location) for thumb2 to be used for linking
-larch	Link architecture specific library
-lstartup	Link run-time environment startup routines. The source code for the modules in this library is provided in the src/libstartup directory
-lind_sd	Link language-independent library, containing support routines for features such as software floating point, run-time error checking, C99 complex numbers, and some general purpose routines of the ANSI C library (for S32K14x or S32M24x devices)
-lind_sf	Link language-independent library, containing support routines for features such as software floating point, run-time error checking, C99 complex numbers, and some general purpose routines of the ANSI C library (for S32K11x devices)
-v	Prints verbose information about the activities of the linker, including the libraries it searches to resolve undefined symbols
-keep=C40_Ip_AccessCode	Avoid linker remove function C40_Ip_AccessCode from Fls module because it is not referenced explicitly
-nostartfiles	Controls the start files to be linked into the executable

## 3.2 Files required for compilation

This section describes the include files required to compile, assemble and link the Mcl Driver for S32K1 microcontrollers.

To avoid integration of incompatible files, all the include files from other modules shall have the same AR\_MAJOR\_VERSION and AR\_MINOR\_VERSION, i.e. only files with the same major and minor versions can be compiled.

### 3.2.0.0.1 MCL Driver Files:

- Mcl\_TS\_T40D2M20I0R0\src\Cache\_Ip.c
- Mcl\_TS\_T40D2M20I0R0\src\Cache\_Ip\_HwAcc\_Lmem.h
- Mcl\_TS\_T40D2M20I0R0\src\CDD\_Mcl.c
- Mcl\_TS\_T40D2M20I0R0\src\CDD\_Mcl\_Ipw.c
- Mcl\_TS\_T40D2M20I0R0\src\Dma\_Ip.c
- Mcl\_TS\_T40D2M20I0R0\src\Dma\_Ip\_Driver\_State.c
- Mcl\_TS\_T40D2M20I0R0\src\Dma\_Ip\_Driver\_State.h
- Mcl\_TS\_T40D2M20I0R0\src\Dma\_Ip\_Hw\_Access.c
- Mcl\_TS\_T40D2M20I0R0\src\Dma\_Ip\_Hw\_Access.h
- Mcl\_TS\_T40D2M20I0R0\src\Dma\_Ip\_Hwv2\_AccessInline.h
- Mcl\_TS\_T40D2M20I0R0\src\Dma\_Ip\_Irq.c
- Mcl\_TS\_T40D2M20I0R0\src\Dma\_Ip\_Multicore.c
- Mcl\_TS\_T40D2M20I0R0\src\Flexio\_Mcl\_Ip.c
- Mcl\_TS\_T40D2M20I0R0\src\Flexio\_Mcl\_Ip\_HwAccess.c
- Mcl\_TS\_T40D2M20I0R0\src\Flexio\_Mcl\_Ip\_Irq.c
- Mcl\_TS\_T40D2M20I0R0\src\Trgmux\_Ip.c
- Mcl\_TS\_T40D2M20I0R0\src\Trgmux\_Ip\_HwAcc.h
- Mcl\_TS\_T40D2M20I0R0\include\Cache\_Ip.h
- Mcl\_TS\_T40D2M20I0R0\include\Cache\_Ip\_Devassert.h
- Mcl\_TS\_T40D2M20I0R0\include\Cache\_Ip\_Types.h
- Mcl\_TS\_T40D2M20I0R0\include\CDD\_Mcl.h
- Mcl\_TS\_T40D2M20I0R0\include\CDD\_Mcl\_Ipw.h
- Mcl\_TS\_T40D2M20I0R0\include\CDD\_Mcl\_Irq.h
- Mcl\_TS\_T40D2M20I0R0\include\Dma\_Ip.h
- Mcl\_TS\_T40D2M20I0R0\include\Dma\_Ip\_Devassert.h
- Mcl\_TS\_T40D2M20I0R0\include\Dma\_Ip\_Hwv3\_Regs.h
- Mcl\_TS\_T40D2M20I0R0\include\Dma\_Ip\_Irq.h
- Mcl\_TS\_T40D2M20I0R0\include\Dma\_Ip\_Multicore.h
- Mcl\_TS\_T40D2M20I0R0\include\Dma\_Ip\_Types.h
- Mcl\_TS\_T40D2M20I0R0\include\Flexio\_Mcl\_Ip.h
- Mcl\_TS\_T40D2M20I0R0\include\Flexio\_Mcl\_Ip\_HwAccess.h

- Mcl\_TS\_T40D2M20I0R0\include\Flexio\_Mcl\_Ip\_Types.h
- Mcl\_TS\_T40D2M20I0R0\include\Mcl.h
- Mcl\_TS\_T40D2M20I0R0\include\Mcl\_Types.h
- Mcl\_TS\_T40D2M20I0R0\include\Trgmux\_Ip.h
- Mcl\_TS\_T40D2M20I0R0\include\Trgmux\_Ip\_Devassert.h
- Mcl\_TS\_T40D2M20I0R0\include\Trgmux\_Ip\_Types.h

### 3.2.0.0.2 MCL Driver Generated Files (must be generated by the user using a configuration tool):

- Cache\_Ip\_Cfg\_Defines.h
- Cache\_Ip\_Cfg\_DeviceRegisters.h
- CDD\_Mcl\_Cfg.h
- CDD\_Mcl\_Cfg\_Defines.h
- Dma\_Ip\_Cfg.h
- Dma\_Ip\_Cfg\_Defines.h
- Dma\_Ip\_Cfg\_DeviceRegistersV2.h
- Dma\_Ip\_Cfg\_Devices.h
- Flexio\_Mcl\_Ip\_Cfg.h
- Flexio\_Mcl\_Ip\_Cfg\_Defines.h
- Flexio\_Mcl\_Ip\_Cfg\_DeviceRegisters.h
- Trgmux\_Ip\_Cfg.h
- Trgmux\_Ip\_Cfg\_Defines.h
- Trgmux\_Ip\_Cfg\_DeviceRegisters.h
- CDD\_Mcl\_Cfg.c
- Dma\_Ip\_Cfg.c
- Trgmux\_Ip\_Cfg.c

#### Note

As a deviation from the standard:

- Mcl\_[VariantName]\_PBcfg.c, Dma\_Ip\_[VariantName]\_PBcfg.c - These files will contain the definition for all parameters that are variant aware, independent of the configuration class that will be selected (PC, LT, PB)
- Dma\_Ip\_Cfg.c - This file will contain the definition for all configuration structures containing only variables that are not variant aware, configured and generated only once. This file alone does not contain the whole structure needed by Mcl\_Init function to configure the driver. Based on the number of variants configured in the EcuC, there can be more than one configuration structure for one module even for VariantPreCompile.

### 3.2.0.0.3 Base Files:

- Base\_TS\_T40D2M20I0R0\include\Mcal.h
- Base\_TS\_T40D2M20I0R0\include\Platform\_Types.h
- Base\_TS\_T40D2M20I0R0\include\Soc\_Ips.h
- Base\_TS\_T40D2M20I0R0\include\Std\_Types.h
- Base\_TS\_T40D2M20I0R0\include\OsIf.h
- Base\_TS\_T40D2M20I0R0\generate\_PC\include\modules.h

### 3.2.0.0.4 DEM Files:

- Dem\_TS\_T40D2M20I0R0\include\Dem.h
- Dem\_TS\_T40D2M20I0R0\include\Dem\_Types.h
- Dem\_TS\_T40D2M20I0R0\generate\_PC\include\Dem\_IntErrId.h
- Dem\_TS\_T40D2M20I0R0\src\Dem.c

### 3.2.0.0.5 DET Files:

- Det\_TS\_T40D2M20I0R0\include\Det.h
- Det\_TS\_T40D2M20I0R0\src\Det.c

### 3.2.0.0.6 RTE Files:

- Rte\_TS\_T40D2M20I0R0\include\SchM\_Mcl.h
- Rte\_TS\_T40D2M20I0R0\src\SchM\_Mcl.c

## 3.3 Setting up the plugins

The MCL driver was designed to be configured by using the EB Tresos Studio (version EB tresos Studio 29.0.0 or later.)



## Chapter 4

### Function calls to module

- [Function Calls during Start-up](#)
- [Function Calls during Shutdown](#)
- [Function Calls during Wake-up](#)

#### 4.1 Function Calls during Start-up

None.

#### 4.2 Function Calls during Shutdown

None.

#### 4.3 Function Calls during Wake-up

None.

## Chapter 5

### Module requirements

- Exclusive areas to be defined in BSW scheduler
- Exclusive areas not available on this platform
- Peripheral Hardware Requirements
- ISR to configure within AutosarOS - dependencies
- ISR Macro
- Other AUTOSAR modules - dependencies
- Data Cache Restrictions
- User Mode support
- Multicore support

#### 5.1 Exclusive areas to be defined in BSW scheduler

In the current implementation, MCL is using the services of Schedule Manager (SchM) for entering and exiting the exclusive areas. The following critical regions are used in the MCL driver:

**Exclusive Areas are used in High level driver layer (HLD)**

**MCL\_EXCLUSIVE\_AREA\_00** is used in function `Mcl_Init` to protect the `DMA_MP_CSR` and `DMA_CRC_GEC` register from read/modify/write operation in `Dma_Ip_Init`.

**MCL\_EXCLUSIVE\_AREA\_01** is used in function `Mcl_DeInit` to protect the `DMA_MP_CSR` and `DMA_CRC_GEC` register from read/modify/write operation in `Dma_Ip_Deinit`.

**MCL\_EXCLUSIVE\_AREA\_02** is used in function `Mcl_SetDmaInstanceCommand` to protect `DMA_MP_CSR` register from read/modify/write operation in `Dma_Ip_SetLogicInstanceCommand`.

**MCL\_EXCLUSIVE\_AREA\_03** is used in function `Mcl_Init` to protect `DMA_CRC_CTL` register from read/modify/write operation in `Dma_Ip_LogicChannelInit`.

**MCL\_EXCLUSIVE\_AREA\_04** is used in function `Mcl_DeInit` to protect All TCDx\_WORDS, DMA\_MP↔\_CH\_GRPRI register from read/modify/write operation in `Dma_Ip_LogicChannelDeinit`.

**MCL\_EXCLUSIVE\_AREA\_05** is used in function `Mcl_SetDmaChannelCommand` to protect TCDx.8TH\_↔WORD register from read/modify/write operation in `Dma_Ip_SetLogicChannelCommand`.

**MCL\_EXCLUSIVE\_AREA\_06** is used in function `Mcl_GetDmaChannelStatus` to protect TCDx.8TH\_W↔ORD register from read/modify/write operation in `Dma_Ip_GetLogicChannelStatus`.

**MCL\_EXCLUSIVE\_AREA\_07** is used in function `Mcl_SetDmaChannelGlobalList` to protect DMA\_MP↔\_CH\_GRPRI and TCDx.8TH\_WORD register from read/modify/write operation in `Dma_Ip_SetLogicChannel↔GlobalList`.

**MCL\_EXCLUSIVE\_AREA\_08** is used in function `Mcl_SetDmaChannelGlobalList` to protect All TCDx\_↔WORDS register from read/modify/write operation in `Dma_Ip_SetLogicChannelGlobalList`.

**MCL\_EXCLUSIVE\_AREA\_09** is used in function `Mcl_SetDmaChannelScatterGatherList` to protect All T↔CDx\_WORDS register from read/modify/write operation in `Dma_Ip_SetLogicChannelScatterGatherList`.

**MCL\_EXCLUSIVE\_AREA\_10** is used in function `Mcl_SetDmaChannelScatterGatherList` to protect All T↔CDx\_WORDS register from read/modify/write operation in `Dma_Ip_SetLogicChannelScatterGatherList`.

**MCL\_EXCLUSIVE\_AREA\_11** is used in function `Mcl_SetDmaChannelScatterGatherConfig` to protect All TCDx\_WORDS register from read/modify/write operation in `Dma_Ip_SetLogicChannelScatterGatherConfig`.

**MCL\_EXCLUSIVE\_AREA\_12** is used in function `Mcl_Init` to protect All TCDx\_WORDS register from read/modify/write operation in `Static_Dma_Ip_SetLogicChannelScatterGatherInit`.

**MCL\_EXCLUSIVE\_AREA\_13** is used in function `Mcl_CacheEnable` to protect S32\_SCB\_CCR register from read/modify/write operation in `Cache_Ip_Enable`.

**MCL\_EXCLUSIVE\_AREA\_14** is used in function `Mcl_CacheDisable` to protect S32\_SCB\_CCR register from read/modify/write operation in `Cache_Ip_Disable`.

**MCL\_EXCLUSIVE\_AREA\_15** is used in function `Mcl_CacheInvalidate` to protect S32\_SCB\_CSSELR and S32\_SCB\_ICIALLU register from read/modify/write operation in `Cache_Ip_Invalidate`.

**MCL\_EXCLUSIVE\_AREA\_16** is used in function `Mcl_CacheClean` to protect S32\_SCB\_CSSELR and S32↔\_SCB\_ICIALLU register from read/modify/write operation in `Cache_Ip_Clean`.

**MCL\_EXCLUSIVE\_AREA\_17** is used in function `Mcl_CacheInvalidateByAddr` to protect S32\_SCB\_CSS↔ELR and S32\_SCB\_ICIMVAU register from read/modify/write operation in `Cache_Ip_InvalidateByAddr`.

**MCL\_EXCLUSIVE\_AREA\_18** is used in function `Mcl_CacheCleanByAddr` to protect S32\_SCB\_CSSELR and S32\_SCB\_ICIMVAU register from read/modify/write operation in `Cache_Ip_CleanByAddr`.

**MCL\_EXCLUSIVE\_AREA\_19** is used in function `Mcl_Init` to protect TRGMUXn register from read/modify/write operation in `Trgmux_Ip_Init`.

**MCL\_EXCLUSIVE\_AREA\_20** is used in function `Mcl_SetTrgMuxInput` to protect TRGMUXn register from read/modify/write operation in `Trgmux_Ip_SetInput`.

**MCL\_EXCLUSIVE\_AREA\_21** is used in function `Mcl_SetTrgMuxLock` to protect TRGMUXn register from read/modify/write operation in `Trgmux_Ip_SetLock`.

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**MCL\_EXCLUSIVE\_AREA\_39** is used in function `Mcl_Init` to protect CTRL register from read/modify/write operation in `Flexio_Mcl_Ip_InitDevice`.

**MCL\_EXCLUSIVE\_AREA\_40** is used in function `Mcl_Init` to protect CTRL register from read/modify/write operation in `Flexio_Mcl_Ip_InitDevice`.

**MCL\_EXCLUSIVE\_AREA\_41** is used in function `Mcl_Init` to protect CTRL register from read/modify/write operation in `Flexio_Mcl_Ip_InitDevice`.

**MCL\_EXCLUSIVE\_AREA\_42** is used in function `Mcl_Init` to protect SHIFTEIEN register from read/modify/write operation in `Flexio_Mcl_Ip_InitDevice`.

**MCL\_EXCLUSIVE\_AREA\_43** is used in function `Mcl_Init` to protect SHIFTSIEN register from read/modify/write operation in `Flexio_Mcl_Ip_InitDevice`.

**MCL\_EXCLUSIVE\_AREA\_44** is used in function `Mcl_Init` to protect SHIFTSDEN register from read/modify/write operation in `Flexio_Mcl_Ip_InitDevice`.

**MCL\_EXCLUSIVE\_AREA\_45** is used in function `Mcl_Init` to protect TIMIEN register from read/modify/write operation in `Flexio_Mcl_Ip_InitDevice`.

**MCL\_EXCLUSIVE\_AREA\_46** is used in function `Mcl_Init` to protect TIMERSDEN register from read/modify/write operation in `Flexio_Mcl_Ip_InitDevice`.

### Exclusive Areas implemented in Low level driver layer (IPL)

**MCL\_EXCLUSIVE\_AREA\_00** is used in function `Dma_Ip_Init()` to protect the updates for:

- DMA\_MP\_CSR
- DMA\_CRC\_GEC

**MCL\_EXCLUSIVE\_AREA\_01** is used in function `Dma_Ip_Deinit()` to protect the updates for:

- DMA\_MP\_CSR
- DMA\_CRC\_GEC

**MCL\_EXCLUSIVE\_AREA\_02** is used in function `Dma_Ip_SetLogicInstanceCommand()` to protect the updates for:

- DMA\_MP\_CSR

**MCL\_EXCLUSIVE\_AREA\_03** is used in function `Dma_Ip_LogicChannelInit()` to protect the updates for:

- DMA\_CRC\_CTL

**MCL\_EXCLUSIVE\_AREA\_04** is used in function `Dma_Ip_LogicChannelDeinit()` to protect the updates for:



- All TCDx\_WORDS
- DMA\_MP\_CH\_GRPRI

**MCL\_EXCLUSIVE\_AREA\_05** is used in function `Dma_Ip_SetLogicChannelCommand()` to protect the updates for:

- TCDx.8TH\_WORD

**MCL\_EXCLUSIVE\_AREA\_06** is used in function `Dma_Ip_GetLogicChannelStatus()` to protect the updates for:

- TCDx.8TH\_WORD

**MCL\_EXCLUSIVE\_AREA\_07** is used in function `Dma_Ip_SetLogicChannelGlobalList()` to protect the updates for:

- DMA\_MP\_CH\_GRPRI
- TCDx.8TH\_WORD

**MCL\_EXCLUSIVE\_AREA\_08** is used in function `Dma_Ip_SetLogicChannelTransferList()` to protect the updates for:

- All TCDx\_WORDS

**MCL\_EXCLUSIVE\_AREA\_09** is used in function `Dma_Ip_SetLogicChannelScatterGatherList()` to protect the updates for:

- All TCDx\_WORDS

**MCL\_EXCLUSIVE\_AREA\_10** is used in function `Dma_Ip_SetLogicChannelCrcList()` to protect the updates for:

- DMA\_CRC\_CTL
- DMA\_CRC\_ICRC

**MCL\_EXCLUSIVE\_AREA\_11** is used in function `Dma_Ip_SetLogicChannelScatterGatherConfig()` to protect the updates for:

- All TCDx\_WORDS

**MCL\_EXCLUSIVE\_AREA\_12** is used in function `Static_Dma_Ip_SetLogicChannelScatterGatherInit()` to protect the updates for:

## Module requirements

- All TCDx\_WORDS

**MCL\_EXCLUSIVE\_AREA\_13** is used in function `Cache_Ip_Enable()` to protect the updates for:

- S32\_SCB\_CCR

**MCL\_EXCLUSIVE\_AREA\_14** is used in function `Cache_Ip_Disable()` to protect the updates for:

- S32\_SCB\_CCR

**MCL\_EXCLUSIVE\_AREA\_15** is used in function `Cache_Ip_Invalidate()` to protect the updates for:

- S32\_SCB\_CSSELR
- S32\_SCB\_ICIALLU

**MCL\_EXCLUSIVE\_AREA\_16** is used in function `Cache_Ip_Clean()` to protect the updates for:

- S32\_SCB\_CSSELR
- S32\_SCB\_ICIALLU

**MCL\_EXCLUSIVE\_AREA\_17** is used in function `Cache_Ip_InvalidateByAddr()` to protect the updates for:

- S32\_SCB\_CSSELR
- S32\_SCB\_ICIMVAU

**MCL\_EXCLUSIVE\_AREA\_18** is used in function `Cache_Ip_CleanByAddr()` to protect the updates for:

- S32\_SCB\_CSSELR
- S32\_SCB\_ICIMVAU

**MCL\_EXCLUSIVE\_AREA\_19** is used in function `Trgmux_Ip_Init()` to protect the updates for:

- TRGMUXn

**MCL\_EXCLUSIVE\_AREA\_20** is used in function `Trgmux_Ip_SetInput()` to protect the updates for:

- TRGMUXn

**MCL\_EXCLUSIVE\_AREA\_21** is used in function `Trgmux_Ip_SetLock()` to protect the updates for:

- TRGMUXn

**MCL\_EXCLUSIVE\_AREA\_39** is used in function `Flexio_Mcl_Ip_SetSoftwareReset()` to protect the updates for:

- CTRL

**MCL\_EXCLUSIVE\_AREA\_40** is used in function `Flexio_Mcl_Ip_SetDebugEnabled()` to protect the updates for:

- CTRL

**MCL\_EXCLUSIVE\_AREA\_41** is used in function `Flexio_Mcl_Ip_SetEnable()` to protect the updates for:

- CTRL

**MCL\_EXCLUSIVE\_AREA\_42** is used in function `Flexio_Mcl_Ip_SetShifterErrorInterrupt()` to protect the updates for:

- SHIFTEIEN

**MCL\_EXCLUSIVE\_AREA\_43** is used in function `Flexio_Mcl_Ip_SetShifterInterrupt()` to protect the updates for:

- SHIFTSIEN

**MCL\_EXCLUSIVE\_AREA\_44** is used in function `Flexio_Mcl_Ip_SetShifterDMARequest()` to protect the updates for:

- SHIFTSDEN

**MCL\_EXCLUSIVE\_AREA\_45** is used in function `Flexio_Mcl_Ip_SetTimerInterrupt()` to protect the updates for:

- TIMIEN

**MCL\_EXCLUSIVE\_AREA\_46** is used in function `Flexio_Mcl_Ip_SetTimerDMARequest()` to protect the updates for:

- IMERSDEN

Table 5.1 Exclusive Areas

#	A R E A _00	A R E A _01	A R E A _02	A R E A _03	A R E A _04	A R E A _05	A R E A _06	A R E A _07	A R E A _08	A R E A _09	A R E A _10	A R E A _11	A R E A _12	A R E A _13	A R E A _14	A R E A _15	A R E A _16	A R E A _17	A R E A _18	A R E A _19	A R E A _20	A R E A _21	A R E A _39	A R E A _40	A R E A _41	A R E A _42	A R E A _43	A R E A _44	A R E A _45	A R E A _46
A R E A _00	x	x																												
A R E A _01	x	x																												
A R E A _02	x	x																												
A R E A _03			x						x																					
A R E A _04				x	x		x	x	x		x	x																		
A R E A _05				x	x		x	x	x		x	x																		
A R E A _06				x	x		x	x	x		x	x																		

#	A R E A  00	A R E A  01	A R E A  02	A R E A  03	A R E A  04	A R E A  05	A R E A  06	A R E A  07	A R E A  08	A R E A  09	A R E A  10	A R E A  11	A R E A  12	A R E A  13	A R E A  14	A R E A  15	A R E A  16	A R E A  17	A R E A  18	A R E A  19	A R E A  20	A R E A  21	A R E A  39	A R E A  40	A R E A  41	A R E A  42	A R E A  43	A R E A  44	A R E A  45	A R E A  46	
A R E A  07				x	x		x	x	x		x	x																			
A R E A  08			x							x																					
A R E A  09				x	x		x	x	x		x	x																			
A R E A  10				x	x		x	x	x		x	x																			
A R E A  11																															
A R E A  12																															
A R E A  13																															

## Module requirements

#	A R E A — 00	A R E A — 01	A R E A — 02	A R E A — 03	A R E A — 04	A R E A — 05	A R E A — 06	A R E A — 07	A R E A — 08	A R E A — 09	A R E A — 10	A R E A — 11	A R E A — 12	A R E A — 13	A R E A — 14	A R E A — 15	A R E A — 16	A R E A — 17	A R E A — 18	A R E A — 19	A R E A — 20	A R E A — 21	A R E A — 39	A R E A — 40	A R E A — 41	A R E A — 42	A R E A — 43	A R E A — 44	A R E A — 45	A R E A — 46	
A R E A — 14																															
A R E A — 15																															
A R E A — 16																															
A R E A — 17																															
A R E A — 18																															
A R E A — 19																				x	x	x									
A R E A — 20																				x	x	x									

#	A R E A  — 00	A R E A  — 01	A R E A  — 02	A R E A  — 03	A R E A  — 04	A R E A  — 05	A R E A  — 06	A R E A  — 07	A R E A  — 08	A R E A  — 09	A R E A  — 10	A R E A  — 11	A R E A  — 12	A R E A  — 13	A R E A  — 14	A R E A  — 15	A R E A  — 16	A R E A  — 17	A R E A  — 18	A R E A  — 19	A R E A  — 20	A R E A  — 21	A R E A  — 39	A R E A  — 40	A R E A  — 41	A R E A  — 42	A R E A  — 43	A R E A  — 44	A R E A  — 45	A R E A  — 46	
A R E A  — 21																				x	x	x									
A R E A  — 39																							x	x	x						
A R E A  — 40																							x	x	x						
A R E A  — 41																							x	x	x						
A R E A  — 42																										x					
A R E A  — 43																												x			
A R E A  — 44																													x		

Module requirements

#	A R E A  00	A R E A  01	A R E A  02	A R E A  03	A R E A  04	A R E A  05	A R E A  06	A R E A  07	A R E A  08	A R E A  09	A R E A  10	A R E A  11	A R E A  12	A R E A  13	A R E A  14	A R E A  15	A R E A  16	A R E A  17	A R E A  18	A R E A  19	A R E A  20	A R E A  21	A R E A  39	A R E A  40	A R E A  41	A R E A  42	A R E A  43	A R E A  44	A R E A  45	A R E A  46	
A R E A  45																														X	
A R E A  46																															X

5.2 Exclusive areas not available on this platform

None.

5.3 Peripheral Hardware Requirements

None.

5.4 ISR to configure within AutosarOS - dependencies

The following ISRs are used by the Mcl Driver when interrupts are switched on (the driver can also be run in polling mode):

ISR Name	NVIC Interrupt ID
DMA0_IRQn	0
DMA1_IRQn	1
DMA2_IRQn	2
DMA3_IRQn	3
DMA4_IRQn	4
DMA5_IRQn	5
DMA6_IRQn	6



ISR Name	NVIC Interrupt ID
DMA7_IRQn	7
DMA8_IRQn	8
DMA9_IRQn	9
DMA10_IRQn	10
DMA11_IRQn	11
DMA12_IRQn	12
DMA13_IRQn	13
DMA14_IRQn	14
DMA15_IRQn	15
DMA_Error_IRQn	16

## 5.5 ISR Macro

RTD drivers use the ISR macro to define the functions that will process hardware interrupts. Depending on whether the OS is used or not, this macro can have different definitions.

**5.5.1 Without an Operating System** The macro *USING\_OS\_AUTOSAROS* must not be defined.

### 5.5.1.1 Using Software Vector Mode

The macro *USE\_SW\_VECTOR\_MODE* must be defined and the ISR macro is defined as:

```
#define ISR(IsrName) void IsrName(void)
```

In this case, the drivers' interrupt handlers are normal C functions and their prologue/epilogue will handle the context save and restore.

### 5.5.1.2 Using Hardware Vector Mode

The macro *USE\_SW\_VECTOR\_MODE* must not be defined and the ISR macro is defined as:

```
#define ISR(IsrName) INTERRUPT_FUNC void IsrName(void)
```

In this case, the drivers' interrupt handlers must also handle the context save and restore.

**5.5.2 With an Operating System** Please refer to your OS documentation for description of the ISR macro.

## 5.6 Other AUTOSAR modules - dependencies

- Mcu: The Microcontroller Unit Driver (MCU Driver) is primarily responsible for initializing and controlling the chips internal clock sources and clock prescalers. The clock frequency may affect the Trigger frequency, Conversion time and Sampling time.
- Det: If development error detection for the MCL module is enabled: The MCL module shall raise errors to the Development Error Tracer (DET) whenever a development error is encountered by this module.
- Base: The Base module contains the common files/definitions needed by all RTD modules.
- Resource: is required to select processor derivative. Current MCL driver has support for the following derivatives, everyone having attached a Resource file: s32g233a\_bga525, s32g234m\_bga525, s32g254a\_bga525, s32g274a\_bga525, s32r45\_bga780.
- Rte: Used to manage the exclusive area inside MCL module.
- EcuC: This module is required for configuring the variant handling in Tresos.
- Os: This module is required for configuring the Partition mapping with core ID in Tresos.
- Plarform: This module is required for configuring the Interrupt controller in Tresos.

## 5.7 Data Cache Restrictions

In the DMA transfer mode, DMA transfers may issue cache coherency problems. To avoid possible coherency issues when D-CACHE is enabled, the user shall ensure that the buffers used as TCD source and destination are allocated in the NON-CACHEABLE area (by means of MCL\_Memmap).

## 5.8 User Mode support

- [User Mode configuration in the module](#)
- [User Mode configuration in AutosarOS](#)

**5.8.1 User Mode configuration in the module** The Mcl can be run in user mode if the following steps are performed:

- Enable **MclEnableUserModeSupport** from the configuration
- Call the following functions as trusted functions:

Function syntax	Description	Available via
void Mcl_Dma_SetUserAccessAllowed(void)	For seting the user access allowed for DMA registers protected by REG_PROT	Dma_Ip_TrustedFunctions.h
LOCAL_INLINE Std_ReturnType hwAcc_Lmem_ProcessorCodeCacheEnable(void)	Enable Instruction Cache	

Function syntax	Description	Available via
LOCAL_INLINE Std_ReturnType hwAcc_Lmem_ProcessorCode↔ CacheDisable(void)	Disable Instruction Cache	
LOCAL_INLINE Std_ReturnType hwAcc_Lmem_ProcessorCode↔ Invalidate(void)	Invalidate Instruction Cache	
LOCAL_INLINE Std_ReturnType hwAcc_Lmem_ProcessorCode↔ Clean(const boolean enInvalidate)	Clean Instruction Cache	
LOCAL_INLINE Std_ReturnType hwAcc_Lmem_ProcessorCode↔ InvalidateByAddr(const uint32 addr, const uint32 length)	Invalidate Instruction Cache By Address	
LOCAL_INLINE Std_ReturnType hwAcc_Lmem_ProcessorCode↔ CacheCleanByAddr(const boolean enInvalidate, const uint32 addr, const uint32 length)	Clean Instruction Cache By Address	
Trgmux_Ip_StatusType hwAcc_↔ Init(TRGMUX_Type * const p↔ Trgmux)	Initialize the Trgmux	Trgmux_Ip_TrustedFunctions.h
void hwAcc_SetInputForOutput(↔ TRGMUX_Type * const pTrgmux, const uint32 Input, const uint32 Output)	Mapping the Input for the Output	
void hwAcc_SetLockForOutput(↔ TRGMUX_Type * const pTrgmux, const uint32 Output)	Lock the Output	
boolean hwAcc_GetLockFor↔ Output(const TRGMUX_Type * const pTrgmux, const uint32 Output)	Get Lock status for the Output	
void Ftm_Mcl_Ip_SetUser↔ AccessAllowed(void)	For seting the user access allowed for FTM registers protected by REG↔ _PROT	Ftm_Ip_TrustedFunctions.h

Note: All of Cache functions are static inline function to avoid using stack. Because cache will work incorrectly when using stack. If user want to use cache with stack, the stack have to be pushed into non-cache memory section. When Using GCC or diab compiler the integrator must ensure that the Cache APIs are properly inlined (forced inline).

### 5.8.2 User Mode configuration in AutosarOS

When User mode is enabled, the driver may have the functions that need to be called as trusted functions in AutosarOS context. Those functions are already defined in driver and declared in the header <IpName>\_Ip↔\_TrustedFunctions.h. This header also included all headers files that contains all types definition used by parameters or return types of those functions. Refer the chapter [User Mode configuration in the module](#) for more detail about those functions and the name of header files they are declared inside. Those functions will be called indirectly with the naming convention below in order to AutosarOS can call them as trusted functions.

## Module requirements

`Call_<Function_Name>_TRUSTED(parameter1,parameter2,...)`

That is the result of macro expansion `OsIf_Trusted_Call` in driver code:

```
#define OsIf_Trusted_Call[1-6params](name,param1,...,param6) Call_##name##_TRUSTED(param1,...,param6)
```

So, the following steps need to be done in AutosarOS:

- Ensure `MCAL_ENABLE_USER_MODE_SUPPORT` macro is defined in the build system or somewhere global.
- Define and declare all functions that need to call as trusted functions follow the naming convention above in Integration/User code. They need to be visible in `Os.h` for the driver to call them. They will do the marshalling of the parameters and call `CallTrustedFunction()` in OS specific manner.
- `CallTrustedFunction()` will switch to privileged mode and call `TRUSTED_<Function_Name>()`.
- `TRUSTED_<Function_Name>()` function is also defined and declared in Integration/User code. It will un-marshalling of the parameters to call `<Function_Name>()` of driver. The `<Function_Name>()` functions are already defined in driver and declared in `<IpName>_Ip_TrustedFunctions.h`. This header should be included in OS for OS call and indexing these functions.

See the sequence chart below for an example calling `Linflexd_Uart_Ip_Init_Privileged()` as a trusted function.

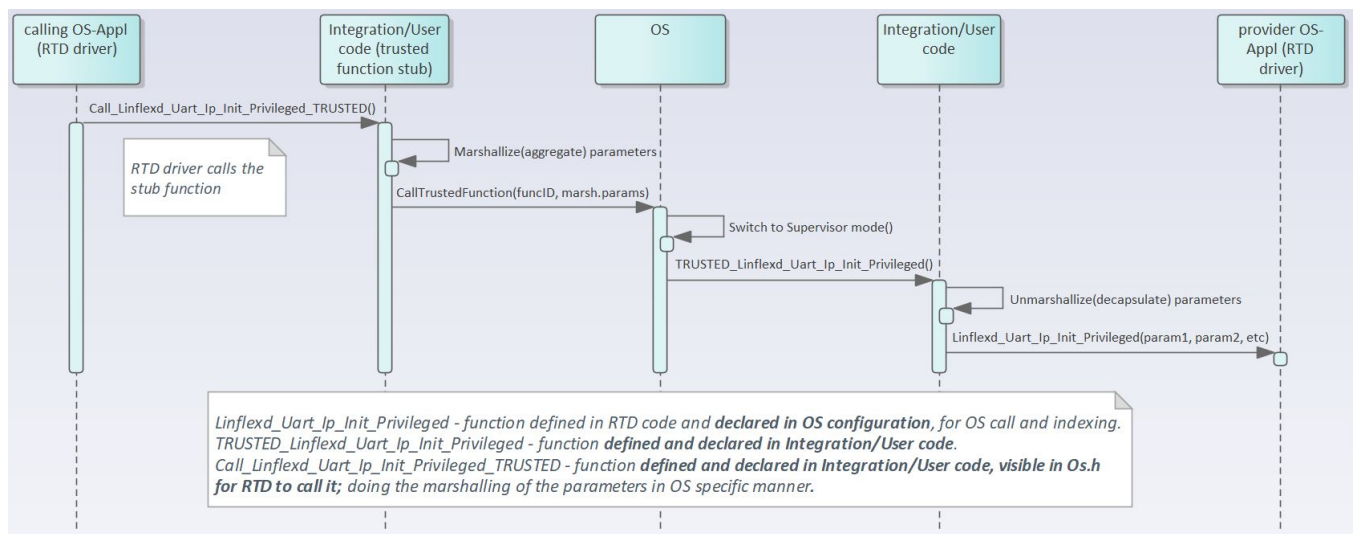


Figure 5.1 Example sequence chart for calling `Linflexd_Uart_Ip_Init_Privileged` as trusted function

## 5.9 Multicore support

The Mcl Driver does not support Multicore for S32K1\_S32M24X.

## Chapter 6

### Main API Requirements

- [Main function calls within BSW scheduler](#)
- [API Requirements](#)
- [Calls to Notification Functions, Callbacks, Callouts](#)

#### 6.1 Main function calls within BSW scheduler

None.

#### 6.2 API Requirements

API: “void Mcl\_SetDmaInstanceCommand(const uint32 Instance, const Mcl\_DmaInstanceCmdType Command)”

The Dma Instance Command is used to trigger a specific action by the DMA Engine. The command is specific and it shall be selected from the “Mcl\_DmaInstanceCmdType” enumeration. Example: If the user desires to pause a specific Logic Instance during runtime, the “Mcl\_DmaInst\_Pause” command shall be used.

API: “void Mcl\_GetDmaInstanceStatus(const uint32 Instance, Mcl\_DmaInstanceStatusType \* const Status)”

The Dma Instance Status is used to get the specific status of the DMA Engine. The status contains hardware information for the selected Logic Instance.

API: “void Mcl\_SetDmaChannelCommand(const uint32 Channel, const Mcl\_DmaChannelCmdType Command)”

The Dma Channel Command is used to trigger a specific action by the DMA Engine regarding the configured TCD. The command is specific and it shall be selected from the “Mcl\_DmaChannelCmdType” enumeration. Example: If the user desires to start the reception of a specific hardware signal, that triggers the Logic Channel, during runtime, the “Mcl\_DmaCh\_StartRequest” command shall be used.

API: “void Mcl\_GetDmaChannelStatus(const uint32 Channel, Mcl\_DmaChannelStatusType \* const Status)”

The Dma Instance Status is used to get the specific status of the DMA TCD. The status contains hardware information for the selected Logic Channel.

## Main API Requirements

API: “Mcl\_SetDmaChannelGlobalList(const uint32 Channel, const Mcl\_DmaChannelGlobalListType List[], const uint32 ListDimension)”

The Dma Channel can be configured during runtime, in case that the generated configuration by Tresos does not cover all the use cases. The Global List configuration configures Logic Channel values, like: Global Control Settings, Request Settings, Interrupt Settings and Priority Settings. The user shall create Global Configuration Lists (“↵ Mcl\_DmaChannelGlobalListType”) based on the required configuration. EXAMPLE: The user needs to configure the Logic Channel Global Configuration Parameters: “Mcl\_DmaSetRequest\_MuxSource”, “Mcl\_DmaSetRequest↵\_EnMuxSource”, “Mcl\_DmaSetPriority\_Level” and “Mcl\_DmaSetPriority\_EnPreemption”.

The order shall be:

Step0: Disable the Mux Source.

Step1: Change the Mux Source Value.

Step2: Change the Priority Level Value.

Step3: Enable the Preemption.

Step4: Enable the Mux Source.

CODE:

```
#define DMA_DSPI0_TX_GLOBAL_CFG0 ((uint32)5U)
```

```
Mcl_DmaChannelGlobalListType DmaChannelSpiTxGlobalCfg0[DMA_DSPI0_TX_GLOBAL_CFG0];
```

```
DmaChannelSpiTxGlobalCfg0[0U].Param = Mcl_DmaSetRequest_EnMuxSource;
```

```
DmaChannelSpiTxGlobalCfg0[0U].Value = FALSE;
```

```
DmaChannelSpiTxGlobalCfg0[1U].Param = Mcl_DmaSetRequest_MuxSource;
```

```
DmaChannelSpiTxGlobalCfg0[1U].Value = DMA_IP_REQ_MUX0_DSPI0_TX;
```

```
DmaChannelSpiTxGlobalCfg0[2U].Param = Mcl_DmaSetPriority_Level;
```

```
DmaChannelSpiTxGlobalCfg0[2U].Value = DMA_IP_LEVEL_PRIO0;
```

```
DmaChannelSpiTxGlobalCfg0[3U].Param = Mcl_DmaSetPriority_EnPreemption;
```

```
DmaChannelSpiTxGlobalCfg0[3U].Value = TRUE;
```

```
DmaChannelSpiTxGlobalCfg0[4U].Param = Mcl_DmaSetRequest_EnMuxSource;
```

```
DmaChannelSpiTxGlobalCfg0[4U].Value = TRUE;
```

```
Mcl_SetDmaChannelGlobalList(CHANNEL_DSPI0_TX, &DmaChannelSpiTxGlobalCfg0[0U], DMA_DSPI0_TX_GLOBAL_
```

API: “void Mcl\_SetDmaChannelTransferList(const uint32 Channel, const Mcl\_DmaChannelTransferListType List[], const uint32 ListDimension)”

The Dma Channel can be configured during runtime, in case that the generated configuration by Tresos does not cover all the use cases. The Transfer List configuration configures Logic Channel Hardware TCD values, like Transfer Control Settings, Source Settings, Destination Settings, MinorLoop Settings and MajorLoop Settings. The user shall create Transfer Configuration Lists ("Mcl\_DmaChannelTransferListType") based on the required configuration. The Transfer Configuration List shall automatically change the Logic Channel configuration from Scatter/Gather Mode to Transfer Mode. EXAMPLE: The user needs to configure the Logic Channel Transfer Configuration Parameters: "Mcl\_DmaSetSource\_Address", "Mcl\_DmaSetSource\_SignedOffset", "Mcl\_DmaSetSource\_TransferSize", "Mcl\_DmaSetDestination\_Address", "Mcl\_DmaSetDestination\_SignedOffset", "Mcl\_DmaSetDestination\_TransferSize", "Mcl\_DmaSetMinorLoop\_Size", "Mcl\_DmaSetMajorLoop\_Count", "Mcl\_DmaSetControl\_BandwidthControl".

The order shall be:

Step0: Change the Source Address Value.

Step1: Change the Source Signed Offset Value.

Step2: Change the Source Transfer Size Value.

Step3: Change the Destination Address Value.

Step4: Change the Destination Signed Offset Value.

Step5: Change the Destination Transfer Size Value.

Step6: Change the Minor Loop Size Value.

Step7: Change the Major Loop Count Value.

Step8: Change the Bandwidth Value.

CODE:

```
#define DMA_DSPIO_TX_TRANSFER_CFG0 ((uint32)9U)

Mcl_DmaChannelTransferListType DmaChannelSpiTxTransferCfg0[DMA_DSPIO_TX_TRANSFER_CFG0];

DmaChannelSpiTxTransferCfg0[0U].Param = Mcl_DmaSetSource_Address;

DmaChannelSpiTxTransferCfg0[0U].Value = &SpiTx_Buffer0;

DmaChannelSpiTxTransferCfg0[1U].Param = Mcl_DmaSetSource_SignedOffset;

DmaChannelSpiTxTransferCfg0[1U].Value = 4U;

DmaChannelSpiTxTransferCfg0[2U].Param = Mcl_DmaSetSource_TransferSize;

DmaChannelSpiTxTransferCfg0[2U].Value = DMA_IP_TRANSFER_SIZE_2_BYTE;

DmaChannelSpiTxTransferCfg0[3U].Param = Mcl_DmaSetDestination_Address;

DmaChannelSpiTxTransferCfg0[3U].Value = &SPI_TX_REG;

DmaChannelSpiTxTransferCfg0[4U].Param = Mcl_DmaSetDestination_SignedOffset;
```

## Main API Requirements

```
DmaChannelSpiTxTransferCfg0[4U].Value = 0U;
```

```
DmaChannelSpiTxTransferCfg0[5U].Param = Mcl_DmaSetDestination_TransferSize;
```

```
DmaChannelSpiTxTransferCfg0[5U].Value = DMA_IP_TRANSFER_SIZE_2_BYTE;
```

```
DmaChannelSpiTxTransferCfg0[6U].Param = Mcl_DmaSetMinorLoop_Size;
```

```
DmaChannelSpiTxTransferCfg0[6U].Value = 2U;
```

```
DmaChannelSpiTxTransferCfg0[7U].Param = Mcl_DmaSetMajorLoop_Count;
```

```
DmaChannelSpiTxTransferCfg0[7U].Value = 8U;
```

```
DmaChannelSpiTxTransferCfg0[8U].Param = Mcl_DmaSetControl_BandwidthControl;
```

```
DmaChannelSpiTxTransferCfg0[8U].Value = DMA_IP_BWC_ENGINE_NO_STALL;
```

```
Mcl_SetDmaChannelTransferList(CHANNEL_DSPIO_TX, &DmaChannelSpiTxTransferCfg0[0U], DMA_DSPIO_TX_TRANS
```

API: “void Mcl\_SetDmaChannelScatterGatherList(const uint32 Channel, const uint32 Element, const Mcl\_Dma↵  
ChannelScatterGatherListType List[], const uint32 ListDimension);”

The Dma Channel can be configured during runtime, in case that the generated configuration by Tresos does not cover all the use cases. The Scatter Gather List configures Logic Channel Software TCD values, like: Transfer Control Settings, Source Settings, Destination Settings, MinorLoop Settings and MajorLoop Settings. The user shall create ScatterGather Configuration Lists (“Mcl\_DmaChannelScatterGatherListType”) based on the required configuration. The “Element” is the Handler(Tag) generated by Tresos and identifies a Software TCD for the Logic Channel.

API: “void Mcl\_GetDmaChannelParam(const uint32 Channel, const Mcl\_DmaChannelInfoParameterType Param, uint32 \* const Value);”

The Dma Channel can return parameter information during runtime. The user selects the parameter from “Mcl\_↵  
DmaChannelInfoParameterType” enumeration. The value of the parameter shall be returned in the Value variable.

API: “void Mcl\_SetDmaChannelScatterGatherConfig(const uint32 Channel, const uint32 Element);”

The Dma Channel can be configured during runtime, in case that the generated configuration by Tresos does not cover all the use cases. The Scatter Gather Configuration loads the selected Element for the Logic Channel into the Hardware TCD. The Element is internally configured to run in ScatterGather Mode.

## 6.3 Calls to Notification Functions, Callbacks, Callouts

calls to notification functions callbacks callouts template.



## Chapter 7

### Memory allocation

- [Sections to be defined in MCL\\_MemMap.h](#)
- [Linker command file](#)

#### 7.1 Sections to be defined in MCL\_MemMap.h

Section name	Type of section	Description
MCL_START_SEC_CODE	Code	Start of memory Section for Code
MCL_STOP_SEC_CODE	Code	End of memory Section for Code
MCL_START_SEC_CONFIG_DATA↔ _UNSPECIFIED	Configuration Data	Start of Memory Section for Config Data
MCL_STOP_SEC_CONFIG_DATA↔ UNSPECIFIED	Configuration Data	End of Memory Section for Config Data
MCL_START_SEC_CONFIG_DATA↔ _UNSPECIFIED_NO_CACHEABLE	Configuration Data	Start of Memory Section for Config Data (no cacheable).
MCL_STOP_SEC_CONFIG_DATA↔ UNSPECIFIED_NO_CACHEABLE	Configuration Data	End of Memory Section for Config Data (no cacheable).
MCL_START_SEC_VAR_CLEARED↔ _UNSPECIFIED	Variables	Used for variables, structures, arrays when the SIZE (alignment) does not fit the criteria of 8,16 or 32 bit. These variables are cleared to zero by start-up code.
MCL_STOP_SEC_VAR_CLEARED↔ UNSPECIFIED	Variables	End of above section.
MCL_START_SEC_VAR_INIT_UNSP↔ PECIFIED	Variables	Used for variables, structures, arrays, when the SIZE (alignment) does not fit the criterion of 8,16 or 32 bit. These variables are initialized with values after every reset.
MCL_STOP_SEC_VAR_INIT_UNSP↔ ECIFIED	Variables	End of above section.
MCL_START_SEC_VAR_CLEARED↔ _UNSPECIFIED_NO_CACHEABLE	Variables	Used for variables, structures, arrays when the SIZE (alignment) does not fit the criteria of 8,16 or 32 bit. These variables are cleared to zero by start-up code (no cacheable)
MCL_STOP_SEC_VAR_CLEARED↔ UNSPECIFIED_NO_CACHEABLE	Variables	End of above section.

## 7.2 Linker command file

Memory shall be allocated for every section defined in the driver's "<Module>\_MemMap.h".

## Chapter 8

### Integration Steps

This section gives a brief overview of the steps needed for integrating this module:

1. Generate the required module configuration(s). For more details refer to section [Files Required for Compilation](#)
2. Allocate the proper memory sections in the driver's memory map header file ("`<Module>_MemMap.h`") and linker command file. For more details refer to section [Sections to be defined in `<Module>\_MemMap.h`](#)
3. Compile & build the module with all the dependent modules. For more details refer to section [Building the Driver](#)

## Chapter 9

### External assumptions for driver

The section presents requirements that must be complied with when integrating the MCL driver into the application.

External Assumption Req ID	External Assumption Text
EA_RTD_00071	If interrupts are locked, a centralized function pair to lock and unlock interrupts shall be used.
EA_RTD_00081	The integrator shall assure that <MSN>_Init() and <MSN>_DeInit() functions do not interrupt each other.
EA_RTD_00082	When caches are enabled and data buffers are allocated in cacheable memory regions the buffers involved in DMA transfer shall be aligned with both start and end to cache line size. Note: <b>Rationale:</b> This ensures that no other buffers/variables compete for the same cache lines.
EA_RTD_00106	Standalone IP configuration and HL configuration of the same driver shall be done in the same project
EA_RTD_00107	The integrator shall use the IP interface only for hardware resources that were configured for standalone IP usage. Note: The integrator shall not directly use the IP interface for hardware resources that were allocated to be used in HL context.
EA_RTD_00108	The integrator shall use the IP interface to build a CDD, therefore the BSWMD will not contain reference to the IP interface
EA_RTD_00113	When RTD drivers are integrated with AutosarOS and User mode support is enabled, the integrator shall assure that the definition and declaration of all RTD functions needed to be called as trusted functions follow the naming convention Call<Function_Name>TRUSTED(parameter1,parameter2,...) in Integration/User code. They need to be visible in Os.h for the driver to call them. They will call RTD <Function_Name>() as trusted functions in OS specific manner.

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