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**ACCURATE, FULL-SYSTEM, THERMAL CHARACTERIZATION
OF SEMICONDUCTOR DEVICES**

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Joseph Nayfach - Battilana

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The Thesis of Joseph Nayfach - Battilana
is approved:

Professor Jose Renau, Chair

Professor Cyrus Bazeghi

Professor Andrea Di Blas

Lisa C. Sloan
Vice Provost and Dean of Graduate Studies

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Abstract

Accurate, Full-System, Thermal Characterization of Semiconductor Devices

by

Joseph Nayfach - Battilana

Here we present a novel temperature modeling infrastructure that offers engineers a new way to explore solutions to a growing array of engineering problems that require accurate thermal characterization of semiconductor devices. A particular benefit of such a thermal modeling infrastructure is that engineers are given the requisite tools needed to expose and solve potentially costly thermal runaway problems sufficiently early in the design cycle so as to reduce the risk that an otherwise viable design exceeds its thermal budget, necessitating a costly redesign and possibly rendering the design ultimately inviable. The modeling framework, called Sesctherm, is a state-of-the-art finite-element-based thermal modeling system. The framework has been verified against transient, empirical data collected using a Delphi thermal test chip and Flomerics FlothermTM thermal simulator. Further, we present the first comprehensive evaluation to determine the importance of accurate thermal characterization of several aspects of a given chip design on the overall accuracy of the thermal model. This includes an evaluation of the importance for accurate modeling of metal interconnect layers, detailed modeling of bulk-silicon technology or silicon-on-insulator device modeling, accurate package modeling, accurate printed-wiring-board modeling, and accurate forced convection flow modeling.

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Part I

A Novel Thermal Modeling Framework

0.1 Introduction

The high rate of technological progress in the semiconductor industry in the last decade has driven a similarly high flow of innovation. This high rate of technological innovation was made possible due to various advances in IC manufacturing and architectural improvements in chip design. A constant stream of ever-improving designs has meant that customers are frequently given the opportunity to purchase new products, replacing an existing design for one that may boast additional features or possibly improved performance. This has created a culture on the part of the consumer where people have come to demand new hardware designs on a regular basis.

To satisfy and exploit the demands of the consumer, the industry has grown a business model that permits the industry to provide moderately priced designs to the consumer, but that same model expects the consumer to upgrade a given purchase on a regular basis to cover the industry's costs associated with research and development. Engaged in this self-perpetuating mechanism, the industry self-imposes increasing time pressures to satisfy the consumer's expectation for these new products.

The success of this business model to date has been largely due to the accelerated rate of innovation made possible through advances in various architectural design techniques[46, 62, 133] and integrated circuit manufacturing improvements [37]. The rate of improvement has historically followed Moore's law, which states that the number of transistors per chip doubles approximately every 18 months [14, 102]. It is likely that these many new technological improvements over the last decade acted as a springboard,

setting off a sequence of events that have led to what is now a self-perpetuating process between a customer-driven market that desires an improved design on an increasingly regular basis and the industry that strives to provide it in a timely manner to meet its own financial ambitions.

Although the industry has enjoyed tremendous success over this time period, there are indications that the trends may be changing. Within the past several years, companies have moved away from a strict performance-based metric of value to one that includes power efficiency as well. Although this shift has been driven by many factors, one of the most significant may be the fact that chip designs can no longer be pushed to improve performance at the same rate as was the case previously. Further, chips are not as reliable as they were before. The lifetime of a chip may be approaching that of a car. Even now the life expectancy of various model designs is less than 10 years [48]. There are many reasons for why chip lifetime is decreasing, while performance improvements are becoming increasingly modest.

First, interconnect traces have become an increasingly serious problem in targeting a given design for a new fabrication technology. While transistors decrease with each technology generation roughly following Moore's Law, interconnect traces cannot be scaled down at the same rate. As the delay associated with transferring a signal through a given transistor decreases relative to the rate of transferring that same signal through the wire interconnect that connects that transistor to the rest of the digital circuit, the wiring delay increasingly limits the performance of the design as a whole. This wiring delay is further a function of the temperature of the interconnect wiring.

As the circuit shrinks in size with each fabrication technology, heat is concentrated in a smaller and smaller area. This exacerbates the wiring delays.

The signal delays force designers to employ more conservative timing strategies. Ultimately, this means that the clock rate at which the device will function may need to be reduced to meet timing constraints. There are many other design strategies that can be employed, but not without accepting some performance tradeoffs.

Ultimately, these interconnect delays limit the ability of designers to exploit the additional real-estate available on the chip die made possible through the shrinking of gate logic with each technology generation. To combat this problem, multi-core implementations are being extensively explored. However, this puts additional pressure on software to adequately load-balance between the multiple cores, and many algorithms cannot be successfully “parallelized” to be targeted for multi-core implementations.

A second reason for the current problems is that chip power dissipation is out-pacing the capability to sufficiently cool the chips for stable operation. The power density of chips is constantly increasing with each technology generation. ITRS 2001 projected that by 2010 microprocessors would be using 200W. Many commercial server components already meet or exceed this. Intel “Skulltrail” systems now have 1KW power supply requirements for stable operation.

The problem is that, even with aggressive active cooling strategies, it remains very difficult to successfully dissipate enough heat to maintain reliable chip operating temperatures. Further, power density will increase with each technology generation. Since the power dissipation of a given transistor is a function of both the voltage of the

device and the switching frequency, the required power dissipation for newer designs with more transistors will always be higher unless there is an attempt to either reduce voltage, the operating frequency of the device, or both. However, the performance of the device is highly a function of the operating frequency, and voltage scaling operates as a linear function of the manufacturing technology. Therefore, it is largely accepted that overall power generation will not likely decrease for each generation if the number of transistors are to increase. As a result, a similar quantity of power will need to be dissipated over an ever shrinking region of the die for each transition to a newer technology generation.

A third reason for these problems is that chip reliability is largely governed by chip operating temperature. Therefore, the increasing power density trends impact chip reliability through electro-migration and dielectric gate breakdown. Electro-migration involves the gradual deformation of metal interconnect over time. Eventually, metal interconnect wires may short, causing a series of possible operating failures. Gate dielectric breakdown involves the chemical reactivity of the thin dielectric insulation for the transistor gate with the surrounding materials. Since the chemical reaction rate is governed by the Arrhenius equation, the rate of dielectric breakdown has a dependence upon temperature of the factor $e^{(\frac{-E_a}{RT})}$. This means chip reliability is highly a function of temperature.

Because the IC market financial model previously described has become so reliant upon a high rate of technological improvement to encourage customers to purchase new products, it must be able to overcome these new roadblocks. This struggle

to overcome technical obstacles is one of the reasons why the cost of IC manufacturing is growing with each technology generation, doubling every four years [12]. Given new technological obstacles and increasing financial pressures, it is critical that the industry find ways of cutting costs as well as solutions for many of these challenging design constraints.

Among the most intractable and costly design challenges previously described is the need to design a high performance chip that can run sufficiently cool so as to function reliably. This can be one of the most costly problems to overcome because there are comparatively fewer design tools engineers can employ late in the design cycle to cool a chip which is overheating than for other design constraints. Unlike other design constraints that can be remedied through modest design changes late in the design cycle, a chip that is significantly over thermal budget may necessitate a costly redesign of the device [74].

Despite the costly consequences of an overheating chip design, the trend is toward newer chips using more power – necessitating further heat dissipation. This means that, as technology advances, increasingly drastic strategies will need to be employed to mitigate the effects of increasing heat density. There are three main reasons why this is the case.

First, the temperature of a chip is highly dependent upon the amount of power the chip dissipates. However, the power dissipated is a function of the speed at which the chip is able to function – the frequency of operation. Therefore, any increase in frequency will produce more power, and more heat will need to be dissipated. And,

although frequency is not a direct measure of performance, one of the simplest ways to improve chip performance is to increase the clock frequency of the design.

Second, as chip technology advances, the amount of power the chip uses when it's idle increases as a percentage of the total power utilization. This is due to the fact that transistors leak current even when they are off. This means that even if the chip is largely inactive, the chip will be using a significant percentage (over 50 percent in some cases) of its overall power budget. This, in turn, means that the chip is still generating a significant amount of heat even when it isn't being used. As leakage power becomes an increasingly larger percentage of the overall power budget, reducing transistor activity becomes a less attractive method for relieving some of the thermal pressures.

Third, the ability of a chip designer to predict the thermal implications of a given architectural design decision early in the design cycle is limited. This is largely due to the fact that, unlike other aspects of chip design, the thermal behavior of a given design is dependent upon so many aspects of a given design – including fabrication technology, design geometry, and runtime behavior – that it is extremely difficult to predict these parameters well ahead of the final design being realized. Even worse, as chip designs and fabrication processes become increasingly complex, the design effort involved in each new design grows relative to the last [12]. This typically means that the design cycle becomes longer, meaning that any feedback to the original architectural engineers on the thermal behavior of their design will happen further away. In fact, many times the target chip fabrication technologies may have changed by the time the

chip design has been implemented – likely altering the thermal characteristics of the final design.

Over the last few years, a variety of temperature modeling frameworks have been developed to assist engineers in the accurate characterization of their chip designs. However, no comprehensive analysis was performed to evaluate the needs of accurately modeling various elements of the thermal system for a chip, the associated package, and system main-board. Specifically, no comprehensive analysis was performed to evaluate the transient thermal accuracy of a temperature modeling infrastructure that models interconnect modeling, transistor density variation, interconnect density variation, silicon-on-insulator technology, and detailed materials modeling for the chip, package and main-board.

Here we present a novel temperature modeling infrastructure that offers engineers a new way to explore solutions to these problems. The modeling framework, called Sesctherm, is a state-of-the-art finite-element-based thermal modeling system. The framework has been verified against transient, empirical data collected using a Delphi thermal test chip, and Flomerics FlothermTM thermal simulator. The framework is open-source and freely available to the academic community under a Gnu Public Licensing scheme.

The rest of the paper is organized as follows. In Chapter 1, we describe an overview of the modeling framework. In Section 2.2, we describe the modes of heat transport being modeled modeled. In Section 2.3 we describe the general algorithm employed by the Sesctherm model, including the Superlu sparse matrix library used. In

Section 2.4, the performance of the Sesetherm model is analyzed. In Section 2.5 the various material models are separately described. In Chapter 3 and Chapter 4, we describe the validation methodology used for the Delphi thermal test chip, and FlothermTM. In Chapters 5 through 9, a systematic evaluation is performed of the error incurred by omitting a reliable evaluation of the interconnect layers, package, interconnect density variation, silicon-on-insulator technology, system main-board, and accurate forced convection cooling modeling. In Chapter 10, we describe future enhancements to the model. In Chapter 11, we conclude. In Chapter 12, related work is described.

Chapter 1

Sesctherm Thermal Modeling

Framework

1.1 General Model Framework

Re-layout or redesign of a chip floor-plan to correct the design of a chip that is overheating can be prohibitively expensive. Late-state redesigns can lead to potentially disastrous consequences for time-to-market viability. This can ultimately cause an otherwise successful design to be non-competitive in the marketplace.

To avoid the need for such late-stage redesigns, companies are increasingly reliant upon thermal modeling early in the design cycle to gauge the thermal budget available for a given design and to explore various thermal optimization schemes. Therefore, it is essential that any thermal model characterize, as accurately as possible, the thermal behavior of the final design.

However, this generates a problem involving two events that are mutually dependent. Specifically, the thermal modeling must be accurate early in the design cycle. However, to perform reliable thermal evaluation of a given design requires detailed knowledge of the chip layout, technology, interconnect layout, ambient thermal conditions, dynamic power response, and static power response. The level of accuracy for the thermal analysis may therefore depend upon many parameters which will likely only be known once a design is finished. However, the need is to make reliable evaluations of the design before it is completed in order to preempt any thermal problems that may occur later in the design cycle. Further, this means that a thermally-aware design is difficult as designers have little knowledge about the consequences of novel design decisions until it may be too late – requiring costly changes to the design. Therefore, one may ask, “Is it possible to predict the thermal behavior of a processor design with only incomplete knowledge of the final design, and in so doing, alert engineers early in the design process about the thermal consequences of their design decisions when there is still time to change course?” This is known as an “*a priori* temperature characterization”.

Currently, there are three different means of *a priori* thermal characterization. The first method involves so-called “two-resistor” models where four nodes are given to the ambient outside environment, the silicon substrate, a pin connector on the outside of the package, and the main-board, respectively. The first junction-to-chip resistance separates the chip node from the node representing the package (the junction). The second junction-to-board resistance separates the junction from the main-board. The junction-to-ambient resistance is not given, and it usually is computed using standard

convection cooling approximations [13]. These so-called “two-resistor” models are typically chosen to avoid the complexity associated with detailed thermal models – where modeling can run for days or weeks [31]. However, naive models like these conservatively demonstrate errors of at least +/- 20 percent [31].

A second method uses detailed, compact resistance models that characterize the thermal resistance throughout the geometry of the design. These models demonstrate errors of at least +/- 5 percent [31]. However, these models do not model any time-varying conditions. This means that these models will only accurately characterize the thermal behavior of a design that has been running at constant power utilization for a long period of time. However, IC designs commonly exhibit wildly varying power utilization. While the power utilization may be regular in nature, so-called “steady-state” modeling like this will miss the time-dependent nature of heat transfer.

Neglecting the temporal nature of thermal behavior can have disastrous consequences. There are many thermal parameters that change over time. This will impact the rate of heat transfer and cooling that occurs. If this behavior is neglected, an otherwise viable design with simple resistance models like these could miss a thermal “run-away” scenario. Further, the reliability of a chip design as evaluated by the “mean-time-to-failure” or MTTF is highly dependent upon temperature, and short-term temperature spikes can cause a significant reduction of the MTTF. These so-called “hot spots,” where heat accumulates within the chip during periods of runtime, can cause chip failures even though the “steady-state” temperature may not exceed device limits.

The third method of thermal analysis involves the use of time-dependent ther-

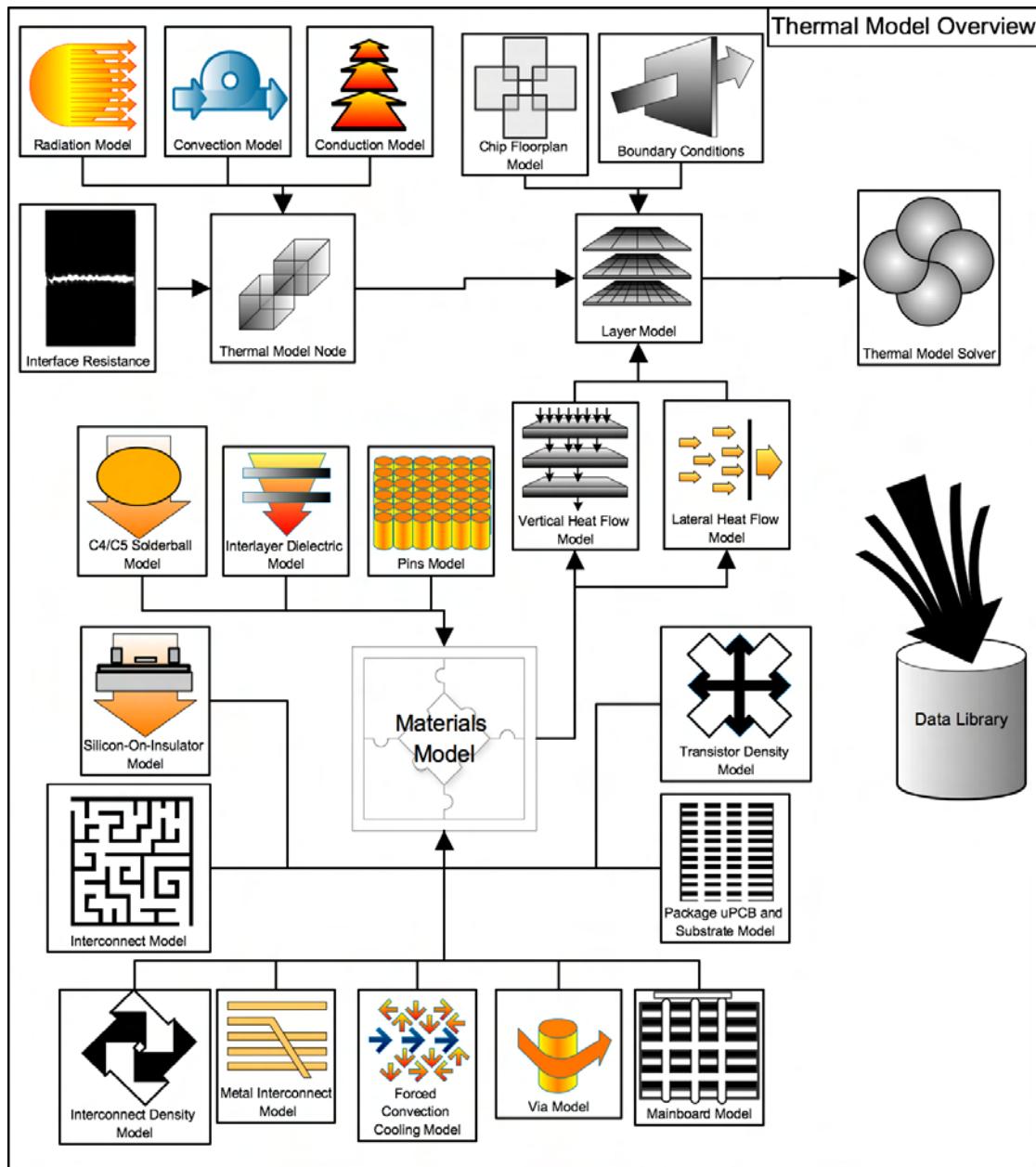


Figure 1.1: Overview of Sesctherm Modeling Framework with a Finite-Element Model, Thermal Simulation Model, and Materials Model

mal models that solve a variety of time-dependent differential equations that represent a variety of forms of heat flow. This method may not exhibit more reliable steady-state behavior than the compact resistance models, but these models will characterize the time-dependent nature of heat transfer. This includes the discovery of “hot spot” regions of the chip where heat may build up. Sesctherm is built based upon this type of model design.

The Sesctherm modeling framework has three discrete parts. The first part is a finite-element modeling framework. The second part is a thermal modeling framework. The third part is a material modeling framework. An overview can be seen in figure 1.1.

Sesctherm was designed to be highly modular and easily expandable. The model was built in C++ and makes full use of the concept of encapsulation and information hiding that is tremendously important in the design of complex modeling infrastructures. The model is self-contained and can be easily integrated with any existing application framework. Very little configuration is necessary as the model includes a library of material and technology parameters for 65, 90, 130, 180, and 250nm processes. The model’s combination of the Matrix Template Library and SuperLU for matrix operations means Sesctherm will benefit from certain improvements of these math libraries as they are improved over time. The model supports the multi-threaded SuperLU solver, although the exhibited parallelism was only modest. The serial libraries were preferred for this study. Sesctherm and all its constituent libraries are licensed under a Gnu Public License model. Any use or alteration of the model is permissible so

long as this thesis is referenced and licensing agreements are not removed.

Chapter 2

Computer-Based Temperature Modeling

2.1 Introduction

At the core of the Sesctherm is a “finite-element” model (FEM). Finite-element analysis involves taking a problem and segmenting the problem into smaller pieces. In the case of Sesctherm, the electronic design that is targeted for thermal analysis has a complex but regular geometry that can be characterized in software. Sesctherm divides the chip, package and associated components into a series of regular cross-sectional regions. Each region is a quadrilateral, and no two cross-sectional regions have abutting sides that are of different height or length.

Each cross-sectional region is called a temperature “node”, and each region has a series of properties. To accurately characterize complex materials and dimensions, Sesctherm subdivides regions by material and geometry. This means that each temperature node is considered to be one material or approximation of a combination

of materials. Further, this means that any irregular shape is approximated by a combination of quadrilateral regions.

Not only does Sesctherm subdivide the chip by geometry and material, but it also subdivides the runtime of the model. To determine the temperature distribution within a chip over a given time series, the model subdivides the time series into a series of small sub-intervals. The model then incrementally solves for the temperature at each sub-interval.

2.2 Modes of Heat Transfer

2.2.1 Conduction

Heat transfer models are highly analogous to electrical circuit theory. Each component of a thermal system can be considered either a heat source, heat sink, thermal capacitance, or thermal resistance. There are, of course, other non-linear devices that exhibit higher-order transient behavior. This model attempts to characterize devices as reliably as possible given the limitations imposed by runtime constraints.

Given the electrical or fluid analogy, heat is like an electrical or fluid current. It characterizes a transfer of energy in the form of intermolecular interactions, molecular excitation, and electromagnetic radiation. Following the same analogy, temperature is analogous to electrical voltage or the desire for water to travel from one point to another due to differing height (potential energy). This thermal “potential” represents the average energy state of a given point. The first principle of thermodynamics states

that all objects wish to be in thermal equilibrium. Also called the concept of entropy, any thermodynamic system wishes to return to the lowest-energy state. This means that if there is a temperature differential within the system, the system wishes to adjust itself so as to normalize the temperature distribution. A temperature difference is therefore a quantification of the degree of disorder in the system. The greater the temperature difference, the more aggressively the system moves toward stability.

Thermal capacitance is a physical property which describes the ability of any substance to store energy in the form of heat. This is analogous to an electrical capacitor or a water basin. Thermal capacitance is a physical property, and therefore the substance does not undergo chemical changes.

Thermal resistance is a physical property which characterizes the ability of a material to resist the transfer of energy in the form of heat. Similar to an electrical resistance or restriction in a tube for water flow, thermal resistance is a relation between the amount of heat dissipated to the subsequent temperature change. The temperature change between two points in any medium is equal to the amount of heat dissipated times the thermal resistance between the two points. This is analogous to “Ohm’s Law”.

There are three forms of heat transfer. Conduction involves the transfer of heat from a region of higher temperature to one of lower temperature through a solid, liquid or gas. Heat transfer in conduction occurs primarily due to intermolecular interactions and molecular movement. Therefore, materials that have higher energy inter-molecular bonds more readily support conduction as a heat transfer mechanism. Due to this requirement, conduction occurs more readily in a solid than liquid and in a liquid than

gas.

The change in temperature is related to heat dissipation and thermal resistance by equation (2.1). Stated another way, the rate of heat transfer is directly proportional to both the cross-sectional area in the direction of heat transfer and the change in temperature. Further, it is inversely proportional to the distance the heat travels. This means that $\frac{\Delta l}{kA}$ is equal to the thermal resistance. This can be seen in equation (2.2).

Equation (2.3) describes the general 3-dimensional thermal conduction equation. Equation (2.4) is a more accurate representation of how Sesctherm works. In particular, the thermal conductivity and specific heat are temperature dependent. In the case of isothermal (dirichlet-type) nodes, equation (2.5) is used. Sesctherm is subject to the boundary conditions described in equation (2.6). There are three types of boundary conditions that Sesctherm uses. First, Sesctherm allows for an isothermal surface – a surface where the temperature is unchanging. This can be defined for “what-if” analysis in the model. Second, Sesctherm allows for insulated surfaces where no heat is allowed to pass through. This allows controlled thermal environments to be modeled. Third, Sesctherm models convective fluid cooling to remove heat from the system. This requires “Robin”-type boundary conditions. These are all described in equation (2.6).

$$\Delta T = R * q$$

where ΔT is the temperature change

(2.1)

R is the thermal resistance

q is the rate of heat transfer

$$q = -\frac{kA\Delta T}{\Delta l}$$

where k is the thermal conductivity of the medium

A is the area normal to the direction of heat transfer

(2.2)

q is the heat transfer rate

Δl is the distance of the heat flow path

ΔT is the change in temperature

$$\frac{\partial}{\partial x} \left(k_x \frac{\partial T}{\partial x} \right) + \frac{\partial}{\partial y} \left(k_y \frac{\partial T}{\partial y} \right) + \frac{\partial}{\partial z} \left(k_z \frac{\partial T}{\partial z} \right) + q''' = \rho c_p \frac{\partial T}{\partial t}$$

where q''' is the power generation within the volume

T is the temperature within the volume

(2.3)

ρ is the density of the material within the volume

c_p is the specific heat of the material within the volume

k_x, k_y, k_z is the thermal conductivity of the material material

$$\nabla [k(x, y, z, T) * \nabla T(x, y, z, t)] + q'''(x, y, z, t) = \rho c_p(T) \frac{\partial T(x, y, z, t)}{\partial t}$$

where $q'''(x, y, z, t)$ is the power generation within the volume

$T(x, y, z, t)$ is the temperature within the volume

ρ is the density of the material within the volume

$c_p(T)$ is the specific heat of the material within the volume at a given temperature

$k_{(x, y, z, T)}$ k is the thermal conductivity at a particular temperature

$r_i(x, y, z)$ is the chosen temperature of a particular unit

(2.4)

$$k(x, y, z, T) \frac{\partial T(x, y, z, t)}{\partial n_i} + h(x, y, z, T)T(x, y, z, t) = r_i(x, y, z)$$

where q''' is the power generation within the volume

T is the temperature within the volume (2.5)

ρ is the density of the material within the volume

c_p is the specific heat of the material within the volume

Boundary Conditions:

Insulation (Neumann-type): $\frac{\partial T(x, y, z, t)}{\partial n_i} = 0$

Convection (Robin-type): $k_{(x,y,z,T)} \frac{\partial T(x, y, z, t)}{\partial n_i} = h(x, y, z, T) (T - T_{\text{ambient}})$

Isothermal (Dirichlet-type): $r_i(x, y, z) = T$

where T is the temperature within the volume

T_{ambient} is the ambient temperature of the environment

$k_{(x,y,z,T)}$ k is the conductivity at a particular temperature

$r_i(x, y, z)$ is the chosen temperature of a particular unit

(2.6)

2.2.2 Convection

Convection involves heat transfer in a fluid. The transfer of heat in this phase of matter is dominated by the moving of molecules, rather than inter-molecular forces due to the weaker inter-molecular attraction in fluids. Due to the fact that the movement of the particles dominates the heat transfer mechanism, accurate convection cooling necessitates a characterization of fluid motion before any analysis of the thermal behavior can be performed.

The motion of a fluid or gas can generally be divided into two domains. The first involves laminar flow conditions, and the second involves turbulent flow conditions. There is a region between the two domains known as the transition region. This region will be an unstable region where the fluid has some percentage laminar and some percentage turbulent character.

In laminar flow, fluid particles follow a continuous, orderly path. Each cross-section of fluid flow does not cross any other. Each particle following one flow path will not intersect another particle on a different flow path. Due to the fact that there isn't any reordering of particles, heat flow within the fluid flow is dominated by conduction between adjacent particles. At the intersection of a fluid and a solid surface, the fluid exchanges heat at the interface of the solid surface and the layer of particles that flows directly parallel to it.

In the case of turbulent flow, particle movement is highly irregular. The particle velocities may be highly random and unpredictable. Thus, the flow may vary

significantly over time. Fluid “eddies” or “vortices” may form in the fluid, where particles are repeatedly mixed. In this case, the rate of heat transfer is dominated by molecular movement and not conduction. The rate at which the particles collide will determine the overall rate of heat transfer.

Fluid flows are classified into either forced or natural convection. Forced convection involves work being performed by an external device to apply a force to static fluid particles to induce an acceleration. This external device may be a fan, pump etc. Natural convection only involves fluid transfer through a pressure gradient within the fluid caused by a temperature differential. Boyle’s Law indicates that the pressure within a fluid is directly proportional to its molar mass and temperature, if the volume is held constant. This means that that, in a closed environment where volume is held constant, a temperature increase in one region of the fluid will cause an increase in fluid pressure, causing that region of the fluid to diffuse. The diffusion of particles due to the pressure gradient will induce a flow within the fluid. For the purpose of this investigation, we use a strong fan to induce forced convection – and we assume natural convection is not present to such a degree that it would have any noticeable thermal effect. Of course, this assumption may not hold in other environments.

For the purpose of this analysis, we assume that air will either pass over the top surface of the chip surface or across the package or main-board. Under all conditions, we assume that the device experiencing cooling through convection can be reliably modeled as a flat plate. See figure 2.1. The region closest to the air inlet (closest to the external fan) will experience laminar flow due to the highly regular nature of the

flow stream exiting the fan, and then the flow will gradually transition to turbulent flow at some distance from the inlet. This “transition point” is the point where flow has a partial laminar and partial turbulent character. The distance from the fluid inlet to the boundary layer is known as the “hydrodynamic entry length” or “characteristic length” and can be computed with a high degree of accuracy.

To quantify the turbulent character of flow, the Reynold’s number is used. The Reynold’s number is a quantification of the turbulent character of flow. As can be seen in equation (2.7), for any substance with a given density and viscosity, the Reynold’s number is directly proportional to the velocity and the characteristic length (length from the fluid inlet). Although it will vary by the flow environment, in the case of flow over a horizontal flat plate, if the Reynold’s number exceeds $5.0 * 10^5$, fluid is generally considered turbulent. As can be seen by the equation, increased fluid velocity or increased length from the inlet will increase the Reynold’s number. This means that the further away from the inlet or the larger the magnitude of velocity, the more the flow will exhibit a turbulent character.

The characteristic length is a function of the fluid properties, geometry of the physical environment through which the fluid will flow, the thermal properties of the system, and the initial fluid velocity at the point of the inlet. In the case of forced convection, given a known Reynold’s number, flow rate and fluid properties, the characteristic length can be computed using (2.7).

$$Re = \frac{\rho VL_c}{\mu} = \frac{VL_c}{\nu}$$

where Re is the Reynold's Number

ρ is the density of the fluid

V is the velocity of the fluid (2.7)

L_c is the characteristic length (hydrodynamic entry length)

μ is the viscosity of the fluid

ν is the kinematic viscosity

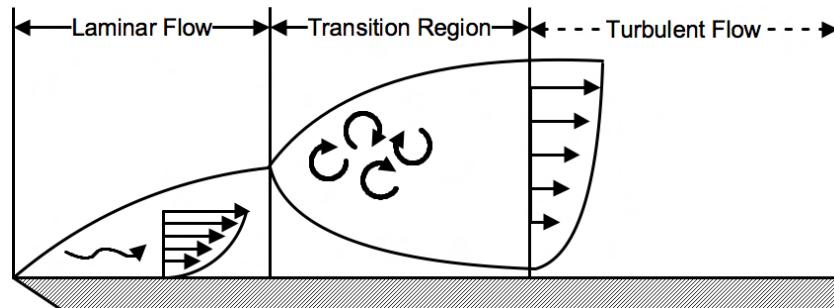


Figure 2.1: Fluid Flow Over Flat Surface

While the Reynold's number characterizes the nature of fluid flow over a given region, the Prandtl number characterizes the thermal character of the fluid. As was described before, heat transfer in a fluid occurs both through inter-molecular interaction and through particle movement. The degree to which heat transfer occurs by one mechanism as compared to the other is determined by the Prandtl number. Specifically, the Prandtl number relates the kinematic viscosity of a fluid to the thermal diffusivity

of that fluid. The kinematic viscosity is the rate at which momentum transfer occurs between fluid particles, while thermal diffusivity is the rate of heat transfer between fluid particles.

A substance with a high Prandtl number will tend to transfer heat primarily through particle movement and not inter-molecular interaction. Such a substance will tend to have higher viscosity (oils) or low density (gases), and therefore such a substance will tend to have a higher rate of momentum transfer and more readily produce turbulent flow. Turbulent flow facilitates a more efficient heat transfer than laminar, as described before.

Further, if a substance has a low thermal conductivity and high specific heat, the substance will have a tendency to store heat rather than transfer the heat, characterized by a small thermal diffusivity. Such a substance would therefore be characterized by a large Prandtl number. Further, such a substance could be a dielectric fluid used for electronic equipment. The low thermal conductivity of the fluid material means that heat transfer is dominated by fluid particle movement and not inter-molecular interactions.

Conversely, a substance that is represented by a low Prandtl number tends to transfer heat primarily through inter-molecular interaction and not particle movement. Such a fluid might be a liquid metal. In such a substance, the high thermal conductivity of the liquid means that heat transfer is dominated by inter-molecular interaction. Further, the low viscosity means that the flow is more likely to be laminar, where inter-molecular interaction dominates heat transfer.

Using both the Prandtl number and Reynold's number together, the complete thermal character of a fluid in a system can be accurately characterized. The number which describes this characterization is the Nusselt number. The Nusselt number is therefore a function of both the Reynold's number and the Prandtl number. Depending upon various properties of the cooling system, the relationship between the Reynold's number, Prandtl number, and Nusselt number will change. Specifically, depending upon whether or not forced convection or natural convection is to be modeled, and depending upon the specific geometry of the area modeled, the relationship between the three numbers may change. For the purpose of modeling fluid flow across the surface of the chip, package or main-board, Sesetherm assumes a one-dimensional system – where fluid flows over a flat plate. The proper relation between these three numbers is chosen specifically for this setup.

The general equation for convective heat transfer can be seen in (2.9). As can be seen, the rate of heat transfer is directly proportional to the temperature difference, the cross-sectional area over which heat transfer occurs, and the convective heat transfer coefficient. The heat transfer coefficient represents the effective thermal conductance. Thus, $\frac{1}{h_{\text{convection}}}$ represents the effective convective thermal resistance between a given surface and a fluid passing over it.

$$\text{Pr} = \frac{\nu}{\alpha} = \frac{\mu * c_p}{k}$$

where Pr is the Prandtl Number

ν is the kinematic viscosity of the fluid $= (\frac{\mu}{\rho})$

α is the thermal diffusivity of the fluid $= (\frac{k}{\rho c_p})$ (2.8)

μ is the viscosity of the fluid

c_p is the specific heat of the fluid

k is the thermal conductivity of the fluid

ρ is the density of the fluid

$$q_{\text{convection}} = h_{\text{convection}} A (T_{\text{surface}} - T_{\text{fluid}})$$

where q is the heat transfer rate between the surface and the fluid

$h_{\text{convection}}$ is the convective heat transfer coefficient (2.9)

A is the surface area over which heat transfer occurs

T_{surface} is the temperature of the surface over which the fluid flows

T_{fluid} is the temperature of the fluid

Therefore, a characterization of the rate of cooling for parallel fluid flow over a flat plate at a given point along the plate may be accurately characterized by the convective cooling coefficient. The convective cooling coefficient $h_{\text{convection}}$ is described

by equation (2.10), where the Nusselt number is described by equation (2.11). The heat transfer coefficient is frequently expressed in terms of the Nusselt number.

$$h_{\text{convection}} = \frac{Nu^*k}{L_c}$$

where $h_{\text{convection}}$ is the convective heat transfer coefficient

Nu is the Nusselt number (2.10)

k is the thermal conductivity of the fluid

L_c is the characteristic length

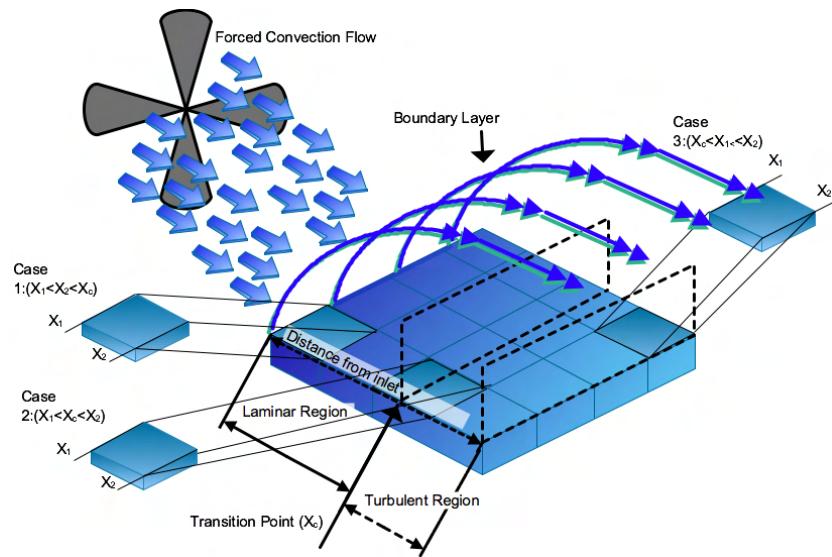


Figure 2.2: Flat Plate in Parallel Flow

Similar to the finite-element method used for conduction modeling, Seschtherm computes the average heat transfer coefficient for each cross-sectional model unit by computing the average Nusselt number for the model unit. This model uses equation

If $(x_1 < x_2 < x_c < x_L)$,

$$\bar{h}_{x_1-x_2} = \frac{k \left(0.332 \sqrt{\frac{u_\infty}{\nu}} \left(\int_{x_1}^{x_2} \frac{1}{\sqrt{x}} dx \right) \right) \sqrt[3]{\text{Pr}}}{x_2 - x_1}$$

$$\text{Integrating : } \bar{h}_{x_1-x_2} = \left(\frac{k}{(x_2 - x_1)} \right) 0.664 (\sqrt{x_2} - \sqrt{x_1}) \sqrt{\frac{u_\infty}{\nu}} \sqrt[3]{\text{Pr}}$$

$$\text{Simplifying : } \overline{\text{Nu}}_{x_1-x_2} = \frac{\bar{h}_{x_1-x_2} (x_2 - x_1)}{k} = 0.664 \left(\sqrt{\text{Re}_{x_2}} - \sqrt{\text{Re}_{x_1}} \right) \sqrt[3]{\text{Pr}}$$

Else If $(x_1 < x_c < x_2 < x_L)$,

$$\bar{h}_{x_1-x_2} = \frac{k \left(0.332 \sqrt{\frac{u_\infty}{\nu}} \left(\int_{x_1}^{x_c} \frac{1}{\sqrt{x}} dx \right) + 0.0296 \left(\frac{u_\infty}{\nu} \right)^{(4/5)} \left(\int_{x_c}^{x_2} \frac{1}{x^{(1/5)}} dx \right) \right) \sqrt[3]{\text{Pr}}}{x_2 - x_1}$$

Integrating :

$$\bar{h}_{x_1-x_2} = \left(\frac{k}{(x_2 - x_1)} \right) \left(\left(0.664 \sqrt{\frac{u_\infty}{\nu}} (\sqrt{x_c} - \sqrt{x_1}) \right) + 0.037 \left(\frac{u_\infty}{\nu} \right)^{(4/5)} (x_2^{4/5} - x_c^{4/5}) \right) \sqrt[3]{\text{Pr}}$$

$$\text{Simplifying : } \overline{\text{Nu}}_{x_1-x_2} = \frac{\bar{h}_{x_1-x_2} (x_2 - x_1)}{k} = \left(0.664 \left(\sqrt{\text{Re}_{x_c}} - \sqrt{\text{Re}_{x_1}} \right) + 0.037 \left(\text{Re}_{x_2}^{4/5} - \text{Re}_{x_c}^{4/5} \right) \right) \sqrt[3]{\text{Pr}}$$

Else If $(x_c < x_1 < x_2 < x_L)$,

$$\bar{h}_{x_1-x_2} = \frac{k \left(0.0296 \left(\frac{u_\infty}{\nu} \right)^{(4/5)} \left(\int_{x_1}^{x_2} \frac{1}{x^{(1/5)}} dx \right) \right) \sqrt[3]{\text{Pr}}}{x_2 - x_1}$$

$$\text{Integrating : } \bar{h}_{x_1-x_2} = \left(\frac{k}{(x_2 - x_1)} \right) \left(0.037 \left(\frac{u_\infty}{\nu} \right)^{(4/5)} (x_2^{4/5} - x_1^{4/5}) \right) \sqrt[3]{\text{Pr}}$$

$$\text{Simplifying : } \overline{\text{Nu}}_{x_1-x_2} = \frac{\bar{h}_{x_1-x_2} (x_2 - x_1)}{k} = 0.037 \left(\text{Re}_{x_2}^{4/5} - \text{Re}_{x_1}^{4/5} \right) \sqrt[3]{\text{Pr}}$$

where $\bar{h}_{x_1-x_2}$ is the convection coefficient between the leading and opposing edges of the model unit

x_c is the transition point where laminar flow transitions to turbulent flow

x_L is the point at the opposite end of the flat plate

k is the thermal conductivity of the fluid

u_∞ is the free stream velocity (velocity at leading edge of flat plate)

ν is the kinematic viscosity

Pr is the Prandtl Number (see Equation (2.8))

Re_x is the Reynold's number, where the characteristic length is x

(2.11)

(2.11) for this purpose. Specifically, to compute the heat transfer coefficient for the case of parallel flow over a flat plate, two different flow domains exist: laminar and turbulent. The point where the flow transitions from laminar to turbulent is x_c .

The model unit has left x-coordinate x_1 and right x-coordinate x_2 . If the model unit is closer to the fluid inlet than x_c or ($x_1 < x_2 < x_c < x_L$), then the Nusselt number at a particular point within the model unit is $0.332Re^{(1/2)}Pr^{(1/3)}$. By integrating from x_1 to x_2 and dividing by the $x_2 - x_1$ we find the average Nusselt number for the laminar region. Similarly, the Nusselt number is found where the model unit is intersected by a perpendicular line representing the transition region at distance x_c or ($x_1 < x_c < x_2 < x_L$). In this region, the flow has both laminar and turbulent character and is modeled accordingly. Further, the Nusselt number is found where the model unit is beyond the transition region ($x_c < x_1 < x_2 < x_L$). In this case, turbulent conditions are modeled. This can be seen in equation (2.11) and in figure 2.2.

2.2.3 Radiation

Unlike conduction and convection which involves heat transfer through molecular interactions or movement, radiation is a heat transfer mechanism by electromagnetic waves. Radiation usually contributes to a comparatively minor degree in the thermal analysis of electronics due to the fact that heat transfer is largely dominated by convection and conduction. However, there are a variety of scenarios where radiation may be the dominant mode of heat transfer. This includes enclosed environments where heat cannot leave the system using any other heat transfer mechanism. This could include

includes vacuum chambers and computer systems targeted for space exploration. Further, at small scales, the participation of these heat transfer mechanisms may change, as described in [60].

The total thermal energy radiating from a given surface is represented by equation (2.12). Similar to the methodology used for convection and conduction, Sesetherm models each model unit with a separate convective heat transfer coefficient. Due to the fact that each model unit is a quadrilateral where no two adjacent units overlap one another, Sesetherm considers each model unit pair to be aligned rectangles. See figure 2.3. In this case the height and width of the model unit is X and Y respectively, while the distance between the centers of model unit pairs is L . Under these conditions, the “view factor”, which characterizes the geometrical properties of the thermal system can be expressed by equation 2.13.

$$q_{\text{radiation}} = h_{\text{radiation}} A(T_1 - T_2) \quad ([55])$$

$$h_{\text{radiation}} = 4\Sigma\sigma F_{1,2}(T_1 T_2)^{3/2} \quad ([13])$$

where $q_{\text{radiation}}$ is the heat transfer through radiation

$h_{\text{radiation}}$ is the heat transfer coefficient of radiation

(2.12)

T_1, T_2 are the temperatures of the two radiating nodes respectively

Σ is the emissivity of the material

σ is the Stefan-Boltzmann constant ($5.67 \times 10^{-8} W/(m^2 K^4)$)

$F_{1,2}$ is the view factor

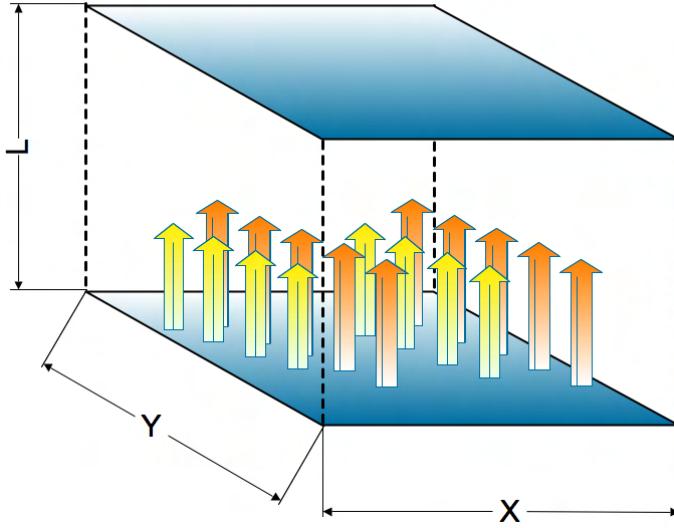


Figure 2.3: Radiation Between Aligned Parallel Rectangles

$$\begin{aligned}
 F_{x,y} = \text{view_factor}(x, y, l) = & \frac{2}{\pi \frac{x}{l} \frac{y}{l}} \left(\sqrt{\ln \left(\frac{\left(1 + \left(\frac{x}{l}\right)^2\right) \left(1 + \left(\frac{y}{l}\right)^2\right)}{1 + \left(\frac{x}{l}\right)^2 + \left(\frac{y}{l}\right)^2} \right)} \right. \\
 & + \frac{x}{l} \sqrt{\left(1 + \left(\frac{y}{l}\right)^2\right)} \tan^{-1} \left(\frac{\frac{x}{l}}{\sqrt{1 + \left(\frac{y}{l}\right)^2}} \right) \\
 & + \frac{y}{l} \sqrt{\left(1 + \left(\frac{x}{l}\right)^2\right)} \tan^{-1} \left(\frac{\frac{y}{l}}{\sqrt{1 + \left(\frac{x}{l}\right)^2}} \right) \\
 & \left. - \frac{x}{l} \tan^{-1} \left(\frac{x}{l} \right) - \frac{y}{l} \tan^{-1} \left(\frac{y}{l} \right) \right)
 \end{aligned} \quad (2.13)$$

2.2.4 Interface Resistance

The transfer of heat between materials that are imperfectly connected is less efficient than heat transfer within a continuous material distribution. At the interface

formed at the adhesion of the two materials, an additional resistance is introduced. Macroscopic properties of the surface roughness, material hardness, and contact pressure determine the overall resistance. This thermal “contact resistance” is the result of small imperfections that create a small air gap at the interface of the two materials. This can be seen in figure 2.4.

Sesctherm models this resistance following the work of Yavanovich citeBejan:2003qq. Specifically, the contact resistance is described by equation (2.14).

It should be noted that a resistance exists even if there is perfect adhesion between the two materials [13]. This is known as a thermal “boundary resistance”, and is not modeled explicitly in Sesctherm. A variety of acoustic mismatch and diffuse mismatch models have been developed [122, 118]. These AMM and DMM models can be used to characterize these interface resistances. This is considered future work.

$$R_{contact} = \left[\frac{500000 \cdot \left(\frac{P}{H}\right)^{0.95} k_1 k_2}{k_1 + k_2} + \frac{0.451926 k_g}{\left(-\frac{\ln P}{H}\right)^{0.547} \sqrt{\sigma_1^2 + \sigma_2^2}} \right]^{-1}$$

where, P is the contact pressure at the interface of the two materials (Pa)

H is the surface micro-hardness of the softer material

k_1, k_2 are the conductivities of materials 1 and 2 respectively

k_g is the interstitial fluid thermal conductivity

σ_1, σ_2 are the surface roughness values for surfaces 1 and 2 respectively

(2.14)

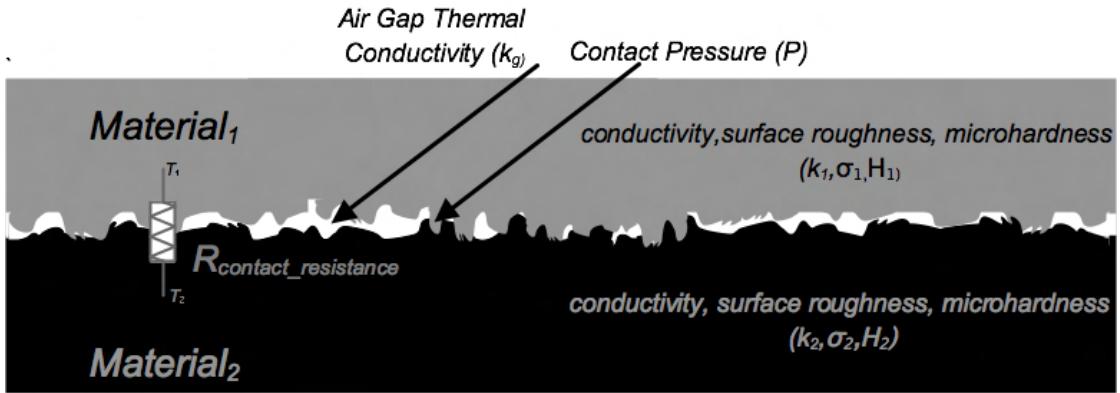


Figure 2.4: Solid-Solid Material Interface

2.2.5 Unifying Heat Equations

Once characterizing the individual contributions of each heat transfer pathway, Sesctherm unifies all the equations to compute the temperatures at each of the temperature nodes for each time-step of the model. Specifically, conduction, convection, and radiation is modeled for each of the relevant model units based upon the the material and geometry.

Each model unit is treated as an isothermal volume. Further, the solution domain includes all the model layers. Flexible boundary conditions exist to allow for convective cooling for every region at the thermal boundary of the solution domain or strict constraints can enforce an infinite thermal insulation at the domain boundaries. There are a variety of conditions where varying boundary conditions may be desirable. A situation that would necessitate the former case could involve a situation where air flow passes over the chip, package, and main-board. Flexible boundary conditions allows

the model to allow convective cooling at all the thermal boundaries automatically. The later case could be useful in a closed system or where strict thermal controls on the thermal model is necessary.

Further, the model allows for any model unit to have a specific temperature set. This allows for modeling of subsets of an otherwise complex thermal system quite easily so long as the thermal boundary conditions of the system are stable. This is especially useful in situations where engineers wish to perform “what-if” studies about the thermal limits of a given system.

Each thermal model unit is governed by equation (2.15). This equation states that the rate of energy entering the model unit, plus the rate of energy generated by the unit, less the rate of energy leaving the unit is equal to rate of change of energy stored in the model unit. Specifically, Sesctherm models each thermal node, as described before, as a quadrilateral.

The cross-sectional area of every adjacent volume has the same dimensions. This means that no two adjacent volumes will overlap. The reason for this is that it avoid certain limitations of modeling thermal spreading resistance, based on work by Lee et al. Spreading resistance is a means for simplifying the analysis where two thermal nodes are of different sizes. The spreading resistance is used to account for the thermal spreading effects as heat transitions from two volumes of different dimensions. However, it has previously been described that although the approximates made by Lee et al. provides approximates for thermal spreading resistance that are within +/- 3 percent error [112] significant error in spreading resistance may be present if the

closed-form expressions provided by Song et al. are used on quadrilaterals where the ratio of any two sides deviates significantly from unity [112]. To avoid any non-idealities associated with the spreading resistance computation, regular quadrilateral regions were used exclusively.

The quadrilateral thermal node Sesctherm uses is depicted in 2.5. As can be seen, the model shows a control volume surrounded by six volumes at each of the six edges. The various boundary conditions present in the model may eliminate one or all of the surrounding temperature nodes and treat that side of the node as an infinite resistance. However, for simplicity, this discussion will focus on a model unit that is surrounded by six other units.

As can be seen in 2.5, three axes are defined, where the “left” node is in the negative x direction, and the “down” node is in the negative z direction. Each of the surrounding six units have a specific thermal conductivity. Further, the center node has four different thermal conductivities defined for thermal heat transfer in both the lateral and vertical directions to the adjacent thermal units. Further, an interface resistance is defined between the center unit and each of the surrounding six units.

It should be noted that each of the surrounding six units is identical to the unit depicted. As such, each of the surrounding six units also has six different thermal conductivities for heat transfer in all six directions. Therefore, in the diagram provided, k_{left} is actually $k_{\text{center,right}}$ for the node to the left, indicating the the thermal conductivity of the left node to its right.

There are three dimensions shown in each of the three axes. On the x axis,

lengths dx_1 , dx_2 , and dx_3 correspond to the widths of the left, center, and right nodes respectively. A similar naming scheme has been adopted for the y and z axis.

Following equation (2.15), for a node in a closed system, rates of heat leaving the system subtracted from the sum of the rates of heat entering and generated by the system is equal to the rate of change in which energy is stored. This can be seen in equation (2.16), where this is a restatement of equation (2.3). We define gamma in equation (2.17) for convenience. Including all relevant equations for thermal conductivity, equation (2.18) is generated. This equation is depicted in 2.6.

This is a discretion of the differential equation (2.3) to be solved using finite-element analysis. There are two classic methods of solving differential equations using computer techniques. The first is the “explicit” method and the second is the “implicit” method. Given initial conditions, the “explicit” method solves attempts to solve the ODE, for the next time step. In this case, the “explicit” method could be used to solve for temperature values at time $p + 1$ if the temperature was known at time p . However, this method has several limitations, the most serious being the fact that the time steps have to be sufficiently small to approximate dt so as not to introduce error. If the time step is too large, the system may become unstable, producing erroneous results.

The “implicit” method is the one used in Sesetherm. Rather than solving the system for some temperature values at time $p + 1$, we take the temperature values at time $t + 1$ and attempt to find temperature values at time p for all the model units that simultaneously satisfy the thermal equations at each of the model units. This involves simultaneously solving the discretized differential equation for each of the model units

simultaneously.

The “implicit” method does not suffer from the instability problems associated with the implicit method. Further, the time steps may be significantly smaller without introducing significant error. This allows Sesctherm the ability to provide a variable level of modeling accuracy with a tradeoff in performance.

Solving the “implicit” form of the discretized differential equation for the temperature at time p , we are given equation (2.19). If the effects of conduction, radiation, and convection are simultaneously included, we are given equation (2.20), where each of the relevant coefficients are described in equations (2.21) and (2.22).

$$\dot{E}_{\text{in}} + \dot{E}_{\text{generated}} - \dot{E}_{\text{out}} = \frac{dE_{\text{stored}}}{dt} = \dot{E}_{\text{stored}} \quad (2.15)$$

$$\begin{aligned} & (q_{\text{bottom}_{\text{conduction,convection,radiation}}} \rightarrow q_{\text{center}}) + (q_{\text{down}_{\text{conduction,convection,radiation}}} \rightarrow q_{\text{center}}) \\ & + (q_{\text{left}_{\text{conduction,convection,radiation}}} \rightarrow q_{\text{center}}) + (q_{\text{right}_{\text{conduction,convection,radiation}}} \rightarrow q_{\text{center}}) \\ & + (q_{\text{top}_{\text{conduction,convection,radiation}}} \rightarrow q_{\text{center}}) + (q_{\text{up}_{\text{conduction,convection,radiation}}} \rightarrow q_{\text{center}}) \\ & + \frac{(dx_2 dy_2 dz_2) \overset{\circ}{q}}{k} \\ & = \frac{\rho (dx_2 dy_2 dz_2) c_p (T_m^{p+1} - T_m^p)}{dt} \end{aligned} \quad (2.16)$$

$$\text{define } \gamma = \frac{\rho (dx_2 dy_2 dz_2) c_p}{dt} \quad (2.17)$$

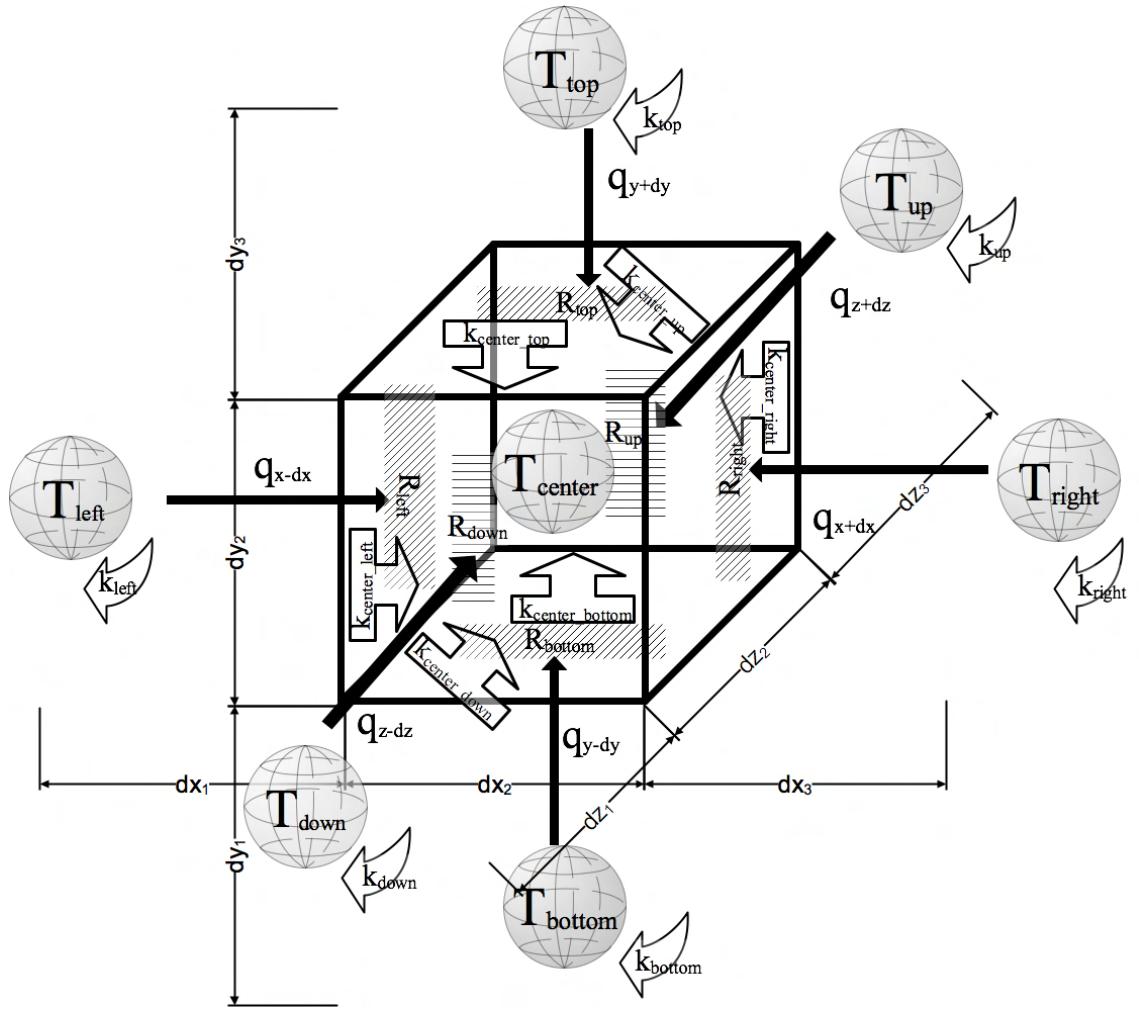


Figure 2.5: Model Unit Visualization

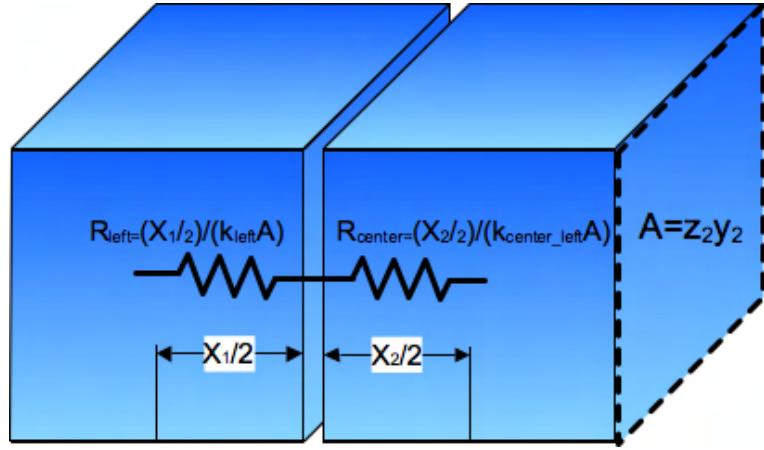


Figure 2.6: Simple Conduction Between Two Model Units

Full equation, modeling only conduction and interface resistance:

$$\begin{aligned}
 & \frac{(k_{\text{bottom}} k_{\text{center}} dz_2 dx_2) (T_{\text{bottom}}^{p+1} - T_{\text{center}}^{p+1})}{\frac{dy_2 k_{\text{bottom}}}{2} + k_{\text{center}} R_{\text{bottom}} k_{\text{bottom}} + \frac{dx_1 k_{\text{center}}}{2}} \\
 & + \frac{(k_{\text{down}} k_{\text{center}} dy_2 dx_2) (T_{\text{down}}^{p+1} - T_{\text{center}}^{p+1})}{\frac{dz_1 k_{\text{center}}}{2} + k_{\text{down}} R_{\text{down}} k_{\text{center}} + \frac{dz_2 k_{\text{down}}}{2}} \\
 & + \frac{(k_{\text{left}} k_{\text{center}} dz_2 dy_2) (T_{\text{left}}^{p+1} - T_{\text{center}}^{p+1})}{\frac{dx_1 k_{\text{center}}}{2} + k_{\text{left}} R_{\text{left}} k_{\text{center}} + \frac{dx_2 k_{\text{left}}}{2}} \\
 & + \frac{(k_{\text{right}} k_{\text{center}} dz_2 dy_2) (T_{\text{right}}^{p+1} - T_{\text{center}}^{p+1})}{\frac{dx_3 k_{\text{center}}}{2} + k_{\text{right}} R_{\text{right}} k_{\text{center}} + \frac{dx_2 k_{\text{right}}}{2}} \\
 & + \frac{(k_{\text{top}} k_{\text{center}} dz_2 dx_2) (T_{\text{top}}^{p+1} - T_{\text{center}}^{p+1})}{\frac{dy_3 k_{\text{center}}}{2} + k_{\text{top}} R_{\text{top}} k_{\text{center}} + \frac{dy_2 k_{\text{top}}}{2}} \\
 & + \frac{(k_{\text{up}} k_{\text{center}} dy_2 dx_2) (T_{\text{up}}^{p+1} - T_{\text{center}}^{p+1})}{\frac{dz_3 k_{\text{center}}}{2} + k_{\text{up}} R_{\text{up}} k_{\text{center}} + \frac{dz_2 k_{\text{up}}}{2}} + q (dx_2 dy_2 dz_2) = \gamma (T_{\text{center}}^{p+1} - T_{\text{center}}^p)
 \end{aligned} \tag{2.18}$$

Solving for T_{center}^p :

$$\begin{aligned}
T_{\text{center}}^{p+1} & \left(\gamma + \frac{(k_{\text{bottom}} k_{\text{center}} dz_2 dx_2)}{\frac{dy_2 k_{\text{bottom}}}{2} + k_{\text{center}} R_{\text{bottom}} k_{\text{bottom}} + \frac{dy_1 k_{\text{center}}}{2}} \right. \\
& + \frac{(k_{\text{down}} k_{\text{center}} dy_2 dx_2)}{\frac{dz_1 k_{\text{center}}}{2} + k_{\text{down}} R_{\text{down}} k_{\text{center}} + \frac{dz_2 k_{\text{down}}}{2}} \\
& + \frac{(k_{\text{left}} k_{\text{center}} dz_2 dy_2)}{\frac{dx_1 k_{\text{center}}}{2} + k_{\text{left}} R_{\text{left}} k_{\text{center}} + \frac{dx_2 k_{\text{left}}}{2}} \\
& + \frac{(k_{\text{right}} k_{\text{center}} dz_2 dy_2)}{\frac{dx_3 k_{\text{center}}}{2} + k_{\text{right}} R_{\text{right}} k_{\text{center}} + \frac{dx_2 k_{\text{right}}}{2}} \\
& + \frac{(k_{\text{top}} k_{\text{center}} dz_2 dx_2)}{\frac{dy_3 k_{\text{center}}}{2} + k_{\text{top}} R_{\text{top}} k_{\text{center}} + \frac{dy_2 k_{\text{top}}}{2}} \\
& + \frac{(k_{\text{up}} k_{\text{center}} dy_2 dx_2)}{\frac{dz_3 k_{\text{center}}}{2} + k_{\text{up}} R_{\text{up}} k_{\text{center}} + \frac{dz_2 k_{\text{up}}}{2}} \Big) \\
& - T_{\text{left}}^{p+1} \left(\frac{(k_{\text{left}} k_{\text{center}} dz_2 dy_2)}{\frac{dx_1 k_{\text{center}}}{2} + k_{\text{left}} R_{\text{left}} k_{\text{center}} + \frac{dx_2 k_{\text{left}}}{2}} \right) \\
& - T_{\text{right}}^{p+1} \left(\frac{(k_{\text{right}} k_{\text{center}} dz_2 dy_2)}{\frac{dx_3 k_{\text{center}}}{2} + k_{\text{right}} R_{\text{right}} k_{\text{center}} + \frac{dx_2 k_{\text{right}}}{2}} \right) \\
& - T_{\text{down}}^{p+1} \left(\frac{(k_{\text{down}} k_{\text{center}} dy_2 dx_2)}{\frac{dz_1 k_{\text{center}}}{2} + k_{\text{down}} R_{\text{down}} k_{\text{center}} + \frac{dz_2 k_{\text{down}}}{2}} \right) \\
& - T_{\text{up}}^{p+1} \left(\frac{(k_{\text{up}} k_{\text{center}} dy_2 dx_2)}{\frac{dz_3 k_{\text{center}}}{2} + k_{\text{up}} R_{\text{up}} k_{\text{center}} + \frac{dz_2 k_{\text{up}}}{2}} \right) \\
& - T_{\text{bottom}}^{p+1} \left(\frac{(k_{\text{bottom}} k_{\text{center}} dz_2 dx_2)}{\frac{dy_2 k_{\text{bottom}}}{2} + k_{\text{center}} R_{\text{bottom}} k_{\text{bottom}} + \frac{dy_1 k_{\text{center}}}{2}} \right) \\
& - T_{\text{top}}^{p+1} \left(\frac{(k_{\text{top}} k_{\text{center}} dz_2 dx_2)}{\frac{dy_3 k_{\text{center}}}{2} + k_{\text{top}} R_{\text{top}} k_{\text{center}} + \frac{dy_2 k_{\text{top}}}{2}} \right) \\
& = \gamma T_{\text{center}}^p + \overset{\circ}{q}(dx_2 dy_2 dz_2)
\end{aligned} \tag{2.19}$$

Simplified, including the effect of conduction, convection and radiation:

$$\begin{aligned}
& T_{\text{center}}^{p+1} (\gamma + \text{conduct}_{\text{conduction},\text{left}} + \text{conduct}_{\text{convection},\text{left}} + \text{conduct}_{\text{radiation},\text{left}} \\
& + \text{conduct}_{\text{conduction},\text{right}} + \text{conduct}_{\text{convection},\text{right}} + \text{conduct}_{\text{radiation},\text{right}} \\
& + \text{conduct}_{\text{conduction},\text{down}} + \text{conduct}_{\text{convection},\text{down}} + \text{conduct}_{\text{radiation},\text{down}} \\
& + \text{conduct}_{\text{conduction},\text{up}} + \text{conduct}_{\text{convection},\text{up}} + \text{conduct}_{\text{radiation},\text{up}} \\
& + \text{conduct}_{\text{conduction},\text{bottom}} + \text{conduct}_{\text{convection},\text{bottom}} + \text{conduct}_{\text{radiation},\text{bottom}} \\
& + \text{conduct}_{\text{conduction},\text{top}} + \text{conduct}_{\text{convection},\text{top}} + \text{conduct}_{\text{radiation},\text{top}}) \\
& - T_{\text{left}}^{p+1} (\text{conduct}_{\text{conduction},\text{left}} + \text{conduct}_{\text{convection},\text{left}} + \text{conduct}_{\text{radiation},\text{left}}) \\
& - T_{\text{right}}^{p+1} (\text{conduct}_{\text{conduction},\text{right}} + \text{conduct}_{\text{convection},\text{right}} + \text{conduct}_{\text{radiation},\text{right}}) \\
& - T_{\text{down}}^{p+1} (\text{conduct}_{\text{conduction},\text{down}} + \text{conduct}_{\text{convection},\text{down}} + \text{conduct}_{\text{radiation},\text{down}}) \\
& - T_{\text{up}}^{p+1} (\text{conduct}_{\text{conduction},\text{up}} + \text{conduct}_{\text{convection},\text{up}} + \text{conduct}_{\text{radiation},\text{up}}) \\
& - T_{\text{bottom}}^{p+1} (\text{conduct}_{\text{conduction},\text{bottom}} + \text{conduct}_{\text{convection},\text{bottom}} + \text{conduct}_{\text{radiation},\text{bottom}}) \\
& - T_{\text{top}}^{p+1} (\text{conduct}_{\text{conduction},\text{top}} + \text{conduct}_{\text{convection},\text{top}} + \text{conduct}_{\text{radiation},\text{top}}) \\
& = \gamma T_{\text{center}}^p + \overset{\circ}{q} (dx_2 dy_2 dz_2)
\end{aligned} \tag{2.20}$$

where $\text{conduct}_{\text{conduction},\text{left}} = \frac{1}{\left(\frac{\left(\frac{dx_2}{2}\right)}{\text{conduct}_{\text{center},\text{left}} * \text{area}_{\text{left,right}}} + R_{\text{left}} + \frac{\left(\frac{dx_1}{2}\right)}{\text{conduct}_{\text{center},\text{left}} * \text{area}_{\text{left,right}}} \right)}$

$$\text{conduct}_{\text{convection},\text{left}} = \max(\text{convection_coefficient}_{\text{left}}, \text{convection_coefficient}_{\text{center}}) * \text{area}_{\text{left,right}}$$

$$\text{conduct}_{\text{radiation},\text{left}} = 4 * \text{emissivity}_{\text{center}} * \sigma * \text{view_factor} \left(dz_2, dy_2, \frac{dx_1}{2} + \frac{dx_2}{2} \right) * (T_{\text{center}}^{p+1} * T_{\text{left}}^{p+1})^{\frac{3}{2}}$$

$$\text{conduct}_{\text{conduction},\text{right}} = \frac{1}{\left(\frac{\left(\frac{dx_2}{2}\right)}{\text{conduct}_{\text{center},\text{right}} * \text{area}_{\text{left,right}}} + R_{\text{right}} + \frac{\left(\frac{dx_3}{2}\right)}{\text{conduct}_{\text{center},\text{right}} * \text{area}_{\text{left,right}}} \right)}$$

$$\text{conduct}_{\text{convection},\text{right}} = \max(\text{convection_coefficient}_{\text{right}}, \text{convection_coefficient}_{\text{center}}) * \text{area}_{\text{left,right}}$$

$$\text{conduct}_{\text{radiation},\text{right}} = 4 * \text{emissivity}_{\text{center}} * \sigma * \text{view_factor} \left(dz_2, dy_2, \frac{dx_3}{2} + \frac{dx_2}{2} \right) * (T_{\text{center}}^{p+1} * T_{\text{right}}^{p+1})^{\frac{3}{2}}$$

$$\text{conduct}_{\text{conduction},\text{down}} = \frac{1}{\left(\frac{\left(\frac{dz_2}{2}\right)}{\text{conduct}_{\text{center},\text{down}} * \text{area}_{\text{down,up}}} + R_{\text{down}} + \frac{\left(\frac{dz_1}{2}\right)}{\text{conduct}_{\text{center},\text{down}} * \text{area}_{\text{down,up}}} \right)}$$

$$\text{conduct}_{\text{convection},\text{down}} = \max(\text{convection_coefficient}_{\text{down}}, \text{convection_coefficient}_{\text{center}}) * \text{area}_{\text{down,up}}$$

$$\text{conduct}_{\text{radiation},\text{down}} = 4 * \text{emissivity}_{\text{center}} * \sigma * \text{view_factor} \left(dx_2, dy_2, \frac{dz_1}{2} + \frac{dz_2}{2} \right) * (T_{\text{center}}^{p+1} * T_{\text{down}}^{p+1})^{\frac{3}{2}}$$

$$\text{conduct}_{\text{conduction},\text{up}} = \frac{1}{\left(\frac{\left(\frac{dz_2}{2}\right)}{\text{conduct}_{\text{center},\text{up}} * \text{area}_{\text{down,up}}} + R_{\text{up}} + \frac{\left(\frac{dz_3}{2}\right)}{\text{conduct}_{\text{center},\text{up}} * \text{area}_{\text{down,up}}} \right)}$$

$$\text{conduct}_{\text{convection},\text{up}} = \max(\text{convection_coefficient}_{\text{up}}, \text{convection_coefficient}_{\text{center}}) * \text{area}_{\text{down,up}}$$

$$\text{conduct}_{\text{radiation},\text{up}} = 4 * \text{emissivity}_{\text{center}} * \sigma * \text{view_factor} \left(dx_2, dy_2, \frac{dz_3}{2} + \frac{dz_2}{2} \right) * (T_{\text{center}}^{p+1} * T_{\text{up}}^{p+1})^{\frac{3}{2}}$$

$$\text{conduct}_{\text{conduction},\text{bottom}} = \frac{1}{\left(\frac{\left(\frac{dy_2}{2}\right)}{\text{conduct}_{\text{center},\text{bottom}} * \text{area}_{\text{bottom,top}}} + R_{\text{bottom}} + \frac{\left(\frac{dy_1}{2}\right)}{\text{conduct}_{\text{center},\text{bottom}} * \text{area}_{\text{bottom,top}}} \right)}$$

$$\text{conduct}_{\text{convection},\text{bottom}} = \max(\text{convection_coefficient}_{\text{bottom}}, \text{convection_coefficient}_{\text{center}}) * \text{area}_{\text{bottom,top}}$$

$$\text{conduct}_{\text{radiation},\text{bottom}} = 4 * \text{emissivity}_{\text{center}} * \sigma * \text{view_factor} \left(dx_2, dz_2, \frac{dy_1}{2} + \frac{dy_2}{2} \right) * (T_{\text{center}}^{p+1} * T_{\text{bottom}}^{p+1})^{\frac{3}{2}}$$

$$\text{conduct}_{\text{conduction},\text{top}} = \frac{1}{\left(\frac{\left(\frac{dy_2}{2}\right)}{\text{conduct}_{\text{center},\text{top}} * \text{area}_{\text{bottom,top}}} + R_{\text{top}} + \frac{\left(\frac{dy_3}{2}\right)}{\text{conduct}_{\text{center},\text{top}} * \text{area}_{\text{bottom,top}}} \right)}$$

$$\text{conduct}_{\text{convection},\text{top}} = \max(\text{convection_coefficient}_{\text{top}}, \text{convection_coefficient}_{\text{center}}) * \text{area}_{\text{bottom,top}}$$

$$\text{conduct}_{\text{radiation},\text{top}} = 4 * \text{emissivity}_{\text{center}} * \sigma * \text{view_factor} \left(dx_2, dz_2, \frac{dy_3}{2} + \frac{dy_2}{2} \right) * (T_{\text{center}}^{p+1} * T_{\text{top}}^{p+1})^{\frac{3}{2}}$$
(2.21)

$$\begin{aligned}
\text{view_factor}(x, y, l) = & \frac{2}{\pi \frac{x}{l} \frac{y}{l}} \left(\sqrt{\ln \left(\frac{\left(1 + \left(\frac{x}{l}\right)^2\right) \left(1 + \left(\frac{y}{l}\right)^2\right)}{1 + \left(\frac{x}{l}\right)^2 + \left(\frac{y}{l}\right)^2} \right)} \right. \\
& + \frac{x}{l} \sqrt{\left(1 + \left(\frac{y}{l}\right)^2\right)} \tan^{-1} \left(\frac{\frac{x}{l}}{\sqrt{1 + \left(\frac{y}{l}\right)^2}} \right) \\
& + \frac{y}{l} \sqrt{\left(1 + \left(\frac{x}{l}\right)^2\right)} \tan^{-1} \left(\frac{\frac{y}{l}}{\sqrt{1 + \left(\frac{x}{l}\right)^2}} \right) \\
& - \frac{x}{l} \tan^{-1} \left(\frac{x}{l} \right) \\
& \left. - \frac{y}{l} \tan^{-1} \left(\frac{y}{l} \right) \right)
\end{aligned} \tag{2.22}$$

where $\text{area}_{\text{left,right}} = dz_2 dy_2$

$\text{area}_{\text{down,up}} = dx_2 dy_2$

$\text{area}_{\text{bottom,top}} = dx_2 dz_2$

2.3 Implementation and General Algorithm

All software systems experience a temperature phenomenon of decay over time [49, 4, 84]. The rate of software decay is highly a function of the number of changes to the source code. The quantification of the decay that a software program experiences is in terms of the level of “difficulty” in changing the source code [66]. Based upon the theory of software evolution, this “changeability” metric is closely related to the interconnectedness of the disparate elements of the source code.

Complex modeling infrastructures, due to the degree of data reuse and complexity in the algorithms, may be among the most complex software architectures, and therefore most prone to a high rate of software decay. Sesctherm has been explicitly written to minimize these effects. There have been several steps taken to ensure that the code-base is easily maintainable, even given substantial changes.

First, Sesctherm never uses any global variables at any point. This is essential if the benefits of object-oriented design are to be exploited. Second, Sesctherm employs a straightforward initialization sequence that can be easily altered. Each initialization step is self-contained, and the order of model events is easily viewable to the code developer. Third, Sesctherm employs an all-to-all connectivity mechanism through a shared data library. Rather than dealing with the complexity associated with accessors and manipulators for each of the numerous data structures, the level of data interconnectedness requires a central data storage mechanism that does not break the object-oriented mechanism of encapsulation. Sesctherm does this by passing a “data library” pointer to every generated object that requires access to data elsewhere in the modeling infrastructure. This makes additions to the model extremely simple as data values stored in new object types can be made immediately visible to the rest of the modeling infrastructure, though the object-oriented model is not broken in the process. Fourth, Sesctherm is extensively commented, and nearly every algorithm is referenced in the code-base. The sequence of events Sesctherm follows for initialization can be seen in figure 2.7, while the sequence of events for each call to the thermal solver can be seen in figure 2.8.

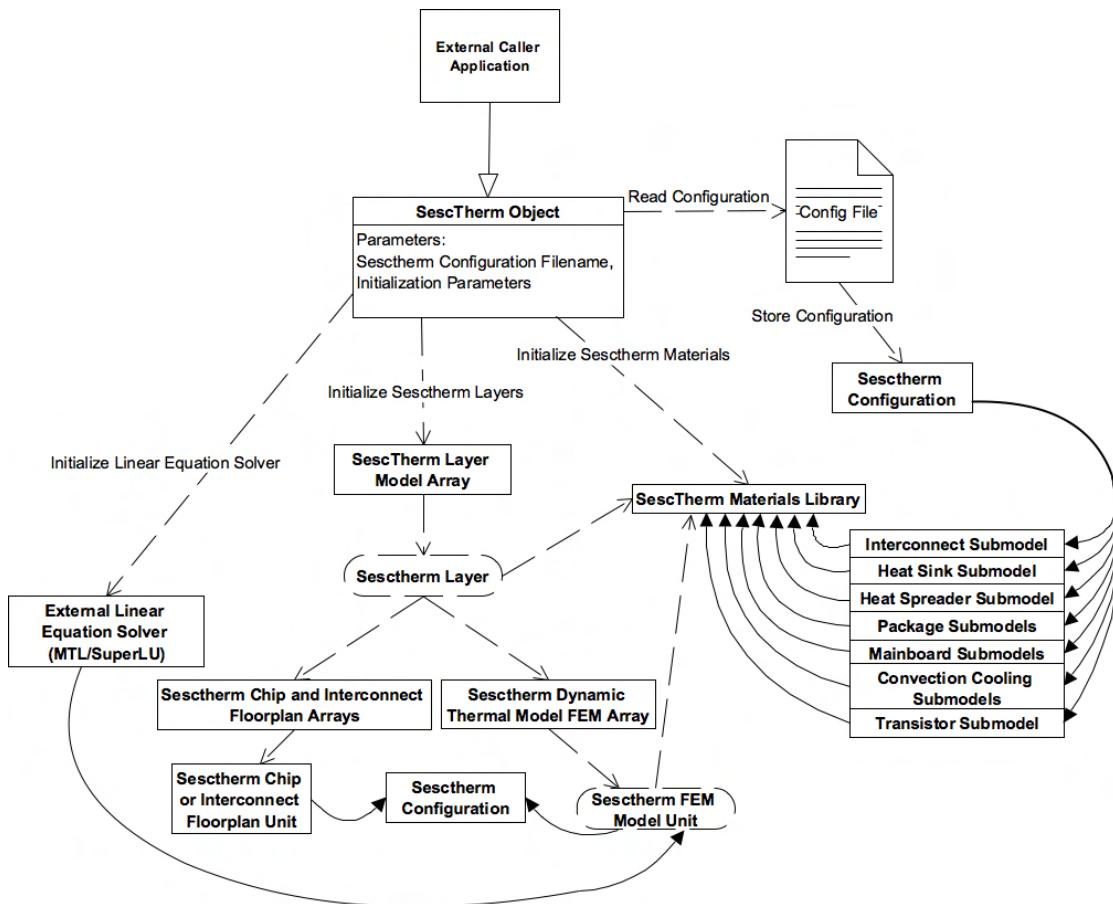


Figure 2.7: Sesctherm Initialization Algorithm Overview

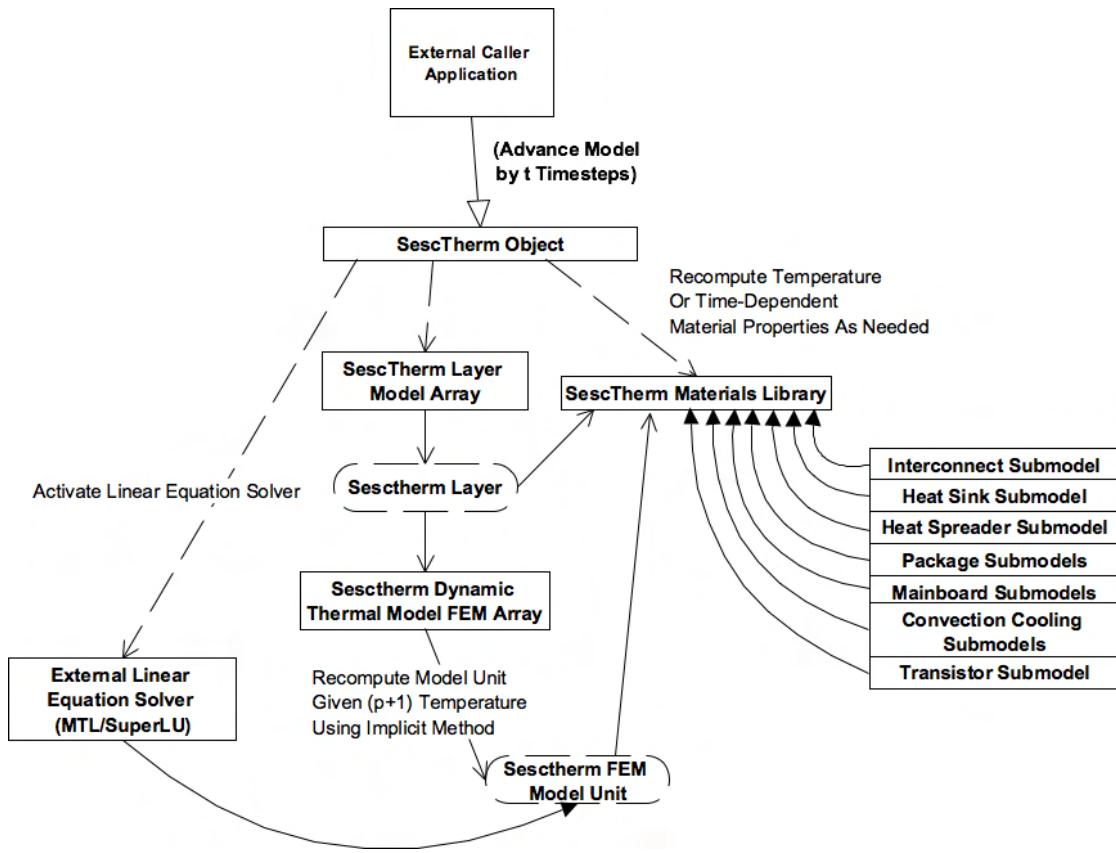


Figure 2.8: Sesctherm Thermal Solver Algorithm Overview

2.3.1 Superlu and Sparse Matrix Manipulation

The SuperLU package was chosen because it is highly optimized to solve sparse linear system of the type $AX=B$. In this case, A is a square, nonsingular matrix of size $n \times n$ while X and B are of dimensions $n \times b$, where there are b solution vectors. In this case, matrix A is of a highly symmetric nature and is diagonally dominant due to the nature of the thermal equations used. A simple example is shown below for the matrices generated for four temperatures nodes in a two-dimensional environment.

As can be seen, the sparse matrix X holds the coefficients for the left-hand side of the temperature equations. Each row in the matrix corresponds to one equation for one of the temperature nodes. Each of the entries in the column corresponds to the coefficient for one of the temperatures node variables within one equation. Since there are n nodes, there are n equations, within n coefficients in each equation (some of the coefficients may be zeroes).

Once the sparse matrix is generated, it is stored in Harwell-Boeing format. To improve performance, once the matrix is allocated, it is never deallocated. Further, indexing operations can be very costly for sparse matrix updates. To improve performance, a pointer is kept for each element of the sparse matrix. When any updates are performed to the model, pointers are dereferenced and values are stored indirectly to memory. This same pointer mechanism is used to swap matrixes X and B for each iteration of the model. This prevents costly memory copies and dramatically improves performance.

SuperLU uses LU decomposition with partial pivoting. Further, it can perform forward or back substitutions. We perform column reordering to improve sparsity in the matrix. This dramatically reduces the runtime. We found that a minimum degree ordering on the matrix structure $A\hat{T}+A$ was highly efficient. Once ordered, the matrix is symbolically factored. The SuperLU factorization algorithm uses graph reduction techniques to improve the performance of the factorization. Further, SuperLU optimizes cache hits through various architectural tuning parameters.

2.4 Performance

As analytical solutions to transient temperature problems are restricted to simple model geometries and boundary conditions, complex systems of the kind that Sesctherm models precludes the use of these simple analytical solutions. Instead, finite-difference methods are explored of the kind described in the preceding sections. While a variety of finite-difference solvers have been developed with varying degrees of performance, Sesctherm attempts to find a compromise between accuracy and performance [135, 72, 136].

There are essentially three phases of the Sesctherm execution. The first is an $O(n^2)$ operation, where n is the number of model nodes, that involves the initial synthesis of model materials, memory allocation, creation of the necessary finite-difference equation, and initialization of the various sub-models and linear system solvers. This largest component of this first execution phase is take up by Gaussian elimination with

partial pivoting by SuperLU [67]. Using amortized analysis, the second phase of the model requires $O(n * [i \bmod k])$ operations, where n is the number of model nodes, i is the number of model iterations, and k is the material re-computation rate (in units of 1/iterations). This phase of the model involves the re-computation of temperature and time-dependent material properties. This also involves re-computation of equation coefficients that are dependent upon the model time-step. Depending upon the level of model accuracy desired, this re-computation may be delayed by a variable number of time-steps. The third phase of the model involves solving the linear system and requires $O(n^2 * i)$ operations, where n is the number of model nodes and i is the number of model iterations. This third portion of the execution takes substantially longer than either or the first two.

As can be seen in figure 2.9, there is apparently nearly linear correlation between the number of nodes and the per-iteration over the range of nodes chosen. This is even the case even when the initialization time is amortized over the length of the runtime of the sample for the number of iterations chosen. The number of nodes is an exponential function of the model granularity. This is the reason for the exponential relationship between model granularity and per-iteration runtime that can be seen in figure 2.10.

It can further be seen in figure 2.11 that at less than 1mm granularity, Sesetherm can actually predict the temperature distribution within the chip faster than the time period it is modeling. Stated simply, Sesetherm can accurately model the temperature distribution faster than how the same temperature distribution would develop

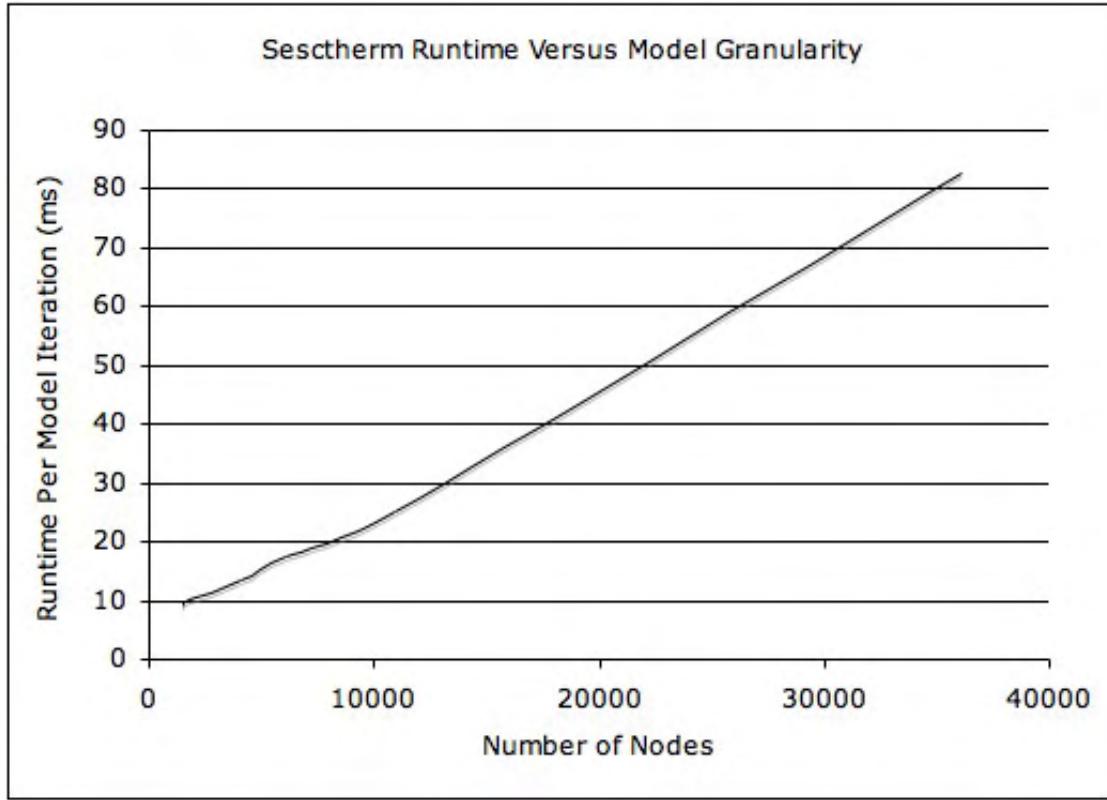


Figure 2.9: Sesctherm Model Performance as a Function of Number of Temperature Nodes

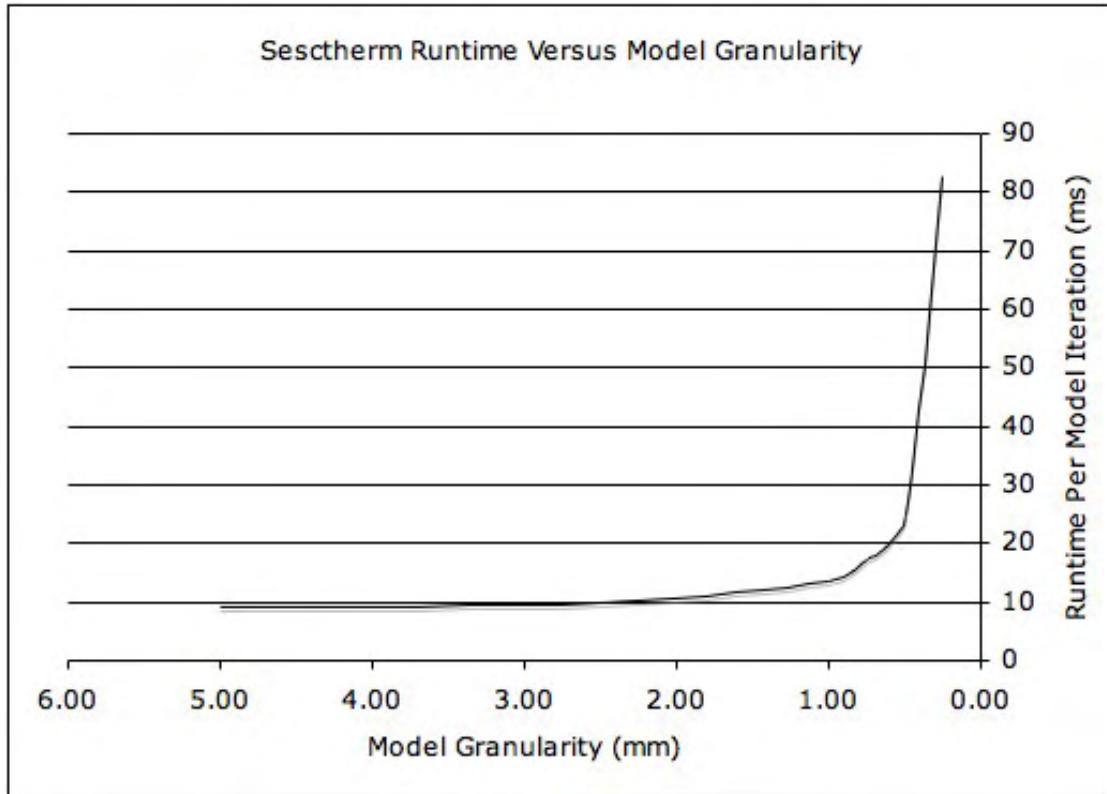


Figure 2.10: Sesctherm Model Performance as a Function of Model Temperature Granularity

Simulation Runtime As A Fraction of Simulated Time Period Versus Model Granularity

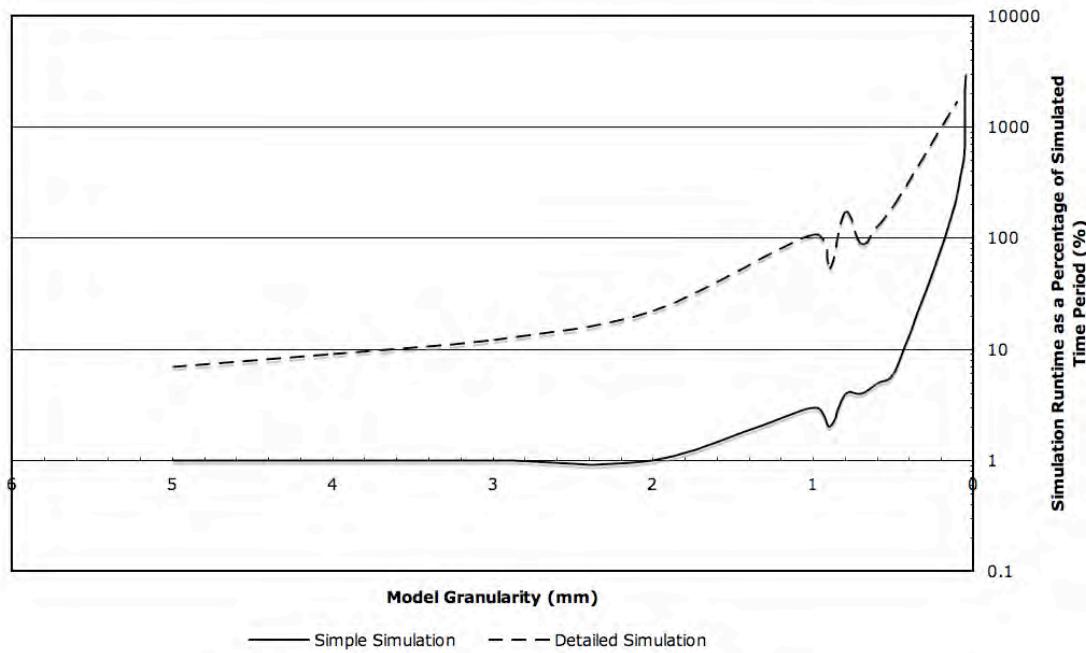


Figure 2.11: Sesctherm Model Simulation Time (shown as a Fraction of the Simulated Time Period) as a Function of Model Temperature Granularity

under real life conditions. This presents new possibilities for accuracy temperature modeling for runtime thermal management.

Although beyond the scope of this analysis, one can imagine that given the relatively slow temperature response seen here, there may be ample time for the operating system to handle thermal management strategies given the fact that any sys-call can be assumed to respond on the order of $10ms$. This opens up a discussion regarding whether complex, costly hardware dynamic-thermal-management strategies may be necessary. Further, given the inherently cyclic nature of processor operations, any thermal management strategies could likely be predicted based upon previous phases of software execution. This is considered future work.

2.5 Materials Modeling

2.5.1 Introduction

One of the most challenging aspects of thermal modeling is providing the thermal modeling infrastructure an accurate representation of geometry and thermal characteristics of the various materials used in the fabrication of a given IC design. Even if the thermal modeling infrastructure supports a variety of different material parameters, including time and temperature dependence, most designers will not be easily able to reliably predict the distribution of materials at the early phases of the design cycle. However, even if thermal simulation is to be employed late in the design cycle, when it may be too late to avoid a costly redesign, it may still be prohibitively

difficult. The reason for this is that even with a completed GDSII design file, it may still be difficult to acquire the necessary parameters from semiconductor fabrication facilities as many of the parameters are covered under patent – and may not even be readily available in technology libraries.

Despite these inherent limitations, the most serious limitation is actually the fact that many designers may have only limited knowledge about a final chip design at the early stages of the design cycle – when thermal simulation may have optimal financial benefit. At this early stage of the design phase, there may be limited knowledge of the design layout. This means that only very general predictions about the design layout may be possible. This lack of circuit-level specific knowledge of the kind that is typically required for most thermal simulations will ultimately limit their overall value to the designer.

For this reason, many thermal simulations rely on ITRS data to provide a statistically representative approximation for the final technology parameters used. Using this technology data, layer “smearing” is used to approximate the lumped (averaged) material properties of a complex distribution of materials that make up a given region of chip design. The most common example of this is for a wiring layer with a complex metal distribution where the entire layer is approximated with a single set of material properties. This is done to handle the complexity of providing an FEM mesh at a sufficiently high level of granularity to model the material distribution. Without these lumped layer properties, thermal simulation run-times would become prohibitively costly.

Unfortunately, while useful for certain applications, ITRS technology data may not have the degree of accuracy necessary to provide an accurate prediction of the thermal properties of a final circuit design. Many of the ITRS parameters are based upon simple heuristics that are designed primarily to provide industry with a realistic technology road-map. However, they are not intended for realistic approximations of the technology parameters for a full design.

Even if accurate technology data were used, many modeling tools use an incorrect averaging technique to determine the effective thermal conductivity of a given material distribution [31]. These tools will simply compute a weighted average of the thermal conductivities of a given materials layer based upon a rough approximation of the percentage of each material used. These approximations are usually made possible through further heuristics, applied to ITRS data. However, these weighted averaging techniques neglect critically important aspects of the material distribution that may change the overall thermal behavior of a given region of the chip [31].

Sesctherm attempts to ameliorate these problems using a combination of statistical techniques, material sub-models, and technology data taken from structural analysis reports of a variety of IC designs to provide a more representative approximation for the material properties – without requiring the full circuit layout. This allows circuit designers to gain critical insight into the final thermal properties of a given design at an early design phase without resorting to naive approximations of the material properties of the given design.

Sesctherm models 12 different types of material layers that most designers will

typically encounter in a given design. A typical layer “stack” can be seen in figure 2.12. Depending upon the level of accuracy desired, designers can adopt varying degrees of accuracy for each of these model layers. Further, the Sesetherm library makes it easy to incorporate new material types.

Rather than computing a single lumped set of material properties for each material layer, Sesetherm employs a different methodology. Each model layer supports unique thermal conductivities in all six directions – both lateral and vertical. This means that a given thermal model unit within this layer can have six unique thermal conductivities defined. Further, these properties are defined based upon a layer “floor-plan”. This “floor-plan” is of the same type used to define regions of power generation within the chip. This means that material properties can change freely within a material layer – they need not be the same. Further, each thermal property is allowed to evolve as a function of temperature and time.

Rather than using simple heuristics to compute the material distribution in a given layer, Sesetherm provides a balance between configurability on the part of the designer and automated material generation. Instead of enforcing a static material distribution based upon fabrication technology and overall geometry dependent heuristics, Sesetherm encapsulates regions of the chip into sub-models, and Sesetherm distributes and interconnects these sub-models based upon the interconnect and transistor density distribution.

It has been observed that while many designers may have limited knowledge of the final circuit layout, a rough approximation of the design complexity for different

floor-plan blocks may be possible – even at an early phase of the design cycle. This could be little more than knowing which regions of a given chip are occupied by memories, floating-point units or otherwise. Using this rough approximation of the final circuit layout, Sesctherm allows designers to input specific information about the transistor or interconnect density for each floor-plan unit. Using this information, ITRS data (validated through analysis of structural analysis reports), a temperature-dependent material property library based upon online material libraries, published studies, and material handbooks, fabrication materials distributions based upon data taken from structural analysis reports, statistical interconnect models, and material sub-models, the Sesctherm materials infrastructure synthesizes material properties for each of the 12 different material layers currently supported. In the following sections, we describe a subset of the material models developed. The remaining models are a straightforward implementation of the models described in [13].

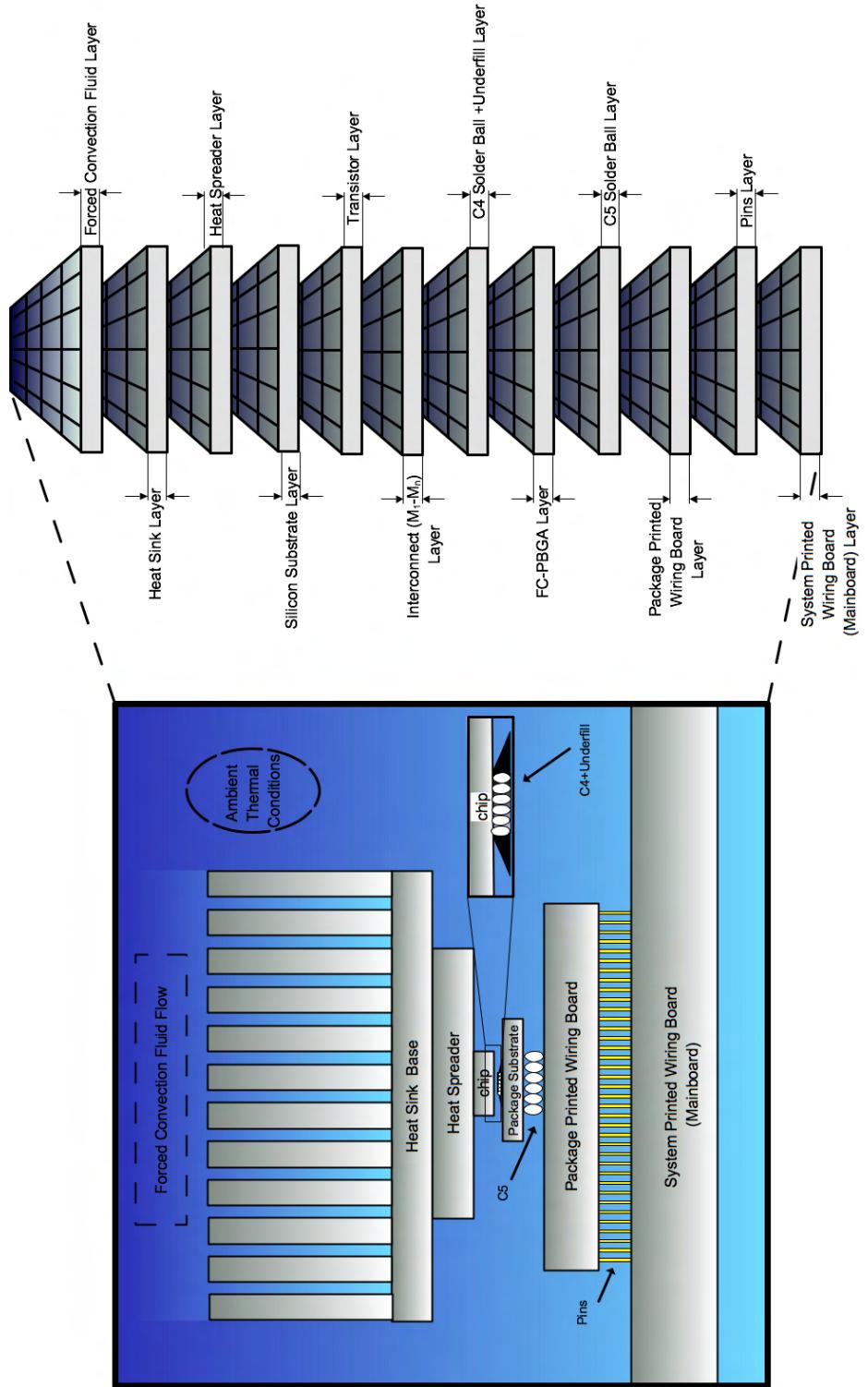


Figure 2.12: Sample Layer Stack for Flip-Chip Pin Grid Array-Type Package Assembly

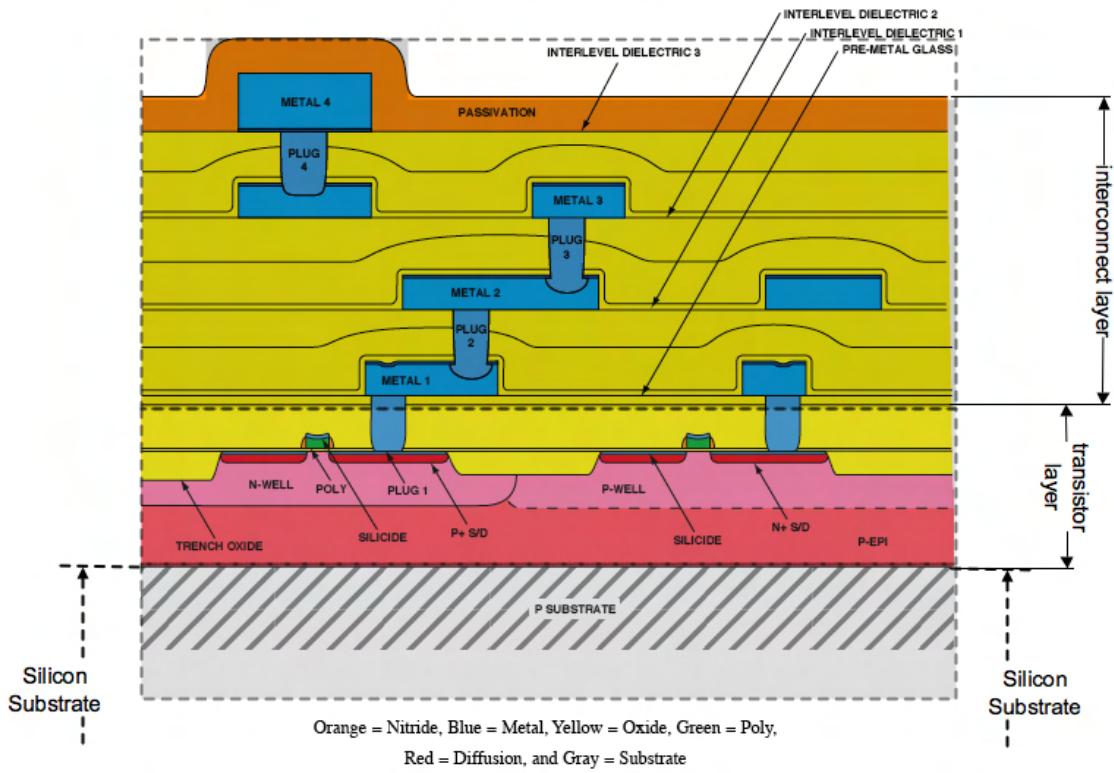


Figure 2.13: Silicon Substrate, Transistor and Interconnect Layers Side-view Diagram

2.5.2 Via Modeling

Seschtherm models two different types of vias. The first via type is modeled after the micro-scale via contacts used either as transistor contact plugs or metal interconnect vias used within a given semiconductor design. The first via type can be fabricated using a variety of the metal deposition methods common to modern semiconductor fabrication technologies. The second via type is used for the chip package printed wiring board or system-level printed wiring board. These vias, shown in figure 2.14 are designed using

micro-drilling technologies. A small drill bit will generate a circular hole where a variety of re-flow techniques can be used to provide a metal plating to the via.

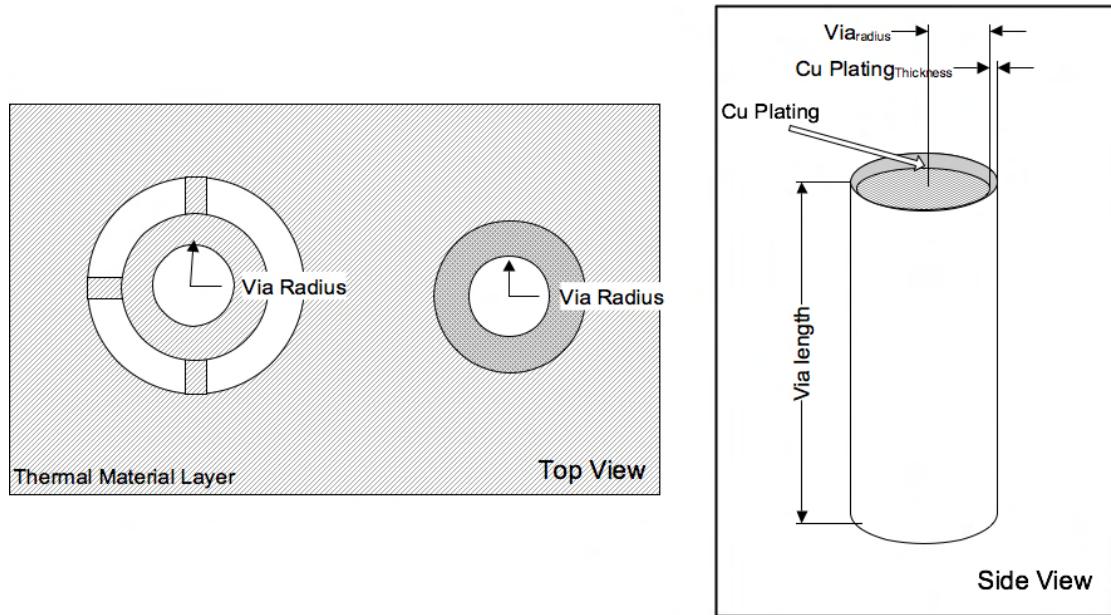


Figure 2.14: Top View and Side View of Via Dimensions

The vertical heat flow through the via is directly proportional to the cross-sectional area of the metal cylinder that can be used to model the via. In the case of the first via, a solid metal cylinder is modeled. The thermal resistance in the case of the first via is therefore equal to $\frac{l_{via}}{k_{metal}\pi(\text{radius}_{via})^2}$. Similarly, the second via is modeled as a hollow cylinder of thickness equal to the plating thickness of the via. This can be seen in equation (2.23).

$$R_{\text{via}} = \frac{l_{\text{via}}}{k\pi (\text{radius}_{\text{via}}^2 - (\text{radius}_{\text{via}} - T_{\text{plating}})^2)}$$

where R_{via} =the via's thermal resistance (K/W)

$$k = \text{the thermal conductivity of Cu (W/mK)} \quad (2.23)$$

$\text{radius}_{\text{via}} = 2 * \text{the via drill diameter}$

T_{plating} =the cu plating of the via (m)

l_{via} =the via length

The lateral heat flow through the first via can be described by figure 2.15. The lateral heat flow is computed by simplifying the cylinder into a quadrilateral, where the height is equal to the thickness of the via, and the height and width are equal to the diameter of the via. The solid metal cylinder modeled for the via is surrounded by inter-layer dielectric material. The lateral heat flow is computed by integrating all one-dimensional heat flows of thickness dx through both the inter-layer dielectric and metal via materials. The closed-form expression for the effective thermal conductivity of this via is shown in equation (2.24).

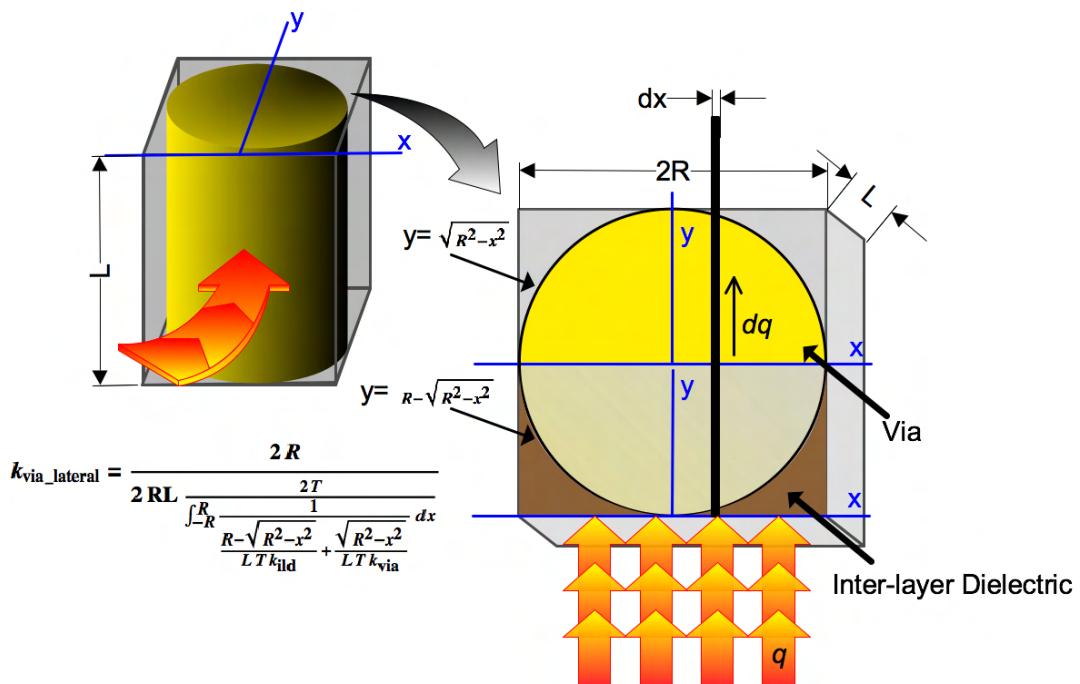


Figure 2.15: Lumped Via Lateral Thermal Conductivity(W/mK) is Computed by Integrating All One-Dimensional Heat Flow Laterally Through Via and Inter-Layer Dielectric (See Equation(2.24))

$$k_{\text{via_lateral}} = \frac{2R}{2RL \int_{-R}^R \frac{1}{\frac{R-\sqrt{R^2-x^2}}{L\Delta T k_{\text{ild}}} + \frac{\sqrt{R^2-x^2}}{L\Delta T k_{\text{via}}}} dx}$$

Assume: $k_{\text{via}} > k_{\text{ild}} > 0 \wedge R > 0 \wedge L > 0$

$$k_{\text{via_lateral}} = \frac{k_{\text{via}} \left(\pi k_{\text{ild}}^2 - 2\pi k_{\text{via}} k_{\text{ild}} + \left(2 \tan^{-1} \left(\frac{k_{\text{via}} - k_{\text{ild}}}{\sqrt{-k_{\text{ild}}(k_{\text{ild}} - 2k_{\text{via}})}} \right) + \pi \right) k_{\text{via}} \sqrt{-k_{\text{ild}}(k_{\text{ild}} - 2k_{\text{via}})} \right)}{2(k_{\text{ild}}^2 - 3k_{\text{via}} k_{\text{ild}} + 2k_{\text{via}}^2)}$$

where: x = horizontal data-point along center of via cross-section

k_{via} = Thermal Conductivity of Via Material (W/mK)

k_{ild} = Thermal Conductivity of Inter-layer Dielectric Material (W/mK)

R = Radius of Via (m)

L = Length of Via (m)

T = Temperature Change Across Via Laterally (K)

(2.24)

Surprisingly, the effective lateral thermal conductivity (W/mK) of the via is actually independent of the radius of the via. Figure 2.16 shows the effect of the thermal conductivities of the metal and the inter-layer dielectric on the effective, lateral thermal conductivity of the via. By replacing the solid metal cylinder with a hollow metal cylinder of thickness equal to the plating thickness, the lateral thermal conductivity can similarly be described for the second via type.

2.5.3 Printed Wiring Board Modeling

The printed wiring board model models heat flow both laterally and vertically through each of the material layers of the main-board. An equivalent lateral and vertical thermal conductivity is synthesized for each of these material layers. Finally, a lumped lateral and vertical thermal conductivity is generated based upon the series and parallel

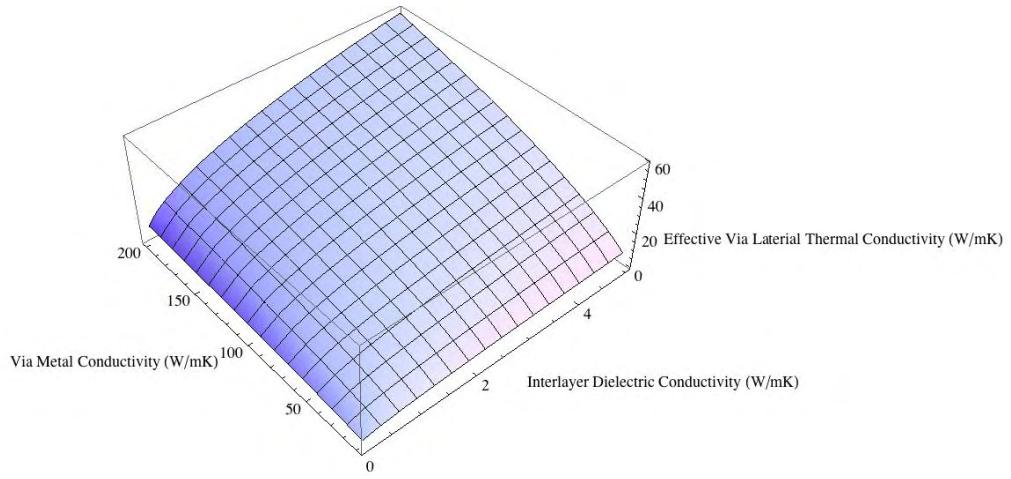


Figure 2.16: Lumped Via Lateral Thermal Conductivity(W/mK) as a Function of Bulk Thermal Conductivities(W/mK) of Inter-layer Dielectric and Via Metal Material

heat flow paths as is shown in figure 2.18 . See equations (2.25) and (2.26).

The printed wiring board model is based upon the work of Nelson et al [85]. A uniform probability density function is generated for the metal interconnect length and spacing distribution in the x and y lateral directions, and fraction of possible via sites that are occupied. See table 2.5.3 for details about the minimum and maximum length and spacing of the wires on each of the signal layers. Finite-element models compute the equivalent lateral and vertical thermal conductivities through each of these layers. The via density is considered in two cases: where 12.5% of the via sites are occupied and where 25% of the via sites are occupied. Table 2.1 describes the dimensions of the dielectric layers and copper traces. A visualization of these layers can be seen in figure 2.17, courtesy Nelson, Richardson [85]. Table 2.5.3 describes some common main-board layer types, and their lateral/vertical thermal conductivities. It should be noted that

the specific heat of the various layers is taken as a straight weighted sum of the specific heats of the various based upon their respective masses. The Future work on this model includes includes modeling non-plated tru-vias, different statistical wiring distributions, different wiring materials, and different dielectric materials.

Material	Dimension (mm)
Cu Wire Width	.2
Cu Wire thickness	.025
Dielectric Layer Thickness	.15
Cu Via Diameter	.2
Cu Via Plating Thickness	.025

Table 2.1: Wire and Dielectric Dimensions Used For PWB Model Generation

Signal Layer	Length _{min}	Length _{max}	Spacing _{min}	Spacing _{max}
Signal 1	3.6	7.2	.6	3.6
Signal 2	7.2	14.4	.6	3.6
Signal 3	7.2	14.4	3.6	7.2
Wired P/G 1	3.6	7.2	.6	3.6
Wired P/G 2	7.2	14.4	3.0	6.0

Table 2.2: Min and Max Metal Wire Lengths and Spacing For Each Layer Type (mm)

$$k_{\text{lateral}} = \frac{\sum_{l=1}^L k_l * \text{Area}_l}{\sum_{l=1}^L \text{Area}_l}$$

where k_{parallel} = the effective lateral thermal conductivity of the printed wiring board for L layers (2.25)

k_l = the thermal conductivity of the l^{th} material layer

Area_l = the area of the l^{th} material layer(length * width)

Layer Type	25% Via Density		12.5% Via Density	
	K_{vertical}	K_{lateral}	K_{vertical}	K_{lateral}
Signal 1, Solid P/G	1.56	13.5	.863	18.8
Signal 2, Solid P/G	1.58	14.8	.872	20.3
Signal 3, Solid P/G	1.55	12.4	.855	17.9
Signal 1, Wired P/G 1	1.55	5.91	.857	6.25
Signal 2, Wired P/G 2	1.57	7.56	.867	0.00

Table 2.3: Effective Vertical and Lateral Conductivities For Four-Layer Main-board Sub-model With Two Signal and Two Power Layers

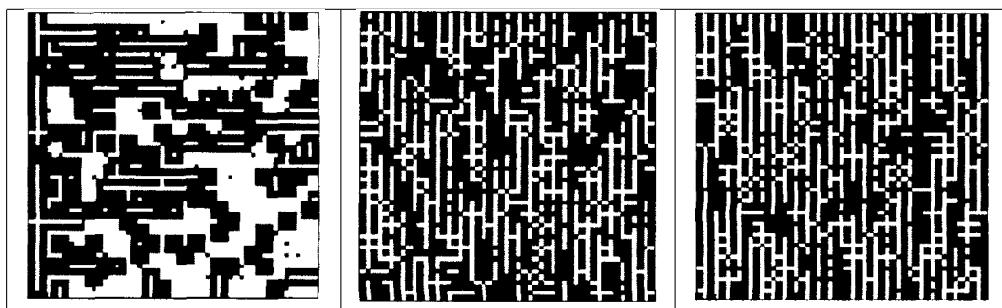


Figure 2.17: Visualization of (a) Wired P/G 2 (b) Signal 1 (c) Signal 2

$$k_{\text{vertical}} = \frac{\sum_{l=1}^L \text{thickness}_l}{\sum_{l=1}^L \frac{\text{thickness}_l}{k_l}}$$

where k_{vertical} = the effective thermal conductivity of the printed wiring board for L layers (2.26)

thickness_l = the thickness of the l^{th} material layer

k_l = the thermal conductivity of l^{th} material layer

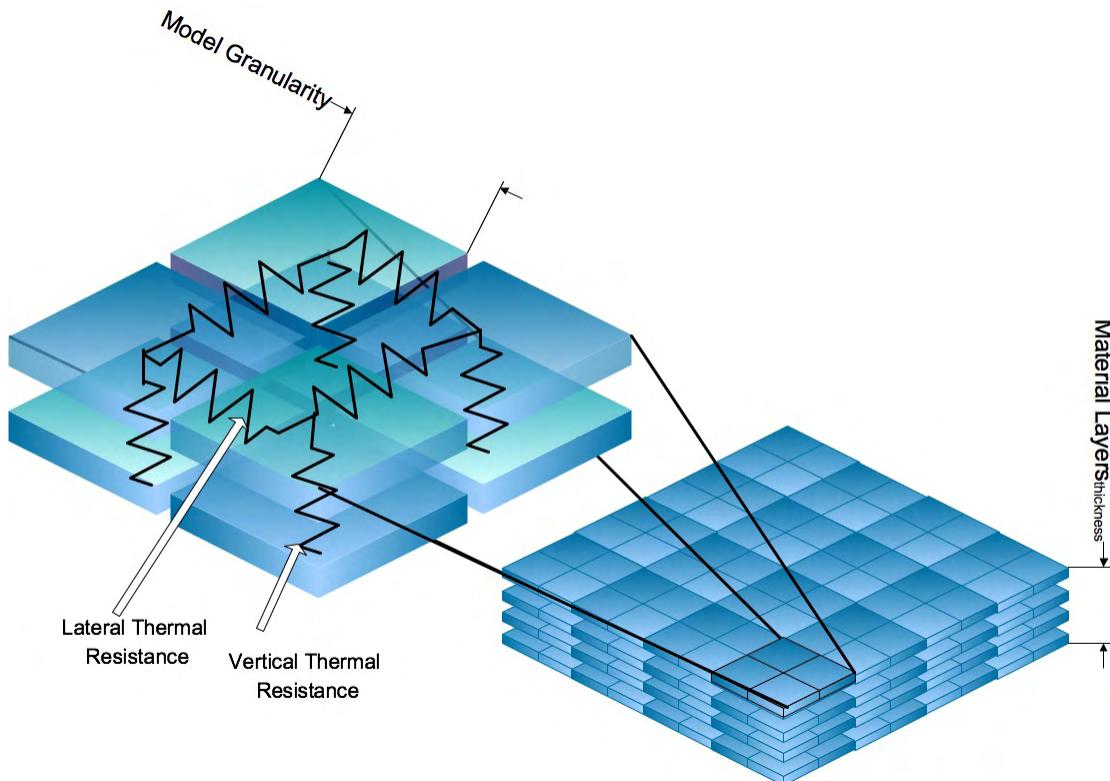


Figure 2.18: Each Model Materials Layer May Include Temperature/Time-Dependent Lateral and Vertical Conductivities

2.5.4 Interconnect Modeling

2.5.4.1 Introduction

The thermal characteristics of various metal interconnect layers within an IC can vary highly depending upon the given design [51, 85]. For this reason, many thermal simulators general equivalent (lumped) material thermal conductivities and heat capacitances are based upon a simple weighted sum of the respective masses of the various materials within a giving metal interconnect layer [31, 51, 85, 109]. However, this technique cannot exploit the thermal characteristics of a given wiring distribution within a given interconnect layer.

Depending upon the metal distribution within a given metal layer, heat pathways can vary in different regions of the layer. Further, due to the Manhattan routing methodology that is typically employed, thermal conductivity is usually biased in the direction of the interconnect routing for a given layer. This is largely due to the fact that the thermal conductivity of the copper or aluminum interconnects is three order of magnitude greater than the interlayer dielectric that electrically insulates the wires from each other. This means that each wire acts like a heat “pipe”, while the inter-layer dielectric surrounding the wire acts as thermal insulation. Further, heat flow will flow vertically through metal vias almost exclusively.

The effect that wiring density distribution has upon the thermal properties of the interconnect layers can be seen in figure 2.21. As can be seen in this thermal image, taken of an AMD Athlon processor, heat will propagate most rapidly along the

interconnect clock distribution. Further, self-heating of interconnect wiring changes the power density distribution of the design. Where the a clock tree can now take over 10% of the total power utilization for a given design, the effect of the self-heating of interconnect wires, as described in equation 2.27, can no longer be neglected.

$$P_{\text{interconnect}} = I_{\text{interconnect}}^2 R_{\text{interconnect}} = \frac{\rho_o L}{Wt}$$

where $P_{\text{interconnect}}$ = interconnect trace power dissipation (W)

$I_{\text{interconnect}}$ = interconnect trace current (A)

$R_{\text{interconnect}}$ = interconnect electrical resistance (Ohms) (2.27)

ρ_o = resistivity of interconnect metal material (Ohm-m)

L = length of interconnect trace (m)

W = width of interconnect trace (m)

t = thickness of interconnect trace (m)

To model these characteristics, Sesctherm extends the previous work of several authors [131, 89, 80, 61, 45, 42, 39, 8, 40, 41, 81]. There are three separate parts of this interconnect model. The first part involves modeling the statistical interconnect distribution across each of the interconnect layers. The second part involves modeling the interlayer-dielectric materials that make up the metal layers. The third part is the creation of an electro-thermal sub-model with many different interconnect layers. This is a single material layer with lumped lateral conductivities, vertical conductivities, density, and specific heat.

As can be seen in figure 2.19, the interconnect structure in many designs is highly regular. This highly regular structure allows reliable thermal characterization of these layers. However, the interconnect density may vary significantly across a given design. Sesctherm therefore attempts to capture the highly regular nature of the interconnect distribution, while allowing for variations in the interconnect density distribution across the die.

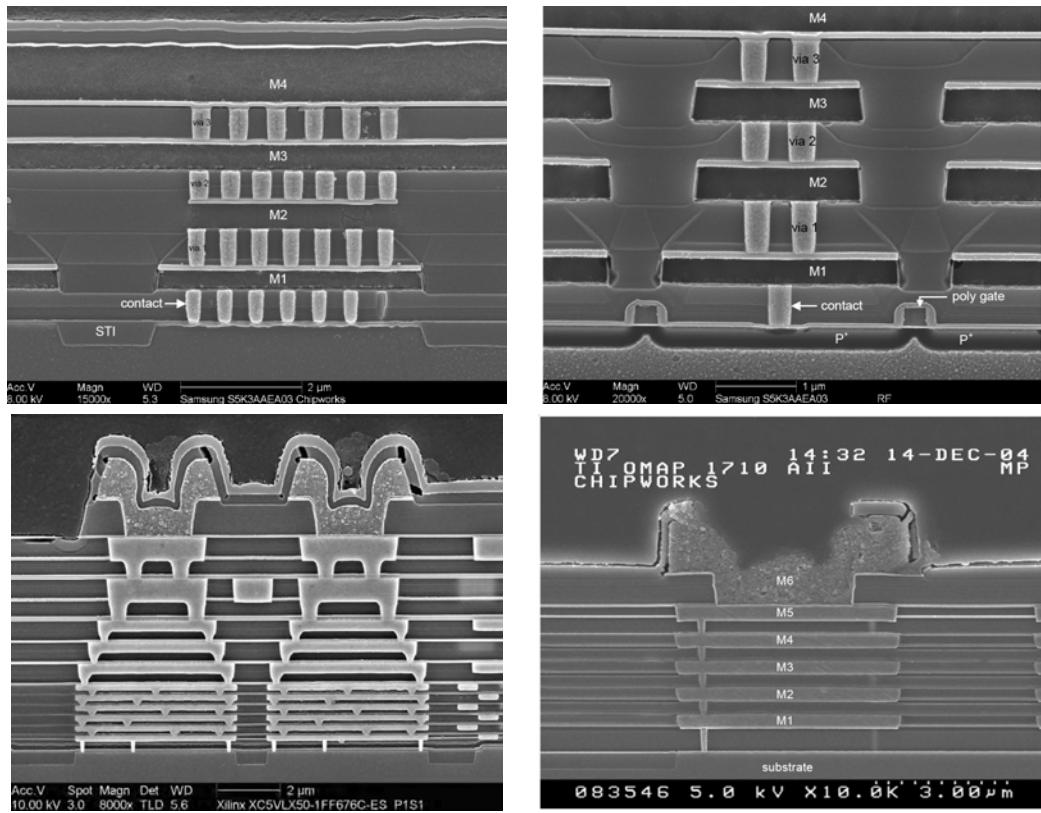


Figure 2.19: Interconnect Side-View of (a,b) Samsung S5K3AAEA03 (c) Xilinx Virtex™ 5 (d) TI OMAP 1710

Sesctherm uses a simple sub-model design that lumps layer materials. This can be seen in figure 2.23. In particular, the parallel heat flow through all the layer vias

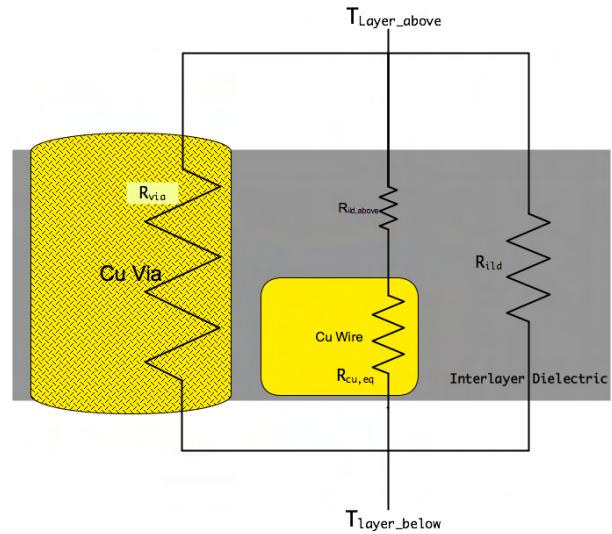


Figure 2.20: Metal Layer Sub-model Diagram

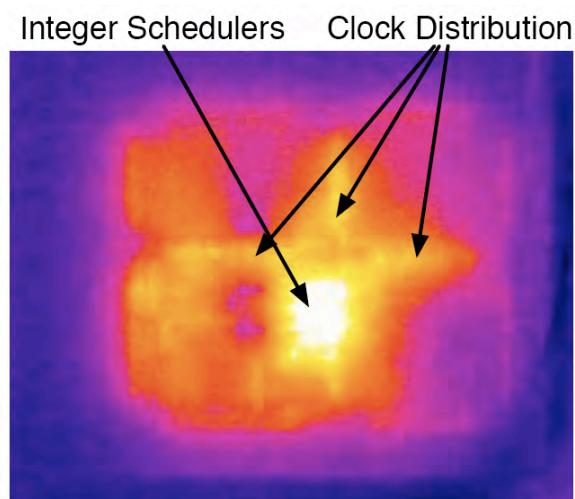


Figure 2.21: Thermal Image of Temperature Distribution Within AMD Athlon

is modeled as a single lumped thermal resistance. This is similarly done for the wiring and interlayer-dielectric materials.

2.5.4.2 Statistical Wire-length Distribution

To model the interconnect distribution for a given series of metal layers, Sesc-therm uses an a-priori stochastic interconnect density function [40]. The function, shown in equation (2.28), relates a given interconnect length to the number of interconnects of that particular length. The lengths are in gate pitches, where one gate pitch is equal to $\sqrt{\frac{A_m}{N_g}}$, where A_m is the area of the macro-cell (the floor-plan unit area) and N_g is equal the number of gates in the particular cell.

The stochastic interconnect distribution for three different designs is shown in figure 2.22. As can be seen, the number of interconnects of shorter length is exponentially greater than the number of greater length. This interconnect “density” function is used throughout the interconnect model.

Region I : $1 \leq l \leq \sqrt{N_g}$

$$i(l) = \frac{\alpha k}{2} \Gamma \left(\frac{l^3}{3} - 2\sqrt{N_g}l^2 + 2N_g l \right) l^{2p-4}$$

Region II : $\sqrt{N_g} \leq l \leq 2\sqrt{N_g}$

$$i(l) = \frac{\alpha k}{2} \Gamma \left(2\sqrt{N_g} - l \right)^3 l^{2p-4}$$

where l = interconnect length in gate pitches $(l = \sqrt{A_m/N_g})$, A_m = floor-plan logic area

N_g = number of logic gates (2.28)

p = rent's exponent(0.6)

k = rents coefficient(4)

α = fraction of sink thermals in the logic area(.75, $\alpha = f.o. / (f.o. + 1)$, $f.o.$ = 3for3 – inputNAND)

Γ = normalizing factor such that

$$\Gamma = \frac{2N_g (1 - N_g^{p-1})}{\left(-N_g^p \frac{1+2p-2^{2p-1}}{p(2p-1)(p-1)(2p-3)} - \frac{1}{6p} + \frac{2\sqrt{N_g}}{2p-1} - \frac{N_g}{p-1} \right)}$$

2.5.4.3 Metal Layer Wire Assignment

Once the wiring distribution has been formed, Sesetherm must determine which wires will be routed on each metal layer. This is done following the work of Davis et al. In particular, wires are assigned to virtual interconnect layers called “tiers”. Each tier is then mapped to one or more physical metal layers. Sesetherm assigns metal layers to tiers such that, if possible, an equal number of metal layers will be assigned to each tier. Further, Sesetherm models each “interconnect” floor-plan unit separately, allowing the wiring density to vary across the die.

Sesetherm assumes that the metal layers involve three tiers. The first tier is for local interconnects, where each interconnect is shorter than the length of the chip. The second, intermediate, tier may include either local or global interconnects. The

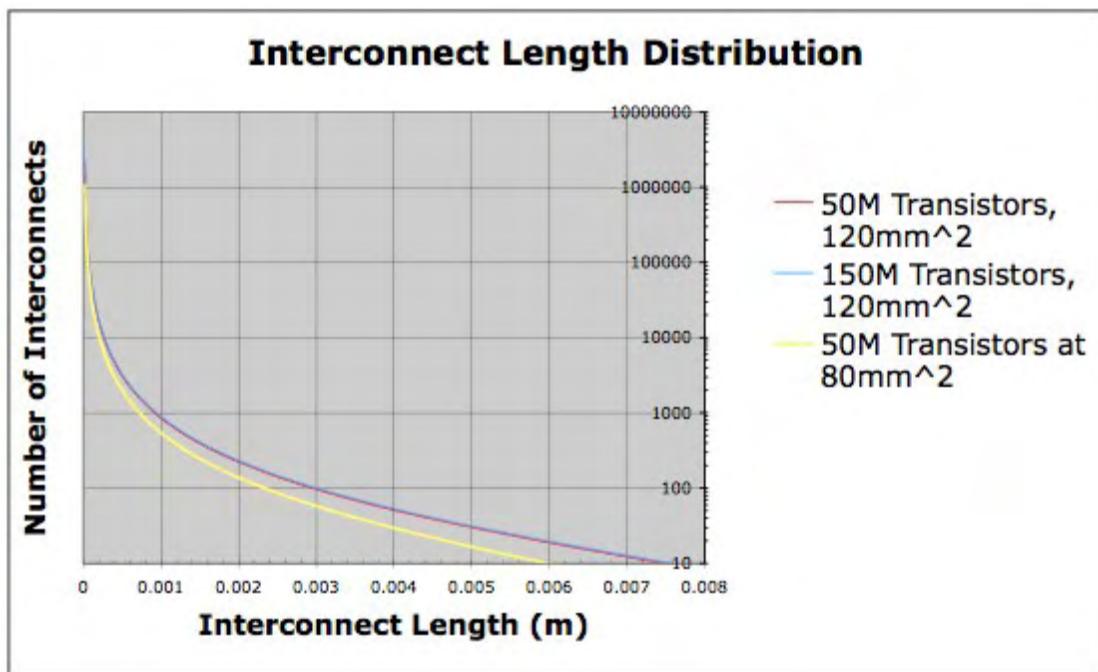


Figure 2.22: Wire-length Distribution for Several Sample Chips

third global tier is used for global interconnect routing.

In order to determine which interconnects are placed on each tier, Sesctherm divides the interconnect distribution defined in equation (2.28) into three segments. The segments are divided such that the longest interconnect in the first tier will be considered the shortest interconnect in the second tier and so forth. Using this methodology, it is only necessary to determine which interconnect length will be considered a maximum for a given tier.

To determine the maximal interconnect lengths for each tier, Sesctherm must first approximate both the available die real-estate available for routing and the required routing area that the interconnect network uses for a network of given length. By equating the available and required routing area, Sesctherm can determine the maximum interconnect length for each tier. This can be seen in equation (2.29). However, the maximum interconnect length for a given tier must also satisfy timing requirements. To ensure this, Sesctherm computes a resistance-capacitance time delay for the longest interconnect in a given tier. Further, Sesctherm requires that this time delay be some fraction of the cycle time [41]. In doing so, the interconnect network for a given tier is assured to meet timing constraints, while simultaneously meeting routing area requirements. The computation of the resistance-capacitance time constant is done following equation (2.34). The effective interconnect capacitance is computed following diagram 2.23.

If maximum length of the global interconnect is assumed to be equal to the length of the chip, while the minimum length of the local interconnect is assumed to be

twice the minimum feature size, then the total length of each interconnect tiers is given by equations (2.30). A complete discussion of these equations is beyond the scope of this study. A complete analysis can be found in the work of Davis et al. and Venkatesan et al. [40, 41, 131].

Rather than model the interconnect distribution for the chip as a whole, Sesetherm models the interconnect distribution for each floor-plan unit separately. This allows Sesetherm to model the varying interconnect wiring density across the die. To vary the interconnect density, a user-specific scalar is applied to scale the interconnect pitch. Constraints are imposed so as to avoid exceeding the available routing area.

$$A_{\text{available}} = n_t e_w A_m = \chi p_t \sqrt{\frac{A_m}{N_g}} \int_{L_{t-1}}^{L_t} l i(l) dl = A_{\text{required}}$$

where n_t = number of metal layers in the t^{th} tier

e_w = the wiring efficiency factor

p_t = the average wiring pitch in the t^{th} tier(um), (this is initially $2F$)

F = feature size for all other layers where the wiring pitch determined by the delay computation

L_t = the longest interconnect length in the t^{th} tier(in gate pitches)

$i(l)$ = is the interconnect density function

(2.29)

$$A_{\text{local tier}} = 2F \sqrt{\frac{A_m}{N_g}} L_{\text{local tier}}$$

where $L_{\text{local tier}} = \chi \int_1^{L_{\text{local}}} li(l) dl$

$$L_{\text{local}} = \frac{4F^2}{4(2.2)\rho\epsilon_r\epsilon_o 6.08} \sqrt{\frac{N_g}{A_m}} \left[-\frac{\sqrt{\epsilon_r}}{c_o} + \sqrt{\frac{\epsilon_r}{c_o^2} + 4\beta_{\text{local}} \frac{4.4\rho\epsilon_r\epsilon_o 6.08}{4F^2 f_{\text{cycle}}}} \right]$$

$$A_{\text{semi tier}} = 11.56F \sqrt{\frac{A_m}{N_g}} L_{\text{semi tier}}$$

where $L_{\text{semi tier}} = \chi \int_{L_{\text{local}}}^{L_{\text{semi}}} li(l) dl$

$$L_{\text{semi}} = \frac{11.56F^2}{4(2.2)\rho\epsilon_r\epsilon_o 6.08} \sqrt{\frac{N_g}{A_m}} \left[-\frac{\sqrt{\epsilon_r}}{c_o} + \sqrt{\frac{\epsilon_r}{c_o^2} + 4\beta_{\text{semi}} \frac{4.4\rho\epsilon_r\epsilon_o 6.08}{11.56F^2 f_{\text{cycle}}}} \right]$$

$$A_{\text{global tier}} = 4 \left(\frac{A_m \sqrt{N_g}}{N_g} \right) \sqrt{\frac{1.1\rho\epsilon_r\epsilon_o 6.08}{\left(\frac{\beta_{\text{global}}}{f_{\text{cycle}}} - 2\sqrt{\frac{A_m}{N_g} \sqrt{N_g} \frac{\sqrt{\epsilon_r}}{c_o}} \right)}} L_{\text{global tier}}$$

where $L_{\text{global tier}} = \chi \int_{L_{\text{semi}}}^{2\sqrt{N}} li(l) dl$

(2.30)

where F is the minimum feature size

A_m is the macro-cell area

N_g is the number of gates

ρ is the resistivity of interconnect material

ϵ_r is the relative dielectric constant

ϵ_o is the electric constant

c_o is the speed of light in free space

f_{cycle} is the cycle frequency

β_t is a fraction of the cycle frequency for tier t

χ is a conversion factor to convert point-to-point interconnect length to a net length

There are several areas of possible improvement to the statistical interconnect

model. First, three interconnect tiers are assumed in the Sesetherm model. This should be extended to support n-tiers. The work of Venkatesan et al, describes an assignment methodology that permits a variable number of tiers [131]. However, due to the fact that the equations used do not permit closed-form solutions, numerical analysis must be used to solve the equations. Second, the resistance-capacitance (RC) time delay of the longest interconnect for each tier is simplified to provide a closed-form solution. This simplification is that all cross-sectional dimensions (W,T,S,etc) are all considered to be equal to half the wiring pitch. This should be extended as shown in equations (2.32),(2.31),(2.33) to support variable dimensions. Third, the interconnect model neglects the effects of repeater insertion on the wiring delay of the longest interconnect in each tier. The work of Venkatesan et al. describes a methodology for computing wiring delays based upon an optimal repeater insertion methodology. Fourth, the time delay on the local tier is determined to be 25 percent of the clock period, while the remaining tiers are 90 percent of the clock period. However, a more realistic delay metric should be used. Fifth, the wire driver resistance is assumed to match the total line resistance. However, a realistic measure of the driver resistance should be modeled. Sixth, the model now relies upon a tier segmentation strategy that assumes a delay, and not area limited design. Seventh, accurate modeling of router efficiency and vias blockage should be performed. This is not currently considered. Eighth, interconnect density is now scaled linearly based upon a user-specified scalar. This should be implemented by reducing the wiring pitch in addition to scaling the number of transistors in the floor-plan unit. The work of Venkatesan et al. describes a methodology for simultaneously

targeting given area and timing constraints. This is considered future work.

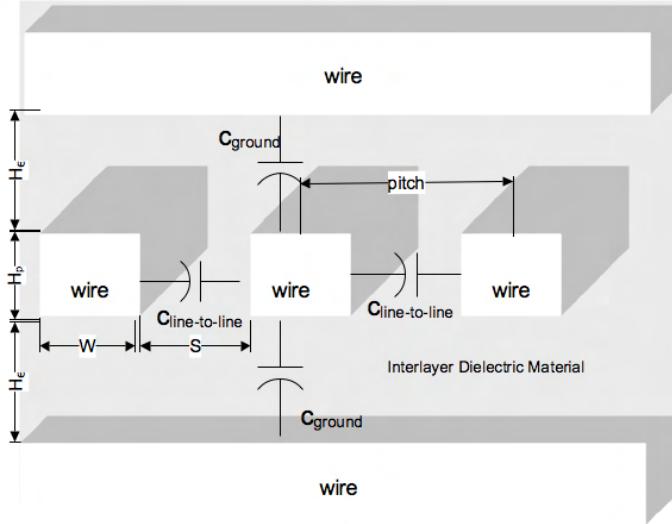


Figure 2.23: Interconnect Sub-model Diagram

$$\begin{aligned}
 c_{\text{ground}} = & 1.086 \left(\frac{H_\rho}{H_\epsilon} \right)^{0.337} \left(\frac{S}{S + 2H_\epsilon} \right)^{0.0476} \left(-0.9964e^{-\frac{SH_\epsilon}{1.42}} + 0.685e^{-\frac{H_\rho}{1.343S}} + 1 \right) \\
 & + \frac{W\epsilon_0\epsilon_r}{H_\epsilon} 1.086 \left(\frac{H_\rho}{H_\epsilon} \right)^{0.337} \left(\frac{S}{S + 2H_\epsilon} \right)^{0.0476} \\
 & * \left(0.685e^{-\frac{0.7446016381236039H_\rho}{S}} - 0.9964e^{-0.7042253521126761SH_\epsilon} + 1 \right) + \frac{W\epsilon_0\epsilon_r}{H_\epsilon} \quad (2.31)
 \end{aligned}$$

$$\begin{aligned}
c_{\text{line-to-line}} = & 1.722 \left(1 - 0.6548 e^{-\frac{W}{0.3477 H_\epsilon}} \right) e^{-\frac{S}{0.651 H_\epsilon}} \\
& + \frac{1}{S} \left(1.302 e^{-\frac{H_\epsilon}{0.082 S}} - 0.1292 e^{-\frac{H_\rho}{1.326 S}} - 1.897 e^{-\frac{H_\epsilon}{0.31 S} - \frac{H_\rho}{2.474 S}} + 1 \right) \\
& * H_\rho \epsilon_0 \epsilon_r 1.722 \left(1 - 0.6548 e^{-\frac{2.876042565429968 W}{H_\epsilon}} \right) e^{-\frac{1.5360983102918586 S}{H_\epsilon}} \\
& + \frac{1}{S} \left(-1.897 e^{\frac{0.4042037186742118 H_\rho}{S} - \frac{3.2258064516129035 H_\epsilon}{S}} + 1.302 e^{-\frac{12.195121951219512 H_\epsilon}{S}} \right. \\
& \left. - 0.1292 e^{-\frac{0.7541478129713424 H_\rho}{S}} + 1 \right) H_\rho \epsilon_0 \epsilon_r
\end{aligned} \tag{2.32}$$

$$c_{\text{line}} = 2c_{\text{ground}} + 2c_{\text{line to line}}$$

$$\begin{aligned}
c_{\text{line}} = & 2 \left(1.086 \left(\frac{H_\rho}{H_\epsilon} \right)^{0.337} \left(\frac{S}{S + 2H_\epsilon} \right)^{0.0476} \right. \\
& * \left(0.685 e^{-\frac{0.7446016381236039 H_\rho}{S}} - 0.9964 e^{-0.7042253521126761 S H_\epsilon} + 1 \right) + \frac{W \epsilon_0 \epsilon_r}{H_\epsilon} \Big) \\
& + 2 \left(1.722 \left(1 - 0.6548 e^{-\frac{2.876042565429968 W}{H_\epsilon}} \right) e^{-\frac{1.5360983102918586 S}{H_\epsilon}} \right. \\
& + \frac{1}{S} \left(-1.897 e^{\frac{0.4042037186742118 H_\rho}{S} - \frac{3.2258064516129035 H_\epsilon}{S}} \right. \\
& \left. \left. + 1.302 e^{-\frac{12.195121951219512 H_\epsilon}{S}} - 0.1292 e^{-\frac{0.7541478129713424 H_\rho}{S}} + 1 \right) H_\rho \epsilon_0 \epsilon_r \right)
\end{aligned}$$

where N_g = number of gates

A_m = logic area, floor-plan block area (m^2)

W = metal width (m)

H_ρ = metal thickness (m)

S = metal spacing (m)

H_ϵ = dielectric thickness above and below metal (m)

ϵ_o = electrical constant

ϵ_r = dielectric constant

c_o = speed of light (m/s)

ρ = metal resistivity (Ohm/m)

(2.33)

If we assume that $W = H_\rho = H_\epsilon = S = \frac{P_t}{2}$ then equation (2.33) simplifies to:

$$\tau = \frac{\beta}{f_c} = 4 * \frac{1.1\rho\epsilon_r\epsilon_o6.2A_m}{p_t^2 * N_g} L_t^2,$$

solving for p_t :

$$p_t = 2\sqrt{\frac{1.1\rho\epsilon_r\epsilon_o f_c}{\beta}} \sqrt{\frac{A_m}{N_g}} L_t \quad (2.34)$$

2.5.4.4 Inter-Layer Dielectric Modeling

One of the problems with accurate thermal simulation is that many material physical properties are not readily available. Specifically, while obtaining the dielectric constant for a particular technology node is made readily available through ITRS to a reasonable approximation, obtaining the thermal conductivity for that dielectric material is not readily available. While the thermal conductivity of several dielectrics has been determined from material databases and structural analysis reports, many frequently used inter-layer dielectric materials lack published data on the thermal properties of the materials. These materials include xerogel, carbon-doped oxide (CDO), methylsilsesquioxane (MSQ), fluorinated silicate glass (FSG), hydrogen-silsesquioxane (HSQ) and others [53].

To obtain a reasonable approximation, the dielectric constant and thermal conductivity of the inter-layer dielectric can be found for a porous dielectric material. This is an application of the work of Im et al [53]. The Bruggemann effective medium theory model (see equation (2.35)) relates the porosity of a given material, the dielectric

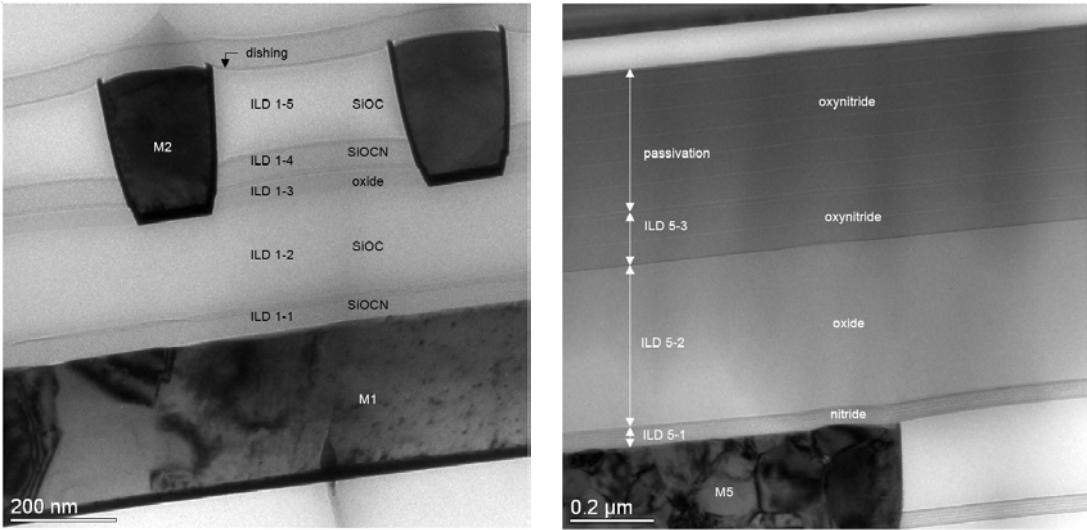


Figure 2.24: (a) TI OMAP1710 Metal 1 Inter-Layer Dielectric Materials (b)TI OMAP1710 Metal 5 Inter-Layer Dielectric Materials and Passivation

constant of the matrix material, the dielectric constant of the pores, and the dielectric constant of the inter-layer dielectric. Therefore, if the dielectric constants are known, the porosity of the material can be determined. Once the porosity is known, the thermal conductivity can be determined through porosity-weighted dilute medium model [53] (see equation (2.36)). If these two equations are solved simultaneously, equation (2.37) is obtained. Sesctherm uses a combination of known thermal parameters and equation (2.37) to determine the thermal conductivity of a given inter-layer dielectric. Graphs of the relationship between the porosity, solution to the Bruggemann effective medium theory equation and the porosity weighted simple medium model are shown in figure 2.25. The relationship between the dielectric constant and thermal conductivity for Xerogel and Fluorinated Silicate Glass (FSG) is shown in figure 2.26.

$$P \left(\frac{k_{\text{pores}} - k_{\text{ild}}}{k_{\text{pores}} - 2k_{\text{ild}}} \right) + (1 - P) \left(\frac{k_{\text{matrix}} - k_{\text{ild}}}{k_{\text{matrix}} - 2k_{\text{ild}}} \right) = 0$$

where P is the porosity ($0 < P < 1$)

$$k_{\text{ild}}$$
 is the dielectric constant of the interlayer dielectric material (2.35)

k_{pores} is the dielectric constant of pores

k_{matrix} is the dielectric constant of matrix matrix

$$K_{\text{ild}} = [\text{PK}_{\text{pores}} + (1 - P)K_{\text{matrix}}] (1 - P^a) + \left(\frac{K_{\text{pores}} K_{\text{matrix}} P^a}{\text{PK}_{\text{matrix}} + (1 - P)K_{\text{pores}}} \right)$$

where P is the porosity ($0 < P < 1$)

K_{ild} is the thermal conductivity of the inter-layer dielectric

K_{pores} is the thermal conductivity of pores

K_{matrix} is the thermal conductivity of matrix matrix

a is a fitting parameter

(2.36)

Solving Equations (2.35) and (2.36) Simultaneously:

$$\begin{aligned} K_{\text{ild}} = & -\frac{1}{k_{\text{ild}} (k_{\text{matrix}} - k_{\text{pores}})} \left(\left(-\frac{(k_{\text{ild}} - k_{\text{matrix}})(2k_{\text{ild}} - k_{\text{pores}})}{k_{\text{ild}} (k_{\text{matrix}} - k_{\text{pores}})} \right)^a - 1 \right) \\ & ((2k_{\text{ild}} - k_{\text{matrix}})(k_{\text{ild}} - k_{\text{pores}})K_{\text{matrix}} - (k_{\text{ild}} - k_{\text{matrix}})(2k_{\text{ild}} - k_{\text{pores}})K_{\text{pores}}) - \\ & \frac{k_{\text{ild}} (k_{\text{matrix}} - k_{\text{pores}}) K_{\text{matrix}} K_{\text{pores}} \left(-\frac{(k_{\text{ild}} - k_{\text{matrix}})(2k_{\text{ild}} - k_{\text{pores}})}{k_{\text{ild}} (k_{\text{matrix}} - k_{\text{pores}})} \right)^a}{(k_{\text{ild}} - k_{\text{matrix}})(2k_{\text{ild}} - k_{\text{pores}})K_{\text{matrix}} - (2k_{\text{ild}} - k_{\text{matrix}})(k_{\text{ild}} - k_{\text{pores}})K_{\text{pores}}} \end{aligned} \quad (2.37)$$

Although Sesctherm refers to a single inter-layer dielectric material, there may

**Solving The Bruggemann Effective Medium Theory Equation and
Porosity Weighted Simple Medium Model Equation Simultaneously
Through Regression**

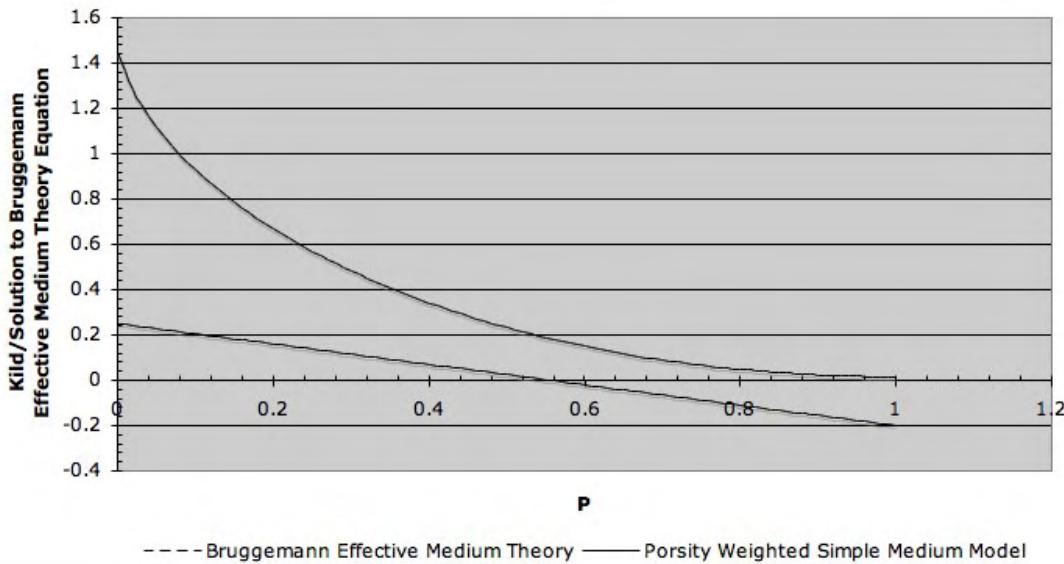


Figure 2.25: To solve the Bruggemann Effective Medium Theory Equation and Porosity Weighted Simple Medium Model Equation simultaneously, a linear regression is performed on the Bruggemann Effective Medium Theory Equation to find the x-intercept. The PWSM is then evaluated for this value of P.

actually me several different dielectric materials used within a given layer – as can be seen in Figure 2.24. To determine the effective interlayer dielectric, an equivalent thermal resistance is found based upon the same methodology used to find the effective lateral and vertical thermal conductivities of the printed wiring board layer (see above).

To find the effective specific heat and density of the various materials, we assume that the specific heat and density do not deviate significantly from the matrix materials. While not entirely correct, this provides a reasonable approximation for the materials used. A more accurate characterization of the specific heat and density of the

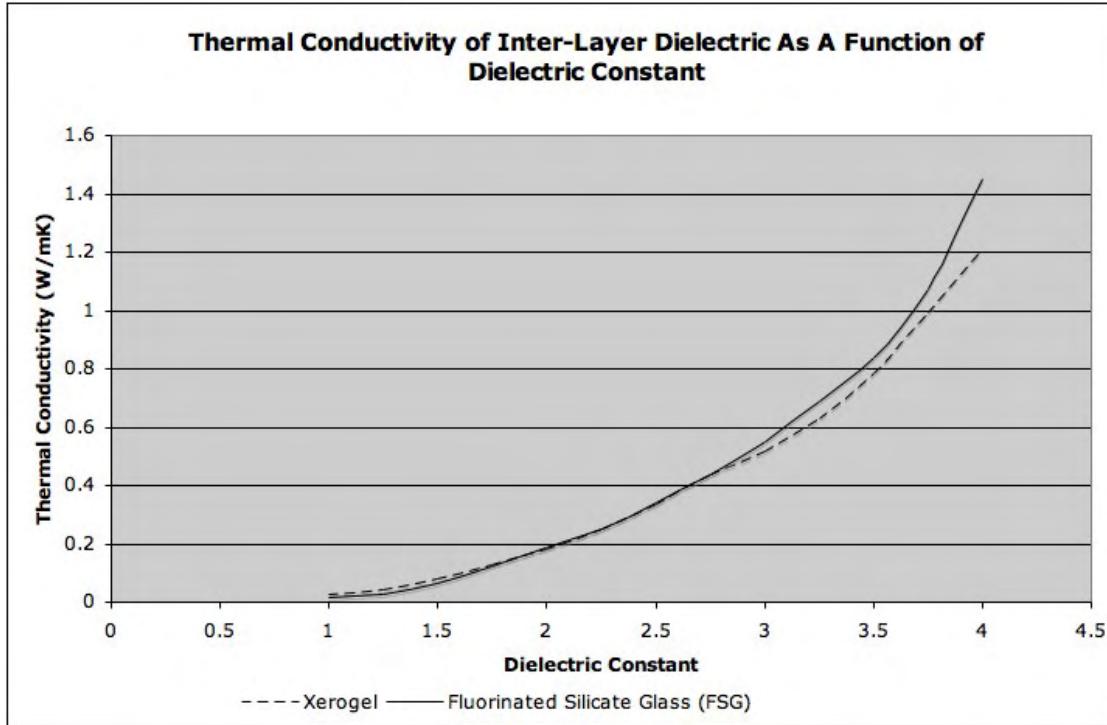


Figure 2.26: Relationship between Dielectric Constant of the Inter-layer Dielectric and the Thermal Conductivity of that Material For Xerogel and Fluorinated Silicate Glass (FSG)[38, 53]

specific inter-layer dielectric materials is in the realm of future work.

To determine the lumped specific heat and density where multiple inter-layer dielectric materials are used, a weighted average by mass is performed. This is reasonable given the fact that each floor-plan unit is assumed to have a uniform material distribution. However, a statistical material distribution model for the purpose of characterizing the dielectric material distribution within a given layer is left for future work.

2.5.4.5 Unified Interconnect Model

Sesctherm creates a stochastic interconnect distribution sub-model for each floor-plan unit. Once this sub-model is created, the model is translated into a lumped electro-thermal model for each floor-plan unit. The electro-thermal model for each floor-plan unit therefore models the heat flow in all the metal layers for that cross-sectional region of the chip.

Heat flow is modeled laterally and vertically. Lateral heat flow is separately modeled both parallel and perpendicular to the routing direction of the interconnects. Density and specific heat computation is performed as a simple weighted average by mass of the density and specific heats of the respective materials within each modeling layer.

In all the equations used, $\int_{L_{\min}}^{L_{\max}}$ is considered the total length of all the interconnects for that particular layer, where L_{\min} is considered the shortest interconnect for that particular layer, and L_{\max} is considered the longest interconnect for that particular layer. These boundaries are determined based upon equations (2.30).

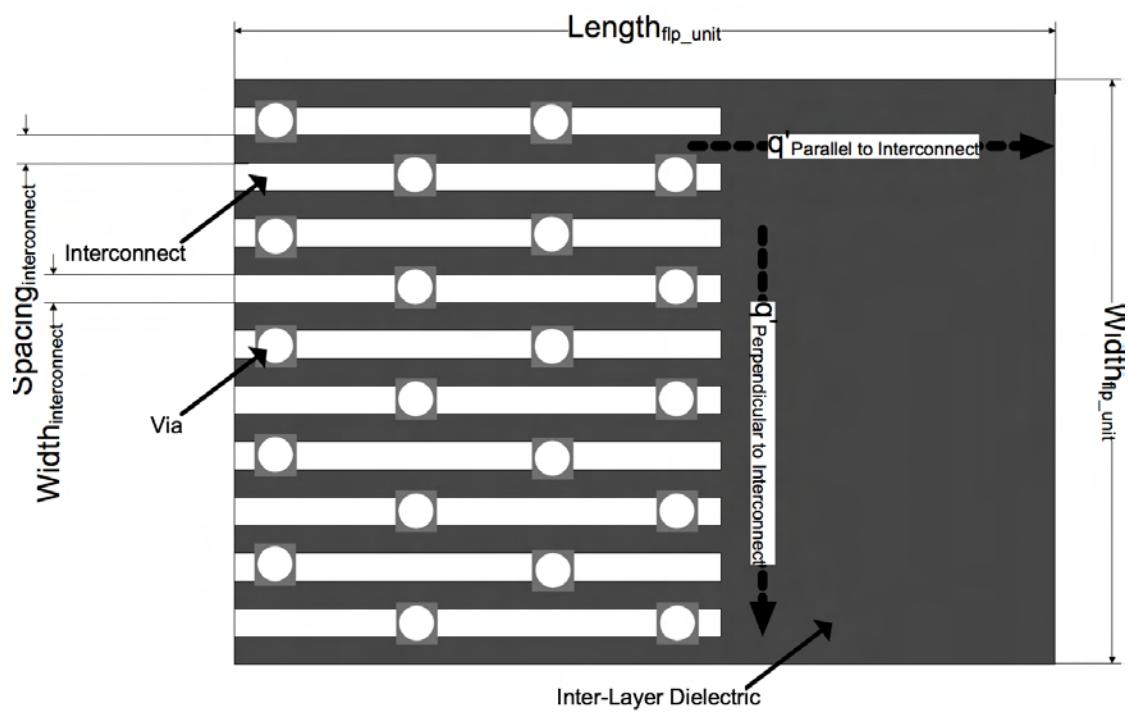


Figure 2.27: Diagram For Electrothermal Model Design of Interconnect Layer

In order to determine the lateral heat flow parallel to the direction of interconnect routing, we assume that a simplified Manhattan routing methodology is used where all the interconnects are routed in the same direction. This simplification may be reasonable given the nature of increasingly restrictive design rules depending upon the chosen technology. However, a more representative modeling methodology that does not depend upon this assumption may improve accuracy. This is considered future work.

Assuming that all wires are routed in the same direction, heat flow through the interconnects is modeled as a parallel electro-thermal circuit. Similarly, heat flow through the inter-layer dielectric between the interconnects is modeled as a parallel circuit. A via efficiency factor, e_{via} is used to describe the average number of vias for each interconnect. To model heat flow above the interconnect, a series/parallel circuit is generated that models the lateral heat flow through both the vias and inter-layer dielectric material, where the lateral thermal conductivity of the vias is determined by equation (2.24). A similar analysis is performed to model heat flow laterally in the direction perpendicular to the routing direction of the interconnects. Equations (2.38) and (2.39) describe the effective electro-thermal resistance laterally across the interconnect layer, parallel to the routing of the interconnect. Equations (2.40) and (2.41) describe the effective electro-thermal resistance laterally across the interconnect layer, perpendicular to the routing of the interconnect. Equations (2.42) and (2.43) describe the effective electro-thermal resistance vertically through the interconnect layer.

There are many possible improvements to the methodology used here to lump the complex interconnect distribution into an effective one-dimensional thermal resis-

tance both laterally and vertically. In particular, thermal “fringing” effects cause the heat flow between interconnects laterally and vertically to be inherently non-linear in nature. Closed form expressions have been developed that describe the heat flow between interconnects to a high degree of precision [16]. These can be seen in equations (2.44).

The most accurate means for characterizing the thermal properties of the interconnect layers involve the creation of a full finite-element sub-model (FEM) [11]. Using a full FEM, the model is able to capture the true thermal behavior of the thermal system without any of the inaccuracies inherent in the simplifications Sesctherm performs. While there may be value in such an approach, this was eschewed for a simpler approach to avoid the costly memory and performance penalties inherent in the implementation of FEM models. Most importantly, the current methodology is sufficiently fast to permit recompilation of temperature or time-dependent, lumped material properties during runtime. Had full FEM models been chosen, runtime re-computation of lumped material parameters would have had a significant performance penalty. However, there could still be value in the dual use of FEM modeling and one-dimensional modeling to improve upon the current interconnect modeling methodology. This is considered future work.

$$\begin{aligned}
R_{\text{interconnect_lateral_parallel}} &= \frac{1}{\frac{\text{width}_{\text{fip_unit}}}{\text{pitch}_{\text{interconnect}}}} \left(\left(\frac{\left(\text{length}_{\text{fip_unit}} - \frac{\int_{L_{\min}}^{L_{\max}} li(l) dl}{\text{width}_{\text{fip_unit}} / \text{spacing}_{\text{interconnect}}} \right)}{(k_{\text{ild}} t_{\text{ild}} \text{spacing}_{\text{interconnect}})} \right) \right. \\
&\quad \left. \left\| \left(\frac{\frac{\int_{L_{\min}}^{L_{\max}} li(l) dl}{\text{width}_{\text{fip_unit}} / \text{pitch}_{\text{interconnect}}} - \frac{d_{\text{via}} \int_{L_{\min}}^{L_{\max}} e_{\text{via}} i(l) dl}{\text{width}_{\text{fip_unit}} / \text{pitch}_{\text{interconnect}}} + \frac{d_{\text{via}} \int_{L_{\min}}^{L_{\max}} e_{\text{via}} i(l) dl}{\text{width}_{\text{fip_unit}} / \text{pitch}_{\text{interconnect}}}}{k_{\text{interconnect}} t_{\text{interconnect}} \text{width}_{\text{interconnect}}} \right) \right\| \right. \\
&\quad \left. \left(\frac{d_{\text{via}} \int_{L_{\min}}^{L_{\max}} e_{\text{via}} i(l) dl}{\text{width}_{\text{fip_unit}} / \text{pitch}_{\text{interconnect}}} + \frac{\text{length}_{\text{fip_unit}} - \frac{d_{\text{via}} \int_{L_{\min}}^{L_{\max}} e_{\text{via}} i(l) dl}{\text{width}_{\text{fip_unit}} / \text{pitch}_{\text{interconnect}}}}{k_{\text{ild}} (t_{\text{ild}} - t_{\text{interconnect}}) d_{\text{via}}} \right) \right) \right) \\
&\quad \left. \left\{ R_{\text{ild_between_interconnects}} \right\} \right. \\
&\quad \left. \left\{ R_{\text{interconnect}} + R_{\text{via_between_interconnect}} \right\} \right. \\
&\quad \left. \left\{ R_{\text{via_above_interconnect}} + R_{\text{ild_above_interconnect}} \right\} \right) \right)
\end{aligned} \tag{2.38}$$

Simplified:

$$\begin{aligned}
R_{\text{interconnect_lateral_parallel}} &= \\
&\frac{k_{\text{interconnect}} k_{\text{via}} \text{spacing}_{\text{interconnect}} t_{\text{interconnect}} \text{width}_{\text{fip_unit}}}{\text{width}_{\text{fip}} / \left(\left(\int_{L_{\min}}^{L_{\max}} li(l) dl \right) k_{\text{via}} + \left(\int_{L_{\min}}^{L_{\max}} i(l) e_{\text{via}} dl \right) (k_{\text{interconnect}} \text{spacing}_{\text{interconnect}} - d_{\text{via}} k_{\text{via}}) \right)} + \\
&\frac{k_{\text{ild}} t_{\text{ild}} \text{width}_{\text{fip_unit}}^2}{\text{pitch}_{\text{interconnect}} \left(\frac{\text{length}_{\text{fip_unit}} \text{width}_{\text{fip_unit}} - \left(\int_{L_{\min}}^{L_{\max}} li(l) dl \right) \text{pitch}_{\text{interconnect}}}{\text{length}_{\text{fip_unit}} \text{width}_{\text{fip_unit}} - \left(\int_{L_{\min}}^{L_{\max}} li(l) dl \right) \text{pitch}_{\text{interconnect}}} + \right. \\
&\quad \left. \frac{k_{\text{ild}} (t_{\text{ild}} - t_{\text{interconnect}})}{\frac{\text{length}_{\text{fip_unit}}}{d_{\text{via}}} + \frac{\left(\int_{L_{\min}}^{L_{\max}} i(l) e_{\text{via}} dl \right) \text{pitch}_{\text{interconnect}} (k_{\text{ild}} (t_{\text{ild}} - t_{\text{interconnect}}) - k_{\text{via}} (t_{\text{via}} - t_{\text{interconnect}}))}{\text{width}_{\text{fip_unit}} k_{\text{via}} (t_{\text{via}} - t_{\text{interconnect}})}} \right) \right)
\end{aligned} \tag{2.39}$$

$$\begin{aligned}
R_{\text{interconnect_lateral_perpendicular}} = & \\
& \frac{\text{width}_{\text{fip}}}{\text{pitch}_{\text{interconnect}}} \left(\left(\frac{\text{spacing}_{\text{interconnect}}}{\left(k_{\text{ild}} t_{\text{ild}} \left(\text{length}_{\text{fip_unit}} - \frac{\int_{L_{\min}}^{L_{\max}} li(l) dl}{\text{width}_{\text{fip_unit}} / \text{pitch}_{\text{interconnect}}} \right) \right)} \right) \right. \\
& + \left. \left(\left(\frac{\text{width}_{\text{interconnect}}}{k_{\text{interconnect}} t_{\text{interconnect}} \frac{\int_{L_{\min}}^{L_{\max}} li(l) dl}{\text{width}_{\text{fip_unit}} / \text{pitch}_{\text{interconnect}}} - \frac{d_{\text{via}} \int_{L_{\min}}^{L_{\max}} e_{\text{via}} i(l) dl}{\text{width}_{\text{fip_unit}} / \text{pitch}_{\text{interconnect}}}} \right) \right) \right. \\
& \left. \left(\frac{d_{\text{via}}}{k_{\text{via}} t_{\text{interconnect}} \frac{d_{\text{via}} \int_{L_{\min}}^{L_{\max}} e_{\text{via}} i(l) dl}{\text{width}_{\text{fip_unit}} / \text{pitch}_{\text{interconnect}}}} \right) \right) \right. \\
& \left. \left(\frac{d_{\text{via}}}{k_{\text{via}} (t_{\text{via}} - t_{\text{interconnect}}) \frac{d_{\text{via}} \int_{L_{\min}}^{L_{\max}} e_{\text{via}} i(l) dl}{\text{width}_{\text{fip_unit}} / \text{pitch}_{\text{interconnect}}}} \right) \right) \\
& \left. \left(\frac{d_{\text{via}}}{k_{\text{ild}} (t_{\text{ild}} - t_{\text{interconnect}}) \left(\text{length}_{\text{fip_unit}} - \frac{d_{\text{via}} \int_{L_{\min}}^{L_{\max}} e_{\text{via}} i(l) dl}{\text{width}_{\text{fip_unit}} / \text{pitch}_{\text{interconnect}}} \right)} \right) \right) \right) \quad (2.40)
\end{aligned}$$

Simplified:

$$\begin{aligned}
R_{\text{interconnect_lateral_perpendicular}} = & \\
& \frac{1}{\text{pitch}_{\text{interconnect}}} \frac{\text{width}_{\text{fip}}}{\text{width}_{\text{fip}} \left(\frac{\text{spacing}_{\text{interconnect}}}{k_{\text{ild}} t_{\text{ild}} \left(\text{length}_{\text{fip_unit}} - \frac{\left(\int_{L_{\min}}^{L_{\max}} li(l) dl \right) \text{pitch}_{\text{interconnect}}}{\text{width}_{\text{fip_unit}}} \right)} \right)} - \\
& \left(d_{\text{via}} \text{width}_{\text{interconnect}} \text{width}_{\text{fip_unit}} \right) / \left(- \int_{L_{\min}}^{L_{\max}} li(l) dl d_{\text{via}} k_{\text{interconnect}} \text{pitch}_{\text{interconnect}} \right. \\
& t_{\text{interconnect}} - \text{length}_{\text{fip_unit}} \text{width}_{\text{interconnect}} \text{width}_{\text{fip_unit}} k_{\text{ild}} (t_{\text{ild}} - t_{\text{interconnect}}) + \\
& \left. \left(\int_{L_{\min}}^{L_{\max}} i(l) e_{\text{via}} dl \right) d_{\text{via}} \text{pitch}_{\text{interconnect}} (d_{\text{via}} - \text{width}_{\text{interconnect}} \right. \\
& \left. \left. (k_{\text{via}} t_{\text{interconnect}} - k_{\text{ild}} (t_{\text{ild}} - t_{\text{interconnect}}) + k_{\text{via}} (t_{\text{via}} - t_{\text{interconnect}}))) \right) \right) \quad (2.41)
\end{aligned}$$

$$\begin{aligned}
R_{\text{interconnect_vertical}} = & \frac{\left| \frac{t_{\text{ild}}}{k_{\text{ild}} \left(\text{width}_{\text{fip_unit}} * \text{length}_{\text{fip_unit}} - \text{width}_{\text{interconnect}} \left(\int_{L_{\min}}^{L_{\max}} (l - d_{\text{via}} e_{\text{via}}) i(l) dl \right) - d_{\text{via}}^2 \left(\int_{L_{\min}}^{L_{\max}} e_{\text{via}} i(l) dl \right) \right)} \right|}{\left| \frac{t_{\text{via}}}{k_{\text{via}} d_{\text{via}}^2 \int_{L_{\min}}^{L_{\max}} e_{\text{via}} i(l) dl} \right|} \\
& \left(\frac{t_{\text{ild}} - t_{\text{interconnect}}}{k_{\text{ild}} \left(\text{width}_{\text{interconnect}} \left(\int_{L_{\min}}^{L_{\max}} (l - d_{\text{via}} e_{\text{via}}) i(l) dl \right) \right)} + \frac{t_{\text{interconnect}}}{k_{\text{interconnect}} \left(\text{width}_{\text{interconnect}} \left(\int_{L_{\min}}^{L_{\max}} (l - d_{\text{via}} e_{\text{via}}) i(l) dl \right) \right)} \right) \quad (2.42)
\end{aligned}$$

Simplified:

$$\begin{aligned}
R_{\text{interconnect_vertical}} = & 1 / \left(\frac{\left(\int_{L_{\min}}^{L_{\max}} i(l) e_{\text{via}} dl \right) (d^2)_{\text{via}} k_{\text{via}}}{t_{\text{via}}} + \right. \\
& \frac{k_{\text{ild}} \left(\text{length}_{\text{fip_unit}} \text{width}_{\text{fip_unit}} - (d^2)_{\text{via}} \left(\int_{L_{\min}}^{L_{\max}} i(l) e_{\text{via}} dl \right) - \text{width}_{\text{interconnect}} \left(\int_{L_{\min}}^{L_{\max}} i(l) (l - d_{\text{via}} e_{\text{via}}) dl \right) \right)}{t_{\text{ild}}} \\
& \left. + \frac{1}{k_{\text{ild}} \left(\text{width}_{\text{interconnect}} \left(\int_{L_{\min}}^{L_{\max}} l i(l) dl - \text{DifferentialID}[l] i(l) d_{\text{via}} e_{\text{via}} \right) \right)} + \frac{t_{\text{interconnect}}}{k_{\text{interconnect}} \left(\text{width}_{\text{interconnect}} \left(\int_{L_{\min}}^{L_{\max}} i(l) (l - d_{\text{via}} e_{\text{via}}) dl \right) \right)} \right) \quad (2.43)
\end{aligned}$$

$$\begin{aligned}
k_{\text{coupling_wire_to_wire_lateral}} &= \frac{(s+w)\dot{q}}{\text{height}_{\text{layer}} t_{\text{layer}} T(\gamma - 1)} \\
k_{\text{coupling_wire_to_wire_vertical}} &= \frac{w^2 \left(k_d * 1.86 \frac{h_\epsilon}{w} \left[\log_{10} \left(1 + \frac{h_\epsilon}{w} \right) \right] - 0.66 \left(\frac{w}{t} \right)^{-0.1} \right)}{l * w} \\
k_{\text{M1_wire_to_substrate_vertical}} &= \frac{36.3 k_d s^{0.12} \left(1 + e^{\left(\frac{-w}{s \cdot 5t} \right)} \right) \left(\frac{2h_\epsilon+t}{h_\epsilon} \right)^{0.2t} \left(1 + \frac{0.88h_\epsilon}{36.3s^{0.12} \left(1 + e^{\left(\frac{-w}{s \cdot 5t} \right)} \right) \left(\frac{2h_\epsilon+t}{h_\epsilon} \right)^{0.2t}} \right)}{l} \\
k_{\text{M2_wire_to_substrate_vertical}} &= \frac{t_{\text{layer SW}} \left(k_d * 1.86 \frac{(2h_\epsilon+t)}{w} \left[\log_{10} \left(1 + \frac{(2h_\epsilon+t)}{w} \right) \right] - 0.66 \left(\frac{w}{t} \right)^{-0.1} \right)}{l * w * (2h_\epsilon + t)} \\
\gamma &= \frac{\ln \left(\frac{a_1+b_1}{a_2+b_2} \right)}{\ln \left(\frac{a_3+b_3}{a_4+b_4} \right)}, \quad \beta_1 = (w+s)^2 + \left(2h+t + \frac{w}{\sqrt{\pi}} \right)^2 - \frac{w^2}{\pi}, \quad \beta_2 = \left(\frac{w}{2} \right)^2 + \left(2h+t + \frac{w}{\sqrt{\pi}} \right)^2 - \frac{w^2}{\pi} \\
a_1 &= \sqrt{\left(\frac{w^2}{\pi} \right) + \frac{\beta_1 + \sqrt{\beta_1^2 + 4 \left(\frac{w^2}{\pi} \right) \left(2h+t + \frac{w}{\sqrt{\pi}} \right)^2}}{2}} \\
b_1 &= \sqrt{\frac{\beta_1 + \sqrt{\beta_1^2 + 4 \left(\frac{w^2}{\pi} \right) \left(2h+t + \frac{w}{\sqrt{\pi}} \right)^2}}{2}} \\
a_2 &= \sqrt{\left(\frac{w^2}{\pi} \right) + \frac{(w+s)^2 + \sqrt{(w+s)^4 + 4 \left(\frac{w^4}{\pi^2} \right)}}{2}} \\
b_2 &= \sqrt{\frac{(w+s)^2 + \sqrt{(w+s)^4 + 4 \left(\frac{w^4}{\pi^2} \right)}}{2}} \\
a_3 &= \sqrt{\left(\frac{w^2}{\pi} \right) + \frac{\beta_2 + \sqrt{\beta_2^2 + 4 \left(\frac{w^2}{\pi} \right) \left(2h+t + \frac{w}{\sqrt{\pi}} \right)^2}}{2}} \\
b_3 &= \sqrt{\frac{\beta_2 + \sqrt{\beta_2^2 + 4 \left(\frac{w^2}{\pi} \right) \left(2h+t + \frac{w}{\sqrt{\pi}} \right)^2}}{2}} \\
a_4 &= \sqrt{\left(\frac{w^2}{\pi} \right) + \frac{\left(\frac{w^2}{4} \right) + \sqrt{\frac{w^4}{16} + 4 \left(\frac{w^4}{\pi^2} \right)}}{2}} \\
b_4 &= \sqrt{\frac{\left(\frac{w^2}{4} \right) + \sqrt{\frac{w^4}{16} + 4 \left(\frac{w^4}{\pi^2} \right)}}{2}}
\end{aligned} \tag{2.44}$$

2.5.5 Transistor Layer Modeling

2.5.5.1 Introduction

The Sesctherm transistor layer model is an attempt to accurately characterize the distribution of materials that make up the cross-section of a given chip design that encompasses everything above the bulk silicon substrate and below the first metal layer. Everything in this region of the chip stack is termed the “transistor” layer. Sesctherm uses a combination of transistor density characterization and various sub-models to model either bulk-silicon-based or silicon-on-insulator transistor-based lumped material layers.

The transistor layer model is designed to allow thermal characterization of a chip design without specifying every aspect of the design implementation. This allows designers to make use of thermal modeling tools at an early design phase – when little is known about the specific implementation about a given design. To accomplish this, a compromise is made between full Computer-Aided-Design-like thermal simulation, where every interconnect and transistor is specifically modeled, and naive materials modeling techniques which will be unlikely to provide a representative prediction about the thermal characteristics of a specific chip design.

To characterize the transistor layer, Sesctherm requires knowledge about the type of manufacturing process that will be used. Sesctherm models both bulk-silicon and silicon-on-insulator technologies. Further, Sesctherm requires knowledge about the relative transistor and interconnect density of each architectural floor-plan block in the

given chip design. The ability to specify transistor densities, interconnect densities, and technology parameters is sufficiently general knowledge to allow “what-if” studies at a very early design phase, while not being so general as to lose valuable insight into the specific thermal properties of a given design by designing a naive “one-size-fits-all” type of model.

To avoid the costly runtime costs associated with implementing a full 3D model to model every transistor and interconnect, Sesctherm computes lumped thermal properties of each floor-plan block. Specifically, Sesctherm computes the equivalent lateral thermal conductivity, equivalent vertical thermal conductivity to the layer above, equivalent vertical thermal conductivity to the layer below, and equivalent specific heat of the material. Using this lumped modeling methodology, Sesctherm is able to model the complex material distribution in this region of the chip without sacrificing performance.

A bulk silicon MOSFET (Metal-Oxide-Field-Effect-Transistor) can be seen in figure 2.28. Each MOSFET transistor is an electrical switch with three connections. In the case of an NMOS transistor, when an electrical potential is applied to the transistor gate input, the source and drain connections are considered to be shorted together, while the lack of an electrical potential will cause the source and drain to be disconnected like an open circuit.

The transistor is made of several parts. The bottom of the transistor is made of silicon that has been “doped”. This means that the silicon material either had electrons added or removed through the application of a strong electric field and heat. Above this “well” of doped silicon is placed a strong electrical dielectric (insulator), that insulates

the gate from the transistor. Above this ribbon of dielectric is placed a thin poly-silicon ribbon. A side view of a bulk silicon MOSFET can be seen in figure 2.32. A description of the model Sesetherm uses in the implementation of the bulk-silicon MOSFET model can be seen in figure 2.34.

It should be noted that a variety of lumped transistor resistance models have been developed [78],[117],[50],[121]. All of these models involved integration of the temperature field to obtain a simple, closed-form expression for the thermal resistance of a solid-state device. However, these models made various assumptions about the overall geometry of the transistor. Some models assume that the transistor can be modeled as a rectangular region of zero thickness [97]. Others neglect the effects of the interconnect.

Most importantly, however, is the fact that these models are designed for transistor thermal characterization less than the characteristic thermal length of the transistor device. For deep sub-micrometer designs, this means a sub micro-second time resolution. Due to the fact that Sesetherm is primarily concerned with thermal characterization on a much larger time scale, we consider the transistor-scale thermal fluctuations insignificant. Therefore, there is a need to develop a thermal sub-model that reliably characterizes the thermal behavior of the transistor layer, made of a complex distribution of transistors, polysilicon interconnect, via contacts, and inter-transistor electrical isolation.

The basis for the thermal model design was that model chip designs exhibit a highly regular nature, as can be seen in figure 2.29. As can be seen here, interconnect

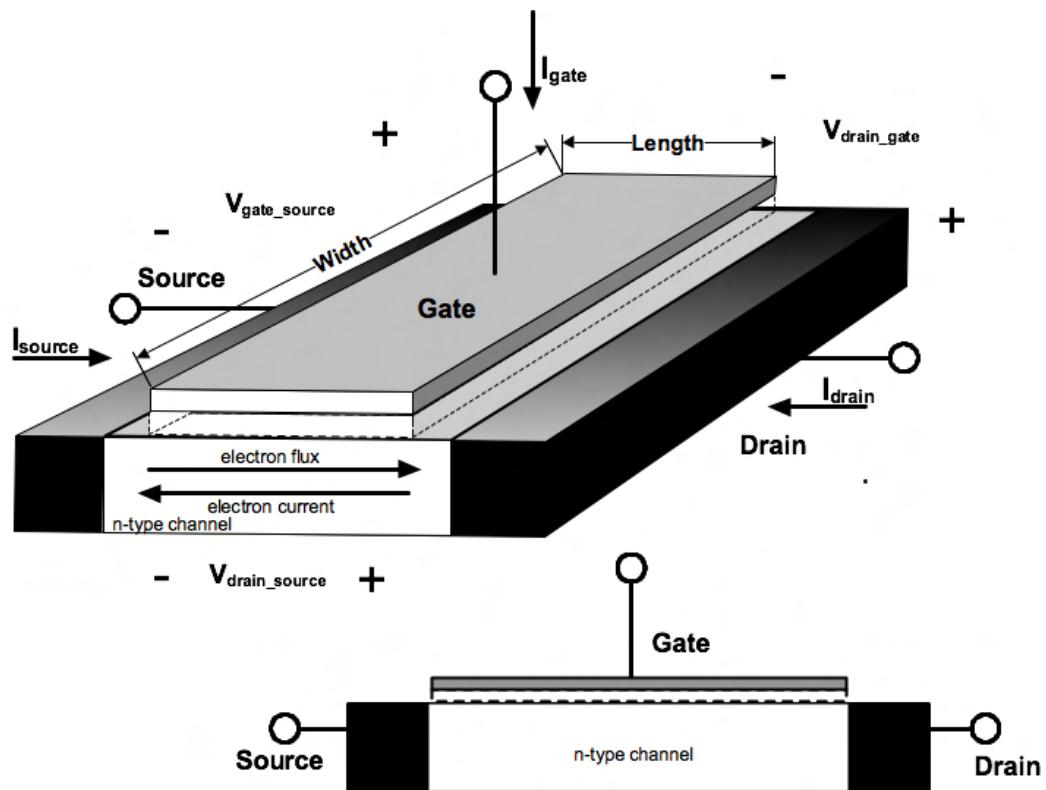


Figure 2.28: Diagram for typical MOSFET Transistor Model

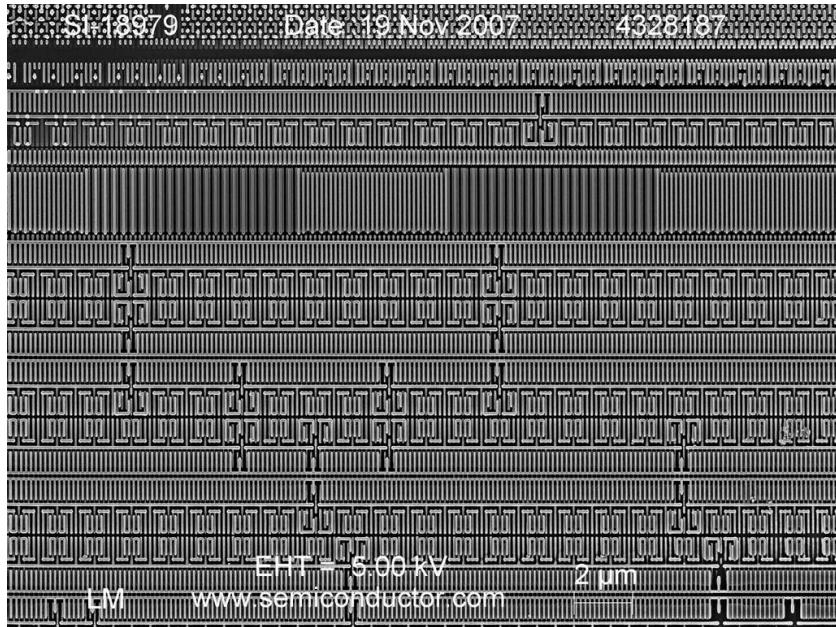


Figure 2.29: Top-down View of Structured Layout for Intel 45nm Process

routing is highly regular. It is this regular nature that provides the basis for the thermal sub-models designed for the transistor layers. As can be seen in figure 2.30, the use of a cell-based design methodology regularizes the distribution of materials across the transistor layer.

This regularizes material distribution, and cell-based layout methodology motivates a simplified layout methodology – depicted in figure 2.31. Each transistor is dedicated a subset of the virtual chip die, termed a transistor “cell”. Each cell contains a single transistor. The ratio of the length and width of each cell is the same as the ratio of the length and width of each floor-plan unit. Further, the area of each cell is equal to the total area of the floor-plan unit divided by the number of transistors. This

can be seen in equations (2.45).

At the center of each transistor cell is the active transistor device. The transistor is surrounded by polysilicon interconnect. The number of vias per interconnect is governed by a via “efficiency factor”, which describes the probability that an interconnect has one or more vertical connections to the first metal interconnect layer. All of the interconnects are assumed to be routed along the length of the floor-plan unit. Further, the transistor is oriented such that the polysilicon gate is parallel to the interconnect routing direction.

In order to determine the distribution of interconnects, the statistical interconnect distribution described previously is used. The model attempts to create polysilicon interconnects within and between each of the transistor cells. Each cell is considered equal to all the others.

Once the interconnect distribution is created, lumped lateral and lumped vertical thermal resistances are created. Similarly, lumped resistances are generated for the transistors themselves. Finally, the lateral and vertical, lumped, resistances are combined to form a unified transistor model for either bulk silicon or silicon-on-insulator technologies.

$$\frac{L_{\text{cell}}}{W_{\text{cell}}} = \frac{L_{\text{flop_unit}}}{W_{\text{flop_unit}}}$$

$$L_{\text{cell}} W_{\text{cell}} = \frac{L_{\text{flop_unit}} W_{\text{flop_unit}}}{N_{\text{transistors}}}$$

Solved Simultaneously: (2.45)

$$L_{\text{cell}} = \frac{L_{\text{flop_unit}}}{\sqrt{N_{\text{transistors}}}}$$

$$W_{\text{cell}} = \frac{W_{\text{flop_unit}}}{\sqrt{N_{\text{transistors}}}}$$

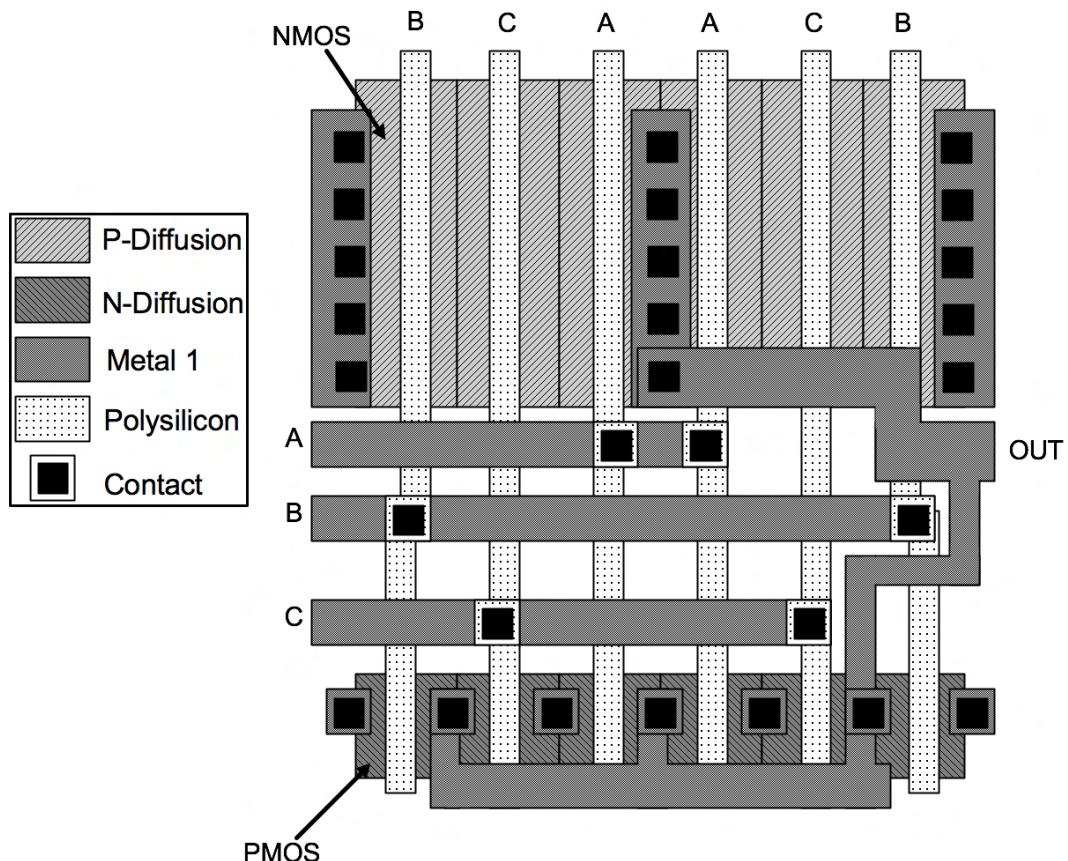


Figure 2.30: Diagram for 3-input NOR Standard Logic Cell

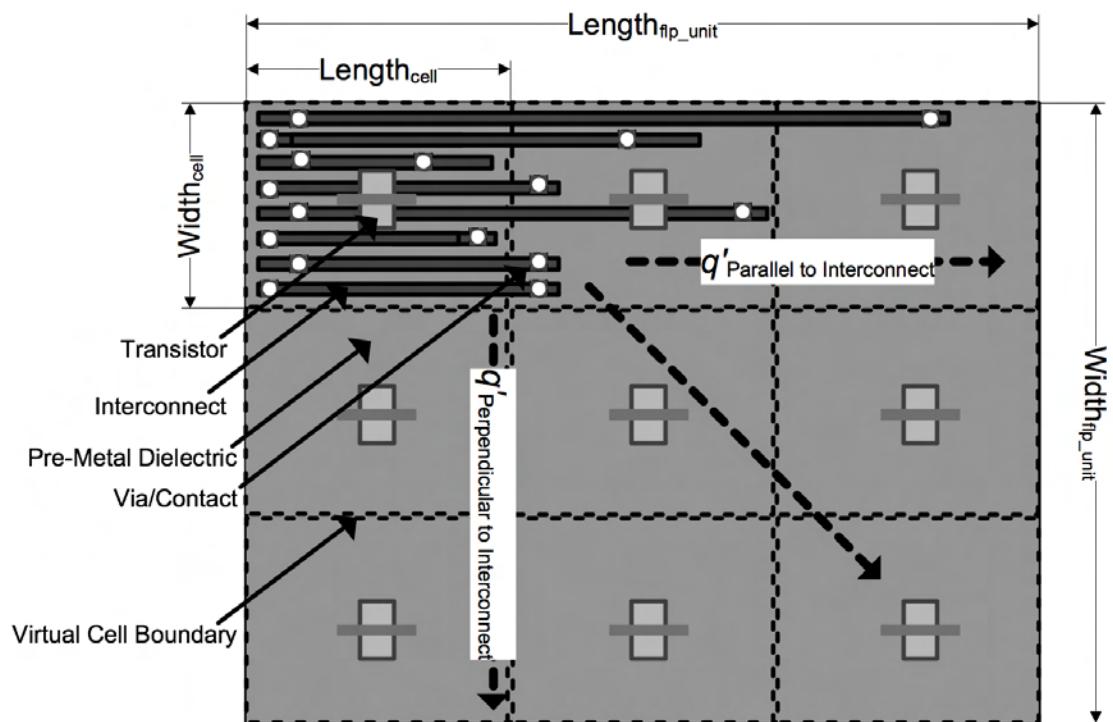


Figure 2.31: Overview of Transistor Layer Electrothermal Model Design (Top-Down View)

It should be noted that a variety of damascene processes have been used over the years. A damascene process is one where the first metal interconnect is fabricated directly over the transistor isolation. In this case the polysilicon interconnect layer is not clearly defined relative to the first metal interconnect layer. This hybrid approach, where the first metal interconnect layer and transistor layer is not clearly defined has been used by Advanced Micro Devices for a variety of their processes. Sesctherm is not currently designed to model such scenarios. This is considered future work.

The following sections describe the methodology to model each of these technology processes. The relevant equations are described.

2.5.5.2 Bulk Silicon CMOS Layer Model

The bulk silicon MOSFET layer is designed to accurately represent the relevant lumped thermal characteristics of a bulk silicon technology process. The general model geometry is shown in figure 2.32. As can be shown a lightly doped p-type silicon substrate layer occurs above the bulk silicon substrate. As can be seen in figure 2.33, the doping profile can be considered highly regular in nature. However, variations in the doping profile may exist. Further, a p-type substrate may not, in fact, be used. The characterization of n-type substrate-based technology process is considered future work.

In this model we model doped nwell regions and heavily doped p-well regions where P^+ or N^+ source/drain diffusion regions occur under the via contacts. This can be seen in figure 2.32. In this model, we assume that the contact plugs are make of

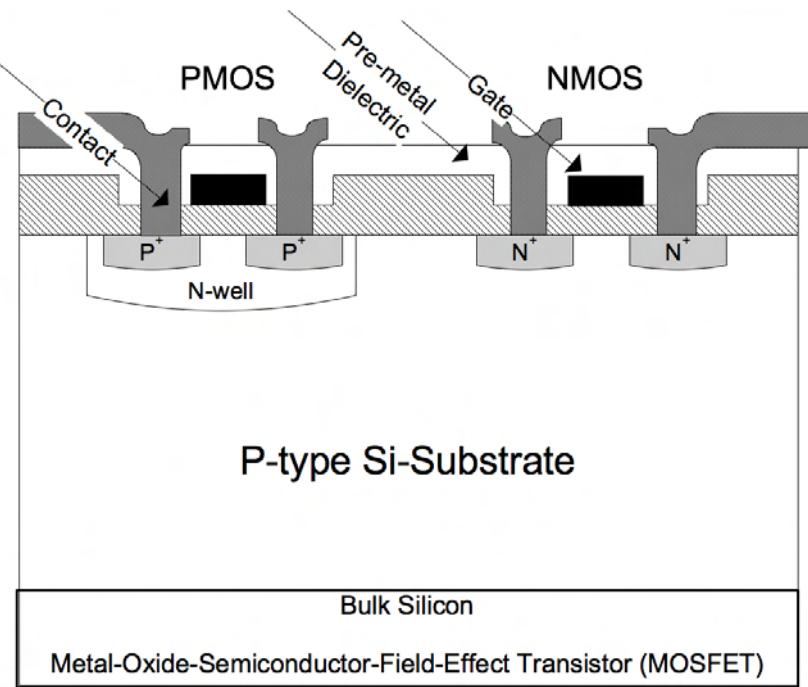


Figure 2.32: Diagram for Bulk Silicon MOSFET

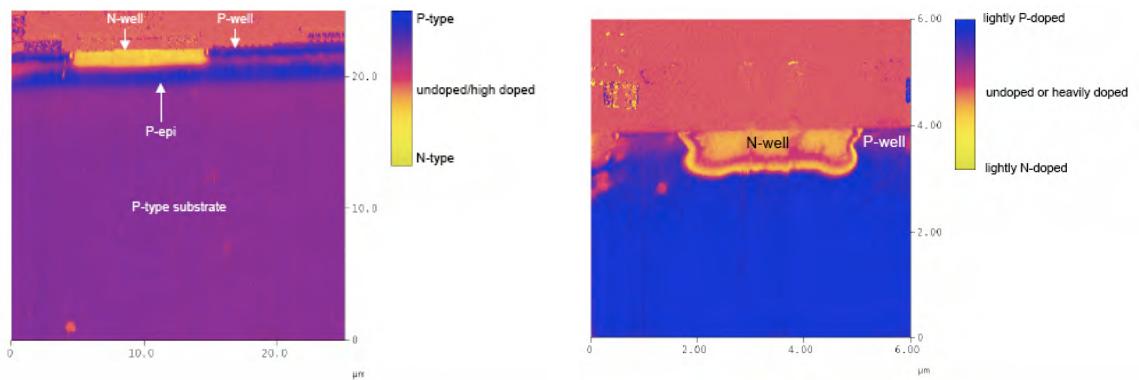


Figure 2.33: Doping Profiles for (a) Samsung 5K3AAEA03 [27] and (b) Texas Instruments 1710 [24]

Tungsten. Further, a thin dielectric film is placed over the junction region – insulating a polysilicon ribbon from the underlying doped silicon substrate.

Between the NMOS and PMOS transistor devices is electrical isolation either in the form of LOCOS (“Local Oxidation of Semiconductor”), where oxygen ion implantation is used to form a silicon dioxide film or STI (shallow trench isolation), where a dielectric deposition is performed. In either case a dielectric material is used that electrically isolates the nwell regions from the pwell regions so as to reduce quiescent leakage current, and avoid electrical malfunctions of the transistor devices. STI is considered a more modern technique.

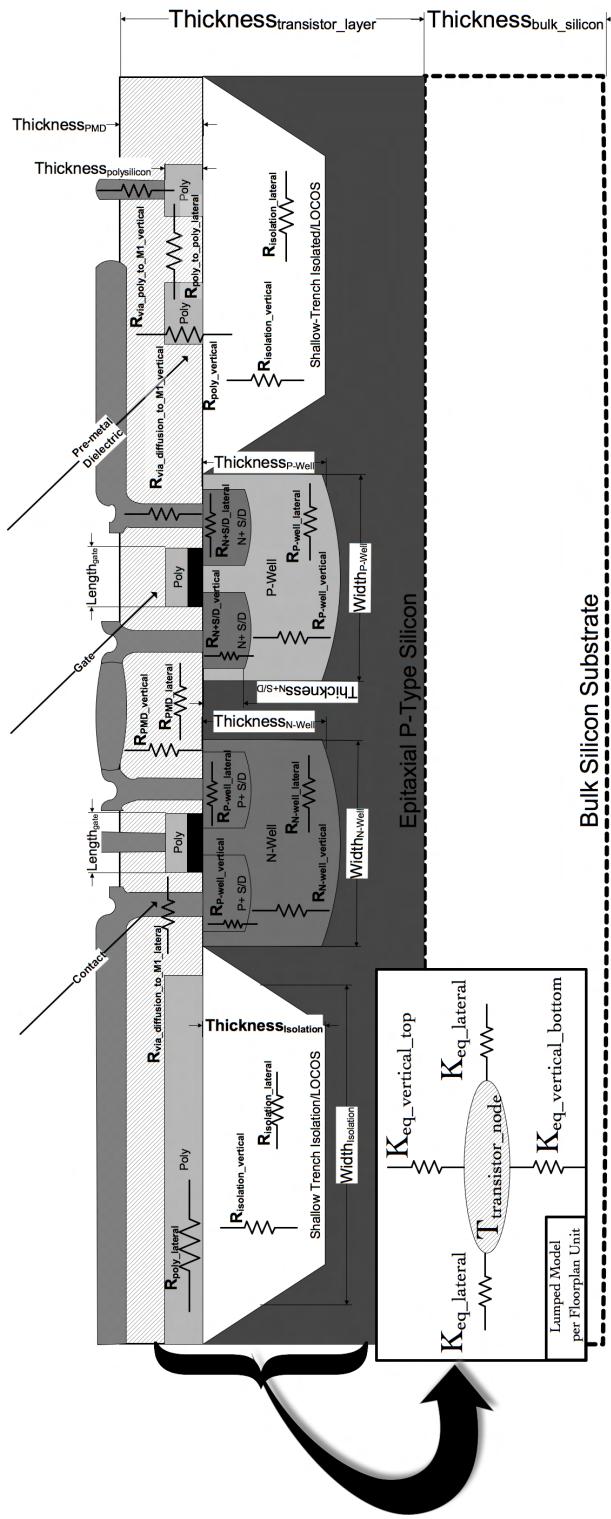


Figure 2.34: Diagrams for Bulk Silicon MOSFET Electrothermal Model

As can be seen in figure 2.34, detailed modeling is performed for both the transistors and the interconnect. The polysilicon interconnect is isolated from the lightly doped p-type silicon substrate using either STI or LOCOS. There are variations in the length of metal contacts depending upon whether or not the contact is made to the transistor gate, source/drain diffusion or a polysilicon interconnect. In order to obtain the relevant dimensions, technology parameters from a variety of structural analysis reports are obtained. This can be seen in Appendix A.

It can further be seen that this relatively simple modeling methodology is actually highly representative of a wide variety of technology processes. This can be seen in figure 2.36. In particular, the variation in contact length can be seen in figure 2.36 (a), where the pre-metal dielectric thickness is enforced, while the contact length is allowed to vary. Figure 2.36 (b) shows that there is no need for electrical isolation between wells of like type – in this image STI is not used between the NMOS transistors. Figure 2.36 (c) shows the use of STI to insulate polysilicon interconnect from the underlying, lightly doped, silicon substrate. It should be noted that a hard titanium liner is frequently used as a stress liner to ensure the structural integrity of various material depositions. We do not consider these to be of significance due to their extremely small physical dimensions (less than 50nm). However, it may be critical to include these liners for the purpose of accurate reliability analysis as there may be a significant impact upon dielectric breakdown and electro-migration phenomenon. This is considered future work.

The transistor modeling used here is only valid for the macroscopic thermal analysis purposes done here. It can be seen in figure 2.37 that the specific material

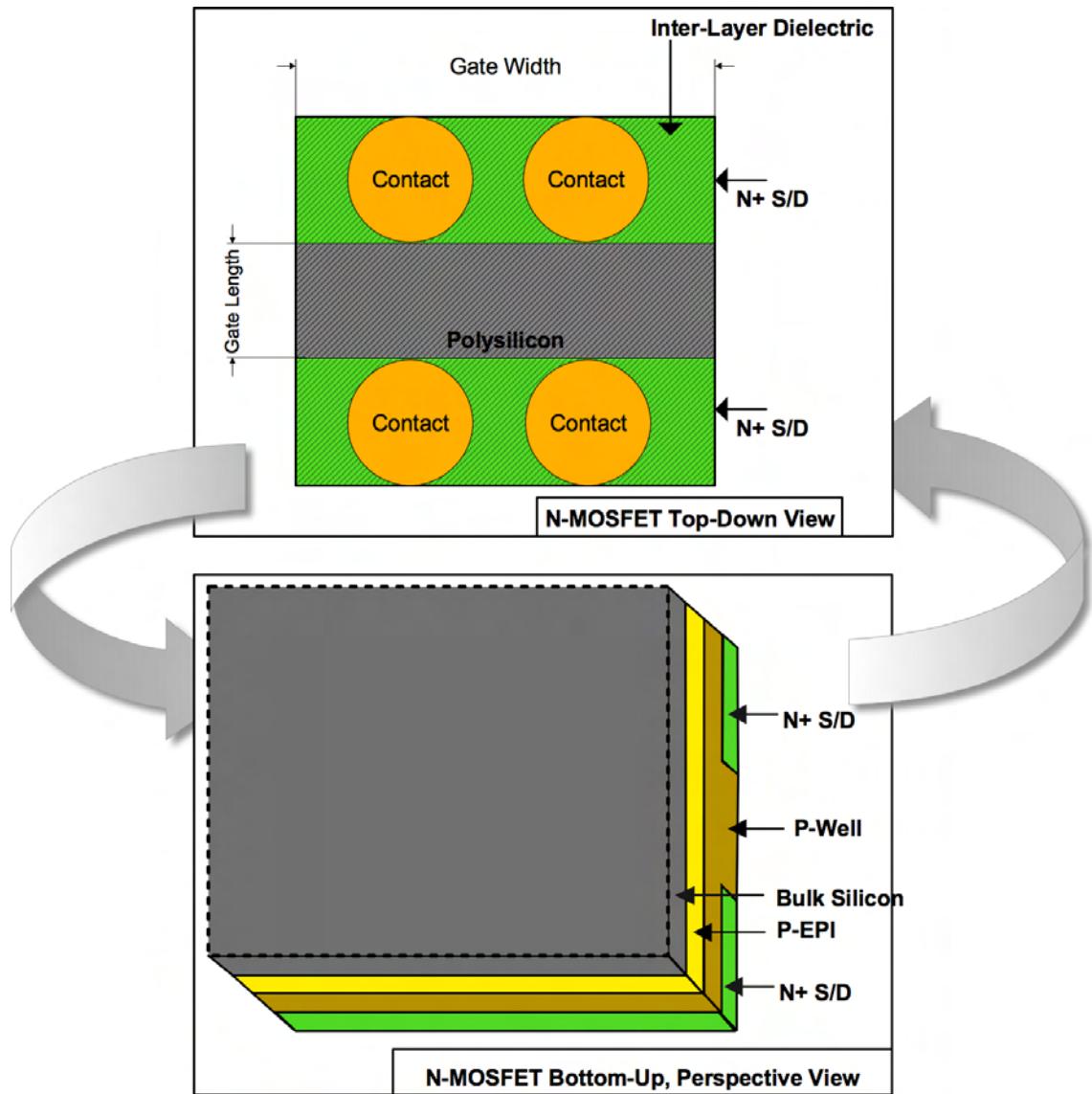


Figure 2.35: Transistor Sub-model Diagram. Lumped Lateral Heat Flows (Along Width Using Equation (2.58), and Along Length of Transistor Using (2.61)) and Vertical Heat Flows Are Developed)

geometry of modern transistors may vary significantly from the general transistor geometry described here. In particular, strained-silicon process using Silicon Germanium are now being used in a variety of technology processes as a means to reduce junction leakage and improve carrier mobility characteristics. An extension of this transistor model to include such devices is considered future work.

As can be seen in figure 2.38, the ratio of length to width of transistor can vary dramatically depending upon various electrical design considerations. Further, the number of source/drain contact plugs is highly a function of transistor width. While most technology reports only describe minimum transistor feature characteristics, Sesetherm is primarily concerned with average feature characteristics. While no perfect solution exists as transistor sizing is highly a function of the particular design rules used, manual inspection of output from standard industry floor-planning and layout tools was used to arrive at the rough approximation that over 90% of the transistors were considered minimum-sized. Given this observation, transistor sizing was not extensively explored here. Accurate characterization of average transistor sizing is considered future work.

The general expression for the lumped thermal resistance for vertical heat flow to the first metal interconnect layer above the transistor layer can be found in equation (2.46).

This is further developed in equation (2.47), and it is described in simplified form in equation (2.48). Similarly, the general expression for vertical heat flow to the bulk silicon substrate below the transistor layer can be found in equation (2.49). This is further developed in equation (2.50), and it is described in simplified form in equation

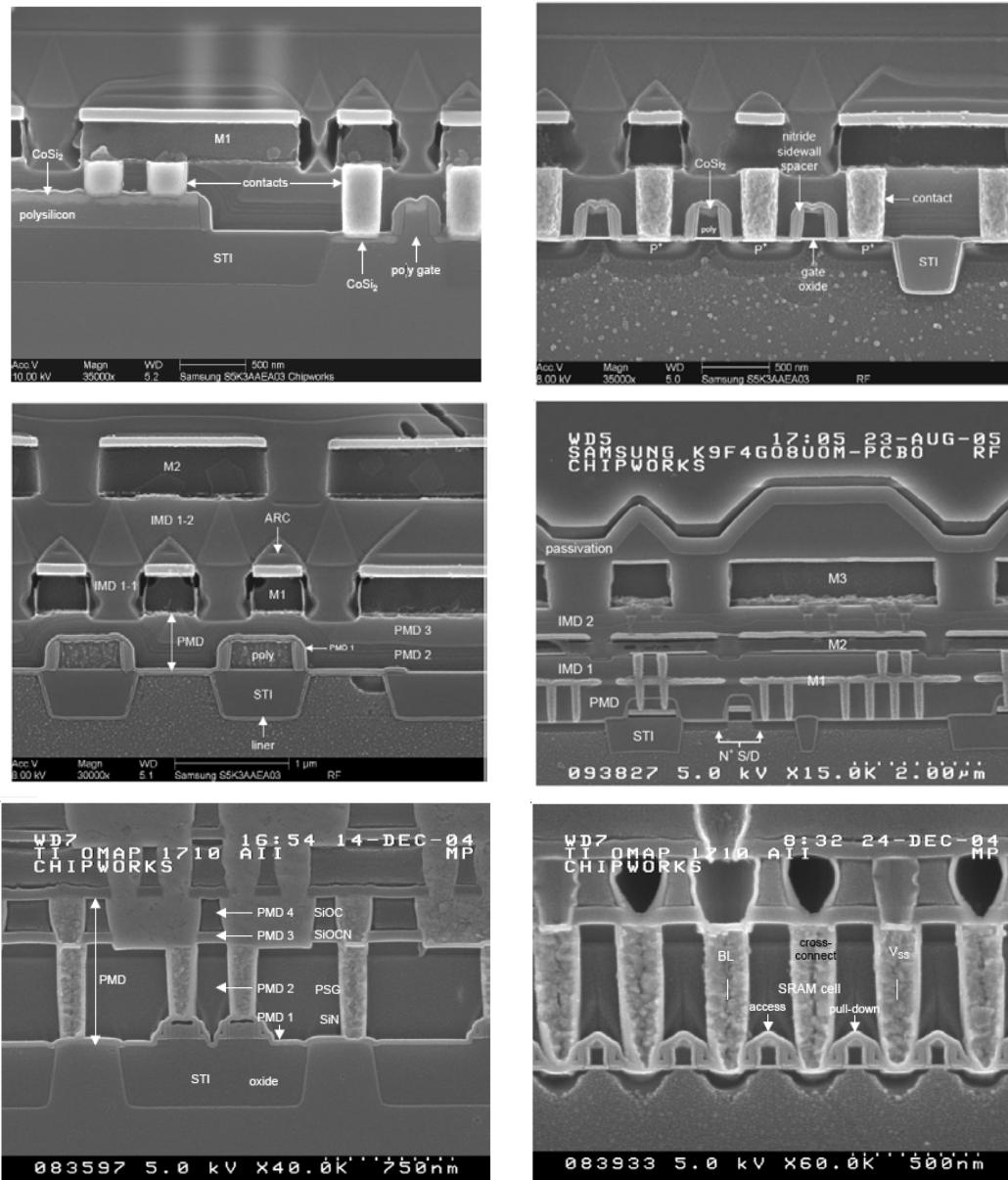


Figure 2.36: Transistor Side-view for (a,b,c) Samsung S5K3AAEA03 [27] (d) Samsung K9F4GO8UOM-PCBO [26] (e,f) Texas Instruments OMAP 1710 [24]

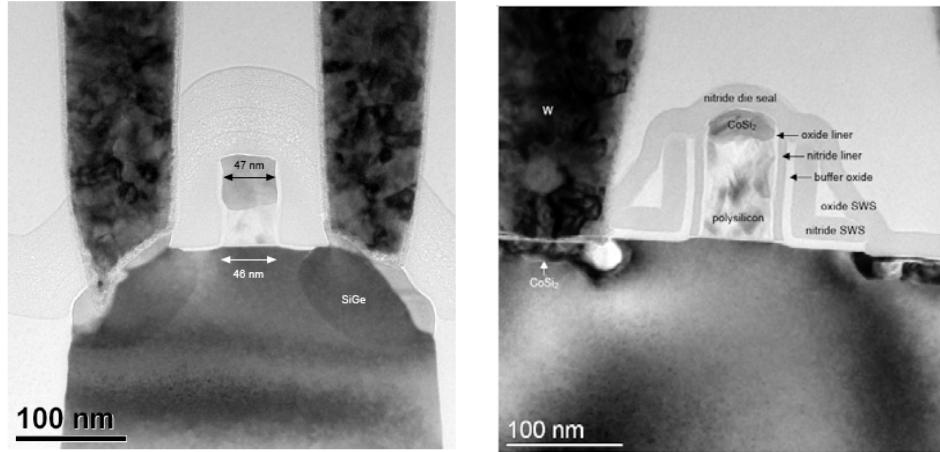


Figure 2.37: Close-up Transistor Side-view for (a) Texas Instruments OMAP 1710 [24](b) Intel Presler 65nm [29]

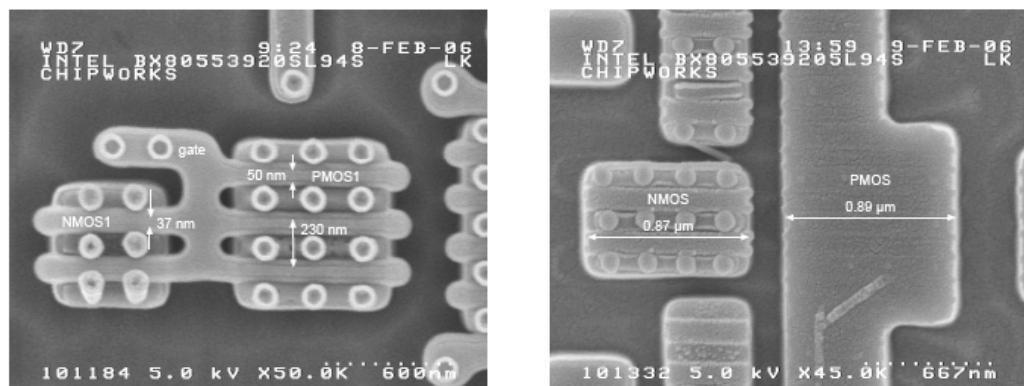


Figure 2.38: Transistor Top-view for (a,b) Intel Presler 65nm [29]

(2.51).

The general expression for lateral heat flow parallel to the routing direction of the interconnects can be found in equation (2.62), and it is described in simplified form in equation (2.63). Similarly, the general expression for lateral heat flow perpendicular to the routing direction of the interconnects can be found in equation (2.64), and it is described in simplified form in equation (2.65). Each macro-scale, transistor-layer lumped resistance equation is dependent upon two other equations.

In particular, the macro-scale transistor-layer model that describes the lateral heat flow parallel to the routing direction of the interconnects is dependent upon a first sub-model that describes lateral heat flow through each of the transistors, and it also dependent upon a second sub-model that describes lateral heat flow through the interconnect distribution, vias, diffusion and insulation. Each of these sub-models model heat flow parallel to the routing direction of the interconnects – which is assumed to be along the length of the chip (see Figure 2.31 above). The first, transistor sub-model is described simply in equation (2.59). It is further developed in equation (2.60), and it is simplified in equation (2.61). The second, interconnect sub-model is described by equation (2.54). This is simplified in equation (2.55).

Similarly, the macro-scale transistor-layer model that describes the lateral heat flow perpendicular to the routing direction of the interconnects is also dependent upon two sub-models – transistor and interconnect. In this case, each sub-model models heat flow perpendicular to the routing direction of the interconnect. As noted above, each transistor is oriented such that the polysilicon gate is parallel to the routing direction

of the interconnect – along the length of the chip. The transistor sub-model used here is described in equation (2.56). This is further developed in equation (2.57), and it is simplified in equation (2.58). The interconnect model is described in equation (2.52), and it is simplified in equation (2.53).

$$\begin{aligned}
 R_{\text{vertical_top}} = & R_{\text{ild_vertical}} \| R_{\text{contact_to_diffusion_vertical}} \| ((R_{\text{contact_to_poly}} \| R_{\text{PMD_vertical_to_poly}}) + R_{\text{poly_vertical}}) \\
 & \| ((R_{\text{contact_to_gate}} \| R_{\text{ild_to_gate}}) + R_{\text{poly}} + R_{\text{gate}}) \\
 & \| (R_{\text{PMD_vertical_to_gate}} + R_{\text{PMD_vertical_to_poly}} + R_{\text{PMD_vertical_to_diffusion}})
 \end{aligned} \tag{2.46}$$

$$\begin{aligned}
R_{\text{vertical-top}} &= \frac{t_{\text{PMD}}}{k_{\text{vertical-top}} * \text{length}_{\text{fp-unit}} * \text{width}_{\text{fp-unit}}} = \\
&\frac{t_{\text{PMD}}}{k_{\text{id}} \left(1 + 0.88 \frac{t_{\text{PMD}}}{\text{width}_{\text{fp-unit}}} \right) \left(l_{\text{fp-unit}} * w_{\text{fp-unit}} \int_{L_{\min}}^{L_{\max}} i(l) dl - W_{\text{gate}} * L_{\text{gate}} * N_{\text{transistors}} - \pi \left(\frac{d_{\text{via}}}{2} \right)^2 ((2 + e_{\text{transistors-via}}) N_{\text{transistors}}) \right)} \\
&\times \\
&\left(\frac{\frac{t_{\text{PMD}}}{k_{\text{via}} \pi \left(\frac{d_{\text{via}}}{2} \right)^2 2 N_{\text{transistors}}}}{\left(\left(\frac{(t_{\text{PMD}} - t_{\text{poly}})}{k_{\text{via}} \pi \left(\frac{d_{\text{via}}}{2} \right)^2 2 \int_{L_{\min}}^{L_{\max}} i(l) dl} \right) k_{\text{id}} \left(1 + 0.88 \frac{t_{\text{PMD}}}{\text{width}_{\text{fp-unit}}} \right) \left(w_{\text{poly}} \int_{L_{\min}}^{L_{\max}} i(l) dl - \pi \left(\frac{d_{\text{via}}}{2} \right)^2 2 \int_{L_{\min}}^{L_{\max}} i(l) dl \right) \right) + \frac{t_{\text{poly}}}{\left(k_{\text{poly}} * w_{\text{poly}} \int_{L_{\min}}^{L_{\max}} i(l) dl \right)} \right) \right. \\
&\left. + \left(\left(\frac{(t_{\text{PMD}} - t_{\text{poly}} - t_{\text{gate}})}{k_{\text{via}} \pi \left(\frac{d_{\text{via}}}{2} \right)^2 e_{\text{transistor-via}} N_{\text{transistors}}} \right) k_{\text{id}} \left(1 + 0.88 \frac{t_{\text{PMD}}}{\text{width}_{\text{fp-unit}}} \right) \left(W_{\text{gate}} * L_{\text{gate}} * N_{\text{transistors}} - \pi \left(\frac{d_{\text{via}}}{2} \right)^2 e_{\text{transistors-via}} N_{\text{transistors}} \right) \right. \right. \\
&\left. \left. + \frac{k_{\text{gate}} W_{\text{gate}} * L_{\text{gate}} * N_{\text{transistors}}}{t_{\text{gate}}} + \frac{k_{\text{poly}} W_{\text{gate}} * L_{\text{gate}} * N_{\text{transistors}}}{t_{\text{poly}}} \right) \right. \\
&\left. \left(\frac{(t_{\text{PMD}} - t_{\text{poly}} - t_{\text{gate}})}{k_{\text{id}} \left(1 + 0.88 \frac{t_{\text{PMD}}}{\text{width}_{\text{fp-unit}}} \right) \left(l_{\text{fp-unit}} * w_{\text{fp-unit}} - \pi \left(\frac{d_{\text{via}}}{2} \right)^2 ((2 + e_{\text{transistors-via}}) N_{\text{transistors}} + 2 \int_{L_{\min}}^{L_{\max}} i(l) dl) \right)} \right. \right. \\
&\left. \left. + \frac{t_{\text{gate}}}{\left(k_{\text{id}} \left(1 + 0.88 \frac{t_{\text{PMD}}}{\text{width}_{\text{fp-unit}}} \right) \left(l_{\text{fp-unit}} * w_{\text{fp-unit}} - \pi \left(\frac{d_{\text{via}}}{2} \right)^2 ((2) N_{\text{transistors}} + 2 \int_{L_{\min}}^{L_{\max}} i(l) dl) - W_{\text{gate}} * L_{\text{gate}} * N_{\text{transistors}} \right) \right) \right. \right. \\
&\left. \left. + \frac{t_{\text{poly}}}{\left(k_{\text{id}} \left(1 + 0.88 \frac{t_{\text{PMD}}}{\text{width}_{\text{fp-unit}}} \right) \left(l_{\text{fp-unit}} * w_{\text{fp-unit}} - \pi \left(\frac{d_{\text{via}}}{2} \right)^2 ((2) N_{\text{transistors}}) \right) \right) \right) \right) \right) \right) \quad (2.47)
\end{aligned}$$

Simplified:

$$\begin{aligned}
R_{\text{vertical,top}} &= \frac{t_{\text{PMD}}}{k_{\text{vertical_top}} * \text{length}_{\text{fp-unit}} * \text{width}_{\text{fp-unit}}} = \\
&1 / \left(\left(\frac{\pi k_{\text{via}} N_{\text{transistors}} d_{\text{via}}^2 + k_{\text{ild}} \left(\frac{0.88 t_{\text{PMD}}}{\text{width}_{\text{fp-unit}}} + 1 \right)}{2 t_{\text{PMD}}} \right) / \left(-\frac{1}{2} \pi \left(\int_{L_{\min}}^{L_{\max}} i(l) dl + N_{\text{transistors}} \right) d_{\text{via}}^2 + l_{\text{fp-unit}} w_{\text{fp-unit}} - L_{\text{gate}} N_{\text{transistors}} W_{\text{gate}} \right. \right. \right. \\
&- \frac{t_{\text{gate}} - t_{\text{PMD}} + t_{\text{poly}}}{l_{\text{fp-unit}} w_{\text{fp-unit}} - \frac{1}{4} \pi d_{\text{via}}^2 \left(2 \int_{L_{\min}}^{L_{\max}} i(l) dl + (e_{\text{transistors-via}} + 2) N_{\text{transistors}} \right)} - \frac{\pi d_{\text{via}}^2 N_{\text{transistors}} - 2 l_{\text{fp-unit}} w_{\text{fp-unit}}}{2 t_{\text{poly}}} \\
&\left. \left. \left. + \left(-\frac{1}{4} \pi (e_{\text{transistors-via}} + 2) N_{\text{transistors}} d_{\text{via}}^2 - \left(\int_{L_{\min}}^{L_{\max}} i(l) dl \right) w_{\text{poly}} + l_{\text{fp-unit}} w_{\text{fp-unit}} - L_{\text{gate}} N_{\text{transistors}} W_{\text{gate}} \right) k_{\text{ild}} \left(\frac{0.88 t_{\text{PMD}}}{\text{width}_{\text{fp-unit}}} + 1 \right) \right) \right. \right. \\
&+ \frac{t_{\text{poly}}}{\left(\int_{L_{\min}}^{L_{\max}} i(l) dl \right) k_{\text{poly}} w_{\text{poly}}} + \frac{t_{\text{PMD}} - t_{\text{poly}}}{\left(\int_{L_{\min}}^{L_{\max}} i(l) dl \right) \pi \left[\frac{d_{\text{via}}}{2} \right]^2 k_{\text{via}}} \left(\pi \left(\int_{L_{\min}}^{L_{\max}} i(l) dl \right) d_{\text{via}}^2 - 2 \left(\int_{L_{\min}}^{L_{\max}} i(l) dl \right) w_{\text{poly}} \right) k_{\text{ild}} \left(\frac{0.88 t_{\text{PMD}}}{\text{width}_{\text{fp-unit}}} + 1 \right) \\
&+ \frac{N_{\text{transistors}}}{\left(-t_{\text{gate}} + t_{\text{PMD}} - t_{\text{poly}} \right) \left(\pi \left[\frac{d_{\text{via}}}{2} \right]^2 e_{\text{transistor-via}} k_{\text{via}} \left(\pi d_{\text{via}}^2 e_{\text{transistors-via}} - 4 L_{\text{gate}} W_{\text{gate}} \right) k_{\text{ild}} \left(\frac{0.88 t_{\text{PMD}}}{\text{width}_{\text{fp-unit}}} + 1 \right) \right. \right. \right. \\
&\left. \left. \left. + \frac{t_{\text{gate}}}{k_{\text{gate}} L_{\text{gate}} W_{\text{gate}}} + \frac{t_{\text{poly}}}{k_{\text{poly}} L_{\text{gate}} W_{\text{gate}}} \right) \right) \right) \\
\end{aligned} \tag{2.48}$$

$$R_{\text{vertical,bottom}} = (R_{\text{isolation-pepi_vertical}} + R_{\text{isolation_vertical}})$$

$$\begin{aligned}
&\frac{\| (R_{\text{P_SD_vertical}} \| R_{\text{P_SD_vertical}}) + R_{\text{nwell_vertical_bottom}} + R_{\text{nwell_pepi_vertical}})}{\| (R_{\text{N_SD_vertical}} \| R_{\text{N_SD_vertical}}) + R_{\text{pwell_vertical_bottom}} + R_{\text{pwell_pepi_vertical}})} \\
&\| R_{\text{pepi}}
\end{aligned} \tag{2.49}$$

$$\begin{aligned}
R_{\text{vertical-bottom}} &= \frac{t_{\text{pepi}}}{k_{\text{vertical-bottom}} * \text{length}_{\text{fip-unit}} * \text{width}_{\text{fip-unit}}} = \\
&\left(\frac{t_{\text{isolation}}}{k_{\text{isolation}} \left(\text{width}_{\text{poly}} \int_{L_{\min}}^{L_{\max}} i_{\text{z}}(l) dl + \left(\frac{N_{\text{transistors}}}{2} * \text{width}_{\text{isolation}} * \text{length}_{\text{transistor}} \right) \right)} \right. \\
&+ \frac{\left(t_{\text{pepi}} - t_{\text{isolation}} \right)}{k_{\text{p-epi}} \left(\text{width}_{\text{poly}} \int_{L_{\min}}^{L_{\max}} i_{\text{z}}(l) dl + \left(\frac{N_{\text{transistors}}}{2} * \text{width}_{\text{isolation}} * \text{length}_{\text{transistor}} \right) \right)} \\
&\left. \left(\left(\frac{t_{\text{p-sd}} - t_{\text{n-sd}}}{k_{\text{p-sd}} \left(2 \frac{N_{\text{transistors}}}{2} * \text{width}_{\text{p-sd}} * \text{length}_{\text{transistor}} \right)} + \frac{t_{\text{nwell}} - t_{\text{p-sd-vertical}}}{k_{\text{nwell}} \left(\frac{N_{\text{transistors}}}{2} * \text{width}_{\text{nwell}} * \text{length}_{\text{transistor}} \right)} + \frac{t_{\text{pepi}} - t_{\text{nwell}}}{k_{\text{pepi}} \left(\frac{N_{\text{transistors}}}{2} * \text{width}_{\text{nwell}} * \text{length}_{\text{transistor}} \right)} \right) \right. \right. \\
&\left. \left. \left(\frac{t_{\text{n-sd}} - t_{\text{pwell}}}{k_{\text{n-sd}} \left(2 \frac{N_{\text{transistors}}}{2} * \text{width}_{\text{n-sd}} * \text{length}_{\text{transistor}} \right)} + \frac{t_{\text{pwell}} - t_{\text{n-sd-vertical}}}{k_{\text{pwell}} \left(\frac{N_{\text{transistors}}}{2} * \text{width}_{\text{pwell}} * \text{length}_{\text{transistor}} \right)} + \frac{t_{\text{pepi}} - t_{\text{pwell}}}{k_{\text{pepi}} \left(\frac{N_{\text{transistors}}}{2} * \text{width}_{\text{pwell}} * \text{length}_{\text{transistor}} \right)} \right) \right. \right. \\
&\left. \left. \left(\left(t_{\text{pepi}} / \left(k_{\text{p-epi}} \left(\text{width}_{\text{fip-unit}} * \text{length}_{\text{fip-unit}} - \frac{N_{\text{transistors}}}{2} * \text{width}_{\text{nwell}} * \text{length}_{\text{transistor}} - \frac{N_{\text{transistors}}}{2} * \text{width}_{\text{pwell}} * \text{length}_{\text{transistor}} \right) \right) \right) \right. \right. \\
&\left. \left. \left. - \text{width}_{\text{poly}} \int_{L_{\min}}^{L_{\max}} i_{\text{z}}(l) dl - \left(\frac{N_{\text{transistors}}}{2} * \text{width}_{\text{isolation}} * \text{length}_{\text{transistor}} \right) \right) \right) \right) \right) \quad (2.50)
\end{aligned}$$

Simplified:

$$\begin{aligned}
R_{\text{vertical,bottom}} &= \frac{t_{\text{pepi}}}{k_{\text{vertical,bottom}} * \text{length}_{\text{fp-unit}} * \text{width}_{\text{fp-unit}}} = \\
&= \frac{1}{1 + \left(\frac{k_{\text{pepi}} \left(\frac{1}{2} \left(-2 \left(\int_{L_{\min}}^{L_{\max}} l(i) \, dl \right) \text{width}_{\text{poly}} - \text{length}_{\text{poly}} - \text{length}_{\text{transistor}} N_{\text{transistors}} (\text{width}_{\text{isolation}} + \text{width}_{\text{nwell}} + \text{width}_{\text{pwell}}) + 2 \text{length}_{\text{fp-unit}} \text{width}_{\text{fp-unit}} \right) \right)}{t_{\text{pepi}}} \right.} \\
&\quad \left. + \frac{1}{\frac{t_{\text{isolation}}}{k_{\text{isolation}} \left(\frac{1}{2} \text{length}_{\text{transistor}} N_{\text{transistors}} \text{width}_{\text{isolation}} + \left(\int_{L_{\min}}^{L_{\max}} l(i) \, dl \right) \text{width}_{\text{poly}} \right)} + \frac{t_{\text{pepi}} - t_{\text{isolation}}}{k_{\text{pepi}} \left(\frac{1}{2} \text{length}_{\text{transistor}} N_{\text{transistors}} \text{width}_{\text{isolation}} + \left(\int_{L_{\min}}^{L_{\max}} l(i) \, dl \right) \text{width}_{\text{poly}} \right)}} \right. \\
&\quad \left. + \frac{1}{\frac{t_{\text{pepi}} - t_{\text{pwell}}}{k_{\text{pepi}} \left(\frac{1}{2} \text{length}_{\text{transistor}} N_{\text{transistors}} \text{width}_{\text{pwell}} \right)} + \frac{t_{\text{pwell}} - t_{\text{verticalIn,SD}}}{k_{\text{pwell}} \left(\frac{1}{2} \text{length}_{\text{transistor}} N_{\text{transistors}} \text{width}_{\text{pwell}} \right)} + \frac{t_{\text{verticalIn,SD}}}{k_{\text{n,SD}} (\text{length}_{\text{transistor}} N_{\text{transistors}} \text{width}_{\text{n,SD}})}} \right. \\
&\quad \left. + \frac{1}{\frac{t_{\text{pepi}} - t_{\text{nwell}}}{k_{\text{pepi}} \left(\frac{1}{2} \text{length}_{\text{transistor}} N_{\text{transistors}} \text{width}_{\text{nwell}} \right)} + \frac{t_{\text{nwell}} - t_{\text{verticalP,SD}}}{k_{\text{nwell}} \left(\frac{1}{2} \text{length}_{\text{transistor}} N_{\text{transistors}} \text{width}_{\text{nwell}} \right)} + \frac{t_{\text{verticalP,SD}}}{k_{\text{p,SD}} (\text{length}_{\text{transistor}} N_{\text{transistors}} \text{width}_{\text{p,SD}})}} \right) \quad (2.51)
\end{aligned}$$

Simplified:

Simplified:

$$R_{\text{mosfet,lateral}\perp} = \frac{R_{\text{diffusion}}}{2} \| R_{P-\text{well}} \| \frac{1}{2} \left(R_{\text{ild,between-vias}} + \frac{\text{width}_{\text{transistor}} R_{\text{via}}}{2d_{\text{via}}} \right) \| R_{\text{pepi}} \| R_{\text{polysilicon}} \| R_{\text{ild,above-polysilicon}}$$
(2.56)

Simplified:

$$k_{\text{mosfet,lateral-}\perp} = \frac{\text{width}_{\text{transistor}} / \left((2d_{\text{via}} + \text{length}_{\text{transistor}}) (t_{\text{epi}} + t_{\text{polm}}) \right) \left(\frac{\text{length}_{\text{transistor}} k_{\text{ild}} (t_{\text{ild}} - t_{\text{poly}})}{\text{width}_{\text{transistor}}} + \frac{(2d_{\text{via}} + \text{length}_{\text{transistor}}) k_{\text{epi}} (t_{\text{epi}} - t_p - \text{well})}{\text{width}_{\text{transistor}}} + \frac{k_p \text{width}_{\text{transistor}} t_{\text{poly}}}{\text{width}_{\text{transistor}}} + \frac{2k_{\text{diffusion}} t_{\text{n+sd}} d_{\text{via}}}{\text{width}_{\text{transistor}}} + \frac{k_{\text{poly}} \text{length}_{\text{transistor}} t_{\text{poly}}}{\text{width}_{\text{transistor}}} + \frac{8k_{\text{ild}} k_{\text{via-lateral}} d_{\text{via}}^2}{\text{width}_{\text{transistor}} k_{\text{via-lateral}} d_{\text{via}}^2} \right) }{ \frac{k_p - \text{well}}{\text{width}_{\text{transistor}}} \text{length}_{\text{transistor}} t_{\text{n+sd}} + \frac{2d_{\text{via}} k_{\text{via-lateral}} (2\text{width}_{\text{transistor}} - \text{Width}_{\text{transistor}}) k_{\text{ild}} \text{width}_{\text{transistor}} \text{Width}_{\text{transistor}}}{\text{width}_{\text{transistor}}}} \quad (2.58)$$

$$R_{\text{mosfet-lateral}\parallel} = \left(2(R_{\text{diffusion}} + R_{P-\text{well-under-poly}}) \parallel R_{P-\text{well-under-transistor}} \parallel R_{\text{epi}} \right) \left(2 \left(\frac{R_{\text{ild-between-vias}} \parallel \frac{R_{\text{via}}}{\text{Width}_{\text{transistor}}}}{2h_{\text{via}}} \right) + (R_{\text{polysilicon}} \parallel R_{\text{ild-above-polysilicon}}) \right) \quad (2.59)$$

$$k_{\text{mosfet_lateral-}\parallel} = \left(\frac{(2d_{v\text{ia}} + \text{length}_{\text{transistor}})}{(t_{\text{pepi}} + t_{\text{pmdd}}) \text{width}_{\text{transistor}}} \right) \parallel \left(\frac{\frac{1}{2d_{v\text{ia}}} \left(\left(\frac{\text{width}_{\text{transistor}} t_{n+sd} k_{\text{diffusion}}}{2d_{v\text{ia}}} + \frac{\text{length}_{\text{transistor}}}{k_{\text{pwel}} \text{width}_{\text{transistor}} t_{n+sd}} \right) \parallel \left(\frac{\text{length}_{\text{transistor}} + 2d_{v\text{ia}}}{\text{width}_{\text{transistor}} (t_{\text{pepi}} - t_{n+sd}) k_{\text{pwel}}} \right) \right) \parallel \left(\frac{\frac{2}{k_{\text{id}} t_{\text{id}}} \left(\frac{d_{v\text{ia}}}{\text{width}_{\text{transistor}} - \frac{\text{width}_{\text{transistor}} d_{v\text{ia}}}{2d_{v\text{ia}}}} \parallel \left(\frac{d_{v\text{ia}}}{k_{\text{v}} d_{v\text{ia}} t_{\text{via}} \frac{\text{width}_{\text{transistor}}}{2d_{v\text{ia}}}} \right) + \left(\frac{\text{length}_{\text{transistor}}}{k_{\text{poly}} \text{width}_{\text{transistor}} t_{\text{poly}}} \parallel \frac{\text{length}_{\text{transistor}}}{k_{\text{id}} \text{width}_{\text{transistor}} (t_{\text{id}} - t_{\text{poly}})} \right) \right) \parallel \left(\frac{\text{length}_{\text{transistor}} + 2d_{v\text{ia}}}{\text{width}_{\text{transistor}} (t_{\text{pepi}} - t_{\text{pwel}}) k_{\text{pepi}}} \right) \right) \parallel \left(\frac{\text{length}_{\text{transistor}} + 2d_{v\text{ia}}}{\text{width}_{\text{transistor}} (t_{\text{pepi}} - t_{\text{poly}}) k_{\text{poly}}} \right) \right) \parallel \left(\frac{\text{length}_{\text{transistor}} + 2d_{v\text{ia}}}{\text{width}_{\text{transistor}} (t_{\text{pepi}} - t_{\text{poly}}) k_{\text{poly}}} \right) \right) \quad (2.60)$$

Simplified:

$$k_{\text{mosfet-lateral}\parallel} = \frac{(2d_{\text{via}} + \text{length}_{\text{transistor}}) /}{\left((t_{\text{pepi}} + t_{\text{pmd}}) \text{width}_{\text{transistor}} \left(\frac{k_{\text{diffusion}} k_{\text{pwell}} t_{n+sa} \text{width}_{\text{transistor}}}{2d_{\text{via}} k_{\text{pwell}}} + \frac{k_{\text{pepi}} \text{width}_{\text{transistor}} (t_{\text{pepi}} - t_{\text{pwell}}) + k_{\text{pwell}} \text{width}_{\text{transistor}} (t_{\text{pwell}} - t_{n+sa})}{2d_{\text{via}} + \text{length}_{\text{transistor}}} \right) \right)} \quad (2.61)$$

$$k_{\text{transistor_layer_||}} = \left(\frac{\text{length}_{\text{fp_unit}}}{\text{width}_{\text{fp_unit}} (t_{\text{iild}} + t_{\text{pepi}})} \right) / \left(\left(\frac{\text{length}_{\text{fp_unit}}}{\text{length}_{\text{cell}}} \right) \left(\left(\frac{\text{length}_{\text{cell}}}{2k_{\text{poly_iild_contacts_diffusion_eq_lateral_||}}} \right)^{\frac{\text{width}_{\text{cell}} - (2d_{\text{via}} + \text{length}_{\text{transistor}})}{2}} (t_{\text{iild}} + t_{\text{pepi}}) \right)^{-1} + \left(\frac{\text{width}_{\text{cell}} - W_{\text{transistor}}}{2(L_{\text{cell}} - W_{\text{transistor}})} \right)^{-1} \right)^{-1} \right) \quad (2.62)$$

Simplified:

$$k_{\text{transistor_layer-}\parallel} = \frac{1}{W_{\text{cell}} \cdot \text{width}_{\text{flop_unit}}} k_{\text{poly-ILD_contacts,diffusion_eq,lateral-}\parallel} \cdot \text{length}_{\text{cell}} W_{\text{flop_unit}} \\ \left(\frac{-2d_{\text{via}} - \text{length}_{\text{transistor}} + \text{width}_{\text{cell}}}{\text{length}_{\text{cell}}} + \frac{k_{\text{mosfet_lateral-}\parallel} (2d_{\text{via}} + \text{length}_{\text{transistor}})}{k_{\text{mosfet_lateral-}\parallel} (L_{\text{cell}} - W_{\text{transistor}}) + k_{\text{poly-ILD_contacts,diffusion_eq,lateral-}\parallel} \cdot \text{width}_{\text{transistor}}} \right) \quad (2.63)$$

$$k_{\text{transistor_layer_}\perp} = \left(\frac{\text{length}_{\text{fip-unit}}}{\text{width}_{\text{fip-unit}} (t_{\text{id}} + t_{\text{pepi}})} \right) / \left(\left(\frac{\frac{W_{\text{fip-unit}}}{W_{\text{cell}}}}{\frac{\text{length}_{\text{fip-unit}}}{\text{length}_{\text{cell}}}} \right)^{-1} + \left(\left(\frac{\frac{2k_{\text{poly_ild_contacts_diffusion_eq_lateral_}\perp}}{\text{width}_{\text{cell}}} \frac{\text{length}_{\text{cell}} - \text{width}_{\text{transistor}}}{2} (t_{\text{id}} + t_{\text{pepi}})} \right)^{-1} + \left(\frac{k_{\text{mosfet_lateral_}\perp} \frac{\text{length}_{\text{transistor}} + 2d_{\text{via}}}{(\text{width}_{\text{transistor}}) (t_{\text{id}} + t_{\text{pepi}})} + \frac{k_{\text{poly_ild_contacts_diffusion_eq_lateral_}\perp}}{(\text{width}_{\text{transistor}}) (t_{\text{id}} + t_{\text{pepi}})} \right)^{-1} \right) \right) \right) \quad (2.64)$$

Simplified:

$$k_{\text{transistor_layer_}\perp} = \frac{k_{\text{poly_ild_contacts_diffusion_eq_lateral_}\perp} (\text{length}_{\text{cell}} - \text{width}_{\text{transistor}})}{\text{width}_{\text{cell}}} + \frac{1}{\frac{2d_{\text{via}} + \text{length}_{\text{transistor}}}{k_{\text{mosfet_lateral_}\perp} (\text{width}_{\text{transistor}})} + \frac{-2d_{\text{via}} - \text{length}_{\text{transistor}} + \text{width}_{\text{cell}}}{k_{\text{poly_ild_contacts_diffusion_eq_lateral_}\perp} (\text{width}_{\text{transistor}})}} \quad (2.65)$$

2.5.5.3 Silicon-on-Insulator CMOS Layer Model

A silicon-on-insulator (SOI) MOSFET can be seen in figure 2.39. These devices are designed out of a need solve many electrical and thermal problems with bulk-SOI devices. In particular, the leakage of current between adjacent bulk-silicon transistors can cause undesirable electrical behavior, which reduces device performance. Further, the current leakage, which worsens as the lithography technology improves, causes devices to draw power even when idle. This is a waste of energy, and this further drives up temperatures – forcing designers to scale back performance targets.

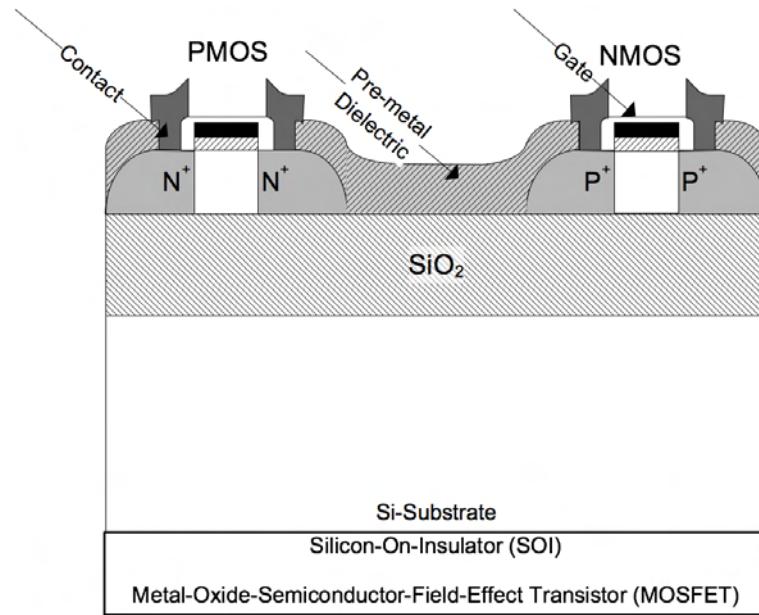


Figure 2.39: Diagram for Silicon-on-Insulator (SOI) MOSFET

To solve the problem of current leaking between transistor devices, each SOI transistor is electrically insulated from the silicon substrate and adjacent SOI transistors.

As can be seen in figure 2.39, each SOI MOSFET is etched into a thin layer of bulk silicon that is insulated from the rest of the silicon substrate through the use of a “buried-oxide” (BOX) layer of electrical insulation material. Further, LOCOS (local oxidation of silicon) or STI (shallow trench isolated) is used to insulate adjacent transistors through the deposition of an electrical insulator material around each transistor.

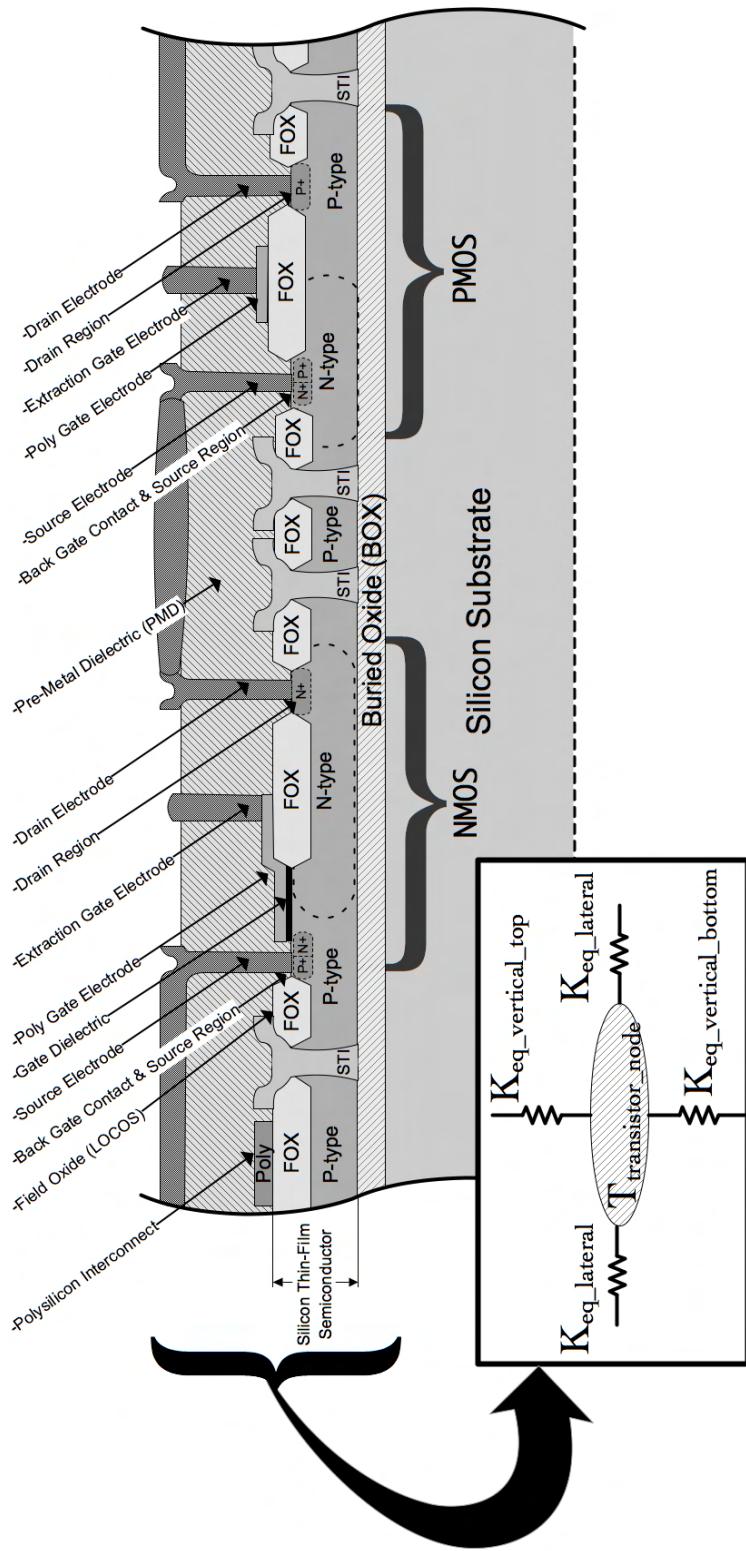


Figure 2.40: Detailed Electrothermal Model Design of Transistor Layer Using Silicon-on-Insulator Technology

This electrical isolation has many benefits. It reduces the silicon real-estate area necessary to implement a given design (increases the integration density), while reducing the overall power utilization at the same time. This is possible because the electrical isolation between transistors allows for tighter design layout rules [113]. Further, the reduction in leakage current means that overall leakage power can decrease dramatically. This means that there can be a performance improvement equivalent to that obtained by moving to the next technology node [113].

The thermal model in Sesctherm is based upon Semiconductor CMOS SOI, US Patent 6,975,003 [77]. As shown in figure 2.40, the silicon-on-insulator device has a more complex geometry than the bulk-silicon MOSFET devices describe previously. It can be seen that the physical model in figure 2.40 closely matches scanning-electron-microscope images in figure 2.41.

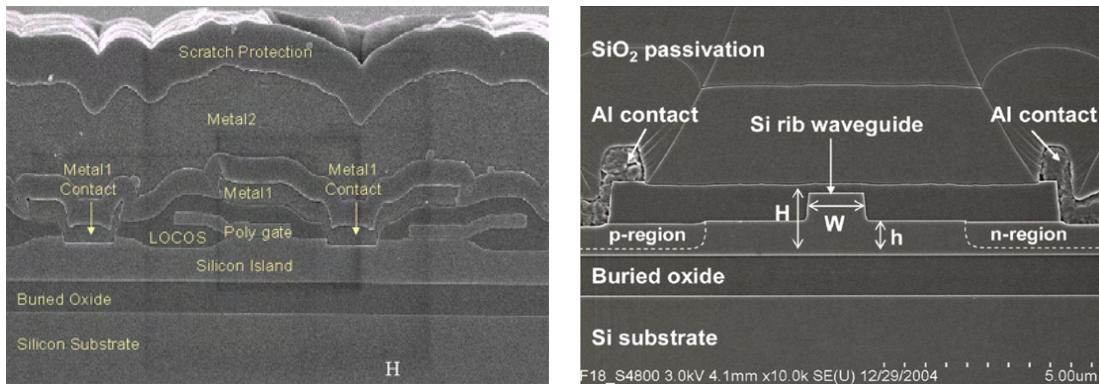


Figure 2.41: Side-view of Silicon-on-Insulator MOSFET Devices

The thermal model that Sesctherm uses is a more accurate representation of the material distribution within the transistor layer of a silicon-on-insulator technology

process than has been described in several other papers [70, 121]. In particular, previous approaches have modeled a simplified transistor geometry. It can be seen in figure 2.40, that both NMOS and PMOS, SOI transistor devices exhibit geometrical variations from the typical transistor device. In particular, the extraction gate electrode for an NMOS transistor is offset from the polysilicon gate electrode, while field oxide (FOX) is used instead of a traditional gate dielectric. Further, Sesctherm models the effective vertical and lateral heat flow through the interconnect distribution in the same manner as was performed for bulk silicon transistor devices. However, unlike the bulk silicon devices described previously, a combination of STI and FOX is used to insulate both NMOS and PMOS transistor devices and also to insulate the polysilicon interconnect from the underlying p-type silicon thin-film.

Using the same methodology described previously to characterize both the lateral and vertical thermal resistance of the bulk silicon transistor layer, Sesctherm computes the lumped resistance values for the SOI technology transistor layer. The transistor layer is defined as the vertical region below the metal interconnect of the first metal interconnect layer and above the bulk silicon substrate. This is shown in figure 2.40. Further, the lateral resistance is characterized both parallel and perpendicular to the routing direction of the interconnect.

The vertical resistance to the first metal interconnect layer above is first described in equation (2.66). This is further developed in equation (2.67), and it is simplified in equation (2.68). Similarly, the vertical resistance to the bulk silicon substrate below is first described by equation (2.69). This is further developed in equation (2.70),

and it is simplified in equation (2.71). The lateral resistance, not including the transistors, parallel to the routing direction of the interconnect is described in equations (2.75) and (2.76). This is simplified in equation (2.77). The lateral resistance, not including the transistors, perpendicular to the routing direction of the interconnect is described in equations (2.72) and (2.73). This is simplified in equation (2.74).

The lateral resistance perpendicular to the routing direction of the interconnect for NMOS devices is described in transistor (2.78). This is further developed in equation (2.79), and it is simplified in equation (2.80). Similarly, the lateral resistance parallel to the routing direction for NMOS devices, in simple, detailed, and simplified form can be found in equations (2.81) ,(2.82), and (2.83).

The lateral resistance perpendicular to the routing direction of the interconnect for PMOS devices is described in transistor (2.84). This is further developed in equation (2.85), and it is simplified in equation (2.86). Similarly, the lateral resistance parallel to the routing direction for PMOS devices, in simple, detailed, and simplified form can be found in equations (2.87) ,(2.88), and (2.89).

The unified model that makes of use of the NMOS and PMOS lumped lateral and vertical resistance models is the same one used for the bulk silicon transistor model described above. Specifically, equations (2.63) and (2.65) are used for lateral resistance of the entire transistor layer in parallel and perpendicular to the routing direction of the interconnect respectively. To determine the vertical resistance, it is a simple parallel resistance of the vertical resistance through the NMOS and PMOS SOI devices along with the interconnect.

$$\begin{aligned}
R_{\text{vertical_top}} = & R_{\text{pmnd_vertical}} \| R_{\text{contact_to_diffusion_vertical}} \| \\
& \left(\left(R_{\text{contact_to_poly}} \| R_{\text{PMD_vertical_to_poly}} \right) + R_{\text{poly_vertical}} \right) \| \\
& \left(\left(R_{\text{contact_to_gate}} \| R_{\text{pmnd_to_gate}} \right) + R_{\text{fox}} + R_{\text{gate}} \right) \| \\
& \left(R_{\text{PMD_vertical_to_gate}} + R_{\text{PMD_vertical_to_poly}} + R_{\text{PMD_vertical_to_diffusion}} \right)
\end{aligned} \tag{2.66}$$

$$R_{\text{vertical,top}} =$$

$$\begin{aligned}
& k_{\text{id}} \left(\frac{0.88 t_{\text{PMD}}}{\text{width}_{\text{fp-unit}}} + 1 \right) \left(-\pi ((e_{\text{transistors-via}} + 2) N_{\text{transistors}}) \left(\frac{d_{\text{via}}}{2} \right)^2 - w_{\text{poly}} \int_{L_{\min}}^{L_{\max}} i(l) dl - W_{\text{gate}} L_{\text{gate}} N_{\text{transistors}} + l_{\text{fp-unit}} w_{\text{fp-unit}} \right) \\
& \left(\frac{t_{\text{PMD}}}{k_{\text{via}} \pi \left(\frac{d_{\text{via}}}{2} \right)^2 N_{\text{transistors}} \{R_{\text{contact-to-diffusion-vertical}}\}} \right) \\
& \left(\left(\frac{\left(t_{\text{PMD}} - t_{\text{poly}} \right)}{k_{\text{via}} \pi \left(\frac{d_{\text{via}}}{2} \right)^2 2 \int_{L_{\min}}^{L_{\max}} i(l) dl} \right) \left(1 + 0.88 \frac{t_{\text{PMD}}}{\text{width}_{\text{fp-unit}}} \right) \left(w_{\text{poly}} \int_{L_{\min}}^{L_{\max}} i(l) dl - \pi \left(\frac{d_{\text{via}}}{2} \right)^2 2 \int_{L_{\min}}^{L_{\max}} i(l) dl \right) \right) \\
& \left(\left(\frac{\left(t_{\text{PMD}} - t_{\text{poly}} \right)}{k_{\text{via}} \pi \left(\frac{d_{\text{via}}}{2} \right)^2 e_{\text{transistor-via}} N_{\text{transistors}} \{R_{\text{contact-to-gate}}\}} \right) \left(1 + 0.88 \frac{t_{\text{PMD}}}{\text{width}_{\text{fp-unit}}} \right) \left(W_{\text{gate}} * L_{\text{gate}} * N_{\text{transistors}} - \pi \left(\frac{d_{\text{via}}}{2} \right)^2 e_{\text{transistor-via}} N_{\text{transistors}} \right) \right) \\
& \left(\frac{t_{\text{fox}}}{k_{\text{fox}} W_{\text{gate}} * L_{\text{gate}} * N_{\text{transistors}} \{R_{\text{fox}}\}} + \left(\frac{t_{\text{poly}}}{k_{\text{poly}} W_{\text{gate}} * L_{\text{gate}} * N_{\text{transistors}} \{R_{\text{contact-to-gate}}\}} \right) \right. \\
& \left. \left(t_{\text{PMD}} - t_{\text{poly}} - t_{\text{gate}} \right) \right) \\
& \left(\frac{k_{\text{id}} \left(1 + 0.88 \frac{t_{\text{PMD}}}{\text{width}_{\text{fp-unit}}} \right) \left(l_{\text{fp-unit}} * w_{\text{fp-unit}} - \pi \left(\frac{d_{\text{via}}}{2} \right)^2 \left((2 + e_{\text{transistor-via}}) N_{\text{transistors}} + 2 \int_{L_{\min}}^{L_{\max}} i(l) dl \right) \right)}{t_{\text{gate}} \{R_{\text{PMD-vertical-to-gate}}\}} \right. \\
& \left. \left(k_{\text{id}} \left(1 + 0.88 \frac{t_{\text{PMD}}}{\text{width}_{\text{fp-unit}}} \right) \left(l_{\text{fp-unit}} * w_{\text{fp-unit}} - \pi \left(\frac{d_{\text{via}}}{2} \right)^2 \left((2) N_{\text{transistors}} + 2 \int_{L_{\min}}^{L_{\max}} i(l) dl \right) - W_{\text{gate}} * L_{\text{gate}} * N_{\text{transistors}} \right) \right) \right) \\
& \left(\frac{t_{\text{poly}}}{\left(k_{\text{id}} \left(1 + 0.88 \frac{t_{\text{PMD}}}{\text{width}_{\text{fp-unit}}} \right) \left(l_{\text{fp-unit}} * w_{\text{fp-unit}} - \pi \left(\frac{d_{\text{via}}}{2} \right)^2 (2) N_{\text{transistors}} \right) \right) \{R_{\text{PMD-vertical-to-diffusion}}\}} \right)
\end{aligned} \tag{2.67}$$

Simplified:

$$\begin{aligned}
& \frac{1}{\left(\frac{t_{\text{fox}}}{k_{\text{fox}} L_{\text{gate}} W_{\text{gate}}} + \frac{4(t_{\text{gate}} - t_{\text{PMD}} + t_{\text{poly}})}{\pi d_{\text{via}}^2 e_{\text{transistors-via}} - 4L_{\text{gate}} W_{\text{gate}}} k_{\text{id}} \left(\frac{0.88t_{\text{PMD}}}{\text{width}_{\text{fp-unit}}} + 1 \right) - 4\pi \left[\frac{d_{\text{via}}}{2} \right]^2 e_{\text{transistor-via}} k_{\text{via}} \right.} \\
& \left. + \frac{k_{\text{gate-dielectric}} t_{\text{poly}} + k_{\text{poly}} t_{\text{gate-dielectric}}}{k_{\text{poly}} k_{\text{gate-dielectric}} L_{\text{gate}} W_{\text{gate}}} \right) + \\
& k_{\text{id}} \left(\frac{0.88t_{\text{PMD}}}{\text{width}_{\text{fp-unit}}} + 1 \right) / \left(-\frac{\pi d_{\text{via}}^2 N_{\text{transistors}} - 2l_{\text{fp-unit}} w_{\text{fp-unit}}}{2t_{\text{poly}}} + \frac{4(t_{\text{gate}} - t_{\text{PMD}} + t_{\text{poly}})}{\pi d_{\text{via}}^2 \left(2 \int_{L_{\text{min}}}^{L_{\text{max}}} i(l) dl + (e_{\text{transistors-via}} + 2) N_{\text{transistors}} \right) - 4l_{\text{fp-unit}} w_{\text{fp-unit}}} \right. \\
& \left. - \frac{2t_{\text{gate}}}{\pi \left(\int_{L_{\text{min}}}^{L_{\text{max}}} i(l) dl + N_{\text{transistors}} \right) d_{\text{via}}^2 - 2l_{\text{fp-unit}} w_{\text{fp-unit}} + 2L_{\text{gate}} N_{\text{transistors}} V_{\text{gate}}}} \right. \\
& \left. + \frac{\pi k_{\text{via}} N_{\text{transistors}} d_{\text{via}}^2}{2t_{\text{PMD}}} \right) + \\
& \left(4 \left(\int_{L_{\text{min}}}^{L_{\text{max}}} i(l) dl \right) w_{\text{poly}} - 4l_{\text{fp-unit}} w_{\text{fp-unit}} + N_{\text{transistors}} \left(e_{\text{transistors-via}} + 2 \right) \pi d_{\text{via}}^2 + 4L_{\text{gate}} W_{\text{gate}} \right) k_{\text{id}} \left(\frac{0.88t_{\text{PMD}}}{\text{width}_{\text{fp-unit}}} + 1 \right) \right) + \\
& 4t_{\text{PMD}} \\
& \left. \frac{1}{\left(\int_{L_{\text{min}}}^{L_{\text{max}}} i(l) dl \right) k_{\text{poly}} w_{\text{poly}} + \frac{2(t_{\text{PMD}} - t_{\text{poly}})}{4 \left(\int_{L_{\text{min}}}^{L_{\text{max}}} i(l) dl \right) k_{\text{via}} \pi \left[\frac{d_{\text{via}}}{2} \right]^2 + \left(2 \int_{L_{\text{min}}}^{L_{\text{max}}} i(l) dl \right) w_{\text{poly}} - \pi \left(\int_{L_{\text{min}}}^{L_{\text{max}}} i(l) dl \right) d_{\text{via}}^2 \right) k_{\text{id}} \left(\frac{0.88t_{\text{PMD}}}{\text{width}_{\text{fp-unit}}} + 1 \right)} \right)
\end{aligned} \tag{2.68}$$

$$k_{\text{transistor_layer_vertical_bottom}} = \frac{t_{\text{ild}} + t_{\text{thin_film}} + t_{\text{box}}}{\text{width}_{\text{flip-unit}} \text{length}_{\text{flip-unit}}} - 1 / \left(\left(\frac{t_{\text{box}}}{k_{\text{box}} \text{width}_{\text{flip-unit}} \text{length}_{\text{flip-unit}}} + \left(\left(\frac{t_{\text{fox}}}{k_{\text{fox}} \left(\text{width}_{\text{poly}} \int_{L_{\min}}^{L_{\max}} i(l) dl \right)} + \frac{\left(t_{\text{thin_film}} - t_{\text{fox}} \right)}{k_{\text{thin_film}} \left(\text{width}_{\text{poly}} \int_{L_{\min}}^{L_{\max}} i(l) dl \right)} \right) \right) \right) \right) \\ + \left(\left(\frac{t_{\text{fox}}}{k_{\text{fox}} \text{width}_{\text{transistor}} N_{\text{transistor}}} + \frac{t_{\text{thin_film}} - t_{\text{fox}}}{k_{\text{thin_film}} \text{width}_{\text{transistor}} N_{\text{transistor}} \text{length}_{\text{transistor}}} \right) \right) \right) \right) \quad (2.69)$$

$$k_{\text{transistor_layer_vertical_bottom}} = \frac{t_{\text{ild}} + t_{\text{thin_film}} + t_{\text{box}}}{\text{width}_{\text{flip-unit}} \text{length}_{\text{flip-unit}}} - 1 / \left(\left(\frac{t_{\text{box}}}{k_{\text{box}} \text{width}_{\text{flip-unit}} \text{length}_{\text{flip-unit}}} + \left(\left(\frac{t_{\text{fox}}}{k_{\text{fox}} \text{width}_{\text{flip-unit}} \text{length}_{\text{flip-unit}}} + \frac{\left(t_{\text{thin_film}} - t_{\text{fox}} \right)}{k_{\text{thin_film}} \left(\text{width}_{\text{poly}} \int_{L_{\min}}^{L_{\max}} i(l) dl \right)} \right) \right) \right) \right) \\ + \left(\frac{t_{\text{fox}}}{k_{\text{fox}} \text{width}_{\text{transistor}} N_{\text{transistor}}} + \frac{t_{\text{thin_film}} - t_{\text{fox}}}{k_{\text{thin_film}} \text{width}_{\text{transistor}} N_{\text{transistor}} \text{length}_{\text{transistor}}} \right)^{-1} + \left(\frac{t_{\text{fox}}}{k_{\text{fox}} \text{width}_{\text{transistor}} \text{width}_{\text{transistor}} N_{\text{transistor}} \text{length}_{\text{transistor}}} \right)^{-1} \right) \right) \quad (2.70)$$

Simplified:

$$\frac{(t_{\text{box}} + t_{\text{ild}} + t_{\text{thin_film}}) / \left(\frac{t_{\text{box}}}{k_{\text{box}}} + (\text{length}_{\text{flip-unit}} \text{width}_{\text{flip-unit}}) / \left(\frac{2 k_{\text{sti}} N_{\text{transistor}} \text{width}_{\text{sti}}}{t_{\text{sti}}} + \frac{t_{\text{thin_film}} - t_{\text{fox}}}{k_{\text{thin_film}} \text{length}_{\text{transistor}} N_{\text{transistor}}} + \frac{1}{k_{\text{fox}} N_{\text{transistor}} (\text{length}_{\text{transistor}} - 3 \text{diameter}_{\text{via}})} \right) \right) + \frac{1}{k_{\text{thin_film}} \left(\left(\frac{L_{\max}}{L_{\min}} i(l) dl \right) \text{width}_{\text{poly}} \right) + \frac{t_{\text{fox}}}{k_{\text{fox}} \left(\left(\frac{L_{\max}}{L_{\min}} i(l) dl \right) \text{width}_{\text{poly}} \right)}} \right) \right) \right) \quad (2.71)$$

Simplified:

$$\begin{aligned}
k_{\text{poly-ild-lateral},\parallel} &= \frac{\text{length}_{\text{fp-unit}}}{(t_{\text{ild}} + t_{\text{thin-film}} + t_{\text{box}}) \text{width}_{\text{fp-unit}}} \frac{1}{\text{length}_{\text{fp-unit}}} \\
&= \left(\int_{L_{\min}}^{\frac{L_{\text{cell}}}{N_{\text{transistors}}} (\text{length}_{\text{fp-unit}} / L_{\text{cell}})} \frac{l}{\frac{(i(l)+1)}{N_{\text{transistors}}} (k_{\text{fox}} t_{\text{fox}} s_{\text{poly}})} \right) \left(\frac{l}{\frac{(i(l)+1)}{N_{\text{transistors}}} (k_{\text{ild}} t_{\text{ild}} s_{\text{poly}})} \right) \left(\frac{l}{\frac{(i(l)+1)}{N_{\text{transistors}}} (k_{\text{thin-film}} (t_{\text{thin-film}} - t_{\text{fox}}) s_{\text{poly}})} \right) \left(\frac{l}{\frac{(i(l)+1)}{N_{\text{transistors}}} (k_{\text{box}} t_{\text{box}} s_{\text{poly}})} \right) \\
&\quad \left(\frac{l}{\frac{i(l)}{N_{\text{transistors}}} (k_{\text{box}} t_{\text{box}} w_{\text{poly}})} \right) \left(\frac{l}{\frac{i(l)}{N_{\text{transistors}}} (k_{\text{fox}} t_{\text{fox}} w_{\text{poly}})} \right) \left(\frac{l}{\frac{i(l)}{N_{\text{transistors}}} (k_{\text{thin-film}} (t_{\text{thin-film}} - t_{\text{fox}}) w_{\text{poly}})} \right) \left(\frac{l}{\frac{i(l)}{N_{\text{transistors}}} (k_{\text{silicon-thin-film,below-fox}})} \right) \\
&\quad \left(\frac{(l - e_{\text{via}} d_{\text{via}})}{\frac{i(l)}{N_{\text{transistors}}} (k_{\text{ild}} (t_{\text{ild}} - t_{\text{poly}}) w_{\text{poly}})} \right) \left(\frac{e_{\text{via}} d_{\text{via}}}{\frac{i(l)}{N_{\text{transistors}}} (k_{\text{via}} l_{\text{via}} d_{\text{via}})} \right) \left(\frac{l}{\frac{i(l)}{N_{\text{transistors}}} (k_{\text{poly}} t_{\text{poly}} w_{\text{poly}})} \right) \\
&\quad \left(\frac{(L_{\text{cell}} - l)}{\frac{i(L_{\text{cell}} - l)}{N_{\text{transistors}}} (k_{\text{fox}} (t_{\text{fox}}) w_{\text{poly}})} \right) \left(\frac{(L_{\text{cell}} - l - e_{\text{via}} d_{\text{via}})}{\frac{i(L_{\text{cell}} - l)}{N_{\text{transistors}}} (k_{\text{thin-film}} (t_{\text{thin-film}} - t_{\text{fox}}) w_{\text{poly}})} \right) \left(\frac{(L_{\text{cell}} - l - e_{\text{via}} d_{\text{via}})}{\frac{i(L_{\text{cell}} - l)}{N_{\text{transistors}}} (k_{\text{ild}} (t_{\text{ild}} - t_{\text{poly}}) w_{\text{poly}})} \right) \left(\frac{(L_{\text{cell}} - l)}{\frac{i(L_{\text{cell}} - l)}{N_{\text{transistors}}} (k_{\text{via}} l_{\text{via}} d_{\text{via}})} \right) \\
&\quad \left(\frac{(L_{\text{cell}} - l)}{\frac{i(L_{\text{cell}} - l)}{N_{\text{transistors}}} (k_{\text{poly}} t_{\text{poly}} w_{\text{poly}})} \right) \left(\frac{(L_{\text{cell}} - l)}{\frac{i(L_{\text{cell}} - l)}{N_{\text{transistors}}} (k_{\text{box}} (t_{\text{box}}) w_{\text{poly}})} \right) \left(\frac{(L_{\text{cell}} - l)}{\frac{i(L_{\text{cell}} - l)}{N_{\text{transistors}}} (k_{\text{thin-film}} (t_{\text{thin-film}} - t_{\text{fox}}) w_{\text{poly}})} \right) \left(\frac{(L_{\text{cell}} - l)}{\frac{i(L_{\text{cell}} - l)}{N_{\text{transistors}}} (k_{\text{box}} t_{\text{box}} w_{\text{poly}})} \right) \\
&\quad \left(\frac{(L_{\text{cell}} - l)}{\frac{(i(L_{\text{cell}} - l) + 1)}{N_{\text{transistors}}} k_{\text{thin-film}} (t_{\text{thin-film}} - t_{\text{fox}}) s_{\text{poly}}^{-1}} \right) \left(\frac{(L_{\text{cell}} - l)}{\frac{(i(l) - i(L_{\text{cell}} - l))}{N_{\text{transistors}}} k_{\text{thin-film}} (t_{\text{thin-film}} - t_{\text{fox}}) w_{\text{poly}}^{-1}} \right) \left(\frac{(L_{\text{cell}} - l)}{\frac{(i(L_{\text{cell}} - l) + 1)}{N_{\text{transistors}}} k_{\text{ild}} (t_{\text{poly}}) s_{\text{poly}}^{-1}} \right) \left(\frac{(L_{\text{cell}} - l)}{\frac{(i(l) - i(L_{\text{cell}} - l))}{N_{\text{transistors}}} k_{\text{ild}} (t_{\text{fox}}) w_{\text{poly}}^{-1}} \right) \\
&\quad \left(\frac{(L_{\text{cell}} - l)}{\frac{(i(L_{\text{cell}} - l) + 1)}{N_{\text{transistors}}} k_{\text{box}} (t_{\text{box}}) s_{\text{poly}}^{-1}} \right) \left(\frac{(L_{\text{cell}} - l)}{\frac{(i(l) - i(L_{\text{cell}} - l))}{N_{\text{transistors}}} k_{\text{box}} (t_{\text{box}}) w_{\text{poly}}^{-1}} \right) \left(\frac{(L_{\text{cell}} - l)}{\frac{(i(L_{\text{cell}} - l) + 1)}{N_{\text{transistors}}} k_{\text{box}} t_{\text{box}} (t_{\text{box}}) w_{\text{poly}}^{-1}} \right) \left(\frac{(L_{\text{cell}} - l)}{\frac{(i(l) - i(L_{\text{cell}} - l))}{N_{\text{transistors}}} k_{\text{box}} t_{\text{box}} s_{\text{poly}}^{-1}} \right) \\
&\quad + \text{rest of RHS (See Equation (2.76))}
\end{aligned} \tag{2.75}$$

$$\begin{aligned}
& \frac{\text{length}_{\text{fp-unit}}}{L_{\text{cell}}} \sum_{n=1}^{(n+1)L_{\text{cell}}} \frac{\text{length}_{\text{fp-unit}}/L_{\text{cell}}(n+1)}{(\text{width}_{\text{fp-unit}}/W_{\text{cell}})} \left(\left(\frac{l}{\frac{(i(l)+1)}{(n+1)N_{\text{transistors}}}\frac{(k_{\text{box}}t_{\text{box}}s_{\text{poly}})}{\{R_{\text{box_below_ild}}\}}} \right)^l \right. \\
& \quad \left. \left| \frac{\frac{(i(l)+1)}{(n+1)N_{\text{transistors}}}\frac{(k_{\text{tox}}t_{\text{fox}}s_{\text{poly}})}{\{R_{\text{box_below_ild}}\}}}{\frac{k_{\text{ild}}t_{\text{ild}}s_{\text{poly}}}{\{R_{\text{ild_between_poly}}\}}} \right|^l \right) \frac{l}{\frac{(n+l)(i(l)+1)}{(n+1)N_{\text{transistors}}}\frac{(k_{\text{thin_film}}(t_{\text{thin_film}} - t_{\text{fox}})s_{\text{poly}})}{\{R_{\text{silicon_thin_film_below_fox}}\}}}} \\
& \quad \left(\frac{l}{\frac{(n+l)\frac{i(l)}{N_{\text{transistors}}}\frac{(k_{\text{box}}t_{\text{box}}w_{\text{poly}})}{\{R_{\text{box_below_thin_film}}\}}}{\frac{k_{\text{fox}}t_{\text{fox}}w_{\text{poly}}}{\{R_{\text{fox_below_poly}}\}}}} \right)^l \right. \\
& \quad \left. \left| \frac{\frac{(n+l)\frac{i(l)}{N_{\text{transistors}}}\frac{(k_{\text{box}}t_{\text{box}}w_{\text{poly}})}{\{R_{\text{box_below_thin_film}}\}}}{\frac{k_{\text{fox}}t_{\text{fox}}w_{\text{poly}}}{\{R_{\text{fox_below_poly}}\}}}}{\frac{(n+l)\frac{i(l)}{N_{\text{transistors}}}\frac{(k_{\text{thin_film}}(t_{\text{thin_film}} - t_{\text{fox}})w_{\text{poly}})}{\{R_{\text{silicon_thin_film_below_fox}}\}}}} \right|^l \right) \\
& \quad \left(\frac{(l - e_{\text{via}}d_{\text{via}})}{\frac{(i(l))}{(n+1)N_{\text{transistors}}}\frac{(k_{\text{ild}}(t_{\text{ild}} - t_{\text{poly}})w_{\text{poly}})}{\{R_{\text{ild_above_poly}}\}}}} \right)^l \right. \\
& \quad \left. \left| \frac{\frac{e_{\text{via}}d_{\text{via}}}{(n+1)\frac{i(l)}{N_{\text{transistors}}}\frac{(k_{\text{via}}l_{\text{via}}d_{\text{via}})}{\{R_{\text{via_above_poly}}\}}}}{\frac{(n+1)\frac{i(l)}{N_{\text{transistors}}}\frac{(k_{\text{poly}}l_{\text{poly}}w_{\text{poly}})}{\{R_{\text{poly}}\}}}} \right|^l \right) \right) \quad (2.76)
\end{aligned}$$

Simplified:

$$\begin{aligned}
k_{\text{poly_ild_lateral_||}} &= \frac{1}{(t_{\text{box}} + t_{\text{ild}} + t_{\text{thin_film}}) \text{width}_{\text{fp_unit}}} \text{length}_{\text{fp_unit}} \left(\int_{L_{\min}}^{L_{\text{cell}}} (\text{length}_{\text{fp_unit}} W_{\text{cell}}) / (L_{\text{cell}} N_{\text{transistors}} \text{width}_{\text{fp_unit}}) \right. \\
&\quad \left(\frac{i(L_{\text{cell}} - l) \left(\frac{k_{\text{via}}l_{\text{via}}}{e_{\text{via}}} + \left(\frac{k_{\text{poly}}t_{\text{poly}}}{L_{\text{cell}} - l} + \frac{k_{\text{ild}}(t_{\text{ild}} - t_{\text{poly}})}{l - L_{\text{cell}}} - \frac{k_{\text{box}}(t_{\text{box}} - t_{\text{poly}})}{l - d_{\text{via}}e_{\text{via}} - L_{\text{cell}}} \right) w_{\text{poly}} \right) + \frac{((i(l - iL_{\text{cell}} - 1)s_{\text{poly}} - i(l)w_{\text{poly}})(k_{\text{box}}(t_{\text{box}} + k_{\text{fox}}(t_{\text{fox}} + k_{\text{ild}}(t_{\text{poly}} + k_{\text{thin_film}} - t_{\text{fox}}))) + k_{\text{thin_film}}(t_{\text{thin_film}} - t_{\text{fox}}))}{l - L_{\text{cell}}} \right. \\
&\quad \left. + \frac{1}{e_{\text{via}}} \left(\frac{(i(l)k_{\text{via}}l_{\text{via}}}{e_{\text{via}}} + \frac{(i(l) + 1)k_{\text{box}}s_{\text{poly}}t_{\text{box}}}{l} + \frac{(i(l) + 1)k_{\text{tox}}s_{\text{poly}}t_{\text{fox}}}{l} + \frac{(i(l) + 1)k_{\text{ild}}s_{\text{poly}}t_{\text{ild}}}{l} + \frac{i(l)k_{\text{box}}t_{\text{box}}w_{\text{poly}}}{l} + \frac{i(l)k_{\text{fox}}t_{\text{fox}}w_{\text{poly}}}{l} + \frac{i(l)k_{\text{poly}}k_{\text{thin_film}}(t_{\text{thin_film}} - t_{\text{fox}})}{l - d_{\text{via}}e_{\text{via}}} + \frac{i(l)w_{\text{poly}}k_{\text{thin_film}}(t_{\text{thin_film}} - t_{\text{fox}})}{l - d_{\text{via}}e_{\text{via}}} \right) \right) \right) dl + \\
&\quad \frac{\text{length}_{\text{fp_unit}}}{L_{\text{cell}}} \sum_{n=1}^{(n+1)L_{\text{cell}}} \frac{1}{nL_{\text{cell}}} \left(\text{length}_{\text{fp_unit}} W_{\text{cell}} \left(\frac{i(l)k_{\text{via}}l_{\text{via}}}{e_{\text{via}}} + \frac{(i(l) + 1)k_{\text{box}}s_{\text{poly}}t_{\text{box}}}{l} + \frac{(i(l) + 1)k_{\text{fox}}s_{\text{poly}}t_{\text{fox}}}{l} + \frac{(i(l) + 1)k_{\text{ild}}s_{\text{poly}}t_{\text{ild}}}{l} + \frac{i(l)k_{\text{box}}t_{\text{box}}w_{\text{poly}}}{l} + \frac{i(l)k_{\text{poly}}k_{\text{thin_film}}(t_{\text{thin_film}} - t_{\text{fox}})}{l} + \frac{i(l)w_{\text{poly}}k_{\text{thin_film}}(t_{\text{thin_film}} - t_{\text{fox}})}{l} \right) / ((n+1)L_{\text{cell}}(n+1)N_{\text{transistors}} \text{width}_{\text{fp_unit}}) \right) dl \quad (2.77)
\end{aligned}$$

$$\begin{aligned}
R_{\text{nnos-mosfet-lateral-}\perp} &= R_{\text{box}} \parallel ((2R_{\text{sti_below_gate}} + R_{\text{thin-film}}) \parallel \\
&\quad (2R_{\text{sti_beside_gate}} + 2R_{\text{fox_beside_gate}} + R_{\text{fox_under_gate}} + 2R_{\text{sd_electrode_beside_gate}} + (R_{\text{poly}} \parallel R_{\text{gate_dielectric}})) \parallel \\
&\quad (R_{\text{pmd_over_sti_fox_gate}} + 2R_{\text{sd_electrode_beside_gate}} + R_{\text{extraction_gate_electrode}} + R_{\text{poly}}))
\end{aligned} \tag{2.78}$$

$$\begin{aligned}
\text{length}_{\text{transistor}} &= (2w_{\text{sti}} + 2w_{\text{fox_beside_gate}} + w_{\text{fox_under_gate}} + \text{length}_{\text{gate}} + 2d_{\text{via}}) \\
\text{width}_{\text{transistor}} &= \text{width}_{\text{gate}}
\end{aligned}$$

$$\begin{aligned}
k_{\text{nnos-mosfet-lateral-}\perp} &= \\
&\frac{\text{length}_{\text{transistor}}}{(t_{\text{thin_film}} + t_{\text{pmd}} + t_{\text{box}}) \text{width}_{\text{transistor}}} \cdot \frac{1}{\left(\frac{\text{length}_{\text{transistor}}}{k_{\text{box}} t_{\text{box}} \text{width}_{\text{transistor}} \{R_{\text{box}}\}} \right)} \left(\frac{2w_{\text{sti}}}{k_{\text{sti}} (t_{\text{thin_film}} - t_{\text{fox}}) \text{width}_{\text{transistor}}} + \frac{\text{length}_{\text{transistor}} - 2w_{\text{sti}}}{k_{\text{thin_film}} (t_{\text{thin_film}} - t_{\text{fox}}) \text{width}_{\text{transistor}}} \right) \\
&\left(\frac{2w_{\text{sti}}}{k_{\text{sti}} (t_{\text{fox}}) \text{width}_{\text{transistor}}} + \frac{2w_{\text{fox_beside_gate}}}{k_{\text{fox}} (t_{\text{fox}}) \text{width}_{\text{transistor}}} + \frac{w_{\text{fox_under_gate}}}{k_{\text{fox}} (t_{\text{fox}}) \text{width}_{\text{transistor}}} + \right. \\
&\quad \left. \frac{2d_{\text{via}}}{k_{\text{via}} (l_{\text{via}}) (d_{\text{via}})} + \left(\frac{\text{length}_{\text{gate}}}{k_{\text{poly}} (t_{\text{poly}}) \text{width}_{\text{transistor}}} \parallel \frac{k_{\text{gate_dielectric}} (t_{\text{gate_dielectric}}) \text{width}_{\text{transistor}}}{\{R_{\text{gate_dielectric}}\}} \right) \right) \parallel \\
&\left(\frac{k_{\text{pmd}} (t_{\text{pmd}} - t_{\text{gate_dielectric}} - t_{\text{poly}}) \text{width}_{\text{transistor}}}{\{R_{\text{pmd_over_sti_fox_gate}}\}} + \frac{2d_{\text{via}}}{k_{\text{via}} (t_{\text{pmd}}) (d_{\text{via}})} + \frac{k_{\text{via}} (t_{\text{pmd}} - 5t_{\text{fox}} - t_{\text{poly}}) (d_{\text{via}})}{\{R_{\text{extraction_gate_electrode}}\}} + \frac{l_{\text{gate}}}{k_{\text{poly}} (t_{\text{poly}}) \text{width}_{\text{transistor}}} \right)
\end{aligned} \tag{2.79}$$

Simplified:

$$k_{\text{nmos_mosfet_lateral_}\perp} = \frac{1}{t_{\text{box}} + t_{\text{pmd}} + t_{\text{thin_film}}} + \left(\frac{\frac{1}{k_{\text{box}} t_{\text{box}} + \text{length}_{\text{transistor}}} \left(\frac{\frac{1}{\text{width}_{\text{transistor}} \left(\frac{\frac{1}{k_{\text{pmd}}(t_{\text{pmd}} - t_{\text{poly}} - t_{\text{gate_dielectric}})} + \frac{l_{\text{gate}}}{k_{\text{poly}}(t_{\text{poly}})} + \frac{2}{k_{\text{via}}(t_{\text{pmd}})} + \frac{1}{k_{\text{via}}(-0.5t_{\text{fox}} + t_{\text{pmd}} - t_{\text{poly}})}} + \frac{1}{\text{width}_{\text{transistor}} \left(\frac{\frac{1}{k_{\text{sti}}(t_{\text{thin_film}} - t_{\text{fox}})} + \frac{\text{length}_{\text{transistor}} - 2w_{\text{sti}}}{k_{\text{thin_film}}(t_{\text{thin_film}} - t_{\text{fox}})} + \frac{1}{k_{\text{poly}}(t_{\text{poly}}) + k_{\text{gate_dielectric}}(t_{\text{gate_dielectric}})} + \frac{\text{length}_{\text{gate}}}{k_{\text{fox}}(t_{\text{fox}})} + \frac{2w_{\text{fox_beside_gate}} + w_{\text{fox_under_gate}}}{k_{\text{fox}}(t_{\text{fox}})} + \frac{2w_{\text{sti}}}{k_{\text{sti}}(t_{\text{fox}})} + \frac{2\text{width}_{\text{transistor}}}{k_{\text{via}}(l_{\text{via}})}} \right) \right) + \frac{R_{\text{fox_under_gate}}}{R_{\text{poly}} \| R_{\text{gate_electrode}} \| R_{\text{pmd_over_sti_fox_gate}} \| R_{\text{extraction_gate_electrode}} \| R_{\text{poly}}} } }{2} \right) \quad (2.80)$$

$$R_{\text{nmos_mosfet_lateral_}\parallel} = R_{\text{box}} \left| \frac{R_{\text{sti}}}{2} \right\| R_{\text{thin_film}} \left\| \frac{R_{\text{fox_beside_gate}}}{2} \right\| \\ R_{\text{fox_under_gate}} \left\| \frac{R_{\text{ad_electrode}}}{2} \right\| R_{\text{poly}} \| R_{\text{gate_dielectric}} \| R_{\text{pmd_over_sti_fox_gate}} \| R_{\text{extraction_gate_electrode}} \| R_{\text{poly}} \quad (2.81)$$

$$\begin{aligned} \text{length}_{\text{transistor}} &= 2d_{\text{via}} + \text{length}_{\text{gate}} + 2w_{\text{sti}} + 2w_{\text{fox,beside-gate}} + w_{\text{fox,under-gate}} \\ \text{width}_{\text{transistor}} &= \text{width}_{\text{gate}} \end{aligned}$$

$$\begin{aligned} k_{\text{unmos-mosfet-lateral-}\parallel} &= \frac{\text{width}_{\text{transistor}}}{(t_{\text{thin-film}} + t_{\text{pmd}} + t_{\text{box}}) \text{length}_{\text{transistor}}} \\ &= \frac{1}{k_{\text{box}} t_{\text{box}} \text{length}_{\text{transistor}} \left\{ R_{\text{box}} \right\}} \left(\frac{\text{width}_{\text{transistor}}}{\frac{2k_{\text{sti}} (t_{\text{thin-film}}) w_{\text{sti}}}{\left\{ \frac{R_{\text{sti}}}{2} \right\}}} \right) \left(\frac{\text{width}_{\text{transistor}}}{\frac{k_{\text{thin-film}} (t_{\text{thin-film}} - t_{\text{fox}}) (\text{length}_{\text{transistor}} - 2w_{\text{sti}})}{\left\{ R_{\text{thin-film}} \right\}}} \right) \left(\frac{\text{width}_{\text{transistor}}}{\frac{2k_{\text{fox}} (t_{\text{fox}}) (w_{\text{fox-beside-gate}})}{\left\{ R_{\text{fox-beside-gate}} \right\}}} \right) \quad (2.82) \\ &= \frac{k_{\text{fox}} (t_{\text{fox}}) (w_{\text{fox,under-gate}})}{k_{\text{pmd}} (t_{\text{pmd}} - t_{\text{gate-dielectric}}) \left\{ R_{\text{pmd-over-sti-fox-gate}} \right\}} \left(\frac{\text{width}_{\text{transistor}}}{\frac{d_{\text{via}}}{\frac{2k_{\text{via}} (l_{\text{via}}) (d_{\text{via}})}{\left\{ R_{\text{sd-electrode}} \right\}}}} \right) \left(\frac{\text{width}_{\text{transistor}}}{\frac{k_{\text{poly}} (t_{\text{poly}}) (\text{length}_{\text{gate}})}{\left\{ R_{\text{poly}} \right\}}} \right) \left(\frac{\text{width}_{\text{transistor}}}{\frac{k_{\text{poly}} (t_{\text{poly}}) (\text{length}_{\text{gate}})}{\left\{ R_{\text{gate-dielectric}} \right\}}} \right) \\ &= \frac{k_{\text{pmd}} (t_{\text{pmd}} - t_{\text{gate-dielectric}} - t_{\text{poly}}) (\text{length}_{\text{gate}} - 3d_{\text{via}})}{k_{\text{via}} (t_{\text{pmd}} - 5t_{\text{fox}} - t_{\text{poly}}) (d_{\text{via}})} \left(\frac{\text{width}_{\text{transistor}}}{\frac{d_{\text{via}}}{\left\{ R_{\text{extraction-gate-electrode}} \right\}}} \right) \left(\frac{\text{width}_{\text{transistor}}}{\frac{k_{\text{poly}} (t_{\text{poly}}) l_{\text{gate}}}{\left\{ R_{\text{poly}} \right\}}} \right) \end{aligned}$$

Simplified:

$$\begin{aligned} R_{\text{unmos-mosfet-lateral-L}} &= \\ &\frac{1}{\text{length}_{\text{transistor}} (t_{\text{box}} + t_{\text{pmd}} + t_{\text{thin-film}})} \left(k_{\text{box}} \text{length}_{\text{transistor}} t_{\text{box}} + 2k_{\text{sti}} t_{\text{thin-film}} w_{\text{sti}} + (2w_{\text{fox,beside-gate}} + w_{\text{fox,under-gate}}) k_{\text{fox}} t_{\text{fox}} \right) - \quad (2.83) \\ &3d_{\text{via}} k_{\text{pmd}} (t_{\text{pmd}} - t_{\text{poly}} - t_{\text{gate-dielectric}}) + l_{\text{gate}} k_{\text{poly}} (t_{\text{poly}}) + \text{width}_{\text{transistor}} (2k_{\text{via}} (l_{\text{via}}) + k_{\text{via}} (-0.5t_{\text{fox}} + t_{\text{pmd}} - t_{\text{poly}})) + \\ &\text{length}_{\text{gate}} (k_{\text{pmd}} (t_{\text{pmd}} - t_{\text{poly}} - t_{\text{gate-dielectric}}) + k_{\text{poly}} (t_{\text{poly}}) + k_{\text{gate-dielectric}} (t_{\text{gate-dielectric}}) + (l_{\text{gate}}_{\text{transistor}} - 2w_{\text{sti}}) k_{\text{thin-film}} (t_{\text{thin-film}} - t_{\text{fox}})) \end{aligned}$$

$$\begin{aligned} R_{\text{pmos-mosfet-lateral-L}} &= \\ &R_{\text{box}} \left\| (2R_{\text{sti,below-gate}} + R_{\text{thin-film}}) \right\| (2R_{\text{sti,beside-gate}} + 2R_{\text{fox,beside-gate}} + R_{\text{fox,under-gate}} + 2R_{\text{sd-electrode-beside-gate}}) \left\| \right. \\ &\left. (R_{\text{pmd-over-sti-fox-gate}} + 2R_{\text{sd-electrode-beside-gate}} + (R_{\text{extraction-gate-electrode}} \| R_{\text{poly}})) \right\| \quad (2.84) \end{aligned}$$

$$\begin{aligned} \text{length}_{\text{transistor}} &= (2w_{\text{sti}} + 2w_{\text{fox,beside-gate}} + w_{\text{fox-under-gate}} + 2d_{\text{via}}) \\ \text{width}_{\text{transistor}} &= \text{width}_{\text{gate}} \end{aligned}$$

$$k_{\text{pmos-mosfet-lateral-}\perp} =$$

$$\begin{aligned} &\left(\frac{\text{length}_{\text{transistor}}}{(t_{\text{thin-film}} + t_{\text{pmd}} + t_{\text{box}}) \text{width}_{\text{transistor}}} - 1 \right) \left(\frac{2w_{\text{sti}}}{k_{\text{sti}} t_{\text{box}} \text{width}_{\text{transistor}} \{R_{\text{box}}\}} \right) \\ &\quad \left(\frac{k_{\text{sti}} (t_{\text{fox}}) (\text{width}_{\text{transistor}})}{\{2R_{\text{sti,beside-gate}}\}} + \frac{2w_{\text{fox,beside-gate}}}{k_{\text{fox}} (t_{\text{fox}}) (\text{width}_{\text{transistor}})} + \frac{w_{\text{fox,under-gate}}}{\{R_{\text{fox,beside-gate}}\}} + \frac{2d_{\text{via}}}{k_{\text{via}} (l_{\text{via}}) (d_{\text{via}})} \right) \\ &\quad \left(\frac{k_{\text{pmd}} (t_{\text{pmd}} - t_{\text{gate,dielectric}} - t_{\text{poly}}) (\text{width}_{\text{transistor}})}{\{R_{\text{pmd,over-sti,fox-gate}}\}} + \frac{2d_{\text{via}}}{k_{\text{via}} (t_{\text{pmd}} - 5t_{\text{fox}} - t_{\text{poly}}) (d_{\text{via}})} \parallel \frac{l_{\text{gate}}}{k_{\text{poly}} (t_{\text{poly}}) (\text{width}_{\text{transistor}})} \right) \\ &\quad \left(\frac{k_{\text{via}} (t_{\text{pmd}}) (d_{\text{via}})}{\{2R_{\text{sd,electrode,beside-gate}}\}} \right) \end{aligned} \quad (2.85)$$

Simplified:

$$\begin{aligned} R_{\text{pmos-mosfet-lateral-}\perp} &= \frac{1}{t_{\text{box}} + t_{\text{pmd}} + t_{\text{thin,film}}} (k_{\text{box}} t_{\text{box}} + \\ &\quad \left(\frac{1}{\text{width}_{\text{transistor}} \left(\frac{\text{length}_{\text{gate}} - 3d_{\text{via}}}{\text{width}_{\text{transistor}} k_{\text{pmd}} (t_{\text{pmd}} - t_{\text{poly}} - t_{\text{gate,dielectric}})} + \frac{2}{k_{\text{via}} (t_{\text{pmd}})} + \frac{1}{\text{width}_{\text{transistor}} k_{\text{poly}} (t_{\text{poly}})} + \frac{1}{l_{\text{gate}}} \right)} \right. \\ &\quad \left. \frac{1}{k_{\text{sti}} (t_{\text{thin,film}} - t_{\text{Fox}}) + \frac{\text{length}_{\text{transistor}} - 2w_{\text{sti}}}{k_{\text{thin,film}} (t_{\text{thin,film}} - t_{\text{Fox}})} + \frac{2w_{\text{fox,beside-gate}} + w_{\text{fox,under-gate}}}{k_{\text{fox}} t_{\text{fox}}} + \frac{2w_{\text{sti}}}{k_{\text{sti}} (t_{\text{fox}})} + \frac{2w_{\text{width}_{\text{transistor}}}}{k_{\text{via}} (d_{\text{via}})}} \right) \right) \end{aligned} \quad (2.86)$$

$$R_{\text{pmos-mosfet-lateral-}\parallel} = R_{\text{box}} \left| \frac{R_{\text{sti}}}{2} \right| R_{\text{thin,film}} \parallel \frac{R_{\text{fox,beside-gate}}}{2} \parallel R_{\text{fox,under-gate}} \parallel \frac{R_{\text{sd,electrode}}}{2} \parallel R_{\text{pmd,over-sti,fox-gate}} \parallel R_{\text{extraction-gate-electrode}} \parallel R_{\text{poly}} \quad (2.87)$$

$$\text{length}_{\text{transistor}} = (2w_{\text{sti}} + 2w_{\text{fox_beside_gate}} + w_{\text{fox_under_gate}} + 2d_{\text{via}})$$

$$\text{width}_{\text{transistor}} = \text{width}_{\text{gate}}$$

$$k_{\text{pmos_mosfet_lateral_}\parallel} = \frac{\left| \frac{\text{width}_{\text{transistor}}}{(t_{\text{thin_film}} + t_{\text{pmd}} + t_{\text{box}}) \text{length}_{\text{transistor}}} - 1 \right| \left(\frac{\frac{\text{width}_{\text{transistor}}}{k_{\text{box}} t_{\text{box}} \text{length}_{\text{transistor}}}}{\frac{2k_{\text{sti}} (t_{\text{thin_film}} - t_{\text{fox}}) (\text{length}_{\text{transistor}} - 2w_{\text{sti}})}{\{R_{\text{thin_film}}\}}} \right)}{\left| \frac{\frac{\text{width}_{\text{transistor}}}{2k_{\text{fox}} (t_{\text{fox}}) (w_{\text{fox_beside_gate}})}}{\frac{d_{\text{via}}}{\{R_{\text{fox_under_gate}}\}}} \right|} \\ \frac{\left| \frac{\text{width}_{\text{transistor}}}{2k_{\text{fox}} (t_{\text{fox}}) (w_{\text{fox_under_gate}})} \right| \left(\frac{d_{\text{via}}}{\frac{2k_{\text{poly}} (t_{\text{poly}}) l_{\text{gate}}}{\{R_{\text{poly}}\}}} \right)}{\left| \frac{\text{width}_{\text{transistor}}}{k_{\text{pmd}} (t_{\text{pmd}} - t_{\text{gate_dielectric}} - t_{\text{poly}}) (\text{length}_{\text{gate}} - 3d_{\text{via}})} \right|} \frac{\left| \frac{d_{\text{via}}}{\frac{k_{\text{via}} (t_{\text{pmd}} - 0.5t_{\text{fox}} - t_{\text{poly}}) (d_{\text{via}})}{\{R_{\text{extraction_gate_electrode}}\}}} \right|}{\left| \frac{\text{width}_{\text{transistor}}}{k_{\text{poly}} (t_{\text{poly}}) l_{\text{gate}}} \right|}$$

Simplified:

$$k_{\text{pmos_mosfet_lateral_}\parallel} = \frac{(k_{\text{box}} \text{length}_{\text{transistor}} t_{\text{box}} + 2k_{\text{sti}} t_{\text{thin_film}} w_{\text{sti}} + (2w_{\text{fox_beside_gate}} + w_{\text{fox_under_gate}}) k_{\text{fox}} (t_{\text{fox}}) + (l_{\text{gate}} + \text{length}_{\text{gate}}) k_{\text{poly}} (t_{\text{poly}}) + \text{width}_{\text{transistor}} (2k_{\text{via}} (l_{\text{via}}) + k_{\text{via}} (-0.5t_{\text{fox}} + t_{\text{pmd}} - t_{\text{poly}})) + (\text{length}_{\text{transistor}} - 2w_{\text{sti}}) k_{\text{thin_film}} (\text{length}_{\text{transistor}} - t_{\text{fox}})) / (\text{length}_{\text{transistor}} (t_{\text{box}} + t_{\text{pmd}} + t_{\text{thin_film}}))}{(l_{\text{gate}} + \text{length}_{\text{gate}}) k_{\text{poly}} (t_{\text{poly}}) + (\text{length}_{\text{transistor}} - 2w_{\text{sti}}) k_{\text{thin_film}} (\text{length}_{\text{transistor}} - t_{\text{fox}})) / (\text{length}_{\text{transistor}} (t_{\text{box}} + t_{\text{pmd}} + t_{\text{thin_film}}))}$$

2.5.6 Package Modeling

The chip package is an important avenue for thermal optimization. Anywhere from 60 to 95 per cent of the thermal energy may be transferred through the chip package. It is therefore critical that any thermal modeling infrastructure include a thorough investigation of the avenues of thermal optimization offered by the chip package design. The general heat flow path can be seen in figure 2.43.

Successful thermal interconnect layout for both the package uPCB and substrate has several factors. These factors are governed by the thermal behavior of the interconnect layers themselves. To exploit the thermal behavior of the system as a whole, a detailed understanding of the underlying heat transfer mechanisms must be understood.

The thermal conductivity of copper is 1000 times that of most polymers (BT, FR-4 and epoxy) that make up most package and main-board interlayer dielectric layers. This means that the primary heat flow path through the interconnect layer stack of either the package or main-board PCB is through the wiring traces. Further, this means that the chosen layout of the traces and the geometry of the traces themselves may have a significant impact upon the thermal performance of the interconnect layer stack.

Thermal resistance is analogous to the resistance of a fluid flowing through a pipe. In the case of a pipe, when there is a severe restriction in one region of the pipe, flow is limited through the rest of the pipe, even if the rest of the pipe has little or no

restriction at all. Similarly, the heat flow laterally across a metal interconnect layer will decrease dramatically if there is a thermal “bottleneck” in one region of the layer where few metal interconnect traces exist to pass heat from one end of the layer to the other. Further, if there is a region of the layer with few vias to pass heat to the layers above and below, this will severely impact the thermal performance of the interconnect stack as a whole. In summary, the region of highest thermal resistance will determine the overall heat flow rate. This can be seen in figure 2.42.

Given these heat flow properties, there are several design guidelines which should be observed. First, copper traces widths should be maximized and trace-to-trace spacing should be minimized. This will decrease the thermal resistance of each metal trace and reduce the amount of dielectric insulation between traces. Thus, this will reduce the “bottleneck” phenomenon whereby interconnect density is reduced sufficiently to negatively impact the thermal flow of the system as a whole. Second, vias should be evenly distributed throughout the metal layer. Vias should be added even if they are not needed from an interconnect objective. These, called “thermal vias”, are explicitly designed to pass heat to the layers above and below. This will ensure that no vertical “bottleneck” is generated. Third, the number and area of copper power planes should be maximized. This would add to thermal spreading. Fourth, the proximity of heat-generating wires should be minimized to spread the active wiring regions to prevent thermal buildup in one region of the chip.

To evaluate the thermal performance of a given device, the historical thermal standard for device thermal characteristics is determined by the Standard-Joint

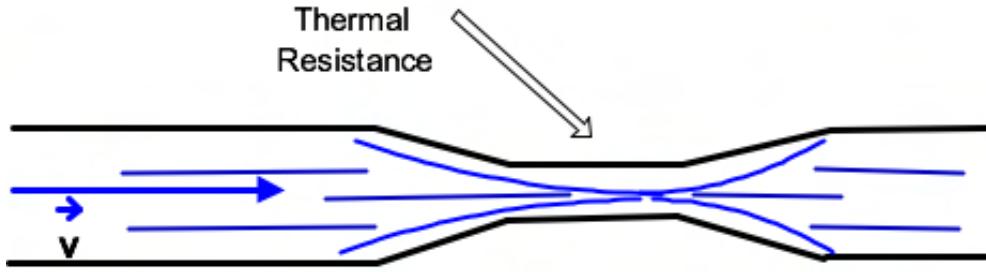


Figure 2.42: Thermal “bottleneck” in a series-connected thermal system restricts the overall heat flow

Electronic Engineering Council (JEDEC) standard [56]. Thermal resistance of the component as defined by JEDEC can be seen in equation (2.90). However, this definition has many inaccuracies. In particular θ_{ja} is not constant [56]. This thermal resistance is a function of the package design and ambient conditions which can change wildly, leading to erroneous results.

$$\theta_{ja} = \frac{T_{junction} - T_{ambient}}{\text{Power}} \quad (2.90)$$

As can be seen in figure 2.44, the heat flow path through the main-board is further dependent upon various factors including the density of thermal vias under the thermal landing pad of the package. Similar to the heat flow through the interconnect layers depicted by figure [interconnect figure], the vertical heat transfer path is a series resistance of the total heat flow path through the main-board layer stack.

For each wiring layer, a lumped resistance is computed for the lateral and vertical thermal resistance. Similar to the package interconnect layers, the vertical heat transfer is a parallel resistance between the interlayer epoxy insulation and the

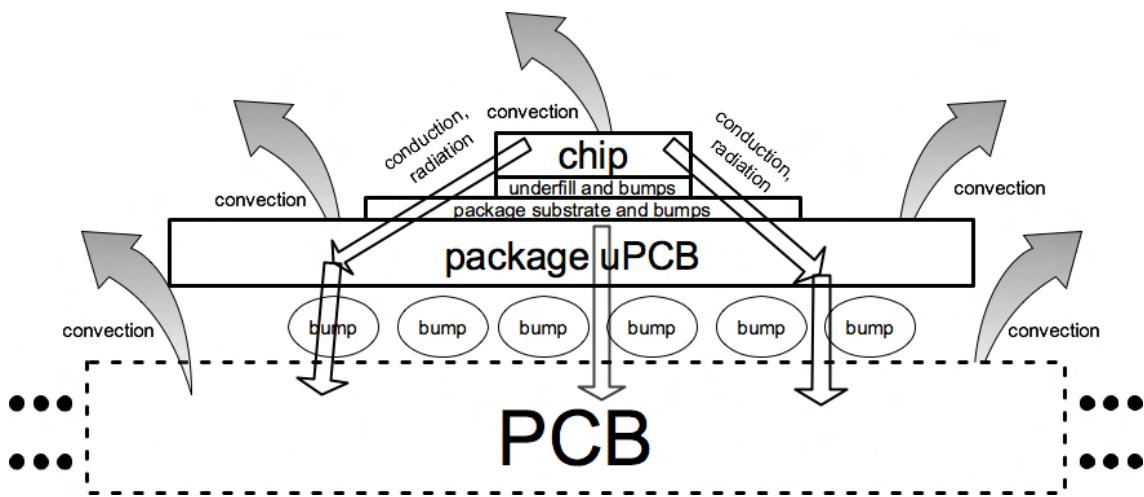


Figure 2.43: General Heat Flow Path Through Chip, Package, and Main-board

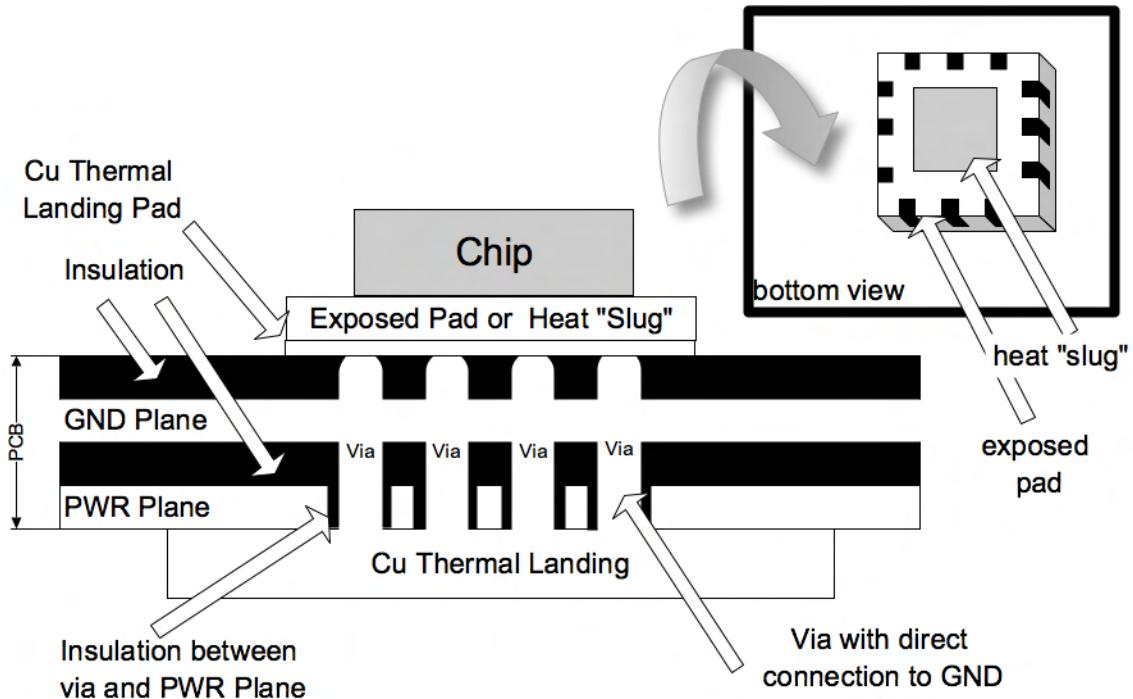


Figure 2.44: Side-view and Bottom View of Heat Flow Path Through Package and Main-board

copper vias. However the vias are modeled differently in this case. Unlike the chip and package vias, which assume that the via metal plating is the same as the radius of the via, the main-board vias have a plating thickness which can vary depending upon the manufacturing process. Thus, the vertical resistance of the main-board via is directly proportional to the via length and inversely proportional to the cross-sectional area of the copper plating. The thermal resistance of a single via is governed by equation (2.23).

See figure 2.14 for the geometry of the via modeled.

The package model is hence a very similar structure to the main-board structure described elsewhere. Sesctherm relies largely upon the flip chip plastic ball grid array material layer stack described by Ramakrishna et al. [94]. Four regions of the package are described. First, is the region modeling the C4 solder balls and chip underfill that reside under the chip die. Second, is the region modeling the package substrate which is placed under the solder ball region of the package. Third, is the region modeling a C5 layer that simulates the thermal properties of the C5 solder balls. Lastly, is a region modeling the package printed wiring board.

The layer stacks used in Sesctherm are described in tables 2.4 and 2.5. The first table describes the cross-section of the package substrate. The second table describes the cross-section of the package printed wiring board.

While the Sesctherm modeling infrastructure is flexible and can accommodate a variety of different package geometries, Sesctherm currently only models a flip chip plastic ball grid array package (FC-PBGA). Further, Sesctherm currently only models a 1s2p JEDEC type package printed wiring board (PWB). Such a printed wiring board

has one signal layer and two power plane layers. In addition, Sesctherm currently only models a 6-metal layer package substrate.

The dimensions of both the PWB and substrate are currently scaled linearly with the total vertical dimension of the chip package specified. Further development of this model should rely upon the same statistical interconnect model used for the chip interconnect layers. Using the statistical analysis model, the number of layers should be automatically computed given constraints on package wiring resources. This is future work.

2.5.7 Forced Air Convective Cooling Model

The forced convection model precisely follows the equations previously described. Although Sesctherm is flexible and can be expanded to handle a variety of flow conditions, a full fluid dynamics model was eschewed towards the use of closed-form expressions. This was done to reduce the runtime penalties associated with incorporating fluid dynamics into the thermal infrastructure.

In its current form, Sesctherm is designed to model mixed flow conditions for air directed parallel to a given materials layer. In this way, we are able to simplify the convection flow to reliably allow for the characterization of parallel flow over a flat plate as was previously described. The coolant material, coolant flow rate, distance of the coolant fluid inlet, and atmospheric pressure conditions are configurable. This allows the model to handle a variety of cooling conditions.

Although this cooling model was satisfactory for the purpose of verifying the

Layer	Name	Material(s)	Thickness(um)
1	Solder Mask Layer	Cu/Solder	22
2	Metal Layer 1	Cu/Bismaleimide-triazine laminate	17
3	BT Layer 1	Cu/Bismaleimide-triazine laminate	33
4	Metal Layer 2	Cu/Bismaleimide-triazine laminate	17
5	BT Layer 2	Cu/Bismaleimide-triazine laminate	33
6	Metal Layer 3	Cu/Bismaleimide-triazine laminate	27
7	BT Core Layer	Cu/Bismaleimide-triazine laminate	800
8	Metal Layer 4	Cu/Bismaleimide-triazine laminate	27
9	BT Layer 3	Cu/Bismaleimide-triazine laminate	33
10	Metal Layer 5	Cu/Bismaleimide-triazine laminate	17
11	BT Layer 4	Cu/Bismaleimide-triazine laminate	33
12	Metal Layer 6	Cu/Bismaleimide-triazine laminate	17
13	Solder Mask Layer	Cu/Solder	22
14	C5 Layer	Cu/Air Gap	460

Table 2.4: Cross-section of Flip-Chip Plastic Ball Grid Array Substrate

Layer	Name	Material(s)	Thickness(um)
1	Solder Mask Layer	Cu/Solder	36
2	Metal Layer	Cu/Bismaleimide-triazine laminate	36
3	FR4 Layer	Cu/Bismaleimide-triazine laminate	392
4	Metal Plane Layer	Cu	36
5	FR4 Core Layer	Cu/Bismaleimide-triazine laminate	613
6	Metal Plane Layer	Cu	36
7	FR4 Layer	Cu/Bismaleimide-triazine laminate	392
8	Solder Mask Layer	Cu/Solder	33

Table 2.5: Cross-section of Flip-Chip Plastic Ball Grid Array Printed Wiring Board

model in this study, clearly further development of this model is necessary to handle other cooling setups. The incorporation of these additional cooling setups is considered future work.

2.5.8 Temperature Dependent Material Modeling

Sesetherm is able to accurately characterize many temperature dependent material parameters at runtime. This was found to be an extremely important component to accurately characterize the thermal response of the system. In its current form, Sesetherm recomputes the thermal conductivity of many of its materials at runtime.

The specific equations used to compute the temperature-dependent conductivity can be found in table B.2. These equations were generated from temperature-dependent empirical data collected from various sources [55, 54]. Using a non-linear regression, an equation was created relating the temperature to thermal conductivity and specific heat of each material. The R^2 value was higher than .99 in each case.

Of particular interest to the analysis of the temperature dependence on the thermal capacitance was specifically the temperature dependence on the thermal capacitance of silicon thin film. As can be see in figures 2.45 and 2.46, the capacitance of silicon thin film versus that of bulk silicon is related by the atomic thickness of the silicon layer and the temperature.

It was found that any discrepancy between the thermal capacitance of silicon thin film versus that of bulk silicon can largely be neglected for any film thickness greater than 10nm. However, at less than 2nm the thermal heat capacitance is more

highly a function of temperature as can be seen in figure 2.46. Although this is not especially alarming, this is one example of the fact that care should be taken to address new thermal phenomena as we further improve manufacturing processes.

The re-computation of these material parameters is a linear function of the number of temperature nodes. As such, this can be a costly operation. Since a temperature change may be infrequent, the model allows this computation to be scheduled at regular intervals.

There are several areas of future work in this model. First, despite the fact that model equations have been generated to model the temperature dependance on the specific heat of each material, these equations are not currently integrated into the infrastructure. Second, the re-computation of material parameters is currently scheduled to occur at regular intervals. However, certain materials have material parameters that are more sensitive to temperature fluctuation than others. The re-computation of these material parameters should therefore be based upon the specific temperature fluctuation in a region of the model that uses each material. The integration of these improvements is considered future work.

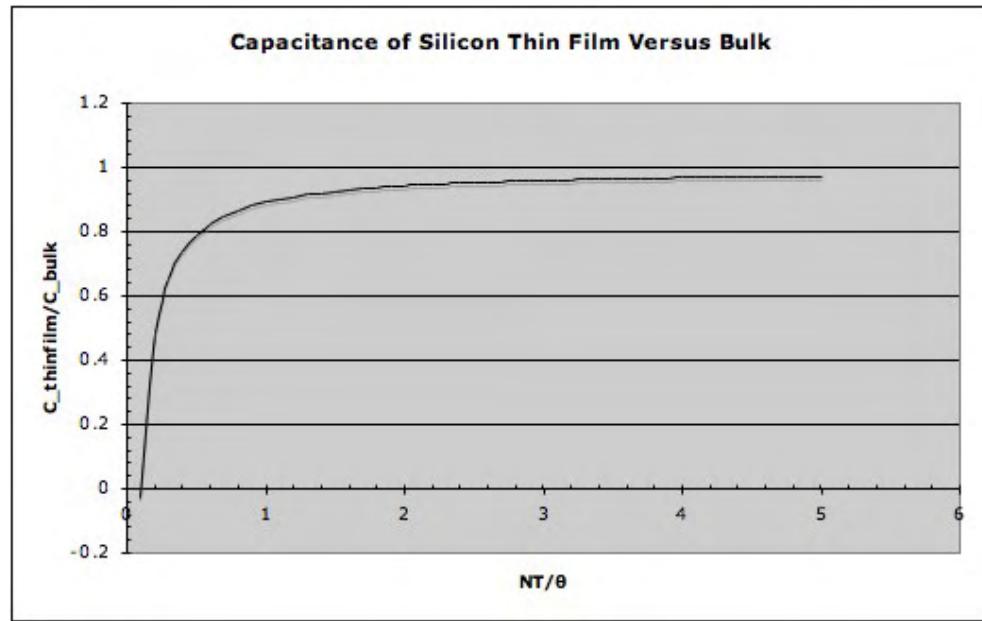


Figure 2.45: Silicon Thin-Film Heat Capacitance Versus Bulk Silicon Related to NT/θ , where N is the atomic thickness of the layer ($\text{thickness}/\frac{54\text{nm}}{\text{Si Atom}}$), T is the temperature of the layer (K), and θ is the Debye temperature (645K for Si)[93]

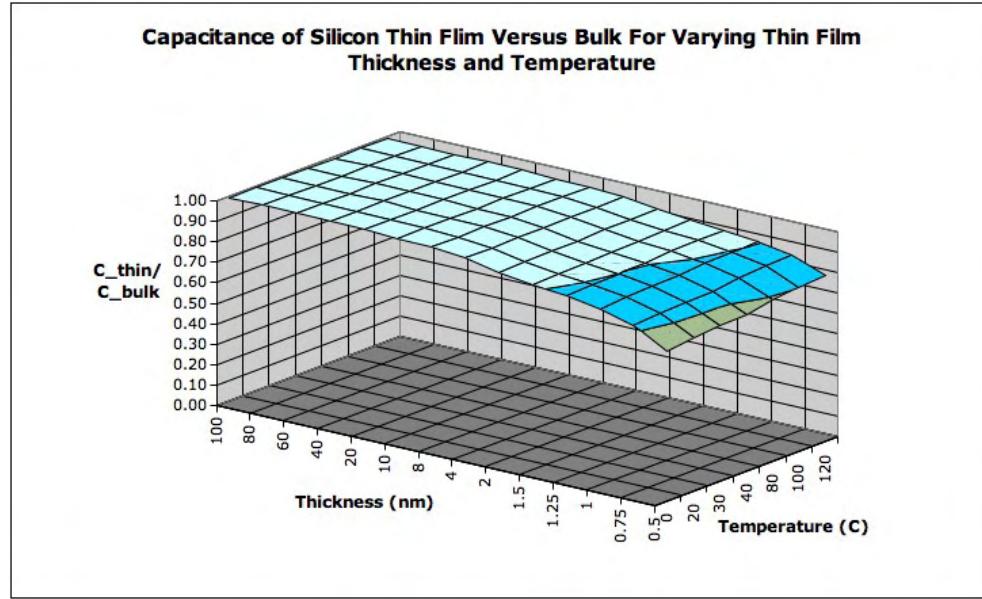


Figure 2.46: Silicon Thin-Film Heat Capacitance Versus Bulk Silicon as a function of thin-film layer thickness (nm) and temperature (deg C)[93]

Part II

Model Verification

2.6 Introduction

Sesctherm is verified against both a Delphi thermal test die and Flomerics FlothermTM thermal modeling infrastructure. The Delphi thermal test die is used for the purpose of comparing the thermal response of the Sesctherm thermal model to actual empirical thermal data. The Dephi thermal test die used is a standard in the industry, and it provides an accurate means for validating the accuracy of the thermal response Sesctherm predicts. Further, Sesctherm is validated by modeling the same thermal system using the Flomerics FlothermTM thermal modeling software. FlothermTM was chosen as it has become an industry standard for reliable thermal characterization. Further, FlothermTM has separately been validated against empirical data taken from a variety of sources.

Chapter 3

Validation Against Delphi Thermal Test Chip

3.1 Introduction

The Delphi PST2-03/8DX Thermal Test Die is explicitly designed to determine thermal characteristics of a given chip package configuration. This includes the JEDEC θ_{jc} or θ_{ja} metrics. The test chip includes both a heating element and temperature monitoring circuit.

The thermal heater is implemented using a simple resistive heater. The heater is activated by driving a current through a doped silicon well between two interconnect bars. The heater is designed to heat the chip uniformly and produce a reliable source of heat.

The temperature monitor is implemented using a temperature monitoring cir-

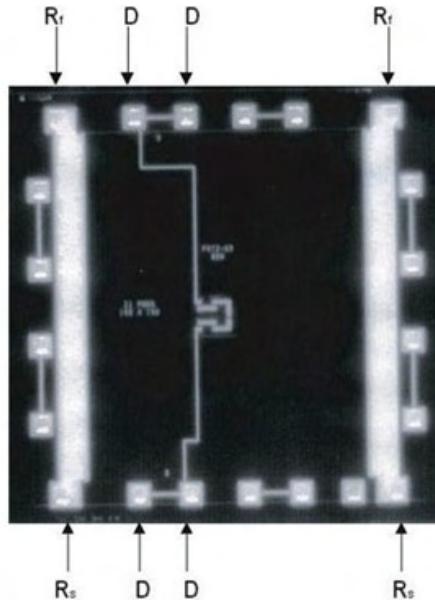


Figure 3.1: Delphi PST2-03-8DX Thermal Test Die

cuit with five diodes connected in series. This can be seen in figure 3.1. The diodes are reverse biased with a constant current source to 3.5VDC. The circuit is designed so that every 10mv voltage drop is equivalent to 1 degree Kelvin.

The chip is fabricated using a 130nm bulk CMOS process. P-type silicon substrate is used. The doping characteristics are expected to be similar to those of other similar processes by various IC fabrication facilities. Aluminum metal interconnect is used with standard SiO_2 isolation. Metal interconnect density is maximized around the bus bars on the edge of the chip and in the center. Transistor density is maximized in the center of the chip where the five-diode temperature monitoring circuit is located. These parameters can be seen in table 3.1.

There is no chip package for this chip. The flip-chip micro-BGA is soldered

directly to the main-board PCB. This makes temperature modeling significantly simpler as there is no package resistance between the test chip and the main-board. The material layer stack used is shown in table 3.3.

Wafer Size (mm ²)	125
Die Thickness (um)	635
Metal Thickness (nm)	2.4
Metal Composition	98Al/1Cu/1Si
Passivation thickness	SiN
Silicon Substrate Type	P-type

Table 3.1: Thermal Test Chip Technology Parameters

3.2 Setup

The setup of the Delphi thermal test chip can be seen in figure 3.3. As can be seen in this figure, five diodes (D1-D5) are reverse biased using a constant current source. The series diodes are reserve biased to 3.5V per the Delphi specifications.

As the temperature of the device increases, the voltage across the diodes will drop due to changes in carrier mobility. The test chip is calibrated for a temperature response of 10mV/deg K. Given the drift in voltage for steady-state measurement, it can be expected that the test chip exhibits an error in the order of 1 deg C.

As can be seen in figure 3.3, a constant voltage is applied to the resistive heater embedded within the silicon substrate. Since the resistance of the heater will change as a function of temperature, current is measured over time. 25 volts is applied over the resistive heater with current of roughly 100mA. This means that approximately 2.5W

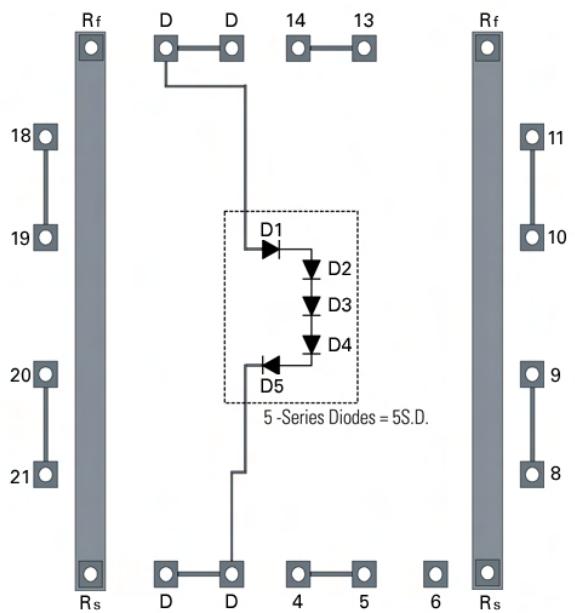


Figure 3.2: Delphi PST2-03-8DX Thermal Test Die

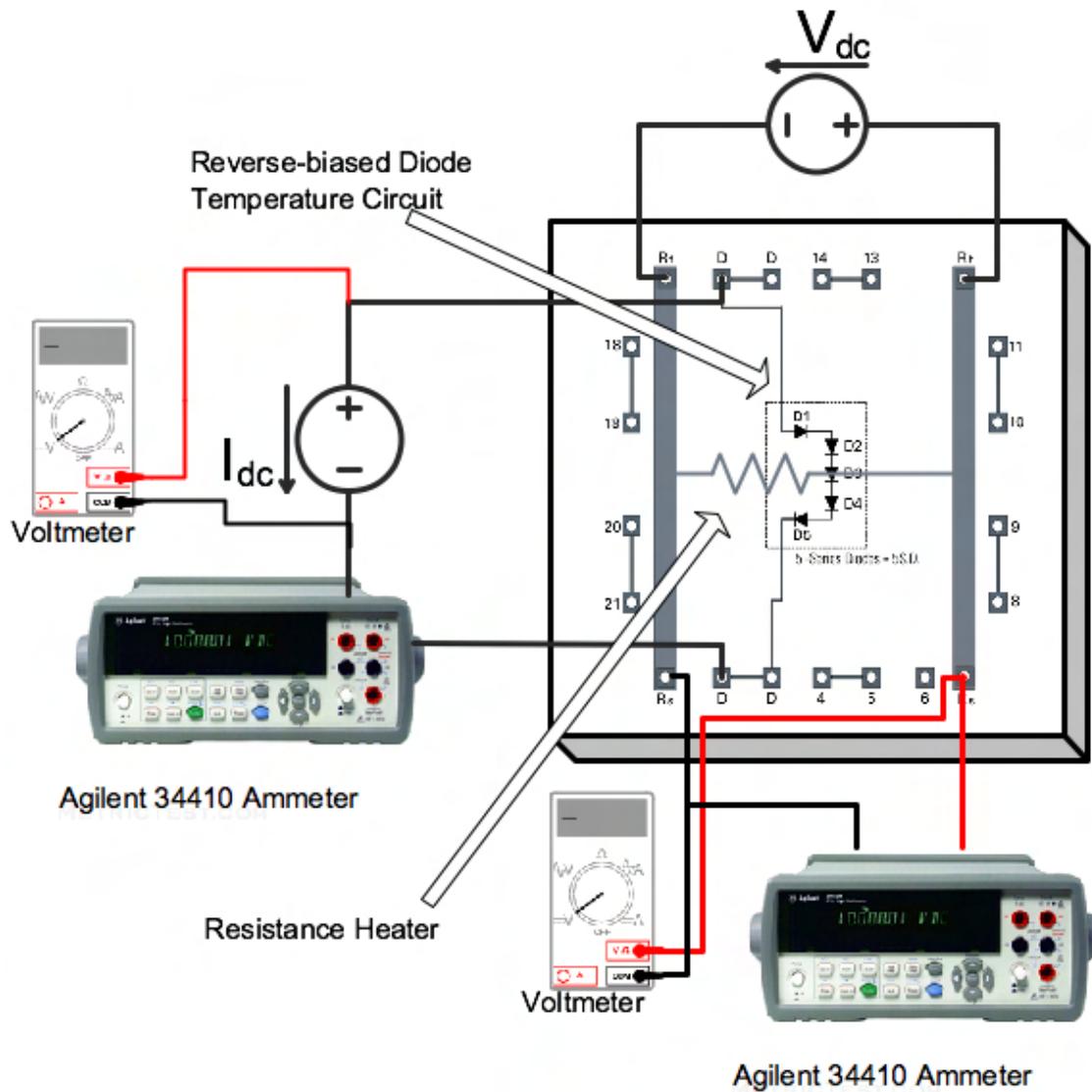


Figure 3.3: Delphi Test Chip Setup

of power is applied to the heater.

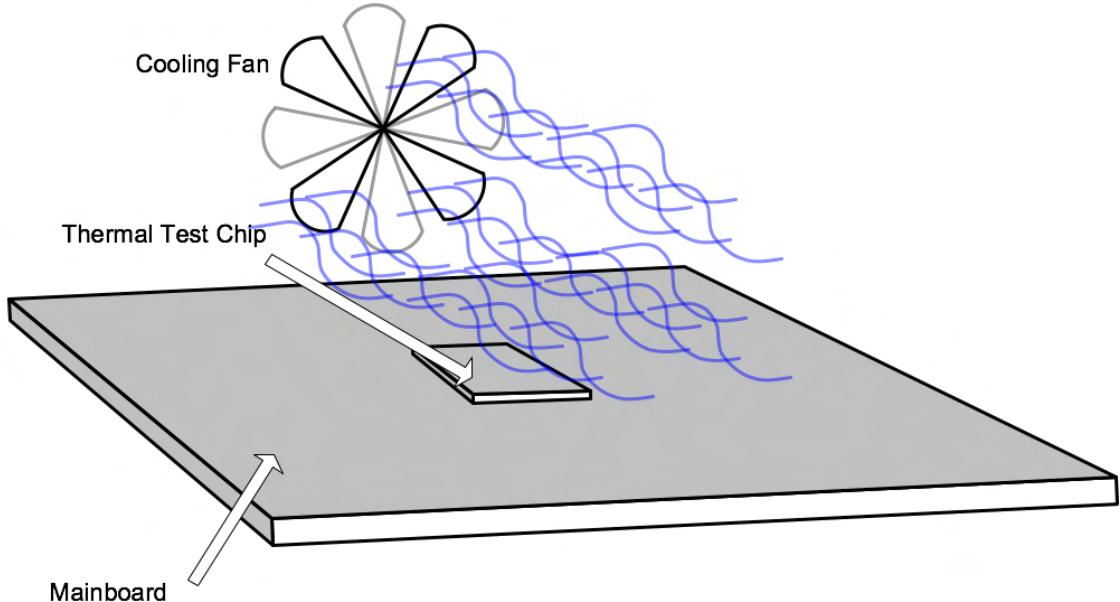


Figure 3.4: Delphi Test Chip Setup Convection Cooling

The constant voltage source applies a square wave of amplitude 25V. As the temperature changes, the voltage across the diodes is measured along with the current through the resistive heater. The temperature is plotted over time.

The cooling setup is very simple for this design. Convection cooling was performed using a standard fan with estimated air speed between $2 \frac{m}{s}$ and $8 \frac{m}{s}$. The thermal test chip placed on a printed circuit board with no other power generation. The ambient air temperature in the room was measured at 21 degrees Celsius. The fan was oriented such that the air passed along the width of the chip. This can be seen in figure 3.4. The parameters used for Sesctherm can be found in table 3.2.

Modeling Parameter	Setting	Justification
Ambient Temperature	21 deg C	Room temperature measured
Forced Convection Flow Rate	2-8 (m/s)	Average Fan Speed
Convection Fluid	Air @ 1atm	Air
Fluid Temperature	21 deg C	same as ambient

Table 3.2: Delphi Test Chip Convection Cooling Setup

Material Layer	Width (m)	Height (m)	Thickness (m)
Air	0.00381	0.00381	model determined
Silicon Substrate	0.00381	0.00381	0.0006
Interconnect	0.00381	0.00381	0.0001
Main-board	0.01	0.01	0.005

Table 3.3: Sesctherm Material Layer Setup For Delphi Test Chip

Using the technology parameters in table 3.1, Delphi-provided chip dimensions, and convection cooling data from table 3.2, a virtual materials layer stack was synthesized. This included a bottom layer for the PCB main-board, where the temperature was held constant at room temperature. An interconnect layer and silicon substrate layer were synthesized based upon Delphi data. Convection cooling across the chip of the chip was synthesized using cooling parameters in table 3.2.

The dimensions of the test chip were taken from the Delphi specifications. However, it is difficult to evaluate where the heater was placed within the silicon substrate. To solve this problem, it is assumed that the heat is dispersed equally over the central region of the chip. The outside regions of the chip are deemed to have high interconnect density, while the inner region of the chip has low interconnect density. The floor-plan used for this analysis was found in table 3.4.

Floor-plan Unit Name	Width (m)	Height (m)	Left X (m)	Bottom Y (m)
Bottom_left	0.000423333	0.000423333	0.00000000000	0.00000000000
Bottom_center	0.002963333	0.000423333	0.000423333	0.00000000000
Bottom_right	0.000423333	0.000423333	0.0033866667	0.00000000000
Center_left	0.000423333	0.002963333	0.00000000000	0.000423333
Center_center	0.002963333	0.002963333	0.000423333	0.000423333
Center_right	0.000423333	0.002963333	0.0033866667	0.000423333
Top_left	0.000423333	0.000423333	0.00000000000	0.0033866667
Top_center	0.002963333	0.000423333	0.000423333	0.0033866667
Top_right	0.000423333	0.000423333	0.0033866667	0.0033866667

Table 3.4: Delphi Test Chip Floor-plan Layout

3.3 Results

A visualization, in perspective, of the thermal distribution across the chip can be found in figure 3.5. As can be seen, the region of the chip that is nearest to the convection air source (the fan) is coolest. As the air passes across the surface of the device, it is heated. Since the convection cooling rate between the chip and forced air flow in this case is a linear function of the temperature difference between the air flow and the surface of the device, the cooling efficiency is reduced as air passes across the chip. It can further be seen that the difference in interconnect density between the central region (where the resistive heat exists) and the outer regions (where interconnect and pads exist) does not appear to have a significant impact upon the thermal profile of the chip.

The results of the thermal evaluation can be found in figure 3.6. As can be seen, Sesetherm tracks the thermal behavior of the test chip well. However, clearly there remains room for improvement.

In particular, it can be seen that while the steady-state behavior of the model can be highly accurate, wild fluctuations in temperature can result in significant error should even very small errors in the transient behavior of the model exist. In particular, the steady-state accuracy of Sesctherm is excellent (± 0.01 degrees C), however the modest differences in transient response can cause significant thermal variation. This can be seen in figure 3.6 at .5s. The deviation between Sesctherm and the test chip approaches 7 Celsius. Averaged out across the entire run, this could be a minor error. However, a dynamic thermal system with wild fluctuation in temperature can cause problems. An investigation into the source of this inaccuracy is left for future work. However, upon further investigation, the observed error may, in fact, be indicative of a more serious problem.

There are several important observations that can be made here. One must remember that nearly all system-level electro-thermal models, including Sesctherm, are based upon the inherent assumption that any thermal system can be accurately modeled as the sum of discrete, linear circuit devices. In particular, Sesctherm assumes that all conduction heat flow can be modeled as a complex resistive-capacitive (RC) network. Although radiation and convection does not easily follow the RC-mechanism, heat flow is dominated by a conduction heat transfer mechanism for semiconductor thermal characterization.

In the case of the test chip, a single current source is used, and heat flow is dominated by a conduction heat transfer mechanism. Using the rule of thevenin/norton equivalence, any electro-thermal circuit of this type should be able to be approximated

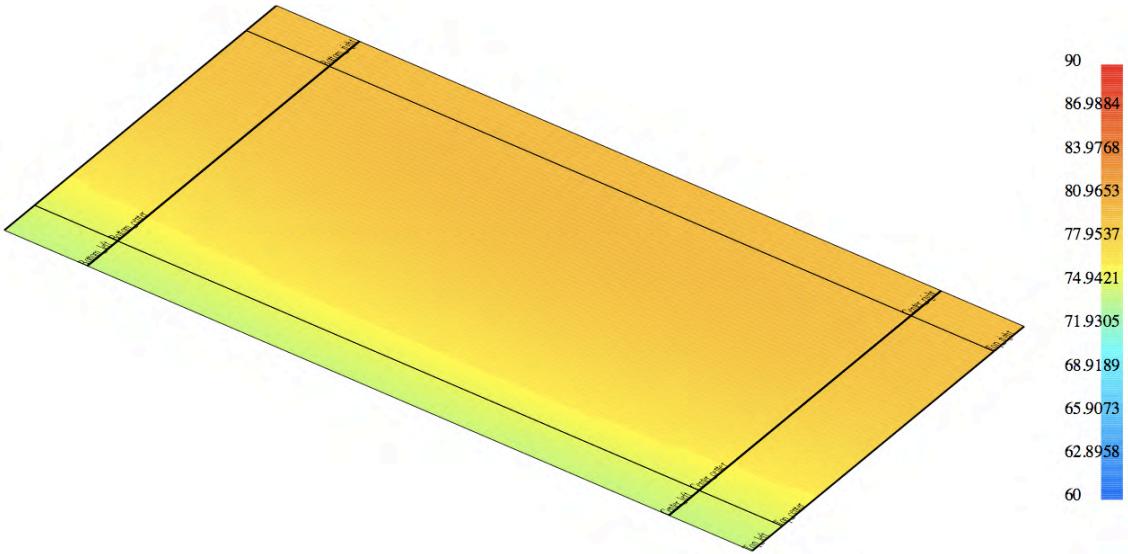


Figure 3.5: Sesctherm Test-chip Graphics Visualization

as a simplified equivalence with single RC-time constant. Therefore, the thermal trace obtained from the test chip should follow the transient behavior of such a circuit to a large degree. However, upon an investigation using a non-linear regression, the trace data deviates from the theoretical equation by more than 5% overall, while the absolute difference in temperature is significantly higher at various times. In fact, this is similar in accuracy to what was obtained using Sesctherm.

A thorough analysis of this phenomenon is beyond the scope of this study. However a realistic evaluation of this thermal behavior could be performed using Fourier transform of the test chip thermal trace, once thermal noise has been removed. If the thermal system can be characterized accurately using the RC mechanism described, higher-order frequency behavior should not be present in any significant way. Indirectly,

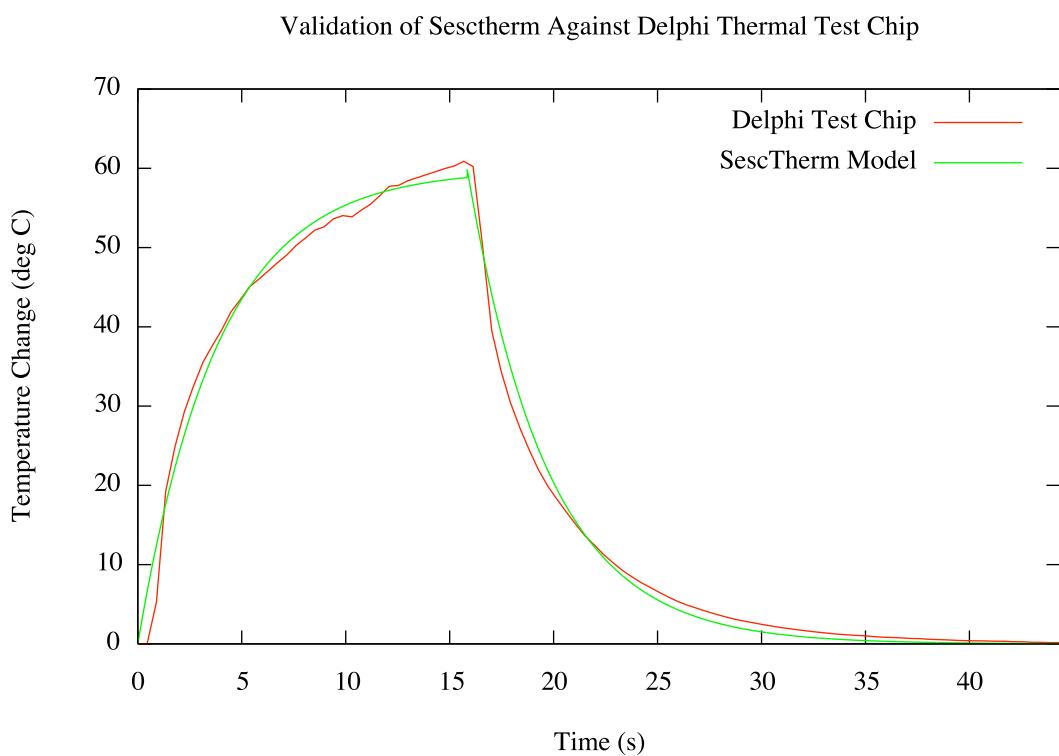


Figure 3.6: Comparison of Thermal Model to Test Chip

we have suggested here that despite the fact that the thermal heat transfer in the test chip is dominated by conduction, there is a high likelihood that significant higher-order frequency terms exist – ones that cannot be captured using the RC methodology used. This analysis is left to future work.

Chapter 4

Validation Against Flomerics

FlothermTM Temperature Modeling

Framework

4.1 Introduction

To provide a more robust validation of the Sesctherm thermal modeling infrastructure, Sesctherm was further validated against FlothermTM from Flomerics. FlothermTM is a powerful thermal modeling infrastructure that is widely used by industry. FlothermTM has been extensively validated against both other software tools and empirical data [129, 90, 98, 99, 110, 65]. FlothermTM is considered an industry standard for the accurate thermal modeling of integrated circuit devices.

In addition to FlothermTM FlopackTM was also used in this validation. FlopackTM is designed to automatically synthesize thermal sub-models for a variety of Integrated

Circuit components. For the purpose of this validation, FlopackTM was used to synthesize a reliable representation of the Advanced Micro Devices AMA3200BEX5AR “Clawhammer” 754 microprocessor. A flip-chip pin-grid-array-based package was further synthesized.

4.2 Setup

In order to provide a reliable like-kind comparison between the data from each of the models, the same material dimensions were input into each model. Further, the chip floor-plan used was the same in both models. The material and floor-plan dimensions can be seen in figure 4.2.

One problem with comparing both models was that FlothermTM uses a different strategy for the characterization of a given IC device. In order to handle the variation, the Sesetherm model configuration had to be modified to compensate. The differences include the fact that FlothermTM uses a slightly different means for synthesizing lumped material parameters and that FlothermTM uses a convection cooling model that is a full fluid dynamics model.

Rather than modeling a fine-grained variation in the material models throughout the chip and package as seen in figures 2.13 and 2.12, FlothermTM is configured by default to model large blocks with equivalent thermal properties. To provide as close an approximation as possible for this modeling methodology, Sesetherm is configured with fewer lumped material layers. In particular, a single material layer is used for the

Model Unit	X(m)	Y(m)	Z(m)	X Size(m)	Y Size(m)	Z Size(m)
Package	0	0	0	0.04	0.04	0.00483
Die	-0.005675	-0.0085	0.00214	0.01135	0.0170464	0.00083
b1_heater	0	0.000385472	0	0.00162755	0.00749528	0.00083
b2_heater	0	0	0	0.00235566	0.00038547	0.00083
b3_heater	0.00162755	0.00488264	0	0.00274113	0.00299811	0.00083
b4_heater	0.00162755	0.00445434	0	0.00274113	0.0004283	0.00083
b5_heater	0.00162755	0.0041117	0	0.00518245	0.00034264	0.00083
b6_heater	0.00162755	0.000385472	0	0.000728113	0.00372623	0.00083
b7_heater	0.00235566	0	0	0.00325509	0.0041117	0.00083
b8_heater	0.00561076	0.00197019	0	0.00119924	0.00214151	0.00083
b9_heater	0.00561076	0.000685283	0	0.00119924	0.00128491	0.00083
b10_heater	0.00561076	0	0	0.00119924	0.00068528	0.00083
b11_heater	0.00436868	0.00445434	0	0.00124208	0.00145623	0.00083
b12_heater	0.00561076	0.00445434	0	0.00119924	0.00145623	0.00083
b13_heater	0.00436868	0.00591057	0	0.00244132	0.00197019	0.00083
b14_heater	0.00681	0	0	0.000256981	0.00788075	0.00083
b15_heater	0.00706698	0.00445434	0	0.00256981	0.00342642	0.00083
b16_heater	0.00706698	0.0041117	0	0.00428302	0.00034264	0.00083
b17_heater	0.00706698	0.00197019	0	0.00102793	0.00214151	0.00083
b18_heater	0.00809491	0.00197019	0	0.00154189	0.00214151	0.00083
b19_heater	0.00706698	0	0	0.00256981	0.00197019	0.00083
b20_heater	0.00963679	0.00321226	0	0.00171321	0.00089943	0.00083
b21_heater	0.00963679	0.00149906	0	0.00171321	0.00171321	0.00083
b22_heater	0.00963679	0	0	0.00171321	0.00149906	0.00083
b23_heater	0.00963679	0.00445434	0	0.00171321	0.00342642	0.00083
b24_heater	0	0.00788075	0	0.01135	0.00916566	0.00083

Table 4.1: FlothermTM Simulation Chip Geometry and Heater Sources

package. The configured layer stack can be seen in table 4.2.

Fluid/Thermal Settings	Modeled Behavior	Fluid Flow, Heat Transfer
	Number of Dimensions	3-Dimensional Modeling
	Transient or Steady-State	Transient Conditions
	Laminar/Turbulent	Laminar Model Used
Convection Settings	Fluid Type	Air at 20 Deg C
	Fan Velocity	10 (m/s)
	Datum Pressure	1 ATM
	External Temperature	20 Deg C
	Total Model Cells	2520
	Time Steps	1001
Model Performance	Simulation Time	2 Hours, 27 Mins, 6 Sec
	Initial Conditions	0W
	Toggle Rate	.25 Sec
Transient Power	Dynamic Power/Unit	100 mW

Table 4.2: Flotherm™ Simulation Setup Parameters

Layer Number	Layer Type
0	Air Layer
1	Package
2	Silicon Substrate
3	Air Layer

Table 4.3: Sesctherm Material Layer Stack Used for Flotherm™ Validation

Sesctherm does not have a full fluid-dynamics model to model coolant flow. To compensate for this variation, both Flotherm™ and Sesctherm are configured to model only laminar flow. The rate of fluid flow is set to be equivalent in both simulations. The detailed set of coolant parameters for Flotherm™ in the simulation can be found in table 4.2.

In the thermal simulation a simple matrix-multiply-based power profile is assumed. In particular, every one of the 23 floor-plan units is power cycled every .25s, with all the units initially off. While each unit is activated, it is considered to use 100mW of dynamic power. While each unit is deactivated, it is considered to use no power.

Clearly such assumptions are not realistic given the ever increasing static power utilization in modern IC designs. However, such details are not relevant for the purpose of validation. This is true for several reasons. First, all of the temperature traces shown here represent the average temperature fluctuation over the entire chip. Therefore, any intra-die fluctuations will not be visible anyway. Second, complicating the input power trace only serves to complicate the temperature output trace, making visualization of the temperature fluctuations more difficult.

4.3 Results

As can be seen in figure 4.1, the data obtained by both models follow quite well. In particular, the average error is less than 0.1 deg C over the 10s run. The maximum error occurs during the initial stage of warmup, where the error is still less than 1 deg C as can be seen in figure 4.3. The error further appears to be related to a slight time shift between the two temperature traces, as can be see in figure 4.2.

Rather than plotting the temperature changes for each functional unit separately, the variation in the average temperature across the entire chip was chosen. This

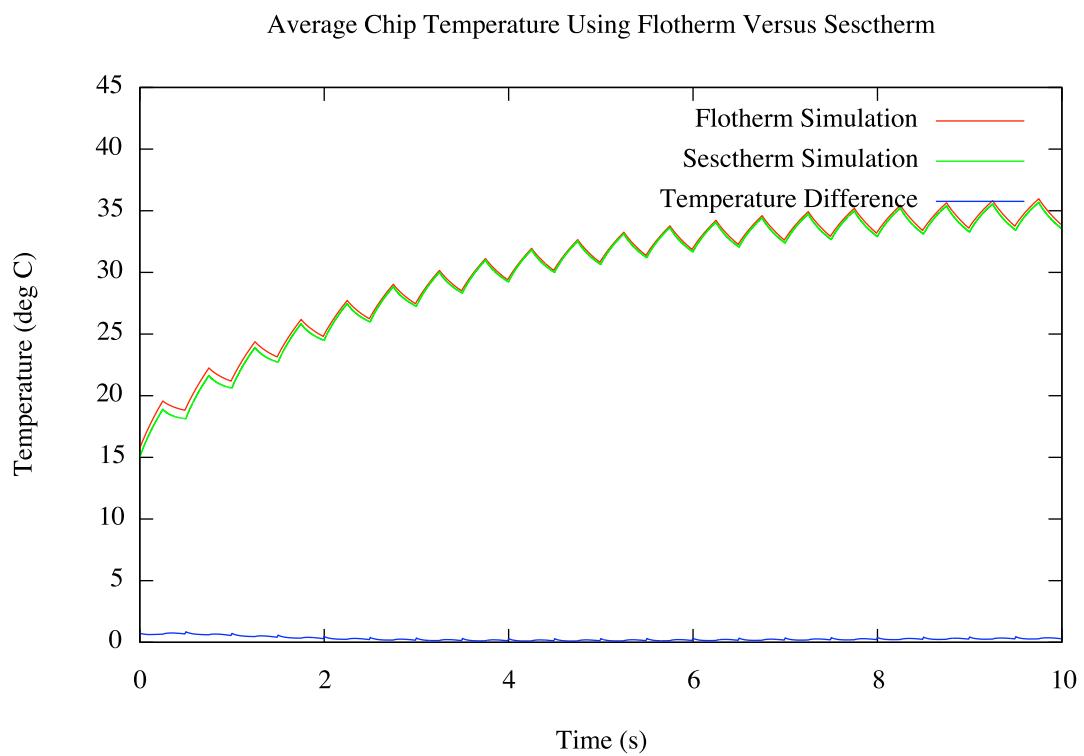


Figure 4.1: Thermal Model Verification Against FlothermTM Thermal Simulation Infrastructure

was done so as to neatly show the variation. However, further simulations are necessary to evaluate the accuracy of the intra-die temperature variation. Such a further validation is necessary to provide assurance that model predictions with regard to points of high heat also known as “hotspots” are accurately reproduced in Sesctherm. This is considered future work.

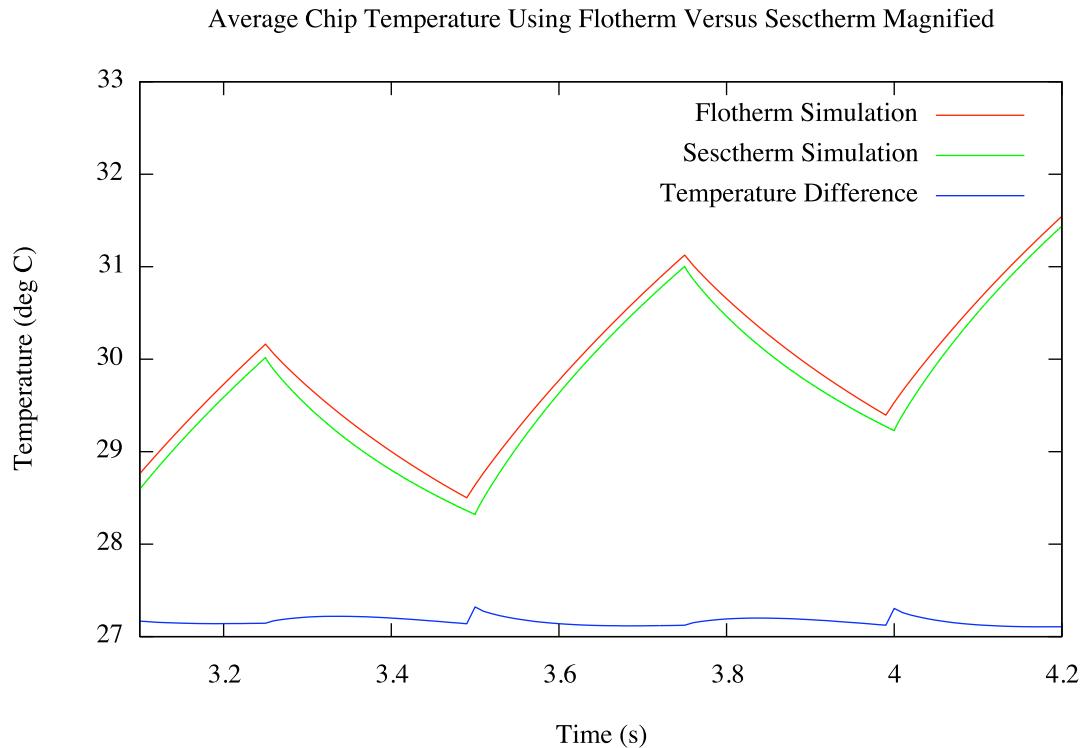


Figure 4.2: Thermal Model Verification Against FlothermTM With Focus on Existing Deviation Between Models

There are clearly still some areas of improvement in Sesctherm. The Sesctherm trace is approximately .1 deg C lower than that of FlothermTM. This can be seen in figure 4.2. This is likely due to the fact that the vertical thermal resistance of the bulk

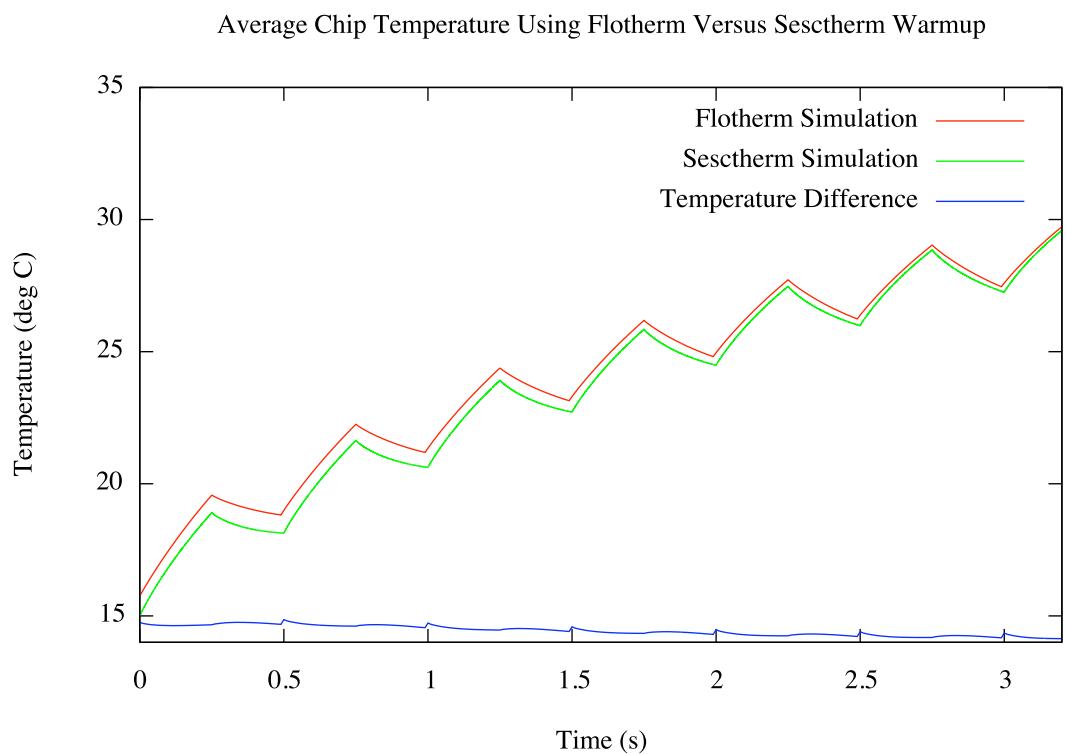


Figure 4.3: Thermal Model Verification Against FlothermTM With Focus on Chip Warmup

silicon layer is overly pessimistic. Further, the resistance-capacitance time constant with each power cycling is slightly lower than that modeled by FlothermTM. This is likely due to the fact that Sesetherm is somewhat optimistic with regard to the capacitance of one or more of its material layers. Both of these characteristics requires further analysis. This is considered future work.

Part III

Cumulative Evaluation of the Importance of Accurate Thermal Characterization for Different Aspects of a Semiconductor Device

4.4 Introduction

Various simplifications to the modeling of semiconductor devices are frequently present. Given the geometrical complexity of modern chip designs as well as the complexity of modern package and cooling systems, it is often not practical to model every aspect of the thermal system. These simplifications can include neglecting to model various elements of the system at fine detail – or simply neglecting to model certain elements of the system entirely.

Given the frequency with which simplifications are made to the thermal system being characterized, it is critical that designers fully understand the effect that neglecting such modeling may have upon the validity of the conclusions drawn from such models. Given the extreme level of complexity inherent in these thermal systems, a seemingly insignificant simplification may ultimately have significant consequences to the accuracy of the thermal model. Therefore, without an appreciation for the significance of neglecting to model certain aspects of the thermal system, designers are unable to provide quality recommendations early in the design cycle to avoid design reliability problems. Without strong confidence in the validity of these thermal systems, their very utility may be in question.

To address these concerns, Sesetherm is used to evaluate the need for accurately modeling various aspects of the thermal system. To evaluate this, we systematically remove or change the thermal characterization of one or more components of the overall thermal model. In doing so, we are able to characterize the effect of neglecting to model

certain elements of a given Integrated Circuit design.

For the purpose of this investigation, we focus on five different components of the thermal system. First, we investigate the significance of modeling the variation in interconnect density within a given design. Second, we determine the significance of including an accurate thermal model for the chip package. Third, we investigate the significance of modeling Silicon-On-Insulator (SOI) technology versus Bulk silicon technology. Fourth, we evaluate the need to model the system main-board. Lastly, we evaluate the effect of different convective cooling setups. While there are clearly many more avenues of investigation, these components of the thermal model were chosen here because of their relative lack of discussion in the literature up to this point. In particular, little discussion has been placed upon the need for modeling of Silicon-On-Insulator technology versus Bulk silicon.

The chip modeled here is an Advanced Micro Devices AMA3200BEX5AR “Clawhammer” 754 microprocessor. This chip was fabricated using a 130nm Silicon-On-Insulator technology process. A flip-chip pin-grid-array-based package is assumed. The chip floor-plan can be seen in figure 4.4. A visualization of the thermal distribution can be see in figure 4.5.

The input power trace is the same as that used in the evaluation of the FlothermTM thermal modeling framework. Specifically, using a matrix-multiply-based power profile, each unit is cycled on and off using a .25s toggle rate. Each unit uses an active power of 100mW with no static power utilization. As mentioned before, the accuracy of this power profile is not considered especially relevant for the purpose of

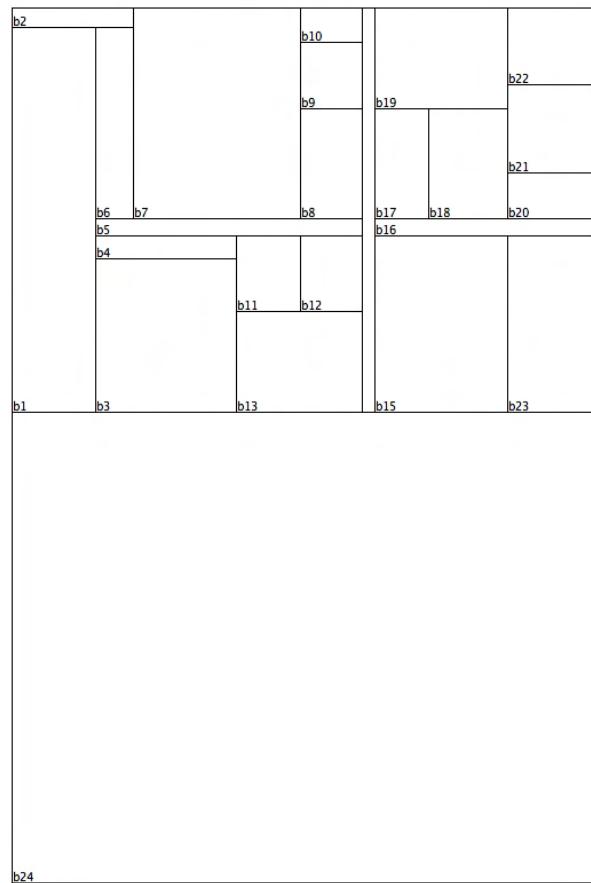


Figure 4.4: AMD Athlon Floor-plan Approximation

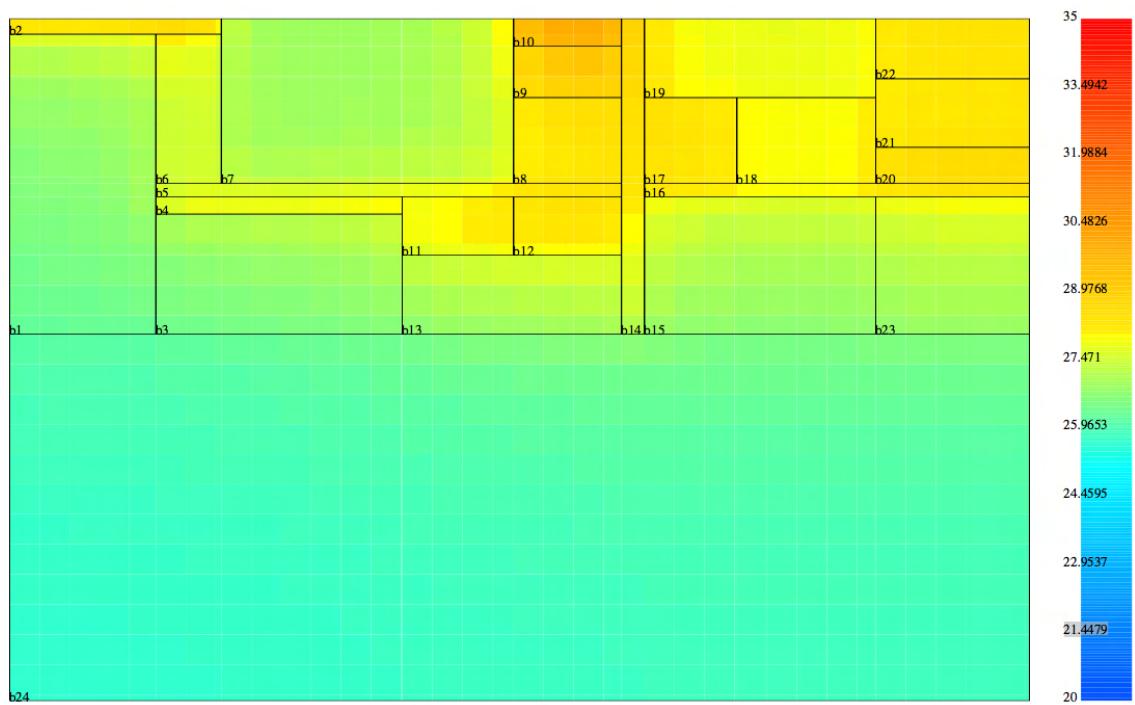


Figure 4.5: AMD Thermal Visualization

this analysis. A simple power profile was chosen to simplify analysis.

Before we separately analyze the implication of each of the thermal model simplifications previously described, it is important to gain an understand for the full combined effect of all of these simplifications. This can be seen in figure 4.6. In this figure, the “Accurate” simulation accurately characterizes the thermal effects of the main-board, package, non-uniform interconnect distribution, and Silicon-on-Insulator technology. The other, “Naive” plot neglects to model any of these elements. As can be seen, the effect on temperature is truly stunning. There is no difference in the cooling environment or input power trace in each of these cases. As can be seen, the temperature response of each of these system is entirely different. While the “Accurate” simulation predicts a transient temperature response within a temperature range of 30 to 40 degrees Celsius, the “Naive” thermal trace predicts thermal runaway, with a temperature rise quickly approaching 140 degrees Celsius.

Figure 4.6 highlights the critical importance of accurate thermal modeling. Next, we specifically analyze the thermal effect of each element here to determine the specific thermal effect on the system as a whole. As has been seen here, even seemly minor simplifications to the thermal modeling regime can have dramatic consequences if not properly understood and addressed.

Summary of Average Chip Temperature With and Without Modeling of the:
Main-board, Interconnect Density Variation, Package, or Silicon-On-Insulator Technology

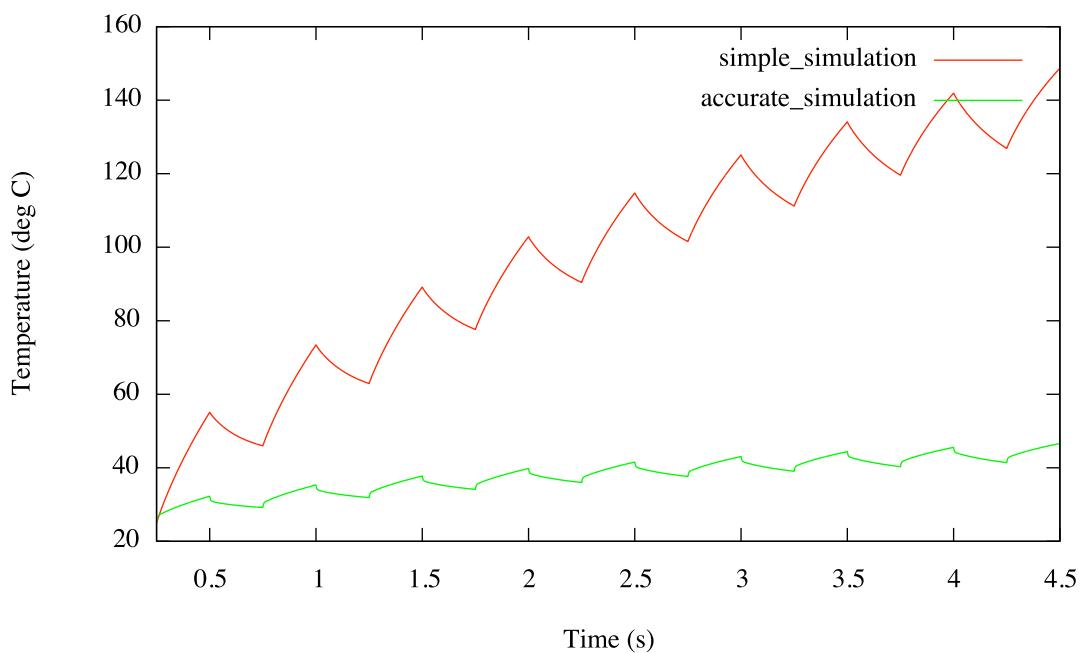


Figure 4.6: Combined Error When Main-board, Package, Interconnect Distribution and Silicon-On-Insulator Technology Are Not Modeled

Chapter 5

Importance of Accurate Interconnect Modeling

5.1 Introduction

Metal interconnect layers are modeled in a variety of different ways depending upon the thermal model. In fact, despite the relative agreement between different thermal models with regard to many aspects of the overall model design, there appears to be little agreement with regard to the appropriate modeling regime to appropriately characterize the temperature distribution in this portion of the chip. There are several reasons why such a disparity in modeling regimes exists with regard to the metal interconnect layers.

First, the detailed modeling of the complex material distributions in this region of the thermal model is very costly to simulation runtime. In particular, with so

much variability in the distribution of metal and dielectric materials, grid-based thermal solvers require a prohibitive number of temperatures nodes to fully characterize the thermal system. This can dramatically lengthen the duration of time for a given thermal simulation. Given this fact, many thermal models attempt to simplify the complex distributions into lumped material properties that capture the effective thermal conductivities, densities, and specific heats for the entire stack of interconnect layers.

Second, there is little agreement with regard to the importance of accurately characterizing these metal interconnect layers. As previously mentioned, many modeling regimes call for simple lumping of the relevant thermal properties for the interconnect layers. However, there are many ways that such lumping can occur. A detailed discussion of these various lumping methods is previously discussed in section 3.5. Without a detailed appreciation for the consequences associated with neglecting certain thermal properties for these layers, no approach is perceived to be better than any other. Further, without an understanding of the loss of accuracy when employing these model simplifications, critical insights into a variety of different thermal phenomena may be missed in the analysis.

For the purpose of this analysis, we explore the question of the significance to modeling the interconnect density distribution across each interconnect layer. While many papers have already been published on various statistical techniques to model the interconnect distribution across the various metal interconnect layers associated with a given design, these models make an inherent assumption that the interconnect distribution laterally across each of the metal layers is uniform. That is, these statistical models

can only describe the number and length of interconnect for each metal layer. However, they cannot describe the detailed, nonuniform, interconnect distribution within each of the interconnect layers.

To address this problem, many models assume that while each metal layer may have a different number of interconnects of certain length, the distribution of such interconnects in each layer is assumed to be uniform. While such assumptions may be reasonable for the purpose of performing a specific analysis, in the general case such approximations may have significant thermal consequences if used inappropriately. We show we that the use of statistical interconnect models may not alone be sufficient to accurately characterize the thermal behavior actually observed from empirical data.

5.2 Setup

As can be see in figure 4.4, floor-plan units b5, b14 and b16 represent the clock interconnect distribution. This is a region of the chip of high interconnect density, but relatively low transistor density. To model this, Sesctherm defines these regions are having 33% of the transistor density as the remainder of the chip, and 300% of the interconnect density. Although these percentages are chosen arbitrarily, manual inspection of clock distribution on similar designs revealed comparative difference in metal interconnect density in these regions of the chip design.

For simplicity, each unit is toggled on and off every 0.25s. When active, each unit uses 100mW of active power. When deactivated, each unit uses no static power.

5.3 Results

As can be seen in figure 5.1, including the effect of the interconnect density distribution decreases the average chip temperature. This intuitively makes sense. However, given the fact that the entire interconnect layer stack is less than $1\mu m$ thick compared to the silicon substrate which can be anywhere from $300\mu m$ to $800\mu m$, it is surprising that even a modest variation in the distribution of metal interconnect can cause such a significant difference in the average chip temperature.

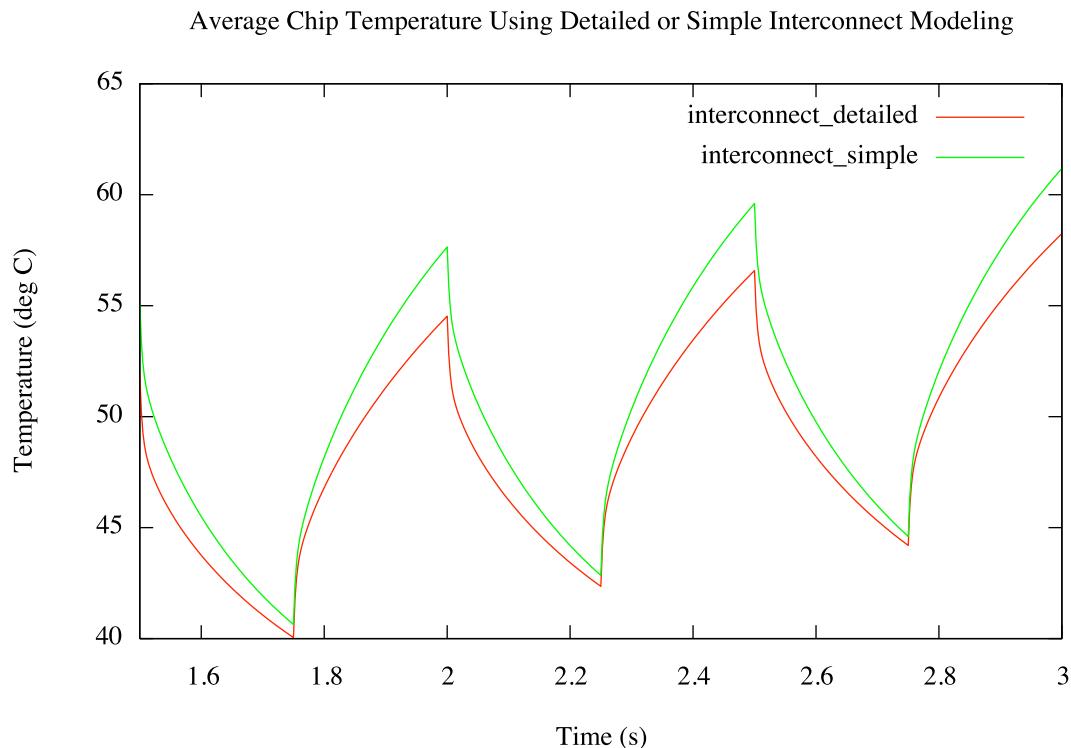


Figure 5.1: Comparison of Detailed and Naive Interconnect Modeling

As can be seen in figure 5.1, the average temperature in the simulation characterizing the interconnect density distribution is anywhere from 1 to 5 degrees Celsius less than the other. While the temperature difference is only modest, this highlights possibly new avenues of research where the existing interconnect could be used as a on-chip heat-spreader-like structure.

It can be seen in figure 5.2, that by modeling the interconnect floor-plan units b5, b14 and b16 as having 300% higher interconnect density than the other blocks, it is shown that the heat is being more evenly spread across the chip. Floorplan unit b10 has a drop in temperature of 10 deg C as a result of the characterization of higher interconnect density in these regions of the chip. This is consistent with figure 5.3, where heat is being seen taken away from the hot instruction schedulers and passed through the clock distribution to the rest of the chip.

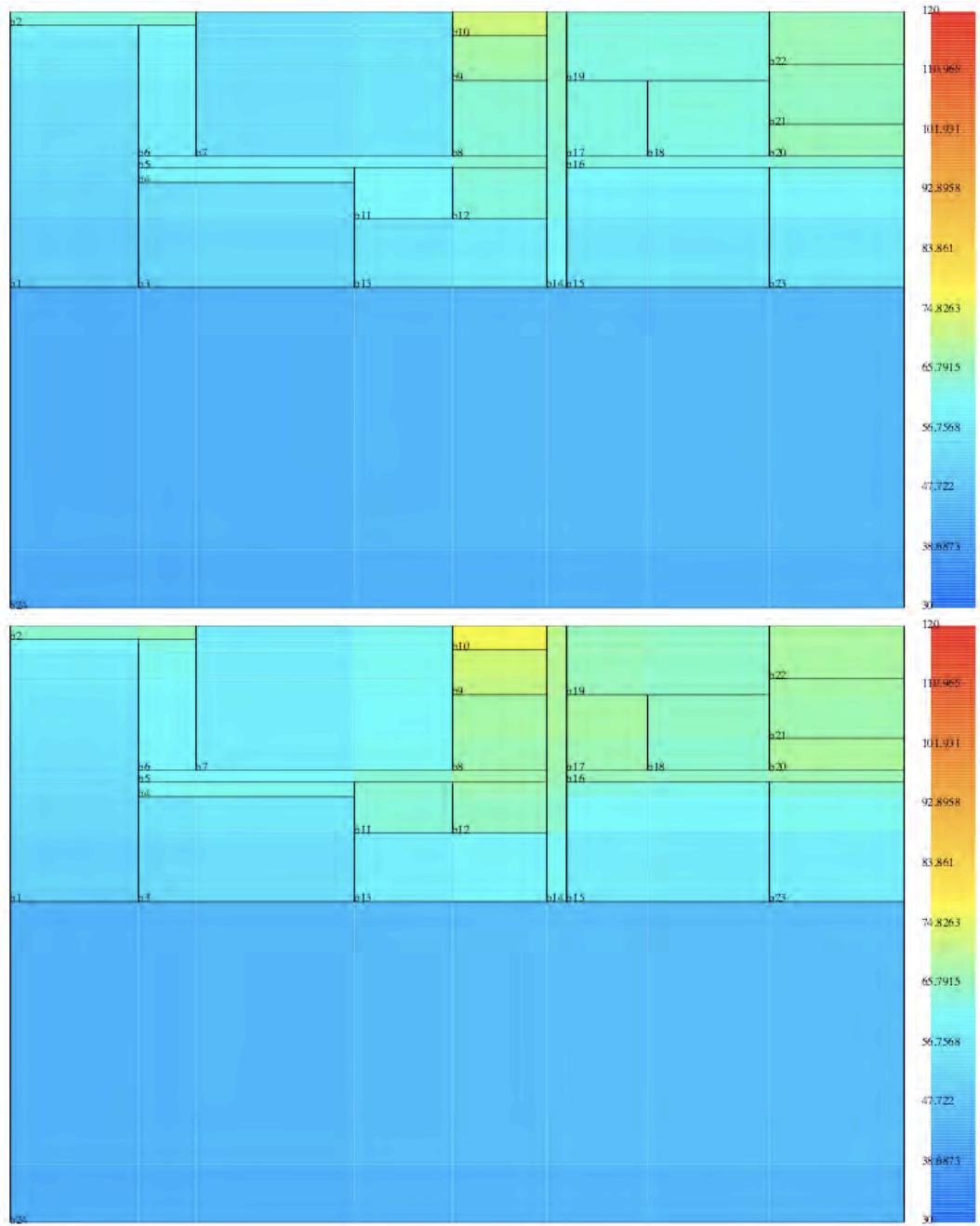


Figure 5.2: Simulation Visualization
 (a) With Variable Interconnect Density Modeling
 (b) Without Variable Interconnect Density Modeling

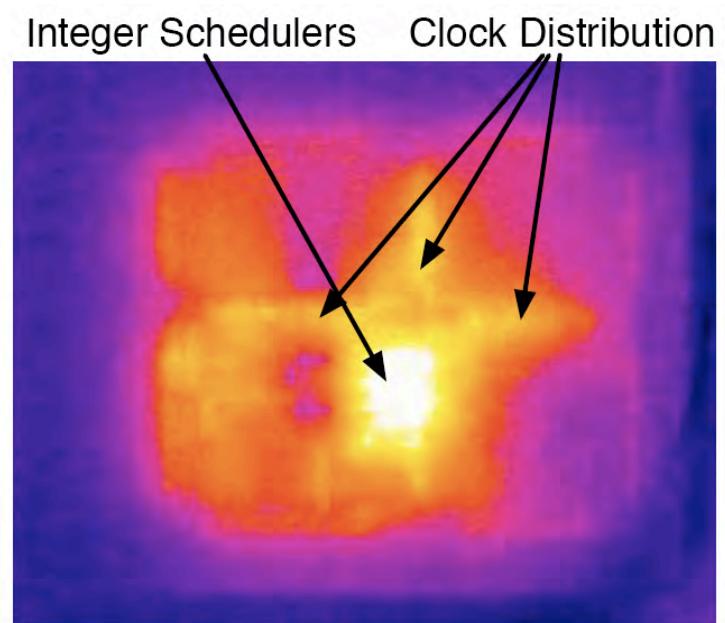


Figure 5.3: Advanced Micro Devices AMA3200BEX5AR “Clawhamme” 754 Microprocessor Thermal Image

Chapter 6

Importance of Accurate Package Modeling

6.1 Introduction

Another area of apparent disagreement is with regard to the significance of accurate modeling for the system package. This is an area that has received greater attention more recently in the literature [71]. Here we show the impact of neglecting to model the system package.

6.2 Setup

Two thermal simulations are performed here. The first simulation uses a full set of material layers to model the Advanced Micro Devices AMA3200BEX5AR micro-processor. A Silicon-On-Insulator technology process is modeled, and the floor-plan is

the same as that described previously. Further the power input trace was the same as previously used. Specifically, a matrix-multiply-like input power trace was used, where each unit was toggled every 0.25s. The active power utilization for each device is 100mW, while the inactive power utilization is 0W.

6.3 Results

As can be seen in figure 6.1, the addition of the system package decreases the dynamic temperature fluctuations. Stated another way, the temperature rise with each temperature spike is more gradual with the inclusion of package modeling. The drop in temperature is on the order of approximately 1 deg C.

This result may be surprising in that one might expect that the including of a relatively poor conducting package that surrounds a given integrated circuit would necessitate an actual increase in temperature both at relatively low time scales of several seconds, to longer time scales of several minutes. Further, it can be seen that this disparity in temperature rise is actually cumulative, where the temperature difference actually increases over time. There are several reasons for this behavior.

The first significant reason is due to a phenomenon that is not specifically shown in figure 6.1. In general, the convective cooling of the chip through forced convection flow of a coolant is directly proportional to the surface area over which the coolant flows. In this particular case, the added surface area of the package, although a relatively poor conductor compared to the chip itself, provides the requisite surface

area over which convective cooling can occur.

The second significant reason for this behavior is that the resistance-capacitance of the thermal system is higher with the addition of the system package. Stated simply, the added heat capacitance of the package to the thermal system allows it to be better able to absorb some of the transient temperature fluctuations. This can be seen in figure 6.1.

In this figure is can be seen that at each temperature spike, there is an initial rapid temperature spike in the silicon substrate. This is due to a self-heating-like effect in the bulk silicon substrate where the limited surface area over which cooling can occur over the top of the silicon substrate, combined with the high thermal resistance between the bottom of the chip and package provides insufficient heat transfer to cool the rapid temperature spike. Much like a hotspot, this means that that system is unable to respond in a sufficiently rapid way to mitigate this rapid increase in heat dissipation. The high resistance between the package and substrate is such that there is little impact upon this hotspot phenomenon.

Despite the fact that this initial temperature spike is relatively unchanged with the inclusion of the package modeling, the second portion of the thermal spike has a significantly longer time-constant for the temperature rise. In particular, this later portion of the temperature spike is a much more gradual temperature increase. The reason for this is that while the thermal resistance between the chip and package is too high to initially allow heat to adequately flow into the system package when the substrate temperature is similar to that of the package substrate, once the substrate

temperature has risen sufficiently, heat is able to flow into the system package. The rate at which this heat transfer occurs from the substrate to the package is not adequate to prevent the substrate temperature to continue to rise, as shown in figure 6.1. However, the heat flowing into the package is sufficient to provide a reduction in the rate of that temperature increase. This is what is the observed behavior here.

It is primarily due to these two factors that the chip temperature drops despite the fact that a poor-conducting package is used to encapsulate the sides and bottom of the chip. Further, this is a key example where a complex thermal system may actually behave in very non-intuitive ways. It is therefore of great importance that designers fully understand the implications of certain model simplifications.

There are clearly areas of additional improvement for Sesetherm. In particular, Sesetherm is currently designed to model a flip-chip pin-grid-array-type package design. Many other package types are common including BGA, PLCC, and TQFP. Given the preponderance of a great many disparate package designs including a variety of SIP-type designs, there is a great opportunity for Sesetherm to develop a more robust package modeling framework.

One possible means for attaining such a robust package modeling framework is one that allows the automatic characterization of both material properties and package geometry using SEM (scanning-electron-microscope) images. An open-source software package for the purpose of performing finite-element analysis of microstructures known as OOF2 may provide the software foundation for such an improvement to the existing package modeling subsystem. While OOF2 is only currently equipped for two-

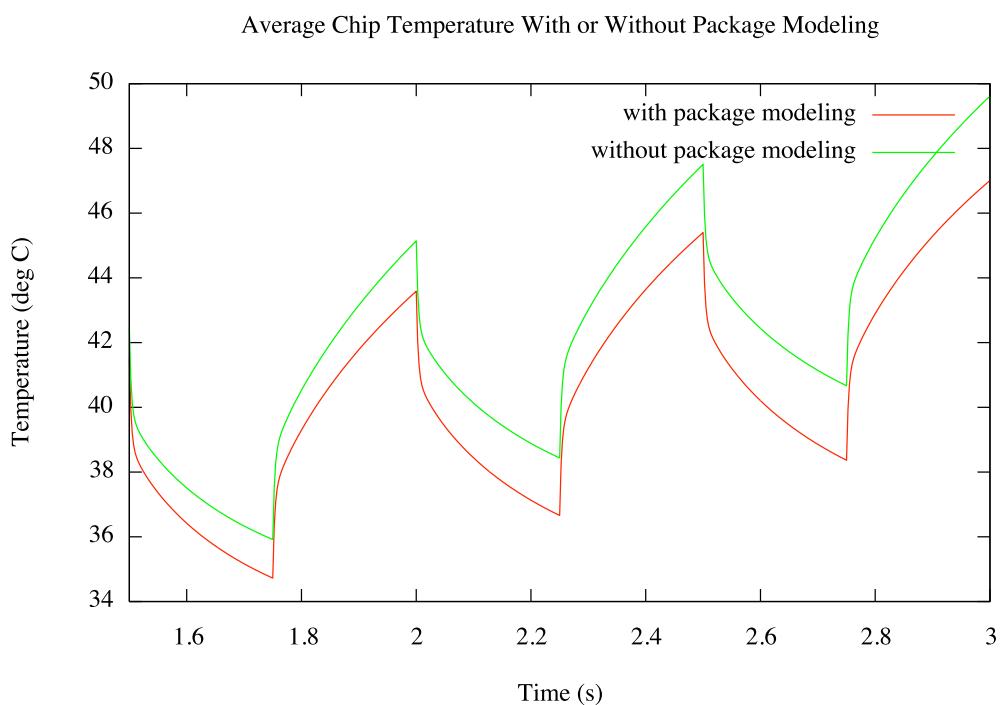


Figure 6.1: Average Temperature Difference With and Without Detailed Package Modeling

dimensional analysis, OOF3, currently in development, is designed to provide three-dimensional materials analysis. This is considered future work.

Chapter 7

Importance of Accurate Silicon-On-Insulator (SOI) Modeling

7.1 Introduction

There has been much discussion recently in the literature with regard to the significance of modeling the self-heating behavior in Silicon-On-Insulator devices [70, 37]. However, discussion in the literature has been largely restricted to the sub-micro-meter thermal behavior of these devices. Little attention has been paid to the cumulative thermal effects of many of these devices operating at chip-level, sub-mm thermal scales. We attempt to evaluate here the macroscopic thermal behavior of Silicon-On-Insulator devices.

7.2 Setup

To evaluate the difference in thermal behavior of Silicon-On-Insulator devices, two thermal simulations are performed. The first thermal simulation assumes a bulk silicon technology process, while the second simulation assumes a Silicon-On-Insulator technology process. The standard modeling setup as has been previously described is used for both simulations. This includes the same forced-convection air cooling setup, same input power trace, and same chip and package geometry.

It should be mentioned that the thickness of the bulk silicon layer for simulation using bulk silicon technology was set to be the same as both the silicon-thin-film layer and bulk silicon layer for Silicon-On-Insulator technology. Although this determination may be considered reasonable in the general case, these thicknesses may actually vary significantly depending upon the specific technology process. Therefore, specific considerations must be made when considering a specific fabrication process.

It should further be mentioned that assuming everything else being the same, a given design implemented using SOI will likely use less power than that of the implementation using a bulk silicon technology process. Despite this fact, this paper is not concerned with the characterization of the input power trace for each of these technologies. We are only concerned with the thermal behavior of each device. Therefore, the same power trace is used to show the variation in thermal behavior in response to the same input power.

7.3 Results

Observing figure 7.1, it can be seen that the SOI simulation clearly showed different thermal behavior than that of the bulk silicon technology. In particular, high-frequency components of the temperature spike seen in the SOI simulation are not present in the bulk silicon temperature trace. These high-frequency components are the reason for the rapid temperature change at the start of each resistance-capacitance curve.

What is of specific curiosity in the SOI temperature trace is that the high-frequency behavior in each transistor device, documented in many papers [70, 121], is actually present to a lesser extent as the macroscopic chip-level scales shown here. This may have dramatic implications to reliability of SOI devices as various reliability metrics including electro-migration, dielectric breakdown, and material structural integrity are highly a function of these rapid temperature spikes. An investigation into the reliability consequences of this behavior is considered future work.

Besides the difference in the high-frequency components to these two thermal traces is the fact that the SOI device exhibits an increase in temperature on the order of 1-2 deg C. This is consistent with self-heating effects described in the literature. It should be reiterated that we assume the same power profile in both designs. In reality, the SOI implementation would likely use less power.

The two thermal traces described in figure 7.1 monitor the average temperature across the bulk silicon substrate for both the SOI and bulk silicon technology

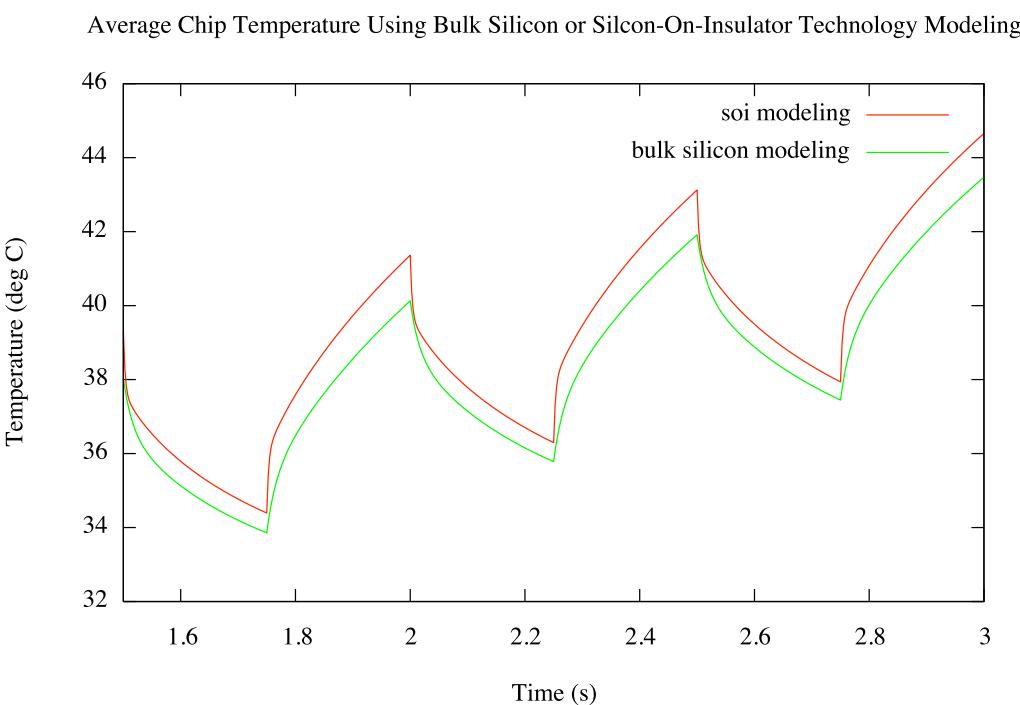


Figure 7.1: Thermal Model Simulation Comparison of Bulk Silicon and Silicon On Insulator Technology

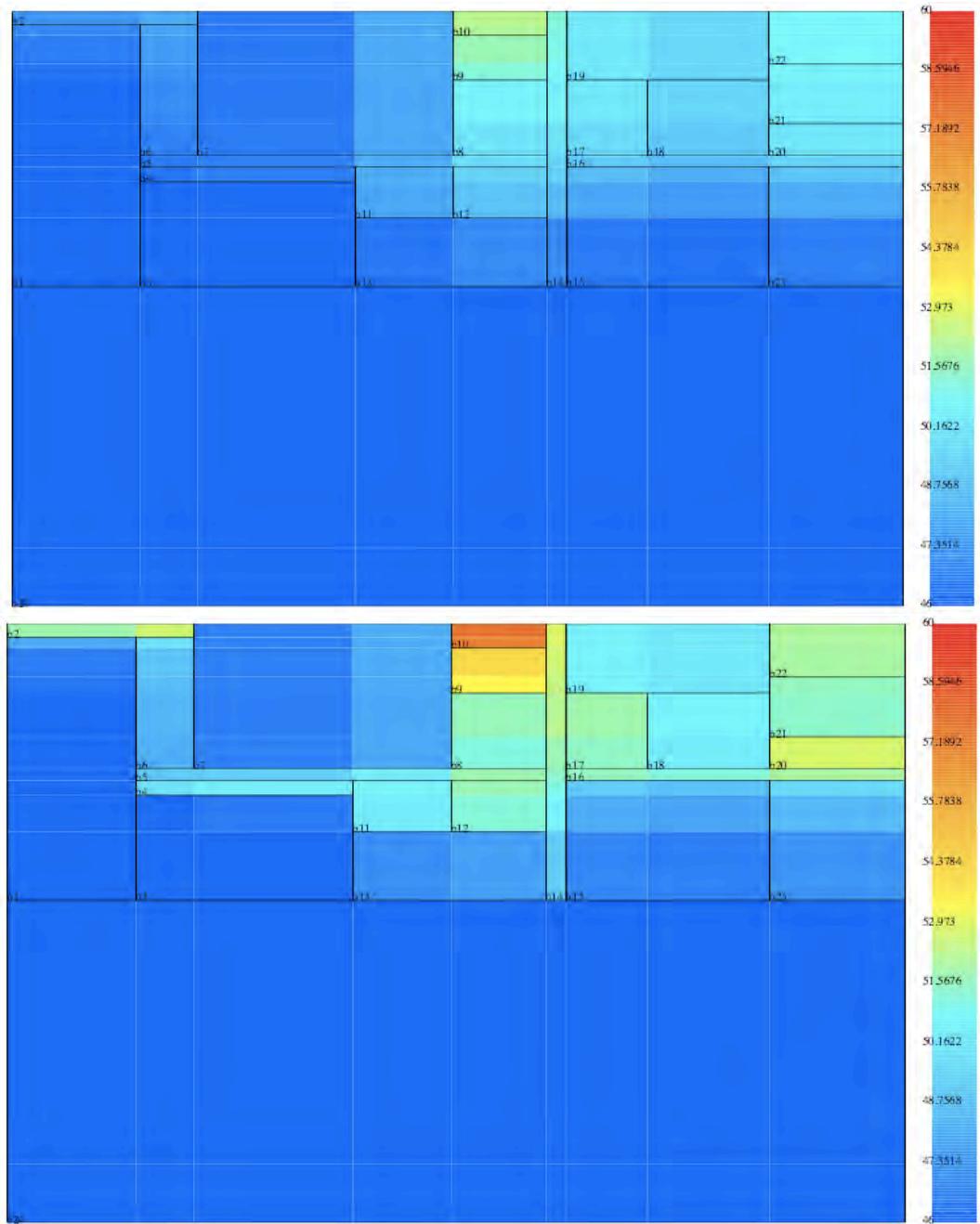


Figure 7.2: Thermal Model Visualization (a) Bulk Silicon and (b) Silicon On Insulator Technology

simulations. However, when the temperature fluctuations in the actual silicon thin-film layer of the device fabricated using SOI technology is compared to the transistor device layer temperature of the device fabricated using bulk silicon technology, the difference is shown to be more significant. This can be seen in the graphical visualizations of the device temperature distributions for both simulations in figure 7.2.

As can be seen in figure 7.2, there is a generalized increase in temperature of the active regions of the device, with some regions experiencing surprisingly large temperature increases. In particular, block b10 at around 52 deg C with the bulk silicon simulation is shown to have a temperature of nearly 58 deg C with Silicon-On-Insulator technology. This amounts to roughly a 6 deg C increase in temperature to this region of the chip. Such rises in temperature may have significant thermal consequences to the reliability and contribute to “hotspot” formation.

Chapter 8

Importance of Accurate Main-board Modeling

8.1 Introduction

Due to the fact that the system main-board temperature does not fluctuate significantly, it may seem reasonable to consider accurate main-board modeling as a relatively insignificant component of the thermal system. As such, the influence of the system main-board on the transient temperature distribution within a given chip design is considered relatively minor. Hence, the main-board may be simplified in a variety of ways, including aggressive lumping with few temperature nodes – or even reducing the entire main-board to a single temperature node with one resistance and one capacitance.

We attempt here to determine the importance of the main-board on the temperature profile of a given chip design. However, the impact of these simplifications is

only briefly analyzed here. Further analysis is necessary to fully appreciate the full influence of the main-board on the thermal system. In particular, multi-processor systems cause heat to be distributed among the processors.

8.2 Setup

The main-board modeling setup was consistent with that of the other thermal simulations. The Advanced Micro Devices floor-plan, chip geometry, and package geometry was used. A main-board geometry was used that is consistent with any standard printed-circuit-board found in a personal computer. The power trace used was the same matrix-multiply-based power trace used in the other simulations. Specifically, each active unit was considered to use 100mW of active power, while each inactive unit was considered to use 0W of static power.

8.3 Results

As can be seen in figure 8.1, the main-board does have a modest impact upon the transient thermal of the system. The inclusion of an accurate main-board model causes a temperature drop between .1 and 1 deg C. However, it can be seen that this temperature difference grows over time as the resistance-capacitance time constant of the entire thermal system has been increased.

In summary, we can see here that the main-board has a similar impact as the inclusion of an accurate package model. Specifically, the fast transient response of

the system is largely unaffected due to the large thermal resistance between the silicon substrate and the main-board. However, it can be seen that the inclusion of the large thermal capacitance of the main-board, along with the additional convective cooling due to the large surface area over which fluid flow occurs causes a modest temperature reduction. Further, it can be seen that the effect is cumulative over time.

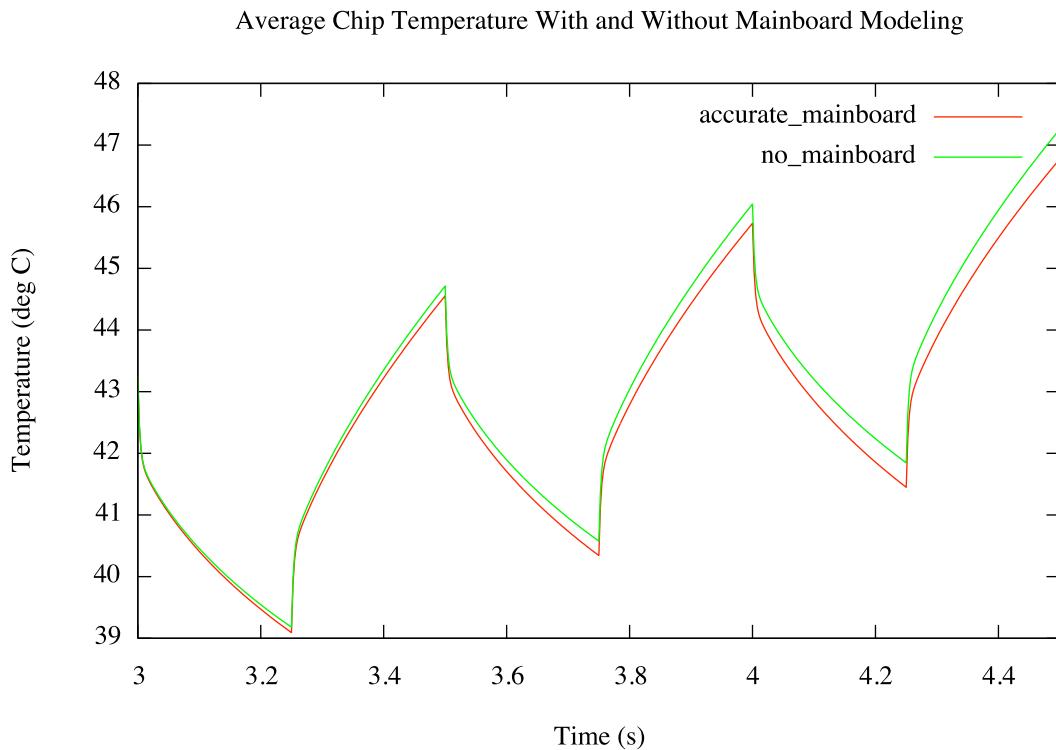


Figure 8.1: Average Temperature Difference With and Without Main-board Modeling

It should be noted that although not readily apparent in figure 8.1, in the absence of effective heat-sink devices, the main-board is an important means for convective cooling activity. While this cooling will not significantly impact the transient response

of the system, there will be an overall reduction in the steady-state temperature of the system. Further, such minor changes may be sufficient to avoid certain thermal runaway phenomenon.

Chapter 9

Importance of Accurate Convective Cooling Modeling

9.1 Introduction

In this analysis, we attempt to characterize the impact of changing different aspects of the forced convection cooling regime. In particular, the impact of changing the inlet distance of the coolant and the impact of changing the flow rate of the coolant over the surface of the chip is analyzed. Further, we show the effect of using an oil coolant instead of air.

9.2 Setup

The setup here is consistent with that used in the other thermal simulations. An Advanced Micro Devices chip, fabricated using a 130nm, Silicon-On-Insulator tech-

nology process is modeled with both a flip-chip pin-grid-array based package and system main-board. As with the other simulations, the top of the bulk silicon substrate is directly exposed to coolant flow.

In the first analysis, the rate of air coolant is held constant, while the distance of the air inlet is allowed to vary. The air flow is considered to flow parallel to the surface of the chip. Further, air is passed both over and under the package and mainboard. The air flows along the width of the chip. To provide a baseline, a simulation with only ambient air is used.

In the second analysis, the inlet distance is held constant, while the fan velocity is allowed to vary. As before, the air flow is considered to flow over the surface of the chip. Likewise, air is allowed to flow over the system package, over the main-board, and under the main-board. In addition to air, a simulation with a mineral oil coolant is used. The rate of oil flow is held constant at 10 m/s.

9.3 Results

As can be seen in figure 9.1 (a), the inlet distance has an amazingly small impact on temperature of the chip. Viewing a higher resolution thermal trace in figure 9.1 (b), it can be seen that the temperature difference between having the air inlet 0mm away from the edge of the chip as opposed to 100mm away from the edge of the chip only impacts the ambient temperature by a maximum of .1 deg C. Further, the impact of having no air flow at all only has a marginal impact.

This result may be surprising, however it should be noted that it is assumed that the ambient air temperature is held constant throughout this simulation at room temperature. Although not shown, when the air temperature is not held constant, this behavior does not follow the trends shown here. When the air temperature is not held constant, the impact of the fan distance is greater than that shown here.

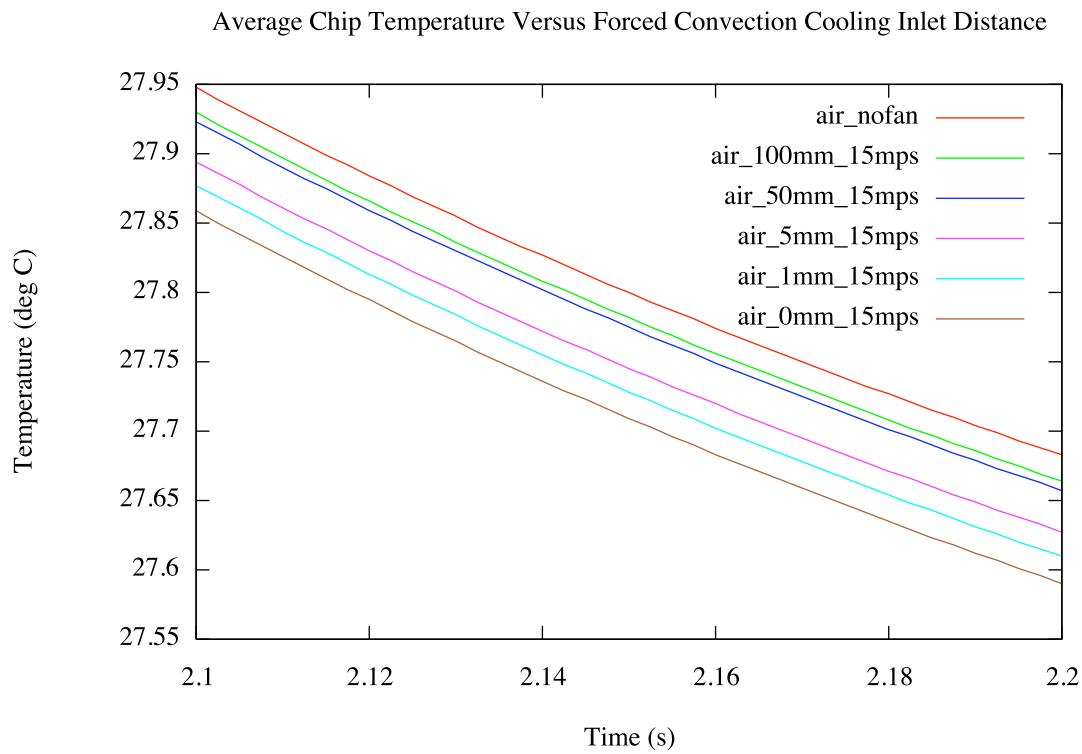
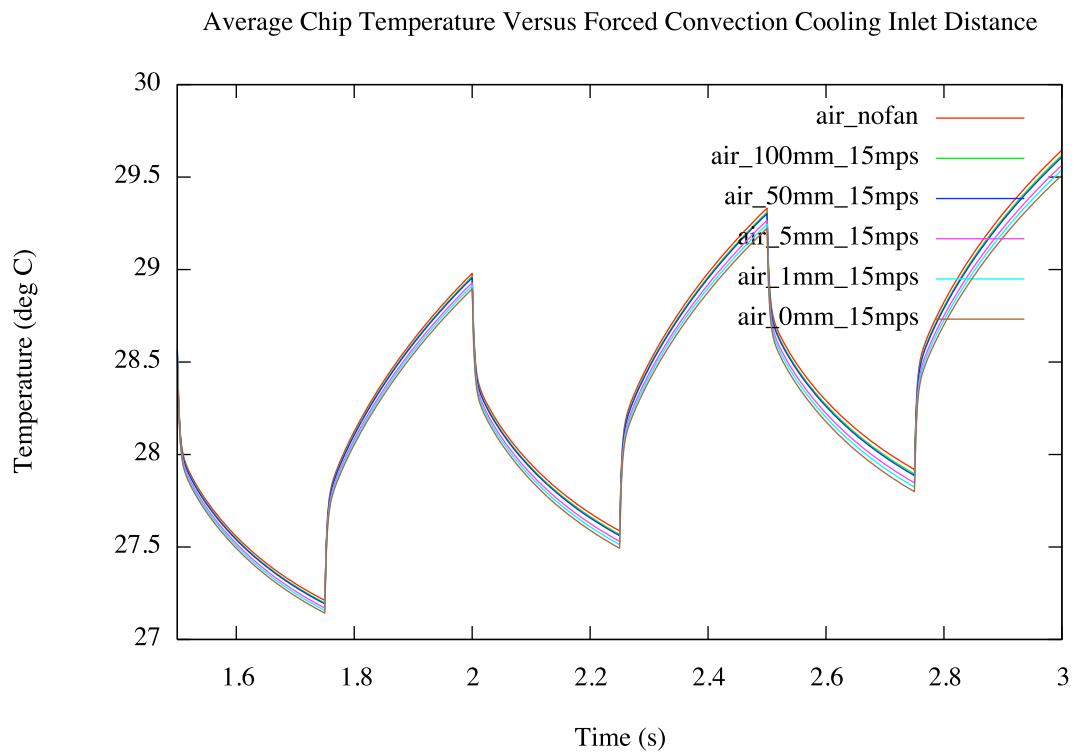
The reason why the air temperature is chosen to be constant is that without detailed knowledge of environment in which the chip is operating, it is difficult to make any predictions about how the heat released into the ambient environment will impact the ambient temperature. Further, this is the reason why many thermal models assume a constant ambient temperature. For the purpose of this analysis, we assumed the ambient temperature to be 21 deg C. Many models assume that if the chip is to be run in a warm chassis, the temperature to be roughly 30 deg C.

Disregarding the fact that the ambient temperature is held constant, it may still be surprising that the temperature change is so modest. This behavior may be shown to be result of several factors. First, the rate of heat transfer is highly a function of the area over which convective cooling occurs, and the area over which convective cooling occurs in these simulations is a very small area. Second, it can be shown that the average coefficient of convective heat transfer only varied modestly. The reason for this is that while the rate of heat transfer is inversely proportional to the distance from the fluid inlet, over the limited range of distances here any negative consequences associated with increased distance from the fluid inlet is somewhat mitigated by the fact that the air flow transitions from laminar to turbulent flow.

In summary, we see here that the distance of the air inlet from the side of the semiconductor device has a very modest effect on the thermal performance of the model when all components of the thermal system are being modeled – package, main-board, and interconnect. Despite this conclusion, it should be noted that these conclusions may no longer be valid if one or more of the previously mentioned simplifications to the modeling regime are employed. In particular, if the main-board or device package are excluded or simplified in some way from the thermal analysis performed here, these conclusions may change somewhat.

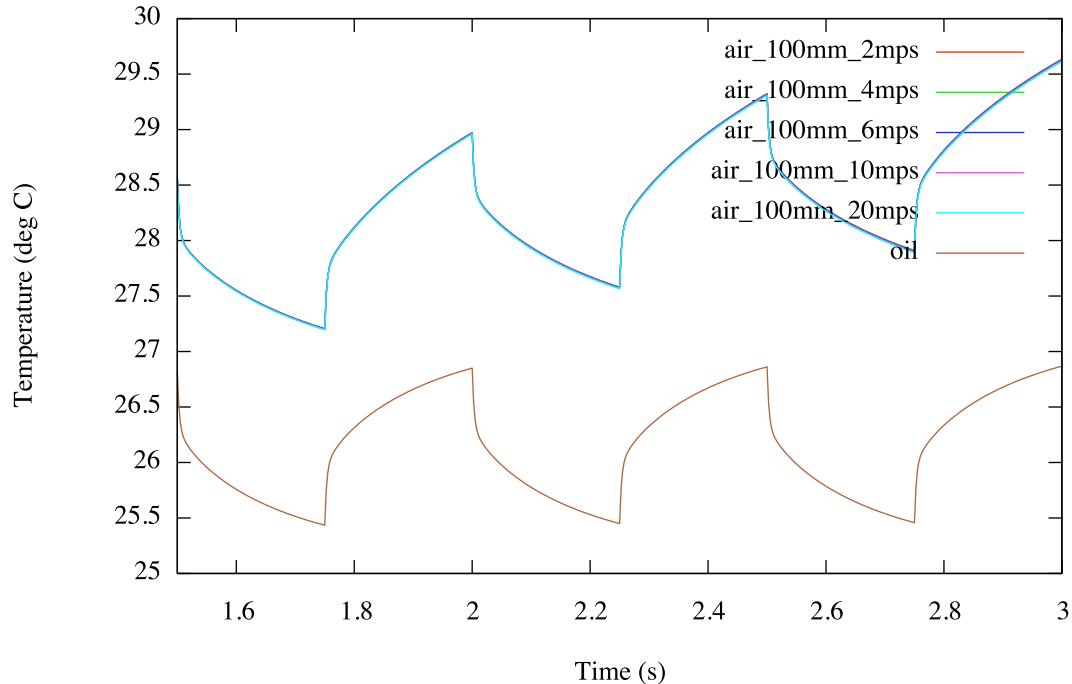
In a second simulation, we allow the air flow rate to vary. It can be seen in figure 9.2 that the effect on temperature is even more modest than that seen in the previous simulation. This is due to the same factors previously described. Namely, given the small area where convective cooling occurs and given the fact that air temperature is held constant, the overall rate of convective cooling is very similar in each simulation.

An added observation here of particular interest is that of using oil as the coolant. As can be seen this causes a modest reduction in temperature. Further, this causes a modest increase in the resistance-capacitance time constant. The reason for this behavior is consistent with that previously described.

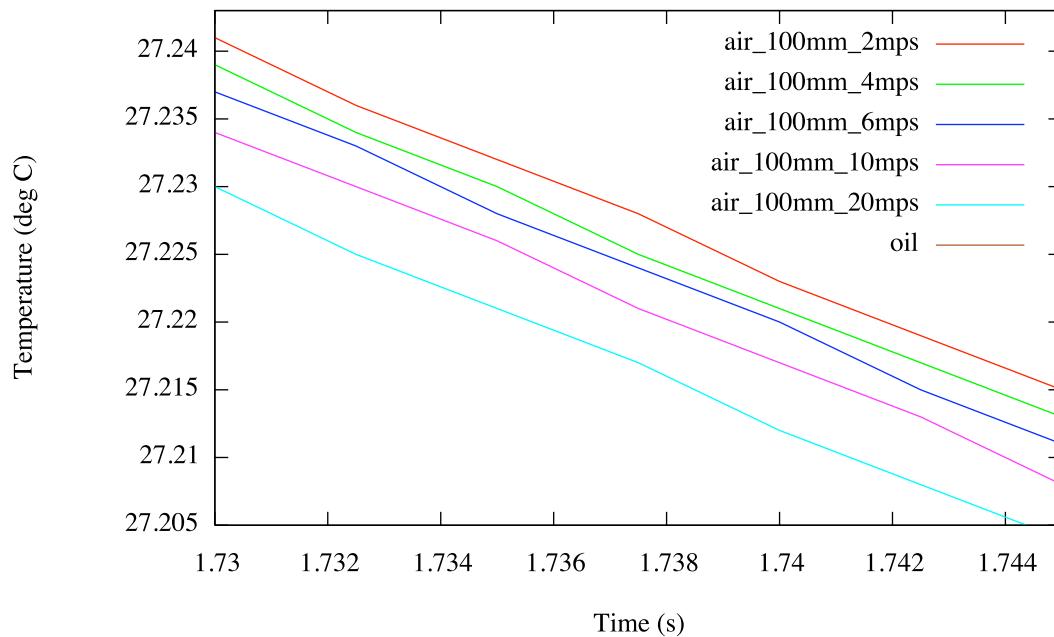


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Figure 9.1: Average Temperature Difference As A Function of Fluid Inlet Distance (a)
and zoomed view (b)

Average Chip Temperature Versus Forced Convection Cooling Flow Rate, including Oil Coolant



Average Chip Temperature Versus
Forced Convection Cooling Flow Rate, including Oil Coolant Flow



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Figure 9.2: Average Temperature Difference As A Function of Fluid Flow Rate (a) and zoomed view (b)

Chapter 10

Future Work

10.1 Validation Against Altera StratixTM II FPGA

Unlike the thermal test chip setup where only one heater was used, real semiconductor devices involve many heat sources operating independently. Therefore, an accurate evaluation of a thermal modeling system necessitates a look at the transient thermal response across different regions of the chip with many independent heat sources. To generate such a system, we chose an Altera StratixTM II FPGA.

An FPGA was chosen in this case because of the highly regular structure of the programmable chip. Further, logic blocks can be locked to particular regions of the chip. This implements a crude floor-plan, where each floor-plan unit is a logic-locked region on the FPGA. Further, each of these logic-locked regions can be independently activated using clock gating. By cycling through each of the logic-locked regions, we can simulate a complex system with multiple heat sources operating independently.

To implement the FPGA design, a multiply-accumulate block was programmed into 255 logic blocks, where each logic block occupies the resources of 3 logic array blocks (LABs). It was found that seventeen of these logic blocks would fit into a single logic array across the width of the chip. Further, fifteen of these logic arrays could be programmed. To simplify the analysis, each three logic arrays were grouped into a single heater group. This would generate fifteen heaters, where each heater would be a horizontal strip along the width of the chip. This can be seen in figure 10.1. Each three columns was therefore designated a single enable. An overview can be seen in figure 10.2. The FPGA design was synthesized at 250MHz.

Power estimation for the design was performed in QuartusTM. Assuming that the logic blocks follow an activation rate that is nearly proportional to a 16-bit binary counter, we assume that the transistors are activated, on average, once for every eight clock cycles. This means that the IO toggle rate will be 12.5% of the clock. However, we also analyzed the temperature distribution where the IO toggle rate was much higher. As can be seen in table 10.1, static power is roughly constant regardless. However, the dynamic power can change widely.

IO Toggle Rate %	Total Power (mW)	Dynamic Power (mW)	Static Power (mW)
80.0	1170	369	766
12.5	991.74	202.29	759.60

Table 10.1: Altera Stratix II Dynamic/Static Power Estimation

Since only one heater group is active at any given time, we assume that the

active power of such a group is equal to the total dynamic power, plus one-fifteenth of the total static power. This methodology is reasonable given the fact that each heater group has the same number of programming logic blocks. Further, the activity rate of each group is equal to all the others. It should be noted that little is known about the unused regions of the chip. We assume that these regions use no dynamic or static power. A more accurate characterization of the power profile of the chip is possible using the methodology described in [82]. This is left as future work.

One of the problem with the mapping of logic blocks to logic-locked regions is that the logic array blocks are not evenly spaced across the FPGA. As can be seen in figure 10.1, unused RAM and DSP blocks segment the logic arrays throughout the design. Further, some of the logic blocks did not precisely fit the multiply-accumulate block. This is the case with heater groups 2 and 3.

Further, even with knowledge about the relative distribution of device elements (memory, logic block, DSP), it is difficult to create an exact geometry of the distribution. The reason for this is that although Altera provides a theoretical mapping of logic blocks to programmable regions of the chip, the actual sizing of each of these theoretical structures is unknown. Therefore, although it appears in figure 10.1 that each of the unused regions between the logic-locked regions is equal in size, the actual size may vary dramatically.

Despite these limitations, we constructed a floor-plan based upon the apparent regions of heat generation. Specifically, each of the 5 heater groups was cycled like a 5-bit barrel shifter. When a given region was activated, the corresponding physical region

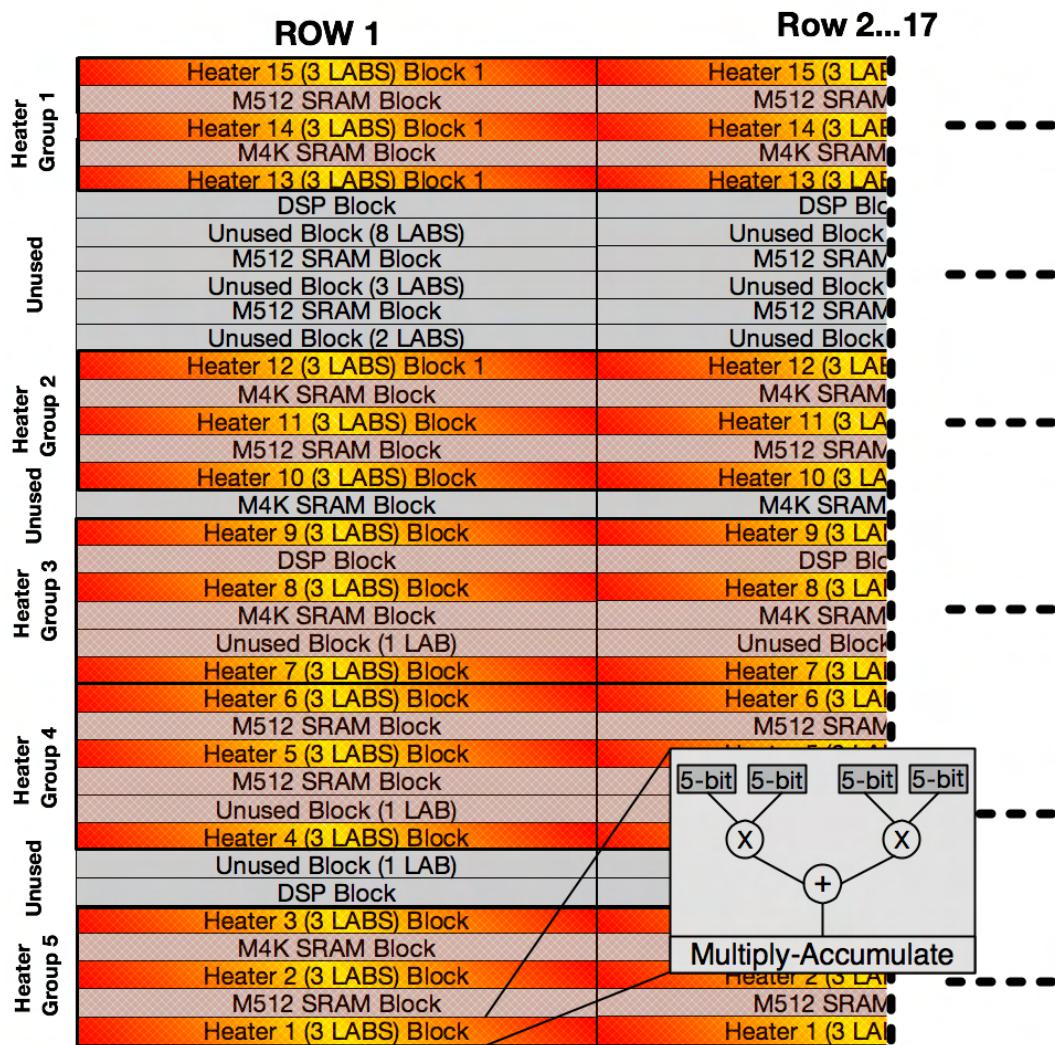


Figure 10.1: Stratix II Heater Block Overview

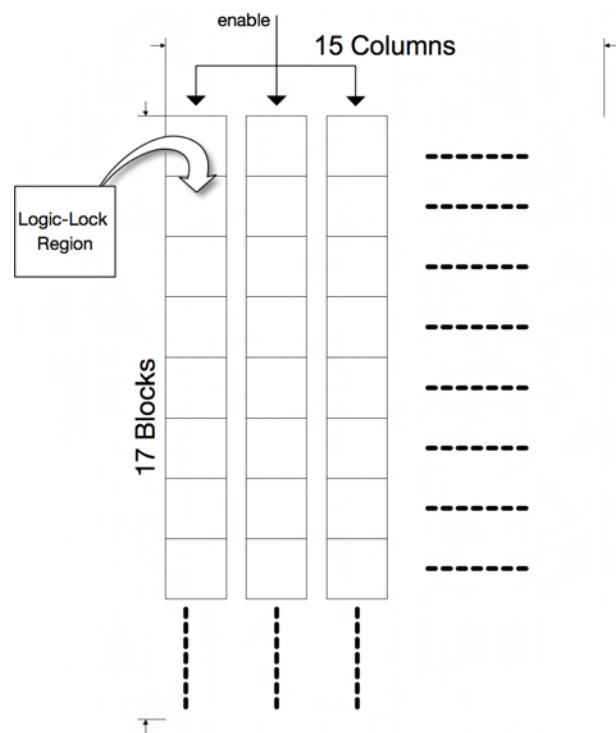


Figure 10.2: Stratix II Heater Block Overview and Logic Locking

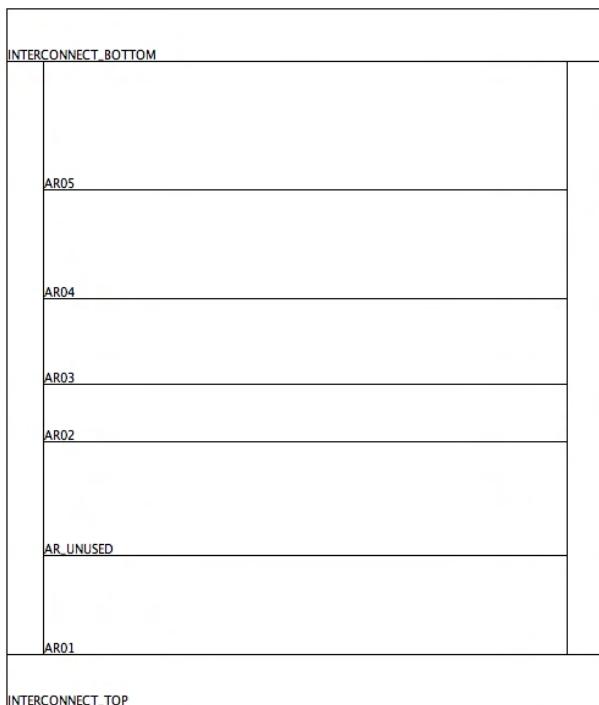


Figure 10.3: Altera Stratix II FPGA Floor-plan Layout

of the chip was deemed the area of the corresponding heater group. This was used to generate the floor-plan in figure 10.3. The regions at the outer boundaries of the chip area are considered IO blocks. Due to the fact that all IO was disabled in the design, these regions are considered to have limited activity.

To determine the temperature distribution across the Altera StratixTM II FPGA, a FLIR SC4000TM infrared thermal camera was used. The FLIR SC4000TM is a science-grade infrared camera with high resolution and sensitivity. Further, the camera is designed to capture infrared radiation in the medium wave infrared range (between 3 um and 5 um). Between 3um and 5um, bulk silicon is partially transparent to infrared radiation. In particular, the transmittance is on the order of 55 % within this range, while it is largely opaque outside of this range.

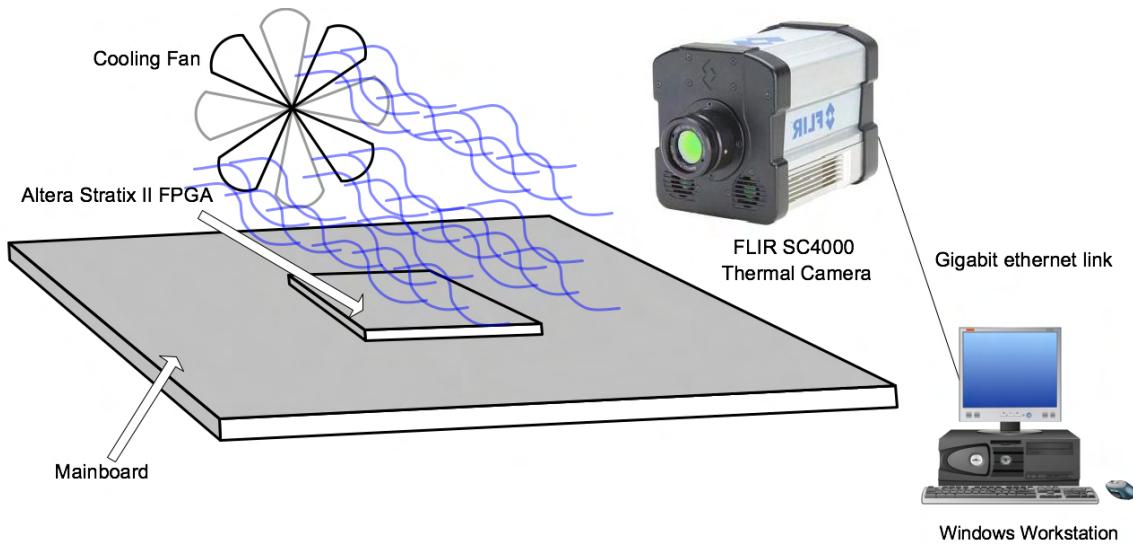


Figure 10.4: Altera Stratix II FPGA Setup

As can be seen in figure 10.4, a gigabit Ethernet connection to windows-based computer was used for data acquisition. Using FLIR ThermaCA ResearcherTM temperatures were averaged for each of the five regions deemed to correspond to each of the five heater groups on the FPGA. A simple convective cooling setup where a fan was used to apply forced convection flow at between 2 (m/s) and 8 (m/s).

One of the problems with the use of any thermal camera for data acquisition is the need to calibrate the device for the particular setup. In particular, the conversion of signal intensity into a temperature measurement is based upon a number of factors. Many of these can be determined automatically by the camera (lens temperature for example). However, it is still necessary to provide the refractive index of the chip surface material. Since the StratixTM II FPGA is a flip-chip design, we characterize the surface to be similar to that of bulk silicon. The refractive index of the chip surface was therefore estimated to be equal to that of pure silicon (3.426 @ 5um).

Despite the successful acquisition of temperature data from the Stratix IITM FPGA, several elements to the data collection have necessitated that this portion of the thermal verification be left as future work. There are three such reasons.

First, reliable estimation of the static and dynamic power utilization of the device has been inadequate. Quartus was used for purpose of predicting a first-order estimation of the power utilization. However, such estimations have been determined to be inadequate.

Second, despite the apparent location of various heat sources, viewable by manual inspection of the thermal data taken from the thermal camera, the actual location of

such heat sources may not necessarily coincide with the specific regions of temperature increase. To know the specific location of each heater necessitates further analysis.

Third, specific knowledge about the material layers used for the Stratix IITM FPGA requires further investigation. While Sesctherm has been designed for the purpose of predicting the temperature behavior of a range of different devices, any validation of the Sesctherm model from empirical data requires that each sub-component of the model coincide with the real-world system it is validated against. It is for all these reasons that a validation of the Sesctherm thermal infrastructure against a Stratix IITM FPGA is left as future work.

Part IV

Conclusion and Related Work

Chapter 11

Conclusion

In order to evaluate the importance of accurate thermal modeling, a novel temperature modeling framework has been described, called Sesctherm. This thermal modeling framework employs the use of state-of-the-art thermal modeling strategies to further improve the accuracy of the thermal characterization of modern semiconductor devices. Using this modeling framework, designers are given critical new insight into the thermal consequences of their design decisions.

Unlike other models, which require detailed knowledge of the device being modeled, Sesctherm uses automated material synthesis sub-models for the purpose of providing a reasonable prediction for the thermal behavior for a design that is not yet complete. This means that designers are able to gain sufficient insight into the thermal behavior of the design without necessitating that the actual design be fully realized. It is through the ability of the model to perform these early-design-cycle predictions that critical design decisions may be made sufficiently early in the design cycle so as to avoid

thermal run-away problems or to avoid a design that exceeds its thermal budget.

Each of the components to this thermal modeling infrastructure has been described in detail. These sub-elements of the model include the various materials models and heat transfer models. It is one of the strengths of the Sesctherm modeling infrastructure that the model may be easily extended to model new materials, components, and modes for heat transfer.

To validate the accuracy of its thermal predictions, Sesctherm was validated against both empirical data taken from a Delphi thermal test die and Flomerics FlothermTM thermal model. We showed that the temperature response of the Delphi test die matched the data from Sesctherm reasonably well, although there was still room for improvement. In particular, higher-frequency components of the thermal trace obtained from the empirical data were not adequately captured in the Sesctherm trace. However, we also showed that the higher frequency components of the temperature trace were also not consistent with the standard resistance-capacitance-based electrothermal models that have become the standard. We hypothesize that future models may need to address this apparent discrepancy, and this is left as future work.

We further showed that Sesctherm matched the output of the FlothermTM thermal model excellently. The improvement of Sesctherm for the purpose of further improving its accuracy is considered future work. This includes the validation of Sesctherm against an Altera Stratix IITM FPGA as previously described.

Once validated, Sesctherm was used to explore the thermal effect of neglecting to model several elements of a semiconductor device. This included the thermal con-

sequences of neglecting to model the system main-board, device package, interconnect density distribution, Silicon-On-Insulator technology, and detailed convection cooling model. It has been shown that neglecting to model these elements can have dramatic consequences.

It has been shown that any a-priori predictions in the absence of detailed modeling may be of limited value, as complex thermal systems like those described here sometimes behave in quite non-intuitive ways. In particular, it was shown that the inclusion of a system package actually reduced the temperature through an increase in the resistance-capacitance of the thermal system as well as an increase in the surface area for convective cooling. Further, it has been shown that seemingly insignificant elements of the thermal system may actually have significant thermal consequences. This was especially apparent in the analysis of the significance of modeling the interconnect density distribution.

While all the metal interconnects in a given design are combined less than one tenth of one percent of the thickness of the materials stack, the high thermal conductivity of the metal makes it an ideal means to normalize the temperature distribution across the die. Validated against empirical data taken from a FLIR thermal camera, it has been shown that despite the apparently insignificant thickness of the interconnect layers, collectively they may actually be a critical tool in the strategic removal of hotspots across the chip. Acting like a heat-speader, the clock interconnect distribution across the chip takes heat from hot regions of the chip and deposits that heat to cooler regions. This is even more important for Silicon-On-Insulator devices where the “buried-oxide”

and “field-oxide” electrical isolation under and beside the transistor devices limits the potential of the devices to conduct heat rapidly through the bulk silicon substrate. This “self-heating” effect is such that the high thermal conductivity of the tungsten gate, source, and drain electrodes is more readily able to remove heat to the interconnect layers, where copper interconnect is able to deposit that heat readily to cooler regions of the chip.

In summary, there is no substitute for a detailed thermal analysis to justify simplifying the thermal model for a semiconductor device. Further, new technologies, including Silicon-On-Insulator technology, pose new challenges for reliable thermal characterization, and simplifications to thermal models that neglect to accurately model these new technologies may dramatically reduce the validity of any conclusions drawn from such models. There is no “free lunch”. When modeling unreliable and complex thermal systems of the kind described here, care must be taken to thoroughly investigate the different components of the thermal system – even those that may seem comparatively insignificant.

Chapter 12

Related Work

There are a variety of thermal models that have already been developed. These include HotSpot by Skadron et al [115], and Illiads-T [18]. It is not the claim of this thesis to compare Sesctherm to these models. Rather, Sesctherm was developed for the purpose of exploring questions regarding the need to accurately model various modern technologies that are not currently modeled using these other software packages as of the time of this writing. This includes Silicon-On-Insulator technology characterization.

This work borrows from many other sources in the development of various material sub-models. The statistical interconnect distribution was determined following the work of Davis et al. [40, 41] and others [10, 16, 53, 81, 101, 131]. The main-board model was developed following the work of Graebner et al. [51]. The package model was developed following the work of Ramakrishna et al. [94] and others [5, 33, 64, 65, 71, 92, 110]. The Silicon-On-Insulator model was based, in part, on the work of Lin et al. [70] and others [121]. However, the bulk of the Silicon-On-Insulator model was

based upon CMOS SOI, US Patent 6,975,003 [77].

Although a variety of other thermal models have been built, this work is not focused on an improvement to existing models. Rather, it is intended to highlight the need for more accurate thermal modeling –regardless of the model used. As such, the work here may be considered unique in that it is the first known study to include a robust validation of a thermal infrastructure using empirical data that is coupled with a detailed analysis for the modeling of new thermal features, including system-level modeling of Silicon-On-Insulator technology, interconnect density variation, package modeling, forced convection modeling, and main-board modeling.

Appendix A

Technology Parameters

Table A.1: Technology Parameters Summary

Technology(nm)	250	180	130	90	65
6-TSRAMCellSize(nm ^ 2)	4643	3083	2000	1000	570
Vdd(V)	2	1.8	1.5	1.057	0.884
GateLength(nm)(averagesizenmos/pmos)	500	360	260	180	130
GateWidth(nm)(averagesizenmos)	11440	824	596	414	300
GateWidth(nm)(averagesizepmos)	5720	412	298	207	150
Leff(nm)	160	100	70	46.571	29.844
tox(Angstroms)	60	45	35	24.472	18.7260
MetalLayers	6	6	7	8	9
k_ild	5.81	4.53	3.6	2.9	2.4
M1Height(nm)	298	217	160	140	90
M1Width(nm)	502	395	319	260	220
M1Spacing(nm)	502	395	319	260	220
M1Resistance(nm)	1589.688171	1547.624512	393.9827542	688.7825641	839.7005831

Continued on next page

Technology(nm)	250	180	130	90	65
M1Capacitance	0.140922039	0.275407057	0.317581512	0.323601485	0.327612261
M1Sopt	4.564777016	2.922899361	6.107996587	4.34055825	3.722697363
M1Thickness(nm)	322	235	97	72	30
M1ViaSpace(nm)	400	260	140	100	70
M1Height(nm)	389	304	280	150	170
M1Width(nm)	445	353	293	220	210
M1Spacing(nm)	445	353	293	220	210
M1Resistance(nm)	1540.715952	1500.414608	384.6548897	669.1671877	682.068109
M1Capacitance	0.14493629	0.279517033	0.319996725	0.325661893	0.329137069
M1Sopt	4.572093864	2.946621908	6.158239884	4.389763505	4.120953955
M1Thickness(nm)	434	329	169	77	57
M1ViaSpace(nm)	299	186	64	63	63
M2Height(nm)	467	378	360	256	190
M2Width(nm)	760	560	425	320	210
M2Spacing(nm)	760	560	425	320	210

Continued on next page

Technology(nm)	250	180	130	90	65
M2Resistance(nm)	1540.715952	1500.414608	384.6548897	669.1671877	682.068109
M2Capacitance	0.14493629	0.279517033	0.319996725	0.325661893	0.329137069
M2Sopt	4.572093864	2.946621908	6.158239884	4.389763505	4.120953955
M2Thickness(nm)	521	409	217	131	64
M2ViaSpace(nm)	1498	968	442	196	63
M3Height(nm)	460	375	360	256	200
M3Width(nm)	743	552	425	320	220
M3Spacing(nm)	743	552	425	320	220
M3Resistance(nm)	107	107	188	414.5524582	627.9467305
M3Capacitance	0.202	0.333	0.336	0.335053232	0.335761407
M3Sopt	14.69594182	10.10927913	8.596396413	5.49851306	4.252293599
M3Thickness(nm)	513	406	217	131	67
M3ViaSpace(nm)	1373	908	442	196	70
M4Height(nm)	766	592	570	320	250
M4Width(nm)	1368	961	718	400	280

Continued on next page

Technology(nm)	250	180	130	90	65
M4Spacing(nm)	1368	961	718	400	280
M4Resistance(nm)	107	107	188	414.5524582	627.9467305
M4Capacitance	0.202	0.333	0.336	0.335053232	0.335761407
M4Sopt	14.69594182	10.10927913	8.596396413	5.49851306	4.252293599
M4Thickness(nm)	854	640	344	164	84
M4ViaSpace(nm)	33628	23606	10573	482	136
M5Height(nm)	1271	935	900	384	300
M5Width(nm)	2167	1470	1064	480	300
M5Spacing(nm)	2167	1470	1064	480	330
M5Resistance(nm)	161.2217667	160.5662844	68.29904873	83.2515535	187.3168749
M5Capacitance	0.193670237	0.325685993	0.346020375	0.347706972	0.348226762
M5Sopt	12.22705083	8.344637493	14.0542228	12.04450737	7.645053143
M5Thickness(nm)	1416	1012	543	197	101
M5ViaSpace(nm)	2006481	1361111	449548	1184	238
M6Height(nm)	0	0	1200	576	430

Continued on next page

Technology(nm)	250	180	130	90	65
M6Width(nm)	0	0	1143	720	480
M6Spacing(nm)	0	0	1143	720	480
M6Resistance(nm)	0	0	68.29904873	83.2515535	187.3168749
M6Capacitance	0	0	0.346020375	0.347706972	0.348226762
M6Sopt	0	0	14.0542228	12.04450737	7.645053143
M6Thickness(nm)	0	0	724	295	145
M6ViaSpace(nm)	0	0	10583333	17535	1262
M7Height(nm)	0	0	0	972	650
M7Width(nm)	0	0	0	1080	720
M7Spacing(nm)	0	0	0	1080	720
M7Resistance(nm)	0	0	0	4.687560857	18.20896974
M7Capacitance	0	0	0	0.357893674	0.358988515
M7Sopt	0	0	0	50.03126038	24.1499628
M7Thickness(nm)	0	0	0	498	219
M7ViaSpace(nm)	0	0	0	1000000e-9	219

Continued on next page

Technology(nm)	250	180	130	90	65
M8Height(nm)	0	0	0	0	975
M8Width(nm)	0	0	0	0	1080
M8Spacing(nm)	0	0	0	0	1080
M8Resistance(nm)	0	0	0	0	18.20896974
M8Capacitance	0	0	0	0	0.3558988515
M8Sopt	0	0	0	0	24.14999628
M8Thickness(nm)	0	0	0	0	329
M8ViaSpace(nm)	0	0	0	0	1000000

Table A.2: Material Properties Taken From Structural Analysis Reports

Product	OMAP 1710	S5K3AAE03	SKY74663	AMD-K6	Pentium II	MPA1016PN	MPC750	XG4036XL-1C	EPM7128
Company	TI	Samsung	Skyworks	AMD	Intel	Motorola	IBM/Motorola	Xilinx	Altera
Year	2004 [24]	2004 [27]	2003 [28]	1997 [19]	1997 [22]	1997 [23]	1997 [21]	1997 [25]	1997 [20]
Package Type	289 Ball BGA	Plastic lensed (QFP)	CPGA	540-pin BGA	84-pin PLCC	360-pin BGA	unknown	160-pin PQFP	
Die Length(nm)	5,92	6,53	4,02	10,30	13,30	6,10	7,80	?	5,00
Die Width(nm)	6,19	6,74	5,10	15,60	14,60	6,20	9,00	?	8,60
Die Area(nm ²)	36,6	44	20,5	161	195	38	70,7	?	43
Process Type	CMOS	CMOS	BiCMOS	CMOS	CMOS	CMOS	CMOS	CMOS	CMOS
Num Metal Layers	6	4	3	6	4	3	6	3	2
Min Transistor Gate Length (nm)	1	1	2	1	1	1	1	1	1
Process Generation (nm)	90	180	170	330	320	250	500	300	550
Isolation	STI	LOCOS	STI	STI	LOCOS	STI	LOCOS	LOCOS	LOCOS
PolySilicon	Polycide	Polycide	Polycide	Polycide	Polycide	Polycide	Polysilicon	Polysilicon	Polysilicon
Substrate	P-type	P-epi/P-type	P-type	P-epi/P-type	P-epi/P-type	P-epi/P-type	P-type	P-type	P-type
Epitaxial Thickness (nm)	0	3,2	0	7	1,6	0	1,7	0	0
N+ S/D diffusion	80	160	190	150	200	250	150	200	150
P+ S/D diffusion	60	150	190	130	250	250	130	250	150
Nwell Depth (nm)	900	1300	1500	1500	800	2500	800	2500	2000
Pwell Depth (nm)	1300	1500	1500	1500	800	2500	800	2500	1500
Chip Thickness (um)	280	700	700	700	500	500	500	380	400
Substrate Thickness (um)	274,185	691,96	691,258	681	491,395	493,75	485,66	372,25	392,5
Substrate Thickness (% of chip)	97,92	98,85	98,75	97,29	98,28	98,75	97,13	97,96	98,13
PMD-1	SiOC	Oxide	TiN	SiO2	Glass 2	SiO2	SiO2	SiO2	SiO2
PMD-1 Thickness (nm)	270	1300	600	130	400	550	450	1500	1500
PMD-2	SiOCN	PSG	-	-	SiO2	-	-	-	-
PMD-2 Thickness(nm)	50	230	-	-	500	-	-	-	-
PMD-3	FSG	Nitride	-	-	-	-	-	-	-
PMD-3 Thickness(nm)	570	30	-	-	-	-	-	-	-
PMD-4	SiN	-	-	-	-	-	-	-	-
PMD-4 Thickness(nm)	20	-	-	-	-	-	-	-	-
Trench Isolation Thickness	347	440	310	450	400	400	400	350	400
Trench Isolation Width	194	290	700	300	280	340	340	250	300
Poly1/2-1 Material(Top)	CoSi2	PolySilicon	Silicide	Silicide	Silicide	Silicide	Silicide	PolySilicon	Silicide
Poly1/2-1 Thickness(Top)(nm)	50	167	50	70	150	30	150	250	100
Poly1/2-2 Material	PolySilicon	TiSi2	PolySilicon	PolySilicon	PolySilicon	PolySilicon	PolySilicon	-	PolySilicon
Poly1/2-2 Thickness(nm)	180	23	150	260	250	200	100	100	150
Poly1/2 Width(nm)	90	151	260	320	500	170	300	300	550
Poly1/2 Spacing(nm)	135	409	770	650	500	1000	450	550	800
Poly1/2 Pitch(nm)	125	409	560	1030	970	1500	620	850	1350
Poly1/2 Thickness(nm)	250	230	190	210	340	350	130	250	250
Poly1/2 Contact Width(nm)	150	280	380	-	500	800	-	W	W
Poly1/2 Contact Spacing(nm)	150	220	430	-	400	700	-	500	900
Poly1/2 Contact Pitch(nm)	300	500	820	-	900	1500	-	1000	1200
Poly1/2 Contact Thickness(nm)	388	455	650	-	700	400	-	450	450
M1 Metal1 Material (Top)	TaN	TiN	TiN	TiN	TiN	TiN	TiN	TiN	TiN
M1-1 Thickness('Top)(nm)	110	90	63	120	50	50	50	50	150
M1-2 Material	Ta	Al	TiAl	W	Al	Al	W	Al	Al
M1-2 Thickness(nm)	9	300	16	400	500	550	450	500	500
M1-3 Material	Cu	Ti	Al	Ti	TiN	-	-	-	-
M1-3 Thickness(nm)	277	40	438	55	-	170	-	-	-
M1-4 Material	-	-	TiN	-	-	-	-	-	-
M1-4 Thickness(nm)	-	-	47	-	-	-	-	-	-
M1-5 Material	-	-	Ti	-	-	-	-	-	-
M1-5 Thickness(nm)	-	-	16	-	-	-	-	-	-
M1 Side Liner Thickness vs Top	0,5	0,5	0	0,5	0,5	0,5	0,5	0,5	0,6
M1 Width(nm)	200	370	550	450	400	600	450	500	800
M1 Thickness(nm)	297	420	650	575	600	720	500	550	650
M1 Pitch(nm)	310	710	1000	900	1000	1400	900	1000	1600
M1 Spacing(nm)	110	340	450	450	500	800	400	450	800

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Product	OMAP 1710	S5K3AAE03	SKY74963	AMD-K6	Pentium II	MPA1016FFN	MPC750	XC4036XL-1C	EPM7128
M1 ILD Material1 (Top)	SiOC	CVD Oxide	TiN	TiN	glass 3	glass 2	Glass 1	glass 2	Spin-on-glass
M1 ILD Material1 Thickness (nm)	190	620	1513	50	550	400	550	800	150
M1 ILD Material2	SiOCN	HDP Oxide	-	SiO2	SiO2	spin-on-glass	-	glass 1	SiO2
M1 ILD Material2 Thickness (nm)	50	483	-	650	250	-	-	100	1350
M1 ILD Material3	SiO2	ARC	-	-	glass 1	glass 1	-	-	-
M1 ILD Material3 Thickness (nm)	40	69	-	-	100	400	-	-	-
M1 ILD Material4	SiOC	-	-	-	-	-	-	-	-
M1 ILD Material4 Thickness (nm)	190	-	-	-	-	-	-	-	-
M1 ILD Material5	SiOCN	-	-	-	-	-	-	-	-
M1 ILD Material5 Thickness (nm)	50	-	-	-	-	-	-	-	-
M1 ILD Thickness Below (nm)	194	227.5	325	0 (damascene M1)	350	200	0	225	750
M1 ILD Thickness Above (nm)	150	307	416.5	350	350	300	400	450	750
M1 Via Material	Cu	Al	W	W	Al	W	W	W	W
M1 Via Width(nm)	150	250	500	600	500	600	500	500	1200
M1 Via Spacing(nm)	150	270	410	650	550	650	550	550	1000
M1 Via Pitch(nm)	300	520	910	1250	1050	1250	1050	1000	2200
M1 Via Thickness(nm)	300	614	833	700	700	600	800	900	1500
M2-1 Material(Top)	TaN	TiN	TiN	TiN	TiN	TiN	TiN	TiN	TiN
M2-1 Thickness(Top)(nm)	11	90	66	100	50	50	50	50	50
M2-2 Material	Ta	Al	TiAl	Al	Al	Al	Al	Al	Al
M2-2 Thickness(nm)	9	400	17	600	800	500	600	550	750
M2-3 Material	Cu	Ti	Al	-	-	-	-	-	-
M2-3 Thickness(nm)	277	40	460	-	-	100	-	-	-
M2-4 Material	-	-	TiN	-	-	-	-	-	-
M2-4 Thickness(nm)	-	-	49	-	-	-	-	-	-
M2-5 Material	-	-	Ti	-	-	-	-	-	-
M2-5 Thickness(nm)	-	-	17	-	-	-	-	-	-
M2 Width(nm)	190	230	810	900	550	900	450	550	800
M2 Thickness(nm)	297	530	680	700	850	650	650	600	800
M2 Pitch(nm)	320	720	1400	1400	1050	2100	900	1150	1600
M2 Spacing(nm)	130	490	590	500	500	1200	450	600	800
M2 ILD Material1 (Top)	SiOC	CVD Oxide	TiN	Glass 2	glass 3	glass 2	glass 2	glass 2	-
M2 ILD Material1 Thickness (nm)	190	966	4229	1400	850	400	850	800	-
M2 ILD Material2	SiOCN	-	Glass 1	TiO2	spin-on-glass	glass 1	glass 1	glass 1	-
M2 ILD Material2 Thickness (nm)	50	-	100	350	400	350	550	100	-
M2 ILD Material3	SiO2	-	-	-	-	-	-	-	-
M2 ILD Material3 Thickness (nm)	60	-	-	-	-	-	-	-	-
M2 ILD Material4	SiOC	-	-	-	-	-	-	-	-
M2 ILD Material4 Thickness (nm)	200	-	-	-	-	-	-	-	-
M2 ILD Material5	SiOCN	-	-	-	-	-	-	-	-
M2 ILD Material5 Thickness (nm)	60	-	-	-	-	-	-	-	-
M2 ILD Material6	SiO2	-	-	-	-	-	-	-	-
M2 ILD Material6 Thickness (nm)	60	-	-	-	-	-	-	-	-
M2 ILD Material7	SiOC	-	-	-	-	-	-	-	-
M2 ILD Material7 Thickness (nm)	200	-	-	-	-	-	-	-	-
M2 ILD Material8	SiOCN	-	-	-	-	-	-	-	-
M2 ILD Material8 Thickness (nm)	60	-	-	-	-	-	-	-	-
M2 ILD Thickness Below (nm)	150	307	416.5	350	350	300	400	450	750
M2 ILD Thickness Above (nm)	135	231	365	600	350	600	600	450	-
M2 Via Material	Cu	Al	W	W	Al	W	W	W	-
M2 Via Width(nm)	150	290	500	550	600	700	700	500	-
M2 Via Spacing(nm)	150	230	410	530	640	640	750	500	-
M2 Via Pitch(nm)	300	520	910	1080	1240	1240	1450	1000	-
M2 Via Thickness(nm)	270	462	729	700	700	1200	1200	900	-
M2-1 Material(Top)	TaN	TiN	TiN	TiN	TiN	TiN	TiN	TiN	TiN
M2-1 Thickness(Top)(nm)	11	70	84	100	50	50	50	50	50
M2-2 Material	Ta	Al	Al	Al	Al	Al	Al	Al	Al
M2-2 Thickness(nm)	9	430	3334	800	750	800	800	850	-
M2-3 Material	Cu	Al	TiN	-	-	-	-	-	-
M2-3 Thickness(nm)	277	40	83	-	-	120	-	-	-
M3 Width(nm)	297	290	3100	750	600	1000	550	650	-
M3 Thickness(nm)	297	540	3500	900	800	970	850	900	-
M3 Pitch(nm)	300	580	6200	1250	1150	2200	1350	1200	-
M3 Spacing(nm)	110	290	3100	500	550	1200	500	550	-
M3 ILD Material1 (Top)	SiOC	CVD Oxide	-	glass 2	glass 3	glass 2	glass 2	-	-
M3 ILD Material1 Thickness (nm)	190	972	-	1500	925	-	625	-	-
M3 ILD Material2	SiOCN	-	-	SiO2	-	glass 1	-	-	-
M3 ILD Material2 Thickness (nm)	50	-	-	80	400	-	725	-	-

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Product	OMAP 1710	S5K3AAE03	SKY74963	AMD-K6	Pentium II	MPA1016FFN	MPC750	XCC4036XL-1C	EPM7128
M3 ILD Material3	SiO2	-	-	-	glass 1	-	-	-	-
M3 ILD Material3 Thickness (nm)	60	-	-	-	100	-	-	-	-
M3 ILD Material3 SiOC	-	-	-	-	-	-	-	-	-
M3 ILD Material3 Thickness (nm)	210	-	-	-	-	-	-	-	-
M3 ILD Material3 SiOCN	-	-	-	-	-	-	-	-	-
M3 ILD Material3 Thickness (nm)	50	-	-	-	-	-	-	-	-
M3 ILD Thickness Below (nm)	135	-	365	600	350	600	600	-	450
M3 ILD Thickness Above (nm)	135	250	-	600	350	-	-	-	-
M3 Via Material	Cu	A1	-	W	W	-	-	-	-
M3 Via Width(nm)	140	300	-	550	600	650	-	-	-
M3 Via Spacing(nm)	160	350	-	600	650	680	-	-	-
M3 Via Pitch(nm)	300	650	-	1150	1250	1330	-	-	-
M3 Via Thickness(nm)	270	500	-	1200	700	1100	-	-	-
M4-1 Material(Top)	TaN	TiN	-	Al	TiN	-	-	-	-
M4-1 Thickness(Top)(nm)	11	40	-	100	1700	-	-	-	-
M4-2 Material	Ta	A1	-	Al	-	-	-	-	-
M4-2 Thickness(nm)	9	820	-	750	-	-	-	-	-
M4-3 Material	Cu	TiN	-	-	-	-	-	-	-
M4-3 Thickness(nm)	277	80	-	-	-	-	-	-	-
M4-4 Material	-	Ti	-	-	-	-	-	-	-
M4-4 Thickness(nm)	-	30	-	-	-	-	-	-	-
M4 Width(nm)	170	560	-	750	1600	-	-	-	-
M4 Thickness(nm)	297	970	-	850	1700	-	-	-	-
M4 Pitch(nm)	300	1000	-	1250	2700	-	-	-	-
M4 Spacing(nm)	130	440	-	500	1100	-	-	-	-
M4 ILD Material1 (Top)	FSG	-	-	-	glass 2	-	-	-	-
M4 ILD Material1 Thickness (nm)	220	-	-	1300	-	-	-	-	-
M4 ILD Material2	SiN	-	-	glass 1	-	-	-	-	-
M4 ILD Material2 Thickness (nm)	50	-	-	100	-	-	-	-	-
M4 ILD Material3	FSG	-	-	-	-	-	-	-	-
M4 ILD Material3 Thickness (nm)	360	-	-	-	-	-	-	-	-
M4 ILD Material4	SiOCN	-	-	-	-	-	-	-	-
M4 ILD Material4 Thickness (nm)	40	-	-	-	-	-	-	-	-
M4 ILD Material5	-	-	-	-	-	-	-	-	-
M4 ILD Material5 Thickness (nm)	-	-	-	-	-	-	-	-	-
M4 ILD Thickness Below (nm)	135	250	-	600	350	-	-	-	-
M4 ILD Thickness Above (nm)	147	-	-	500	-	-	-	-	-
M4 Via Material	Cu	-	-	W	W	-	-	-	-
M4 Via Width(nm)	180	-	-	550	-	-	-	-	-
M4 Via Spacing(nm)	120	-	-	580	-	-	-	-	-
M4 Via Pitch(nm)	300	-	-	1130	-	-	-	-	-
M4 Via Thickness(nm)	294	-	-	1200	-	-	-	-	-
M5-1 Material(Top)	TaN	-	-	TiN	-	-	-	-	-
M5-1 Material Thickness(Top)(nm)	13	-	-	60	-	-	-	-	-
M5-2 Material	Ta	-	-	Al	-	-	-	-	-
M5-2 Material Thickness(nm)	10	-	-	800	-	-	-	-	-
M5-3 Material	Cu	-	-	-	-	-	-	-	-
M5-3 Material Thickness(nm)	317	-	-	-	-	-	-	-	-
M5 Width(nm)	140	-	-	900	-	-	-	-	-
M5 Thickness(nm)	340	-	-	860	-	-	-	-	-
M5 Pitch(nm)	300	-	-	1700	-	-	-	-	-
M5 Spacing(nm)	160	-	-	800	-	-	-	-	-
M5 ILD Material1 (Top)	SiON	-	-	glass 2	-	-	-	-	-
M5 ILD Material1 Thickness (nm)	280	-	-	900	-	-	-	-	-
M5 ILD Material2	SiO2	-	-	glass 1	-	-	-	-	-
M5 ILD Material2 Thickness (nm)	400	-	-	200	-	-	-	-	-
M5 ILD Material3	SiN	-	-	-	-	-	-	-	-
M5 ILD Material3 Thickness (nm)	50	-	-	-	-	-	-	-	-
M5 ILD Material3	-	-	-	-	-	-	-	-	-
M5 ILD Material3 Thickness (nm)	-	-	-	-	-	-	-	-	-
M5 ILD Material3 Thickness (nm)	-	-	-	-	-	-	-	-	-

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Product	OMAP 1710	S5K3AAE03	SKY74963	AMD-K6	Pentium II	MPA1016FFN	MPC750	XCC4036XL-1C	EPM7128
M5 ILD Thickness Below (nm)	147	-	-	500	-	-	600	-	-
M5 ILD Thickness Above (nm)	353	-	-	550	-	-	600	-	-
M5 Via Material	Cu	-	-	W	-	-	W	-	-
M5 Via Width(nm)	3100	-	-	1400	-	-	1200	-	-
M5 Via Spacing(nm)	3100	-	-	1400	-	-	1400	-	-
M5 Via Pitch(nm)	6200	-	-	2800	-	-	2600	-	-
M5 Via Thickness(nm)	706	-	-	1000	-	-	1200	-	-
M6-1 Material(Top)	Al	-	-	Al	-	-	TiN	-	-
M6-1 Thickness(Top)(nm)	1340	-	-	2100	-	-	40	-	-
M6-2 Material	TiN	-	-	-	-	-	Al	-	-
M6-2 Thickness(nm)	60	-	-	-	-	-	1900	-	-
M6-3 Material	-	-	-	-	-	-	-	-	-
M6-3 Thickness(nm)	-	-	-	-	-	-	-	-	-
M6 Width(nm)	5800	-	-	3000	-	-	2000	-	-
M6 Thickness(nm)	1400	-	-	2100	-	-	1940	-	-
M6 Pitch(nm)	11600	-	-	5300	-	-	3700	-	-
M6 Spacing(nm)	5800	-	-	2300	-	-	1700	-	-
M6 ILD Thickness Below (nm)	353	-	-	550	-	-	600	-	-
Passivation Material	SiON	-	Nitride	SiON	SiON	SiON	SiN	SiN	SiN/SiO2
Passivation Thickness	320	-	1400	1600	700	1000	800	950	700/350

Appendix B

Material Thermal Properties

Table B.1: Thermal Properties of Materials Used

Material	Material Type	Typical Material Usage	Conductivity (W/mK)	Specific Heat (J/kg·K)	Density (kg/m ³)	Reference
AlN	Conductor	CMP Material	180.00	740.00	3260.00	[33, 54, 128]
Alumina, 96% Al ₂ O ₃	Insulator	Interlayer-Dielectric	25.00	880.00	3800.00	[33, 54, 128]
Aluminum(Al)	Conductor	Interconnect Metal	237.00	910.00	2702.00	[33, 54, 128]
Bismaleimide-triazine (BT) laminate	Insulator	Package PCB Layers	0.19	1400.00	1300.00	[33, 54, 128]
Copper	Conductor	Interconnect Metal	380.76	376.56	8938.30	[33, 54, 128]
Diamond	Thermal Conductor	Heat Conduction	2000.00	472.00	3520.00	[33, 54, 128]
Boron Fiber Epoxy	Insulator	Package Substrate Layers	0.61	1359.80	2499.52	[33, 54, 128]
Graphite Fiber Epoxy	Insulator	Package Substrate Layers	5.70	709	2210	[55]
Fiberglass	Insulator	Inter-layer Dielectric	0.29	836.80	1799.19	[33, 54, 128]
FR-4 Epoxy Fiberglass laminate	Insulator	Package/ Main-board PCB Layers	0.8(x,y); 0.3(z)	1150.00	1800.00	[33, 54, 128]
G10 epoxy Fiberglass laminate	Insulator	Package substrate Layers	0.29	800.00	2000.00	[33, 54, 128]
Glass/pyrex	Insulator	Interlayer-Dielectric	1.02	837.00	2230.00	[33, 54, 128]
Gold	Conductor	Package Contact	294.22	125.52	19270.21	[33, 54, 128]
IR glass	Insulator	Interlayer-Dielectric	0.22	276.14	4677.87	[33, 54, 128]
Plastic package mold compounds	Insulator	Package Encapsulant	0.09	800.00	1900.00	[33, 54, 128]
Polyimide	Insulator	Gate Dielectric	0.49	1420.00	1820.00	[33, 54, 128, 78]
Sapphire Aluminum Oxide (Al ₂ O ₃)	Thermal Conductor	Heat Conduction	25.20	761.00	3980.00	[33, 54, 128]
Silicon @ 20C	Semiconductor	Chip Substrate	150.05	794.96	2330.69	[33, 54, 128]
Silicon, Lightly Doped Thin Film	Semiconductor	Chip Substrate	50.00	770.00	2250	[76]
Silicon, Heavily Doped Thin Film	Semiconductor	Chip Substrate	10.00	760.00	2210	[76]
SiN	Conductor	CMP Material	27.00	691.00	2300.00	[33, 54, 128]
SiO ₂ (96%)	Insulator	Interlayer-Dielectric	1.38	750.00	2180.00	[33, 54, 128]
Solder (63%Sn/37%Pb)	Conductor	Solder	51.23	167.36	8858.21	[33, 54, 128]
Spun-on-Glass (SOG) Fiber	Insulator	Interlayer-Dielectric	1.45	737.00	2460.00	[33, 54, 128]
Titanium (Ti)	Conductor	CMP Material	22.00	502.08	4429.10	[33, 54, 128]
Titanium Nitride (TiN)	Conductor	CMP Material	19.00	627.00	5220.00	[33, 54, 128]
Tungsten (W)	Conductor	Interconnect Metal	161.65	133.89	19300.64	[33, 54, 128]
W/Cu(90%W/10 Cu)	Conductor	Interconnect Metal	209.42	163.18	17000.39	[33, 54, 128]

Table B.2: Temperature-Dependent Material Properties

Material	Conductivity (W/mK)	Specific Heat (J/kg·K)	Reference
Aluminum	$0.701(\frac{T}{100})^4 - 13.72(\frac{T}{100})^3 + 92.695(\frac{T}{100})^2 - 254.59(\frac{T}{100}) + 476.37$	$-1.7671(\frac{T}{100})^4 + 37.128(\frac{T}{100})^3 - 276.61(\frac{T}{100})^2 + 907.65(\frac{T}{100}) - 183.51$	[55, 54]
Sapphire Al ₂ O ₃	$1.0669(\frac{T}{100})^4 - 26.502(\frac{T}{100})^3 + 230.82(\frac{T}{100})^2 - 829.33(\frac{T}{100}) + 1058.3$	$-0.2768(\frac{T}{100})^4 + 9.3125(\frac{T}{100})^3 - 119.23(\frac{T}{100})^2 + 713.5(\frac{T}{100}) - 531.43$	[55]
Polycrystalline Al ₂ O ₃	$0.0887(\frac{T}{100})^4 - 2.681(\frac{T}{100})^3 + 28.787(\frac{T}{100})^2 - 131.42(\frac{T}{100}) + 233.86$	$-0.2768(\frac{T}{100})^4 + 9.3125(\frac{T}{100})^3 - 119.23(\frac{T}{100})^2 + 713.5(\frac{T}{100}) - 531.43$	[55, 54]
Epoxy (Boron Fiber)	heat flow \parallel : $(7 \times 10^{-15})(\frac{T}{100})^3 - 0.0335(\frac{T}{100})^2 + 0.245(\frac{T}{100}) + 1.9$ heat flow \perp : $-0.0117(\frac{T}{100})^3 + 0.06(\frac{T}{100})^2 + 0.0217(\frac{T}{100}) + 0.3$	$-4.6667(\frac{T}{100})^3 + 14(\frac{T}{100})^2 + 383.67(\frac{T}{100}) - 29$	[55, 54]
Copper	$0.0841(\frac{T}{100})^4 - 2.4854(\frac{T}{100})^3 + 25.569(\frac{T}{100})^2 - 113.14(\frac{T}{100}) + 567.2$	$-0.3577(\frac{T}{100})^4 + 8.6185(\frac{T}{100})^3 - 72.482(\frac{T}{100})^2 + 260.41(\frac{T}{100}) + 57.031$	[55, 54]
Epoxy (Graphite Fiber)	heat flow \parallel : $0.0167(\frac{T}{100})^3 - 0.4(\frac{T}{100})^2 + 4.0833(\frac{T}{100}) + 2$ heat flow \perp : $0.0117(\frac{T}{100})^3 - 0.0855(\frac{T}{100})^2 + 0.3933(\frac{T}{100}) + 0.14$	$(4 \times 10^{-12})(\frac{T}{100})^3 - 6(\frac{T}{100})^2 + 323(\frac{T}{100}) + 20$	[55, 54]
SiO ₂	heat flow \perp : $36.22(\frac{T}{100}) - 1.087$	$2.625(\frac{T}{100})^3 - 49.125(\frac{T}{100})^2 + 386.75(\frac{T}{100}) - 44$	[55, 54]
Polysilicon	$-0.0004(\frac{T}{100})^4 + 0.0154(\frac{T}{100})^3 - 0.1663(\frac{T}{100})^2 + 0.8186(\frac{T}{100}) + 0.0323$	$-0.2566(\frac{T}{100})^4 + 8.9114(\frac{T}{100})^3 - 114.56(\frac{T}{100})^2 + 672.85(\frac{T}{100}) - 461.05$	[55, 54]
SiN	$0.0004(\frac{T}{100})^4 - 0.0213(\frac{T}{100})^3 + 0.4342(\frac{T}{100})^2 - 4.2632(\frac{T}{100}) + 25.363$	$(-2 \times 10^{-16})(\frac{T}{100})^4 + (9 \times 10^{-15})(\frac{T}{100})^3 - (3 \times 10^{-13})(\frac{T}{100})^2 + (\frac{T}{100}) - (2 \times 10^{-11})$	[55, 54]
Silicon	$\begin{cases} 1 < \left(\frac{T}{100}\right) < 3 \\ 3 = < \left(\frac{T}{100}\right) < 15 \end{cases}$ $866.97(\frac{T}{100}) - 1.6394$ $0.0017(\frac{T}{100})^6 - 0.0928(\frac{T}{100})^5 + 2.0928(\frac{T}{100})^4$ $-24.504(\frac{T}{100})^3 + 158.41(\frac{T}{100})^2 - 550.172(\frac{T}{100}) + 887.86$	$-0.002(\frac{T}{100})^6 + 0.1105(\frac{T}{100})^5 - 2.5251(\frac{T}{100})^4$ $+29.984(\frac{T}{100})^3 - 197.35(\frac{T}{100})^2 + 714.06(\frac{T}{100}) - 285.3$	[55, 54]
Tungsten (W)	$(-8 \times 10^{-06})(\frac{T}{100})^6 + 0.0006(\frac{T}{100})^5 - 0.0158(\frac{T}{100})^4$ $+0.1444(\frac{T}{100})^3 + 0.6519(\frac{T}{100})^2 - 21.413(\frac{T}{100}) + 227.81$	$(-4 \times 10^{-05})(\frac{T}{100})^6 + 0.0029(\frac{T}{100})^5 - 0.0948(\frac{T}{100})^4$ $+1.5481(\frac{T}{100})^3 - 13.295(\frac{T}{100})^2 + 58.104(\frac{T}{100}) + 40.153$	[55, 54]

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