MA65C22

PARALLEL INTERFACE/TIMER

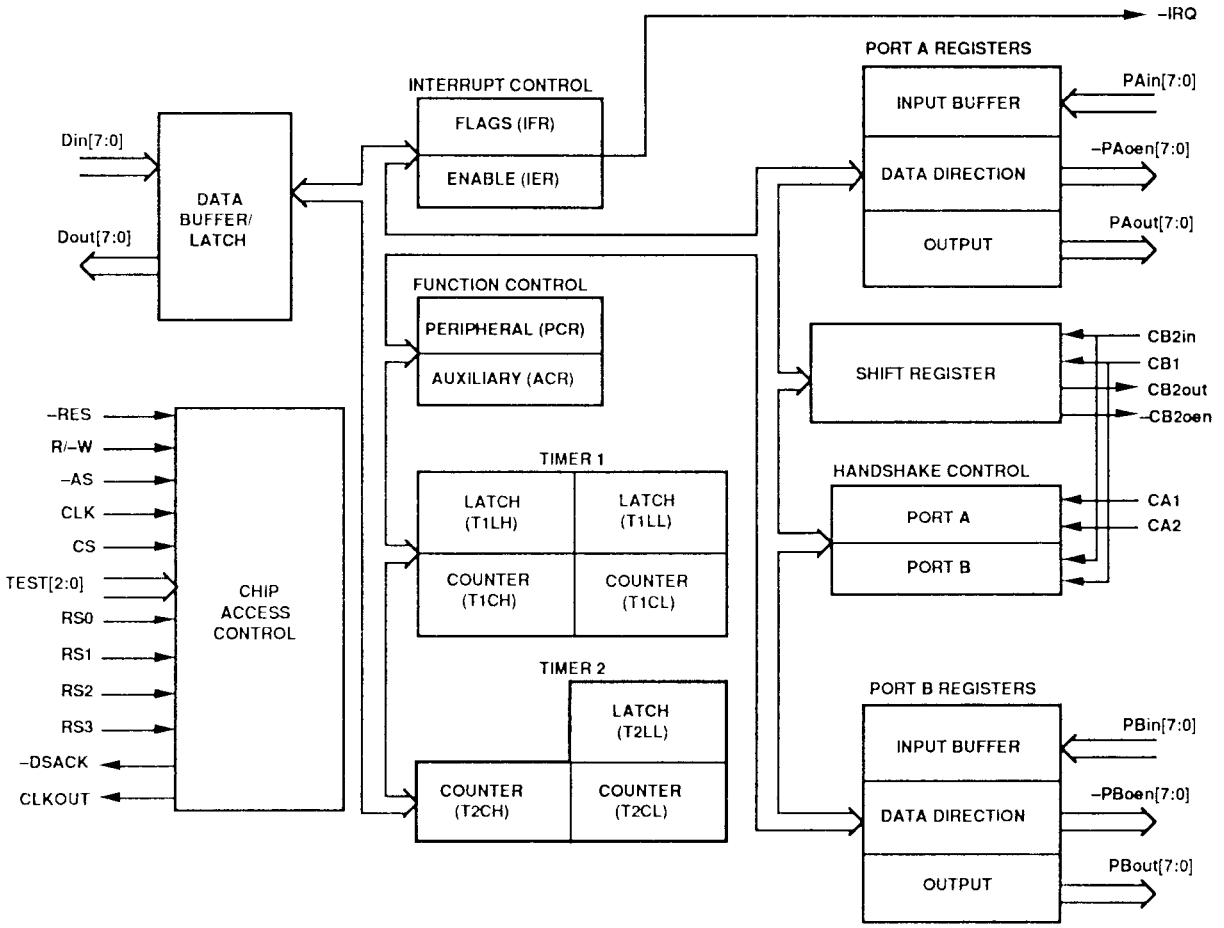
FEATURES

- Low-power CMOS
- Two 8-bit Bidirectional I/O Ports
- Two 16-bit Timer/Counters
- Serial Bidirectional Peripheral I/O Port
- Programmable Data Direction Registers

DESCRIPTION

The MA65C22 is a flexible Functional System Block (FSB) for use with the 68xxx family of processors. It includes functions for programmed control of up to two peripheral devices (Ports A and B). Two program-controlled 8-bit bidirectional peripheral I/O ports allow direct interfacing between the microprocessor and selected peripheral devices. Two programmable Data Direction Registers (A and B) allow selection of data direction (input versus output) on an individual line-by-line basis. Also provided are two programmable 16-bit counter/timers with latches. Timer 1 may be operated in a one-shot interrupt mode with interrupts on each count-to-zero, or in a free-running mode with a series of evenly spaced interrupts. Timer 2 functions as an interval counter and may be operated in a one-shot interrupt mode. Serial data transfers are provided by a shift register. Application versatility is further increased by various control registers, including an interrupt flag register, an interrupt enable register, and two function control registers.

BLOCK DIAGRAM



SIGNAL DESCRIPTIONS

Signal Name	Signal Description
-RES	A low reset input clears all internal registers to logic 0 (except T1 and T2 latches, counters, and shift register). This places all peripheral interface lines in the input state, disables the timers, shift register, and interrupts from the MA65C22.
CLK	Input clock used for internal synchronization.
R/-W	The direction of data transfer between the MA65C22 and the system processor is controlled by the R/-W and CS signals. When R/-W is low (write operation), and CS is active, data is transferred from the processor bus into the selected MA65C22 register. When R/-W is high (read), with CS active, data is transferred from the selected register to the CPU.
Din[7:0]	Data bus input lines.
Dout[7:0]	Data bus output lines.
CS	Chip select.
RS0, RS1, RS2, RS3	Address inputs to select one of the 16 internal registers.
-IRQ	Interrupt Request output that goes low whenever an internal interrupt flag is set and the corresponding interrupt enable bit is a logic 1.
PAin[7:0]	Port A input lines.
PAout[7:0]	Port A output lines.
-PAoen[7:0]	Port A direction control lines. Any of these 8 bits, when low, can be used to enable the corresponding output buffer.
PBin[7:0]	Port B input lines.
PBout[7:0]	Port B output lines.
-PBoen[7:0]	Port B direction control lines. Any of these 8 bits, when low, can be used to enable the corresponding output buffer.
CA1, CA2	Control Lines CA1 and CA2 serve as interrupt inputs for Peripheral Data Port A. Each line controls an internal Interrupt Flag with a corresponding Interrupt Enable bit.
-AS	Address Strobe input from the system.
CB1, CB2in, CB2out	Control lines CB1 and CB2in are interrupt inputs for Peripheral Data Port B. Like Port A, these two lines control an internal interrupt flag each with a corresponding interrupt enable bit. CB1, CB2in, CB2out lines also form a serial data port under the control of a shift register.
-CB2oen	This output control signal enables serial shifting out of data from CB2out.
TEST[2-0]	Test lines to configure the MA65C22 for normal operation or operation under test mode. These should be tied to 0 for normal operation.
-DSACK	Active low acknowledge output signal in response to -AS.
CLKOUT	Buffered output version of CLK.

FUNCTIONAL DESCRIPTION

PERIPHERAL DATA PORTS (PORT A, PORT B)

Each Peripheral Data Port operates in conjunction with a Data Direction Register (DDRA or DDRB). Under program control, the Data Direction Registers specify which lines within the port bus are to be designated as inputs or outputs. A Logic 0 in any bit position of the register will cause the corresponding line to be an input, while a Logic 1 will cause the line to be an output.

When a line is programmed as an output, it is controlled by a corresponding bit in the Output Register (on Port A or Port B). A Logic 1 in the Output Register will cause the corresponding output line to go high on PAout or PBout, while a Logic 0 will cause the line to go low. Under program control, data is written into the Output Register bit positions corresponding to the output lines that have been programmed as outputs. Should data be written into bit positions corresponding to lines that have been programmed as inputs, the output lines will be unaffected.

When reading a Peripheral Data Port, the values on lines (PAin or PBin) are transferred onto the Data Bus for lines defined as inputs, and the values output on PAout or PBout, for lines defined as outputs.

DATA TRANSFER - HANDSHAKE

The MA65C22 provides absolute control over data transfers between the microprocessor and peripheral devices. For Port A, CA1, and CA2 can be used as handshake/interrupt inputs. Typically, to accomplish a read or write handshake, the peripheral device generates a data ready signal on CA1 or CA2. In most cases, this will generate an interrupt to the microprocessor which will then read the data. Of the two signals, CA2 can be used as an independent interrupt. In other words, while CA1 can be used as a handshake signal (for Port A) only, CA2 can also be used as an independent interrupt input.

In Port B, CB1 and CB2in can be used as handshake/interrupt inputs, with CB2in capable of being used as an independent interrupt input.

INTERRUPT OPERATION

There are three basic operations, including: setting the flag within the Interrupt Flag Register (IFR), enabling the interrupt by way of a corresponding bit in the Interrupt Enable Register (IER), and signaling the microprocessor with an Interrupt Request (IRQ). An Interrupt Flag can be set by conditions internal to the FSB or by inputs from external sources. Normally, an Interrupt Flag remains set until the interrupt is serviced. To determine the source of an interrupt, the microprocessor must examine each flag in order, from highest to lowest priority. This is accomplished by reading the contents of the Interrupt Flag Register into the microprocessor accumulator, shifting the contents either left or right and then using conditional branch instructions to detect an active interrupt. Each Interrupt Flag has a corresponding Interrupt Enable bit in the Interrupt Enable Register. The enable bits are controlled by the microprocessor (set or reset). If an Interrupt Flag is high (Logic 1), and the corresponding Interrupt Enable bit is high (Logic 1), the Interrupt Request (IRQ) will go active low (Logic 0).

All Interrupt Flags are contained within a single Interrupt Flag Register. Bit 7 of this register will be high (Logic 1) whenever an Interrupt Flag is set, allowing convenient polling of several devices within a system to determine the source of the interrupt. (The Interrupt Flag Register (IFR) and Interrupt Enable Register (IER) format and operation is shown in Figures 20 and 21 respectively.)

The Interrupt Flag Register may be read directly by the microprocessor, and individual flag bits may be cleared by writing a "1" into the appropriate bit of the IFR. Bit 7 of the IFR indicates the status of the Interrupt Request (IRQ) output. Bit 7 corresponds to the following logic function: IRQ = IFR6 x IER6 + IFR5 x IER5 + IFR4 x IER4 + IFR3 x IER3 + IFR2 x IER2 + IFR1 x IER1 + IFR0 x IER0 (x = LogicAND, + = LogicOR).

Bit 7 is not a flag. For this reason, Bit 7 is not directly cleared by writing a "1" into its bit position. It can be cleared, however, by clearing all the flags within the register, or by disabling all active interrupts. Interrupts are enabled or disabled by writing into the interrupt enable register (IER). When writing into IER, if D7=0, then bits which are 1 between bit D6 and D0 will disable the corresponding interrupt.

If on the other hand, D7=1, then bits between D6 and D0 that are 1 will enable the corresponding interrupt.

TIMER OPERATION

Timer 1 Operation - Interval Timer T1 consists of two 8-bit latches and a 16-bit counter. The latches serve to store data that is to be loaded into the counter. Once the counter is loaded under program control, it decrements at a clock rate of CLK divided by 20. Upon reaching zero, an Interrupt Flag is set, causing Interrupt Request (IRQ) to go low (Logic 0) if the corresponding Interrupt Enable bit is set. Once the Timer reaches a count of zero, it will either disable any further interrupts (provided it has been programmed to do so), or it will automatically transfer the contents of the latches into the counter and proceed to decrement again. A control bit is provided in the Auxiliary Control Register (Bit 6) to allow selection of Timer 1 operating modes.

It should be noted that the microprocessor does not write directly into the low-order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low-order register when the microprocessor writes into the high-order register and counter. It may not be necessary to write to the low-order register in some applications, since the timing operation is triggered by writing to the high-order register and counter.

Timer 1 One-Shot Mode - Interval Timer T1 may operate in the One-Shot Mode which allows the generation of a single Interrupt Flag each time the Timer is loaded.

To generate a single interrupt, it is required that Bit 6 of the Auxiliary Control Register be low (Logic 0). The low-order T1 counter (T1C-L) or the low-order T1 latch (T1L-L) must then be loaded with the low-order count value. Note that a load to T1C-L is effectively a load to T1L-L. Next, the high-order count value must be loaded into the high-order T1 counter (T1C-H), at which time the value is simultaneously loaded into high-order T1 latch (T1L-H). During

FUNCTIONAL DESCRIPTION (Cont.)

this load sequence, the contents of T1L-L is transferred to T1C-L. The counter will start counting down at a rate of (CLK/20) from the time the counter is loaded. Once the T1 counter reaches a zero count, the Interrupt Flag is set. Once set, the T1 Interrupt Flag is reset by either loading T1C-H, which starts a new count, or by reading T1C-L.

Timer 1 Free-Run Mode - An important advantage within the MA65C22 is the ability of the latches associated with the T1 counter to provide a continuous series of evenly-spaced interrupts. It should also be noted that the continuous series of interrupts is not affected by variations in the microprocessor interrupt response time. These advantages are all produced in the Free-Run Mode. When operating in the Free-Run Mode, the Interrupt Flag is set each time the counter reaches a count of zero. In the Free-Run Mode, however, the counter does not continue to decrement after reaching a zero count. Instead, the counter automatically transfers the contents of the latch into the counter (16 bits) and then decrements from the new count value. As can be seen, it is not necessary to reload the timer in order to set the Interrupt Flag on the next count of zero. When set, the Interrupt Flag can be cleared by either reading T1C-L, by writing directly into the Interrupt Flag Register (IFR), or by a load into T1C-H when a new count value is desired.

Since the interval timers are all retriggerable, reloading the counter will always reinitialize the time-out period. Should the microprocessor continue to reload the counter before it reaches zero, counter time-out can be prevented. Timer 1 is able to operate in this manner provided the microprocessor writes into the high-order counter (T1C-H). By loading the latches only, the microprocessor can access the timer during each count-down operation without affecting the time-out in progress. In this way, data loaded into the latches will determine the length of the next subsequent time-out period.

Timer 2 Operation - Timer 2 operates in the One-Shot Mode only (as an interval timer). Timer 2 is made up of a write-only low-order latch (T2L-L), a read-only low-order counter (T2C-L), and a read/write high-order counter (T2C-H). This 16-bit counter decrements at a rate of (CLK/20).

Timer 2 One-Shot Mode - Operation of Timer 2 in the One-Shot Mode is similar to Timer 1. For each load T2C-H operation, Timer 2 sets the Interrupt Flag for each countdown to zero. However, after a time-out, the T2 counters roll over to all ones (FFFF) and continue to decrement. This two's-complement decrement allows the user to determine how long the T2 Interrupt Flag has been set. Since the Interrupt Flag logic is disabled after the initial interrupt set (zero count), further interrupts cannot be set by a subsequent count to zero. To enable the Interrupt Flag logic, the microprocessor must reload T2C-H. The Interrupt Flag is cleared by either reading T2C-L or by loading T2C-H.

SHIFT REGISTER OPERATION AND MODES

Shift Register Operation - The Shift Register performs bidirectional serial data transfers on lines CB2in and CB2out. These transfers are controlled by an internal modulo-8 counter. Shift pulses can be applied to the CB1 line for controlling external devices. Each Shift Register operating mode is controlled by control bits within the Auxiliary Control Register.

All combinations of Auxiliary Control Register (ACR) bits 4, 3, 2 except combinations 011 and 111 will disable the shift register.

Shift In - External CB1 Clock Control (011) - In this mode, CB1 provides the input clock and CB2in the data input to the Shift Register. In this way, an external device can load the Shift Register at its own pace. The Shift Register counter will interrupt the microprocessor after each eight bits have been shifted in. The Shift Register counter does not stop the shifting operation. Its function is simply that of a pulse counter. Reading or writing the Shift Register resets the Interrupt Flag and initializes the counter to count another eight pulses. Note that data is shifted during the first positive transition of CLK cycle following the positive-going edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle following CB1 going high.

Shift Out - External CB1 Clock Control (111) - In this mode, shifting is controlled by external pulses applied to the CB1 line. The Shift Register Counter sets the Interrupt Flag for each eight-pulse count, but does not disable the shifting function. In the case of shift out, the shift occurs on the positive going transition of CLK following the negative going edge of CBI. Each time the microprocessor reads from or writes to the Shift Register, the Interrupt Flag is reset and the counter is initialized to begin counting the next eight pulses on the CB1 line. After eight shift pulses, the Interrupt Flag is set. The microprocessor can then load the Shift Register with the next eight bits of data.

PERIPHERAL INTERFACE CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Unit
tR,tF	Rise and Fall Time for CA1, CB1, CA2 and CB2in Input Signals		1.0	µs
tSR1	Shift-Out Delay Time - Time From CB1 Falling Edge to CB2out Data	2 tcy + 9 ns		
tSR2	Shift-In Set-up Time - Time from CB2in Data to CB1 Rising Edge	tcy		
tSR3	CB2in to CB1 hold time	tcy		
tICW	Pulse Width - CB1 Input Clock	2 tcy		
tICS	Pulse Spacing -CB1 Input Clock	2 tcy		

FIGURE 1. TIMING FOR SHIFT OUT WITH EXTERNAL SHIFT CLOCKING

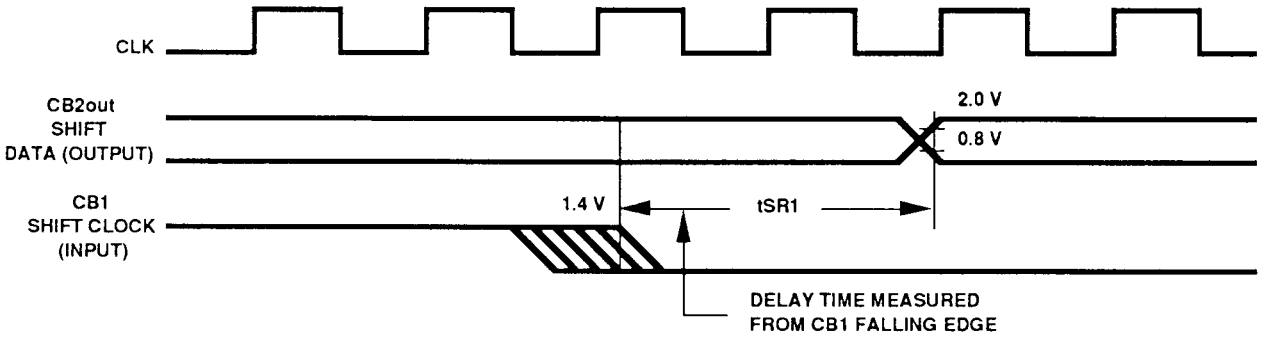


FIGURE 2. TIMING FOR SHIFT IN WITH EXTERNAL SHIFT CLOCKING

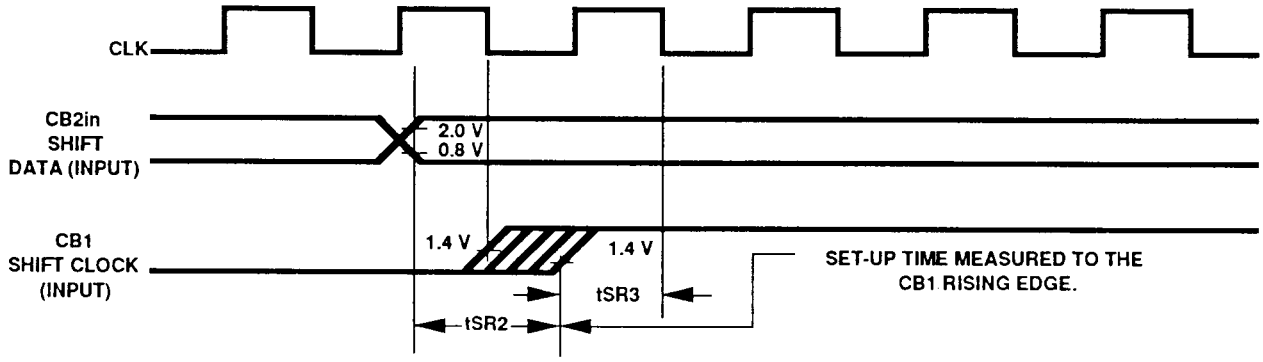


FIGURE 3. EXTERNAL SHIFT CLOCK TIMING

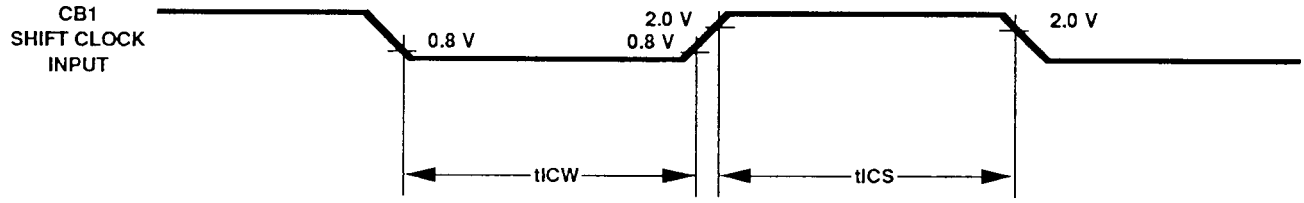


FIGURE 4. CLOCK SPECIFICATION

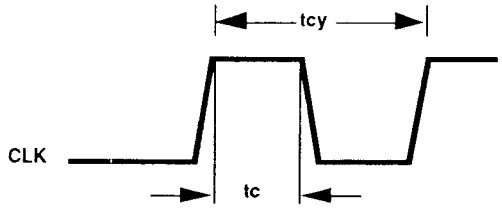


FIGURE 5. READ TIMING

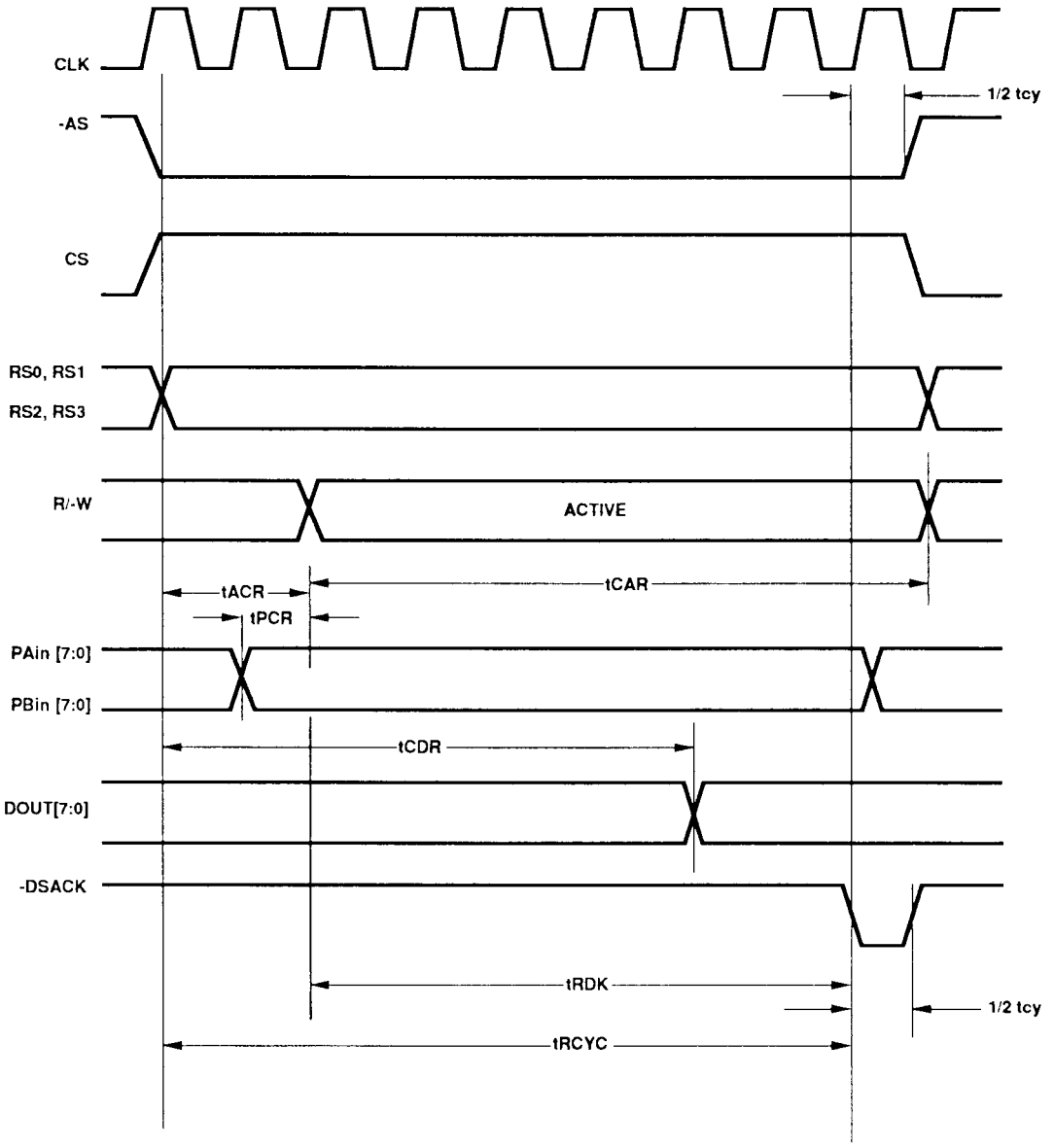
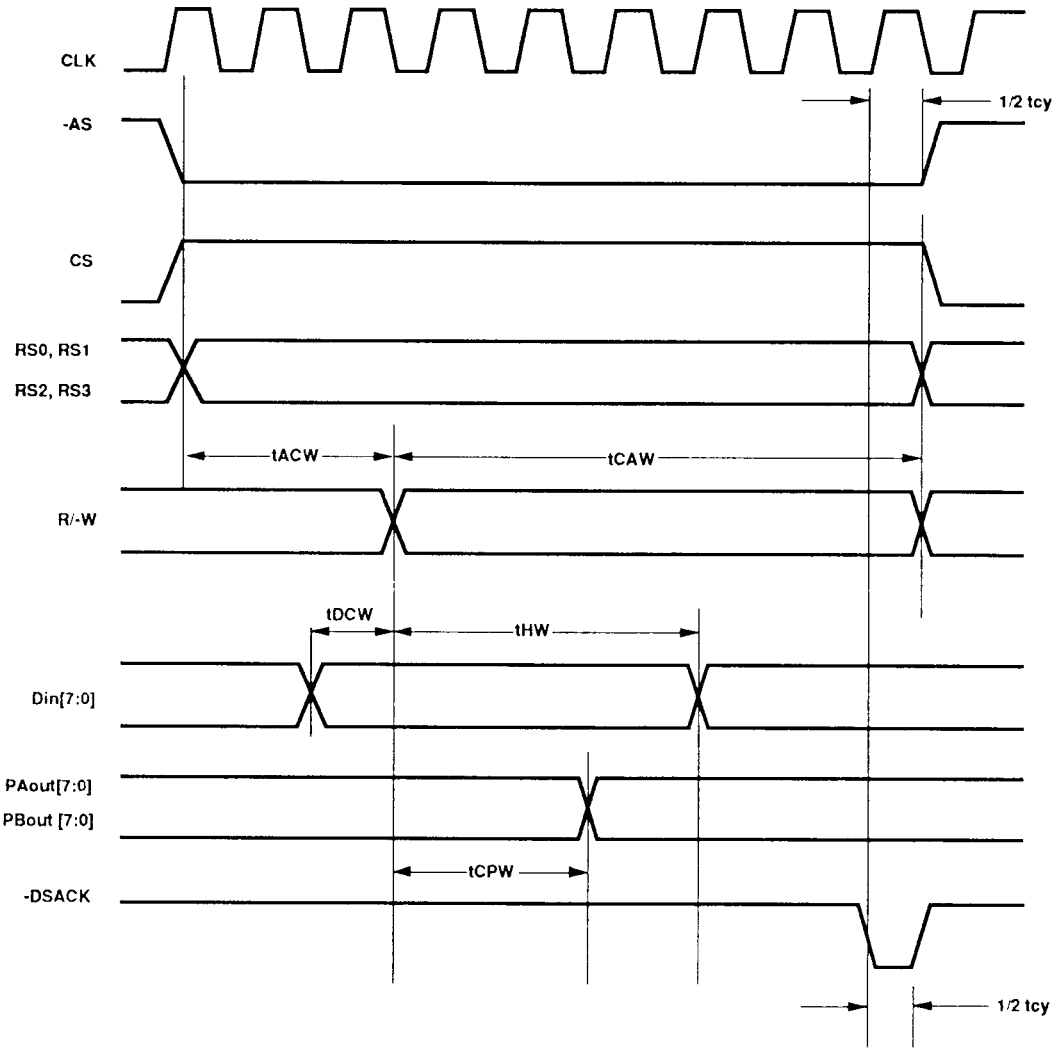


FIGURE 6. WRITE TIMING



REGISTER SELECT

	RS Coding					Register/Description	
Register Number	3	2	1	0	Register Designation	Write (R/-W=0)	Read (R/-W=1)
0	0	0	0	0	ORB/IRB	Output Register B	Input Register B
1	0	0	0	1	ORA/IRA	Output Register A	Input Register A
2	0	0	1	0	DDRB	Data Direction Register B	
3	0	0	1	1	DDRA	Data Direction Register A	
4	0	1	0	0	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1C-H	T1 High-Order Counter	
6	0	1	1	0	T1L-L	T1 Low-Order Latches	
7	0	1	1	1	T1L-H	T1 High-Order Latches	
8	1	0	0	0	T2C-L	T1 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2C-H	T1 High-Order Counter	
10	1	0	1	0	SR	Shift Register	
11	1	0	1	1	ACR	Auxiliary Control Register	
12	1	1	0	0	PCR	Peripheral control Register	
13	1	1	0	1	IFR	Interrupt Flag Register	
14	1	1	1	0	IER	Interrupt Enable Register	
15	1	1	1	1	ORA/IRA	Output Register A	Input Register A

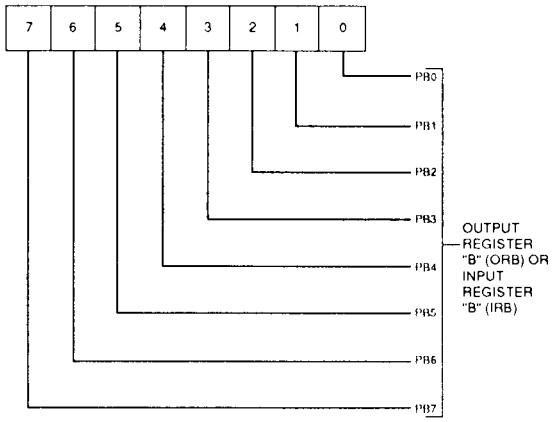
READ TIMING

		CLK=20 MHz		
Symbol	Parameter	Min.	Max.	Units
tcy	Cycle Time	50	60	ns
tc	Pulse Width	44	-	ns
tRDK	Read/Write to DSACK delay	4.5 tcy	23.5 tcy	
tACR	Address Setup Time	6 tcy	-	
tCAR	Address Hold Time	5 tcy	24 tcy	
tRCYC	-AS to DSACK delay	9.5 tcy	28.5 tcy	
tPCR	Peripheral Data Setup Time	0	-	ns
tCDR	Data Bus Delay Time	2.5 tcy	11.5 tcy	

WRITE TIMING

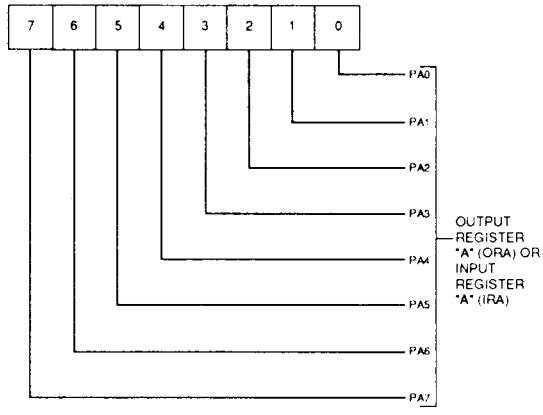
Symbol	Parameter	Min.	Max.	Units
tACW	Address Setup Time	5 tcy	-	
tCAW	Address Hold Time	5 tcy	24 tcy	
tDCW	Data Bus Setup Time	0	-	
tHW	Data Bus Hold Time	3 tcy	-	
tCPW	Peripheral Data Delay Time	13 ns + 3.5 tcy	13 ns + 22 tcy	

FIGURE 7. REGISTER 0, ORB/IRB



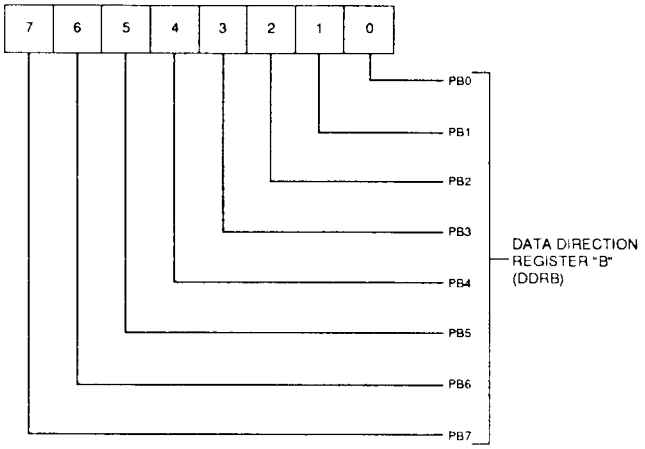
PIN DATA DIRECTION SELECTION	WRITE	READ
DDRB = "1" (OUTPUT)	MPU WRITES OUTPUT LEVEL INTO ORB (PBout)	MPU READS VALUE IN ORB (PBout)
DDRB = "0" (INPUT)	MPU WRITES INTO ORB, BUT NO EFFECT ON PBout PIN LEVEL UNTIL DDRB CHANGED	MPU READS LEVEL ON PBin PIN

FIGURE 8. REGISTER 1, ORA/IRA



PIN DATA DIRECTION SELECTION	WRITE	READ
DDRA = "1" (OUTPUT)	MPU WRITES OUTPUT LEVEL INTO ORA (PAout)	MPU READS VALUE OF ORA (PAout)
DDRA = "0" (OUTPUT)	MPU WRITES INTO ORA, BUT NO EFFECT ON PBout PIN LEVEL UNTIL DDRA CHANGED	MPU READS INPUT LEVEL ON PAin PIN

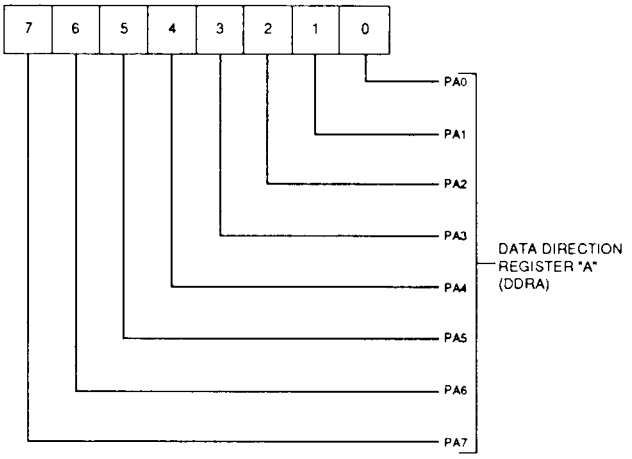
FIGURE 9. REGISTER 2, DDRB



"0" ASSOCIATED PB PIN IS AN INPUT (HIGH IMPEDANCE) (PBin ACTIVE)

"1" ASSOCIATED PB PIN IS AN OUTPUT WHOSE LEVEL IS DETERMINED BY ORB REGISTER BIT (PBout ACTIVE)

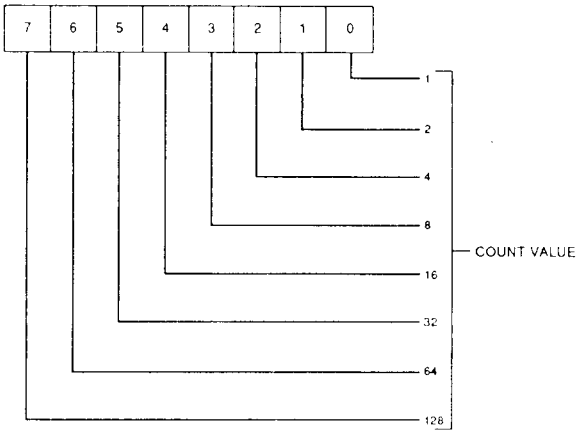
FIGURE 10. REGISTER 3, DDRA



"0" ASSOCIATED PA PIN IS AN INPUT (HIGH IMPEDANCE) (PAin ACTIVE)

"1" ASSOCIATED PA PIN IS AN OUTPUT WHOSE LEVEL IS DETERMINED BY ORA REGISTER BIT (PAout ACTIVE)

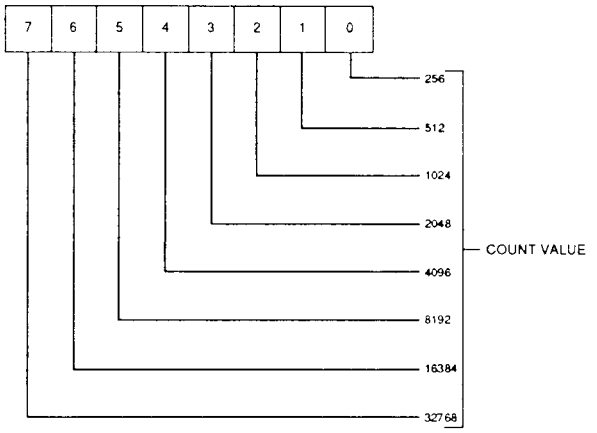
FIGURE 11. REGISTER 4, TIMER 1 LOW-ORDER COUNTER



WRITE - 8 BITS LOADED INTO T1 LOW-ORDER LATCHES. LATCH CONTENTS ARE TRANSFERRED INTO LOW-ORDER COUNTER AT THE TIME THE HIGH-ORDER COUNTER IS LOADED (REG 5)

READ - 8 BITS FROM T1 LOW-ORDER COUNTER TRANSFERRED TO MPU. IN ADDITION, T1 INTERRUPT FLAG IS RESET (BIT 6 IN INTERRUPT FLAG REGISTER)

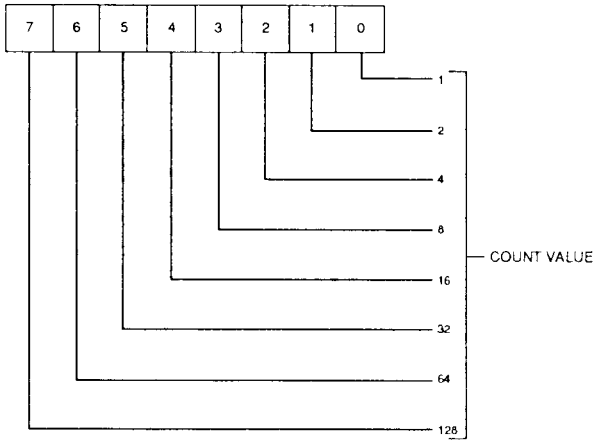
FIGURE 12. REGISTER 5, TIMER 1 HIGH-ORDER COUNTER



WRITE - 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES. ALSO AT THIS TIME BOTH HIGH- AND LOW-ORDER LATCHES TRANSFERRED INTO T1 COUNTER. T1 INTERRUPT FLAG ALSO IS RESET.

READ - 8 BITS FROM T1 HIGH-ORDER COUNTER TRANSFERRED TO MPU.

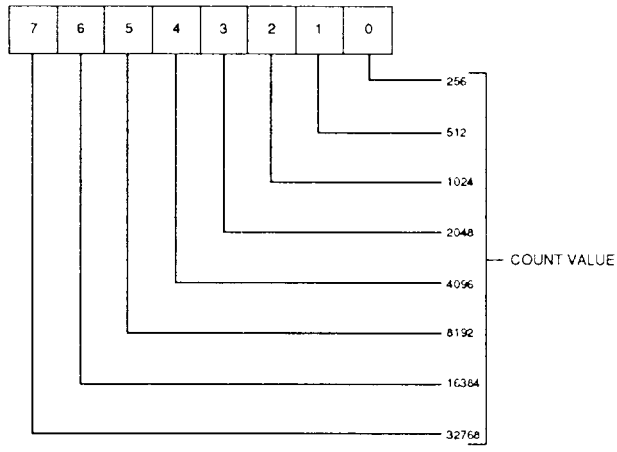
FIGURE 13. REGISTER 6, TIMER 1 LOW-ORDER LATCH



WRITE - 8 BITS LOADED INTO T1 LOW-ORDER LATCHES. THIS OPERATION IS NO DIFFERENT THAN A WRITE INTO REG 4.

READ - 8 BITS FROM T1 LOW-ORDER LATCHES TRANSFERRED TO MPU. UNLIKE REG 4 OPERATION, THIS DOES NOT CAUSE RESET OF T1 INTERRUPT FLAG.

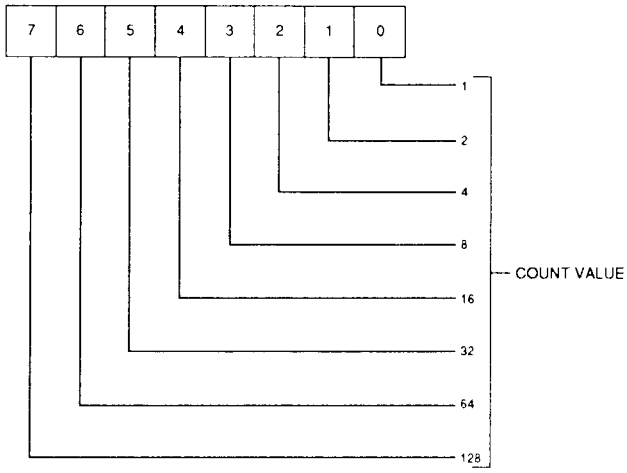
FIGURE 14. REGISTER 7, TIMER 1 HIGH-ORDER LATCH



WRITE - 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES. UNLIKE REG 4 OPERATION NO LATCH-TO-COUNTER TRANSFERS TAKE PLACE.

READ - 8 BITS FROM T1 HIGH-ORDER LATCHES TRANSFERRED TO MPU.

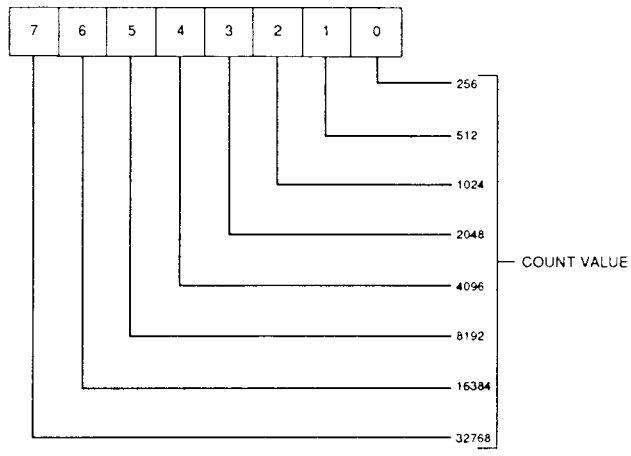
FIGURE 15. REGISTER 8, TIMER 2 LOW-ORDER LATCH/ COUNTER



WRITE - 8 BITS LOADED INTO T2 LOW-ORDER LATCH.

READ - 8 BITS FROM T2 LOW-ORDER COUNTER TRANSFERRED TO MPU. T2 INTERRUPT FLAG IS RESET.

FIGURE 16. REGISTER 9, TIMER 2 HIGH-ORDER LATCH/ COUNTER



WRITE - 8 BITS LOADED INTO T2 HIGH-ORDER COUNTER. ALSO LOW-ORDER LATCH TRANSFERRED TO LOW-ORDER COUNTER. IN ADDITION T2 INTERRUPT FLAG IS RESET.

READ - 8 BITS FROM T2 HIGH-ORDER COUNTER TRANSFERRED TO MPU.

FIGURE 17. REGISTER 10, SHIFT REGISTER, REGISTER, Notes 1 and 2

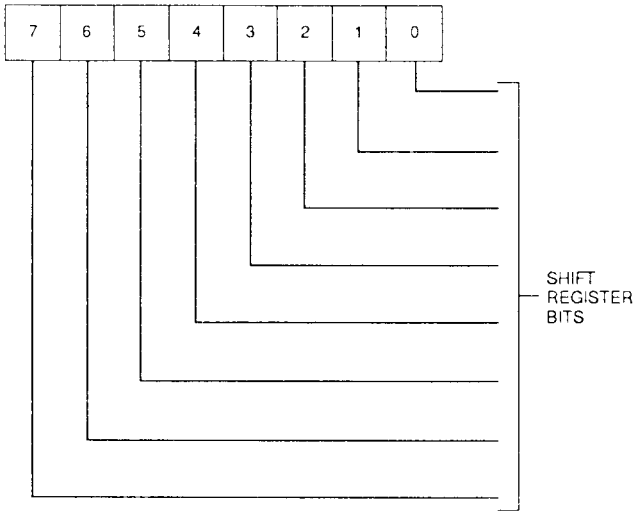
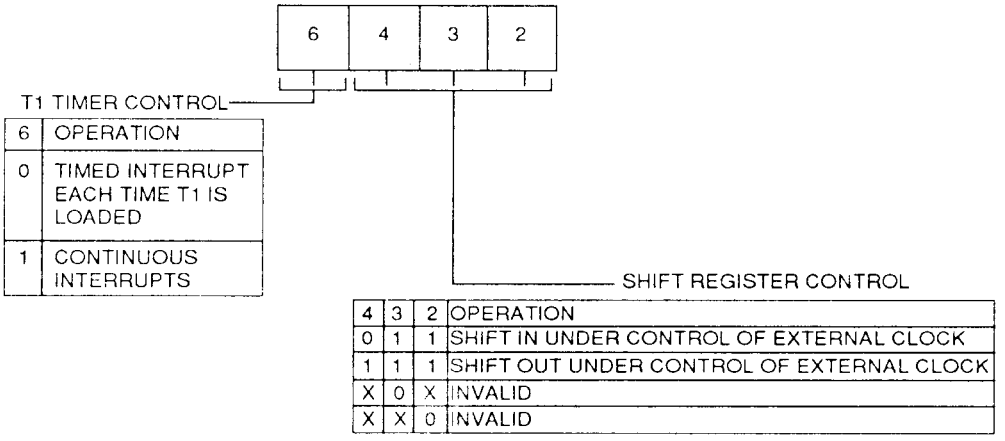


FIGURE 18. REGISTER 11, AUXILIARY CONTROL REGISTER, Note 3

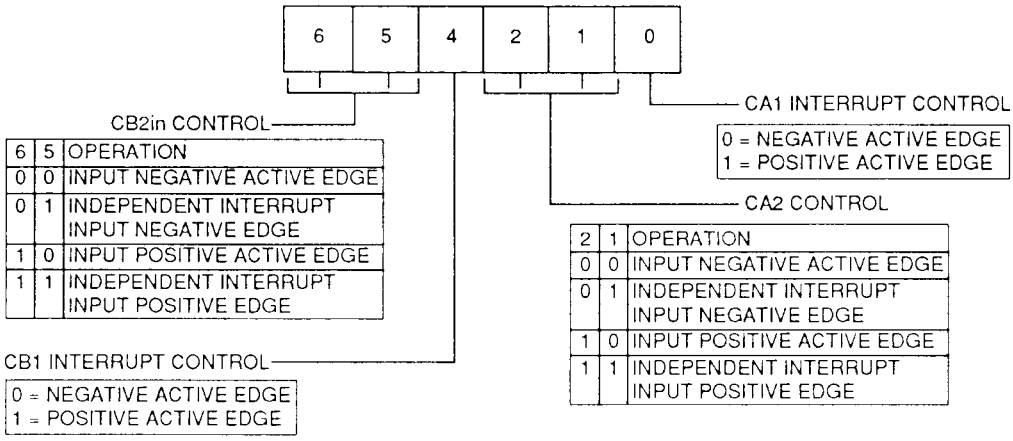


6	OPERATION
0	TIMED INTERRUPT EACH TIME T1 IS LOADED
1	CONTINUOUS INTERRUPTS

4	3	2	OPERATION
0	1	1	SHIFT IN UNDER CONTROL OF EXTERNAL CLOCK
1	1	1	SHIFT OUT UNDER CONTROL OF EXTERNAL CLOCK
X	0	X	INVALID
X	X	0	INVALID

Notes:
1. When shifting out, Bit 7 is the first bit out and simultaneously is rotated back into Bit 0.
2. When shifting in, Bit 0 enters first and Bit 7 last.
3. All unused bits can be 0 or 1.

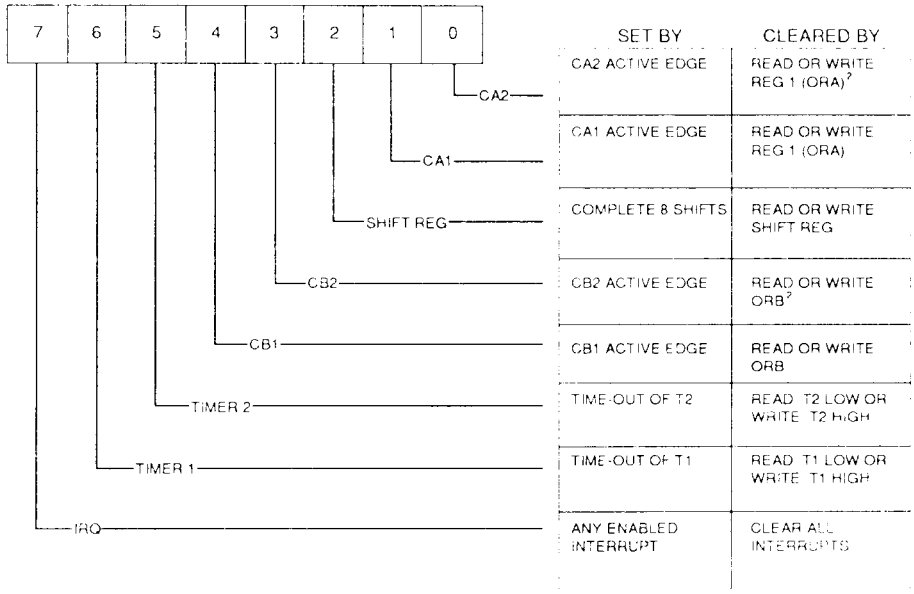
FIGURE 19. REGISTER 12, PERIPHERAL CONTROL REGISTER, Note 1



6	5	OPERATION
0	0	INPUT NEGATIVE ACTIVE EDGE
0	1	INDEPENDENT INTERRUPT INPUT NEGATIVE EDGE
1	0	INPUT POSITIVE ACTIVE EDGE
1	1	INDEPENDENT INTERRUPT INPUT POSITIVE EDGE

2	1	OPERATION
0	0	INPUT NEGATIVE ACTIVE EDGE
0	1	INDEPENDENT INTERRUPT INPUT NEGATIVE EDGE
1	0	INPUT POSITIVE ACTIVE EDGE
1	1	INDEPENDENT INTERRUPT INPUT POSITIVE EDGE

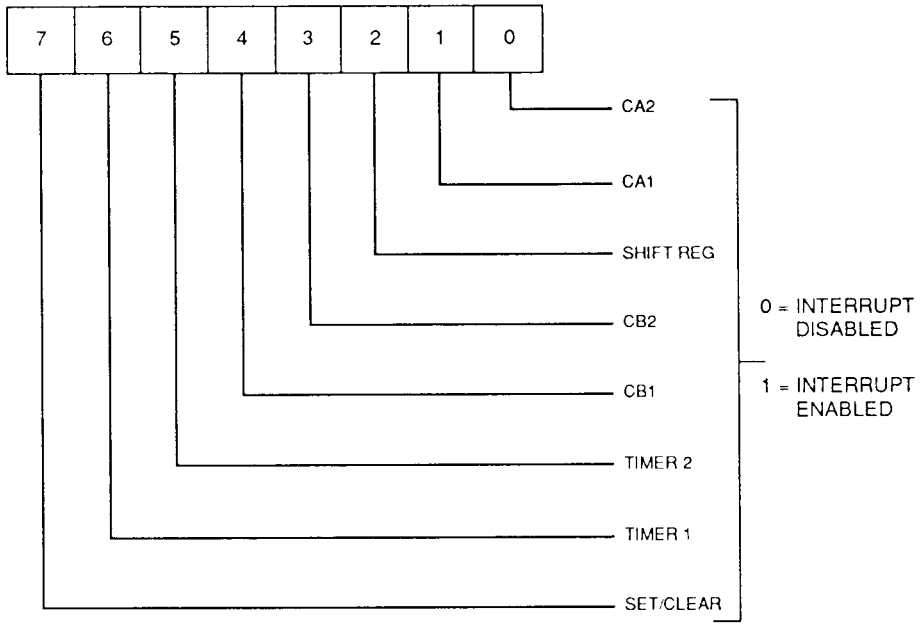
FIGURE 20. REGISTER 13, INTERRUPT FLAG REGISTER, Note 2



	SET BY	CLEARED BY
CA2	CA2 ACTIVE EDGE	READ OR WRITE REG 1 (ORA)[2]
CA1	CA1 ACTIVE EDGE	READ OR WRITE REG 1 (ORA)
SHIFT REG	COMPLETE 8 SHIFTS	READ OR WRITE SHIFT REG
CB2	CB2 ACTIVE EDGE	READ OR WRITE ORB[2]
CB1	CB1 ACTIVE EDGE	READ OR WRITE ORB
TIMER 2	TIME-OUT OF T2	READ T2 LOW OR WRITE T2 HIGH
TIMER 1	TIME-OUT OF T1	READ T1 LOW OR WRITE T1 HIGH
IRQ	ANY ENABLED INTERRUPT	CLEAR ALL INTERRUPTS

Notes:
1. All unused bits can be 0 or 1.
2. If the CA2/CB2 control in the PCR is selected as "independent" interrupt input, then reading or writing the output register ORA/ORB will not clear the flag bit. Instead, the bit must be cleared by writing into the IFR, as described previously.

FIGURE 21. REGISTER 14, INTERRUPT ENABLE REGISTER, Notes 1-3



Notes:

1. If Bit 7 is a "0" then each "1" in Bits 0-6 disables the corresponding interrupt.
2. If Bit 7 is a "1" then each "1" in Bits 0-6 enables the corresponding interrupt.
3. If a read of this register is done, Bit 7 will be "1" and all other bits will reflect their enable/disable state.

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