ENGG1000
Engineering Design and Innovation
Supplementary Course Outline – Semester 1, 2016

Never Stand Still | Faculty of Engineering | School of Electrical Engineering and Telecommunications

Supplementary Details for Projects in the School of Electrical Engineering and Telecommunications

Introductory Note

ENGG1000 is a single course coordinated by the Faculty of Engineering. Most of the course is run by individual schools within the Faculty, through a collection of structured projects. This document provides supplementary information which is specific to projects undertaken within the School of Electrical Engineering and Telecommunications (EE&T); it is intended to be **read in conjunction with the faculty-wide course outline**, which you can obtain via Moodle (https://moodle.telt.unsw.edu.au/login/index.php).

Course Staff

EET Project Coordinator: Dr. Alex von Brasch, Room MSE719A, a.vonbrasch@unsw.edu.au

Consultations: The Project Coordinator will be available during most scheduled laboratory times, and will generally also be available for consultation from 5:30pm to 6:30pm on Mondays and Thursdays during the semester (either in the lab or in his office). Due to his other teaching and research commitments, and commitments in industry, he may unavailable or not in his office at other times. Please contact him via email to make an appointment. ALL email enquiries should be made from your student email address with ENGG1000 in the subject line, otherwise they may not be answered.

Staff Mentors: Staff Mentors: Each student will be assigned to an individual mentor group, with guidance from members of academic staff. A substantial component of the marks are derived from your mentor's assessment of your learning and participation.

Laboratory Demonstrators: Each laboratory will be staffed by a number of experienced demonstrators.

Keeping Informed: Announcements may be made during classes, via email (to your student email address) and/or via online learning and teaching platforms – in this course, we will use Moodle https://moodle.telt.unsw.edu.au/login/index.php. Please note that you will be deemed to have received this information, so you should take careful note of all announcements.

Course Summary

Contact Hours

The course comprises lectures, mentor meetings and laboratory work up to 5-6 hours per week, depending on the activities scheduled in each week (refer to schedule below in this outline and also the faculty-wide schedule in the Faculty ENGG1000 Course Outline). The nominal break-down is as follows:

Lectures	**Day**	**Time**	**Location**
	Monday	2pm - 3pm	EEG25
	Thursday	2pm - 3pm	CLB8
Mentor Sessions	Thursday	3pm – 4pm or 4pm – 5pm	Allocated in Week 2 and posted on Moodle
Laboratory Times	Monday	2pm - 5pm	EE101/102 EE113/114
	Thursday	2pm – 5pm	EE101/102 EE113/114

Lectures

(Mondays 2-3pm in the EEG25 and Thursdays 2-3pm in CLB8), starting Thursday, Week 2. Note that there will also be some faculty-run lectures in various locations through the course. A detailed calendar showing week to week activities will be kept up-to-date on the course Moodle website.

Laboratories

Nominally on Mondays 2:00-5:00pm, in EE101/102/113/114. These labs are all located on the 1st floor of the EE building. The laboratories begin in Week 4.
Note that the lab opening times will be extended as needed throughout the session, potentially covering Monday 2:00-6:00pm and Thursday 2:00-7:00pm. Attendance at the laboratories outside the scheduled times is optional, and this is provided merely to provide project teams with access to the facilities to help them work on their project.

Mentor Group Locations:

These will be allocated in Week 2, and posted on the Course Moodle website. The Mentor Sessions begin in Week 2.

Aims within the School of EE&T

The main aims of ENGG1000 are clearly explained in the Faculty Course Outline. In keeping with these, the ElecEng project aims to provide a framework for experiential learning, to introduce you to the design process, and to familiarize you with the many facets of engineering projects. Within the school, however, there are some specific additional aims:

a. To convey some basic details of the principles of electrical devices, construction of electronic circuits and analysis techniques, in order to design, build and test simple circuits.
b. To familiarize you with the test equipment available in the electronics laboratories, in order to evaluate your design effectively.
c. To motivate the learning you will undertake in future courses, both in science and engineering, through a practical design problem.

Perhaps unlike some other projects in ENGG1000, many students may not begin the course with much experience in building circuits or measuring electrical quantities. This course provides a fairly gentle (and hopefully fun!) but brief introduction to electronic circuits, while keeping the emphasis on engineering design.

It is not the aim of this course to provide a detailed understanding of electronics. A common question is why so many complex devices and circuits are introduced. The answer is simple: purely resistive circuits are not interesting as design projects. The technical stream of this course tries to give the minimal detail required in order to use a wide array of different kinds of circuits, while mastery is left for later courses.

If you feel at various points in the course that you don't have enough knowledge and skills to undertake the project, you are not alone (indeed many professional engineers feel this way when beginning a new project). The aim of this course is not to convince you of how much you do or don't know, it is to help you develop the skills to identify for yourself and your team what is and is not known, what needs to be researched, what answers need to be found, what needs to be done and what resources or people are needed for this.

Course Schedule

Period	Monday	Thursday
Week 1 (29 Feb)	2:00 Introductory Lecture (Clancy Auditorium or Science Theatre)	2:00 **Impromptu Design Activity (assessable)** – see Faculty Outline. Venue to be advised at First Lecture and through Moodle.
Week 2 (7 Mar)	2:00 **Impromptu Design Review (assessable)** – see Faculty Outline.	2:00 Lecture 1 (CLB8) 3:00-4:00 or 4:00-5:00 Mentor Meeting 1
Week 3 (14 Mar)	2:00 Lecture 2 (EEG25)	2:00 Lecture 3 (CLB8) 3:00-4:00 or 4:00-5:00 Mentor Meeting 2
Week 4 (21 Mar)	2:00 Lecture 4 (EEG25) 3:00-5:00 Laboratory	2:00 Lecture 5 (CLB8) 3:00-4:00 or 4:00-5:00 Mentor Meeting 3
Mid-semester Break		
Week 5 (4 Apr)	2:00 Lecture 6 (EEG25) 3:00-5:00 Laboratory	2:00 Lecture 7 (CLB8) 3:00-4:00 or 4:00-5:00 Mentor Meeting 4
Week 6 (11 Apr)	2:00 Lecture 8 (EEG25) 3:00-5:00 Laboratory	2:00 Lecture 9 (CLB8) 3:00-4:00 or 4:00-5:00 Mentor Meeting 5
Week 7 (18 Apr)	2:00-4:00 **Circuit Principles Test**(TBA) 2:00-5:00 Laboratory	2:00 Lecture 10 (CLB8) 3:00-4:00 or 4:00-5:00 Mentor Meeting 6
Week 8 (25 Apr)	Public Holiday	2:00 Lecture 11 (CLB8) 3:00-4:00 or 4:00-5:00 Mentor Meeting 7
Week 9 (2 May)	2:00-5:00 **Laboratory Skills Test**(TBA)	2:00-5:00 **Project Team Presentations (TBA)**
Week 10 (9 May)	2:00-5:00 Laboratory	2:00-5:00 **Acceptance Testing(EE319)**
Week 11 (16 May)	2:00-5:00 Laboratory	2:00 Lecture 12 (CLB8) 3:00-4:00 or 4:00-5:00 Mentor Meeting 8
Week 12 (23 May)	2:00-5:00 Laboratory	2:00-5:00 Laboratory 3:00-4:00 or 4:00-5:00 Mentor Meeting 9
Week 13 (30 May)	2:00-5:00 **Final Testing(EE319)**	No Class

Laboratory rooms are EE101, 102, 113, 114
Yellow shading denotes Faculty of Engineering activities

Key Dates

Week 1 (Friday): By now you must have selected your project, by following the instructions on Moodle (https://moodle.telt.unsw.edu.au/login/index.php)
Week 4 (Friday): Submit a project plan on Moodle. This is not assessable, but is your first opportunity for formal feedback.
Week 7 (Friday): Submit your design proposal on Moodle.
Week 13 (Friday): Submit your team's final report on Moodle. Ensure that the cover sheet has been signed by all team members and is attached to your electronic submission.

Assessment Specific to the EE&T Project

Assessment in the ElecEng project has similar components to the other projects throughout ENGG1000, however an effort has been made to keep the number of assessments to a minimum, to provide a positive learning experience and in response to student feedback from previous semesters. This is made possible largely through the mentoring process.

Assessment	Weight
Faculty-wide Impromptu Design Activity (Individual)	5%
Active learning, planning, group participation (important!), and lab notebooks, assessed by mentors (Individual)	10%
Technical Assessment (Individual) Two from (10% each): • Lab Checkpoints & Lab Report • Circuit Principles Test • Lab Skills Test	20%
Calibrated Peer Review (Individual)	10%
Design proposal report (Group)	10%
Project Presentations (Group)	10%
Acceptance Testing (Group)	5%
Final Testing (Group)	15%
Final Report (Group)	15%

The assessment is thus roughly evenly distributed between individual and team marks, reflecting the requirement of the project. Experience from previous semesters has shown that well-organised groups that communicate, set high standards, self-organise and resolve conflicts effectively are essential to succeeding in the project.

The learning, planning and participation mark will be assigned by your mentor. Please note:

- High marks will be given for the following: Committed to project, actively contributing to mentor meetings and non-timetabled meetings, to the design and its implementation and testing, and to the written submissions. Demonstrates commitment to the success of the group (as defined by the group at the beginning of the project) and helps the group to function effectively.
- Low marks will be given for the following: Non-attendance without advance explanation, lack of engagement or participation (including silence in mentor meetings), failure to deliver on tasks assigned by the group, poorly detailed/missing lab notebooks, or obstruction to group progress (e.g. falling out of contact while holding key project details). Feedback on whether your participation has been satisfactory is available at any time from your mentor and also from your group. Formal peer assessment from your group members will be conducted mid-way through the project.
- ***You must pass this assessment item to pass the course.*** Failure in this assessment item can result in an overall grade of Unsatisfactory Fail (UF), even if your overall course mark is above 50. This would usually occur when both the

mentor and group finds that participation has been unsatisfactory. If you believe that your individual circumstances pose risks to your group participation, act early and discuss these with your group and mentor ahead of time, to avoid disappointment.

Lab notebooks are a means of recording design, technical and organizational information for later use, and are a helpful tool both during study and in professional life. You must bring your lab notebook to all classes, and record both the introductory lab and notes from mentor meetings and later labs. Lab notebooks will be assessed according to the following criteria: purpose of notes (why were they made?), date (when were they made?), clarity (could someone else understand them?), detail (e.g. if you sketch your circuit diagram, could someone else build it exactly from the sketch?), completeness of experimental notes, interpretation of results or discussion of design/circuit, and evidence of research or individual input (i.e. repeating lecture notes will not attract marks). Marks will be assigned in week 12, but the lecturer or mentor may request your notebook at any time, and their mark will be based on your overall effort.

Not being the major focus of the course, 20% of your assessment for ENGG1000 is to be taken from technical assessment. To this end the EE&T project offers three assessment tasks worth 10% each – a student may undertake any two of three available assessments to make the 20% technical component assessment. The three assessment are: The Laboratory Skills Test; the Circuit Principles Test; and the Lab Checkpoints & Lab Book Report Assessment.

The laboratory skills test will assess your familiarity with basic circuit construction, circuit analysis, and laboratory equipment, gained while completing the introductory labs, and will give you feedback on your understanding. Marks will be assigned by lab demonstrators according to pre-determined criteria. This assessment task will be held on Monday 2nd May 2-5pm (Week 9). To be eligible to sit for this laboratory exam, students must enroll to do on the Course Website (http://moodle.telt.unsw.edu.au) one full week prior to this exam, by 10pm on Tuesday 26th April – failure to do so will mean the student will not be permitted to undertake this assessment task.

The circuit design principles test will assess your understanding of simple circuit analysis and design using a multiple choice exam of 30 min duration. Marks will be assigned based on the correctness of your answers. This exam will be held on Monday 18th April 2-4pm (Week 7). To be eligible to sit for this laboratory exam, students must enroll to do on the Course Website (http://moodle.telt.unsw.edu.au) one full week prior to this exam, by 10pm on Monday 11th April – failure to do so will mean the student will not be permitted to undertake this assessment task.

The Electrical Stream lab program features four optional labs. However, for assessment purposes a student may complete either Lab 2, 3, or 4 to achieve 10% of their final mark. This requires the student to have all checkpoints marked off by a lab demonstrator, and submit a written lab report containing all circuit designs, measurements made, and results obtained. This report must be submitted to the lecturer before 5pm Friday 6th May (Week 9).

Calibrated Peer Review is used in assessment of the first three phases of the design process. Students are required to submit a short essay reflecting on the corresponding aspect of the design process, using the recommended text as the main resource, and then to assess and give feedback to other students on their submissions. The aim of this process is both to allow students to reflect on and express their thoughts on the design process they are undertaking, and also to enable students to develop the important skill of giving critical and constructive feedback. A student's mark is determined not only by the quality of their own work but also on the accuracy and value of the feedback given to other students. You will be able to logon directly following the link in Moodle, using your Moodle login details

(zPass). The Calibrated Peer Review is done using an application in Moodle called the Workshop Tool.

Written and oral communication are consistently among the top priorities for engineering employers, and developing report writing skills are an important aspect of design and innovation. The criteria for assessing the design proposal and final design reports are given on the respective report cover sheets.

On Thursday 5th May (Week 9) your group will be scheduled a time to present your design to your lecturers and mentors. This will be a short 15-20 minute verbal presentation of the group's proposed design and plan for completion of the project. The design team should treat the mentor as a client for this task. The group will be assessed on the clarity and professionalism of the presentation, as well as the use of verbal and non-verbal cues. (5% of final grade)

The acceptance testing and final testing assess the success of the group's solution to the given problem. The details and marking criteria used during the testing are given in the ElecEng project brief.

The final testing and final report marks will be moderated on an individual basis by peer assessment. Peer assessment will be conducted as follows:

- After the acceptance testing, you will score all your fellow team members on their contribution to the project. This feedback will be anonymously passed to them, and the scores will not be used for assessment purposes. Students with low scores should act quickly to discuss this with their team and mentors.
- At the final mentor meeting, you will again score all your fellow team members on their contribution to the project. The scores of your team members will be averaged to produce a peer assessment score for the project. This score will then be used to moderate the final testing and final report marks, i.e. if you contribute little to the team, then your final testing and final report marks may be lower than for others in the team, while if you are a strong contributor to the team, then your final testing and final report marks may be higher than for others. The peer assessment will be applied as an individual weighting to the final testing and final report group marks.

Peer assessment is an important part of assessing group projects, because your contribution to the team is vital to the team's success.

Late submissions of assessed work attract a penalty of 5% per day, including weekends. After 10 days, a mark of zero will be awarded.

Course Details

Credits

The course is a 6 UoC course; expected workload is 10 hours per week throughout the 13 week session.

Relationship to Other Courses

Within the School of EE&T there are courses on design and innovation at nearly every level of the curriculum: in second and third year, ELEC2117 and ELEC3117 are design courses in which a substantive project is undertaken, while in fourth year, ELEC4123 builds on students' design proficiency and in most cases design is an aspect of the final year honours project. ENGG1000 can thus be seen as an introduction to a design theme that runs throughout electrical/telecommunications/photonics engineering. ENGG1000 also provides

introductory-level knowledge of aspects of electrical energy, electronics, telecommunications and control systems, which together form the majority of courses within the EE&T degree programs.

Learning outcomes

Additionally to the faculty learning outcomes, on successful completion you should be able to:

1. Explain some of the design challenges faced by electrical and telecommunications engineers, and what kinds of skills and knowledge are needed to tackle them.
2. Give examples of design trade-offs typically experienced during electrical design.
3. Explain the types of applications of simple electronic circuits, and suggest example circuit designs for simple problems.
4. Understand basic electrical quantities, in particular voltage and current, from a practical perspective: how to measure them and what values to expect for a given circuit design or application.
5. Suggest approaches for debugging simple circuit problems.

This course is designed to provide the above learning outcomes which arise from targeted graduate capabilities listed in ***Appendix A***. The targeted graduate capabilities broadly support the UNSW and Faculty of Engineering graduate capabilities (listed in ***Appendix B***). This course also addresses the Engineers Australia (National Accreditation Body) Stage I competency standard as outlined in ***Appendix C***.

Teaching Strategies

The teaching strategies are explained in more detail in the faculty course outline. Like other projects, the teaching in the ElecEng project is centred around the project. For example, you will develop communication skills by communicating about the project; you will develop team work and project management skills in endeavouring to accomplish your project on time; you will experience the kinds of technical problems that engineers deal with on industrial projects; you will learn the importance of identifying sub-systems within a design and planning carefully for their integration by solving a complex problem; you will develop design skills by following a design process, by evaluating and comparing designs and by reflecting on them; you will learn information literacy as you sift through large amounts of information to focus in on exactly what you need to propose and implement your design. Although other courses in your degree may vary in their teaching strategy, your understanding of and ownership of the learning process developed in this course should prove invaluable for the remainder of your degree program.

The course consists of lectures, labs and tutorials. The lectures will provide the rationale for the design process followed in the course and some basic electrical engineering principles to act as a starting point for addressing the design brief. The labs and mentor meetings are intended to provide guidance on your self-directed path of discovering the relevant information and skills needed to successfully complete the project. Mentor meetings in particular have been found to provide a very effective means of transferring knowledge and guidance. Each project team, of approximately 8 students, meets with an academic staff mentor for 1 hour in each of weeks 2 through 12.

Mentors will:

- facilitate discussions of the design process and help you to reflect upon your learning in the course
- expect you to arrive prepared, having completed your assigned actions from the previous meeting
- expect to see your laboratory notebooks and discuss your design ideas with you

- expect to you to arrive with questions (better quality questions means better quality answers)
- expect to see teams meeting regularly, developing action points for team members, and follow-up on these by individuals
- guide you through the design process
- help to put the role of other classes such as Maths and Physics into perspective with respect to engineering
- help you to understand design concepts, background knowledge in electronic circuits, and many other things, but you need to take the initiative to use this resource by coming prepared to your mentor meetings

Mentors will not:

- solve the problem for you or your team, but they will help you to solve it yourself
- 'rescue' your team if you fall behind schedule or are underprepared

Mentors will assess your individual learning and contribution to your team's design project. Your design proposal will be marked by your own mentor, but your final report will be marked by another group's mentor. This provides calibration data to help equalize scores given by different markers and also motivates you to write clearly for others to read your work.

Learning in this course

You are expected to attend all lectures, tutorials, labs, and mid-semester exams in order to maximise learning. You must prepare well for your laboratory classes and your lab work will be assessed. In addition to the lecture notes/video, you should read relevant sections of the recommended text. Reading additional texts will further enhance your learning experience. Group learning is also encouraged. UNSW *assumes* that self-directed study of this kind is undertaken in addition to attending face-to-face classes throughout the course.

Laboratory program

You are advised to do the following in preparation for you**r first electronics laboratory:**

- Wear covered shoes. Without these you will be refused entry to all Electrical Engineering labs.
- Obtain a prototyping board before the first lab. If you do not own one, you can purchase one from the Electrical Engineering School Office for $15.
- You may also find it helpful to have a small pair of pliers and a set of small screwdrivers.
- Complete the online safety training (instructions via Moodle) before the first lab. Under no circumstances is 240V to be used at any stage during this course. All voltages must be safe for consumer electronics without requiring any special insulation (i.e. typically 1.5V to 9V DC).
- Get a lab notebook, and bring it to every lab (and every mentor meeting and team project meeting).
- Read the laboratory exercises in advance of the lab.
- Read the related lecture notes in advance of the lab, and bring them to the lab.
- If you expect to do soldering (more likely in the later labs), bring safety goggles or purchase them from the Electrical Engineering School Office for $5.

The Electronics Workshop is located in room G15, on the ground floor of the Electrical Engineering building. Any of the components whose datasheets appear on the course website at http://moodle.unsw.edu.au may be purchased from the Electronics Workshop, and in some cases may be obtained in very small quantities free of charge, after obtaining

permission from a lab demonstrator (via signed component request form). This form may also be found on the course web site.

Laboratory Exemption

There is no laboratory exemption for this course. Regardless of whether equivalent labs have been completed in previous courses, all students enrolled in this course for Semester 1, 2016 must take the labs. If, for medical reasons, (note that a valid medical certificate must be provided) you are unable to attend a lab, you will need to apply for a catch-up lab during another lab time, as agreed by the laboratory coordinator.

Course Resources

Wondering where or how to get started? Here are some suggestions, from various sources:

- The **recommended** text book for ENGG1000, required for the calibrated peer review assessment:
  - Dym, C. L., and Little, P., *Engineering Design: A Project-Based Introduction*, 3rd Edition, Wiley, 2008.
- Another good one for introductory engineering design is:
  - Horenstein, M. N., *Design Concepts for Engineers*, Pearson/Prentice Hall, 2006
- More specifically for electrical engineering design are:
  - Wilcox, A. D., *Engineering Design for Electrical Engineers*, Pearson/Prentice-Hall, 1989 (this interprets design perhaps more closely to EE&T than the others, and in various sections discusses aspects of specific relevance to Electrical Engineering)
  - J.E. Salt and R Rothery, *Design For Electrical and Computer Engineers*, John Wiley & Sons 2002.
  - Stadtmiller, D. J., *Applied Electronic Design*, Prentice-Hall, NJ, 2003.
- More technical books that may help (most helpful in bold) include:
  - Brindley, K., ***Starting Electronics***, Elsevier, Burlington, MA, 2005. (very clearly written, this is an excellent introduction to electronics for anyone new to the subject) – in UNSW library
  - Kybett, H., and Boysen, E., ***All new electronics self-teaching guide***, Wiley, Indianapolis, IN, 2008. (another great book for getting started on electronics principles, includes revision exercises) – available online from UNSW library
  - Scherz, P., ***Practical Electronics for Inventors***, McGraw-Hill, 2000 (this is a ***very helpful*** book on introductory electronics, and includes example circuits and practical design tips) – in UNSW library
  - Slone, G. R., *Tab Electronics Guide to Understanding Electricity and Electronics*, McGraw-Hill, 2000. – Google books
  - Mims, F. M., *Getting Started in Electronics*, Master Publishing Inc, 2003. (practical set of notes at a very introductory level, still mainly theory)
  - Radio Society of Great Britain, *Radio and Electronics Cookbook*, Newnes, Woburn, MA, 2001 (maybe some useful circuit ideas) – Google books
  - Carlson, A. B., and Gisser, D. G., *Electrical Engineering: Concepts and Applications* (this is not a design text, but is written at about the right level to provide a useful resource for circuit analysis)
- Also:
  - The EE&T project Moodle web site http://moodle.unsw.edu.au (may be updated as the semester unfolds)

- Kerzner, H., *Project Management: A Systems Approach to Planning, Scheduling and Controlling*, Wiley, 2007
- D. A. Norman, *The Design of Everyday Things*, Currency-Doubleday, 1990. (a general text on design by a design guru)
- Selinger, C., *Stuff you don't learn in engineering school: Skills for success in the real world*, Wiley, 2004 (how to work in a team, etc. Read it for interest, or before you do your industrial training)
- P. Horowitz and W. Hill, *The Art of Electronics*, Cambridge University Press, 1989 (this is not an introductory book, but is full of insightful design tips).
- Circuit example web sites, for example:
  - http://www.aldinc.com/ald_circuitideas.htm
  - http://www.discovercircuits.com/list.htm
  - http://www.allaboutcircuits.com/
  - http://www.opencircuits.com/Basic_Circuits_and_Circuit_Building_Blocks
  - http://www.kpsec.freeuk.com/trancirc.htm
  - http://www.eleinmec.com/index.asp
  - http://hobby_elec.piclist.com/e_pic.htm (PIC microcontrollers)

Other Matters

Academic Honesty and Plagiarism

Plagiarism is the unacknowledged use of other people's work, including the copying of assignment works and laboratory results from other students. Plagiarism is considered a form of academic misconduct, and the University has very strict rules that include some severe penalties. For UNSW policies, penalties and information to help you avoid plagiarism, see http://www.lc.unsw.edu.au/plagiarism. To find out if you understand plagiarism correctly, try this short quiz: https://student.unsw.edu.au/plagiarism-quiz.

Student Responsibilities and Conduct

Students are expected to be familiar with and adhere to all UNSW policies (see https://my.unsw.edu.au/student/atoz/ABC.html), and particular attention is drawn to the following:

Workload

It is expected that you will spend at least **ten to twelve hours per week** studying a 6 UoC course, from Week 1 until the final assessment, including both face-to-face classes and *independent, self-directed study*. In periods where you need to need to complete assignments or prepare for examinations, the workload may be greater. Over-commitment has been a common source of failure for many students. You should take the required workload into account when planning how to balance study with employment and other activities.

Attendance

Regular and punctual attendance at all classes is expected. UNSW regulations state that if students attend less than 80% of scheduled classes they may be refused final assessment.

General Conduct and Behaviour

Consideration and respect for the needs of your fellow students and teaching staff is an expectation. Conduct which unduly disrupts or interferes with a class is not acceptable and students may be asked to leave the class.

Work Health and Safety

UNSW policy requires each person to work safely and responsibly, in order to avoid personal injury and to protect the safety of others.

Special Consideration and Supplementary Examinations

You must submit all assignments and attend all examinations scheduled for your course. You should seek assistance early if you suffer illness or misadventure which affects your course progress. All applications for special consideration must be **lodged online through myUNSW within 3 working days of the assessment**, not to course or school staff. For more detail, consult https://my.unsw.edu.au/student/atoz/SpecialConsideration.html.

Continual Course Improvement

This course is under constant revision in order to improve the learning outcomes for all students. Please forward any feedback (positive or negative) on the course to the course convener or via the Course and Teaching Evaluation and Improvement Process. You can also provide feedback to ELSOC who will raise your concerns at student focus group meetings. As a result of previous feedback obtained for this course and in our efforts to provide a rich and meaningful learning experience, we have continued to evaluate and modify our delivery and assessment methods.

Administrative Matters

On issues and procedures regarding such matters as special needs, equity and diversity, occupational health and safety, enrolment, rights, and general expectations of students, please refer to the School and UNSW policies:
http://www.engineering.unsw.edu.au/electrical-engineering/policies-and-procedures
https://my.unsw.edu.au/student/atoz/ABC.html

Appendix A: Targeted Graduate Capabilities

Electrical Engineering and Telecommunications programs are designed to address the following targeted capabilities which were developed by the school in conjunction with the requirements of professional and industry bodies:

- The ability to apply knowledge of basic science and fundamental technologies;
- The skills to communicate effectively, not only with engineers but also with the wider community;
- The capability to undertake challenging analysis and design problems and find optimal solutions;
- Expertise in decomposing a problem into its constituent parts, and in defining the scope of each part;
- A working knowledge of how to locate required information and use information resources to their maximum advantage;
- Proficiency in developing and implementing project plans, investigating alternative solutions, and critically evaluating differing strategies;
- An understanding of the social, cultural and global responsibilities of the professional engineer;
- The ability to work effectively as an individual or in a team;
- An understanding of professional and ethical responsibilities;
- The ability to engage in lifelong independent and reflective learning.

Appendix B: UNSW Graduate Capabilities

The course delivery methods and course content directly or indirectly addresses a number of core UNSW graduate capabilities, as follows:

- Developing scholars who have a deep understanding of their discipline, through lectures and solution of analytical problems in tutorials and assessed by assignments and written examinations.
- Developing rigorous analysis, critique, and reflection, and ability to apply knowledge and skills to solving problems. These will be achieved by the laboratory experiments and interactive checkpoint assessments and lab exams during the labs.
- Developing capable independent and collaborative enquiry, through a series of tutorials spanning the duration of the course.
- Developing digital and information literacy and lifelong learning skills through assignment work.
- Developing ethical practitioners who are collaborative and effective team workers, through group activities, seminars and tutorials.
- Developing independent, self-directed professionals who are enterprising, innovative, creative and responsive to change, through challenging design and project tasks.
- Developing citizens who can apply their discipline in other contexts, are culturally aware and environmentally responsible, through interdisciplinary tasks, seminars and group activities.

UNSW seeks to develop leaders who are:

- enterprising, innovative and creative
- capable of initiating as well as embracing change
- collaborative team workers

Appendix C: Engineers Australia (EA) Professional Engineer Competency Standard

	Program Intended Learning Outcomes	
PE1: Knowledge and Skill Base	PE1.1 Comprehensive, theory-based understanding of underpinning fundamentals	
	PE1.2 Conceptual understanding of underpinning maths, analysis, statistics, computing	
	PE1.3 In-depth understanding of specialist bodies of knowledge	
	PE1.4 Discernment of knowledge development and research directions	
	PE1.5 Knowledge of engineering design practice	✓
	PE1.6 Understanding of scope, principles, norms, accountabilities of sustainable engineering practice	✓
PE2: Engineering Application Ability	PE2.1 Application of established engineering methods to complex problem solving	✓
	PE2.2 Fluent application of engineering techniques, tools and resources	✓
	PE2.3 Application of systematic engineering synthesis and design processes	✓

	PE2.4 Application of systematic approaches to the conduct and management of engineering projects	✓
PE3: Professional and Personal Attributes	PE3.1 Ethical conduct and professional accountability	
	PE3.2 Effective oral and written communication (professional and lay domains)	✓
	PE3.3 Creative, innovative and pro-active demeanour	✓
	PE3.4 Professional use and management of information	✓
	PE3.5 Orderly management of self, and professional conduct	✓
	PE3.6 Effective team membership and team leadership	✓