## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | +25 | | | |
| | $V_O$ (V) | $V_{IN}$ (V) | $V_{DD}$ (V) | −55 | −40 | +85 | +125 | Min. | Typ. | Max. | |
| Quiescent Device Current, $I_{DD}$ Max. | – | 0,5 | 5 | 0.25 | 0.25 | 7.5 | 7.5 | – | 0.01 | 0.25 | μA |
| | – | 0,10 | 10 | 0.5 | 0.5 | 15 | 15 | – | 0.01 | 0.5 | |
| | – | 0,15 | 15 | 1 | 1 | 30 | 30 | – | 0.01 | 1 | |
| | – | 0,20 | 20 | 5 | 5 | 150 | 150 | – | 0.02 | 5 | |
| Output Low (Sink) Current $I_{OL}$ Min. | 0.4 | 0,5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | – | mA |
| | 0.5 | 0,10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | – | |
| | 1.5 | 0,15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | – | |
| Output High (Source) Current, $I_{OH}$ Min. | 4.6 | 0,5 | 5 | −0.64 | −0.61 | −0.42 | −0.36 | −0.51 | −1 | – | |
| | 2.5 | 0,5 | 5 | −2 | −1.8 | −1.3 | −1.15 | −1.6 | −3.2 | – | |
| | 9.5 | 0,10 | 10 | −1.6 | −1.5 | −1.1 | −0.9 | −1.3 | −2.6 | – | |
| | 13.5 | 0,15 | 15 | −4.2 | −4 | −2.8 | −2.4 | −3.4 | −6.8 | – | |
| Output Voltage: Low-Level, $V_{OL}$ Max. | – | 0,5 | 5 | 0.05 | | | | – | 0 | 0.05 | V |
| | – | 0,10 | 10 | 0.05 | | | | – | 0 | 0.05 | |
| | – | 0,15 | 15 | 0.05 | | | | – | 0 | 0.05 | |
| Output Voltage: High-Level, $V_{OH}$ Min. | – | 0,5 | 5 | 4.95 | | | | 4.95 | 5 | – | |
| | – | 0,10 | 10 | 9.95 | | | | 9.95 | 10 | – | |
| | – | 0,15 | 15 | 14.95 | | | | 14.95 | 15 | – | |
| Input Low Voltage, $V_{IL}$ Max. | 0.5 | – | 5 | 1.5 | | | | — | — | 1.5 | V |
| | 1 | – | 10 | 3 | | | | — | — | 3 | |
| | 1.5 | – | 15 | 4 | | | | — | — | 4 | |
| Input High Voltage, $V_{IH}$ Min. | 0.5,4.5 | – | 5 | 3.5 | | | | 3.5 | — | — | |
| | 1,9 | – | 10 | 7 | | | | 7 | — | — | |
| | 1.5,13.5 | – | 15 | 11 | | | | 11 | — | — | |
| Input Current $I_{IN}$ Max. | | 0,18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | – | $±10^{-5}$ | ±0.1 | μA |

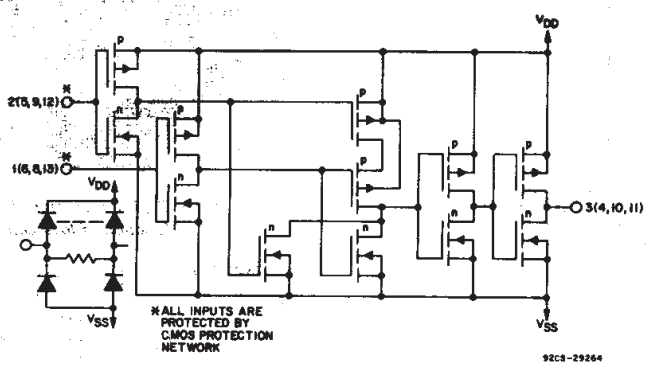


*Fig. 1 – Schematic diagram for CD4081B (1 of 4 identical gates).*

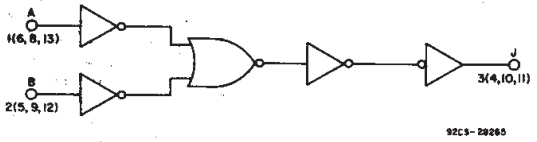


*Fig. 2 – Logic diagram for CD4081B (1 of 4 identical gates).*

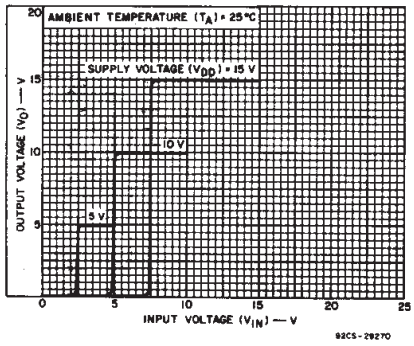


*Fig. 3 – Typical voltage transfer characteristics.*

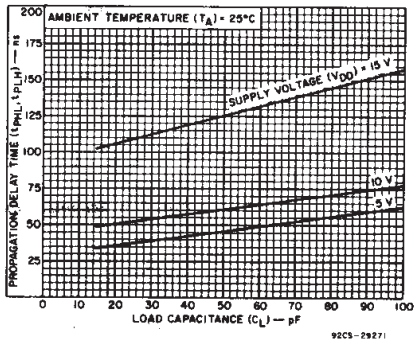


*Fig. 4 – Typical propagation delay time as a function of load capacitance.*

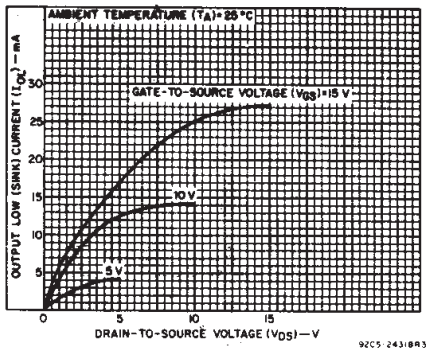


*Fig. 5 – Typical output low (sink) current characteristics.*

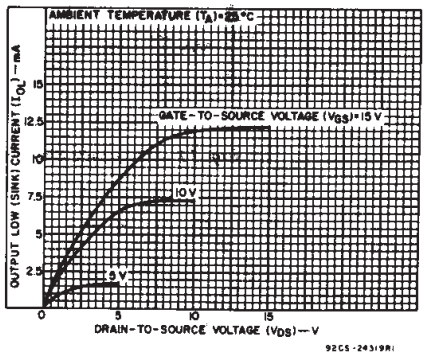


*Fig. 6 – Minimum output low (sink) current characteristics.*