Schematics For Lunzn r68s

RK3568

Main Functions Introduction

1) PMIC: RK809-5+DiscretePower
2) RAM: LPDDR4 1x32Bit 16Gb
3) ROM: eMMC5.1 64Gb
4) Support: 1 x USB3.0 OTG + 1 x USB3.0 HOST
5) Support: 2 x 1Lanes PCIe - 2.5G Ethernet
6) Support: 2 x 10/100/1000 Ethernet(RGMII)
7) Support: 1 x IR Receiver
8) Support: 1 x Power LED,1 x Sytem LED RJ45^LED
9) Support: 1 x Recovery Key
10) Support: Debug UART

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Project	Lunzn_R66s	
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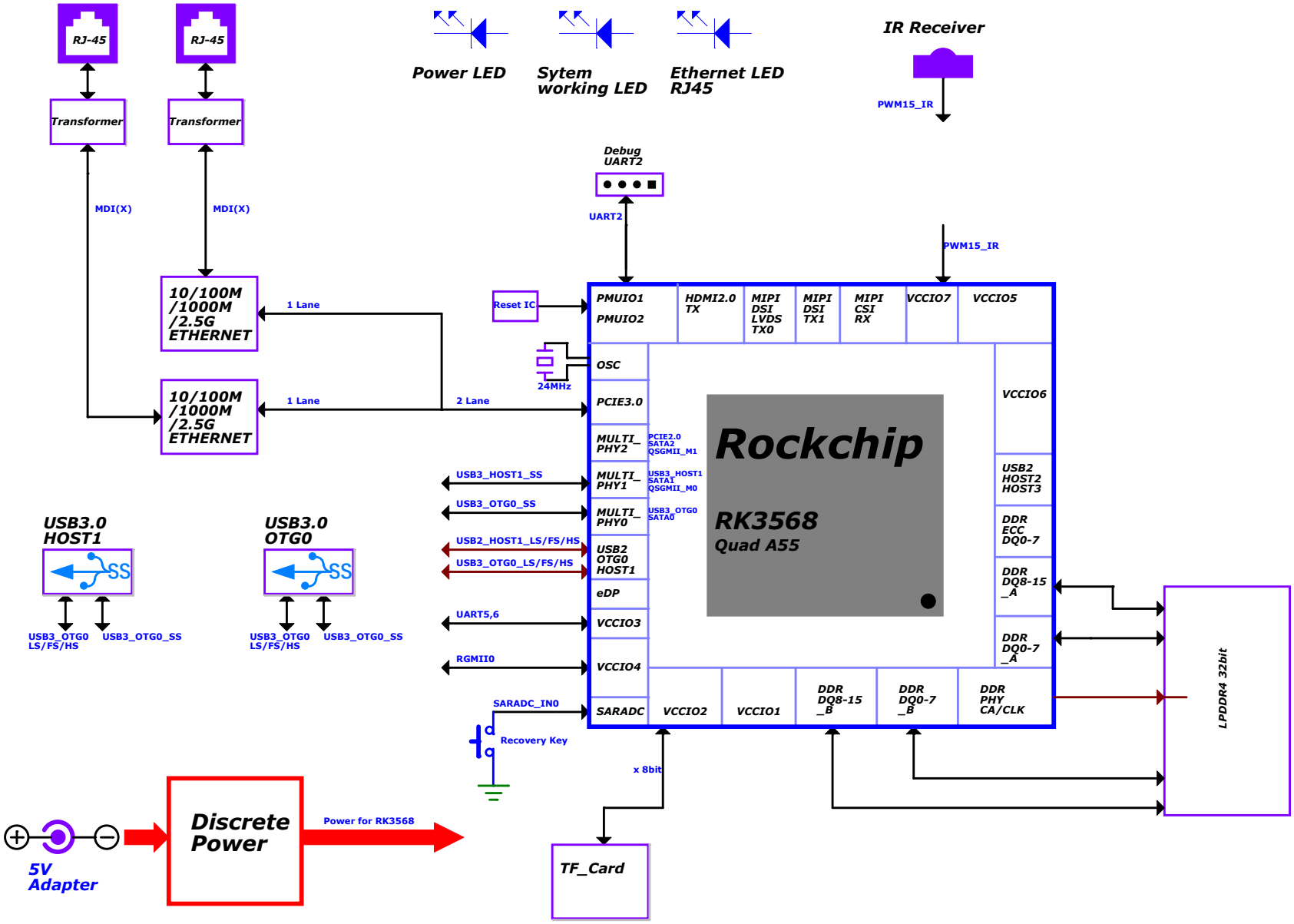
Lunzn r68s Block Diagram



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Project	Lunzn_R66s		
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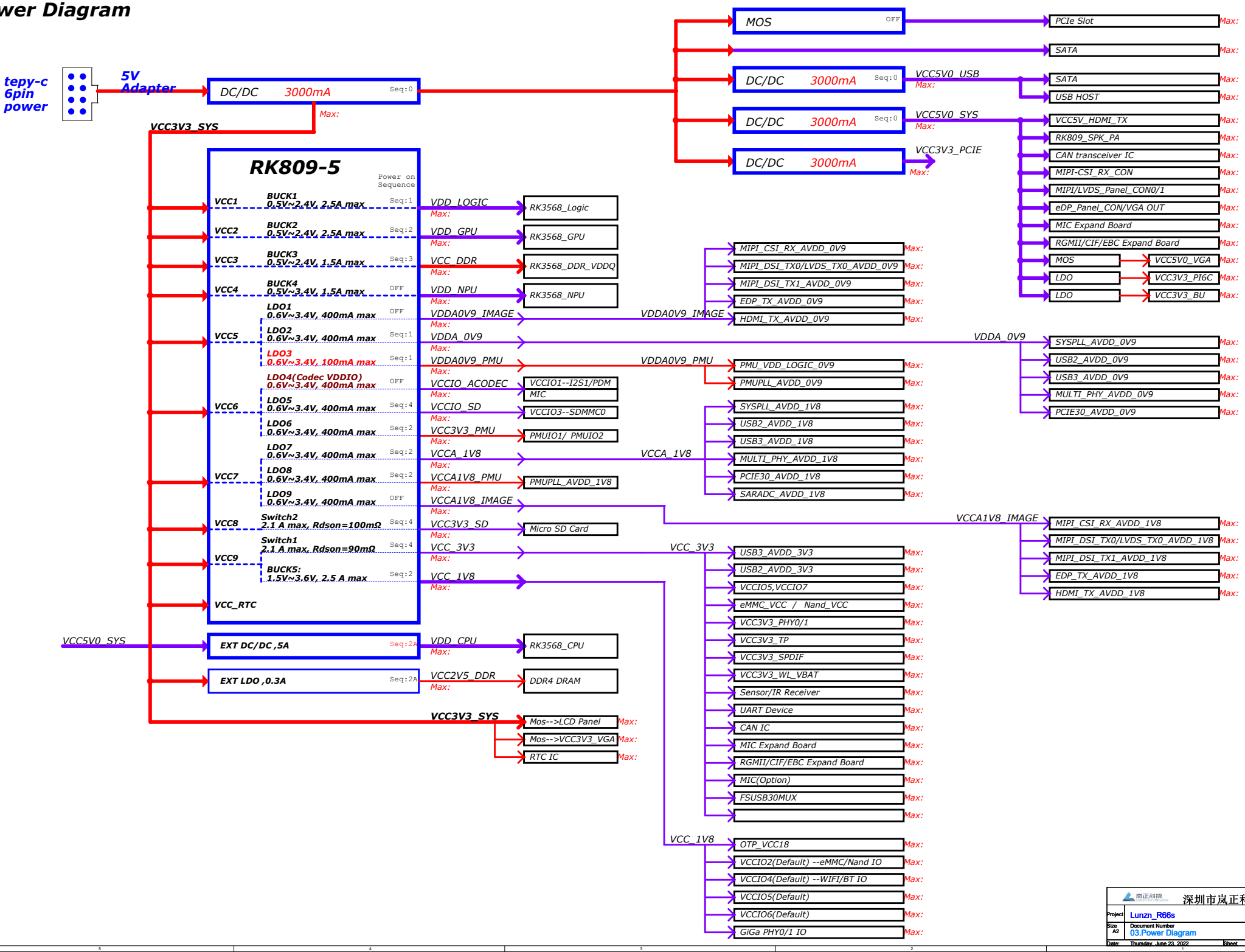
Power Diagram



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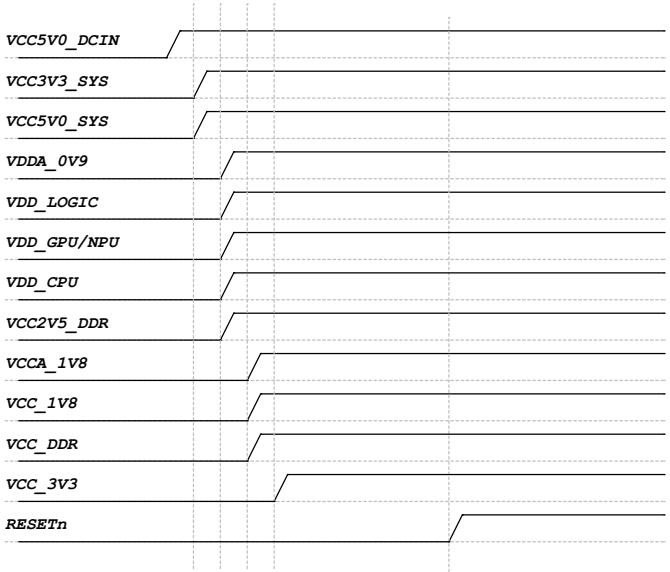
Power Sequence



Power Supply	Channel	Supply Limit	Power Name	Time Slot	Default Voltage
VCC12V_DCIN	BUCK	3.0A	VCC3V3_SYS	Slot:0	3.3V
VCC12V_DCIN	BUCK	3.0A	VCC5V0_SYS	Slot:0	5.2V
VCC3V3_SYS			VCC3V3_PMUIO	Slot:0	3.3V
VCC3V3_SYS	LDO	0.3A	VDDA_0V9	Slot:1	0.9V
VCC3V3_SYS	BUCK	1.5A	VDD_LOGIC	Slot:1	0.9V
VCC3V3_SYS	BUCK	3.0A	VDD_GPU/NPU	Slot:1	0.9V
VCC3V3_SYS	BUCK	5.0A	VDD_CPU	Slot:1	0.9V
VCC3V3_SYS	LDO	0.3A	VCC2V5_DDR	Slot:1	2.5V
VCC3V3_SYS	LDO	0.5A	VCC_1V8	Slot:2	1.8V
VCC3V3_SYS	LDO	0.5A	VCCA_1V8	Slot:2	1.8V
VCC3V3_SYS	BUCK	1.5A	VCC_DDR	Slot:2	1.2V DDR4
VCC3V3_SYS	MOS	2A	VCC_3V3	Slot:3	3.3V
VCC3V3_PMUIO	RESETn				

IO Power Domain Map

Updates must be Revision accordingly!

IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	Pin Y20	✓	✗	VCC_3V3	VCC_3V3	3.3V	
PMUIO2	Pin W19	✓	✓	VCC_3V3	VCC_3V3	3.3V	
VCCIO1	Pin H17	✓	✓	VCC_3V3	VCC_3V3	3.3V	
VCCIO2	Pin H18	✓	✓	VCCIO_FLASH	VCC_1V8	1.8V	PIN "FLASH_VOL_SEL" must be logic High if VCCIO_FLASH=3.3V,FLASH_VOL_SEL must be logic low
VCCIO3	Pin L22	✓	✓	VCC_3V3	VCC_3V3	3.3V	
VCCIO4	Pin J21	✓	✓	VCC_1V8	VCC_1V8	1.8V	
VCCIO5	Pin V10 Pin V11	✓	✓	VCC_3V3	VCC_3V3	3.3V	
VCCIO6	Pin R9 Pin U9	✓	✓	VCC_1V8	VCC_1V8	1.8V	
VCCIO7	Pin V12	✓	✓	VCC_3V3	VCC_3V3	3.3V	

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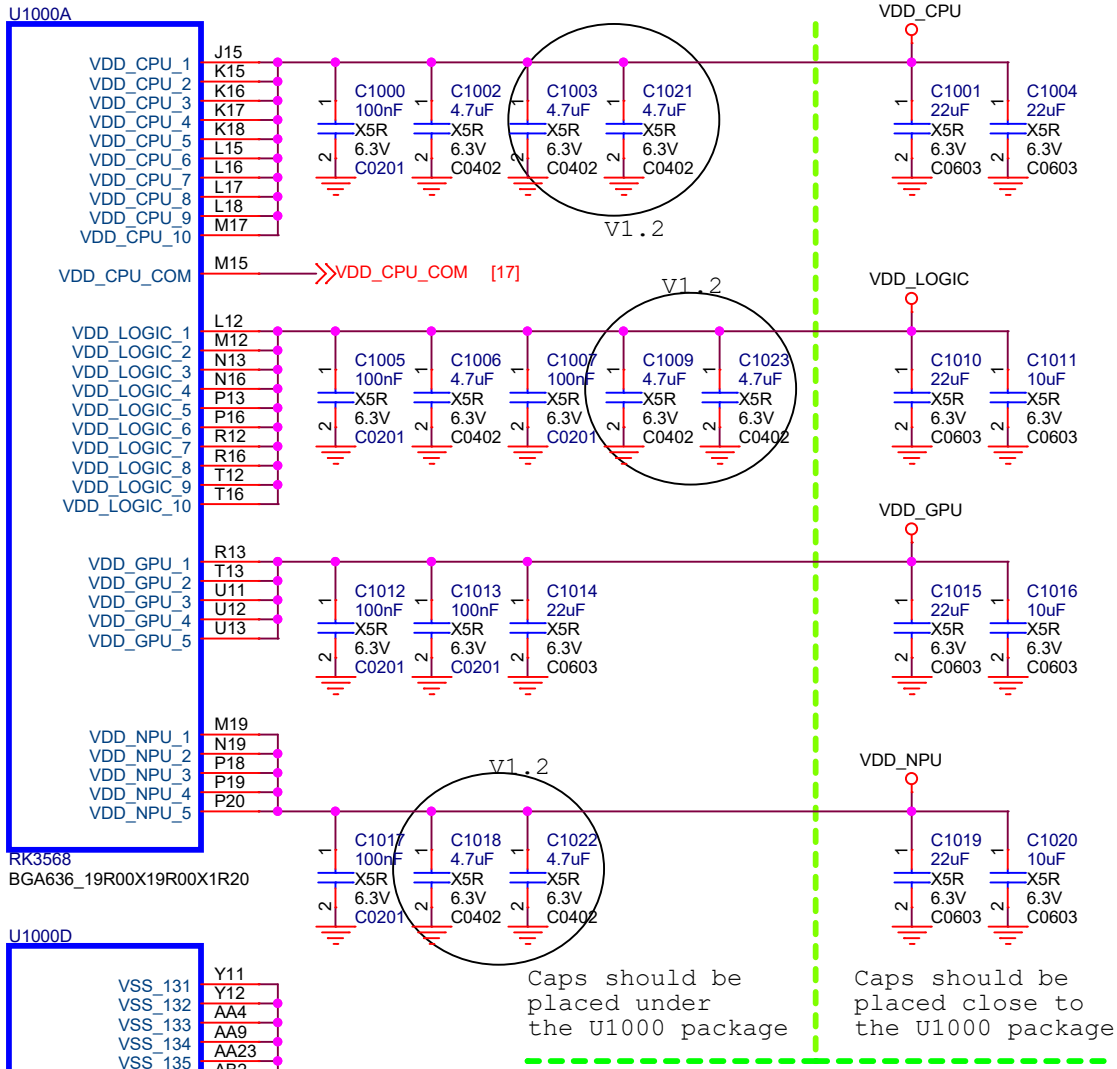
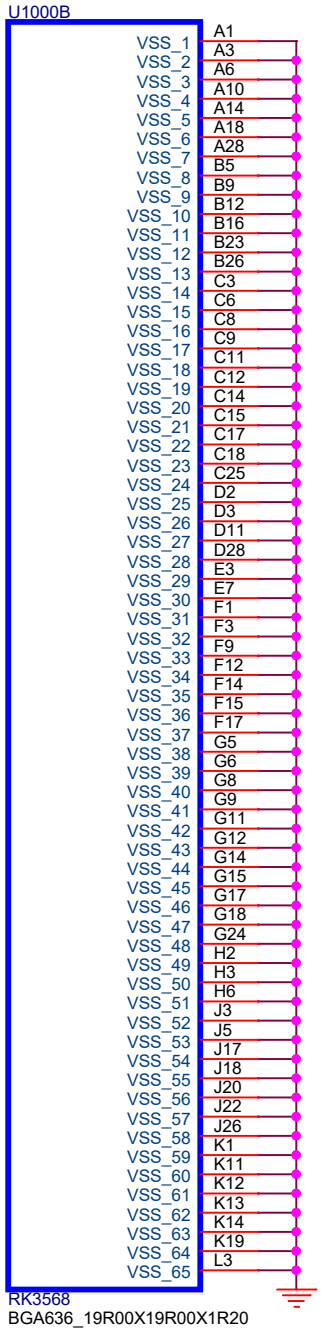
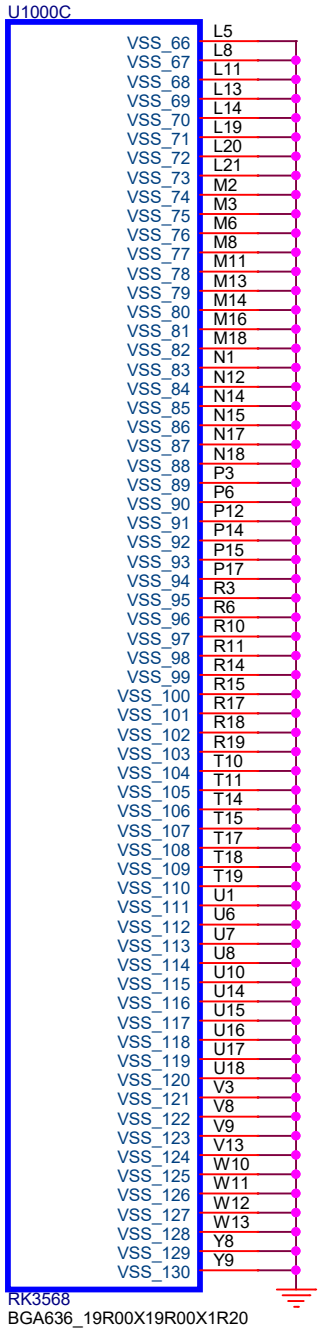
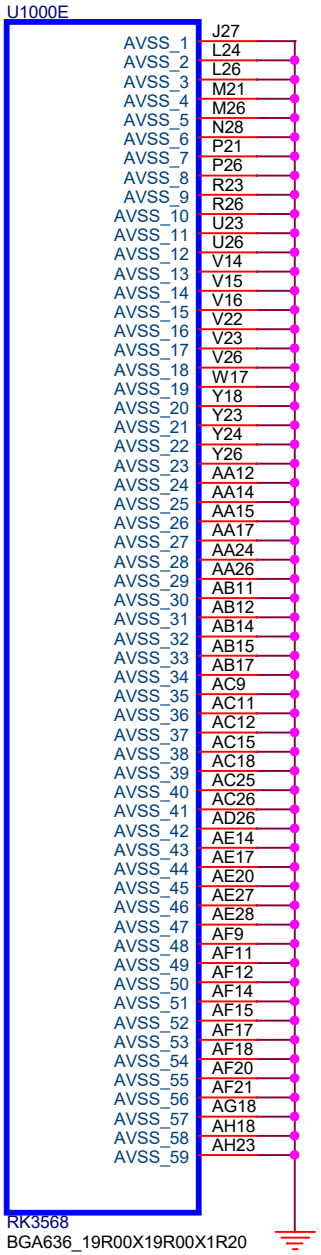
RK3568_ABCDE (Power&Gnd)









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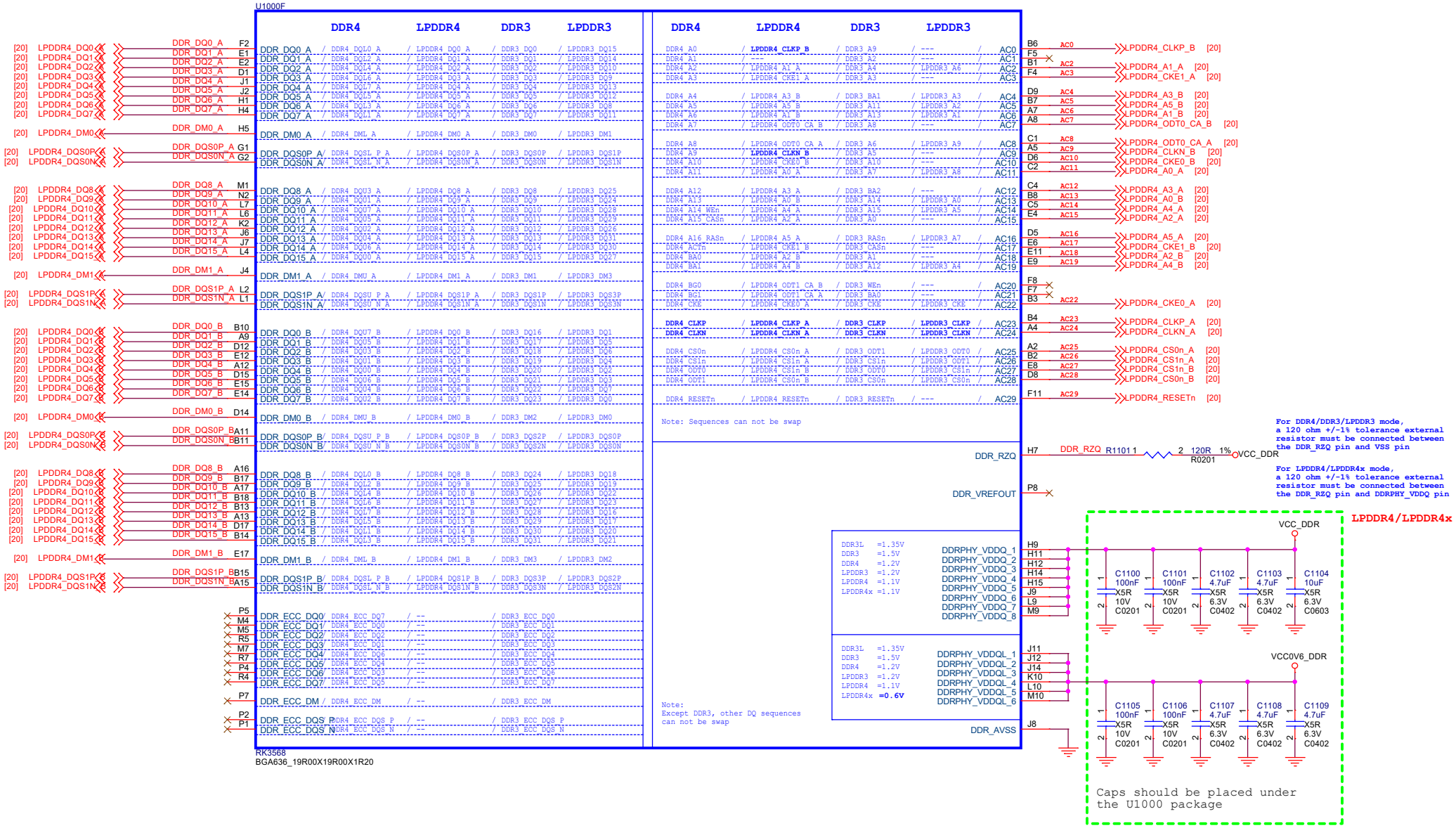
RK3568_F (DDR PHY)



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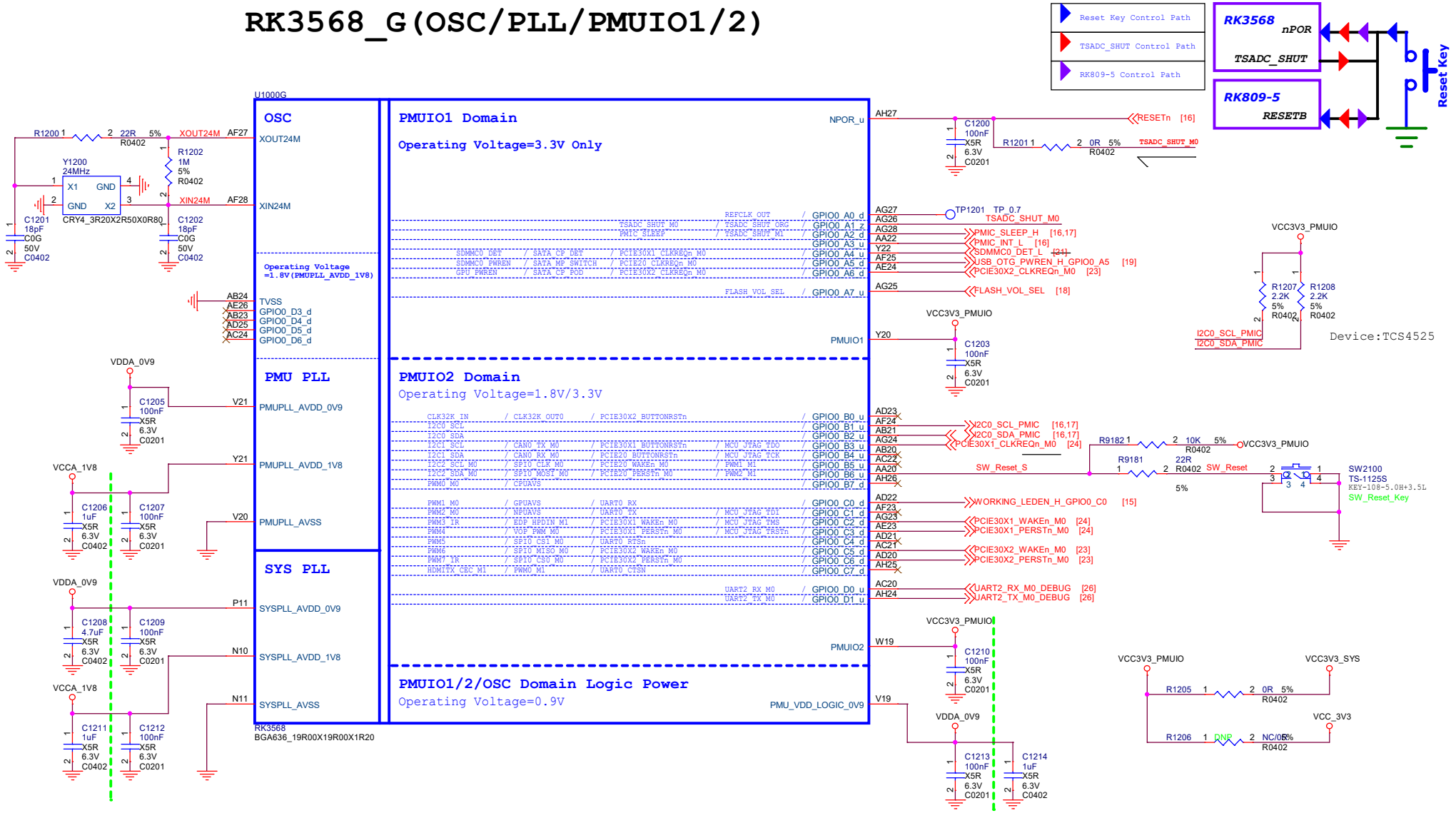
RK3568_G(OSC/PLL/PMUIO1/2)



Company	深圳市岚正科技有限公司
Project	Lunzn_R66s
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RK3568_I(VCCIO2 Domain)

U1000I

VCCIO2 Domain

Operating Voltage=1.8V/3.3V

EMMC_D0	/ FLASH_D0	/ GPIO1_B4_u	A24	
EMMC_D1	/ FLASH_D1	/ GPIO1_B5_u	C21	
EMMC_D2	/ FLASH_D2	/ GPIO1_B6_u	B24	
EMMC_D3	/ FLASH_D3	/ GPIO1_B7_u	D21	
EMMC_D4	/ FLASH_D4	/ GPIO1_C0_u	A25	
EMMC_D5	/ FLASH_D5	/ GPIO1_C1_u	E21	
EMMC_D6	/ FLASH_D6	/ GPIO1_C2_u	E22	
EMMC_D7	/ FLASH_D7	/ GPIO1_C3_u	B25	
EMMC_CMD	/ FLASH_WRn	/ GPIO1_C4_u	B22	
EMMC_CLKOUT	/ FLASH_DQS	/ GPIO1_C5_d	A23	
EMMC_DATA_STROBE	/ FSPI_CS1n / FLASH_CLE	/ GPIO1_C6_d	A26	
EMMC_RSTn	/ FSPI_D2 / FLASH_WPn	/ GPIO1_C7_d	F20	
	FSPI_CLK / FLASH_ALE	GPIO1_D0_d	A22	
	FSPI_D0 / FLASH_RDY	GPIO1_D1_u	C24	
	FSPI_D1 / FLASH_RDn	GPIO1_D2_u	D23	
	FSPI_CS0n / FLASH_CS0n	GPIO1_D3_u	C23	
	FSPI_D3 / FLASH_CS1n	GPIO1_D4_u	A27	

Default is determined by Pin
FLASH_VOL_SEL/GPIO0_A7_u:
L:VCCIO2 must supply 3.3V
H:VCCIO2 must supply 1.8V

VCCIO2 H18

VCCIO_FLASH

C1300
100nF
X5R
6.3V
C0201

RK3568
BGA636_19R00X19R00X1R20

RK3568_J(VCCIO3 Domain)

U1000J

VCCIO3 Domain

Operating Voltage=1.8V/3.3V

SDMMC0_D0	/ UART2_TX_M1 / UART6_TX_M1	/ PWM8_M1	/ GPIO1_D5_u	J25	SDMMC0_D0 [21]
SDMMC0_D1	/ UART2_RX_M1 / UART6_RX_M1	/ PWM9_M1	/ GPIO1_D6_u	J24	SDMMC0_D1 [21]
SDMMC0_D2	/ ARMJTAG_TCK / UART3_CTSn_M0		/ GPIO1_D7_u	H26	SDMMC0_D2 [21]
SDMMC0_D3	/ ARMJTAG_TMS / UART3_RTSn_M0		/ GPIO2_A0_u	J23	SDMMC0_D3 [21]
SDMMC0_CMD	/ PWM10_M1 / UART5_RX_M0	/ CAN0_TX_M1	/ GPIO2_A1_u	H27	SDMMC0_CMD [21]
SDMMC0_CLK	/ TEST_CLKOUT / UART5_TX_M0	/ CAN0_RX_M1	/ GPIO2_A2_d	H28	SDMMC0_CLK [21]

VCCIO3 L22

VCCIO_SD

C1301
100nF
X5R
6.3V
C0201

RK3568
BGA636_19R00X19R00X1R20

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

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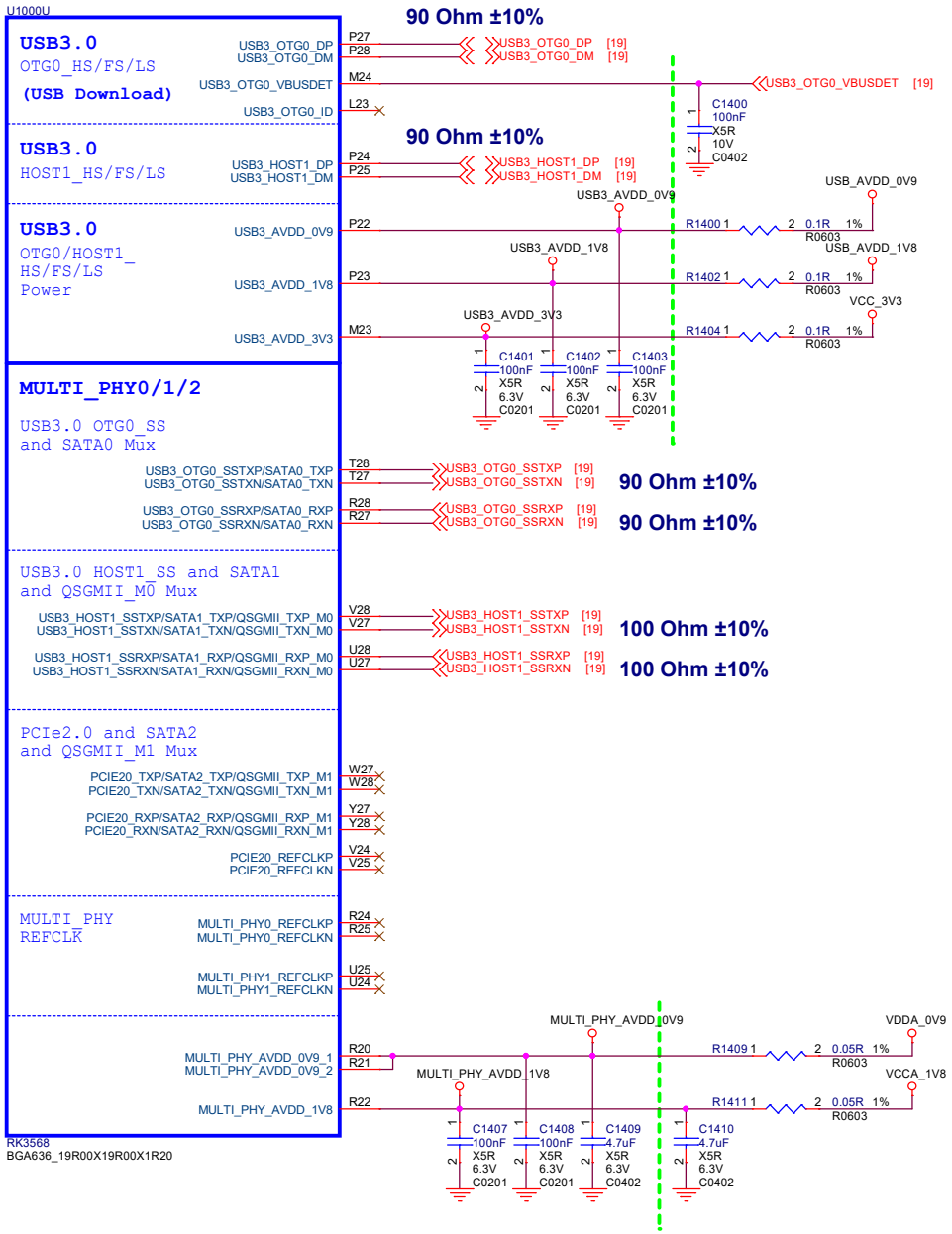
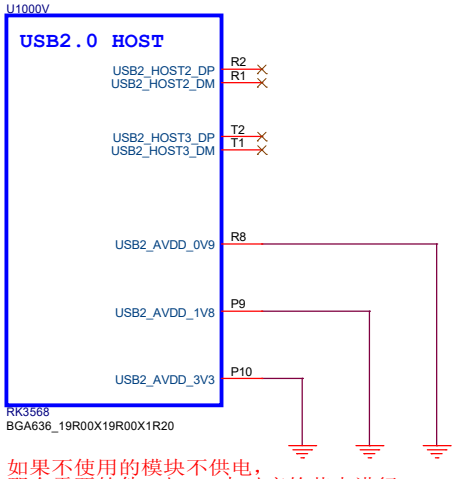
RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)



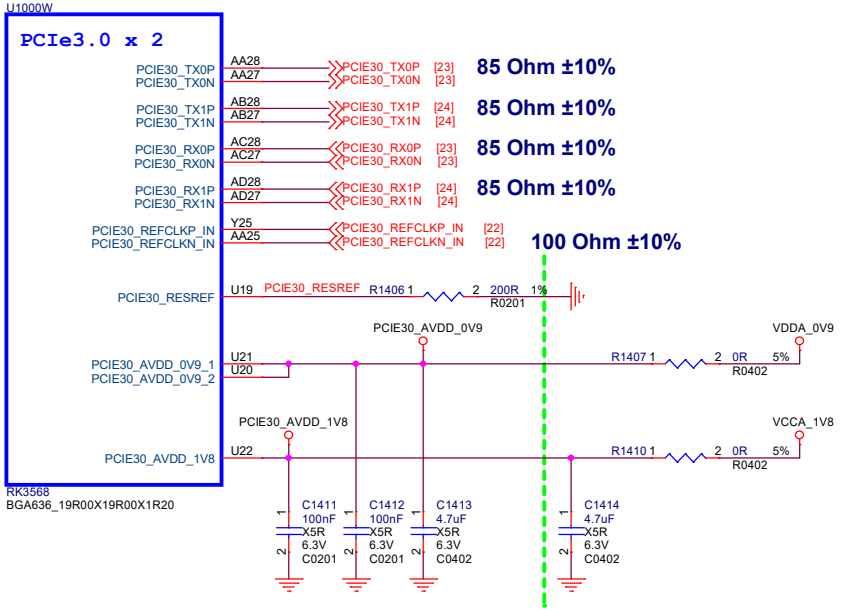
Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_V(USB2.0 HOST)



如果不使用的模块不供电，
那么需要软件 对DTS 中对应的节点进行 disable isable 配置 ，
否则 可能 会 引起内核初始化卡死现象。

RK3568_W(PCIe3.0 x2)



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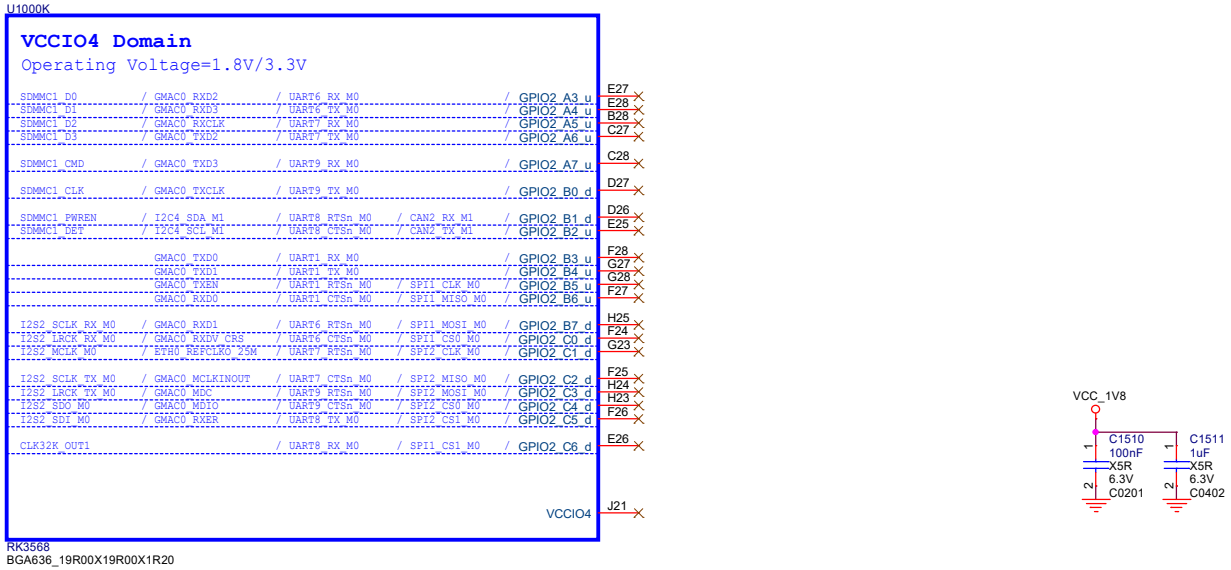
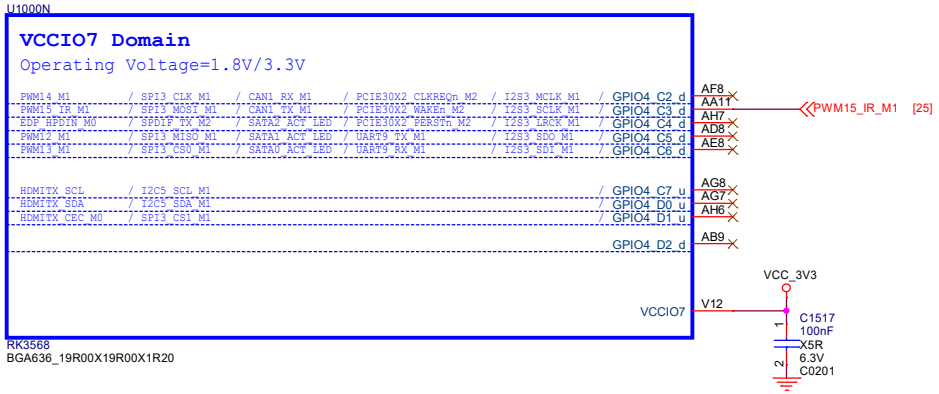
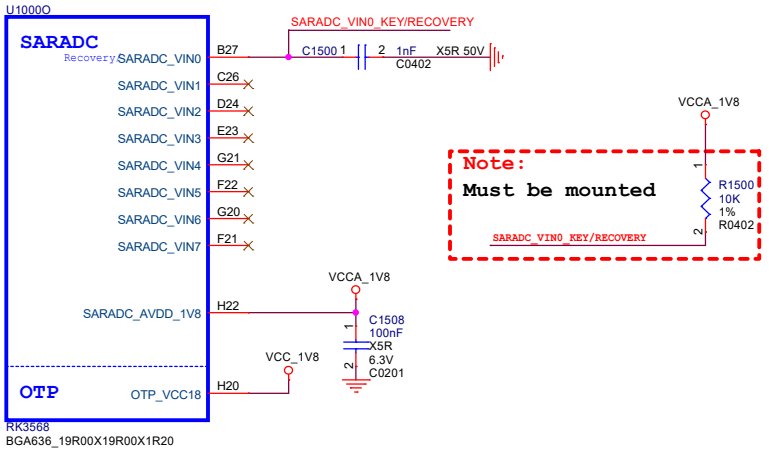
RK3568_K(VCCIO4 Domain)



RK3568_N(VCCIO7 Domain)



RK3568_O(SARADC/OTP)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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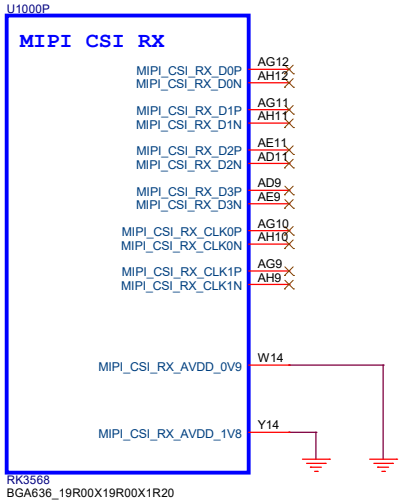
RK3568_P(MIPI_CSI_RX)



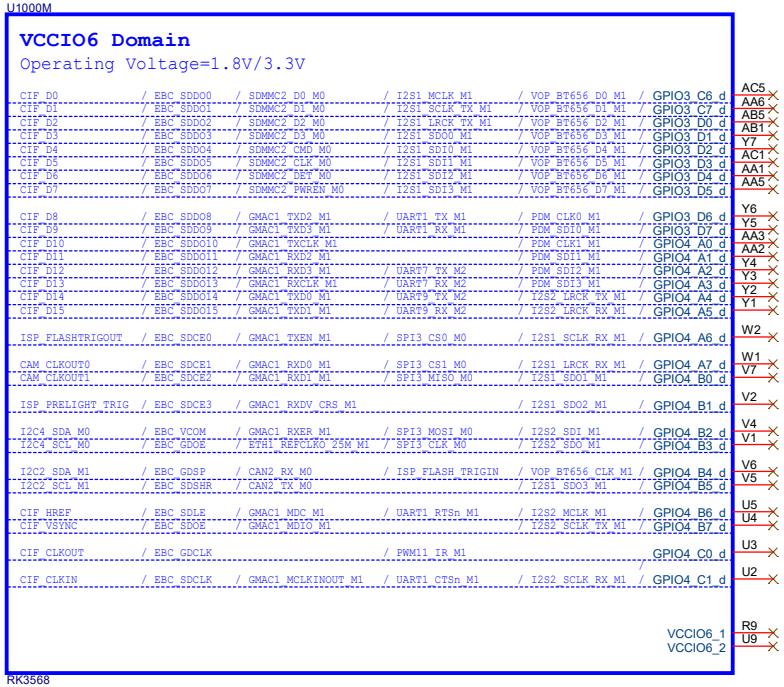
Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

如果不使用的模块不供电，
那么需要软件 对DTS 中对应的节点进行 disable isable 配置 ，
否则 可能 会 引起内核初始化卡死现象。

Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

RK3568_M(VCCIO6 Domain)



Note:

Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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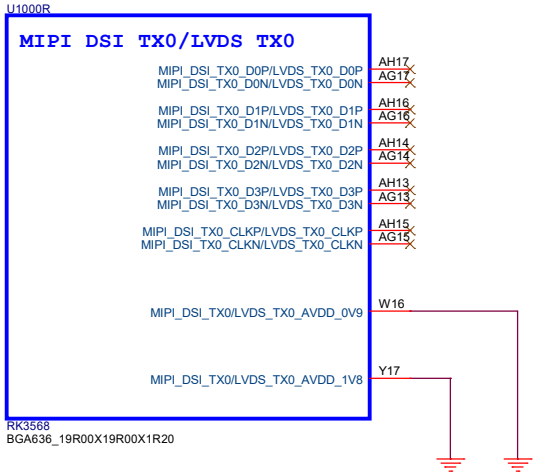
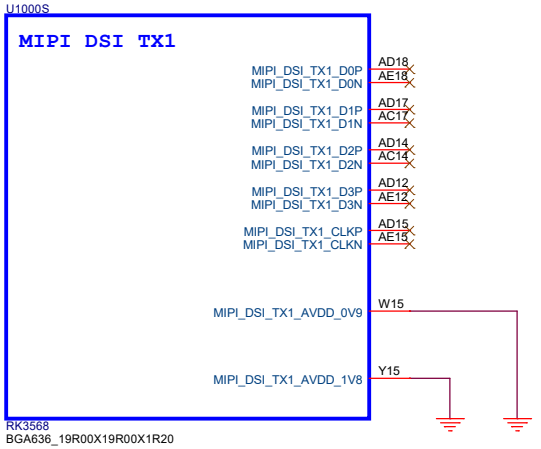
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



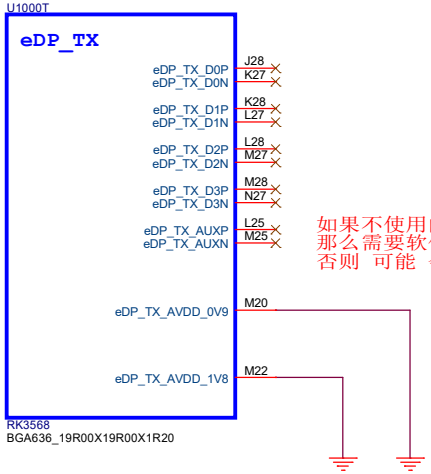
如果不使用的模块不供电，
那么需要软件 对DTS 中对应的节点进行 disable isable 配置 ，
否则 可能 会 引起内核初始化卡死现象。

RK3568_S(MIPI_DSI_TX1)



如果不使用的模块不供电，
那么需要软件 对DTS 中对应的节点进行 disable isable 配置 ，
否则 可能 会 引起内核初始化卡死现象。

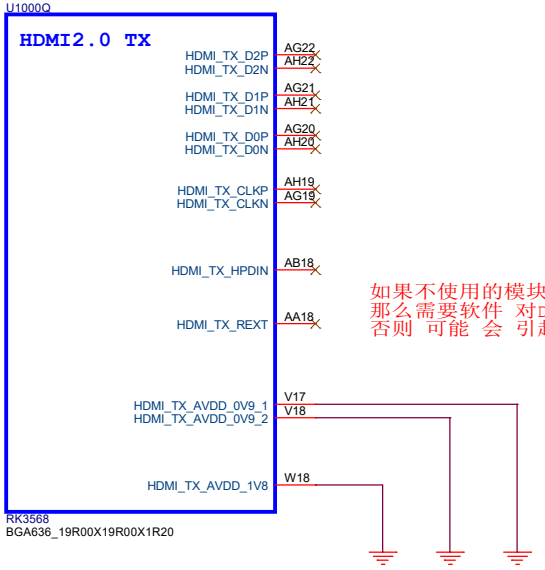
RK3568_T(eDP TX)



如果不使用的模块不供电，
那么需要软件 对DTS 中对应的节点进行 disable isable 配置 ，
否则 可能 会 引起内核初始化卡死现象。

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_Q(HDMI2.0 TX)



如果不使用的模块不供电，
那么需要软件 对DTS 中对应的节点进行 disable isable 配置 ，
否则 可能 会 引起内核初始化卡死现象。

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RK3568_L(VCCIO5 Domain)

U1000L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0	VOP_BT656_D0_M0	SPI0_MISO_M1	PCIE20_CLKREQn_M1	I2S1_MCLK_M2	GPIO2_D0_d	AG6
LCDC_D1	VOP_BT656_D1_M0	SPI0_MOSI_M1	PCIE20_WAKEn_M1	I2S1_SCLK_TX_M2	GPIO2_D1_d	AD7
LCDC_D2	VOP_BT656_D2_M0	SPI0_CS0_M1	PCIE30X1_CLKREQn_M1	I2S1_LRCK_TX_M2	GPIO2_D2_d	AC8
LCDC_D3	VOP_BT656_D3_M0	SPI0_CLK_M1	PCIE30X1_WAKEn_M1	I2S1_SDI0_M2	GPIO2_D3_d	AC7
LCDC_D4	VOP_BT656_D4_M0	SPI2_CS1_M1	PCIE30X2_CLKREQn_M1	I2S1_SDI1_M2	GPIO2_D4_d	AF5
LCDC_D5	VOP_BT656_D5_M0	SPI2_CS0_M1	PCIE30X2_WAKEn_M1	I2S1_SDI2_M2	GPIO2_D5_d	AF6
LCDC_D6	VOP_BT656_D6_M0	SPI2_MOSI_M1	PCIE30X2_PERSTn_M1	I2S1_SDI3_M2	GPIO2_D6_d	AD6
LCDC_D7	VOP_BT656_D7_M0	SPI2_MISO_M1	UART8_TX_M1	I2S1_SDO0_M2	GPIO2_D7_d	AH5
LCDC_CLK	VOP_BT656_CLK_M0	SPI2_CLK_M1	UART8_RX_M1	I2S1_SDO1_M2	GPIO3_A0_d	AH4
LCDC_D8	VOP_BT1120_D0	SPI1_CS0_M1	PCIE30X1_PERSTn_M1	SDMMC2_D0_M1	GPIO3_A1_d	AB8
LCDC_D9	VOP_BT1120_D1	GMAC1_TXD2_M0	I2S3_MCLK_M0	SDMMC2_D1_M1	GPIO3_A2_d	AE5
LCDC_D10	VOP_BT1120_D2	GMAC1_TXD3_M0	I2S3_SCLK_M0	SDMMC2_D2_M1	GPIO3_A3_d	AG4
LCDC_D11	VOP_BT1120_D3	GMAC1_RXD2_M0	I2S3_LRCK_M0	SDMMC2_D3_M1	GPIO3_A4_d	AF4
LCDC_D12	VOP_BT1120_D4	GMAC1_RXD3_M0	I2S3_SDO_M0	SDMMC2_CMD_M1	GPIO3_A5_d	AH3
LCDC_D13	VOP_BT1120_CLK	GMAC1_TXCLK_M0	I2S3_SDI_M0	SDMMC2_CLK_M1	GPIO3_A6_d	AG3
LCDC_D14	VOP_BT1120_D5	GMAC1_RXCLK_M0		SDMMC2_DET_M1	GPIO3_A7_d	AH2
LCDC_D15	VOP_BT1120_D6	ETH1_REFCLKO_25M_M0		SDMMC2_PWREN_M1	GPIO3_B0_d	AG2
LCDC_D16	VOP_BT1120_D7	GMAC1_RXD0_M0	UART4_RX_M1	PWM8_M0	GPIO3_B1_d	AG1
LCDC_D17	VOP_BT1120_D8	GMAC1_RXD1_M0	UART4_TX_M1	PWM9_M0	GPIO3_B2_d	AF2
LCDC_D18	VOP_BT1120_D9	GMAC1_RXDV_CRS_M0	I2C5_SCL_M0	PDM_SDI0_M2	GPIO3_B3_d	AF1
LCDC_D19	VOP_BT1120_D10	GMAC1_RXER_M0	I2C5_SDA_M0	PDM_SDI1_M2	GPIO3_B4_d	AE1
LCDC_D20	VOP_BT1120_D11	GMAC1_TXD0_M0	I2C3_SCL_M1	PWM10_M0	GPIO3_B5_d	AE2
LCDC_D21	VOP_BT1120_D12	GMAC1_TXD1_M0	I2C3_SDA_M1	PWM11_IR_M0	GPIO3_B6_d	AE3
LCDC_D22	PWM12_M0	GMAC1_TXEN_M0	UART3_TX_M1	PDM_SDI2_M2	GPIO3_B7_d	AD4
LCDC_D23	PWM13_M0	GMAC1_MCLKINOUT_M0	UART3_RX_M1	PDM_SDI3_M2	GPIO3_C0_d	AD2
LCDC_HSYNC	VOP_BT1120_D13	SPI1_MOSI_M1	PCIE20_PERSTn_M1	I2S1_SDO2_M2	GPIO3_C1_d	AD1
LCDC_VSYNC	VOP_BT1120_D14	SPI1_MISO_M1	UART5_TX_M1	I2S1_SDO3_M2	GPIO3_C2_d	AA7
LCDC_DEN	VOP_BT1120_D15	SPI1_CLK_M1	UART5_RX_M1	I2S1_SCLK_RX_M2	GPIO3_C3_d	AC4
PWM14_M0	VOP_PWM_M1	GMAC1_MDC_M0	UART7_TX_M1	PDM_CLK1_M2	GPIO3_C4_d	AC3
PWM15_IR_M0	SPDIF_TX_M1	GMAC1_MDIO_M0	UART7_RX_M1	I2S1_LRCK_RX_M2	GPIO3_C5_d	AC2
					VCCIO5_1	V10
					VCCIO5_2	V11

RK3568
BGA636_19R00X19R00X1R20

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

岚正科技 LUNZN TECHNOLOGY	深圳市岚正科技有限公司		
Project	Lunzn_R66s		
Size A4	Document Number 13.RK3568_VO Interface_2		Rev V1.1
Date: Thursday, June 23, 2022	Sheet 13 of 27		

RK3568_H(VCCIO1 Domain)

U1000H

VCCIO1 Domain

Operating Voltage=1.8V/3.3V

I2C3_SDA_M0	/ UART3_RX_M0	/ CAN1_RX_M0		/ AUDIOPWM_LOUT_P	/ ACODEC_ADC_DATA	/ GPIO1_A0_u
I2C3_SCL_M0	/ UART3_TX_M0	/ CAN1_TX_M0		/ AUDIOPWM_LOUT_N	/ ACODEC_ADC_CLK	/ GPIO1_A1_u
I2S1_MCLK_M0	/ UART3_RTSn_M0	/ SCR_CLK	/ PCIE30X1_PERSTn_M2			/ GPIO1_A2_d
I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ SCR_IO	/ PCIE30X1_WAKEn_M2		/ ACODEC_DAC_CLK	/ GPIO1_A3_d
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0		/ SPDIF_TX_M0		/ GPIO1_A4_d
I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ SCR_RST	/ PCIE30X1_CLKREQn_M2		/ ACODEC_DAC_SYNC	/ GPIO1_A5_d
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0		/ AUDIOPWM_ROUT_P		/ GPIO1_A6_d
I2S1_SDO0_M0	/ UART4_CTSn_M0	/ SCR_DET		/ AUDIOPWM_ROUT_N	/ ACODEC_DAC_DATAL	/ GPIO1_A7_d
I2S1_SDO1_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0	/ PCIE20_CLKREQn_M2		/ ACODEC_DAC_DATAR	/ GPIO1_B0_d
I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_WAKEn_M2		/ ACODEC_ADC_SYNC	/ GPIO1_B1_d
I2S1_SDO3_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_PERSTn_M2			/ GPIO1_B2_d
	I2S1_SDI0_M0	/ PDM_SDI0_M0				/ GPIO1_B3_d

D18	
E18	
A19	
B19	
F18	
A20	
C20	
B20	
D20	
E20	
A21	
B21	
VCCIO1	H17

RK3568

BGA636_19R00X19R00X1R20

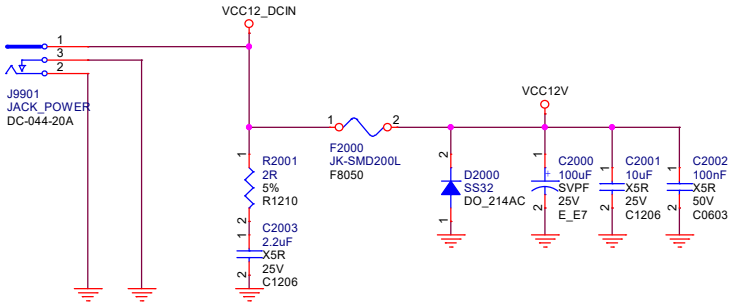
Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

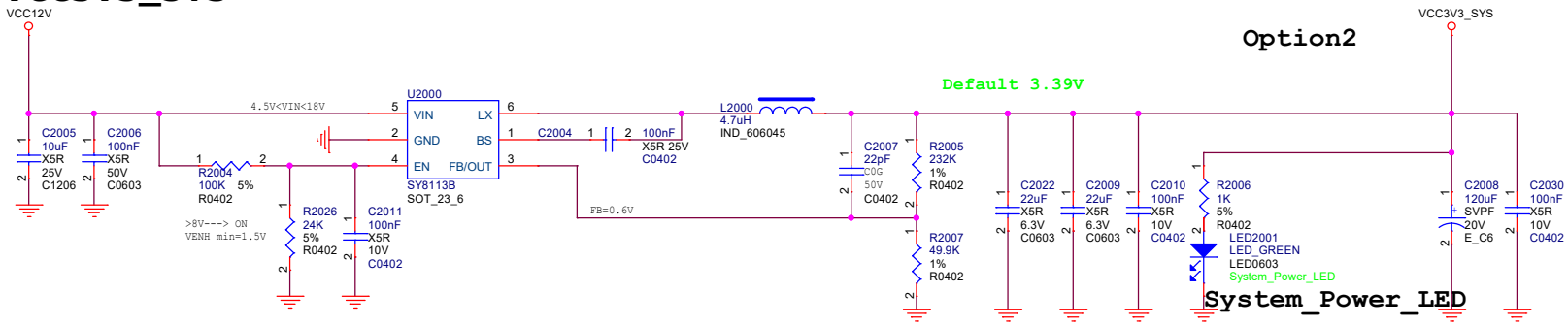
岚正科技 LUNZN TECHNOLOGY 深圳市岚正科技有限公司

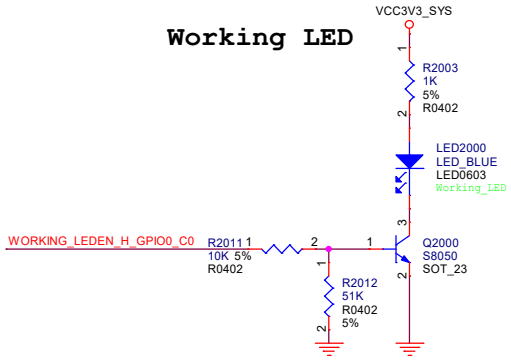
Project	Lunzn_R66s		
Size A4	Document Number 14.RK3568_Audio Interface		Rev V1.1
Date: Thursday, June 23, 2022	Sheet 14 of 27		

DC_IN

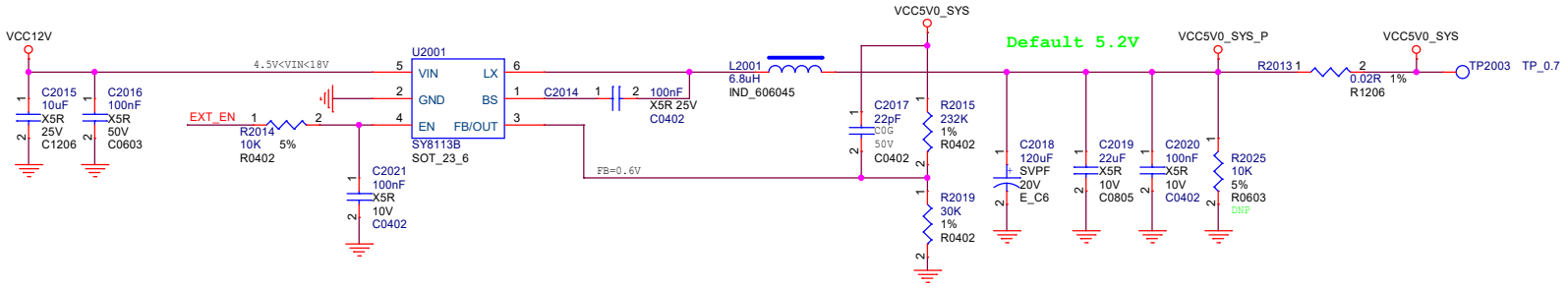


VCC3V3_SYS





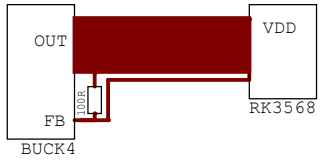
VCC5V0_SYS



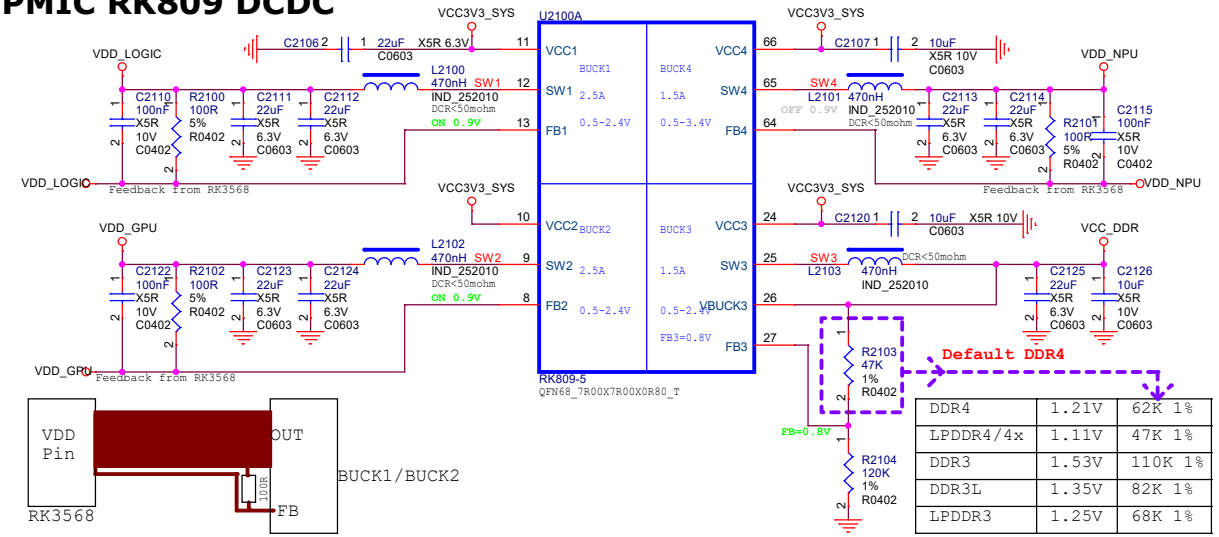
VCC5V0_USB

岚正科技 LUNZN TECHNOLOGY	深圳市岚正科技有限公司	
Project	Lunzn_R66s	
Size A3	Document Number 15.Power_DC IN	Rev V1.1
Date: Thursday, June 23, 2022	Sheet 15 of 27	

I2C0_SCL_PMIC [7,17]
I2C0_SDA_PMIC [7,17]
PMIC_INT_L [7]
PMIC_SLEEP_H [7,17]
RESETn [7]
RK809_PWRON
EXT_EN [15]

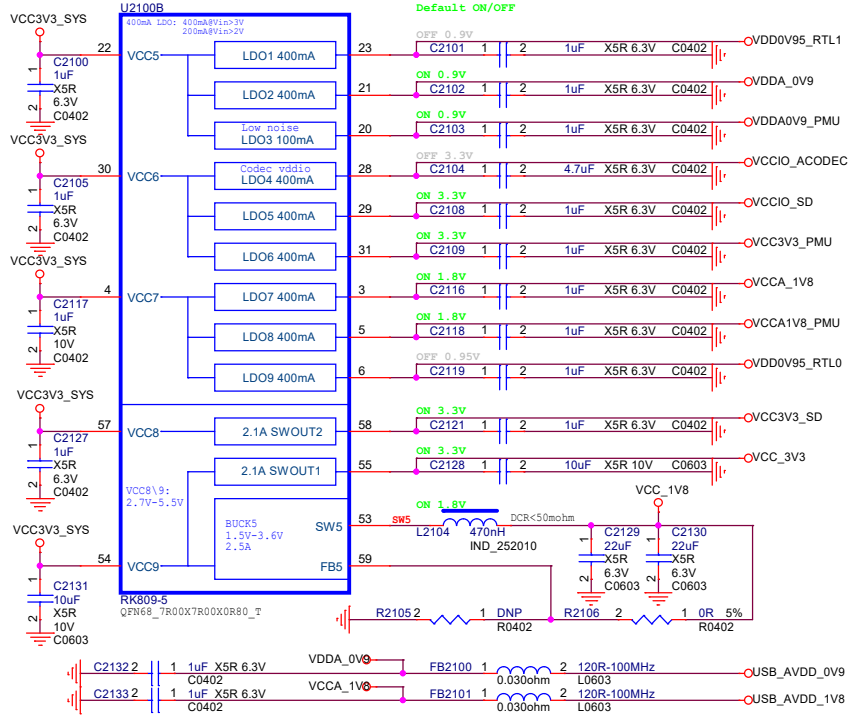


PMIC RK809 DCDC

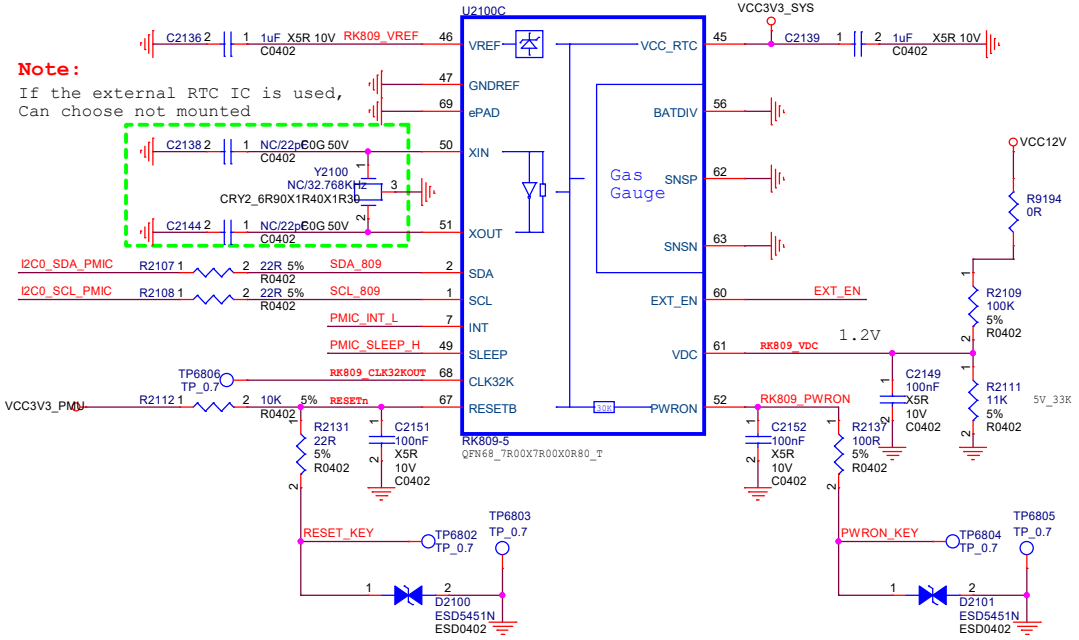


DDR4	1.21V	62K 1%
LPDDR4/4x	1.11V	47K 1%
DDR3	1.53V	110K 1%
DDR3L	1.35V	82K 1%
LPDDR3	1.25V	68K 1%

PMIC RK809 LDO

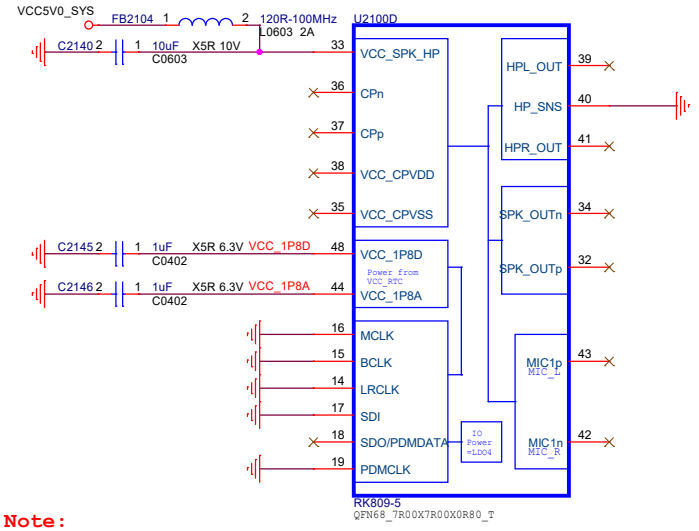


PMIC RK809 Managerment



Note:
If the external RTC IC is used,
Can choose not mounted

PMIC RK809 CODEC

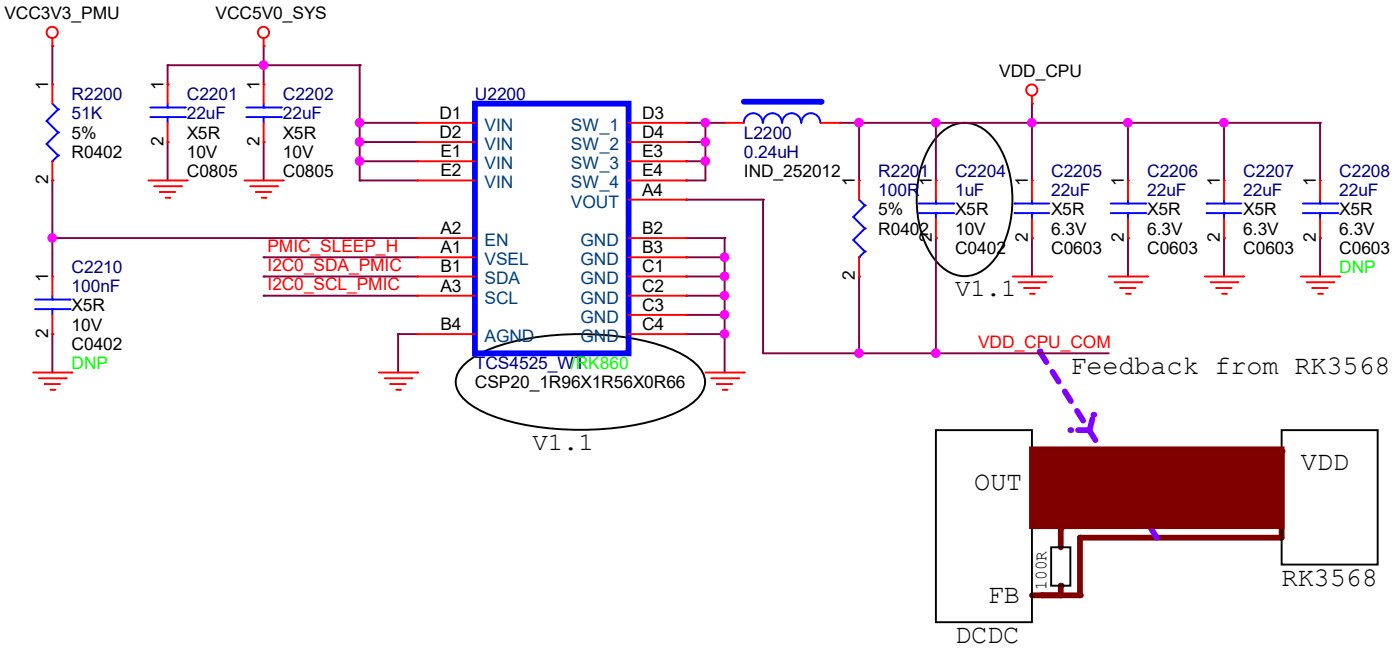


Note:
If RK809-5 codec is not used,
then Pin 14,15,16,17,19,40 Tie VSS
Pin 18,36,37,38,35,39,41,34,32,43,42
Leave floating

深圳市岚正科技有限公司			
Project	Lunzn_R66s		
Size A3	Document Number 16.Power_PMIC		Rev V1.1
Date: Thursday, June 23, 2022	Sheet 16 of 27		

I2C0_SCL_PMIC [7,16]
I2C0_SDA_PMIC [7,16]
PMIC_SLEEP_H [7,16]
VDD_CPU_COM [5]

VDD_CPU

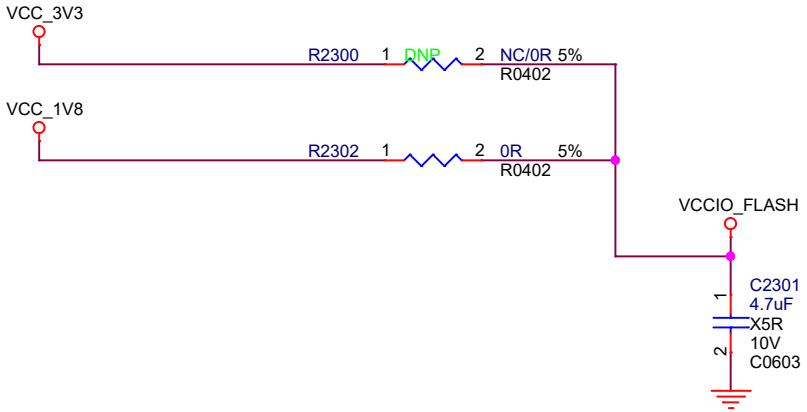


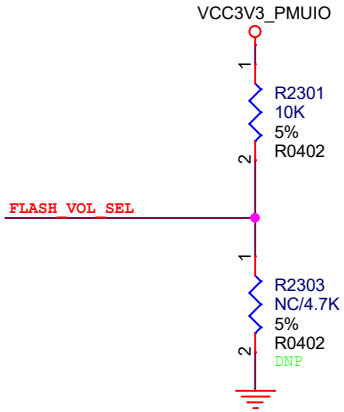
深圳市岚正科技有限公司		
Project	Lunzn_R66s	
Size A4	Document Number 17.Power_CPU	Rev V1.1
Date: Thursday, June 23, 2022	Sheet 17 of 27	

FLASH_VOL_SEL [7]

Flash Power Manage

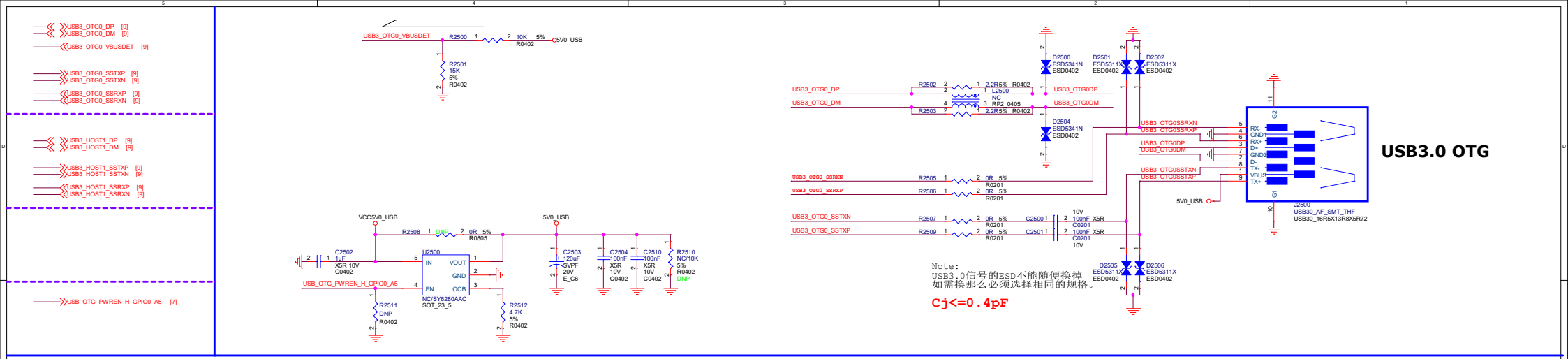
	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)



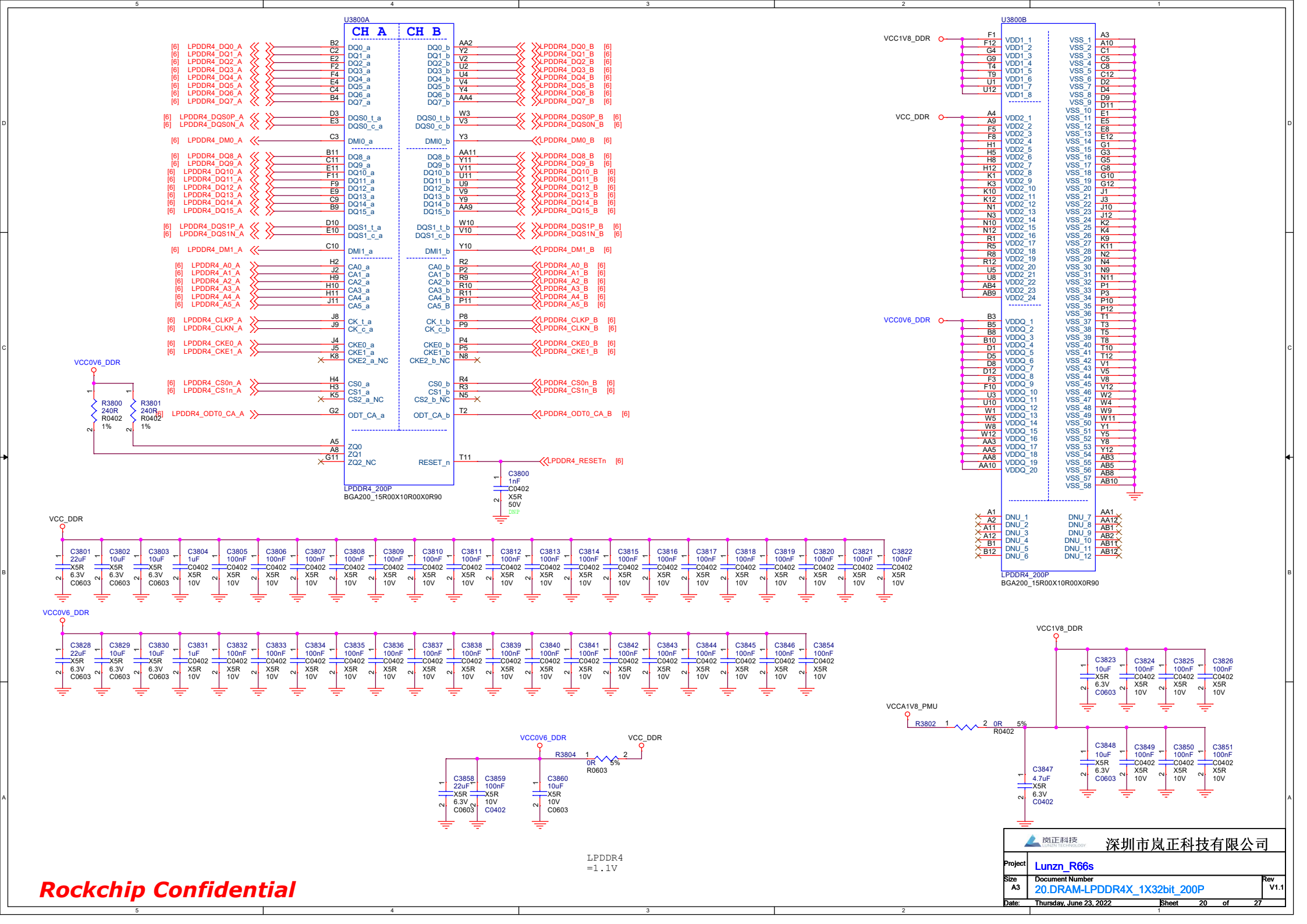


Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

岚正科技 LUNZN TECHNOLOGY 深圳市岚正科技有限公司			
Project	Lunzn_R66s		
Size A4	Document Number 18.Power_Flash Power Manage		Rev V1.1
Date: Thursday, June 23, 2022		Sheet 18 of 27	



深圳市岚正科技有限公司		
Project	Lunzn_R66s	
Size A2	Document Number 19.USB2/USB3 Port	Rev V1.1
Date: Thursday, June 23, 2022	Sheet 19 of 27	


U3800A
CH A
CH B
LPDDR4_200P
BGA200_15R00X10R00X0R90
U3800B
LPDDR4_200P
BGA200_15R00X10R00X0R90
VCC0V6_DDR
VCC_DDR
VCC1V8_DDR
VCCA1V8_PMU
R3800 240R R0402 1%
R3801 240R R0402 1%
R3802 0R R0402 5%
R3804 0R R0603 5%
C3800 1nF C0402 X5R 50V DNP
LPDDR4
=1.1V
Rockchip Confidential
深圳市岚正科技有限公司
Lunzn_R66s
20.DRAM-LPDDR4X_1X32bit_200P
Rev V1.1
Thursday, June 23, 2022
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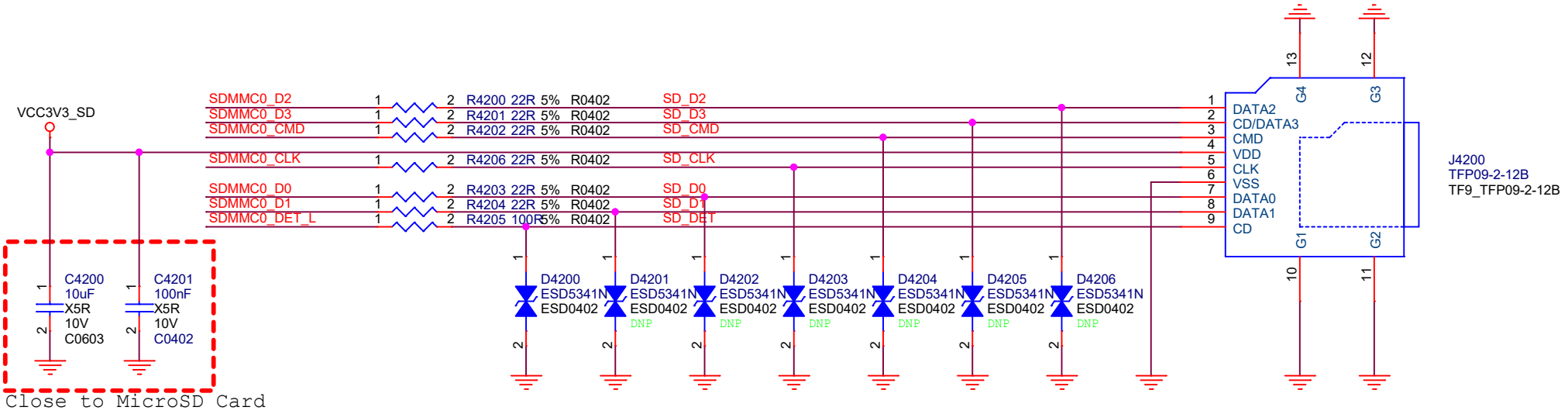
SDMMC0_D0 [8]
SDMMC0_D1 [8]
SDMMC0_D2 [8]
SDMMC0_D3 [8]
SDMMC0_CMD [8]
SDMMC0_CLK [8]
SDMMC0_DET_L [7]



MicroSD Card

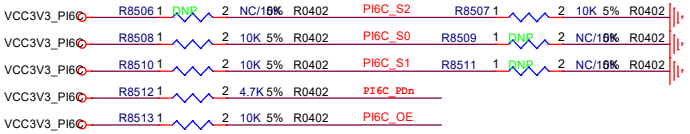
岚正科技 LUNZN TECHNOLOGY	深圳市岚正科技有限公司
Project	Lunzn_R66s
Size A4	Document Number 21.Flash-MicroSD Card
Rev	V1.1
Date:	Thursday, June 23, 2022
Sheet	21 of 27

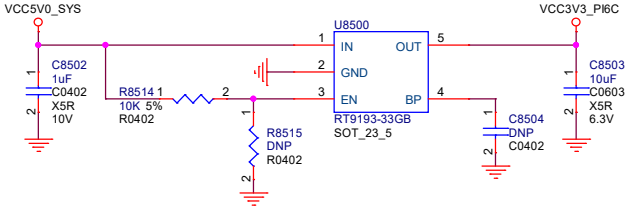
PCIE30_REFCLKP_IN [9]
PCIE30_REFCLKN_IN [9]

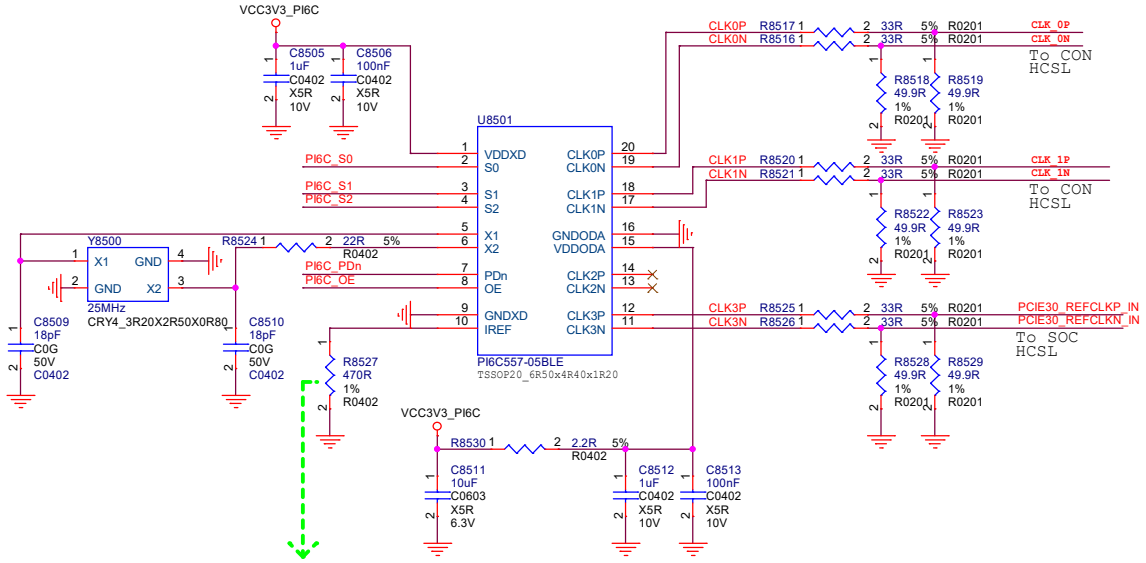
CLK_0P [23]
CLK_0N [23]

CLK_1P [24]
CLK_1N [24]

PI6C_S2	PI6C_S1	PI6C_S0	Spread %	Out Freq
0	0	0	-0.5	100MHz
0	0	1	-1.0	100MHz
0	1	0	-1.5	100MHz
0	1	1	No Spread	100MHz

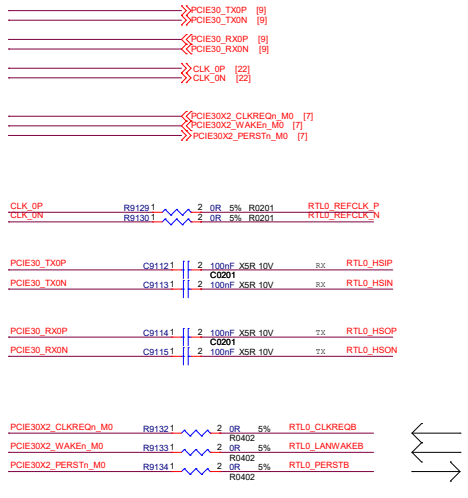


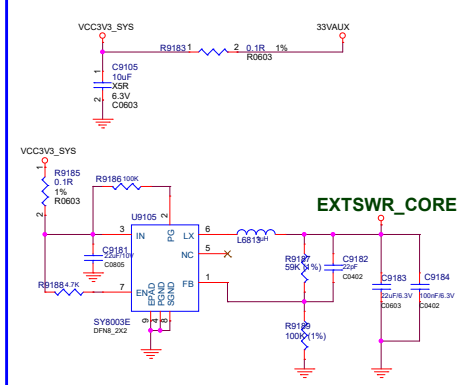


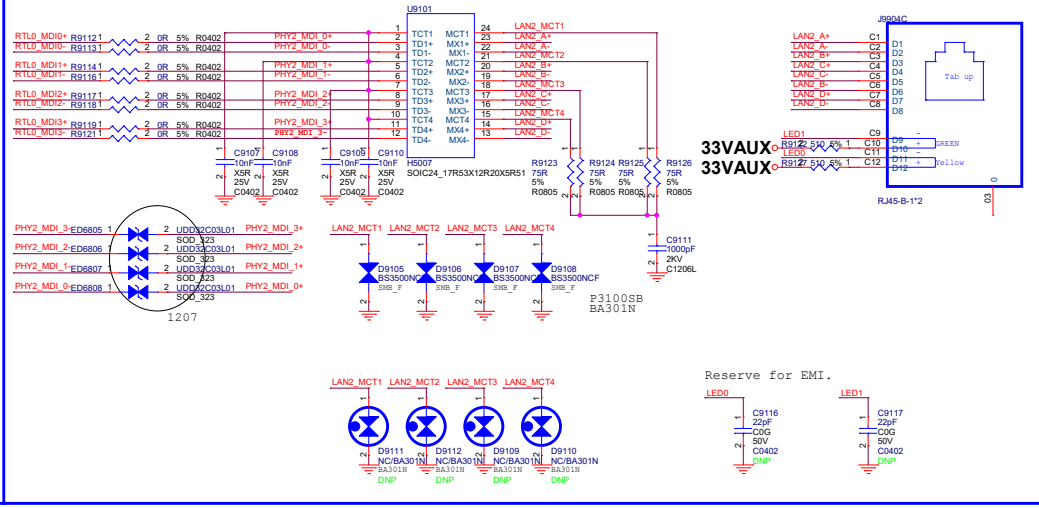


If board target trace impedance is 50ohm
then R = 475ohm providing an IREF of 2.32 mA . The output current (IOH) is 6 * IREF .
6x2.32X50=696mV

岚正科技 LUNZN TECHNOLOGY	深圳市岚正科技有限公司		
Project	Lunzn_R66s		
Size A3	Document Number 22.PCIE-Clock Generator		Rev V1.1
Date: Thursday, June 23, 2022	Sheet 22 of 27		







Ethernet PHY

For RTL8125B(S)_BG(S)_BI & RTL8111K(I)
* Place C26 close to HSOP pin -- 38
* Place C27 close to HSON pin -- 39

*If not special purpose , configure the chipset to standard PCIE protocol.

R9 for RTL8125B(S)_BG(S)_BI only
R9135 0R

Pin Notice

	8111K(I)	8125B(G)_BI	8125BS_BGS
Pin 40	DVDD10	GND	GND
Pin 43	DVDD10	EVDD33	EVDD33
Pin6	ENSWREG	POW_EXT_SWR	ENSWREG

U9102
RTL8125B(S)
RTL8125B(S)(I)
RTL8111K(I)

33VAUX
R9136 1K
R9137 15K
R9138 2.49K 1%
* R16 value should be 2.49K (1%) and be placed close to IC

LED0	LED1
ACT	LINK
Transmit	LINK

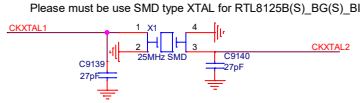
33VAUX
R9141 NC/4.7K
R9142 NC/4.7K
POW_EXT_SWR/ENSWREG

For RTL8125B(I)_BG
* Leave R17 to R18 NC
For RTL8125BS_BGS
* R17 for Enable SWR
* R18 for Disable SWR
For RTL8111K(I)
* R17 for SWR mode
* R18 for LDO mode or external power source

Refer to the page of "Power" for more detailed configuration of R17 and R18 when using different 0.95V/1.0V supply source.

Clock Source

Please must be use SMD type XTAL for RTL8125B(S)_BG(S)_BI



Refer to the page of "Reserved Components" for External Clock Source

For RTL8125B(S)_BG(S)_BI
* R27 is based on the XTAL drive level spec to choose the appropriate resistor. Do not cascade R25 on CKXTAL1 patch.
For RTL8111K(I)
* R25 is based on the XTAL drive level spec to choose the appropriate resistor. Do not cascade R27 on CKXTAL2 patch.

External Resistor

33VAUX
R9143 4.7k GPI/GPO
R9144 4.7k RTL0_LANWAKEB
R9145 4.7k LED1
RTL8125B(S)_BG(S)_BI Only

R29 PU for normal application

33VAUX
R9146 4.7k RTL0_CLKREQB

For RTL8125B(S)_BG(S)_BI & RTL8111K(I)
*. R26 is needed for ensuring IC latch to normal operation mode.
*. R28, R30 could be saved by sharing the pull-up resistors which might be possibly existed on the chipset side already.

3.3V

33VAUX

L6801 0R
C9118 2.2uF
C9119 2.2uF
C9120 2.2uF
AVDD33

For RTL8125B(S)_BI_BG(S)
* Place C3, C4 2.2uF close to AVDD33 pin -- 19, 33,
*C2=NC
For RTL8111K(I) with SWR
* Place C2 0.1uF close to AVDD33 pin -- 19
* Place C4 4.7uF close to AVDD33 pin -- 19
* C3= NC
For RTL8111K(I) with External power or LDO
*. C2 ,C3 and C4 NC

L6802 Bead 33ohm@100Mhz
C9124 0.1uF
C9125 22uF
AVDD33_PLL

For RTL8125B(S)_BG(S)_BI
L6 =33ohm
For RTL8111K(I)
L6=0R,C51=NC

L6803 0R
C9128 0.1uF
C9129 0.1uF
DVDD33

For RTL8125B(S)_BG(S)_BI
* Place C14 to C15 close to DVDD33 pin -- 29, 46
For RTL8111K(I)
* Place C14 close to DVDD33 pin -- 29
* Leave C15 NC

L6804 0R
C9131 0.1uF/X5R
C9132 4.7uF/X5R
VDDREG

Reserved
RTL8111K(I) 1.0V source @ SWR mode
RTL8125BS_BGS 0.95V source

For RTL8125BS_BGS & RTL8111K(I)
* Place C18 to C19 close to VDDREG pin -- 5

C9133 0.1uF/X5R
C9134 4.7uF/X5R
VDDREG/DVDD33

For RTL8125BS/8125BGS
* Place C20 to C21 close to VDDREG pin -- 4
For RTL8111K(I)
* Place C20 close to DVDD33 pin -- 4
* Leave C21 NC

L6805 0R
C9138 2.2uF
AVDD33_XTAL

For RTL8125B(S)_BG(S)_BI Only
* Place C25 close to AVDD33_XTAL pin -- 34

RTL8125B(S)_BI_BG(S) 0.95V
RTL8111K(I) 1.0V

VDD09/VDD10

C9121 2.2uF
C9122 2.2uF
C9123 2.2uF
AVDD09_10

For RTL8125B(S)
* Place C6 to C8 2.2uF close to AVDD09 pin -- 11, 16, 22
For RTL8111K
* Place C6 to C8 0.1uF close to AVDD10 pin -- 11, 16, 22

C9126 0.1uF
C9127 10uF
EVDD09_10

For RTL8125B(S)_BI_BG(S)
* Place C12 1uF to C13 close to EVDD09 pin -- 37
For RTL8111K(I)
* Place C12 0.1uF to C13 close to EVDD10 pin -- 37

R9138 NC/0R
C9130 0.1uF
EVDD33/DVDD10
33VAUX
R9140 0R

Notice

For RTL8125B(S)_BI_BG(S)
* Leave R2 NC and connect R3
* Place C17 1uF close to EVDD33 pin -- 43
For RTL8111K(I)
* Leave R3 NC and connect R2
* Place C17 0.1uF close to DVDD10 pin -- 43

VDD09/VDD10

C9135 2.2uF
C9136 10uF
C9137 10uF
DVDD09_10

For RTL8125B(S)_BI_BG(S)
* Place C9 to C10 10uF close to DVDD09 pin -- 8, 28
* Place C11 2.2uF close to DVDD09 pin -- 47
For RTL8111K(I)
* Place C9 0.1uF close to DVDD10 pin -- 8
* Leave C10 to C11 NC

Core Source Option

VDD09/VDD10

REG_OUT
L6806 NC/2.2uH
C9141 NC/4.7uF
C9142 NC/0.1uF/X5R
core_source
R9147 NC/0R
R9190 1 2 0R 1% R0402
EXTSWR_CORE
R9191 NC/0R
VDD0V95_RTL0

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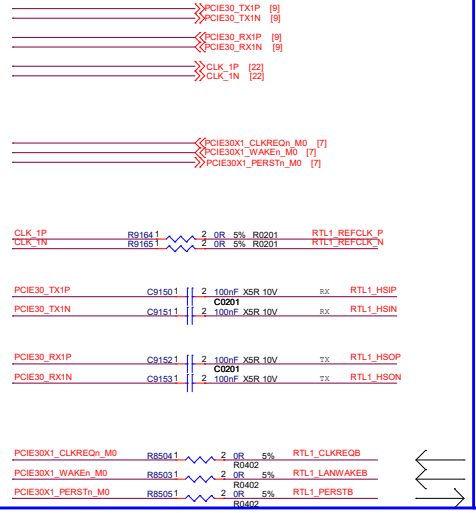
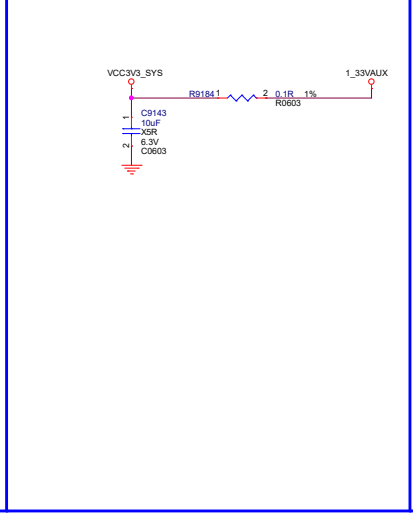
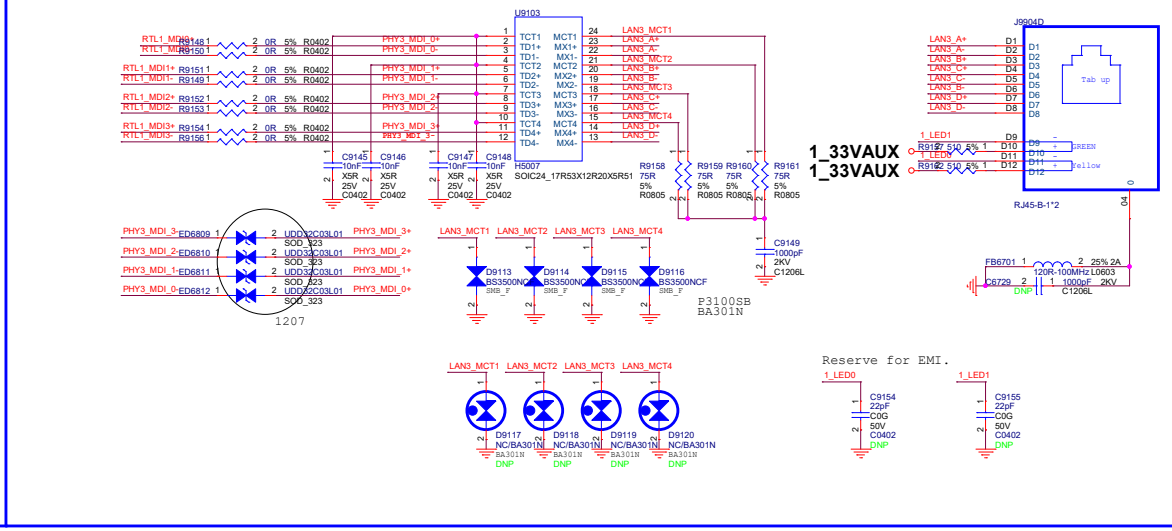






Ethernet PHY

For RTL8125B(S)_BG(S)_BI & RTL8111K(I)
* Place C26 close to HSOP pin -- 38
* Place C27 close to HSON pin -- 39

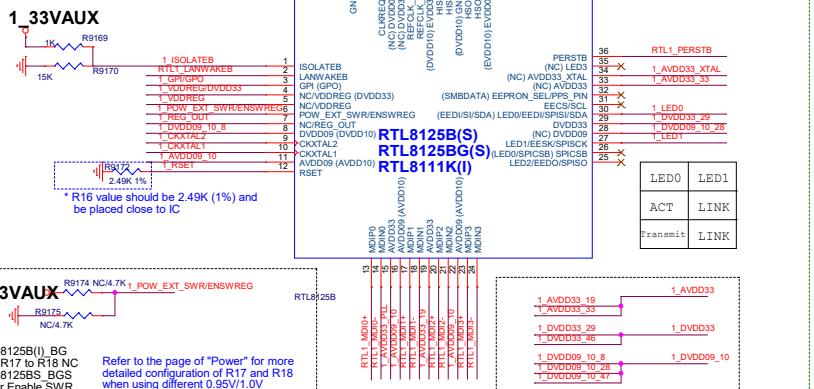
*If not special purpose ,
configure the chipset to standard PCIE protocol.

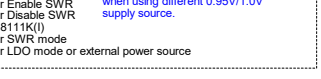
R9 for RTL8125B(S)_BG(S)_BI only

R9168 0R

Pin Notice

	8111K(I)	8125B(G)_BI	8125BS_BGS
Pin 40	DVDD10	GND	GND
Pin 43	DVDD10	EVDD33	EVDD33
Pin6	ENSWREG	POW_EXT_SWR	ENSWREG



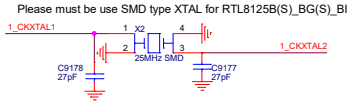


For RTL8125B(I)_BG
* Leave R17 to R18 NC
For RTL8125B_BGS
* R17 for Enable SWR
* R18 for Disable SWR
For RTL8111K(I)
* R17 for SWR mode
* R18 for LDO mode or external power source

Refer to the page of "Power" for more detailed configuration of R17 and R18 when using different 0.95V/1.0V supply source.

Clock Source

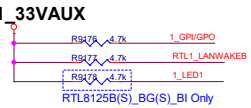
Please must be use SMD type XTAL for RTL8125B(S)_BG(S)_BI



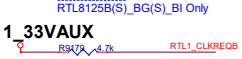
Refer to the page of "Reserved Components" for External Clock Source

For RTL8125B(S)_BG(S)_BI
* R27 is based on the XTAL drive level spec to choose the appropriate resistor. Do not cascade R25 on CKXTAL1 patch.
For RTL8111K(I)
* R25 is based on the XTAL drive level spec to choose the appropriate resistor. Do not cascade R27 on CKXTAL2 patch.

External Resistor

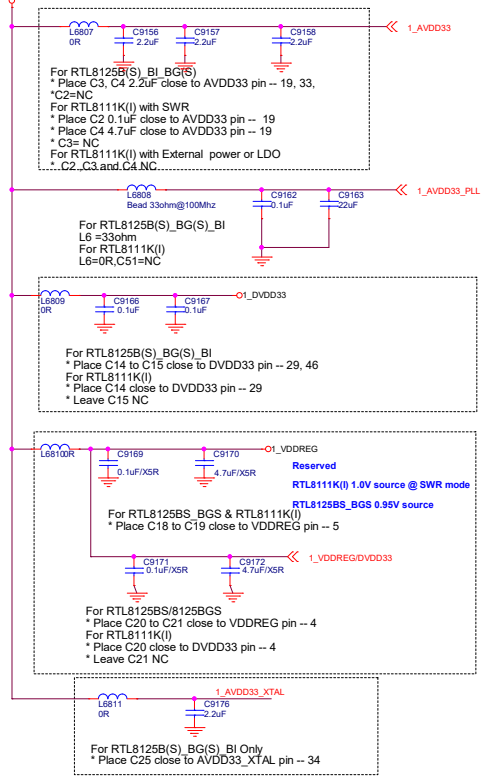


R29 PU for normal application

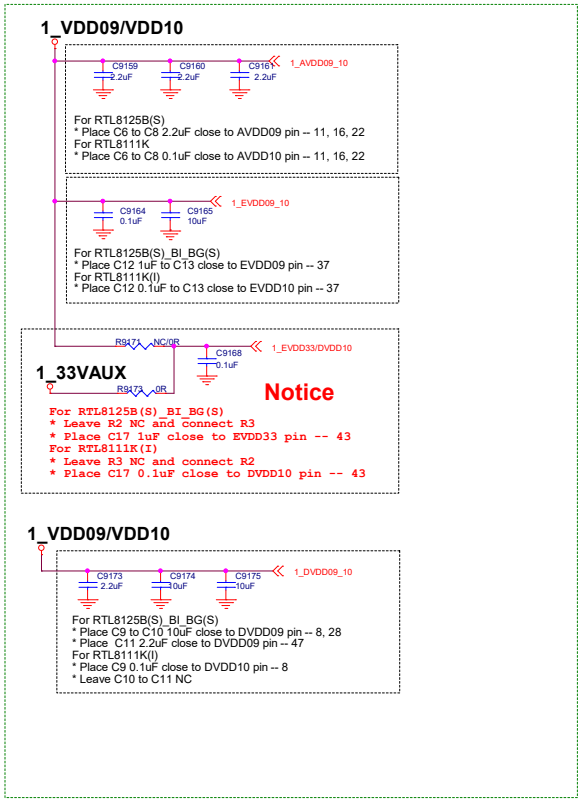


For RTL8125B(S)_BG(S)_BI & RTL8111K(I)
*. R26 is needed for ensuring IC latch to normal operation mode.
*. R28, R30 could be saved by sharing the pull-up resistors which might be possibly existed on the chipset side already.

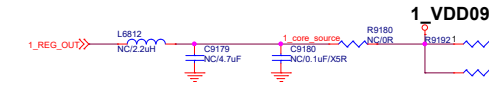
3.3V



RTL8125B(S)_BI_BG(S) 0.95V
RTL8111K(I) 1.0V



Core Source Option



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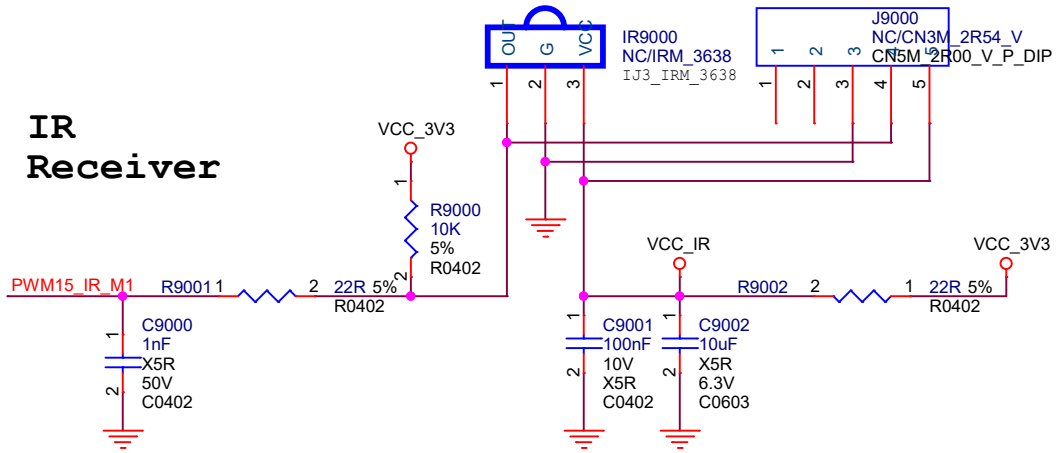
PWM15_IR_M1 [10]

IR Receiver



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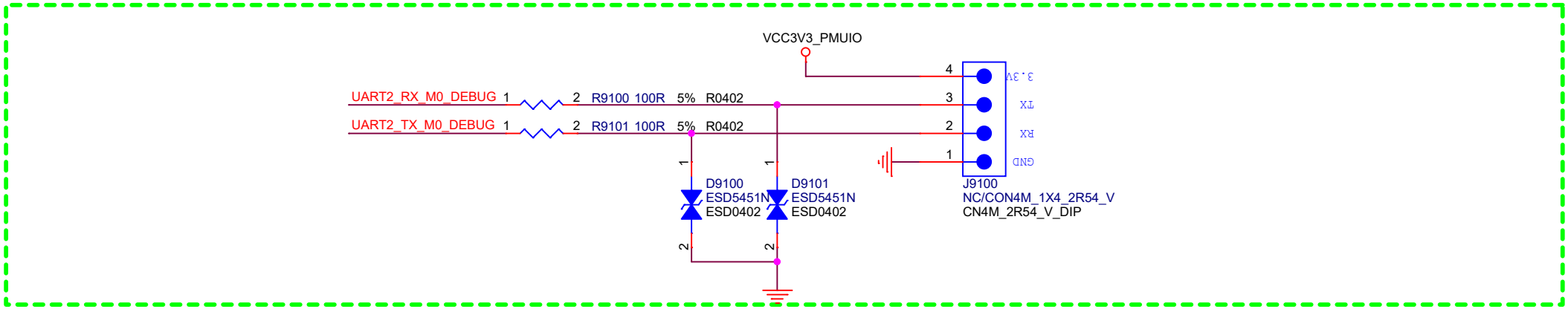
UART2_RX_M0_DEBUG [7]
UART2_TX_M0_DEBUG [7]

Debug UART2



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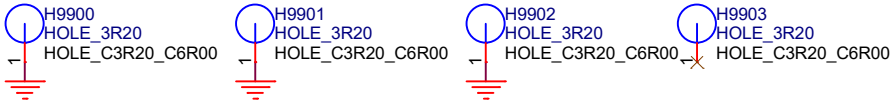

TOP Mark

BOTTOM Mark

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