

**INTELLEC® SERIES III  
MICROCOMPUTER  
DEVELOPMENT SYSTEM  
INSTALLATION AND CHECKOUT  
MANUAL**

Order Number: 121612-001

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## PREFACE

This manual, which is intended for the design engineer, programmer, or technician who will install and maintain the Intellec Series III Microcomputer Development System, is divided into six chapters and five appendixes as follows:

- Chapter 1, General Information, provides a functional description and salient specifications of the system. Also included are tabulations of power supply current capabilities and optional device current demands.
- Chapter 2, Installation, includes incoming inspection information, installation considerations, a step-by-step installation procedure, and firmware diagnostic routine checks.
- Chapter 3, CONFID Confidence Test, describes and provides step-by-step operating instructions for this interactive user test of the IPC-85 processor board, including its onboard RAM memory, and the system integral CRT, integral diskette drive, keyboard, and peripheral devices.
- Chapter 4, CON86 Confidence Test, describes and provides step-by-step operating instructions for this noninteractive user test of the RPB-86 processor board, including its onboard RAM memory, PROM memory, and real-time counters, and the system address bus, data bus, and offboard memory.
- Chapter 5, Installing Options, provides detailed instructions for installing system options.
- Chapter 6, Service Information, includes basic troubleshooting hints and instructions for obtaining service and repair assistance.
- Appendix A, Configuring the Serial Interfaces, describes the facilities available to customize the serial channel interfaces to specific devices.
- Appendix B, Modifying the Baud Rate, describes how to programmatically change the baud rates for Serial Channel 1 and Serial Channel 2.
- Appendix C, Teletypewriter Modifications, describes how to modify and attach an ASR-33 Teletypewriter to the system.
- Appendix D, Chassis-Signal Ground, describes how to isolate chassis ground from signal ground.
- Appendix E, Diskette Drive Preventive Maintenance, provides a maintenance schedule and maintenance procedures for the integral diskette drive and the optional dual double density diskette drives.

Additional information on the system is provided in the *Intellec Series III Microcomputer Development System Product Overview*, Order Number 121575.



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## **1-1. INTRODUCTION**

This chapter provides a functional description and salient specifications of the Intellec Series III Microcomputer Development System shown in figure 1-1. Also included are tabulations of the power supply current capabilities and current demands of the system options.

## **1-2. FUNCTIONAL DESCRIPTION**

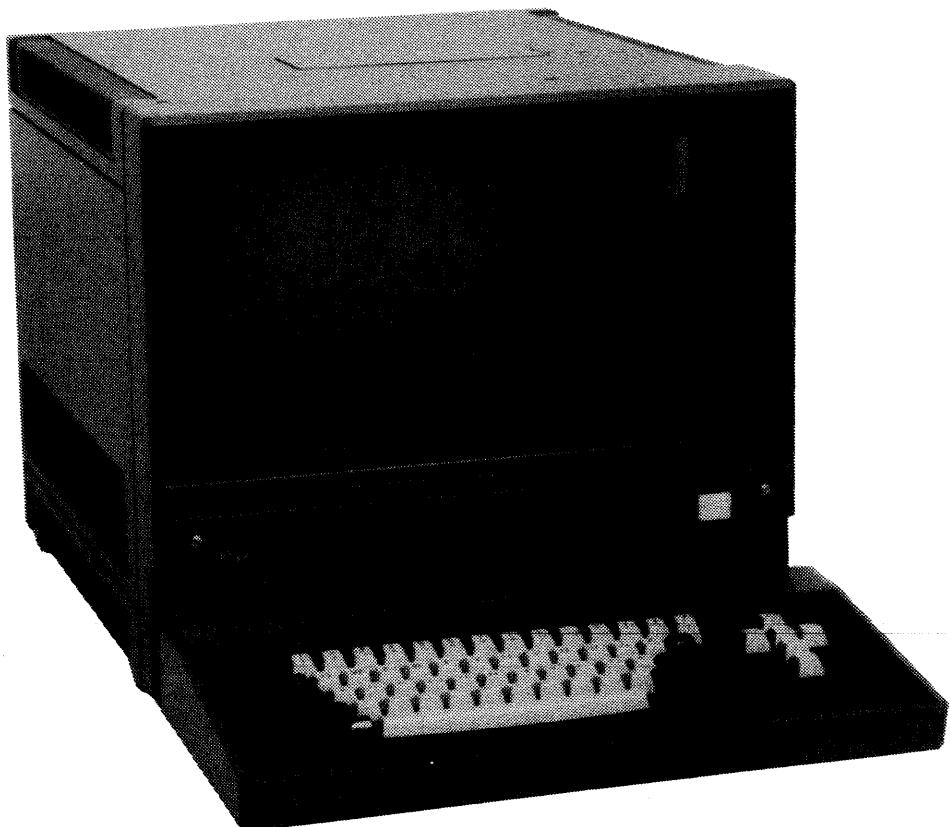
The Series III system includes the mainframe models 286, 287, 288, and 289. All four system models are identical except for the input power and color differences noted in table 1-1. A functional description of the Series III system is given in the following paragraphs.

## **1-3. SYSTEM MAINFRAME**

The system mainframe, commonly called the CRT chassis, consists of a six-slot cardcage, power supply, CRT, single density diskette drive, fans, and cables. A separate ASCII keyboard connects to the mainframe by a single cable. The rear panel includes connectors for the keyboard, two serial I/O channels, a line printer, a paper tape reader, a paper tape punch, and the Intel Universal PROM Programmer.

## **1-4. INTEGRATED PROCESSOR CARD**

The Integrated Processor Card (IPC-85) is located in the topmost slot in the six-slot cardcage. Included on the IPC-85 are an 8085A-2 8-bit NMOS microprocessor running at 4.0 MHz, 62k of read/write



**Figure 1-1. Intellec® Series III Microcomputer Development System**

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memory, 4k of read-only memory, an interrupt system, two serial I/O channels, and bus interface circuits. The 4k of read-only memory contains the Intellec System Monitor, bootstrap loader, and firmware diagnostics. An eight-level vectored priority interrupt system is structured around an 8259A Programmable Interrupt Controller. Each of the two serial I/O channels is RS232C compatible and capable of running asynchronously from 110 to 19.2k baud, or synchronously from 150 to 64k baud. Each channel is implemented using an 8251A USART. Baud rate selection is accomplished programmatically through an 8253 Programmable Interval Timer, which also serves as a real-time clock for the entire system. I/O activity through both serial channels is signaled to the system through a secondary 8259A Programmable Interrupt Controller operating in a polled mode and nested to the primary 8259A Programmable Interrupt Controller.

## 1-5. INPUT/OUTPUT CONTROLLER

The I/O Controller (IOC) board, which is responsible for the remaining I/O activity, is mounted at the rear of the mainframe. Included on the IOC board are an 8080A-2 8-bit NMOS microprocessor running at 2.0 MHz, 8k of private read/write memory, 8k of read-only memory containing I/O routines, and I/O interface circuits. The IOC provides interface for the integral diskette, CRT, keyboard, and standard peripherals including a line printer, high-speed paper tape reader, high-speed paper tape punch, and the Intel Universal PROM Programmer. Communication between the IPC-85 and the IOC is maintained over a separate 8-bit bidirectional data bus.

## 1-6. KEYBOARD

The keyboard interfaces directly to the IOC processor over an 8-bit data bus. The keyboard contains a UPI-41 Universal Peripheral Interface, which scans the keyboard, encodes the characters, and buffers the characters to provide N-key rollover.

## 1-7. INTEGRAL CRT

The CRT is a 12-inch raster scan type monitor with a 50/60 Hz vertical scan rate and 15.5 kHz horizontal scan rate. The interface to the IOC is provided through an 8275 Programmable CRT Controller. Timing for CRT control is provided by an 8253 Programmable Interval Timer.

## 1-8. INTEGRAL DISKETTE DRIVE

The integral 250k byte, single density, floppy diskette drive is controlled by an 8271 Programmable Floppy Disk Controller. The 8271 transfers data via an 8257 DMA Controller between an IOC RAM buffer and the diskette. The 8271 handles reading and writing of data, formatting diskettes, and reading status, all upon appropriate commands from the IOC microprocessor.

## 1-9. RESIDENT PROCESSOR BOARD

The Resident Processor Board (RPB-86) occupies two slots of the six-slot cardcage. Included on the RPB-86 are an 8086 16-bit HMOS microprocessor running at 5.0 MHz, 62k of read/write memory, 16k of read-only memory, and a real-time counter. The 16k of read-only memory contains a firmware program (DEBUG 86) for debugging 8086-based programs. The real-time counter is used to generate an interrupt to wake the IPC-85 processor. Communication between the RPB-86 and the IPC-85 is accomplished through a 2k byte window in the IPC-85 onboard memory.

## 1-10. SYSTEM MEMORY

Figure 1-2 shows the system memory allocation. The user may expand RAM memory above absolute location 1FFFFH by installing 32k or 64k RAM boards. The 1-megabyte address space of the 8086 microprocessor is divided into 16 pages of 64k bytes each. Page 0 is the RPB-86 onboard RAM memory, page 1 is the first (standard) offboard RAM memory board, and pages 2 through F are reserved for system RAM expansion. (The top 16k bytes of page F contains the DEBUG 86 firmware.)

## 1-11. USER CONTROL

User control is maintained through the keyboard and front panel, which consists of a power switch and indicator, reset/boot switch, run/halt light, and eight interrupt switches and indicators. The front panel circuit board is attached directly to the IPC-85 board, allowing the eight interrupt switches to connect to the primary 8259A Programmable Interrupt Controller as well as to the system bus.

## 1-12. CARD CAGE EXPANSION

Cardcage expansion to ten slots can be achieved through the addition of an Intel expansion chassis.

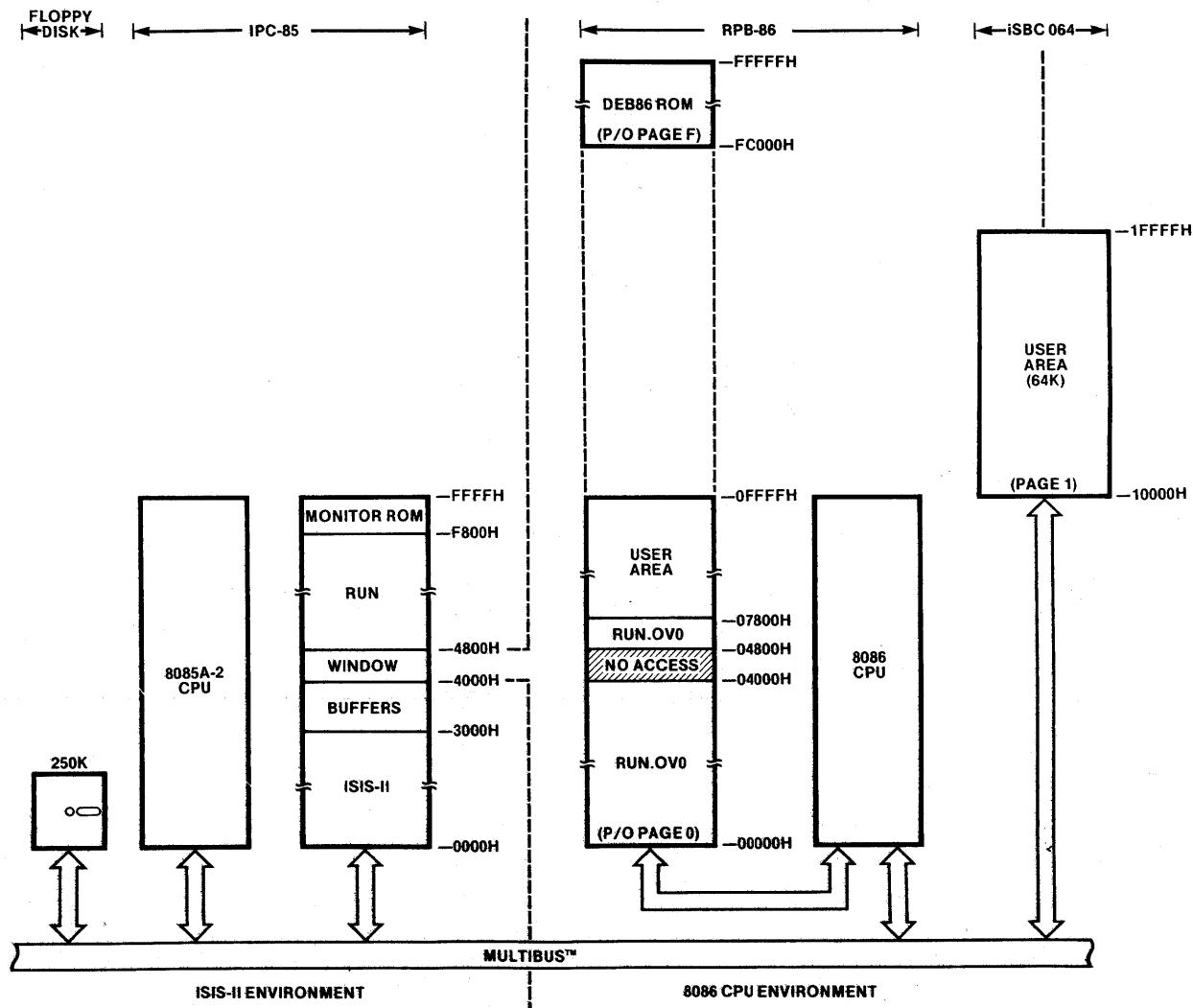


Figure 1-2. Series III System Memory Allocation

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## 1-13. MULTIBUS™ CAPABILITY

The Series III system implements Intel's Multibus architecture, which enables several bus masters, such as CPU and DMA devices, to share the bus and memory by operating at different priority levels. Resolution of bus exchanges is synchronized by a bus clock signal derived independently from the IPC-85 clock.

## 1-14. SPECIFICATIONS

Table 1-1 lists the salient specifications of the Series III system. Table 1-2 lists the mainframe power supply current loading, table 1-3 lists the power supply current capability of the optional expansion chassis, and table 1-4 lists the current demands of optional peripheral devices.

**Table 1-1. Intellec® Series III System Specifications**

<b>Integrated Processor Card (IPC-85)</b>	
Microprocessor:	8085A-2 operating at 4.0 MHz
RAM:	62k
ROM:	4k (2k for monitor, 2k for boot/diagnostic)
Bus:	Multibus architecture; bus clock rate is 9.8304 MHz
<b>Resident Processor Board (RPB-86)</b>	
Microprocessor:	8086 operating at 5.0 MHz
RAM:	62k
ROM:	16k for program debugging
Interrupts:	8-level, maskable, nested priority interrupt network initiated from front panel or user-selected devices.
<b>I/O Interfaces</b>	
Serial:	Two RS232 channels at 110-19.2k baud (asynchronous) or 150-64k baud (synchronous); programmable baud rates and serial formats. Serial Channel 1 provided with 20 mA current loop.
Parallel:	Paper tape punch, paper tape reader, line printer, and UPP-103 Universal PROM Programmer
<b>Direct Memory Access (DMA):</b>	
Standard capability of Multibus architecture; implemented for user-selected DMA devices. Maximum transfer rate of 2 MHz.	
<b>Integral Diskette Drive</b>	
No. of Drives:	One, single density
Storage Capacity:	250k bytes (formatted)
Transfer Rate:	160k bytes/second
Access Time:	Track-to-track: 10 ms Head setting time: 10 ms
Average Random Positioning:	260 ms
Rotational Speed:	360 rpm
Average Rotational Latency:	83 ms
Recording Mode:	FM
<b>AC Requirements</b>	
Model 286:	5.9A @ 100/120 Vac ±10%, 60 Hz ±5%, single phase
Model 287/288:	3.1A @ 220/240 Vac ±10%, 50 Hz ±5%, single phase
Model 289:	5.9A @ 100 Vac ±10%, 50 Hz ±5%, single phase
<b>Power Supply Capacity:</b>	See tables 1-2 and 1-3.
<b>Environmental Characteristics</b>	
Operating Temperature:	32° to 95°F (0° to 35°C)
Relative Humidity:	To 90% without condensation

**Table 1-1. Intellec® Series III System Specifications (Cont'd.)**

<b>Physical Characteristics</b>	
Mainframe:	Width: 17.37 in. (44.12 cm) Height: 15.81 in. (40.16 cm) Depth: 19.13 in. (48.59 cm) Weight: 86 lb (39 kg) Color: Model 286/287/289-blue Model 288-gray
Keyboard:	Width: 17.37 in. (44.12 cm) Height: 3.0 in. (7.62 cm) Depth: 9.0 in. (22.86 cm) Weight: 6.0 lb (2.72 kg) Color: Same as mainframe

**Table 1-2. Mainframe Power Supply Current Loading (Basic System)**

<b>Component</b>	<b>Power Supply</b>					
	<b>+5V</b>	<b>+12V</b>	<b>+15V</b>	<b>+24V</b>	<b>-10V</b>	<b>-12V</b>
<b>MAINFRAME</b>						
Power Supply Capacity	<b>30.0A</b>	<b>2.5A</b>	<b>1.5A</b>	<b>1.7A</b>	<b>1.0A</b>	<b>0.3A</b>
IPC-85 Processor	4.3A	0.5A	—	—	0.02A	0.2A
IOC	2.8A	0.1A	—	—	0.01A	—
CRT	—	—	1.5A	—	—	—
Keyboard	0.4A	—	—	—	—	—
Integral Diskette Drive	1.0A	—	—	1.7A	—	—
iSBC 064 64k RAM Board	3.2A	0.6A	—	—	—	0.01A
RPB-86 Processor	5.4A	0.4A	—	—	—	0.04A
Total Current Demand*	<b>17.1A</b>	<b>1.6A</b>	<b>1.5A</b>	<b>1.7A</b>	<b>0.03A</b>	<b>0.25A</b>
Available for Options	12.9A	0.9A	0	0	0.97A	0.05A

\*Worst case

**Table 1-3. Optional Expansion Chassis Power Supply Current Capability**

<b>See Table 1-4</b>	<b>Power Supply</b>					
	<b>+5V</b>	<b>+12V</b>	<b>+15V</b>	<b>+24V</b>	<b>-10V</b>	<b>-12V</b>
Power Supply Capacity	<b>20.0A</b>	<b>2.0A</b>	<b>N/A</b>	<b>N/A</b>	<b>1.0A</b>	<b>0.3A</b>

Table 1-4. Optional Peripheral Device Current Demand

Option*	Power Supply			
	+5V	+12V	-10V	-12V
Model 720 Double Density FDC Controller	7.5A	—	0.2A	—
Model 740 Hard Disk Controller	6.5A	—	—	—
ICE 22 Emulator	11-13A	0.1A	—	0.03A
ICE 41A Emulator	8-10A	0.1A	—	0.03A
ICE 49 Emulator	7-10A	0.08A	—	0.02A
ICE 51 Emulator	7-10A	0.08A	—	0.02A
ICE 80 Emulator	6.9-9.8A	0.08A	—	0.001A
ICE 85 Emulator	10-12A	0.08A	—	0.001A
ICE 86 Emulator	11-15A	0.08A	—	0.001A
ICE 88 Emulator	11-15A	0.08A	—	0.001A
Multi-ICE (41A + 85)	18-22A	0.18A	—	0.031A
Multi-ICE (49 + 85)	17-22A	0.16A	—	0.021A
Multi-ICE (85 + 85)	20-24A	0.16A	—	0.002A
iSBC 032 32k RAM Board**	3.2A	0.6A	—	0.01A
iSBC 064 64k RAM Board**	3.2A	0.6A	—	0.01A

\*Only allowable options in system (except expansion chassis)

\*\*System supports a maximum of two additional memory boards



## CHAPTER 2 INSTALLATION

### 2-1. INTRODUCTION

This chapter provides incoming inspection information, installation considerations, a step-by-step installation procedure, and firmware diagnostic tests for the Intellic Series III Microcomputer Development System.

### 2-2. INCOMING INSPECTION

Inspect the exterior of the shipping cartons immediately upon receipt for evidence of mishandling during transit. If either shipping carton is severely damaged or waterstained, request that the carrier's agent be present when that carton is opened. If the carrier's agent is not present, and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, contact the Intel MCSD Technical Service Center to obtain a Return Authorization Number and further instructions. (Refer to Chapter 6.) A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be reshipped.

### 2-3. INSTALLATION CONSIDERATIONS

The physical characteristics (width, height, depth, and weight) of the Series III system are given in table 1-1. Ensure that the work area (bench, table, desk, or other structure) will accommodate and support the combined weight of the basic system components and options.

The power cords for the system (mainframe, optional expansion chassis, and each optional dual double density diskette drive chassis) plug into three-conductor power outlets. The round pin on each power cord is safety power ground. If your facility does not have three-conductor power outlets, do not defeat the safety ground feature by using three-prong to two-prong adapters. Have a qualified electrician rewire the system power outlets to accommodate the third wire.

As with most sensitive electronic equipment, the Series III system is not totally immune to its environment, in particular with respect to electrostatic discharge (ESD). To minimize performance problems related to ESD:

- a. Maintain a relatively high (>60%) humidity environment.
- b. Use antistatic mats in the work area.

If these precautionary steps are taken and you experience problems seemingly related to ESD, you can obtain service and repair assistance from Intel as directed in Chapter 6.

### 2-4. INSTALLATION PROCEDURE

The following step-by-step procedure is primarily for the *initial* installation of the *basic* Series III system; i.e., the mainframe (CRT chassis), keyboard, integrated processor card (IPC-85), resident processor board (RPB-86), and 64k RAM memory board. Because system options may be installed during this initial installation, certain steps in the following procedure direct the user to branching instructions in Chapter 5 (Installing Options) for the installation of that particular option. After the option is installed, return to and continue with the basic installation procedure. If the option is not being installed, simply omit the step and proceed with the next sequential step. Proceed as follows:

- a. Interconnect optional expansion chassis and mainframe as described in paragraph 5-3. (Paragraph 5-3 also includes instructions for installing the controller cable for one or two optional dual diskette drives.) After completion, proceed with step c.
- b. If system includes optional dual diskette drive(s) but not an optional expansion chassis, install controller cable in mainframe as described in paragraph 5-8. After completion, proceed with step g.
- c. Refer to figure 2-1 and loosen top cover of mainframe by removing the two screws near front of cover and the two screws on rear of cover. Lift off top cover.
- d. There are five edge connectors (J14 through J18) on top edge of IOC board at rear of mainframe chassis. (See figure 2-2.) Carefully disconnect attaching cable from each of these connectors, one at a time, and then push it firmly back on to ensure proper seating.

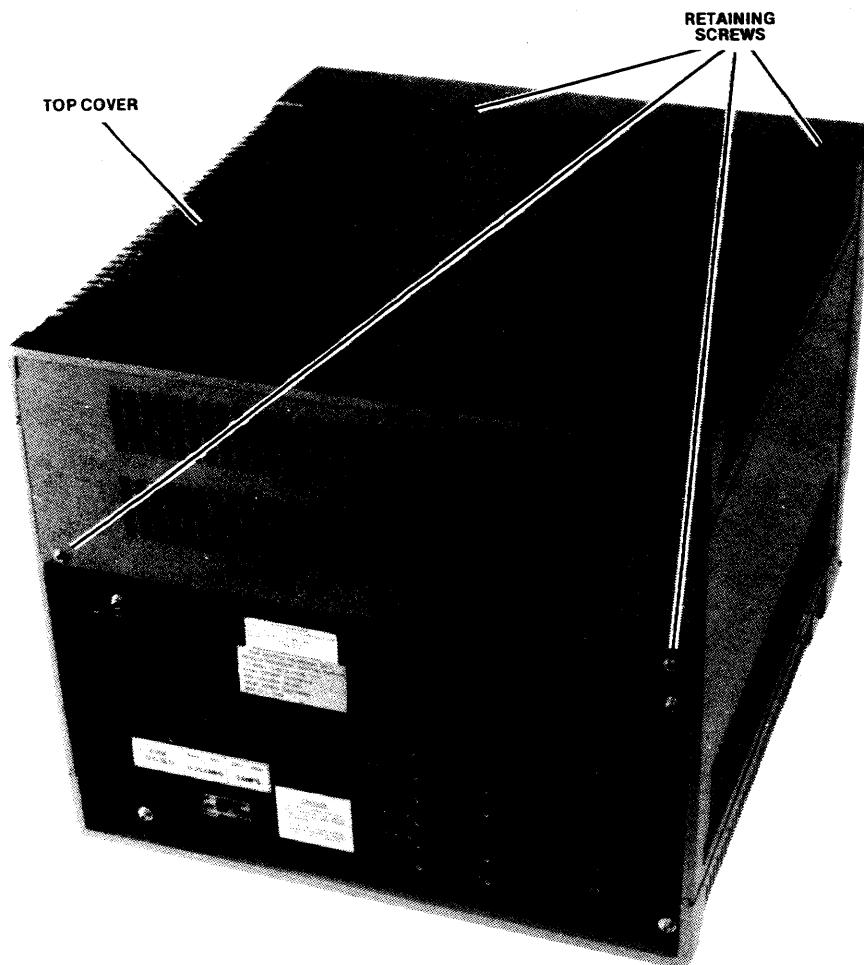


Figure 2-1. Mainframe Top Cover Retaining Screws

559-46A

- e. On mainframe front panel (figure 2-3), rotate the two retaining screws counterclockwise and remove front panel.
- f. Remove foam packing material in mainframe cardcage. (Save packing material for possible future use.)
- g. Disengage and remove IPC-85 board (figure 2-4) from top slot in cardcage by pulling outward on card extractor handles on each side of board. Press firmly inward on all socket-mounted integrated circuits to ensure proper seating. Verify the following plug-on jumper configuration:

1-2  
4-5  
7-8  
11-12  
14-15  
19-21

23-24  
25-26  
C-D

#### NOTE

Figure 2-5 shows the mainframe cardcage configuration when the system does not include an optional expansion chassis. Figure 2-6 shows the mainframe /expansion chassis cardcage configuration when an expansion chassis is installed.

- h. Install IPC-85 board in top slot of mainframe cardcage; push firmly inward on extractor handles to seat IPC-85 firmly into its mating connector in cardcage.
- i. Remove RPB-86 board (figure 2-7) from shipping carton. Press firmly inward on all socket-mounted integrated circuits to ensure

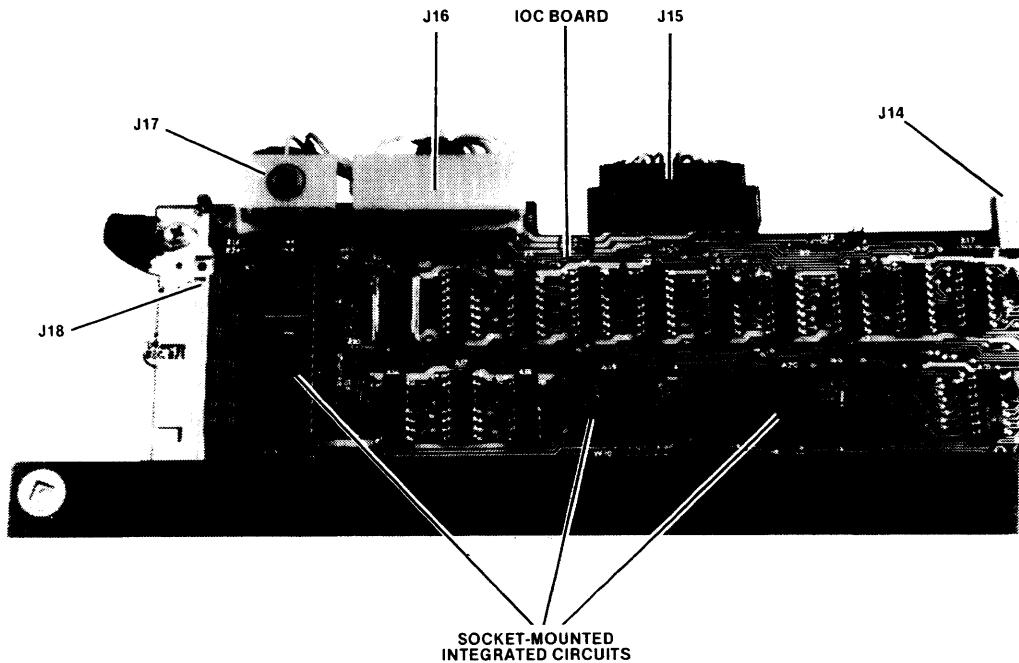


Figure 2-2. Edge Connectors and Socket-Mounted Integrated Circuits

559-48A

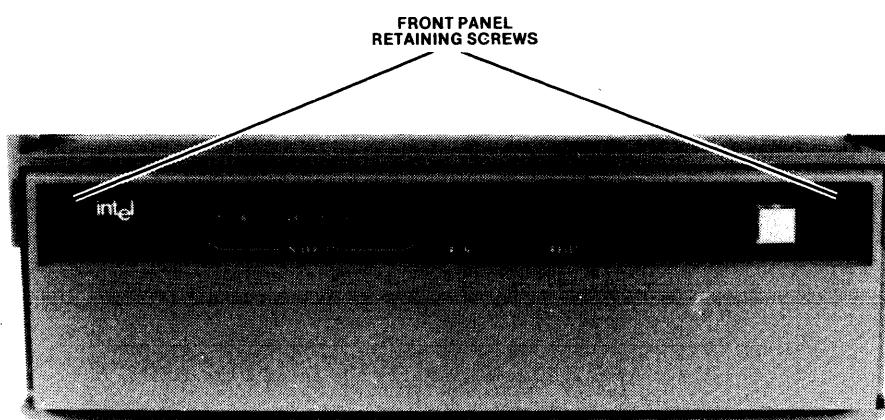


Figure 2-3. Mainframe Front Panel

559-54A

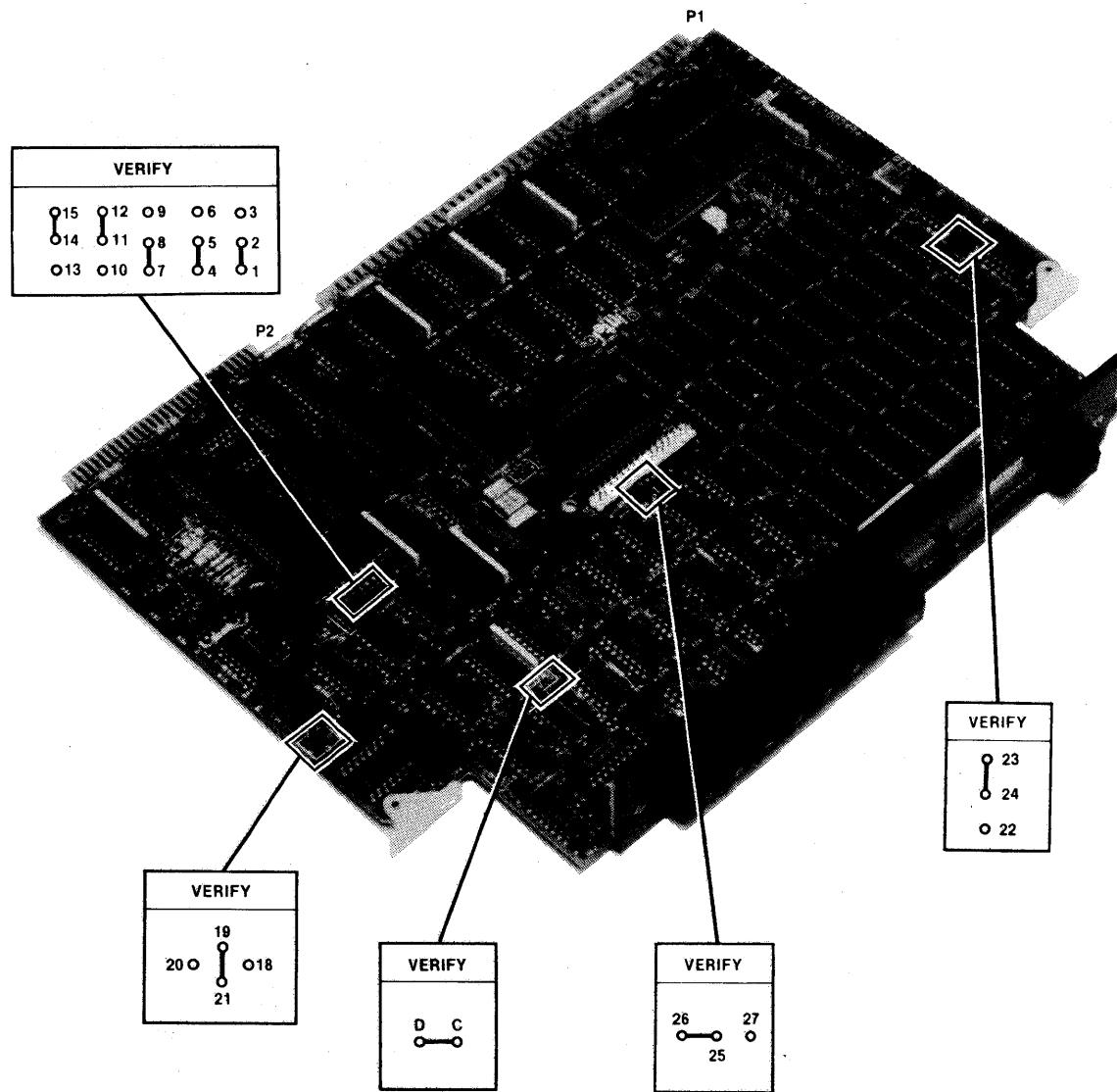


Figure 2-4. Integrated Processor Card (IPC-85)

121612-3

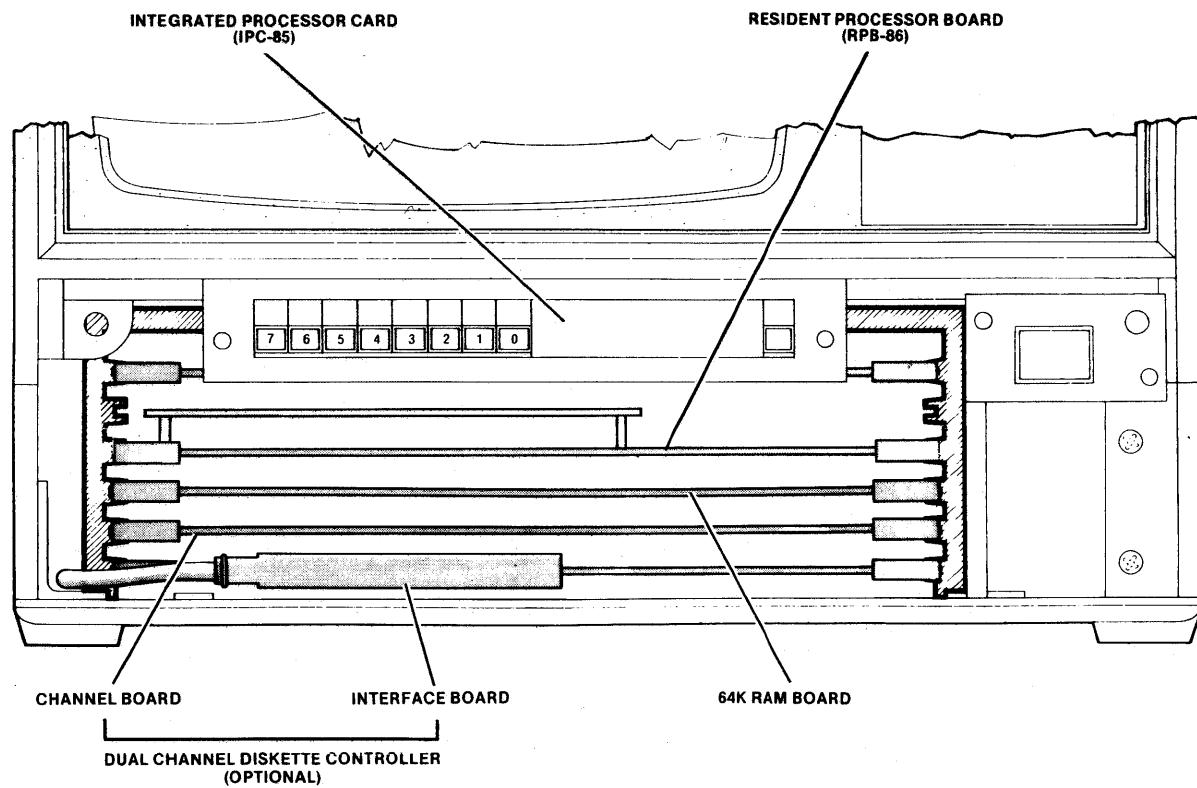


Figure 2-5. Mainframe Cardcage Configuration

121612-4

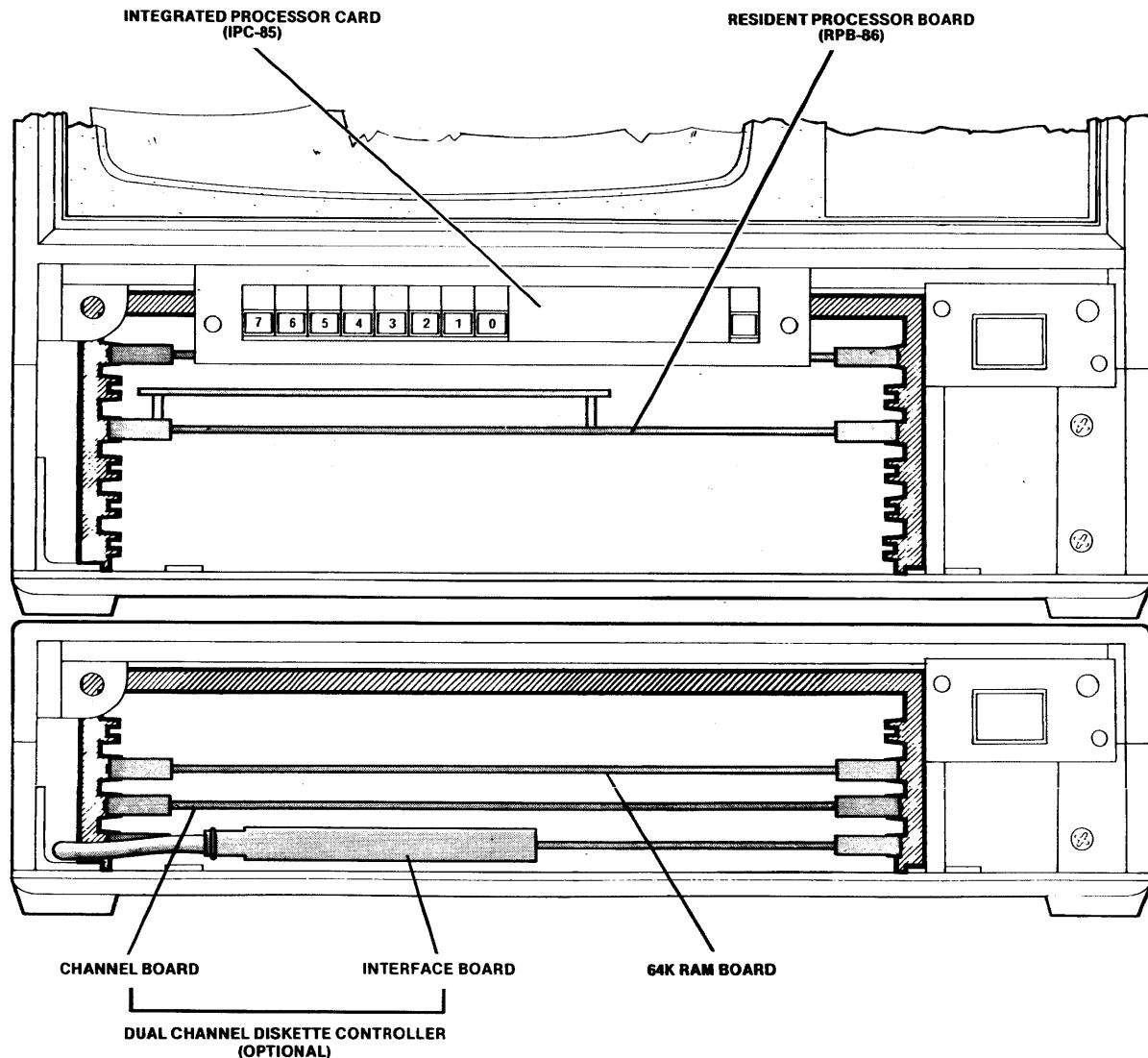
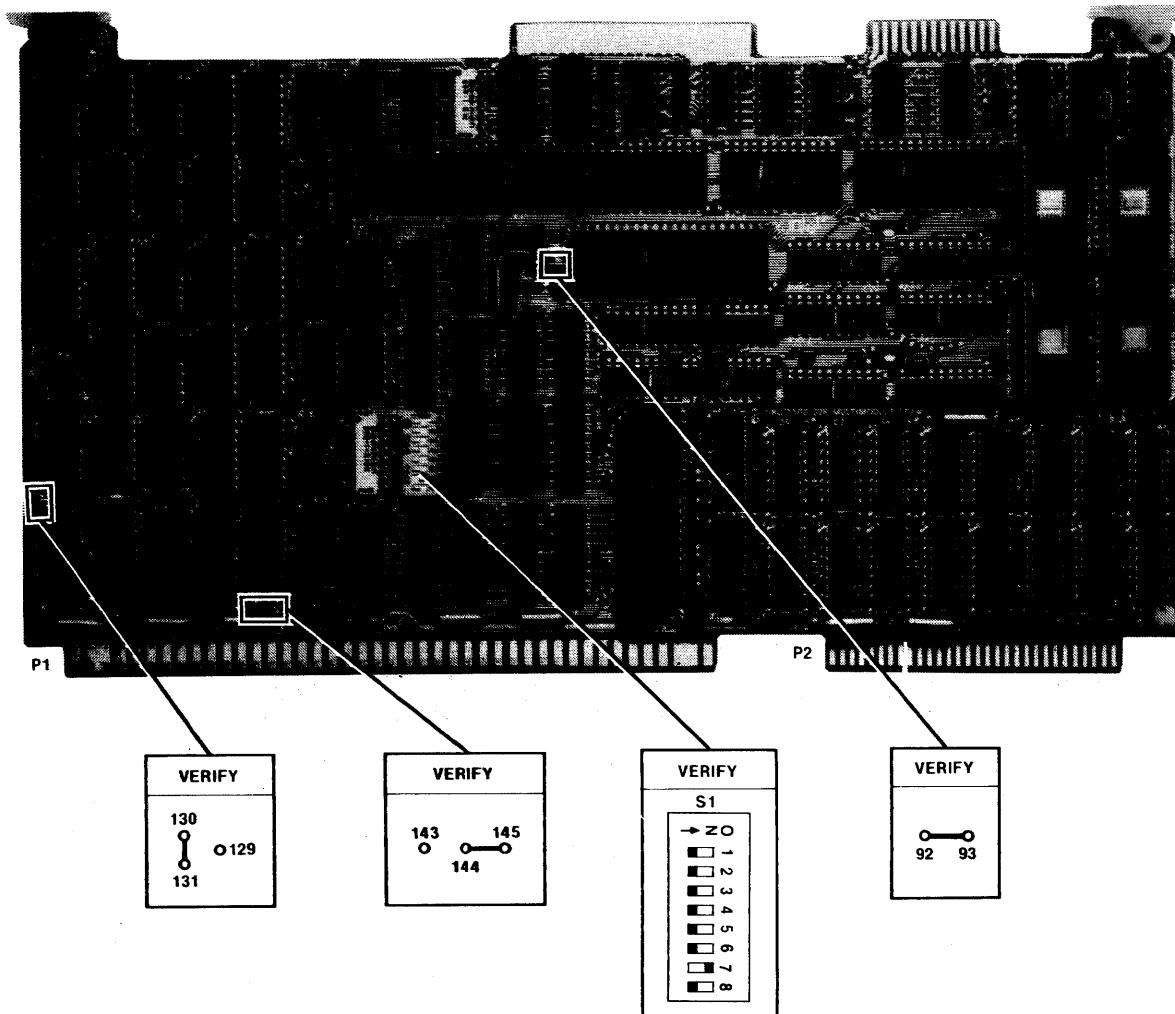


Figure 2-6. Mainframe/Expansion Chassis Cardage Configuration

121612-5



NOTE: S1-7 IS THE ONLY SWITCH POSITION THAT IS SET TO ON.

Figure 2-7. Resident Processor Board (RPB-86) Configuration

121612-6

proper seating. Verify the following plug-on jumper and switch configurations:

92-93  
130-131  
144-145  
S1-1 OFF  
S1-2 OFF  
S1-3 OFF  
S1-4 OFF  
S1-5 OFF  
S1-6 OFF  
S1-7 ON  
S1-8 OFF

- j. Install RPB-86 board in the two adjacent slots directly below IPC-85 board. (Refer to figure 2-5)

or 2-6, as appropriate.) Push firmly inward on extractor handles to seat RPB-86 board into its mating connector in cardcage.

- k. Remove 64k RAM board from shipping carton. Refer to figure 2-8 and verify the following plug-on jumper configuration:

E1-E9  
E2-E12  
E3-E14  
E4-E15  
E5-E22  
E7-E17  
E8-E18  
E29-E30

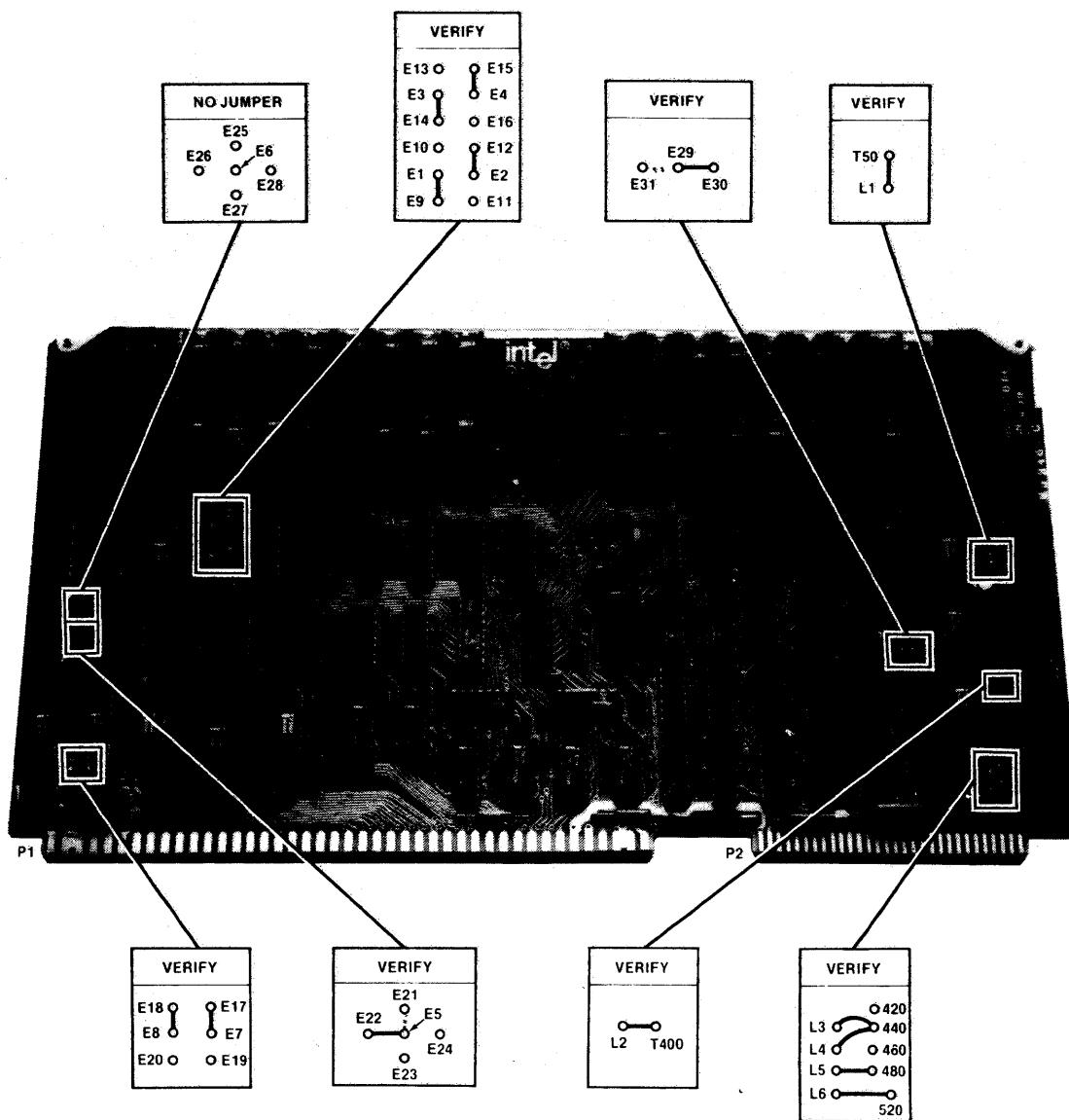


Figure 2-8. iSBC 064™ 64k RAM Board Configuration (Standard)

121612-7

1. Install 64k RAM board in any vacant cardcage slot; push firmly inward on extractor handles to seat RAM board firmly into its mating connector in cardcage.
- m. If system includes optional dual double density diskette drive(s), configure and install controller channel and interface boards as described in paragraph 5-9.
- n. Refer to figure 2-9 and disconnect keyboard cable at point of connection to keyboard assembly, and then push it firmly back on to ensure proper seating. Make certain that ground wire is attached securely to mounting screw next to keyboard cable plug. If ground wire is loose, turn keyboard assembly over, remove the two recessed Phillips head screws, and remove keyboard overlay plate. Tighten ground wire screw and replace keyboard overlay plate.
- o. Insert free end of keyboard cable into KEYBOARD connector J1 on rear chassis panel. *Do not route keyboard cable underneath chassis.* Fasten keyboard cable ground wire to screw next to connector J1. (See figure 2-10.)
- p. On rear panel of mainframe, disconnect power cord (if connected) and slide fuse holder door on main power socket to left as shown in figure 2-11. Remove voltage switching card and reinstall it in position corresponding to your

available commercial power. Verify that proper fuse is installed: 6.25A slow-blow fuse for 100V or 120V; 3A slow-blow fuse for 220V or 240V. Close fuse holder door and install mainframe power cord and, if present, expansion chassis power cord.

- q. Reinstall front panel on mainframe and optional expansion chassis (if present). Omit step r if optional dual channel diskette drive(s) is not part of initial system installation.
- r. Install optional dual channel diskette drive(s) as described in paragraph 5-10.

This completes the initial system installation. Verify the system performance by executing the firmware diagnostics (paragraph 2-5), disk-based CONFID confidence test (Chapter 3), and disk-based CON86 confidence test (Chapter 4).

## 2-5. FIRMWARE DIAGNOSTIC TESTS

There are three firmware diagnostic tests, a disk-based CONFID confidence test, and a disk-based CON86 confidence test for the Series III system. Although each test will detect errors in the system, all five tests must be run to provide complete verification of system performance. In the three firmware diagnostic tests described in following paragraphs, operator commands and responses to test prompts are shown in **reverse video**.

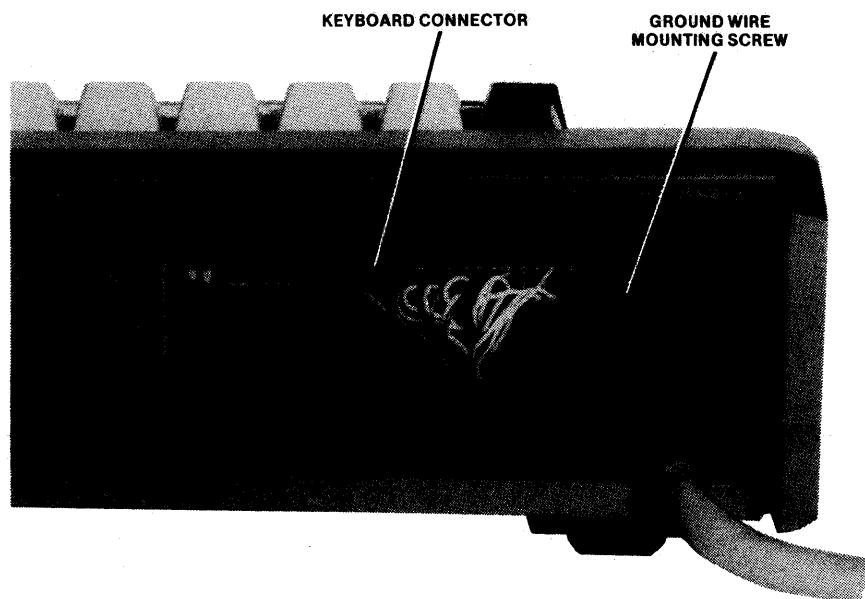


Figure 2-9. Keyboard Cable Internal Connection

121612-8

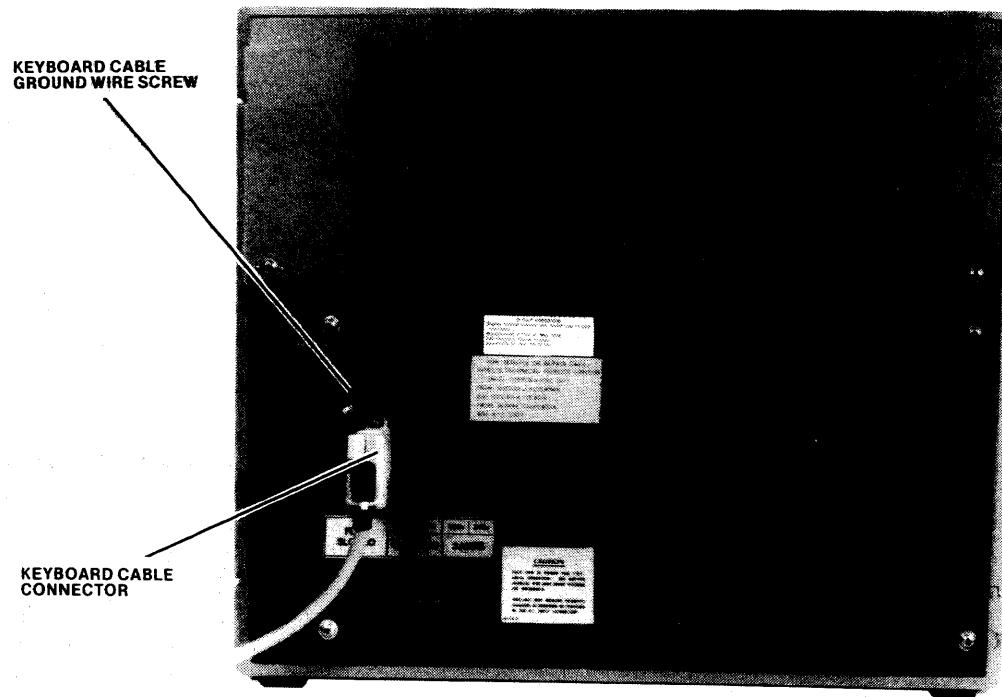


Figure 2-10. Keyboard Cable Rear Panel Connection

559-53

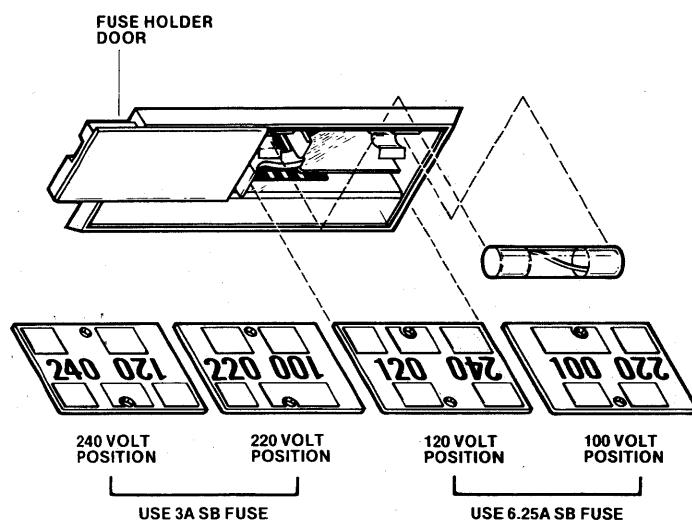


Figure 2-11. Mainframe Voltage Switching Card and Fuse

121612-9

## 2-6. POWER-UP/RESET DIAGNOSTIC

The power-up/reset diagnostic runs automatically when power is first applied to the system and whenever the front panel RESET switch is pressed. This diagnostic verifies operation of the basic IPC-85 and IOC circuits, but is not comprehensive. If this is the initial system installation, or if there is any question about the system's operation, perform the IPC-85 and IOC diagnostics described in paragraphs 2-7 and 2-8, the CONFID test described in Chapter 3, and the CON86 test described in Chapter 4.

The system gives no indication that it has passed the power-up/reset diagnostic. If failures are detected, an error message (or messages) will be displayed on the CRT.

## 2-7. IPC-85 DIAGNOSTIC

The IPC-85 diagnostic tests circuits on both the IPC-85 and the IOC. It is more comprehensive than the power-up/reset diagnostic and is easily called, but does not test all system functions. Specifically, this diagnostic checks (1) ROM and parallel input-output (PIO) checksums, (2) IOC interrupts and RAM, (3) PIO interrupts and RAM, and (4) the 62k RAM on the IPC-85 processor board.

To run the IPC-85 diagnostic, proceed as follows:

1. Ensure that DIAGNOSTIC/LINE/LOCAL switch on rear panel is set to LINE (middle) position.
2. Turn power on and press RESET. The system responds with the monitor sign-on message

SERIES II MONITOR, Vx.y

where x.y indicates the version and release number of the monitor.

3. Call IPC-85 diagnostic by typing

Z\$<cr>

where <cr> denotes the system keyboard RETURN key.

The IPC-85 diagnostic executes automatically and, if no errors are detected, the CRT displays:

```
INTELLEC SERIES II DIAGNOSTIC Vx.y
TESTING CHECKSUMS-PASSED
TESTING IOC-PASSED
TESTING PIO-PASSED
TESTING RAM-PASSED
END DIAGNOSTIC
```

If the diagnostic detects errors, error messages will be displayed under the TESTING CHECKSUMS, TESTING IOC, TESTING PIO, or TESTING RAM messages as appropriate. The error messages and probable failures are shown in table 2-1.

**Table 2-1. IPC-85 Firmware Diagnostic Error Messages**

Error Message	Probable Failure*
FAILURE—BOOT CHECKSUM	IPC-85
FAILURE—IOC CHECKSUM	IOC
FAILURE—IOC INTERRUPTS	IPC-85 or IOC**
FAILURE—IOC NOT RESPONDING	IOC
FAILURE—IOC RAM	IOC
FAILURE—MONITOR CHECKSUM	IPC-85
FAILURE—PIO CHECKSUM	IOC
FAILURE—PIO INTERRUPTS	IPC-85 or IOC**
FAILURE—PIO NOT RESPONDING	IOC
FAILURE—PIO RAM	IOC
FAILURE—RAM BANK mmK-nnK	IPC-85

\*Before replacing any board, run IOC diagnostic. Make decision based on results of all tests.

\*\*Most probable cause is IPC-85, but may be IOC. Replace IPC-85 first.

## 2-8. IOC DIAGNOSTIC

The IOC diagnostic tests circuits that (except for the reset) are exclusively located on the IOC. It is therefore a good test to use to isolate troubles to either the IOC or the IPC-85. The IOC diagnostic also provides an audible indication of the test and can therefore be run as a starting point when the CRT is not providing correct indications.

In addition to testing the IOC, the IOC diagnostic also tests the keyboard, the CRT, and the integral disk drive. Probable causes of failures encountered during execution of the IOC firmware diagnostic are listed in table 2-2.

To run the IOC diagnostic, proceed as follows:

1. On rear panel, set DIAGNOSTIC/LINE/LOCAL switch to DIAGNOSTIC (up) position. Press RESET.
2. System runs a "five-beep" test automatically when RESET is pressed. If test executes correctly, you will hear the five beeps spaced as follows: two beeps, slight pause, three beeps. After fifth beep, system displays the following sign-on message:

INTELLEC SERIES II IOC DIAGNOSTIC Vx.y  
TYPE CNTL-@, RUBOUT, 'U' AND '\*'.

REQUESTED RECEIVED

3. Type

CNTL-@ (CNTL and @ keys simultaneously)

RUBOUT (RUBOUT key)

U

\*

4. System checks and displays each input and then displays the test menu as follows:

REQUESTED RECEIVED

```
↑@ 00000000 ↑@ 00000000
RO 01111111 RO 01111111
U 01010101 U 01010101
* 00101010 * 00101010
```

D-DISK  
G-GENERAL  
K-KEYBOARD

If REQUESTED and RECEIVED data do not match, system will display ERROR and indicate faulty bits. For example:

REQUESTED RECEIVED

```
↑@ 00000000 ↑@ 00000000
RO 01111111 W 01010111 ERROR 00101000
U 01010101 U 01010101
* 00101010 # 00100011 ERROR 00001001
```

**2-9. INTEGRAL DISK DRIVE TEST.** This test may be selected only when IOC diagnostic test menu is displayed. Proceed as follows:

1. Type

D

System prompts

DISK TEST

Insert SCRATCH disk and type "#".

2. Insert scratch diskette; ensure that diskette is write enabled. Type

#

3. System runs test in approximately 40 seconds. Indicator on drive lights during test and you can hear drive operating. If system passes test, the test menu is displayed. If there is a failure, system displays

READ ERROR

or

ERROR nnnnnnnn (see table 2-2)

**2-10. GENERAL TEST.** To select and execute the general test from IOC diagnostic test menu:

1. Type

G

2. System displays

TEST PASSED

or

TEST FAILED

and menu.

**2-11. KEYBOARD TEST.** To select and execute the keyboard test from IOC diagnostic test menu:

1. Type

K

2. System displays full screen (25 lines, 80 characters per line) of characters.

3. Type each keyboard character. System displays full screen of each typed character. Note that pressing CNTL and any other key displays ↑x, where "x" is other key. Note that letters are displayed as capitals unless TPWR key is also pressed and latched. Letters follow SHIFT key when TPWR key is released.

4. On rear panel, set DIAGNOSTIC/LINE/LOCAL switch to LINE (middle) position. Press RESET. System displays

SERIES II MONITOR, Vx.y

**Table 2-2. IOC Firmware Diagnostic Errors/Error Messages**

Errors/Error Message	Problem Failure
Failed Power-Up Reset Test	Faulty IPC-85 or IOC. Analyze error message.
Failed Integral Disk (D) Test	
READ ERROR	Faulty IOC, diskette, cable, or diskette drive.
ERROR nnnnnnnn	Fields of result byte nnnnnnnn are:
	<p>7 6 5 4 3 2 1 0 (LSB)</p> <p>Deleted record</p> <p>CRC error</p> <p>Seek error</p> <p>Address error</p> <p>Data overrun/underrun error</p> <p>Write protect</p> <p>Write error</p> <p>Not ready</p>
Failed General (G) Test	Faulty IOC.
Failed Keyboard (K) Test	Single bad character indicates faulty keyboard or keyboard cable. Multiple bad characters indicate faulty IOC.



# CHAPTER 3

## CONFID CONFIDENCE TEST

### 3-1. INTRODUCTION

The CONFID confidence test, which runs under Version 4.0 (or later) of the ISIS-II Disk Operating System, provides a comprehensive diagnostic check of the ISIS-II processor (IPC-85), the on-board IPC-85 read/write (RAM) memory, the CRT and keyboard, the integral floppy disk drive, and all installed peripherals. For each functional test (except the memory test), CONFID outputs a PASSED or FAILED message based on actual versus expected results of the test, or prompts the operator to make a PASS or FAIL decision based on the visual output. For the memory test, CONFID reports all errors as soon as they are detected during the test and outputs an audible beep at the end of the test.

Successful execution of the CONFID test described in this chapter and the CON86 confidence test described in Chapter 4 demonstrates the complete functional capabilities of the Series III system.

### 3-2. TEST DESCRIPTION

There are two levels of test software: CONFID and CONFID.OVx. CONFID is the control module that selects which functional test is to be executed by accepting and interpreting the parameters passed to it by CONF (the Test Manager). CONFID.OVx is the overlay files containing the 12 functional tests to be executed (x is the overlay number).

The 12 functional tests listed below and described in following paragraphs are almost totally interactive in that all but two of the tests require some operator response. If the requested response is not received in a predetermined period of time, that particular functional test times out and is not executed.

Test	Function
0	PROCESSOR TEST
1	CRT CHARACTER SET TEST
2	KEYBOARD CHARACTER SET TEST
3	CRT WRITE TEST
4	CRT CURSOR TEST
5	TTY TEST
6	LINE PRINTER TEST
7	HIGH SPEED PUNCH TEST
8	HIGH SPEED READER TEST
9	FRONT PANEL INTERRUPT TEST
A	FLOPPY DISK TEST
B	MEMORY TEST

### 3-3. TEST 0—PROCESSOR TEST

This test executes all IPC-85 (8085) instructions and verifies the results. If a failure occurs, the test terminates and displays the address of the failure. (This address is a function of the Monitor and cannot be used to determine the exact failure.) If a failure is encountered, control is passed to the Monitor. The remaining tests are not executed because further results are meaningless if the IPC-85 is malfunctioning.

### 3-4. TEST 1—CRT CHARACTER SET TEST

This test outputs all the displayable characters to the integral CRT, and prompts the operator to examine the output and make a PASS or FAIL decision based on the quality of the displayed characters.

### 3-5. TEST 2—KEYBOARD CHARACTER SET TEST

This test checks the integral keyboard and prompts the operator to type each key. Any nonfunctioning key or bad keycode will be detected. If the test detects a failure, the test will continue checking the rest of the keyboard.

### 3-6. TEST 3—CRT WRITE TEST

This test outputs two screenfuls of characters to the integral CRT. The first screenful is filled with the numbers 0 through 9 repeatedly. Since no carriage returns are issued, the last line will show if any characters have been lost; the last line should be a full line of output. The second screenful is blank; i.e., the cursor moves through each position of the CRT screen without outputting characters. The operator is prompted to make a PASS or FAIL decision after each screenful.

### 3-7. TEST 4—CRT CURSOR TEST

This test, using cursor controls, outputs a rectangular pattern of asterisks (\*) to the integral CRT. The operator is prompted to examine the screen at the end of the test and make a PASS or FAIL decision based on the display.

### 3-8. TEST 5—TTY TEST

This test checks the TTY keyboard and the TTY printer, punch, and reader. First, two lines of the standard ASCII character set are printed, after which the program echoes back to the TTY all keys as they are being typed on the TTY keyboard.

The test then punches a null leader, two lines of the standard ASCII character set, and a null trailer, and prompts the operator to turn off the punch and load the paper tape that was just punched into the TTY reader. Finally, the tape is read and compared with correct data that should have been punched.

### 3-9. TEST 6—LINE PRINTER TEST

This test outputs the standard ASCII character set to the lineprinter and prompts the operator to examine the print quality and make a PASS or FAIL decision.

### 3-10. TEST 7—HIGH SPEED PUNCH TEST

This test punches a null header, two lines of the standard ASCII character set, and a null trailer. The punched tape may be examined for correct data or the tape can be used in the High Speed Reader Test described next.

### 3-11. TEST 8—HIGH SPEED READER TEST

This test prompts the operator to load the paper tape produced during the High Speed Punch Test into the high speed tape reader. The tape is read and compared with the correct data that should have been punched.

### 3-12. TEST 9—FRONT PANEL INTERRUPT TEST

This test checks the front panel interrupt switch operation. The operator is prompted to press each interrupt switch in any order. The test then services them in the selected order and verifies that the priority and jump addresses are correct.

### 3-13. TEST A—FLOPPY DISK TEST

This test exercises all installed floppy disk drives, starting with the external drive(s) (if installed) and ending with the integral drive. First, the disk(s) are formatted, then data is randomly written and read

from a variety of tracks and sectors, both in a single sector mode and multisector mode. Finally, the test performs a write, verify, and recalibrate on each drive.

### 3-14. TEST B—MEMORY TEST

This test checks the 62k of RAM memory installed on the IPC-85, detects failures, and reports errors to aid in system diagnosis. This test allows the operator to select and run one of the following five types of tests:

1. A marching ones and zeros test to provide a quick check for stuck cells and addressing problems. The test, using FFH as a default foreground pattern or a user-specified foreground pattern, marches (writes) a background pattern (the complement of the foreground pattern) upward through memory and then marches the foreground pattern downward through memory. The test reads and checks the data after each write.
2. A galloping pattern (galpat) test to check for pattern sensitivity and access problems. The test, using FFH as a default foreground pattern or a user-specified foreground pattern, initially writes the complement of the foreground pattern into all 62k of IPC-85 memory. Starting at the low end of memory, the test (1) establishes the first test location, (2) writes the foreground pattern into that test location, and (3) reads all other locations to verify that the data is unchanged. Between each of these read operations, the test also verifies that the foreground pattern in the first test location remains unchanged. After completing this procedure for the first test location, the test (1) complements the foreground pattern in the first test location, (2) complements the pattern in the second test location (next sequential address), and (3) reads and verifies memory as stated above. This method of selecting test locations and checking all other locations continues until all 62k of memory is checked. After this sequence is performed with the top of memory selected as the test location, the test performs a second pass with the foreground pattern written throughout memory and the complement written in the test locations.
3. A walking ones and zeros test, which is an abbreviated two-pass version of the galpat test just described. This test is identical to the galpat test except that it does not verify the foreground pattern in the test location between read operations of the other locations.
4. A refresh test to check for RAM refresh failures not detectable by the other types of memory tests, which refresh RAM by reading and writing. The test writes a pattern (FFH) into all

62k of IPC-85 memory and then waits beyond the 2-millisecond refresh cycle and checks for changes in data. The test then complements the pattern (00H) in memory and repeats the write, wait, and check sequence.

5. An address test to locate addressing problems. The test checks the integrity of the low byte addresses by writing values 0-255 in corresponding bytes of each 256-byte block and then verifying the contents. The test checks the integrity of the high byte addresses by writing a block number (starting with 1) in the tenth byte of each sequential 256-byte block and then verifying the contents.

If an error occurs with any of these five tests, the test displays the failing address together with the expected versus received data.

### 3-15. COMMAND SYNTAX CONVENTIONS

Table 3-1 summarizes the syntax convention used in the Test Manager commands and the memory test utility commands.

**Table 3-1. CONFID Command Syntax Conventions**

Notation	Description
UPPERCASE letters	Elements in uppercase are specific keywords that must be entered exactly as shown (or abbreviated as described in paragraph 3-16).
<i>lowercase italics</i>	Elements in lowercase italics identify tokens. From each set, select and enter a specific identifier.
...	Elements followed by an ellipsis (...) may be repeated indefinitely.
[ ]	When only one element is enclosed in brackets, that element is optional. When two or more elements are enclosed in brackets, ALL elements are optional, but only ONE element may be entered.
{ }	One, and <i>only</i> one, of the elements enclosed in braces must be entered.

### 3-16. TEST MANAGER COMMANDS

There are nine Test Manager commands that allow the operator to specify the test sequence and report the result in an orderly manner. These test commands are described in following paragraphs. As shown below, any command consisting of four or more letters can be abbreviated to the first three letters of the command. Additionally, the letter T is accepted as an abbreviation for TEST.

Command	Abbreviation	Paragraph
TEST	TES (or T)	3-17
DEBUG	DEB	3-18
LIST	LIS	3-19
SUMMARY	SUM	3-20
CLEAR	CLE	3-21
DESCRIBE	DES	3-22
IGNORE	IGN	3-23
RECOGNIZE	REC	3-24
EXIT	EXI	3-25

The function and syntax of each command, including examples, are given in paragraphs 3-17 through 3-25. Test B (memory test) includes utility commands associated only with that specific test. These commands are described in paragraph 3-26.

In the examples given in following paragraphs, operator commands and responses to test prompts are shown in reverse video; the asterisk (\*) is the CONFID test prompt for operator input and the <cr> denotes the keyboard RETURN key.

#### 3-17. TEST COMMAND

##### SYNTAX

<b>TEST</b> <i>test# [, test#]... test# TO test#</i>	[ <b>ON ERROR</b> <b>ON NOERROR</b> <b>COUNT nnnn</b> <b>FOREVER</b> ]
--	---

where

*test#* is a test number as listed and described in paragraphs 3-2 through 3-14, and

*nnnn* is the number of test iterations in hexadecimal (H), decimal (T), octal (Q), or binary (Y); the default number base is hexadecimal if the base suffix (H, T, Q, or Y) is omitted. The maximum number of iterations specifiable by *nnnn* is 65,535<sub>10</sub>.

**DESCRIPTION**

The TEST command uses the operator-supplied elements to load and execute one or more software procedures (i.e., tests). The tests are executed in numerical order regardless of the order in which they are specified. If a *test#* (i.e., test number) is specified for which no test exists, an error results. If no *test#* is specified, all 12 tests will be executed.

If ON ERROR is specified, the tests will execute in numerical order and loop only if one or more of the tests return an error condition.

If ON NOERROR is specified, the tests will execute in numerical order and loop only if all tests run without error.

If the COUNT element is included, the specified tests will execute in numerical order *n* times. If *n* = 0, or if *n* is omitted, the tests will not be executed, although the first test will be loaded into memory.

If FOREVER is specified, the tests will execute in numerical order, regardless of errors, and loop repeatedly until the operator hits the ESC key.

It should be noted that Test 0 (Processor Test) is the only test that does not require operator response. For all other tests, the COUNT, ON ERROR, ON NOERROR, or FOREVER element, when included in the TEST command, does not obviate the need for the usual operator response.

**EXAMPLES**

- Run all tests (0-B) in numerical sequence.

\*TEST<cr>

- Run a single test (e.g., Test 5).

\*TEST 5<cr>

- Run a sequence of tests (e.g., Tests 0 through 10).

\*TEST 0 TO TEST 10<cr>

- Run Tests 4, 9, 2, and 8 in numerical sequence.

\*TEST 4, 9, 2, 8<cr>

The TEST command will load and execute Tests 2, 4, 8, and 9 in numerical sequence.

- Execute a single test (e.g., Test 0) and loop only if no error occurs.

\*TEST 0 ON NOERROR<cr>

- Beginning with Test 7, run and loop on Tests 7, 8, and 9 in sequence until an error occurs and then abort.

\*TEST 7 TO 9 ON NCERROR<cr>

- Run and loop on a single test (e.g., Test 7) only if an error occurs.

\*TEST 7 ON ERROR<cr>

- Beginning with Test 7, run and loop on Tests 7, 8, 9, and A only if at least one of the tests produces an error.

\*TEST 7 TO A ON ERROR<cr>

- Run and loop continuously on a single test (e.g., Test 5) regardless of error or no error.

\*TEST 5 FOREVER<cr>

- Beginning with Test 7, run and loop continuously on Tests 7, 8, 9, and A regardless of error or no error.

\*TEST 7 TO A FOREVER<cr>

- Run a single test (Test 0) 100 (decimal) times.

\*TEST 7 COUNT 100T<cr>

- Run a sequence of tests (e.g., Tests 7 through 9) five times.

\*TEST 7 TO 9 COUNT 5<cr>

**3-18. DEBUG COMMAND****SYNTAX**

```
DEBUG = 0
DEBUG = 1
```

**DESCRIPTION**

The DEBUG command is used to selectively suppress (DEBUG = 0) or display (DEBUG = 1) error messages. The debug switch is cleared during CONFID initialization (i.e., the default condition is DEBUG = 0).

**EXAMPLES**

- Run Test 0 through Test 4 and display error messages.

\*DEBUG = 1<cr>

\*TEST 0 TO 4<cr>

### 3-19. LIST COMMAND

#### SYNTAX

**LIST pathname**

#### DESCRIPTION

The LIST command causes a copy of all subsequent output, including prompts, input, line echo, and error messages, to be sent to the ISIS-II file *pathname*. If the *pathname* :CO: (the console display) is specified, there is effectively no list file (the initial setting).

#### EXAMPLES

- Run Test A and print (copy) all output, including error messages, on line printer.

```
*DEBUG = 1<cr>
*LIST :LP:<cr>
*TEST A<cr>
```

### 3-20. SUMMARY COMMAND

#### SYNTAX

**SUMMARY [test# [,test#]...] [EO]**

#### DESCRIPTION

For each specified test, the following information is displayed by the SUMMARY command: the test number, the number of times executed, the number of times an error occurred, and whether the test was ignored or not. If no test(s) is specified, a summary of all tests will be included. If EO (Errors Only) is specified, only those tests with a non-zero error count will be displayed. The summary listing will be concluded with a statement as to whether any of the specified tests show a non-zero error count. Note that all error counts are given in hexadecimal.

#### EXAMPLES

- Display summary of Tests 3, 4, and 5.

```
*SUMMARY 3 TO 5<cr>
00003H CRT WRITE TEST
    EXECUTE 00002H TIMES, 00000H FAILURES
00004H CRT CURSOR TEST
    EXECUTE 00002H TIMES, 00001H FAILURES
00005H TTY TEST
    EXECUTE 00002H TIMES, 00000H FAILURES
```

- Display summary of Tests 3, 4, and 5 only if a non-zero error count exists.

```
*SUMMARY 3 TO 5<cr>
00004H CRT CURSOR TEST
    EXECUTE 00002H TIMES, 00001H FAILURES
```

### 3-21. CLEAR COMMAND

#### SYNTAX

**CLEAR [test# [,test#]...] [test# TO test#]**

#### DESCRIPTION

For each specified test, or for all tests if *test* range is missing, the execution count and the error count are set to zero. The CLEAR command does not affect the status (ignored or recognized) of a test, nor is the CLEAR command affected by the status of a test.

#### EXAMPLES

- Clear execution count and error count on Tests 3, 4, and 5.

```
*CLEAR 3,4,5<cr>
```

### 3-22. DESCRIBE COMMAND

#### SYNTAX

**DESCRIBE [test# [,test#]...] [test# TO test#]**

#### DESCRIPTION

The DESCRIBE command displays the name, or description, of the specified test(s), and whether the test(s) would be ignored by the TEST command. If *test* range is missing, the descriptions of all tests will be displayed.

#### EXAMPLES

- Describe Tests 3, 4, 5, and 6. (Assume that the IGNORE command has previously been specified for Test 5.)

```
*DESCRIBE 3 TO 6<cr>
00003H CRT WRITE TEST
00004H CRT CURSOR TEST
00005H TTY TEST      ****IGNORED****
00006H LINE PRINTER TEST
```

### 3-23. IGNORE COMMAND

#### SYNTAX

```
IGNORE [test# [, test#]...]
      test# TO test# ]
```

#### DESCRIPTION

The IGNORE command allows the operator, at the beginning of the CONFID session, to declare which test(s) is not to be run. The IGNORE command remains valid until negated, all or in part, by the RECOGNIZE command.

#### EXAMPLES

- Run all tests except Tests 5, 6, and 8.

```
*IGNORE 5,6,8<cr>
*TEST<cr>
```

### 3-24. RECOGNIZE COMMAND

#### SYNTAX

```
RECOGNIZE [test# [, test#]...]
      test# TO test# ]
```

#### DESCRIPTION

The RECOGNIZE command allows the operator to negate all or part of a previously issued IGNORE command.

#### EXAMPLES

- Assume that Tests 5, 6, and 8 are presently ignored and it is desired to run all tests except Test 6; i.e., Test 6 will remain ignored.

```
*RECOGNIZE 5,8<cr>
*TEST<cr>
```

### 3-25. EXIT COMMAND

#### SYNTAX

```
EXIT
```

#### DESCRIPTION

When at the CONFID prompt (\*) level, the EXIT command ends the test session and returns control to the ISIS-II Disk Operating System.

#### EXAMPLES

```
*EXIT<cr>
```

### 3-26. MEMORY TEST UTILITY COMMANDS

The Memory Test (Test B) includes a set of utility commands to allow the operator to selectively run the five RAM memory tests described in paragraph 3-14. These utility commands, which are defined in table 3-2, also allow the operator to (1) examine and optionally modify the test patterns, (2) display or clear the pass and error counts, and (3) display or clear the error table. Any illegal character entered in response to the Memory Test prompt (>) causes the diagnostic to print a query (?) to indicate a syntax error.

#### NOTE

Loading the Memory Test (Test B) into memory destroys the CONFID code. To execute any test other than the Memory Test, the CONFID software must be reloaded.

Typical execution times for testing the 62k of RAM on the IPC are as follows:

Test	Execution Time
Address (A)	14.7 seconds
Marching (M)	7.1 seconds
Refresh (R)	16.5 seconds
Walking (W)	2.4 hours
Galpat (G)	4.4 hours

### 3-27. RUNNING THE CONFID TEST

Step-by-step procedures for initializing CONFID and running each individual test routine are provided in table 3-3. To simplify the procedure, the software DEBUG switch is turned off by default (see paragraph 3-18); however, a list of error messages that may occur with the DEBUG switch turned on is presented in paragraph 3-28.

An individual test may be aborted by pressing the keyboard "ESC" key. (It may be necessary in some cases to press "ESC" several times to effect an

Table 3-2. CONFID Memory Test Utility Commands

Command	Syntax	Description
A	A	Run address test to locate RAM address errors.
C	C	Clear error table.
E	E	Display current pass and error counts in the form  PASS=nnnn ERRS=nnnn This message is also output during test after any key (other than ESC) is pressed. This feature gives interim test status and evidence that test is still running.
G	G[ <i>pattern</i> ]	Run standard galloping pattern (galpat) test on all IPC installed RAM, starting from 0040H. Foreground default pattern is FFH if no <i>pattern</i> is entered.
Kx	K{ A M R W G }	Loop on specified test, where x is any one of five tests (A, M, R, W, or G).
KS	KS	Loop on short tests A, M, and R.
KL	KL	Loop on all five tests (A, M, R, W, and G).
M	M[ <i>pattern</i> ]	Run marching ones and zeros test on all IPC installed RAM, starting from 0040H. Foreground default pattern is FFH if no <i>pattern</i> is entered.
P	P[ <i>new pattern</i> ]	Examine and optionally modify foreground pattern used for galpat (G), marching ones and zeros (M), and walking ones and zeros (W) test.
R	R	Test refresh circuits by writing a pattern, waiting beyond typical 2 ms refresh limit, and verifying pattern.
S	S	Display error table (most recent 20 errors) in the form  ADDRESS      EXPECTED      RECEIVED XX XX            XX            YY ·                 ·             · ·                 ·             · ·                 ·             ·
W	W[ <i>pattern</i> ]	Run walking ones and zeros test on all IPC installed RAM, starting from 0040H. Foreground default pattern is FFH if no <i>pattern</i> is entered.
Z	Z	Clear pass and error counts and return to Memory Test prompt level (>).

abort.) Aborting from Test 0 through Test A returns the program to the CONFID prompt (\*) level; aborting from Test B returns the program to the memory test prompt (>) level.

In the test procedure given in table 3-3, all operator commands and responses to CONFID test prompts are highlighted in reverse video. After you become familiar with each test routine, you will probably call

for a sequence of tests using a single command as described in paragraph 3-17.

### 3-28. CONFID ERROR MESSAGES

Error messages that may occur when running the CONFID test with the DEBUG switch turned on (DEBUG=1) are listed in table 3-4.

Table 3-3. CONFID Test Procedure

CONFID TEST INITIALIZATION
<p>Turn on system power. Monitor signs on</p> <p><b>SERIES II MONITOR, Vx.y</b></p> <p>Turn on system drive, load Series III Diagnostic Confidence Test Diskette, and press mainframe front panel RESET switch. After ISIS-II system signs on, initialize CONFID in one of the following ways.</p> <p>If your system does <i>not</i> include a hard disk subsystem, initialize CONFID as follows:</p> <pre>ISIS-II, Vx.y -CONF&lt;cr&gt; ISIS-II CONF, Vx.y *INIT CONFID&lt;cr&gt; SERIES II DIAGNOSTIC CONFIDENCE TEST, Vx.y USER RETURN *</pre> <p>If your system <i>includes</i> a hard disk subsystem, initialize CONFID as follows:</p> <pre>ISIS-II, Vx.y -:F4:CONF&lt;cr&gt; ISIS-II CONF, Vx.y *INIT :F4:CONFID&lt;cr&gt; SERIES II DIAGNOSTIC CONFIDENCE TEST, Vx.y USER RETURN *</pre> <p>Comment: CONFID is ready for execution. The following test procedure is run with error messages suppressed by default (i.e., DEBUG = 0). When finished with CONFID test session, return to ISIS-II system with EXIT command. (Refer to paragraph 3-25.) If you are unable to initialize CONFID, execute firmware diagnostics described in Chapter 2.</p>
TEST 0—PROCESSOR TEST
<pre>*TEST 0&lt;cr&gt; PROCESSOR TEST  0000H PROCESSOR TEST    "PASSED" *</pre> <p>Comment: If an error is detected, test terminates with four-digit hexadecimal address and passes control back to system Monitor. (The address is displayed as a function of the Monitor and cannot be used to isolate a malfunction.) Remaining CONFID tests are not executed because further results will be meaningless. Replace IPC-85 board and re-try test.</p>

Table 3-3. CONFID Test Procedure (Cont'd.)

TEST 1—CRT CHARACTER SET TEST
*TEST 1<cr>
<b>CRT CHARACTER SET TEST</b>
A B C D E F G H I J K L M N O P Q R S T U V W X Y Z
0 1 2 3 4 5 6 7 8 9 0
! " # \$ % & ( ) * = : - < > ? / + ; [ ] , .
***** * EXAMINE OUTPUT-TYPE P(PASS)/F(FAIL) * *****
P 0001H CRT CHARACTER SET TEST "PASSED" *
Comment: If "F" is typed, or if neither "P" nor "F" is typed, test outputs "FAILED" instead of "PASSED". (If neither "P" nor "F" is typed, test times out and assumes that test failed.) If test fails, replace IOC board and re-try test.
TEST 2—KEYBOARD CHARACTER SET TEST
*TEST 2<cr>
<b>KEYBOARD CHARACTER SET TEST</b>
***** * TYPE FOLLOWING CHARACTERS * *****
Test outputs entire keyboard character set, one character at a time, and waits for you to type appropriate characters on keyboard. Assuming ALL keys test correctly, test outputs
0002H KEYBOARD CHARACTER SET TEST "PASSED" *
Test will detect any nonfunctioning key or bad keycode, in which case it outputs
KEY INPUT ERROR EXPECTED=x RECEIVED=y
and continues test. Upon completion, test will output
0002H KEYBOARD CHARACTER SET TEST "FAILED" *
If keyboard test fails catastrophically, test terminates immediately with the message
TEST ABORTED 0002H KEYBOARD CHARACTER SET TEST "FAILED" *
Comment: If test fails, check or replace keyboard cable, keyboard, and IOC board, and re-try test.

Table 3-3. CONFID Test Procedure (Cont'd.)

## TEST 3—CRT WRITE TEST

\*TEST 3<cr>  
CRT WRITE TEST

Test outputs 18 lines (80 characters per line) of the numerals 0 through 9. Since no carriage (cursor) returns are included, last line will show if any characters have been lost (last line should be equal in length to previous 17 lines). Test then prompts

\*\*\*\*\*  
\* EXAMINE OUTPUT-TYPE P(PASS)/F(FAIL) \*  
\*\*\*\*\*

P

Test moves cursor through each printable position on CRT screen without printing characters; i.e., screen is blank. Test then prompts

\*\*\*\*\*  
\* EXAMINE OUTPUT-TYPE P(PASS)/F(FAIL) \*  
\*\*\*\*\*

P

0003H CRT WRITE TEST "PASSED"

\*

Comment: If "F" is typed, or if neither "P" nor "F" is typed, test outputs "FAILED" instead of "PASSED". (If neither "F" nor "P" is typed, test times out and assumes that test fails.) If test fails, replace IOC board and re-try test.

## TEST 4—CRT CURSOR TEST

\*TEST 4<cr>  
CRT CURSOR TEST

Test outputs a 2-inch by 3-inch rectangular pattern of asterisks (\*) and prompts

\*\*\*\*\*  
\* EXAMINE OUTPUT-TYPE P(PASS)/F(FAIL) \*  
\*\*\*\*\*

P

0004H CRT CURSOR TEST "PASSED"

\*

Comment: If "F" is typed, or if neither "P" nor "F" is typed, test outputs "FAILED" instead of "PASSED". (If neither "F" nor "P" is typed, test times out and assumes that test failed.) If test fails, replace IOC board and re-try test.

Table 3-3. CONFID Test Procedure (Cont'd.)

**TEST 5—TTY TEST**

Set teletypewriter LINE/OFF/LOCAL to LINE position; ensure that printer paper and blank paper tape are in place.

\*TEST 5<cr>

TTY TEST

DEPRESS ANY KEY ON TTY KEYBOARD

On TTY keyboard, press any key. Teletypewriter prints two lines

```
ABCDEFIGHIJKLMNOPQRSTUVWXYZ0123456789 !#$%&(*+,-./:;<=>?@[ ]  
ABCDEFIGHIJKLMNOPQRSTUVWXYZ0123456789 !#$%&(*+,-./:;<=>?@[ ]
```

and test prompts (1)

TYPE CHARACTERS FROM TTY KEYBOARD UNTIL ALTMODE KEY IS PRESSED

Type in any key(s) and verify that proper character(s) is echoed back. When finished, press "ALTMODE" key. Test prompts (2)

TURN ON TTY PUNCH

WHEN READY DEPRESS P KEY ON CRT KEYBOARD

Turn on teletypewriter tape punch. On CRT keyboard, press "P" key.

Test punches null leader, two lines of standard ASCII character set, and null trailer. Test then prompts (3)

TURN OFF TTY PUNCH

LOAD PUNCHED TAPE IN TTY READER

WHEN READY DEPRESS R KEY ON CRT KEYBOARD

Turn off teletypewriter tape punch and turn on tape reader. On CRT keyboard, press "R" key. Test reads tape and outputs

0005H TTY TEST "PASSED"

\*

Comment: Test outputs "FAILED" instead of "PASSED" if response to any of the three prompts are ignored. (Test times out and assumes that test failed.) If test fails (other than from an ignored prompt), replace IPC-85 board and re-try test.

**TEST 6—LINE PRINTER TEST**

Turn on line printer; ensure that paper is loaded.

\*TEST 6<cr>

LINE PRINTER TEST

Lineprinter prints ASCII character set on four lines as follows and then prompts

```
ABCDEFGHIJKLMNPQRSTUVWXYZ  
0123456789  
abcdefghijklmnopqrstuvwxyz  
!"#$%&(*+=:-<>?/+;[],.
```

**Table 3-3. CONFID Test Procedure (Cont'd.)**

```
*****
* EXAMINE OUTPUT-TYPE (PASS)/F(FAIL) *
*****
```

**P**  
0006H LINE PRINTER TEST "PASSED"  
\*

Comment: If "F" is typed, or if neither "P" nor "F" is typed, test outputs "FAILED" instead of "PASSED". (If neither "P" nor "F" is typed, test times out and assumes that test failed.) If test fails, replace IOC board and re-try test.

#### **TEST 7—HIGH SPEED PUNCH TEST**

Turn on high speed punch; ensure that blank paper tape is in place.

\*TEST 7<cr>  
HIGH SPEED PUNCH TEST

Punch punches null leader, two lines of standard ASCII character set, and null trailer. Test then outputs

0007H HIGH SPEED PUNCH TEST "PASSED"  
\*

Comment: Test checks only that punch accepted data; punched tape may be examined for correct data or verified in high speed reader test (Test 8). If test outputs "FAILED" instead of "PASSED", replace IOC board and re-try test.

#### **TEST 8—HIGH SPEED READER TEST**

Turn on high speed reader.

\*TEST 8<cr>  
HIGH SPEED READER TEST

LOAD HIGH SPEED READER WITH TAPE FROM PUNCH TEST  
AND DEPRESS R KEY WHEN READY TO READ TAPE

Load prepunched tape in high speed reader. On CRT keyboard, press "R" key. Test reads tape and outputs

0008H HIGH SPEED READER TEST "PASSED"  
\*

Comment: Test reads data punched in Test 7. If incorrect data is read, test outputs "FAILED" instead of "PASSED". In this case, replace IOC board and re-try test.

Table 3-3. CONFID Test Procedure (Cont'd.)

**TEST 9—FRONT PANEL INTERRUPT TEST**

\*TEST 9<cr>  
FRONT PANEL INTERRUPT TEST

\*\*\*\*\*  
\* ENTER INTERRUPT SWITCHES \*  
\*\*\*\*\*

On IPC, press interrupt switches 0-7 in any order. Test checks them in selected order, verifying that priority and jump addresses are correct. Test then outputs

0009H FRONT PANEL INTERRUPT TEST "PASSED"  
\*

Comment: Test times out and outputs "FAILED" instead of "PASSED" if one or more switches are not pressed. If test fails for any other reason, replace IPC-85 board and re-try test.

**TEST A—FLOPPY DISK TEST**

Turn on all diskette drives to be tested.

\*TEST A<cr>  
FLOPPY DISK TEST

\*\*\*WARNING\*\*\*  
DISKETTE FILES ON DRIVES TESTED WILL BE DESTROYED  
LOAD WRITE ENABLED SCRATCH DISKETTE INTO ANY DRIVE TO BE TESTED  
DEPRESS RETURN KEY WHEN READY TO CONTINUE

Load write enabled scratch diskettes into drives to be tested and press "RETURN" key.

TESTING DRIVE #0  
RECALIBRATE TEST  
FORMAT TEST  
VERIFY CRC TEST  
RANDOM READ/WRITE TEST

Test repeats for Drives #1, #2, #3, and then Integral Drive. If a drive is not present or not ready (door open, door closed and no diskette, power off, etc.), test outputs

TESTING DRIVE X  
RECALIBRATE TEST  
#DRIVE NOT READY#

After the Integral Drive is tested as shown above, a drive selection sequence is performed and repeated ten times. During this sequence, the test outputs

DRIVE SELECT SEQUENCE  
TESTING DRIVE #0  
TESTING DRIVE #1  
TESTING DRIVE #2  
TESTING DRIVE #3  
TESTING INTEGRAL DRIVE

Table 3-3. CONFID Test Procedure (Cont'd.)

After executing the sequence eleven times, test outputs

**\*\*\*WARNING\*\*\***

BEFORE PERFORMING ANY OTHER TEST THE ISIS  
SYSTEM DISKETTE MUST BE PLACED IN ITS DRIVE  
DEPRESS RETURN KEY WHEN READY TO CONTINUE

Remove scratch diskettes, place ISIS system test diskette in system drive, and press "RETURN" key.

000AH FLOPPY DISK TEST "PASSED"  
\*

Comment: Test outputs "FAILED" instead of "PASSED" if one or more of the drives are either not present or not ready. If test fails otherwise, replace appropriate board(s) and re-try test:

Integral Drive: IOC board

All Other Drives: Diskette Controller (Channel board and Interface board)

### TEST B—MEMORY TEST

This procedure runs all five basic memory tests. Hitting "ESC" key while a memory test is running aborts test and returns program to Memory Test prompt level (>). Hitting any key (other than "ESC") gives interim test status as evidence that test is still running. The memory tests do not output a "passed" or "failed" message. If test runs without errors, it outputs an audible beep and a prompt (>). If test fails, it (1) tries to restore correct memory location so error message is not repetitively output for same error, and (2) returns to currently executing test and continues executing. A typical error message heading and error data would look like:

PASS	ADDR	EXPECTED	RECEIVED	ERRS
0000	5256	55	FF	0001
0001	5256	55	FF	0002
.	.	.	.	.
.	.	.	.	.

Loading Test B (Memory Test) into memory destroys all other CONFID test code in memory. In order to execute any other test once Test B is loaded, ISIS-II system must be rebooted and CONFID reinitialized.

\*TEST B<cr>  
MEMORY TEST

Immediately after test is initiated, the system memory size is computed. If during this process a memory failure is encountered, test outputs

RAM MEMORY SIZE, 32 OR 48 OR 64? 64<cr>

>A<cr>  
ADDRESS TEST  
  
>M<cr>  
MARCH TEST  
  
>R<cr>  
REFRESH TEST  
  
>W<cr>  
WALK TEST  
  
>G<cr>  
GALPAT TEST

} See paragraph 3-26 for execution times of these tests.

Comment: For any Memory Test hard failure, replace IPC-85 and re-try test.

Table 3-4. CONFID Test Error Messages

Error Message	Probable Fault
ADDRESS ERROR	Note
CRT ILLEGAL COMMAND	IOC card
CRT ILLEGAL STATUS REQUEST	IOC card
CRT NOT PRESENT	IOC card
CRT OPERATION ERROR	CRT
DATA/ADDRESS MARK ERROR	Note
DATA CRC ERROR	Note
DATA OVERRUN	Note
DELETED RECORD ERROR	Note
DRIVE NOT READY	Note
DRIVE STATUS CHANGE	Note
FLOPPY OPERATION ERROR	Disk drive
HIGH SPEED READER DATA ERROR	Tape reader, IOC card
ID CRC ERROR	Note
INTERRUPT ERROR LEVEL X	IPC-85 board
IOC DEVICE ERROR RCV	IOC card
IOC ILLEGAL COMMAND	IOC card
IOC ILL DATA RQST	IOC card
IOC INPUT ERROR	Peripheral device
IOC OPERATION ERROR XMIT	IOC card
IOC TIMEOUT	IOC card
IOC TIMEOUT RCV	IOC card
IOC TIMEOUT XMIT	IOC card
KEY INPUT ERROR	Keyboard, cable, IOC card
KEYBD ILL STATUS REQUEST	IOC card
KEYBOARD NOT PRESENT	Keyboard, cable, IOC card
KEYBD OPERATION ERROR	Keyboard, cable
KEYBD TIMEOUT	Operator response, keyboard, cable
LPT DEVICE ERROR	Line printer
LPT ILLEGAL COMMAND	IOC card
LPT ILLEGAL STATUS REQUEST	IOC card
LPT NOT PRESENT	Line printer, cable, IOC card
LPT NOT SELECTED	IOC card
LPT TIMEOUT XMIT	IOC card
NO DISKETTE CONTROLLER PRESENT	Interface board, channel board
PIO DEVICE ERROR RCV	IOC card
PIO OPERATION ERROR	IOC card
PIO TIMEOUT	IOC card
PIO TIMEOUT RCV	IOC card
PIO TIMEOUT XMIT	IOC card
SEEK ERROR	Note
SYNC ERROR	Note
TAPE PUNCH DEVICE ERROR	Tape punch, cable
TAPE PUNCH ILLEGAL COMMAND	IOC
TAPE PUNCH ILL STATUS REQUEST	IOC card, cable
TAPE PUNCH NOT PRESENT	Tape punch, cable, IOC card
TAPE PUNCH TIMEOUT	Tape punch, cable, IOC card
TAPE RDR DEVICE ERROR	Tape reader, cable
TAPE RDR NOT PRESENT	Tape reader, cable, IOC card
TAPE READER TIMEOUT	Tape reader, cable, IOC card

**Table 3-4. CONFID Test Error Messages (Cont'd.)**

Error Message	Probable Fault
TEST ABORTED	Operator request, keyboard
TIME OUT	Note
TTY READER DATA ERROR	TTY reader, IPC-85 board
UNEXPECTED I/O COMPLETE	Note
USART 0 DEVICE ERROR	TTY, cable, IPC-85 board
USART 1 DEVICE ERROR	Device, cable, IPC-85 board
USART 0 TIMEOUT RCV	TTY, cable
USART 1 TIMEOUT RCV	Device, cable
WRITE ERROR	Note
WRITE PROTECTED	Note
	Note: Integral Drive: Drive or IOC card External Drive: Drive, controller, cable, IPC-85 board



## CHAPTER 4 CON86 CONFIDENCE TEST

### 4-1. INTRODUCTION

The CON86 confidence test, which runs under Version 4.1 (or later) of the ISIS-II Disk Operating System, provides a complete check of the resident processor board (RPB-86), including its CPU, onboard RAM memory, PROM memory, timers, and interrupts. The test also checks the system address and data lines and the offboard RAM memory.

### 4-2. TEST DESCRIPTION

The CON86 confidence test is comprised of the 19 individual tests listed below and described in following paragraphs. Once invoked, these tests run automatically without operator intervention.

Test	Function
0	DATA BUS RIPPLE TEST
1	ADDRESS BUS RIPPLE TEST
2	OFFBOARD MEMORY MARCH TEST
3	ONBOARD MEMORY MARCH TEST
4	OFFBOARD MEMORY REFRESH TEST
5	ONBOARD MEMORY REFRESH TEST
6	OFFBOARD MEMORY ADDRESS TEST
7	ONBOARD MEMORY ADDRESS TEST
8	BYTE/WORD TRANSFER TEST
9	CPU TEST
A	TIMER COUNT TEST
B	TIMER INTERRUPT TEST
C	SOFTWARE INTERRUPT TEST
D	PROM CHECKSUM TEST
E	FAILSAFE TIMER TEST
F	OFFBOARD MEMORY GALPAT TEST
10	ONBOARD MEMORY GALPAT TEST
11	OFFBOARD MEMORY WALK TEST
12	ONBOARD MEMORY WALK TEST

The entire 62k of RAM memory located on the RPB-86 processor board is checked during the onboard memory tests. The test range for the offboard memory tests may be specified using the V variables described in paragraph 4-22.

### 4-3. TEST 0—DATA BUS RIPPLE TEST

Using absolute address 1F000H as the test location, this test ripples a logic 1 across the data bus. Data is written to the test location and verified as each data line becomes a logic 1. If an error occurs, the test displays immediately the failing address together with the expected versus received data.

### 4-4. TEST 1—ADDRESS BUS RIPPLE TEST

Using 10000H as the absolute starting address, this test writes 00H into RAM memory while rippling a logic 1 across the address bus. For each test location, the data is read, complemented, and read again for verification. This test is performed only page 1 in offboard memory (absolute locations 10000H-1FFFFH). If a failure occurs, the test displays immediately the failing address together with the expected versus received data.

### 4-5. TEST 2—OFFBOARD MEMORY MARCH TEST

Using the V variables to establish the offboard RAM memory test range, this test marches (writes) a pattern of ones and zeroes through memory to provide a quick check for stuck cells and addressing problems. The test first marches a background pattern (5AA5H) upward through memory and then marches the complement (A55AH) downward through memory, checking the data after each write operation. If a failure occurs, the test displays immediately the failing address together with the expected versus received data.

### 4-6. TEST 3—ONBOARD MEMORY MARCH TEST

This test marches (writes) a pattern of ones and zeros through RAM memory on the RPB-86 board to provide a quick check for stuck cells and addressing problems. The test first marches a background pattern (5AA5H) upward through memory and then marches the complement (A55AH) downward through memory, checking the data after each write operation. If a failure occurs, the test displays at the end of the test the failing address(es) together with the expected versus received data.

### 4-7. TEST 4—OFFBOARD MEMORY REFRESH TEST

Using the V variables to establish the offboard RAM memory test range, this test writes a background pattern (FFH) to all locations, waits beyond the 2-millisecond refresh cycle, and checks for changes in data. The test then complements the pattern (00H) and repeats the write, wait, and check sequence. If a failure occurs, the test displays immediately the failing address together with the expected versus received data.

#### **4-8. TEST 5—ONBOARD MEMORY REFRESH TEST**

This test writes a background pattern (FFH) to all RAM memory locations on the RPB-86 board, waits beyond the 2-millisecond refresh cycle, and checks for changes in data. The test then complements the pattern (00H) and repeats the write, wait, and check sequence. If a failure occurs, the test displays at the end of the test the failing address(es) together with the expected versus received data.

#### **4-9. TEST 6—OFFBOARD MEMORY ADDRESS TEST**

Using the V variables to establish the offboard RAM memory test range, this test locates RAM addressing problems. The test checks the integrity of the low byte addresses by writing values 0-255 in corresponding bytes of each 256-byte block and then verifying the contents. The test checks the integrity of the high byte addresses by writing a block number (starting with 1) in the tenth byte of each sequential 256-byte block and then verifying the contents. If an error occurs, the test displays immediately the failing address together with the expected versus received data.

#### **4-10. TEST 7—ONBOARD MEMORY ADDRESS TEST**

This test locates RAM addressing problems associated with RAM memory on the RPB-86 board. The test checks the integrity of the low byte addresses by writing values 0-255 in corresponding bytes of each 256-byte block and then verifying the contents. The test checks the integrity of the high byte addresses by writing a block number (starting with 1) in the tenth byte of each sequential 256-byte block and then verifying the contents. If an error occurs, the test displays at the end of the test the failing address(es) together with the expected versus received data.

#### **4-11. TEST 8—BYTE/WORD TRANSFER TEST**

This test performs both byte (8-bit) and word (16-bit) data transfers to onboard and offboard RAM memory. Absolute addresses 0F000H and 0F001H are the test locations in onboard memory; absolute addresses 1F000H and 1F001H are the test locations in offboard memory. If a failure occurs, the test displays immediately the failing address together with the expected versus received data.

#### **4-12. TEST 9—CPU TEST**

This test executes the 8086 microprocessor instruction set and verifies the results. If a failure occurs, the test terminates immediately; execution of the remaining tests should not be attempted because the results would be meaningless.

#### **4-13. TEST A—TIMER COUNT TEST**

This test, which verifies the count accuracy of the 8253 Programmable Interval Timer chip, programs counter 1 to interrupt on terminal count (mode 0). At a specified time, the count is read and compared with the expected results. If an error occurs, the test displays immediately the counter number together with the expected versus received count.

#### **4-14. TEST B—TIMER INTERRUPT TEST**

This test, which checks the interrupt capability of the 8253 Programmable Interval Timer, programs counter 0 to interrupt on terminal count (mode 0). The test verifies that interrupt level 2 is generated when counter 0 reaches the terminal count. If the test fails, it outputs a FAILED message.

#### **4-15. TEST C—SOFTWARE INTERRUPT TEST**

This test checks all 256 software interrupts, the interrupt on overflow (INTO) condition, and the single-step capability. If an error occurs, the test displays immediately the type of failure.

#### **4-16. TEST D—PROM CHECKSUM TEST**

This test reads the DEB86 PROM and computes and verifies its checksum. If the PROM cannot be read or if the checksum is wrong, the test outputs a FAILED message.

#### **4-17. TEST E—FAILSAFE TIMER TEST**

This test attempts to read a non-existent absolute memory location (F0000H) and verifies that the failsafe timer on the IPC-85 board times out approximately 10 milliseconds after the read command is issued. (Note that for this test to execute properly, location F0000H must not be existent in the system.) If the test fails, it outputs a FAILED message.

#### **4-18. TEST F—OFFBOARD MEMORY GALPAT TEST**

Using the V variables to establish the offboard RAM memory test range, this test gallops (writes) a pattern of ones and zeroes through memory to check for pattern sensitivity and access problems. The test initially writes 00H as a background pattern into all locations. Then, starting at the low end of memory, the test (1) establishes the first test location, (2) writes FFH into that test location, and (3) reads all other locations to verify that the data is unchanged. Between each of these read operations, the test also verifies that the pattern in the first test location remains unchanged. After completing this procedure for the first test location, the test (1) complements the pattern in the first test location, (2) writes FFH into the second test location (next sequential address), and (3) reads and verifies memory as stated above. This method of selecting test locations and checking all other locations continues until the range of memory is tested. If a failure occurs, the test displays immediately the failing address together with the expected versus received data.

#### **4-19. TEST 10—ONBOARD MEMORY GALPAT TEST**

This test gallops (writes) a pattern of ones and zeroes through RAM memory on the RPB-86 board to check for pattern sensitivity and access problems. The test initially writes 00H as a background pattern to all locations. Then, starting at the low end of memory, the test (1) establishes the first test location, (2) writes FFH into that test location, and (3) reads all other locations to verify that the data is unchanged. Between each of these read operations, the test also verifies that the pattern in the first test location remains unchanged. After completing this procedure for the first test location, the test (1) complements the pattern in the first test location, (2) writes FFH into the second test location (next sequential address), and (3) reads and verifies memory as stated above. This method of selecting test locations and checking all other locations continues until all 62k of RAM memory is tested. If a failure occurs, the test displays at the end of the test the failing address(es) together with the expected versus received data.

#### **4-20. TEST 11—OFFBOARD MEMORY WALK TEST**

This test is an abbreviated two-pass version of the offboard RAM memory galpat test. Using the V variables to establish the RAM memory test range, the test initially writes 00H as a background pattern

into all locations. Starting at the low end of memory, the test (1) establishes the first test location, (2) writes FFH into that location, and (3) reads the background locations to verify that the data is unchanged. The test then complements the pattern in the first test location, writes FFH into the second test location (next sequential address), and then reads the background locations. This process is repetitive until a one is “walked” through the test range. If a failure occurs, the test displays immediately the failing address together with the expected versus received data.

#### **4-21. TEST 12—ONBOARD MEMORY WALK TEST**

This test is an abbreviated two-pass version of the onboard RAM memory galpat test. The test initially writes 00H as a background pattern into all locations and, starting at the low end of memory, (1) establishes the first test location, (2) writes FFH into that location, and (3) reads the background locations to verify that the data is unchanged. The test then complements the pattern in the first test location, writes FFH the second test location (next sequential address), and then reads the background locations. This process is repetitive until a one is “walked” through the test range. If a failure occurs, the test displays at the end of the test the failing address(es) together with the expected versus received data.

#### **4-22. V VARIABLES**

The 1-megabyte address space of the 8086 microprocessor is divided in 16 pages of 64k bytes each. Page 0 is the RPB-86 onboard RAM memory, page 1 is the first (standard) offboard 64k RAM board, and pages 2 through F are reserved for system RAM expansion. (The top 16k of page F is the RPB-86 onboard PROM memory and any attempt to test this area will generate an error message).

Variables V(0) through V(4) are used by the offboard RAM memory tests to determine the test range. If the variables are not specified, testing defaults to page 1 and tests all 64k locations (absolute addresses 10000H through 1FFFFH).

Variable V(0) is the test descriptor where

V(0) = 0 tests page 1 only.

V(0) = 1 tests a range of offboard memory; the starting and ending addresses are determined by V(1), V(2), V(3), and V(4). When V(0) = 1, indicating a

range of memory to test, the starting and ending addresses are compared. If the range specified is less than 256 bytes, the test aborts and outputs an error message.

- V(0) = 2** tests all offboard memory; the ending address is determined by V(3) and V(4).

Variable V(1) specifies the starting page number, which must be in the range 1 through F.

Variable V(2) defines the 16-bit offset address within the page number specified by V(1). To determine the absolute starting address, the test simply appends the offset to the page number specified by V(1). For example, if V(1) = 2 and V(2) = FC20H, the absolute starting address is 2FC20H. The offset defined by V(2) can be any number from 0H to FFFFH.

Variable V(3) specifies the ending page number, which must be in the range 1 through F.

Variable V(4) defines the 16-bit offset address within the page specified by V(3). To determine the absolute ending address, the test simply appends the offset to the page number specified by V(3). For example, if V(3) = 3 and V(4) = A400H, the absolute ending address is 3A400H. The offset defined by V(4) can be any number from 0H to FFFFH.

The V variables must be specified before commencing the test of offboard RAM memory, otherwise the testing defaults to the first 64k RAM board. Each variable may be entered individually or entered as a string. In the examples given below, the asterisk (\*) is the prompt for operator input and the <cr> denotes the RETURN key; for clarity, operator entries are shown in reverse video.

**Example 1.** Test all offboard RAM memory (assuming two 64k RAM boards and one 32k RAM board). Each variable can be individually input as follows:

```
*V(0) = 2<cr>
*V(3) = 3<cr>
*V(4) = 7FFFH<cr>
```

In this example, the test range is 10000H (the absolute starting address on the first 64k RAM board) to 37FFFH (the absolute ending address on the 32k RAM board).

Alternatively, the same V variables can be input as a string as follows:

```
*V(0) LEN 5 = 2,0,0,3,7FFFH<cr>
```

**Example 2.** Test offboard memory from 27000H to 42000H.

```
*V(0) LEN 5 = 1,2,7000H,4,2000H<cr>
```

Note that in this example the starting absolute address as well as the ending absolute address must be specified.

**Example 3.** Once the V variables have been specified, the same test range is used in all subsequent offboard RAM testing until a new set of variables is specified. The V variables are cleared automatically when exiting CON86, and may be cleared during a CON86 test session as follows:

```
*V(0) = 0<cr>
```

After the V variables are thus cleared, subsequent offboard RAM memory testing will be done on page 1 only.

## 4-23. COMMAND SYNTAX CONVENTIONS

Table 4-1 summarizes the syntax convention used in the test commands described in following paragraphs.

Table 4-1. CON86 Command Syntax Conventions

Notation	Description
UPPERCASE letters	Elements in uppercase are specific keywords that must be entered exactly as shown (or abbreviated as described in paragraph 4-24).
<i>lowercase italics</i>	Elements in lowercase italics identify tokens. From each set, select and enter a specific identifier.
...	Elements followed by an ellipsis (...) may be repeated indefinitely.
[ ]	When only one element is enclosed in brackets, that element is optional. When two or more elements are enclosed in brackets, ALL elements are optional, but only ONE element may be entered.
{ }	One, and <i>only</i> one, of the elements enclosed in braces must be entered.

## 4-24. TEST COMMANDS

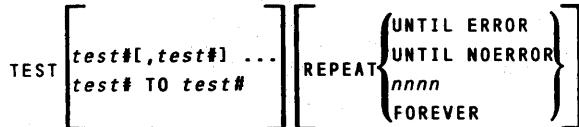
There are 11 commands that allow the operator to specify the test sequence and report the result in an orderly manner. These test commands are described in following paragraphs. As shown below, any command consisting of four or more letters can be abbreviated to the first three letters of the command. Additionally, the letter T is accepted as an abbreviation for TEST.

Command	Abbreviation	Paragraph
TEST	TES (or T)	4-25
ERRONLY	ERR	4-26
DEBUG	DEB	4-27
LIST	LIS	4-28
SUMMARY	SUM	4-29
CLEAR	CLE	4-30
DESCRIBE	DES	4-31
IGNORE	IGN	4-32
RECOGNIZE	REC	4-33
REPEAT	REP	4-34
EXIT	EXI	4-35

The function and syntax of each command, including examples, are given in paragraphs 4-25 through 4-35. In the examples, all operator input is shown in **reverse video**. The asterisk (\*) is the prompt for operator input and the <cr> denotes the RETURN key.

## 4-25. TEST COMMAND

### SYNTAX



where

*test#* is a test number as listed and described in paragraphs 4-3 through 4-21, and

*nnnn* is the number of test iterations in hexadecimal (H), decimal (T), octal (Q), or binary (Y); the default number base is hexadecimal if the base suffix (H, T, Q, or Y) is omitted. The maximum number of iterations specifiable by *nnnn* is 65,535<sub>10</sub>.

### DESCRIPTION

The TEST command uses the operator-supplied elements to load and execute one or more software procedures (i.e., tests). The tests are executed in numerical order regardless of the order in which they are specified. If a *test#* (i.e., test number) is specified for which no test exists, an error results. If no *test#* is specified, all 19 tests will be executed.

The REPEAT element, together with one of its four modifiers FOREVER, UNTIL ERROR, UNTIL NOERROR, and *nnnn*, allows the selected test(s) to be repeated.

If REPEAT FOREVER is specified, or if REPEAT is specified without a modifier, the tests will execute in numerical order, regardless of errors, and loop repeatedly until the operator hits the CNTL and C (CNTL-C) keys simultaneously.

When REPEAT UNTIL ERROR is specified, the test(s) will execute in numerical order and loop only until one or more of the tests return an error condition.

When REPEAT UNTIL NOERROR is specified, the test(s) will execute in numerical order and loop until all tests run without error.

When REPEAT *nnnn* is specified, the test(s) will execute in numerical order *nnnn* times. If *nnnn* = 0, the tests will not be executed, although the first test will be loaded into memory.

### EXAMPLES

- Run all tests (0-12 hexadecimal) in numerical sequence; the setting of V variables is not required because only one 64k RAM board is in the system.  
**\*TEST<cr>**
- Run a single test (e.g., Test B).  
**\*TEST B<cr>**
- Run Tests A, B, C, and D as long as one or more of these tests fail.  
**\*TEST A TO D REPEAT UNTIL NOERROR<cr>**
- Run Tests 9, C, D, and E until one or more of these tests fail.  
**\*TEST 9, C TO E REPEAT UNTIL ERROR<cr>**
- Run Test A 500 (decimal) times.  
**\*TEST A REPEAT 500<cr>**

6. Run Tests B and C continuously regardless of error or no error.

```
*TEST B, C REPEAT FOREVER<cr>
—or—
*TEST B, C REPEAT<cr>
```

7. Run Tests 4, 6, and 8 on all offboard RAM memory (assume system includes one 64k RAM board and one 32k RAM board).

```
*V(0) LEN 5 = 2,0,0,2,7FFFH<cr>
*TEST 2,4,6<cr>
```

8. Run Test 12 on offboard RAM absolute locations 10100H to 10200H.

```
*V(0) LEN 5 = 1,1,100H,1,200H<cr>
*TEST 12<cr>
```

#### 4-26. ERONLY Command

##### SYNTAX

```
ERONLY = 0
ERONLY = 1
```

##### DESCRIPTION

The ERONLY command is used to selectively suppress (ERONLY = 1) or display (ERONLY = 0) "PASSED" messages. The erronly switch is cleared during CON86 initialization (i.e., the default condition is ERONLY = 0).

##### EXAMPLES

1. Run Test 9 ten (decimal) times and suppress PASSED messages.

```
*ERR = 1<cr>
*TEST 9 REPEAT 10T<cr>
```

If no errors occur, the test displays only the prompt (\*) after the tenth test iteration.

2. Run Test 9 fifty (hexadecimal) times and print PASSED or FAILED message. (Assumes that ERR = 1 has been entered previously.)

```
*ERR = 0<cr>
*TEST 9 REPEAT 50<cr>
```

#### 4-27. DEBUG COMMAND

##### SYNTAX

```
DEBUG = 0
DEBUG = 1
```

##### DESCRIPTION

The DEBUG command is used to selectively suppress or display error messages. The debug switch is cleared during CON86 initialization (i.e., the default condition is DEBUG = 0).

##### EXAMPLES

1. Run Test 9 through Test C and display error messages.

```
*DEBUG = 1<cr>
*TEST 9 TO C<cr>
```

2. Run Test C 100 (octal) times and suppress error messages. (Assumes that DEBUG = 1 has been entered previously.)

```
*DEBUG = 0<cr>
*TEST C REPEAT 100Q<cr>
```

#### 4-28. LIST COMMAND

##### SYNTAX

```
LIST 'pathname'
```

##### DESCRIPTION

The LIST command causes a copy of all subsequent output, including prompts, input, line echo, and error messages, to be sent to the ISIS-II file *pathname*. If the ':CO:' (the console display) is specified, there is effectively no list file (the initial setting).

##### EXAMPLE

1. Run Test 5 and print (copy) all output, including error messages, on line printer.

```
*DEBUG = 1<cr>
*LIST ':LP:'<cr>
*TEST 5<cr>
```

#### 4-29. SUMMARY COMMAND

##### SYNTAX

```
SUMMARY [test# [,test#]...] [EO]
[ test# TO test# ]
```

**DESCRIPTION**

For each specified test, the following information is displayed by the SUMMARY command: the test number, the number of times executed, the number of times an error occurred, and whether the test was ignored or not. If no test(s) is specified, a summary of all tests will be included. If EO (Errors Only) is specified, only those tests with a non-zero error count will be displayed. The summary listing will be concluded with a statement as to whether any of the specified tests show a non-zero error count. Note that all error counts are given in hexadecimal.

**EXAMPLES**

1. Display summary of Tests A, B, and C.

```
SUMMARY A TO C<cr>
0000AH TIMER COUNT TEST
    0001 FAILED IN 105A TRIALS ←
0000BH TIMER INTERRUPT TEST
    0000 FAILED IN 01FF TRIALS ←
0000CH SOFTWARE INTERRUPT TEST
    000C FAILED IN 1FFF TRIALS ←
```

2. Display summary of Tests A, B, and C only if a non-zero error count exists.

```
*SUMMARY A TO C EO<cr>
0000BH TIMER INTERRUPT TEST
    0001 FAILED IN 01FF TRIALS ←
```

**4-30. CLEAR COMMAND****SYNTAX**

```
CLEAR [test# [,test#]...]
      [test# TO test#]
```

**DESCRIPTION**

For each specified test, or for all tests if *test* range is missing, the execution count and the error count are set to zero. The CLEAR command does not affect the status (ignored or recognized) of a test, nor is the CLEAR command affected by the status of a test.

**EXAMPLE**

1. Clear execution count and error count on Tests A, B, and C.

```
*CLEAR A,B,C<cr>
```

**4-31. DESCRIBE COMMAND****SYNTAX**

```
DESCRIBE [test# [,test#]...]
          [test# TO test#]
```

**DESCRIPTION**

The DESCRIBE command displays the name, or description, of the specified test(s), and whether the test(s) would be ignored by the TEST command. If *test* range is missing, the descriptions of all tests will be displayed.

**EXAMPLE**

1. Describe Tests 9, A, B, and C. (Assume that the IGNORE command has previously been specified for Test 9.)

```
*DESCRIBE 9 TO C<cr>
00009H CPU TEST ****IGNORED****
0000AH TIMER COUNT TEST
0000BH TIMER INTERRUPT TEST
0000CH SOFTWARE INTERRUPT TEST
```

**4-32. IGNORE COMMAND****SYNTAX**

```
IGNORE [test# [,test#]...]
       [test# TO test#]
```

**DESCRIPTION**

The IGNORE command allows the operator, at the beginning of the CON86 session, to declare which test(s) is not to be run. The IGNORE command remains valid until negated, all or in part, by the RECOGNIZE command.

**EXAMPLE**

1. Run all tests except Tests 5, 6, and 8.

```
*IGNORE 5,6,8<cr>
*TEST<cr>
```

### 4-33. RECOGNIZE COMMAND

#### SYNTAX

```
RECOGNIZE [test# [, test#]...]
          test# TO test#
```

#### DESCRIPTION

The RECOGNIZE command allows the operator to negate all or part of a previously issued IGNORE command.

#### EXAMPLE

1. Assume that Tests 5, 6, and 8 are presently ignored and it is desired to run all tests except Test 6; i.e., Test 6 will remain ignored.

```
*RECOGNIZE 5,8<cr>
*TEST <cr>
```

### 4-34. REPEAT COMMAND

#### SYNTAX

```
REPEAT [nnnn]
      :
ENDR
```

where

*nnnn* is the number of repeat iterations in hexadecimal (H), decimal (T), octal (Q), or binary (Y); the default number base is hexadecimal if the base suffix (H, T, Q, or Y) is omitted. The maximum number of repeat iterations specifiable by *nnnn* is 65,535<sub>10</sub>.

#### DESCRIPTION

This compound command repeats the sequence of test commands between REPEAT and ENDR (end repeat). The default condition is "forever" if *nnnn* is not specified. Note in the example below that a nested prompt (\*) is issued while inputting the REPEAT command parameters.

#### EXAMPLE

1. Over an extended period of time, compile a cumulative list and a backup list of the test summary.

```
*REPEAT<cr>
.*LIST 'X.LST'<cr>
.*TEST<cr>
.*SUMMARY<cr>
.*LIST 'Y.LST'<cr>
.*TEST<cr>
.*SUMMARY<cr>
.*ENDR<cr>
```

### 4-35. EXIT COMMAND

#### SYNTAX

EXIT

#### DESCRIPTION

When at the CON86 prompt (\*) level, the EXIT command ends the test session and returns control to the ISIS-II Disk Operating System.

#### EXAMPLE

```
*EXIT<cr>
```

### 4-36. MULTIPLE COMMANDS PER LINE

Two or more of the CON86 commands (except the compound command REPEAT...ENDR) may be entered on a single line as follows:

```
cmd1; cmd2; cmd3; ... ; cmdn
```

Each command must be separated by a semicolon, and the execution of commands is from left to right. For example, the multiple command

```
*TEST 9; TEST 3; SUMMARY; EXIT<cr>
```

runs Test 9 and then Test 3, outputs a test summary, and returns control to the ISIS-II Disk Operating System. Alternatively, the same multiple command may be abbreviated as follows:

```
*T 9; T 3; SUM; EXI<cr>
```

### 4-37. RUNNING THE CON86 TEST

Step-by-step procedures for initializing CON86 and running the test routine are provided in table 4-2. To simplify the procedure, the software DEBUG switch is turned off by default (see paragraph 4-27); however, a list of error messages that may occur with the DEBUG switch turned on is presented in paragraph 4-38.

Any test in progress may be aborted by simultaneously pressing the CNTL and C (CNTL-C) keys, which returns the program to the CON86 prompt (\*) level. Note that it may take up to 20 seconds to effectively abort an onboard memory test because the test manager must restore the original onboard memory contents. If you abort any onboard memory test, the test will print out any errors that occurred before the abort command. Execution times for testing the 62k bytes of onboard memory and 64k bytes of offboard memory are as follows:

Test	Function	Execution Time
2	OFFBOARD MEMORY MARCH	6 seconds
3	ONBOARD MEMORY MARCH	9 seconds
4	OFFBOARD MEMORY REFRESH	43 seconds
5	ONBOARD MEMORY REFRESH	1.5 minutes
6	OFFBOARD MEMORY ADDRESS	9 seconds
7	ONBOARD MEMORY ADDRESS	14 seconds
F	OFFBOARD MEMORY GALPAT	4.45 hours
10	ONBOARD MEMORY GALPAT	4.45 hours
11	OFFBOARD MEMORY WALK	2.56 hours
12	ONBOARD MEMORY WALK	2.56 hours

### 4-38. CON86 ERROR MESSAGES

Error messages that may occur when running the CON86 test with the DEBUG switch turned on (DEBUG=1) are listed in table 4-3.

Table 4-2. CON86 Test Procedure

CON86 TEST INITIALIZATION
Turn on system power. Monitor signs on
SERIES II MONITOR, Vx.y
.
Turn on system drive, load Series III Diagnostic Confidence Test Diskette, and press mainframe front panel RESET switch. After ISIS-II system signs on, initialize CON86 in one of the following ways.
If your system does <i>not</i> include a hard disk subsystem, initialize CON86 as follows:
ISIS-II, Vx.y -RUN CON86<cr> SERIES III DIAGNOSTIC CONFIDENCE TEST, Vx.y *
If your system <i>includes</i> a hard disk subsystem, initialize CON86 as follows:
ISIS-II, Vx.y -F4:RUN :F4:CON86<cr> SERIES III DIAGNOSTIC CONFIDENCE TEST, Vx.y *
Comment: CON86 is ready for execution. If you are unable to initialize CON86, initialize and run CONFID test as described in Chapter 3.

Table 4-2. CON86 Test Procedure (Cont'd.)

**CON86 TEST EXECUTION**

The following test procedure, which is run with error messages suppressed by default (i.e., DEBUG=0), presumes two offboard 64k RAM boards are present.

Note: The V variables can be omitted if only one 64k RAM board is present. (Refer to paragraph 4-23.) Tests F through 12 may be omitted unless testing overnight to locate intermittent RAM failures.

```
*V(0) LEN 5 = 2,0,0,2,FFFFH<cr>
*TEST<cr>
```

0000H	DATA BUS RIPPLE TEST	"PASSED"
0001H	ADDRESS BUS RIPPLE TEST	"PASSED"
0002H	OFFBOARD MEMORY MARCH TEST	"PASSED"
0003H	ONBOARD MEMORY MARCH TEST	"PASSED"
0004H	OFFBOARD MEMORY REFRESH TEST	"PASSED"
0005H	ONBOARD MEMORY REFRESH TEST	"PASSED"
0006H	OFFBOARD MEMORY ADDRESS TEST	"PASSED"
0007H	ONBOARD MEMORY ADDRESS TEST	"PASSED"
0008H	BYTE/WORD TRANSFER TEST	"PASSED"
0009H	CPU TEST	"PASSED"
000AH	TIMER COUNT TEST	"PASSED"
000BH	TIMER INTERRUPT TEST	"PASSED"
000CH	SOFTWARE INTERRUPT TEST	"PASSED"
000DH	PROM CHECKSUM TEST	"PASSED"
000EH	FAILSAFE TIMER TEST	"PASSED"
000FH	OFFBOARD MEMORY GALPAT TEST	"PASSED"
0010H	ONBOARD MEMORY GALPAT TEST	"PASSED"
0011H	OFFBOARD MEMORY WALK TEST	"PASSED"
0012H	ONBOARD MEMORY WALK TEST	"PASSED"

\*

After the last test is executed and the test prompt is displayed, return to the ISIS-II system with the EXIT command:

```
*EXIT<cr>
ISIS-II, Vx.y
-
```

Comment: If an error occurs in any test, the test outputs "FAILED" instead of "PASSED".

**Table 4-3. CON86 Test Error Messages**

Test	Error Message			Probable Fault
0	ADDRESS XXXXH	EXPECTED XXH	RECEIVED XXH	Off board RAM,* RPB-86 board
1	Same as Test 0			Offboard RAM,* RPB-86 board
2	Same as Test 0			Offboard RAM*
2	V VARIABLE ERROR			Wrong V variable input
3	Same as Test 0			RPB-86 board
4	Same as Test 0			Offboard RAM*
4	V VARIABLE ERROR			Wrong V variable input
5	Same as Test 0			RPB-86 board
6	Same as Test 0			Offboard RAM*
6	V VARIABLE ERROR			Wrong V variable input
7	Same as Test 0			RPB-86 board
8	Same as Test 0			Offboard RAM,* RPB-86 board
9	Same as Test 0			RPB-86 board
A	COUNTER 1 IS NOT ACCURATE, EXPECTED E8H, RECEIVED XXH			RPB-86 board
B	NO INTERRUPT OCCURRED			RPB-86 board
B	MASK REGISTER FAILURE			RPB-86 board
B	WRONG VECTOR ADDRESS			RPB-86 board
C	SOFTWARE INTERRUPT LEVEL XXH FAILED			RPB-86 board
C	SOFTWARE INTERRUPT ON OVERFLOW OCCURRED			RPB-86 board
C	SINGLE STEP INTERRUPT FAILED			RPB-86 board
D	FAILED			RPB-86 board
E	FAILED			IPC-85 board
F	Same as Test 0			Offboard RAM*
F	V VARIABLE ERROR			Wrong V variable input
10	Same as Test 0			RPB-86 board
11	Same as Test 0			Offboard RAM*
11	V VARIABLE ERROR			Wrong V variable input
12	Same as Test 0			RPB-86 board

\*Page number of defective offboard RAM board (see tables 5-1 and 5-2) is identified by most-significant hexadecimal digit in ADDRESS portion of error message.

### 5-1. INTRODUCTION

This chapter provides step-by-step procedures for installing options to the Intellec Series III system. Before adding any option to your system, refer to tables 1-2 and 1-3 and ensure that the reserve capacity of the mainframe and/or expansion chassis power supply is adequate to support the additional current demand. Before starting to install a kit, unpack it and perform an incoming inspection as described in Chapter 2 (paragraph 2-2).

#### CAUTION

To prevent possible equipment damage, do not install a board in or remove a board from the cardcage while power is applied to the chassis!

### 5-2. EXPANSION CHASSIS

The optional expansion chassis, which includes an integral power supply, provides a cardcage with four additional slots. The expansion chassis may be included as part of the *initial system installation* or may be added as an *operational system upgrade*.

### 5-3. INITIAL SYSTEM INSTALLATION

Before commencing the initial installation of the basic system as described in paragraph 2-4, perform the electrical and mechanical interconnection between the mainframe and expansion chassis as follows:

#### NOTE

If the initial installation also includes an optional dual double density diskette drive(s), perform all steps (steps a through o) of the following procedure. If the initial installation does *not* include an optional dual double density drive(s), omit steps a through g.

- a. Referring to figure 5-1, rotate the two expansion chassis front panel retaining screws counter-clockwise and remove front panel.
- b. Loosen the two expansion chassis top cover retaining screws and remove top cover. (See figure 5-2.)
- c. Remove the four screws securing rear panel to expansion chassis. (See figure 5-2.) Pull edge of rear panel away from chassis to allow connector installation in top and bottom connector holes.

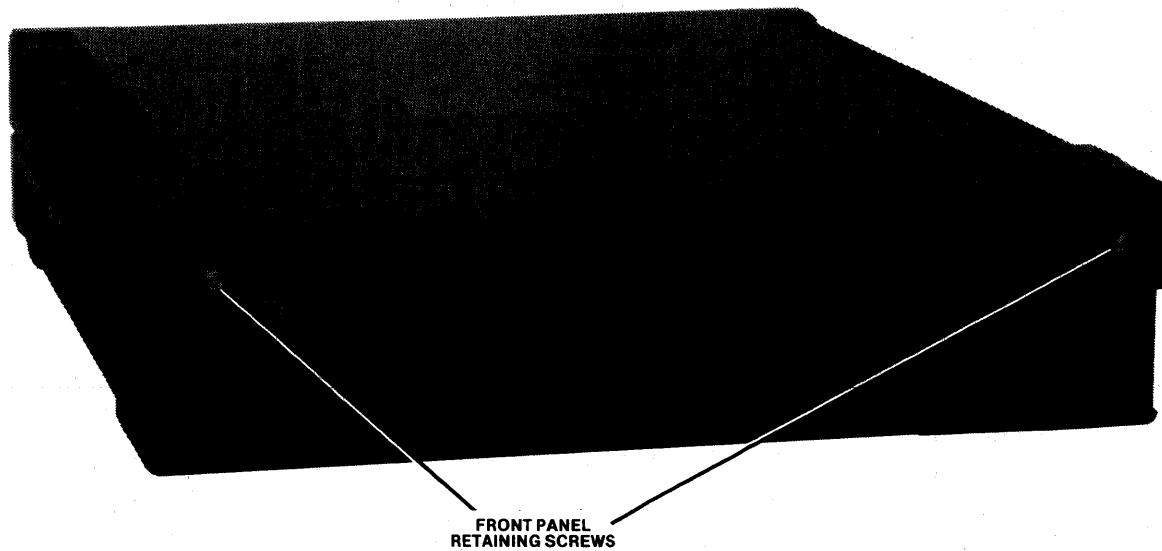


Figure 5-1. Expansion Chassis (Front View)

121612-10

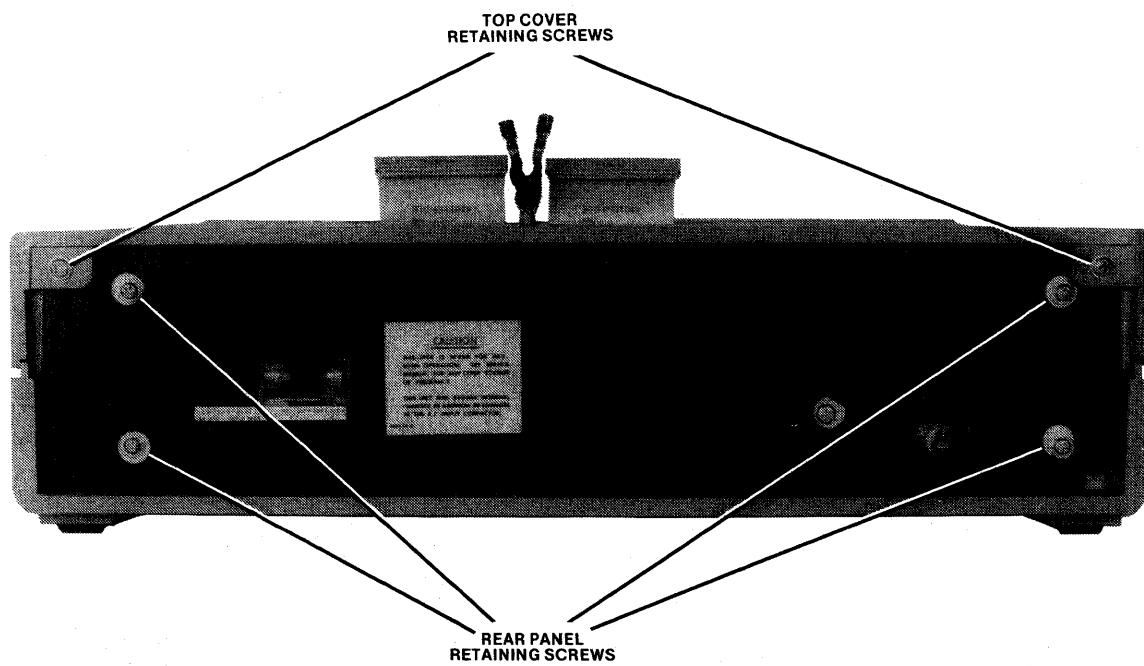


Figure 5-2. Expansion Chassis (Rear View)

121612-11

- d. The controller cable has a hooded 100-pin connector on one end and two 37-pin connectors labeled "J8 DRIVE 0,1" and "J9 DRIVE 2,3" on opposite end. Using hardware supplied, install connector labeled "J8 DRIVE 0,1" in top hole on rear panel.
- e. Install connector labeled "J9 DRIVE 2, 3" in bottom hole on rear panel.
- f. Route cable along inside right-hand edge of chassis (as viewed from rear). Make certain that there is ample cable slack to allow hooded connector to be attached to front edge of controller interface board when installed in cardcage.
- g. Reinstall rear panel and top cover.

**CAUTION**

The mainframe weighs 86 pounds (39 kilograms). To prevent personal injury and/or equipment damage, have someone assist in performing steps h through m.

- h. Turn mainframe on its side as shown in figure 5-3. Remove cable port covers from mainframe and expansion chassis.
- i. Refer to figure 5-4 and remove jumpers W1 and W2 from underneath connector J16 (accessible through mainframe cable port). Save port covers

- and jumpers in case expansion chassis is disconnected from mainframe in future.
- j. Using supplied hardware, install ground strap on expansion chassis as shown in figure 5-5. Connect the two bus extension cables to connectors inside expansion chassis cable port.
- k. Place mainframe on top of expansion chassis and tilt it backward.
- l. Holding mainframe tilted backward, connect the other ends of the two bus extension cables to J14 and J16 inside mainframe cable port. Attach quick-disconnects on ground strap to the two ground lugs between J14 and J16.
- m. Lower mainframe in place over expansion chassis. Attach aluminum ground strip between rear panels of mainframe and expansion chassis as shown in figure 5-6.
- n. On rear panel of expansion chassis, disconnect power cord (if connected) and slide fuse holder door on main power socket to left. (Refer to figure 5-7.) Remove voltage switching card and reinstall it in position corresponding to your available commercial power. Verify that proper fuse is installed: 4A normal-blow fuse for 100V or 120V; 2A normal-blow fuse for 220V or 240V. Close fuse holder door.
- o. Install basic system as described in paragraph 2-4.

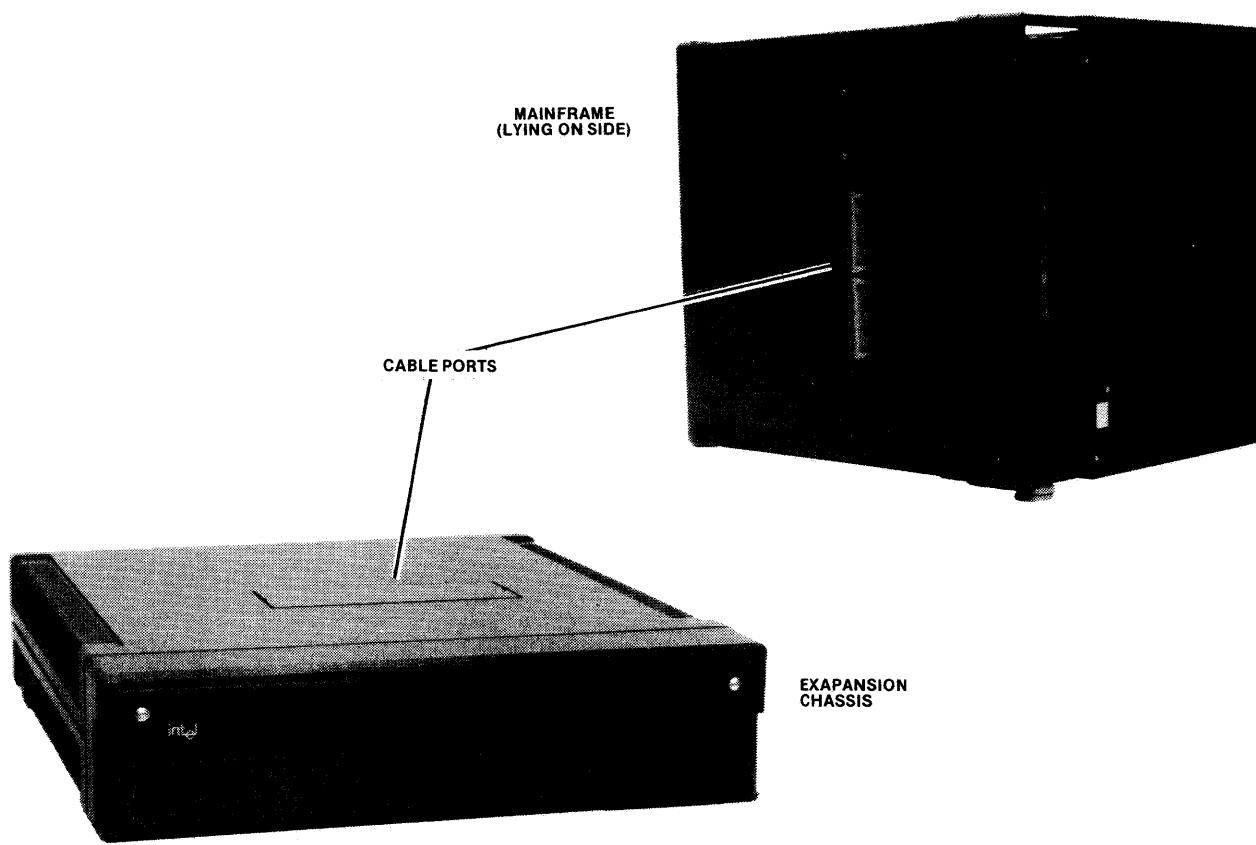


Figure 5-3. Mainframe and Expansion Chassis Cable Ports

121612-12

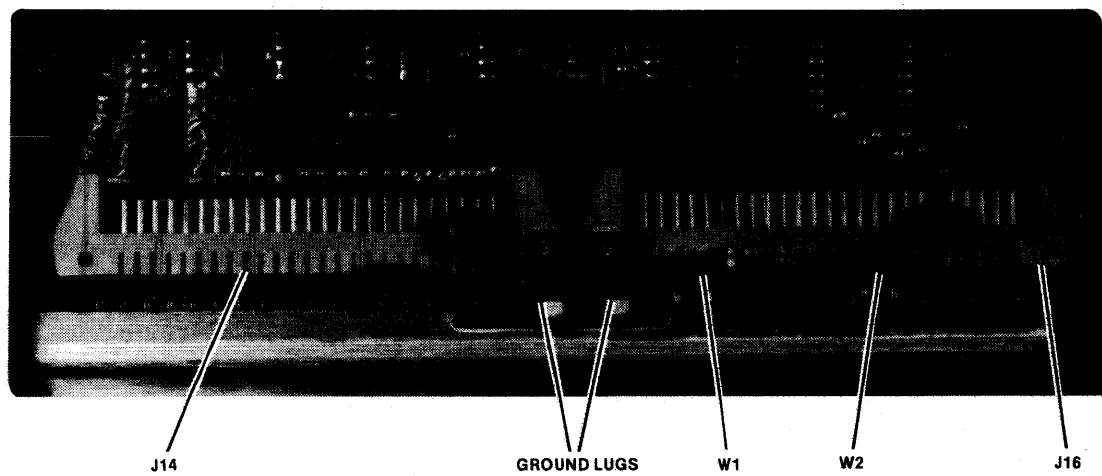


Figure 5-4. Mainframe Cable Port Details

559-75A

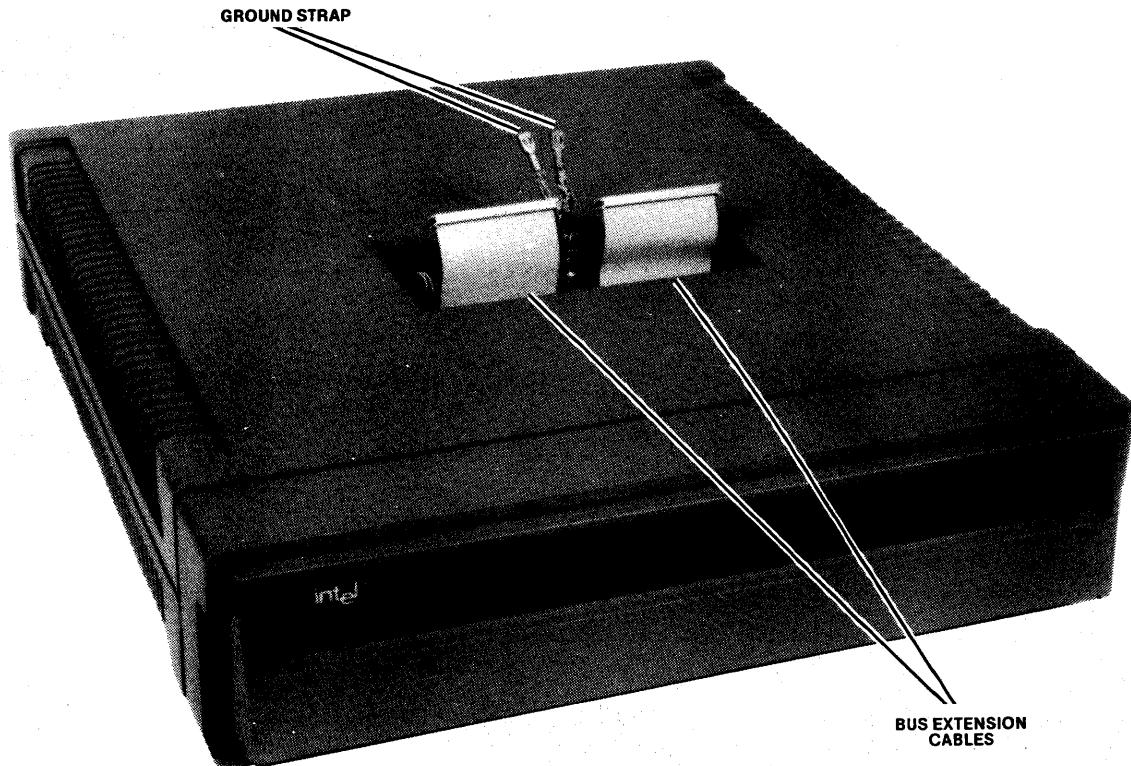


Figure 5-5. Expansion Chassis Cable Port Details

559-74A

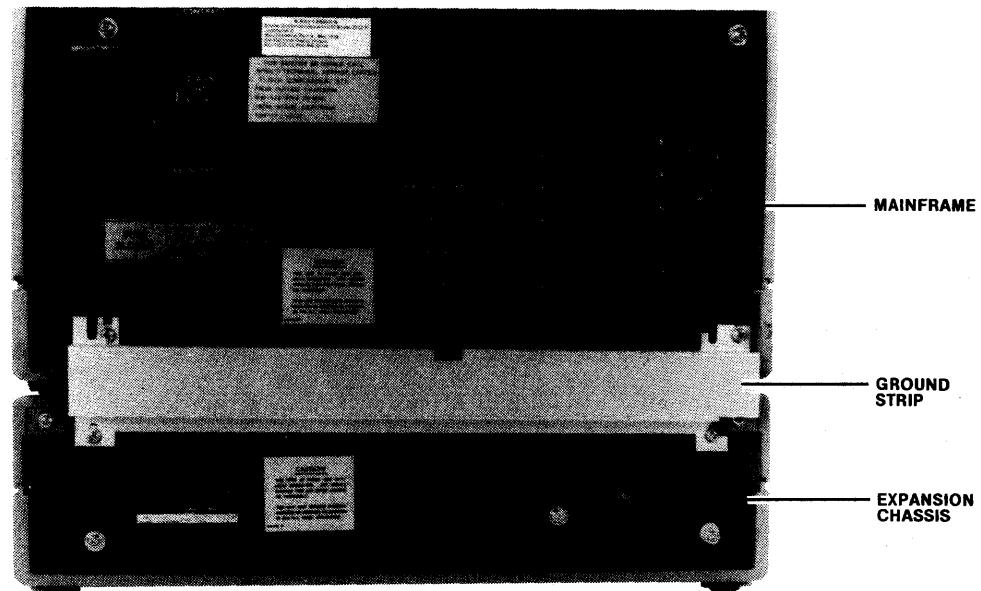


Figure 5-6. Expansion Chassis/Mainframe Ground Strip Installation

559-76A

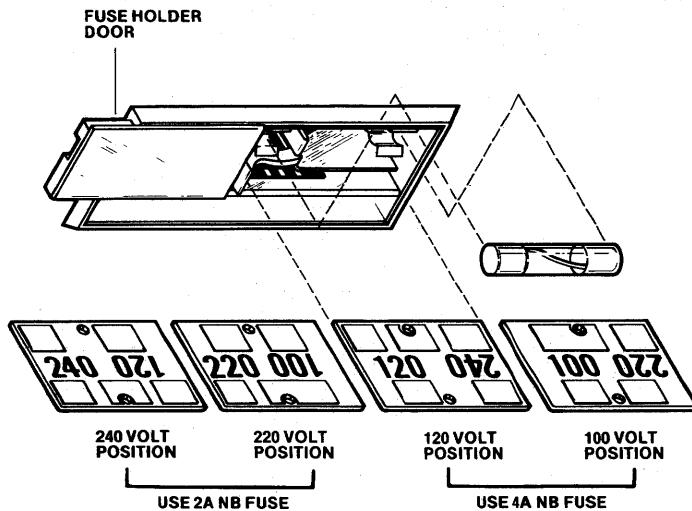


Figure 5-7. Expansion Chassis Voltage Switching Card and Fuse

121612-13

#### 5-4. OPERATIONAL SYSTEM UPGRADE

If the optional expansion chassis is being added to an operational system (i.e., after the initial system installation as described in paragraph 2-4), the system must be partially disassembled to allow the electrical and mechanical interconnection between the mainframe and expansion chassis. Proceed as follows:

- Turn off system power and disconnect mainframe and peripheral power cords.
- On mainframe rear panel, disconnect keyboard cable. Disconnect all other peripheral cables attached to connectors on rear panel.

##### NOTE

To obtain the maximum throughput rate, the optional dual double density diskette controller (DDDC) must have the highest bus priority in the system. This requires that the DDDC interface board and channel board be installed in the bottom two slots in the expansion chassis. Perform the remaining applicable steps of this procedure based on the following system configurations:

- DDDC presently installed in mainframe (perform *all* steps of procedure).

- DDDC not presently installed in mainframe but is being added at this time (omit steps c through h).
- DDDC is not presently installed in mainframe nor being added at this time (omit steps c through o).
  - Refer to figure 5-13 and remove ground strips between the mainframe and Drive 0, 1. Remove drive(s) from top of mainframe.
  - Remove mainframe front panel and disconnect hooded connector from double density diskette controller (DDDC) interface card. (See figure 2-5.)
  - Remove mainframe top cover. Refer to figure 5-8 and carefully disconnect connectors J14 through J18 from mating connectors on top edge of IOC assembly.
  - Remove the four rear panel retaining screws shown in figure 5-8. Gently pull rear panel away from mainframe chassis to access rear of connectors J8 and J9.
  - Disconnect controller cable connectors from J8 and J9. Remove controller cable from mainframe and reattach rear panel.
  - Reconnect cables to connectors J14 through J18 on IOC assembly. (Refer to figure 5-8.) Replace mainframe top cover.
  - Referring to figure 5-1, rotate the two expansion chassis front panel retaining screws counter-clockwise and remove front panel.

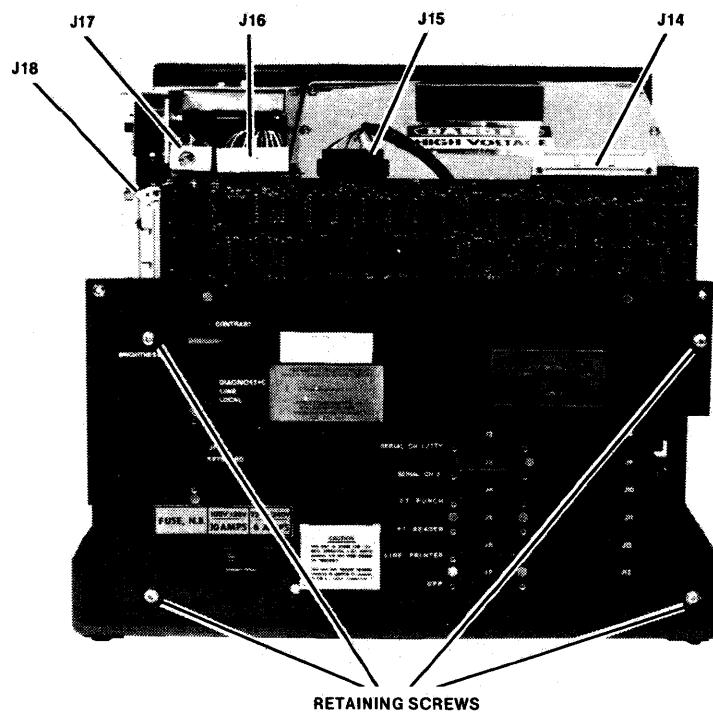


Figure 5-8. Mainframe Rear Panel

878-27A

- j. Loosen the six expansion chassis top cover retaining screws and remove top cover. (Refer to figures 5-1 and 5-2.)
  - k. Remove the four screws securing rear panel to expansion chassis. (See figure 5-2.) Pull edge of rear panel away from chassis to allow connector installation in top and bottom connector holes.
  - l. The controller cable has a hooded 100-pin connector on one end and two 37-pin connectors labeled "J8 DRIVE 0, 1" and "J9 DRIVE 2, 3" on opposite end. Using the hardware supplied, install connector labeled "J8 DRIVE 0, 1" in top hole on rear panel.
  - m. Install connector labeled "J9 DRIVE 2, 3" in bottom hole on rear panel.
  - n. Route cable along inside right-hand edge of expansion chassis (as viewed from rear). Make certain that there is ample cable slack to allow hooded connector to be attached at front of card cage.
  - o. Reinstall expansion chassis rear panel and top cover.
- CAUTION**
- p. Turn mainframe on its side as shown in figure 5-3. Remove cable port covers from mainframe and expansion chassis.
  - q. Refer to figure 5-4 and remove jumpers W1 and W2 from underneath connector J16 (accessible through mainframe cable port). Save port covers and jumpers in case expansion chassis is disconnected from mainframe in future.
  - r. Using supplied hardware, install ground strap on expansion chassis as shown in figure 5-5. Connect the two bus extension cables to connectors inside expansion chassis cable port.
  - s. Place mainframe on top of expansion chassis and tilt it backward.
  - t. Holding mainframe tilted backward, connect the other ends of the two bus extension cables to J14 and J16 inside mainframe cable port. Attach quick-disconnects on ground strap to the two ground lugs between J14 and J16.
  - u. Lower mainframe in place over expansion chassis. Attach aluminum ground strip between rear panels of mainframe and expansion chassis as shown in figure 5-6.

The mainframe weighs 86 pounds (39 kilograms). To prevent personal injury or equipment damage, have someone assist in performing steps p through u.

- v. On rear panel of expansion chassis, disconnect power cord (if connected) and slide fuse holder door on main power socket to left. (Refer to figure 5-7.) Remove voltage switching card and reinstall it in position corresponding to your available commercial power. Verify that proper fuse is installed: 4A normal-blow fuse for 100V or 120V; 2A normal-blow fuse for 220V or 240V. Close fuse holder door.
- w. Remove mainframe front panel and configure cardcages as shown in figure 2-6.
- x. Reinstall mainframe and expansion chassis front panels. Refer to figure 5-12 and attach power cords and peripheral cables to rear panel connectors.
- y. Turn on system power and execute CONFID and CON86 confidence tests.

## 5-5. DUAL DOUBLE DENSITY DISKETTE DRIVE(S)

This option consists of a dual channel diskette controller, controller cable, and one or two drives. To obtain this maximum throughput rate, the dual channel diskette controller (DDDC) must have the highest bus priority in the system. This requires that the DDDC, which consists of a channel board and an interface board, be installed in the bottom two system cardcage slots; i.e., the bottom two cardcage slots of the optional expansion chassis (if present), otherwise the bottom two cardcage slots of the mainframe. The installation procedures for installing the controller cable, controller, and dual drive(s) are given in following paragraphs.

## 5-6. CONTROLLER CABLE INSTALLATION

**5-7. EXPANSION CHASSIS.** The procedure for installing the controller cable in the optional expansion chassis is included as part of the expansion chassis installation procedure. Refer to paragraph 5-3 (Initial System Installation) or paragraph 5-4 (Operational System Upgrade) as appropriate.

**5-8. MAINFRAME.** Install the controller cable in the mainframe as follows:

- a. If system is operational, turn off system power and disconnect mainframe power cord.
- b. On front panel (figure 2-3), rotate the two retaining screws counterclockwise and remove front panel.
- c. Loosen top cover of mainframe by removing the two screws near front of cover and the two screws on rear of cover. (See figure 2-1.) Lift off top cover.
- d. Refer to figure 5-8 and carefully disconnect connectors J14 through J18 from mating connectors on top edge of IOC assembly. Remove the four rear panel retaining screws. Gently pull rear panel assembly away from mainframe to access rear of connectors J8 and J9.
- e. The controller cable has a hooded 100-pin connector on one end and two 37-pin connectors labeled "J8 DRIVE 0, 1" and "J9 DRIVE 2, 3" on opposite end. Using supplied hardware, install 37-pin connector labeled "J8 DRIVE 0, 1" in hole marked "J8" on rear panel.
- f. Install 37-pin connector labeled "J9 DRIVE 2, 3" in hole marked "J9" on rear panel.

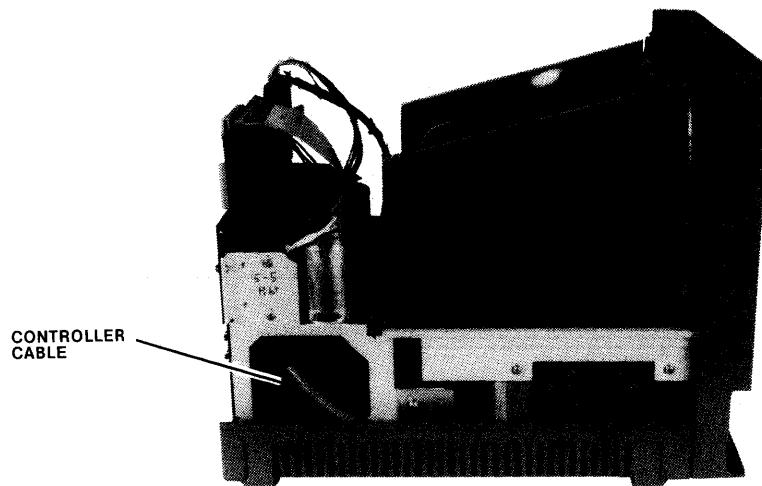


Figure 5-9. Double Density Diskette Controller (DDDC) Cable Routing

559-62A

- g. Route controller cable along side of chassis as shown in figure 5-9. Make certain there is ample cable slack to allow hooded connector to be attached to front edge of controller interface board when installed in cardcage.
- h. Reinstall and fasten rear panel assembly onto mainframe. Reinstall connectors J14 through J18 on appropriate mating connectors along top edge of IOC assembly.
- i. Reinstall top cover.

## 5-9. CONTROLLER INSTALLATION

As shown in figure 5-10, the dual channel diskette controller (DDDC) consists of a channel board, an interface board, and a dual auxiliary connector. Configure and install the DDDC boards as follows:

- a. On channel board, set address select switches to 78H as shown in figure 5-11.
- b. On interface board, set interrupt select switch to position 3.

### NOTE

Figure 5-10 shows the dual auxiliary connector installed such that the interface board will be mounted above the channel board when installed in the mainframe or optional expansion chassis cardcage. As shown in figures

2-5 and 2-6, the positions of these two boards can be reversed (channel board above the interface board) without affecting their operation.

- c. On interface board, verify that a hardware jumper exists between points D and C as shown in figure 5-10. If jumper exists between points D and E, remove it and reinstall as shown.
- d. Install dual auxiliary connector on channel board and interface board edge connectors as shown in figure 5-10. Make certain that connector is properly aligned with traces brought out to edge of boards.
- e. Install controller boards in bottom two slots of cardcage. (Refer to figure 2-5 or 2-6 as appropriate.) Press firmly inward on all four card extractors to seat both boards firmly into their mating connectors in cardcage.
- f. Install hooded connector of controller cable on interface board.

## 5-10. DUAL DRIVE INSTALLATION

Unpack dual drive(s), drive cable(s), and attaching hardware. Refer to figure 5-12 or 5-13, as appropriate, and proceed as follows:

- a. Place first dual drive (Drive 0, 1) squarely on top of mainframe.

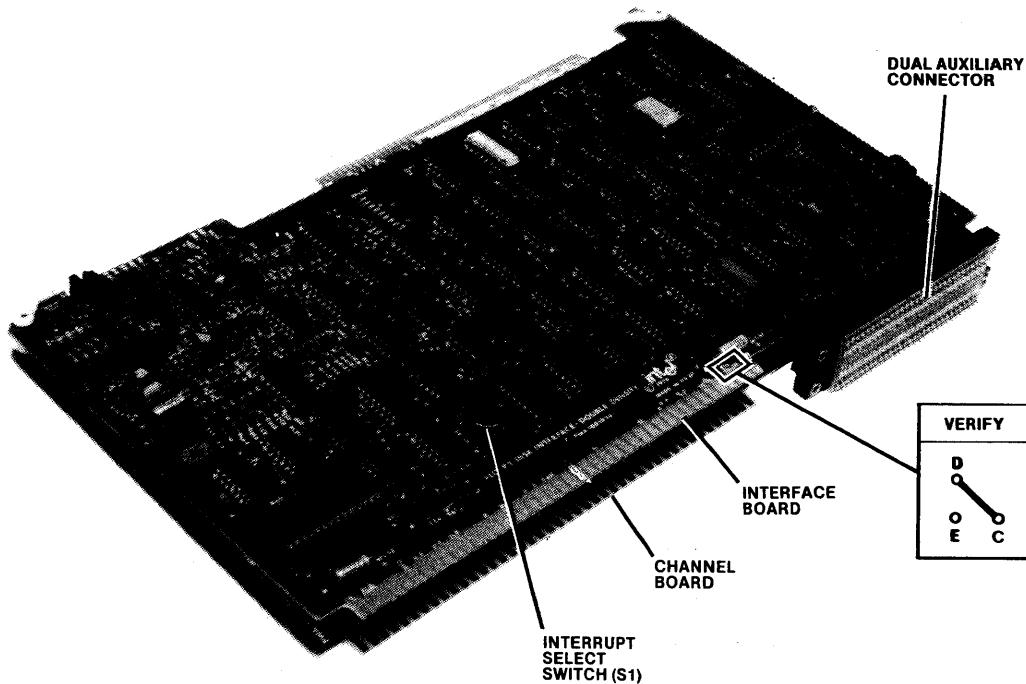


Figure 5-10. Double Density Diskette Controller

559-57B

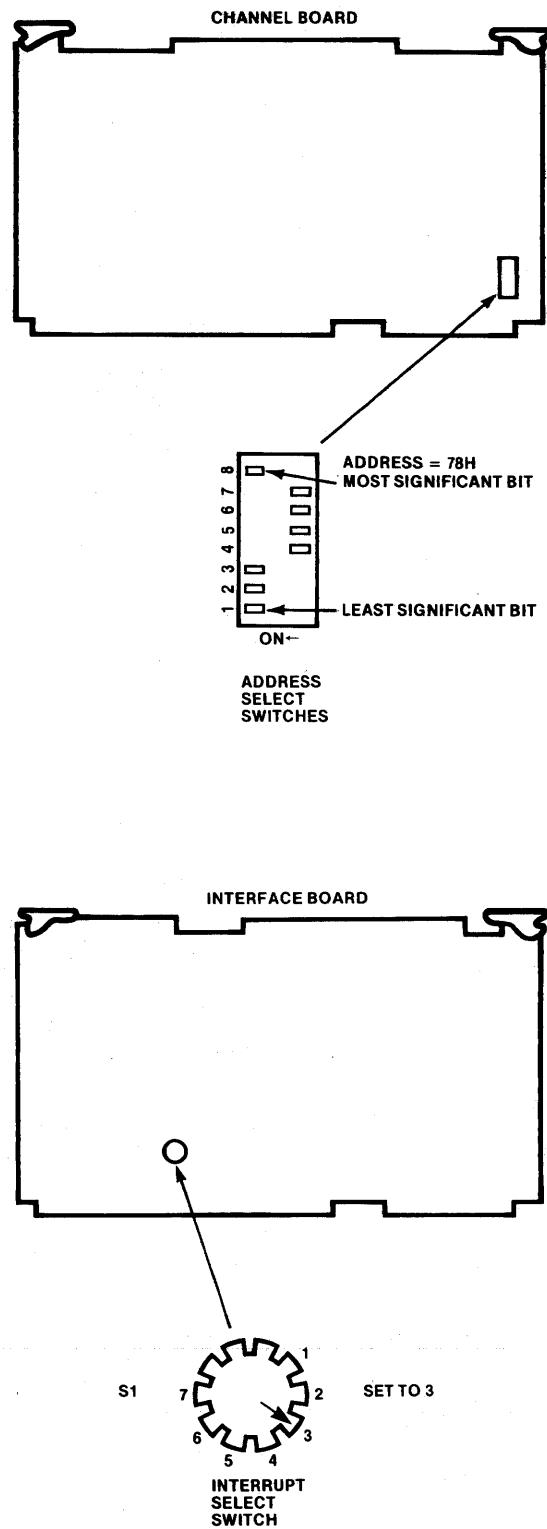


Figure 5-11. Channel Board and Interface Board Switch Settings

1505-3-1A

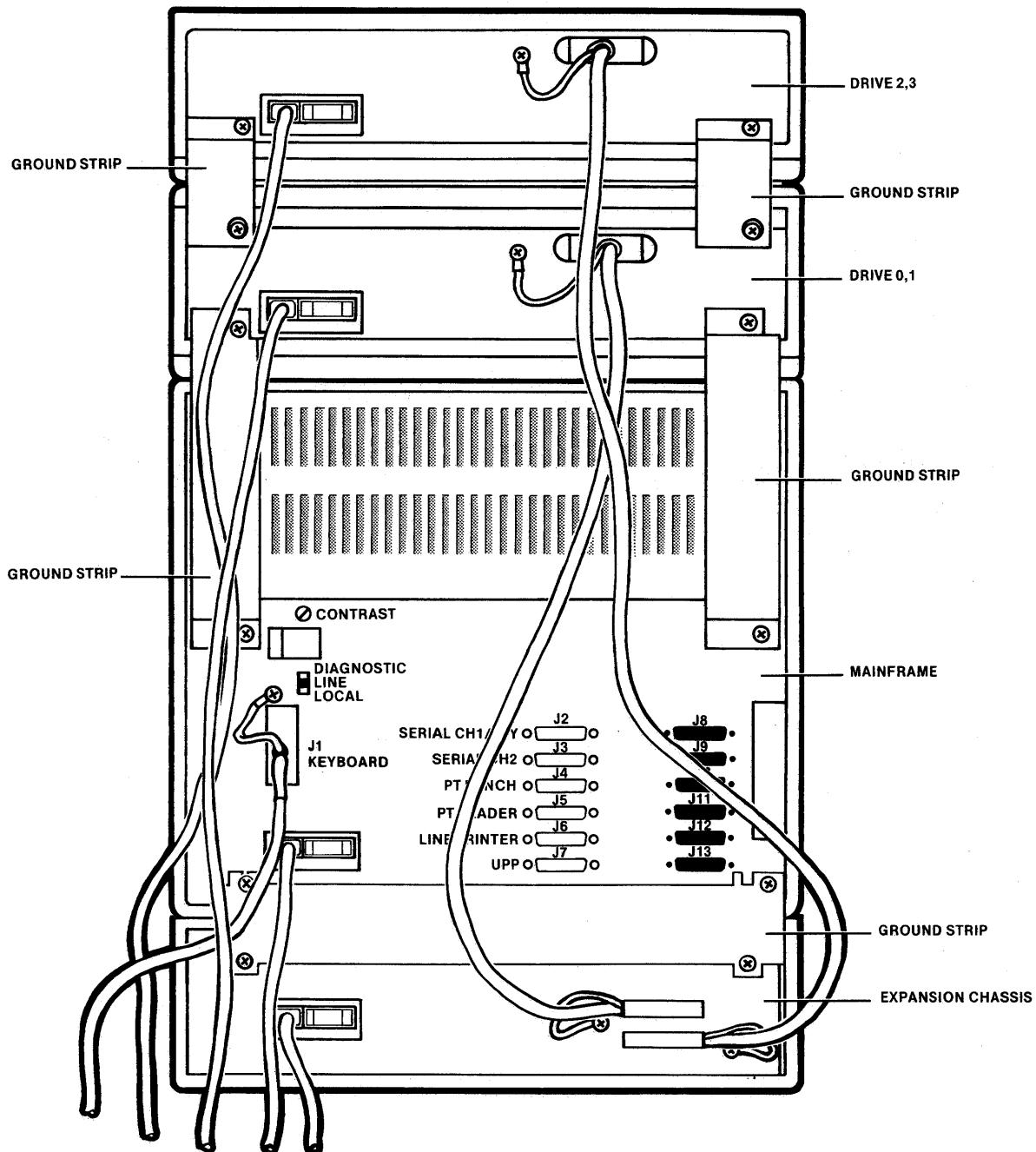


Figure 5-12. Diskette Drive/Expansion Chassis Cabling Details

121612-14

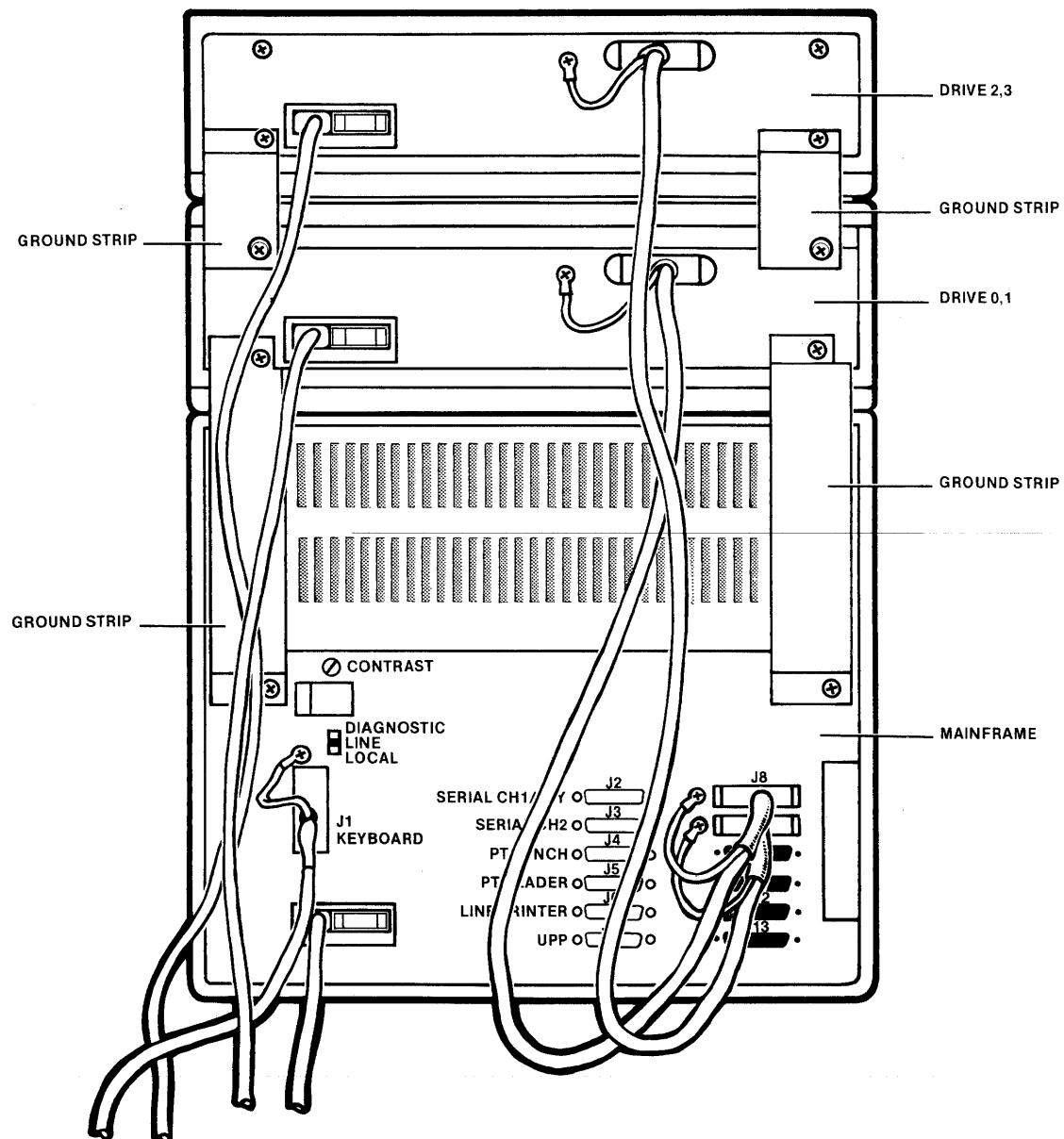


Figure 5-13. Diskette Drive/Mainframe Cabling Details

121612-15

- b. Install the two long aluminum ground strips between rear panels of dual drive and mainframe.
- c. Attach drive cable to connector on rear panel of dual drive chassis; connect ground wire lead to adjacent screw.
- d. Attach other end of drive cable to top connector on rear panel of expansion chassis (if installed) or to connector J8 on rear panel of mainframe. Connect ground wire lead to adjacent screw.

**NOTE**

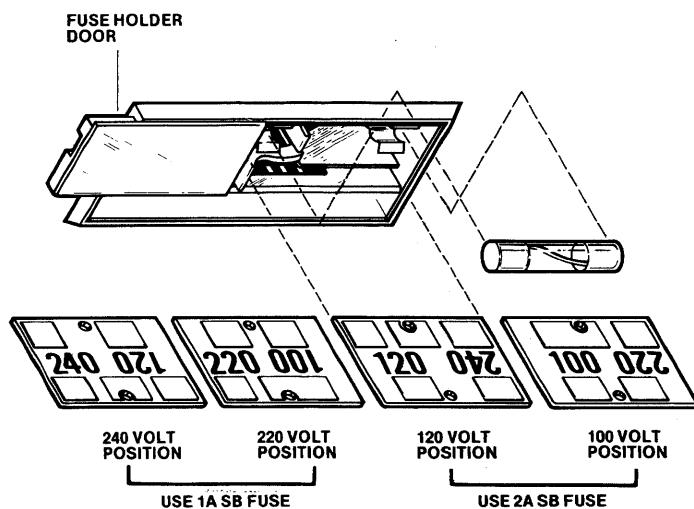
The internal power supply for the double density diskette drive is configured at the factory for 110V or 220V ac. This power supply *cannot be reconfigured in the field* (i.e., 110V to 220V or vice versa).

- e. Check voltage stickers on disk drive; voltage must match your available commercial power. On rear panel of dual drive, disconnect power cord (if connected) and slide fuse holder door on main power socket to left. (Refer to figure 5-14.) Remove voltage switching card and reinstall it in position corresponding to your available commercial power. Verify that proper fuse is installed: 2A slow-blow fuse for 110V or 120V; 1A slow-blow fuse for 220V or 240V. Close fuse holder door and install power cord.
- f. This completes the installation of Drive 0, 1. The integral single density drive is redesignated Drive 4 by default.

**NOTE**

If you are installing a second dual drive (Drive 2, 3), proceed with step h of this procedure.

- g. Install mainframe power cord. If installation of drive is part of initial system installation, verify system performance by running Firmware Diagnostic Tests (Chapter 2), CONFID Confidence Test (Chapter 3), and CON86 Confidence Test (Chapter 4). If installation of drive is an add-on to an operational system, execute IOC firmware diagnostic (Chapter 2) and Test A of CONFID test (Chapter 3).
- h. Place second dual drive (Drive 2, 3) squarely on top of first dual drive. (Refer to figure 5-12 or 5-13, as appropriate.)
- i. Install the two short aluminum ground strips between rear panels of the two drives.
- j. Attach drive cable to connector on rear panel of second dual drive; connect ground wire lead to adjacent screw.
- k. Attach other end of drive cable to bottom connector on rear panel of expansion chassis (if installed) or to connector J9 on rear panel of mainframe. Connect ground wire to adjacent screw.
- l. Perform step e for second drive.
- m. This completes the installation of Drive 2, 3. Install mainframe power cord and perform checkout as directed in step g.



**Figure 5-14. Diskette Drive Voltage Switching Card and Fuse**

121612-16

## 5-11. MEMORY UPGRADE

As shown in figure 1-2, the standard Intellec Series III system includes one iSBC 064 64k RAM Board occupying page 1 (absolute addresses 10000H through 1FFFFH) in offboard memory. Additional read/write (RAM) memory can be installed in 32k or 64k increments using iSBC 032 or iSBC 064 RAM boards are described in paragraphs 5-12 and 5-13.

## 5-12. iSBC 032™ RAM BOARD

The iSBC 032 RAM Board, which includes 32k of dynamic read/write memory, can be configured to

occupy either the lower 32k or upper 32k in any of the 16 pages of the 8086 microprocessor address space. For example, to configure the board in the 192-224k address range (the lower 32k of page 3), proceed as follows:

- Referring to figure 5-15 and table 5-1, configure the following six plug-on jumpers:

E1 to E9	}	(Lower 32k)
E4 to E16		
E5 to E24	}	(Page 3)
E7 to E17		
E8 to E18	}	
E29 to E30		(Delayed write mode)

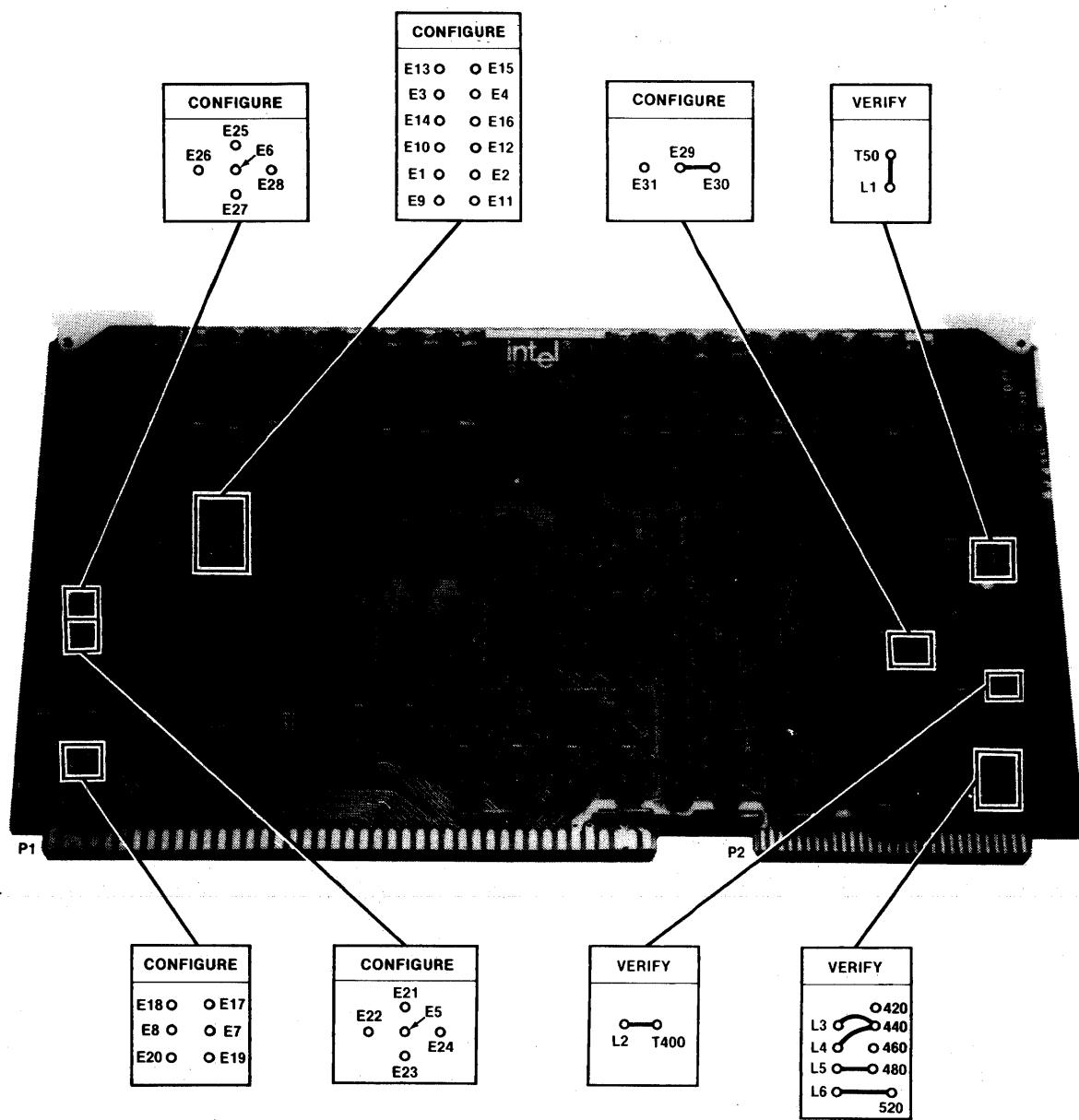


Figure 5-15. iSBC 032™ 32k RAM Board Configuration Jumpers

121612-17

Table 5-1. iSBC 032™ 32k RAM Board Address Allocation Jumpers

Page	Address Range	Lower 32k		Upper 32k		Page Select Jumpers		
		0-16k	16-32k	32-48k	48-64k			
0*	0-64k	E1-E9	E4-E16	E1-E10	E4-E15	E5-E21	E7-E17	E8-E18
1**	64-128k					E5-E22		
2	128-192k					E5-E23		
3	192-256k					E5-E24		
4	256-320k					E6-E25		
5	320-384k					E6-E26		
6	384-448k					E6-E27		
7	448-512k					E6-E28	E7-E17	E8-E18
8	512-576k					E5-E21	E7-E19	E8-E20
9	576-640k					E5-E22		
A	640-704k					E5-E23		
B	704-768k					E5-E24		
C	768-832k					E6-E25		
D	832-896k					E6-E26		
E	896-960k					E6-E27		
F***	960-1024k	E1-E9	E4-E16	E1-E10	E4-E15	E6-E28	E7-E19	E8-E20

\*Occupied by RPB-86 on-board RAM.  
 \*\*Occupied by standard 64k RAM board.  
 \*\*\*Top 16k (FC000-FFFFF) shadowed by RPB-86 on-board PROM.

- b. Verify the following six wirewrap and hardwired timing jumpers:
  - L1 to T50 } (Acknowledge timing)
  - L2 to T400 } (Refresh timing)
  - L3 to T440 }
  - L4 to T440 }
  - L5 to T480 }
  - L6 to T520 } (Write command timing)
- c. Turn off system power and remove mainframe or expansion chassis front panel. Install RAM board in any vacant cardcage slot.
- d. Replace front panel and turn on system power. Boot system test diskette, enter disk-based CON86, and execute Test 2 (Offboard Memory March).
- a. Referring to figure 5-16 and table 5-2, verify the following four plug-on jumpers:
  - E1 to E9 } (Bank/block select)
  - E2 to E12 }
  - E3 to E14 }
  - E4 to E15 }
- b. Configure the following four plug-on jumpers:
  - E5 to E23 } (Page 2)
  - E7 to E17 }
  - E8 to E18 }
  - E29 to E30 } (Delayed write mode)
- c. Verify the following six wirewrap and hardware timing jumpers:
  - L1 to T50 } (Acknowledge timing)
  - L2 to T400 }
  - L3 to T440 }
  - L4 to T440 } (Refresh timing)
  - L5 to T480 }
  - L6 to T520 } (Write command timing)
- d. Turn off system power and remove mainframe or expansion chassis front panel. Install RAM board in any vacant cardcage slot.
- e. Replace front panel and turn on system power. Boot system test diskette, enter CON86, and execute Test 2 (Offboard Memory March).

### 5-13. iSBC 064™ RAM BOARD

The iSBC 064 RAM Board includes 64k of dynamic read/write memory and can be configured to occupy any one of the 16 pages of the 8086 microprocessor address space. For example, to configure the board in the 128-192k address range (page 2), proceed as follows;

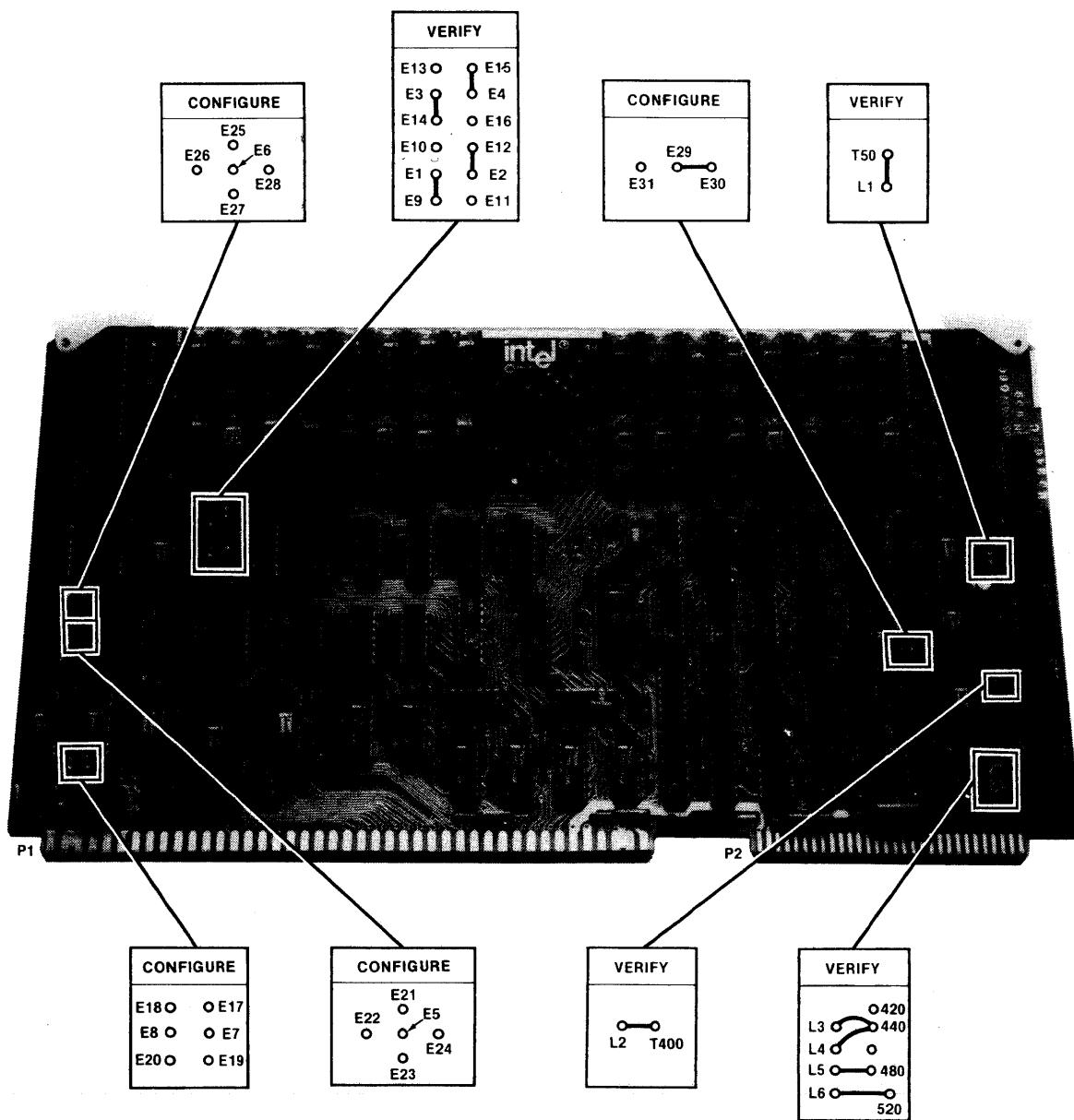


Figure 5-16. iSBC 064™ 64k RAM Board Configuration Jumpers

121612-18

**Table 5-2. iSBC 064™ 64k RAM Board Address Allocation Jumpers**

Page	Range	Bank/Block Select Jumpers				Page Select Jumpers		
0*	0-64k	E1-E9	E2-E12	E3-E14	E4-E15	E5-E21	E7-E17	E8-E18
1**	64-128k	↑	↑	↑	↑	E5-E22		
2	128-192k					E5-E23		
3	192-256k					E5-E24		
4	256-320k					E6-E25		
5	320-384k					E6-E26		
6	384-448k					E6-E27		
7	448-512k					E6-E28	E7-E17	E8-E18
8	512-576k					E5-E21	E7-E19	E8-E20
9	576-640k					E5-E22		
A	640-704k					E5-E23		
B	704-768k					E5-E24		
C	768-832k					E6-E25		
D	832-896k					E6-E26		
E	896-960k					E6-E27		
F***	960-1024k	E1-E9	E2-E12	E3-E14	E4-E15	E6-E28	E7-E19	E8-E20

\*Occupied by RPB-86 on-board RAM.  
\*\*Occupied by standard 64k RAM board.  
\*\*\*Top 16k (FC000-FFFFF) shadowed by RPB-86 on-board PROM.

## 5-14. ADDING IN-CIRCUIT EMULATORS

Any of the currently available Intel Corporation in-circuit emulators may be used with the Series III systems. Emulator boards may be installed in any vacant cardcage slots, as long as the slots are contiguous to one another. Complete installation instructions are provided in the appropriate *ICE™ In-Circuit Emulator Operating Instructions for ISIS-II Users* manual. Ensure that the mainframe power supply has ample reserve capacity to support the selected emulator. (Refer to tables 1-2, 1-3, and 1-4.)

## 5-15. ADDING PERIPHERALS

The mainframe rear panel includes connectors for the following peripheral devices:

J2: Serial Channel 1/Teletypewriter

J3: Serial Channel 2

J4: High-Speed Paper Tape Punch

J5: High-Speed Paper Tape Reader

J6: Line Printer

J7: Universal PROM Programmer (UPP)

Tables 5-3 through 5-8 list the pin numbers, signal mnemonics, and functions for each of the peripheral connectors. Serial Channel 1 and Serial Channel 2 include extensive line jumpering to allow interfacing to a variety of RS232C devices; this capability is discussed and illustrated in Appendix A.

**Table 5-3. SERIAL CH 1/TTY Connector J2 Pin Assignments**

Pin	Signal	Function	Current Drive		Current Load	
			Low ( $I_{OL}$ )	High ( $I_{OH}$ )	Low ( $I_{IL}$ )	High ( $I_{IH}$ )
1	PROT GND	Protective Ground				
2	RxD (RS232)	Transmitted Data In				
3	TxD (RS232)	Received Data Out				
4	RTS (RS232)	Request to Send				
5	CTS (RS232)	Clear to Send				
6	DSR (RS232)	Data Set Ready				
7	GND	Signal Ground				
8		Not Used				
9		Not Used				
10		Not Used				
11		Not Used				
12	RxD (CURRENT LOOP)	Transmitted Data In				
13	TxD (CURRENT LOOP)	Received Data Out				
14	TTY RDY	Same as DSR (pin 6)				
15	TxC	Transmit Clock				
16	DTR (CURRENT LOOP)	Data Terminal Ready (Reader Control)				
17	RxC	Receive Clock				
18		Not Used				
19		Not Used				
20	DTR (RS232)	Data Terminal Ready				
21	DTR RET	Reader Control Return (to -12V)				
22		Not Used				
23		Not Used				
24	RxD RET (CURRENT LOOP)	RxD Return (to + 12V)				
25	TxD RET (CURRENT LOOP)	TxD Return (to -12V)				

Note: The required mating connector is a Cannon DEC-25P (or equivalent).  
 \*At 12.0 volts

**Table 5-4. SERIAL CH 2 Connector J3 Pin Assignments**

Pin	Signal	Function	Current Drive		Current Load	
			Low ( $I_{OL}$ )	High ( $I_{OH}$ )	Low ( $I_{IL}$ )	High ( $I_{IH}$ )
1	PROT GND	Protective Ground				
2	TxD	Transmitted Data Out	6mA	-6mA		
3	RxD	Received Data In			-1.7mA	1.7mA
4	RTS	Request to Send	6mA	-6mA	-1.7mA	1.7mA
5	CTS	Clear to Send			-1.7mA	1.7mA
6	DSR	Data Set Ready			-1.7mA	1.7mA
7	GND	Signal Ground				
8		Unassigned				
9		Not Used				
10		Not Used				
11	+12V	+12V (requires jumper connection)				
12		Not Used				
13		Not Used				
14		Not Used				
15	TxC	Transmit Clock			-1.7mA	1.7mA
16		Not Used				
17	RxC	Receive Clock			-1.7mA	1.7mA
18		Not Used				
19		Not Used				
20	DTR	Data Terminal Ready	6mA	-6mA		
21		Not Used				
22		Not Used				
23	-12V	-12V (requires jumper connection)				
24	EXT TxC	External Transmit Clock	6mA	-6mA		
25	+5V	+5V (requires jumper connection)				

Note: The required mating connector is a Cannon DEC-25P (or equivalent).

**Table 5-5. PT PUNCH Connector J4 Pin Assignments**

Pin	Signal	Function	Current Drive		Current Load		Termination
			Low ( $I_{OL}$ )	High ( $I_{OH}$ )	Low ( $I_{IL}$ )	High ( $I_{IH}$ )	
1	DATA TRACK 1/	Output Data Bit 1	15mA	-1mA			
2	DATA TRACK 2/	Output Data Bit 2	15mA	-1mA			
3	DATA TRACK 3/	Output Data Bit 3	15mA	-1mA			
4	DATA TRACK 4/	Output Data Bit 4	15mA	-1mA			
5	DATA TRACK 5/	Output Data Bit 5	15mA	-1mA			
6	DATA TRACK 6/	Output Data Bit 6	15mA	-1mA			
7	DATA TRACK 7/	Output Data Bit 7	15mA	-1mA			
8	DATA TRACK 8/	Output Data Bit 8	15mA	-1mA			
9		Not Used					
10	DIRECTION	Direction Control					
11	PUNC COMMAND/	Punch Command	16mA	-800µA			1kΩ pullup
12	PUNCH READY/	Punch Ready					
13	SYSTEM READY/	System Ready					
14	INPUT MODE SELECT	Select Input Mode					
15	OUTPUT MODE SELECT	Select Output Mode					
16	CHASSIS GND	Chassis Ground					
17	CHASSIS GND	Chassis Ground					
18	GND	Ground					
19		Not Used					
20		Not Used					
21		Not Used					
22		Not Used					
23	GND	Ground					
24		Not Used					
25	GND	Ground					

Note: \*Slash (/) after signal mnemonic denotes that signal is true when  $\leq 0.4V$ .

The required mating connector is a Cannon DEC-25P (or equivalent).

**Table 5-6. PT READER Connector J5 Pin Assignments**

Pin	Signal	Function	Current Drive		Current Load		Termination
			Low ( $I_{OL}$ )	High ( $I_{OH}$ )	Low ( $I_{IL}$ )	High ( $I_{IH}$ )	
1	DATA TRACK 1/	Input Data Bit 1			-0.25mA	40µA	
2	DATA TRACK 2/	Input Data Bit 2			-0.25mA	40µA	
3	DATA TRACK 3/	Input Data Bit 3			-0.25mA	40µA	
4	DATA TRACK 4/	Input Data Bit 4			-0.25mA	40µA	
5	DATA TRACK 5/	Input Data Bit 5			-0.25mA	40µA	
6	DATA TRACK 6/	Input Data Bit 6			-0.25mA	40µA	
7	DATA TRACK 7/	Input Data Bit 7			-0.25mA	40µA	
8	DATA TRACK 8/	Input Data Bit 8			-0.25mA	40µA	
9	DATA READY/	Data Ready			-0.25mA	40µA	
10		Not Used					
11	GND	Ground					
12	GND	Ground					
13	GND	Ground					
14	SYSTEM READY/	System Ready					
15		Not Used					
16	DR/	Paper Tape Drive Right	16mA	-800µA			
17	DL/	Paper Tape Drive Left	16mA	-800µA			
18		Not Used					
19		Not Used					
20		Not Used					
21		Not Used					
22		Not Used					
23		Not Used					
24	GND	Ground					
25	CHASSIS GND	Chassis Ground					

Note: \*Slash (/) after signal mnemonic denotes that signal is true when  $\leq 0.4V$ .

The required mating connector is a Cannon DEC-25P (or equivalent).

**Table 5-7. LINE PRINTER Connector J6 Pin Assignments**

Pin	Signal	Function	Current Drive		Current Load		Termination
			Low ( $I_{OL}$ )	High ( $I_{OH}$ )	Low ( $I_{IL}$ )	High ( $I_{IH}$ )	
1	DATA 1	Output Data Bit 1	15mA	-1mA			
2	DATA 2	Output Data Bit 2	15mA	-1mA			
3	DATA 3	Output Data Bit 3	15mA	-1mA			
4	DATA 4	Output Data Bit 4	15mA	-1mA			
5	DATA 5	Output Data Bit 5	15mA	-1mA			
6	DATA 6	Output Data Bit 6	15mA	-1mA			
7	DATA 7	Output Data Bit 7	15mA	-1mA			
8	DATA 8	Output Data Bit 8	15mA	-1mA			
9	GND	Ground					
10	GND	Ground					
11	GND	Ground					
12	GND	Ground					
13		Not Used					
14	LPT DATA STROBE/	Data Strobe					
15	GND	Ground	16mA	-800μA			
16	ACKNOWLEDGE /	Data Acknowledge					
17	BUSY/	Printer Busy			-0.25mA	40μA	470Ω pullup
18		Not Used			-0.25mA	40μA	470Ω pullup
19	LPT CTL 1/	Control Line 1	16mA	-800μA			
20	LPT CTL 2/	Control Line 2	16mA	-800μA			
21		Not Used					
22	SELECT/	Printer Select					
23		Not Used					
24		Not Used					
25	CHASSIS GND	Chassis Ground					

Note: \*Slash (/) after signal mnemonic denotes that signal is true when  $\leq 0.4V$ .  
The required mating connector is a Cannon DEC-25P (or equivalent).

Table 5-8. UPP Connector J7 Pin Assignments

Pin	Signal	Function	Current Drive		Current Load		Termination
			Low ( $I_{OL}$ )	High ( $I_{OH}$ )	Low ( $I_{IL}$ )	High ( $I_{IH}$ )	
1	GND	Ground					
2	PPACK/	PROM Programmer Acknowledge					
3	PPRC1/	PROM Programmer Read Control Line 1					
4	PPRC0/	PROM Programmer Read Control Line 2					
5	PRD7/	PROM Read Data Bit 7					
6	PRD6/	PROM Read Data Bit 6					
7	PRD5/	PROM Read Data Bit 5					
8	PRD4/	PROM Read Data Bit 4					
9	PRD3/	PROM Read Data Bit 3					
10	PRD2/	PROM Read Data Bit 2					
11	PRD1/	PROM Read Data Bit 1					
12	PRD0/	PROM Read Data Bit 0					
13	GND	Ground					
14	INIT/	Initialize					
15	PWD7/	PROM Write Data Bit 7	16mA	-800µA	-0.5mA	80µA	470Ω pullup
16	PWD6/	PROM Write Data Bit 6	16mA	-800µA	-0.25mA	40µA	
17	PWD5/	PROM Write Data Bit 5	16mA	-800µA	-0.25mA	40µA	
18	PWD4/	PROM Write Data Bit 4	16mA	-800µA	-0.25mA	40µA	
19	PWD3/	PROM Write Data Bit 3	16mA	-800µA	-0.25mA	40µA	
20	PWD2/	PROM Write Data Bit 2	16mA	-800µA	-0.25mA	40µA	
21	PWD1/	PROM Write Data Bit 1	16mA	-800µA	-0.25mA	40µA	
22	PWD0/	PROM Write Data Bit 0	16mA	-800µA	-0.25mA	40µA	
23	PPWC2/	PROM Programmer Write Control Line 2	16mA	-800µA	-0.25mA	40µA	
24	PPWC1/	PROM Programmer Write Control Line 1	16mA	-800µA	-0.25mA	40µA	
25	PPWC0/	PROM Programmer Write Control Line 0	16mA	-800µA	-0.25mA	40µA	

Note: \*Slash (/) after signal mnemonic denotes that signal is true when  $\leq 0.4V$

The required mating connector is a Cannon DEC-25P (or equivalent).



## CHAPTER 6 SERVICE INFORMATION

### 6-1. INTRODUCTION

This chapter provides basic troubleshooting procedures and instructions on how to obtain service and repair assistance.

### 6-2. BASIC TROUBLESHOOTING

When the mainframe powers up, it supplies +12V to energize relay K1 inside the expansion chassis. The contacts of K1, in turn, connect ac power to the expansion chassis power supply and fans. If neither the mainframe nor expansion chassis will power up, check ac power input to the mainframe as follows:

- a. Verify that facility power is available at main power outlet.
- b. Ensure that power cord is seated firmly in mainframe power receptacle and main power outlet.
- c. Disconnect mainframe power cord, open fuseholder door, and check fuse. (See figure 2-11.)

If the mainframe powers up, but the expansion chassis fans are not operating, check the ac power input to the expansion chassis as follows:

- a. Verify that facility power is available at main power outlet.
- b. Ensure that power cord is seated firmly in expansion chassis power receptacle and power outlet.
- c. Disconnect expansion chassis power cord, open fuseholder door, and check fuse. (See figure 5-7.)
- d. Verify that bus extension cable connectors are properly seated onto mating receptacles inside mainframe and expansion chassis. (Refer to figure 5-5.)

If the mainframe and expansion chassis power up, but the system is failing otherwise, isolate the problem as follows:

1. Run IPC-85 and IOC firmware diagnostics as described in Chapter 2.
2. Run CONFID and CON86 confidence tests as described in Chapters 3 and 4, respectively.

If any of these tests fails to execute properly, check the integrity of all connectors and socket-mounted IC's as described in paragraph 2-4 (Installation Procedure). Also make certain that all boards in the cardcage are fully seated into the backplane connectors.

Try again to run the failing diagnostic. If the diagnostic still doesn't execute properly, refer to the "Probable Fault" column in one of the following tables:

Failing Diagnostic	Probable Fault Table
IPC-85 Firmware Diagnostic	2-1
IOC Firmware Diagnostic	2-2
CONFID Confidence Test	3-4
CON86 Confidence Test	4-3

### 6-3. PREVENTIVE MAINTENANCE

Preventive maintenance instructions for the integral diskette drive and optional dual double density diskette drive are provided in Appendix E.

### 6-4. SERVICE AND REPAIR ASSISTANCE

The best service for your Intel product will be provided by an Intel Customer Engineer. These trained professionals will provide prompt, efficient on-site installation, preventive maintenance, or corrective maintenance services that will keep your equipment in the best possible operating condition.

Your Intel Customer Engineer can provide the service you need through a prepaid service contract or on an hourly charge basis. For further information, contact your local Intel office.

When it is impossible for you to use the services of an Intel Customer Engineer or when Intel service is not available in your local area, you may contact the Intel Service Center directly at one of the following numbers:

#### Telephone:

From Alaska, Arizona, or Hawaii call—  
(602) 869-4600

From all other U.S. locations call toll free—  
(800) 528-0595

TWX: 910-951-1330

Never return equipment to Intel for service or repair before you contact an Intel Customer Engineer or the Intel Service Center.

If return of your equipment is necessary, you will be given a Repair Authorization Number, shipping instructions, and other important information that will help Intel provide you with fast, efficient service. If the product is being returned because of damage sustained during shipment, or if the product is out of warranty, a purchase order is necessary in order for the Intel Service Center to make the repair.

When preparing the product for shipment to the Service Center, use the original factory packaging material if available. If the original packaging is not

available, wrap the product in a cushioning material such as Air Cap SD-240, manufactured by the Sealed Air Corporation, Hawthorne, N.J. (or equivalent) and enclose in a heavy-duty corrugated shipping carton. Seal the carton securely, mark it "FRAGILE" to ensure careful handling, and ship it to the address specified by the Intel Service Center.

#### **NOTE**

Customers outside of the United States should contact their sales source (Intel Sales Office or Authorized Intel Distributor) for directions on obtaining service or repair assistance.

## APPENDIX A CONFIGURING THE SERIAL INTERFACES

The problems that sometimes occur when connecting devices from different manufacturers through an RS232C interface are usually due to different interpretations of the RS232C specification.

The Intellec Series III serial interface channels (SERIAL CH 1/SERIAL CH 2) are designed to be adaptable to any interpretation of the specification. The serial interfaces are implemented with extensive line jumpering capability.

As shipped, SERIAL CH 1 is jumpered for a standard current-loop TTY terminal configuration.

SERIAL CH 2 is jumpered for modem or CRT terminal.

The jumpers are located at the top right corner of the IOC board and are accessible by removing the chassis top cover. Figure A-1 shows the lines and jumpers available for SERIAL CH 1, with the jumpers shown as shipped. Figure A-2 shows the lines and jumpers available for SERIAL CH 2, with the jumpers shown as shipped.

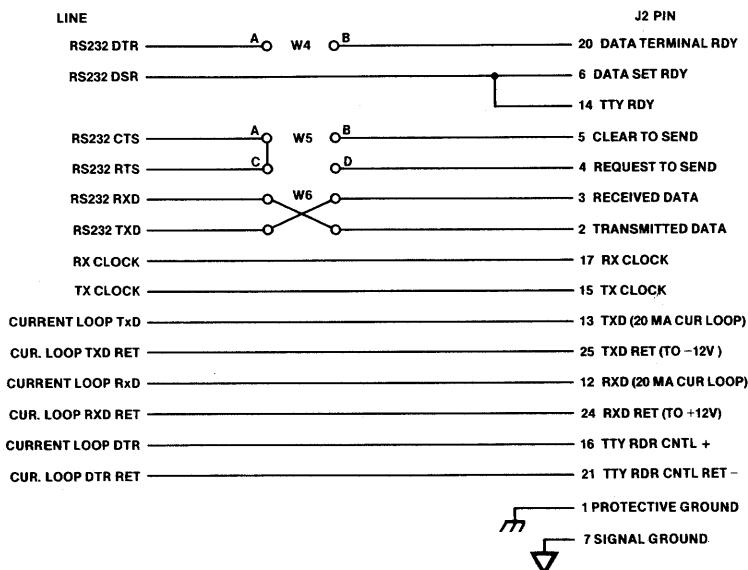


Figure A-1. SERIAL CH 1 Lines and Jumpers

559-10B

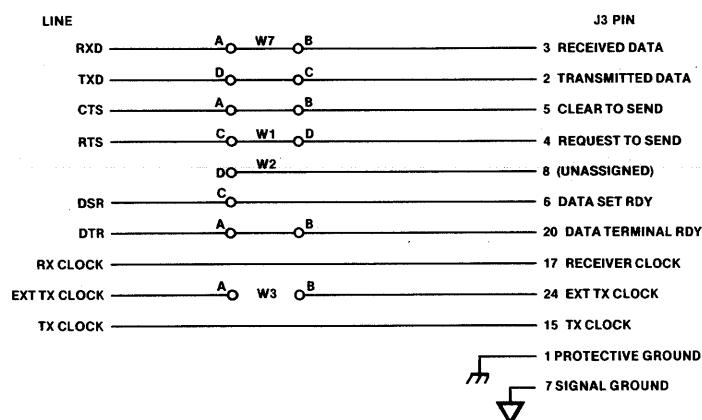


Figure A-2. SERIAL CH 2 Lines and Jumpers

559-11A



## APPENDIX B MODIFYING THE BAUD RATE

```
; THIS PROGRAM MODIFIES THE BAUD RATES FOR THE SERIES-III
; SERIAL CHANNELS. SPECIFICALLY, AS IT IS WRITTEN, SERIAL
; CHANNEL 2 BAUD RATE WOULD BE MODIFIED. TO CHANGE THE
; BAUD RATE FOR SERIAL CHANNEL 1 (TTY), CHANGE THE THREE
; OCCURRENCES OF "OUT 0F7H" TO "OUT 0F5H", THE TWO
; OCCURRENCES OF "OUT 0F1H" TO "OUT 0F0H", THE ONE
; OCCURRENCE OF "MVI A, 076H" TO "MVI A, 036H", AND REASSEMBLE.
;
;
; BE SURE TO SUBSTITUTE THE PROPER BAUD CODE AND MULTIPLIER
; INTO THE ASSEMBLY LANGUAGE CODE PRIOR TO ASSEMBLING+
;
;
CSEG
START: MVI      A,040H          ; RESET THE 8251 USART
       OUT     0F7H
       MVI      A,076H          ; PROGRAM THE 8253 COUNTER FOR
       OUT     0F3H          ; MODE 3 AND LSB FOLLOWED BY MSB
;
;
; BAUD RATE CODES
;
; RATE      CODE      MULTIPLIER
; 110       2BAH      0CEH
; 150       080H      0CFH
; 300       040H      0CFH
; 600       020H      0CFH
; 1200      010H      0CFH
; 2400      020H      0CEH
; 4800      010H      0CEH
; 9600      008H      0CEH
; 19200     004H      0CEH
;
LXI      H, BAUD CODE    ; LOAD 8253 WITH LSB OF BAUD
MOV      A,L            ; CODE FIRST, FOLLOWED BY
OUT     0F1H            ; MSB OF BAUD CODE
MOV      A,H
OUT     0F1H
;
; OBTAIN PROPER MULTIPLIER FROM BAUD RATE CODE TABLE ABOVE
;
MVI      A, MULTIPLIER  ; LOAD MULTIPLIER
OUT     0F7H
MVI      A,025H          ; ENABLE TRANSMITTER, RECEIVER AND RTS
OUT     0F7H
RST      01H
END      START
```



## APPENDIX C

# TELETYPEWRITER MODIFICATIONS

### INTRODUCTION

This appendix provides information required to modify a Model ASR-33 Teletypewriter for use with the Intellec Series III system.

### INTERNAL MODIFICATIONS

#### WARNING

Hazardous voltages are exposed when the top cover of the teletypewriter is removed. To prevent accidental shock, disconnect the teleprinter power cord before proceeding beyond this point.

Remove the top cover and modify the teletypewriter as follows:

1. Remove blue lead from 750-ohm tap on current source register; reconnect this lead to 1450-ohm tap. (Refer to figures C-1 and C-2.)
2. On terminal block, change two wires as follows to create an internal full-duplex loop (refer to figures C-1 and C-3):
  - a. Remove brown/yellow lead from terminal 3; reconnect this lead to terminal 5.
  - b. Remove white/blue lead from terminal 4; reconnect this lead to terminal 5.
3. On terminal block, remove violet lead from terminal 8; reconnect this lead to terminal 9. This changes the receiver current level from 60 mA to 20 mA.

A relay circuit card must be fabricated and connected to the paper tape reader driver circuit. The relay circuit card to be fabricated requires a relay, a diode, a thyrauctor, a small vector board for mounting the components, and suitable hardware for mounting the assembled relay card.

A circuit diagram of the relay circuit card is included in figure C-4; this diagram also includes the part numbers of the relay, diode, and thyrauctor. (Note that a 470- ohm resistor and a  $0.1\mu F$  capacitor may be substituted for the thyrauctor.) After the relay circuit card has been assembled, mount it in position as shown in figure C-5. Secure the card to the base plate using two self-tapping screws. Connect the relay circuit to the distributor trip magnet and mode switch as follows:

1. Refer to figure C-4 and connect a wire (Wire A) from relay circuit card to terminal L2 on mode switch (see figure C-6).
2. Disconnect brown wire shown in figure C-7 from plastic connector. Connect this brown wire to terminal 12 on mode switch. (Brown wire will have to be extended.)
3. Refer to figure C-4 and connect a wire (Wire B) from relay circuit board to terminal L1 on mode switch.

### EXTERNAL CONNECTIONS

Connect a two-wire receive loop, a two-wire send loop, and a two-wire tape reader control loop to the external device as shown in figure C-4. The external connector pin numbers shown in figure C-4 are for serial channel 1 on the Intellec Series III system.

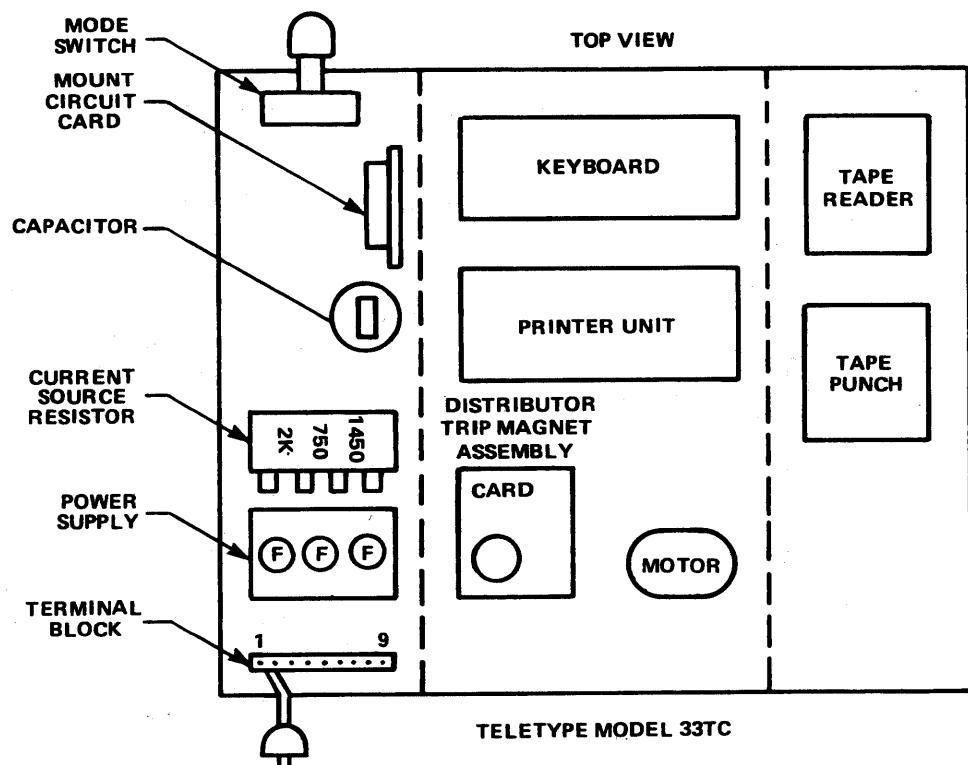


Figure C-1. Teletype Component Layout

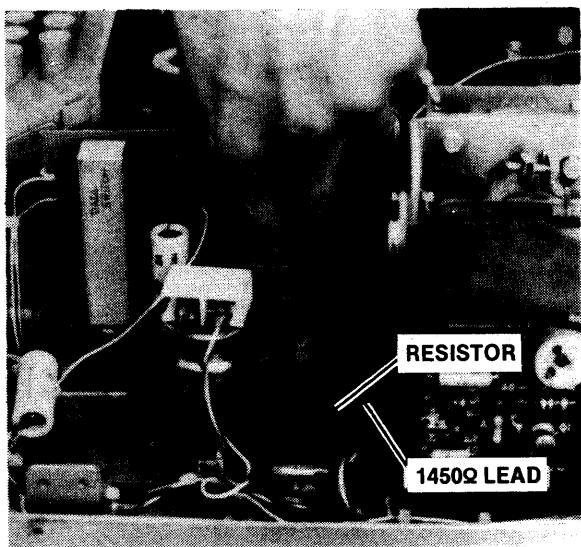


Figure C-2. Current Source Resistor

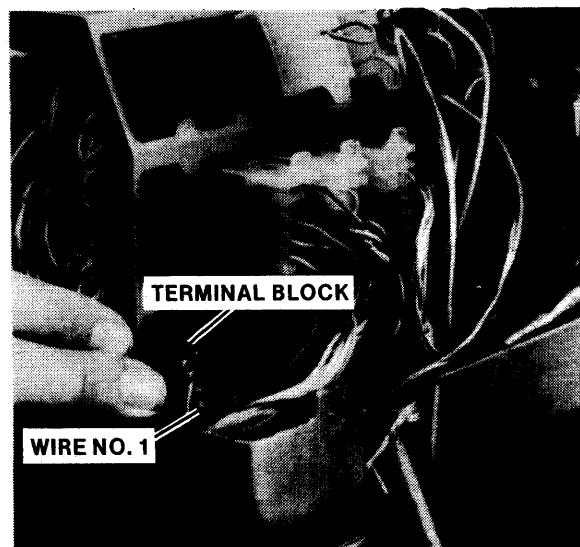


Figure C-3. Terminal Block

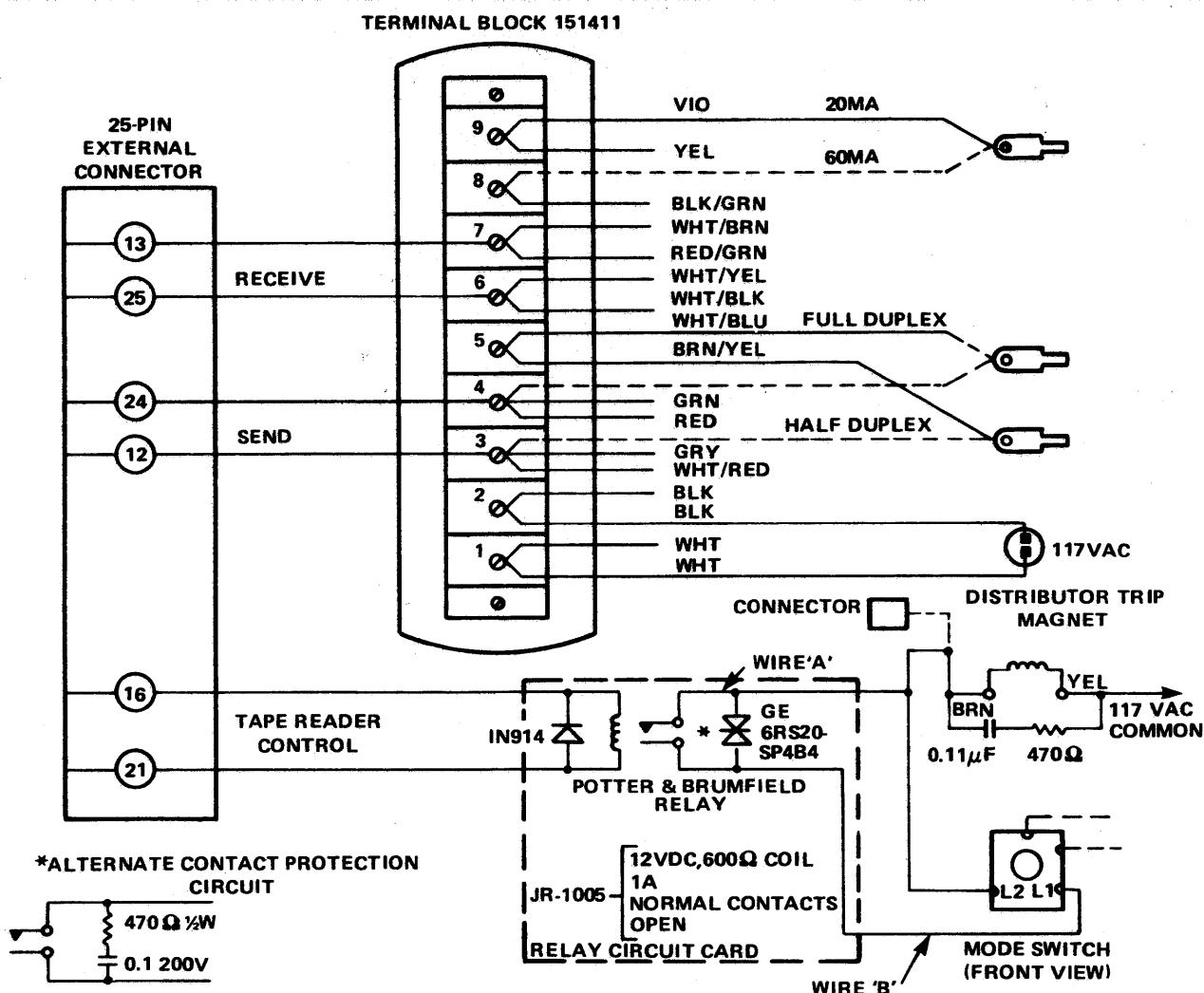


Figure C-4. Teletypewriter Modifications

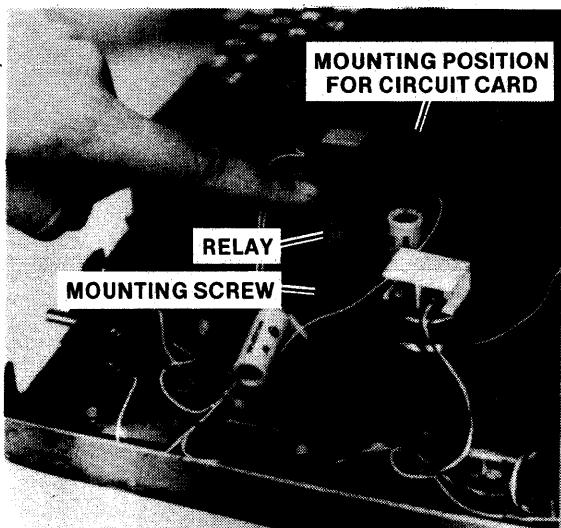


Figure C-5. Relay Circuit

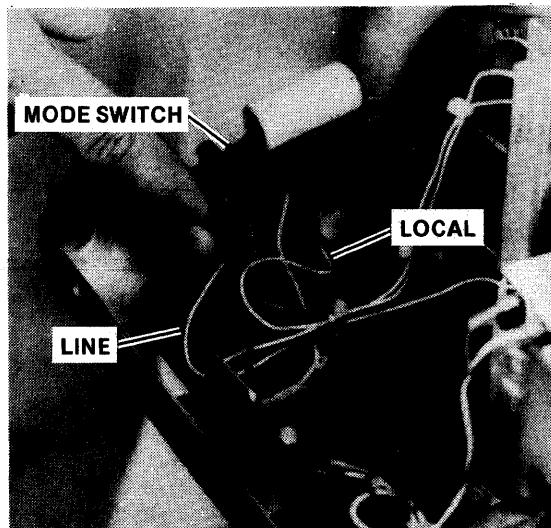


Figure C-6. Mode Switch

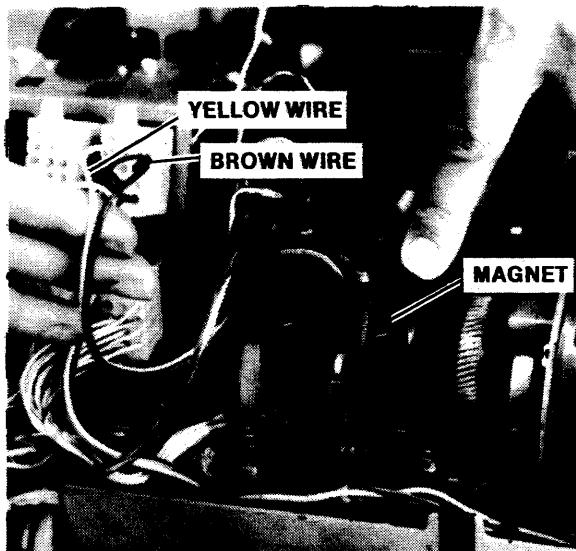


Figure C-7. Distributor Trip Magnet

In development work it is sometimes necessary to isolate chassis ground from signal ground. You can isolate these grounds in the Intellic Series III system by disconnecting a single wire from the power supply.

**WARNING**

Hazardous voltage is present in the vicinity of the power supply. Before proceeding, disconnect the system power cord from facility power.

To isolate the two grounds, you must first remove the top cover of the system. The ground connection is a yellow and green wire connected to the power supply. (Refer to figure D-1.)

The wire is connected to the power supply with a spade connector. Disconnect the wire and insulate the spade lug to prevent an accidental short. Replace the top cover and reconnect the system power cord to facility power.

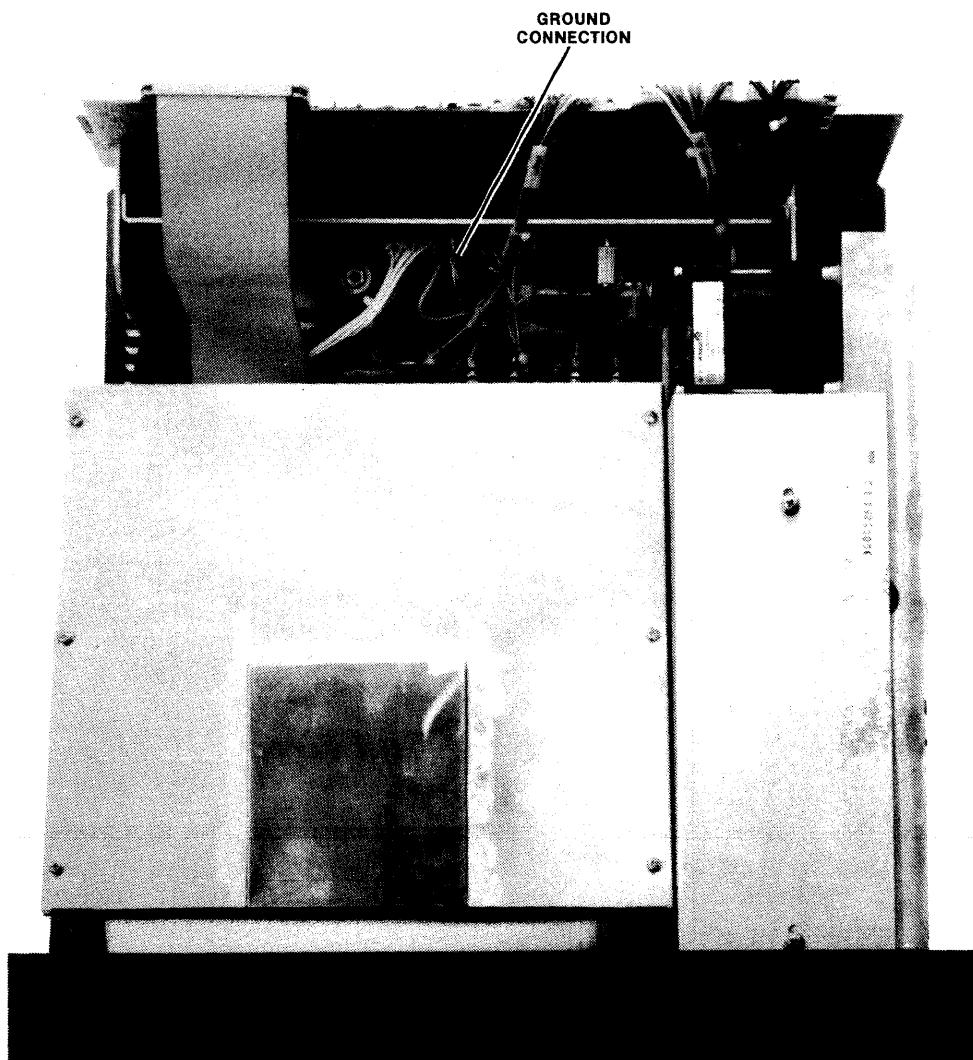


Figure D-1. Ground Connection

### E-1. MAINTENANCE SCHEDULE

The diskette drive or drives associated with the development system require periodic preventive maintenance. The recommended preventive maintenance schedule for normal (40 hours per week) operation is at 6-month intervals (shorter intervals are required for excessive operation and/or adverse environments). Table E-1 outlines the preventive maintenance requirements for diskette drives.

**Table E-1. Preventive Maintenance Requirements**

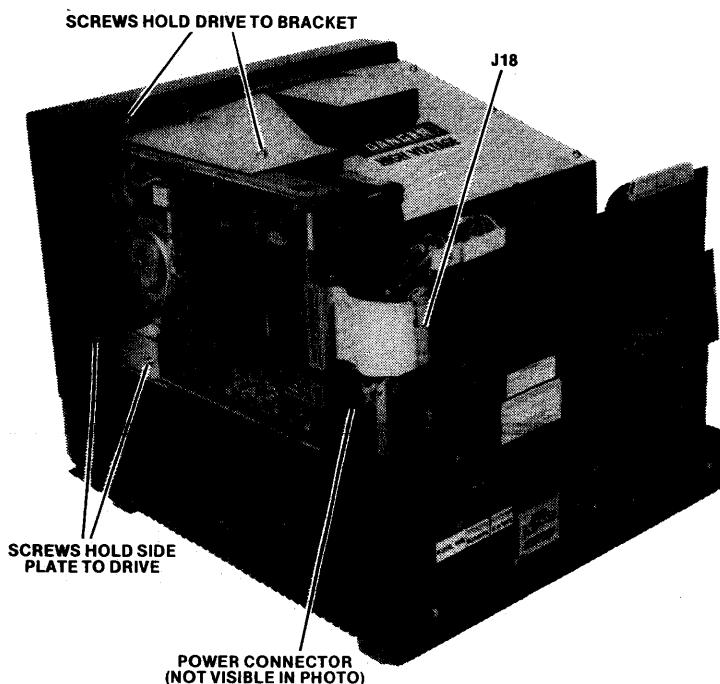
Inspect	Check For	Corrective Action
Read/Write head	Oxide build-up	Clean Read/Write head only if necessary
Head load pad	Wear, glazing	Replace head load pad
Drive belt	Fraying, cracks, loss of tension	Replace drive belt

In order to perform preventive maintenance on a drive, the drive must be removed from its chassis.

### E-2. INTEGRAL DRIVE REMOVAL

Remove the integral drive from the mainframe as follows:

- a. Power down system and disconnect mainframe power cord.
- b. Remove mainframe top cover and disconnect the following cable connectors at the drive:
  - (1) P25—controller interface connector
  - (2) P24—ac power connector
  - (3) P23—dc power connector
- c. Remove large braided ground strap (if present) between drive printed circuit board and mainframe chassis.
- d. Referring to figure E-1, remove the two screws securing drive to top mounting bracket, and remove the two screws securing side retainer plate to drive.
- e. Slide side retainer plate forward approximately  $\frac{1}{4}$ -inch to disengage “ears” and remove plate by raising it up and out of channel.
- f. Once side retainer plate is removed, pull rear of drive away from chassis.



**Figure E-1. Integral Drive Removal**

### E-3. DUAL DRIVE CHASSIS DRIVE REMOVAL

Remove the drives mounted in the dual drive chassis as follows:

- a. Power down both mainframe and dual drive chassis and disconnect power cords.
- b. Disconnect drive interface cable from rear panel of dual drive chassis.
- c. Place dual drive chassis on bench or suitable work surface capable of supporting chassis weight (approximately 43 pounds).
- d. Referring to figure E-2, remove the six Allen screws that secure top cover panel to drive chassis (a 7/64-inch angled Allen wrench is required) and remove top cover panel.
- e. Disconnect "daisy-chain" controller interface ribbon cable from top of each drive adapter printed circuit board; disconnect ac power connector (J3 and J4) and dc power connector (J1 and J2) from each drive.
- f. Each drive is secured to chassis by four screws accessible from bottom of drive chassis. Slide front of chassis over edge of work surface just

far enough to expose drive mounting screws. In the interest of safety, have someone hold chassis while screws are removed.

- g. Remove the four drive mounting screws, slide chassis back on work surface, and lift out drives.

## E-4. MAINTENANCE PROCEDURES

### E-5. READ/WRITE HEAD

Raise the spring-loaded head load arm and examine the head for oxide build-up. If, AND ONLY IF, oxide build-up is present (noted by a yellow-brown dull film visible on the clear surface of the head), clean the head using a cotton swab and isopropyl alcohol.

### E-6. HEAD LOAD PAD

The head load pad, which is subject to wear and "glazing" (a hardening of the pad surface), is press-

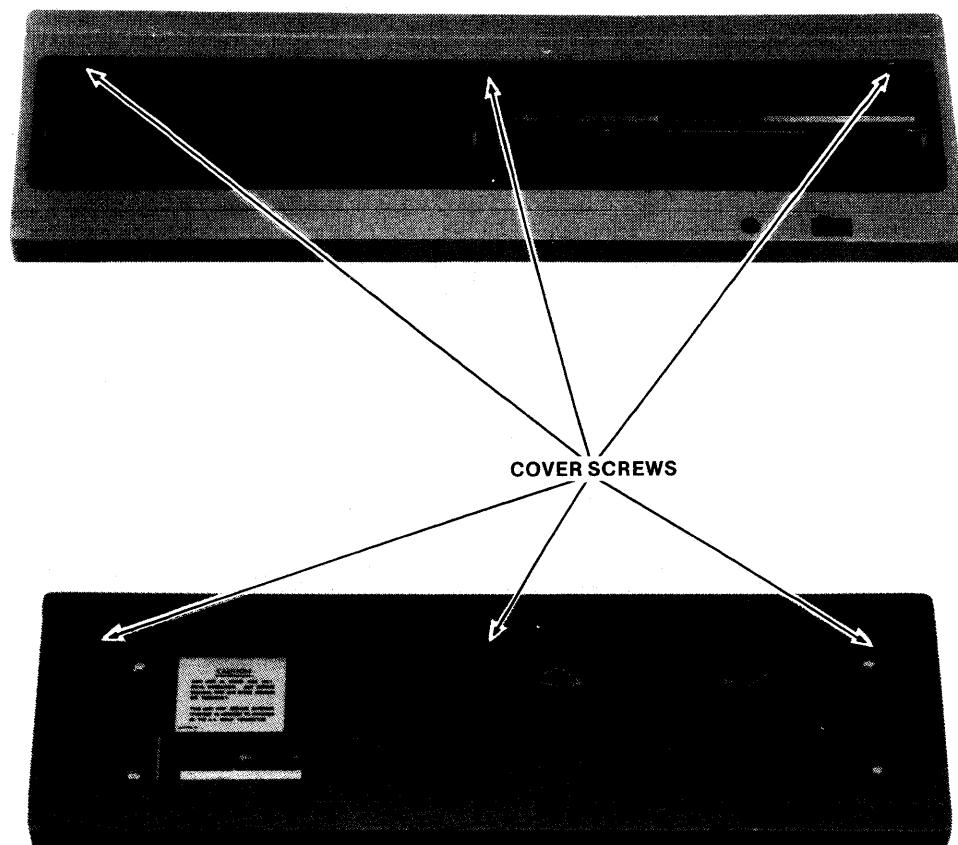


Figure E-2. Dual Drive Chassis Top Cover Removal

fit into the end of the head load arm. If the pad needs replacing, raise the head load arm (to avoid possibly damaging the read/write head) and, working from the back side of the pad with a small pair of needle-nose pliers, carefully pinch the pad halves together and push the halves down to clear the locking mechanism. Once clear of the locking mechanism, pry the pad out with a small screwdriver or fingernail. To install the new pad, simply press the pad into the head load arm until it locks in place.

## E-7. DRIVE BELT

The drive belt is subject to fraying or cracking that can lead to loss of belt tension or breakage. To examine the drive belt, turn the drive over. The belt is located under the printed circuit board and only a portion of the belt is visible at the drive motor pulley. Slowly rotate the pulley to examine the entire belt. Note that if the belt must be replaced, the printed circuit board must first be removed from the drive.



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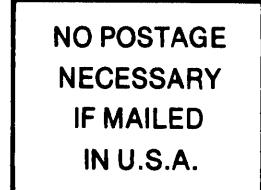
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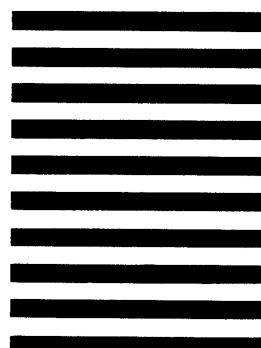
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