INTELLEC® SERIES II
MICROCOMPUTER
DEVELOPMENT SYSTEM
DOUBLE-DENSITY
DISKETTE SUBSYSTEM

schematic drawings

intel®

INTELLEC® SERIES II MICROCOMPUTER DEVELOPMENT SYSTEM DOUBLE-DENSITY DISKETTE SUBSYSTEM

Manual Order Number: 9800425-02 Rev. B

Additional copies of this manual or other Intel literature may be obtained from:

Literature Department
Intel Corporation
3065 Bowers Avenue
Santa Clara, CA 95051

The information in this document is subject to change without notice.

Intel Corporation makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Intel Corporation assumes no responsibility for any errors that may appear in this document. Intel Corporation makes no commitment to update nor to keep current the information contained in this document.

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied.

Intel software products are copyrighted by and shall remain the property of Intel Corporation. Use, duplication or disclosure is subject to restrictions stated in Intel's software license, or as defined in ASPR 7-104.9(a)(9).

No part of this document may be copied or reproduced in any form or by any means without the prior written consent of Intel Corporation.

The following are trademarks of Intel Corporation and may be used only to identify Intel products:

BXP	Intellec	Multibus
i	iSBC	Multimodule
ICE	iSBX	PROMPT
iCS	Library Manager	Promware
Insite	MCS	RMX
Intel	Megachassis	UPI
Intelevision	Micromap	μScope

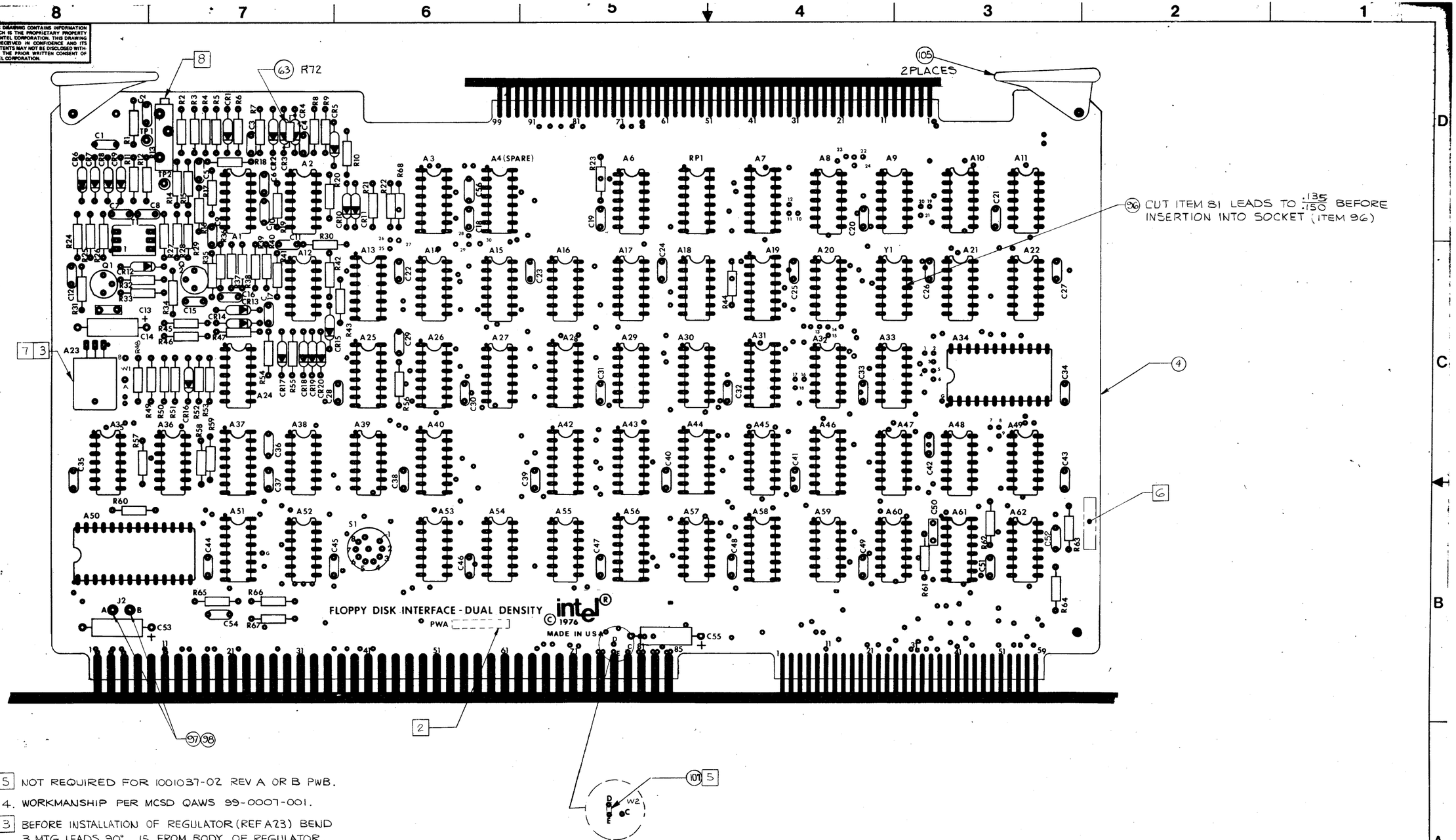
and the combination of ICE, iCS, iSBC, iSBX, MCS, or RMX and a numerical suffix.

Copyright © 1980 Intel Corporation
Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

CONTENTS

TITLE	NUMBER
CONTROLLER	
Printed Wiring Assembly, F.D. INTFC Dual Density	1001036
Schematic, FDC Interface Double Density (6 sheets)	123178
Printed Wiring Assembly, Floppy Disk Controller Channel	1000467
Schematic, Floppy Disk Controller Channel (4 sheets)	2000469
Controller Cable Dual Floppy	4002175
DRIVE CHASSIS	
Systems Interconn. Diagram, MDS-7XX (2 sheets)	2001926
Power Supply, MDS-71X/72X/73X (3 sheets)	4501498
Power Supply, Schematic, MDS-7XX (4 sheets)	2002677
Printed Wiring Assembly Signal Adaptor (sic)	1002242
Schematic, Signal Adapter	2002244
DC Signal Cable, Floppy Disk	4001496
Peripheral Cable Interconnect	4002176

THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.



5 NOT REQUIRED FOR 1001037-02 REV A OR B PWB.

4. WORKMANSHIP PER MCSD QAWS 99-0007-001.

3 BEFORE INSTALLATION OF REGULATOR (REF A23) BEND 3 MTG LEADS 90°, .15 FROM BODY OF REGULATOR.

2 MARK ASSY DASH NO. AND REV LEVEL WITH CONTRASTING PERM. COLOR, NON-CONDUCTIVE, .12 INCH HIGH APPROX WHERE SHOWN.

1. ASSY PART NO. IS 1001036-04. ASSY AND PL ARE TRACKING DOCUMENT.

NOTES: UNLESS OTHERWISE SPECIFIED

8 SEAL R13 WITH GLYPTOL OR EQUIVALENT AFTER TEST AND ADJUSTMENT.

7 INSULATE UNDER A23 HEATSINK (ITEM 32) USING ITEM 109.

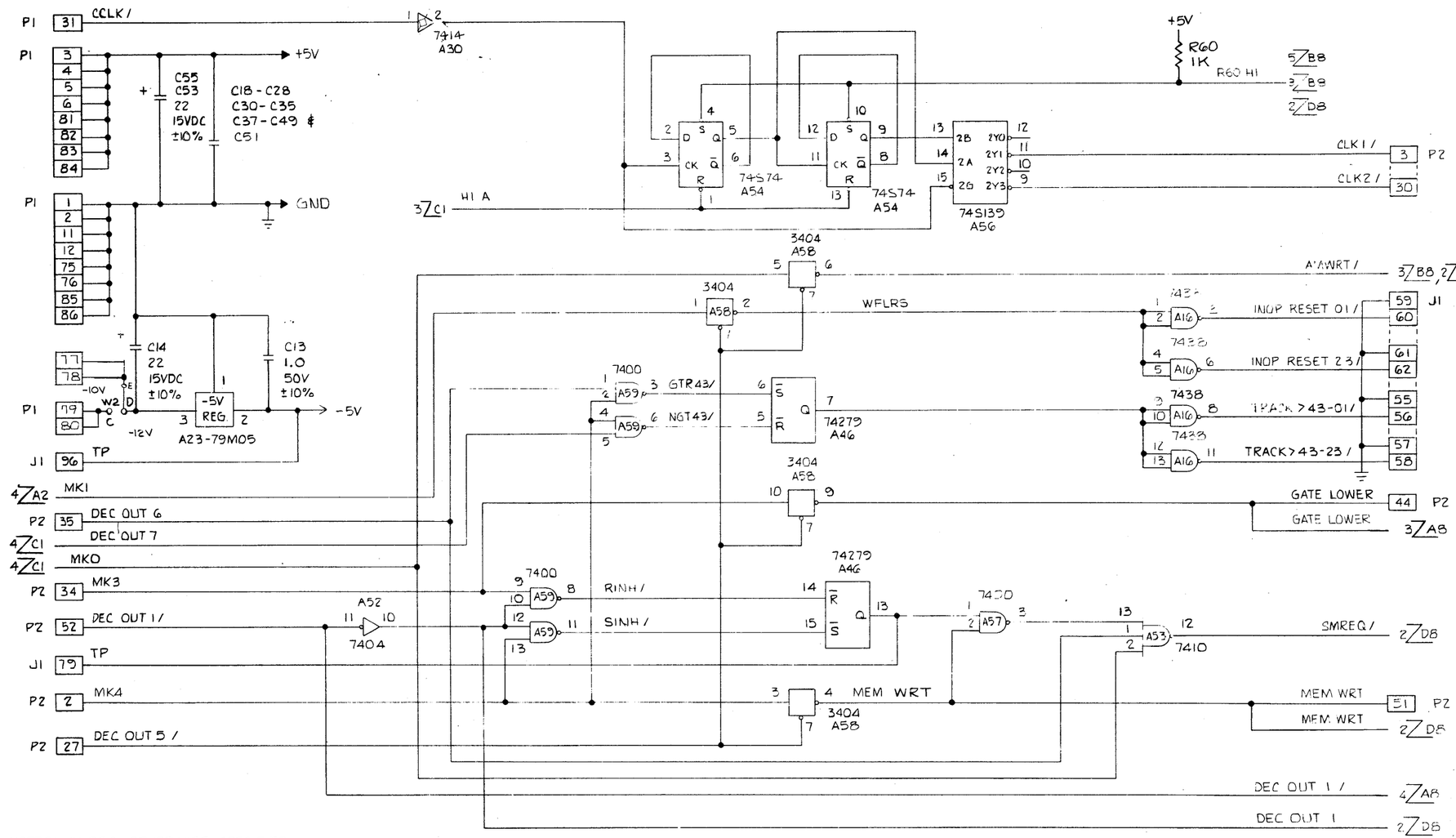
6 MARK ASSY VENDOR ID WITH CONTRASTING PERM. COLOR, NON-CONDUCTIVE, .12 INCH HIGH, APPROX WHERE SHOWN.

intel © INTEL 1977 3065 BOWERS AVE. SANTA CLARA CALIF 95051

PRINTED WIRING ASSEMBLY
F.D. INTFC DUAL DENSITY

SIZE	DEPT	DRAWING NO	REV
D	MCSD	P1001036	P

CODE | SHEET 1 OF 1



NOTES: UNLESS OTHERWISE SPECIFIED.

1. REMOVED
2. RESISTANCE VALUES ARE IN OHMS ±5%, 1/4W.
3. CAPACITANCE VALUES ARE IN MICROFARADS
4. CAPACITORS ARE 0.1UF, +80%, -20%, 50V, MONO.
5. DIODES ARE IN4148. #
6. THIS SWITCH SYMBOL —o—#—o— # DENOTES A MANUFACTURING CUT/JUMP OPTION FOR MFM ENCODING (DEFAULT = M²FM)

THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.

intel © INTEL '79 3065 BOWERS AVE. SANTA CLARA CALIF. 95051

TITLE SCHEMATIC FDC INTERFACE DOUBLE DENSITY

SIZE	DCLC	CL CODE	RLSE LVL	DWG NO.	REV
D	13	01	P	123178	A

CODE: SHEET 1 OF 6

THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.

P2 40 INT /
1/B2 MEM WRT — 5 A52 6 7404
RG0 HI
1/D3 OVRN CLK /
4/C1 SM REQ /
1/B2
P1 23 XACK /
1/A2 MK6 — 5 4 A57 6 MK6 /
DEC CUT 1
4/C1 MK5 — 12 13 A57 11 MK5 /
7400
74LS74 A 39
P2 37 (READ RI) /
P2 57 (READ INT) /
P2 49 RESET /
3/A8 (READ INT) /
4 3 5 6 7410 A53
P1 14 INIT /
P2 56 MR
4/C2 MR
5 4 A35 6 7400
9 8 7404 A52
P1 21 IORC / — 9 7414 8 A36 — 9 10 A38 8 7432
P1 22 IOWC / — 11 7414 10 A36
P2 53 WRT CMD
P2 60 READ CMD
P1 15 BPRN /
P1 3 BCLK /
5/B1 DISK WRITE
DISK WRITE / 5/B1
1/C2 A/V WRT /
3/D1 HEAD LOAD
3/C8 QC
3/B1 CLOCK GATE

74125 A55 — 5 6 — 5 4 7432 A38 — 6 11 A37 — 12
9602 RX2 CX2 Q 10 CD Q 9 13
RG7 5.6K +5V — 14 15
RG6 1K +5V
74LS112 A51 — 3 4 5 J S Q; 1 CK; 2 K R Q 6
74LS112 A51 — 11 10 9 J S Q; 13 CK; 12 K R Q 7 — 15 14
74LS74 A 39 — 2 D S Q 5; 3 CK; 4 R Q 6 — 1

XFER REQ / P2 39
1 INT0 / 41 P1
2 INT1 / 42
3 INT2 / 39
4 INT3 / 40
5 INT4 / 37
6 INT5 / 38
7 INT6 / 35
8 INT7 / 36
12 13 11 74125 A55 S1

+5V
9 28 MRDR / BPRO / 23 — J2 B A — BPRO / 16 P1
7 MWTR /
8 IORR / BREQ / 21 — BREQ / 18
6 IOWR /
BUSY / 18 — BUSY / 17
24 BCR2 /
25 BCR1 MWTC / 16 — MWTC / 20
3 XSTR MRDC / 12 — MRDC / 19 P1
4 XCP / IORC / 13
26 RSTB / IOWC / 17
27 OVRD
ANYR 10
22 BPRN / RDD 11
20 BCLK / XCY / 5 — TP 5 P2
2 CLRSH /
15 DLYADJ ADEN / 19 — 3 4 7404 A52 — SELECTED 43
INIT / 14 1
52-104 A50

RG5 240
C54 220PF 500V ±5%

MR / 4/A8
MR / 46 P2
DOR / 16
STB MEM IN 29
TP 59

7438
1 2 A9 3 (WRT GT 0,1) / 14 J1
4 5 A9 6 (WRT GT 2,3) 13 16 15
7438

74S04 A20 — 1 2
74164 A8 — R; A; B; CK 8; 9; 2; 1; QA QB QC QD QE QF QG QH 3 4 5 6 10 11 12 13
A20 10 11 74S04 — 7402 A22 — 12 13 (DL)
74111 A32 — 9 10 11 8 (D)
7408 A21 — 12 13 11
7408 A21 — 10 9 8 (C)
A20 9 8 74S04 — 7402 A22 — 8 9 10 (DE)
A20 13 12 74S04 — 13 14 15 1 A32 12 (CE) — 74H11 — 2
10 12 11

74157 — +5V 1 16; S VCC; 2 1A 1B 2A 2B 3A A7 3B 4A 4B STB; 3 5 6 11 10 14 13 15; 1Y 2Y 3Y 4Y; 4 7 9 12; GND 8
22 23 24
1 2 3 4 5 6
74150 A34 — +5V 24; S 9; W 10; E15 E14 E13 E12 E11 E10 E9 E8 E7 E6 E5 E4 E3 E2 E1 E0 16 17 18 19 20 21 22 23 1 2 3 4 5 6 7 8; A B C D 15 14 13 11; 12
K115A 8MHZ OSC — 1 11 12 10 2 3 13; 14 PIN SOCKET Y1 — 6 5 9 4; +5V 14 7

7404 A32 — 10 11
7438 — 9 10 12 13 A9 — 8 (WRT DAT 0,1) / 11 (WRT DAT 2,3) / — 10 9 12 11
WRT DAT / 3/C8

SD A
SD B
SD C
SD D — 3/1B
WRITE CLOCK 3/C8, 5/A8

SCALE: NONE	SIZE	DEPT	DRAWING NO.	REV
SHEET 2 OF 6	D	13	123178	A

© INTEL 1977

4/C1 HEAD LOAD /

+5V
RP1 220
J1 READY 0 /
READY 1 /
READY 2 /
READY 3 /
WPROT 0,1/
WPROT 2,3/
RP1 330
7414 A30 (4 PLCS)

+5V
74153 A31
1C0 1C1 1C2 1C3 2G 2C0 2C1 2C2 2C3 1Y 2Y

+5V
74S139 A56
1A 1B 1G 1Y0 1Y1 1Y2 1Y3

P2 9 USA
P2 12 USB

2/A1 WRITE CLOCK
2/A8 QC
2/B1 WRT DAT /

74LS74 A10
74LS74 A10

1/C2 AM WRT/
J1 73 TP
+5V R23 1K
4/B2 RDY RS /
4/C1 W DATA /
1/D3 RG0 HI

74LS112 A44
74LS112 A44
74LS112 A43
74LS112 A43

2/C8 (READ INT)/
1/C2 GATE LOWER

(SEL DR NRDY)/ P2 20
(DISK WPROT) / 14
LED 0 / J1 54
LED 1 / 53
LED 2 / 66
LED 3 / 65
74367 (4 PLCS) A28
HEAD LOAD 64
2/B8 63
DRV SEL 3/ 68
DRV SEL 2/ 67
DRV SEL 1/ J1 52
DRV SEL Ø/ 51
50
49
48
47
46
45
7404 (5PLCS) A29
7438 (4PLCS) A17

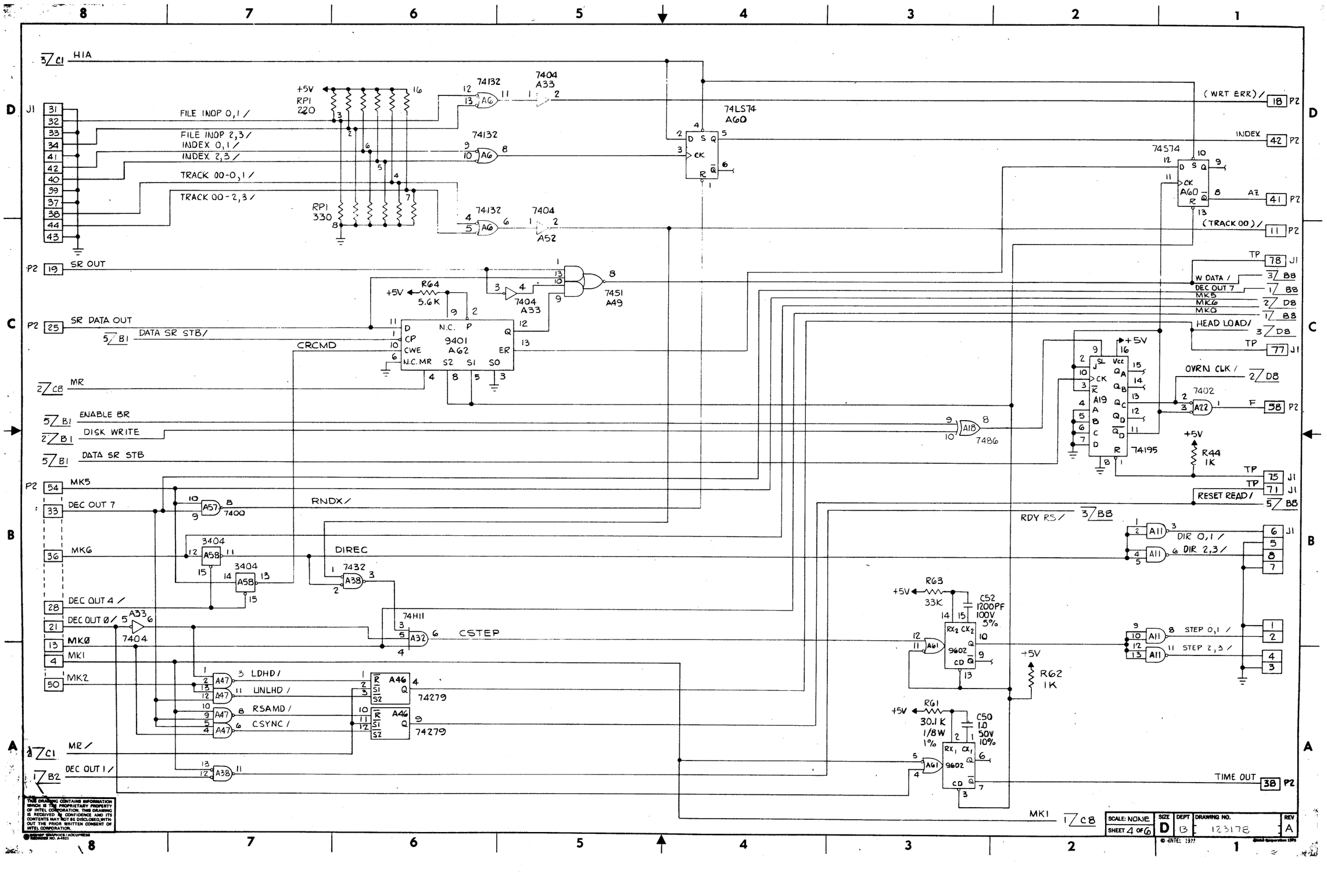
TP J1 76
2F CLOCK 5/C8
HIA 5/A8
4/D8
1/D6
7486 A18
74164 A48
TP J1 69
SD D
SD C
SD B
SD A 2/A1

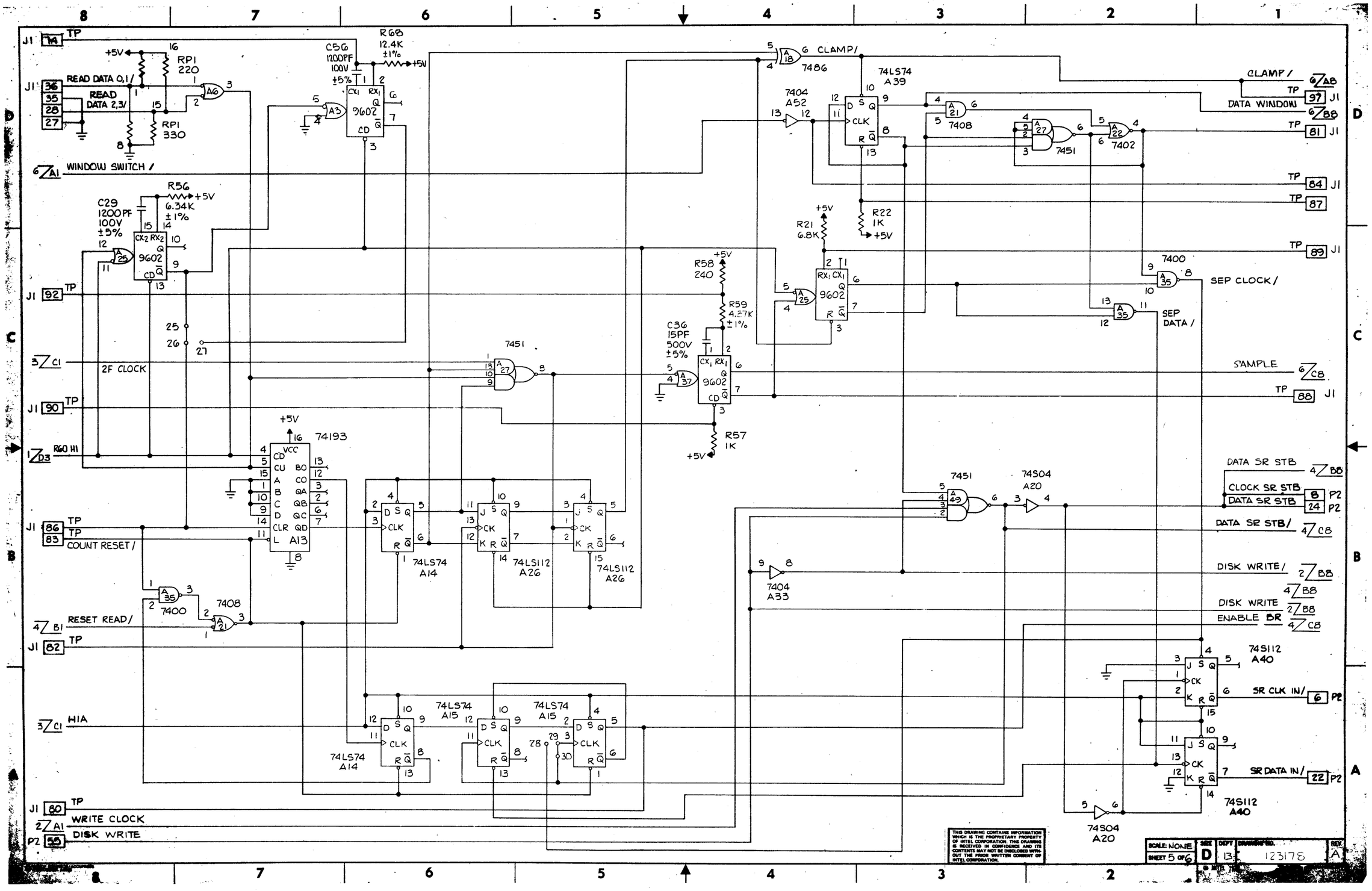
CLOCK GATE 2/A8
DAT 0 / P1 73
(DR2/) DR0 / P2 15
DAT 1 / P1 74
(DR3/) DR1 / P2 17
DAT 5 / P1 70
DAT 6 / P1 67
DAT 4 / P1 69
7400 A45
74367 A42
74367 A28
7404 A29
74125 A55

THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.

SCALE: NONE	SIZE	DEPT	DRAWING NO.	REV
SHEET 3 OF 6	D	B	123178	A

©Intel Corporation 1979


HIA
J1
FILE INOP 0,1/
FILE INOP 2,3/
INDEX 0,1/
INDEX 2,3/
TRACK 00-0,1/
TRACK 00-2,3/
+5V
RP1 220
RP1 330
74132 A46
74132 A36
74132 A52
7404 A33
7404 A52
74LS74 A60
(WRT ERR)/ 18 P2
INDEX 42 P2
74S74 AG0
A7 41 P2
(TRACK 00)/ 11 P2
SR OUT
SR DATA OUT
DATA SR STB/
CRCMD
R64 5.6K
7451 A49
9401 A62
N.C. P D CP CWE N.C. MR S2 S1 S0 Q ER
MR
ENABLE BR
DISK WRITE
DATA SR STB
MK5
DEC OUT 7
MK6
DEC OUT 4/
DEC OUT 0/
MK0
MK1
MK2
RNDX/
DIREC
7400 A57
3404 A58
7432 A38
74H11 A32
CSTEP
LDHD/
LINLHD/
RSAMD/
CSYNC/
74279 A46
74279 A46
ME/
DEC OUT 1/
7486 A18
74195 A19
7402 A22
TP 78 J1
W DATA/ 3/B8
DEC OUT 7 1/B8
MK5 2/D8
MK6 1/B8
MK0 3/D8
HEAD LOAD/
TP 77 J1
OVRN CLK/ 2/D8
F 38 P2
R44 1K
TP 75 J1
TP 71 J1
RESET READ/ 5/B8
RDY RS/ 3/B8
DIR 0,1/
DIR 2,3/
STEP 0,1/
STEP 2,3/
R63 33K
C52 1200PF 100V 5%
9602 A61
R62 1K
R61 30.1K 1/8W 1%
C50 1.0 50V 10%
TIME OUT 38 P2
MK1 1/C8
THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED, WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.
SCALE: NONE
SHEET 4 OF 6
SIZE D
DEPT 13
DRAWING NO. 123178
REV A
© INTEL 1977


J1 14 TP
+5V
RP1 220
READ DATA 0,1/
J1 36
J1 35
READ DATA 2,3/
J1 28
J1 27
RP1 330
C56 1200PF 100V ±5%
R68 12.4K ±1%
+5V
9602
6 A1 WINDOW SWITCH /
C29 1200PF 100V ±5%
R56 6.34K ±1% +5V
J1 92 TP
25
26
27
3 C1 2F CLOCK
J1 90 TP
1 D3 R60 H1
7451
74193
J1 86 TP
J1 83 TP
COUNT RESET /
7400
7408
4 B1 RESET READ /
J1 82 TP
3 C1 H1A
74LS74 A14
74LS112 A26
J1 80 TP
2 A1 WRITE CLOCK
P2 50 DISK WRITE
7486
CLAMP /
7404 A52
74LS74 A39
7408
7451
7402
CLAMP / 6 A8
TP 97 J1
DATA WINDOW
6 B8
TP 81 J1
TP 84 J1
TP 87
R21 6.8K
R22 1K +5V
TP 89 J1
R58 240
R59 4.27K ±1%
C36 15PF 500V ±5%
R57 1K
7400
SEP CLOCK /
SEP DATA /
SAMPLE 6 C8
TP 88 J1
7404 A33
7451
7404 A20
DATA SR STB 4 B8
CLOCK SR STB
DATA SR STB 8 P2 24 P2
DATA SR STB / 4 C8
DISK WRITE / 2 B8 4 B8
DISK WRITE ENABLE BR 2 B8 4 C8
74S112 A40
SR CLK IN / 6 P2
SR DATA IN / 22 P2
74S04 A20
THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.
SCALE: NONE
SHEET 5 OF 6
SIZE D
DEPT 13
DRAWING NO. 123178
REV A

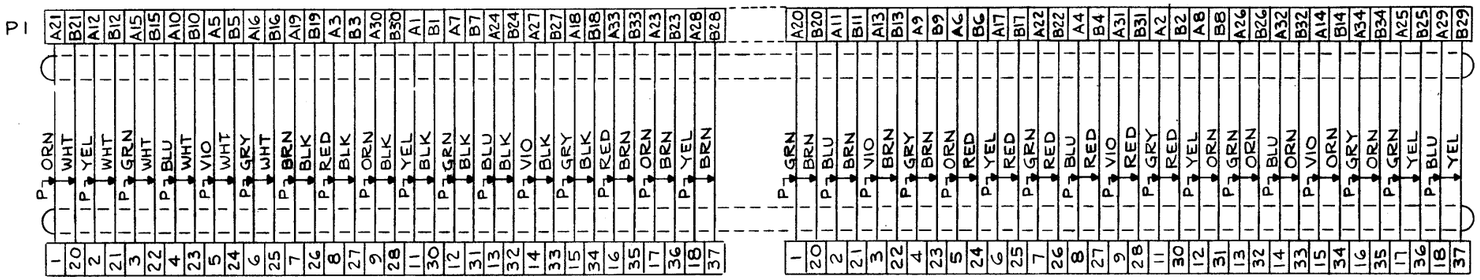
THIS DRAWING AND SPECIFICATION, EITHER IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION, AND IS LOANED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.

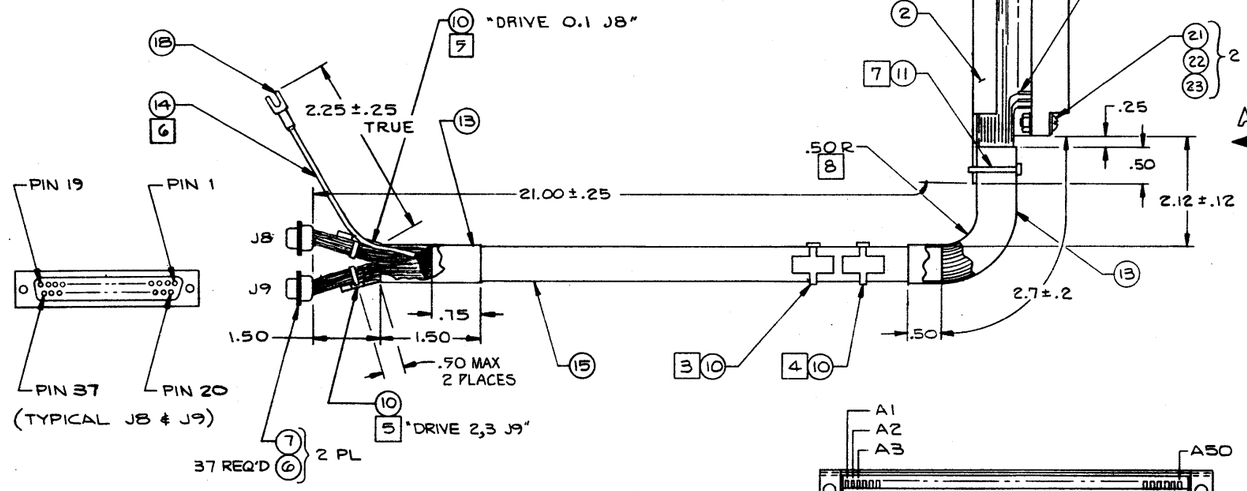
TP1
TI
R12 100
R11 200 ±1%
R24 200 ±1%
TP2
+5V
R33 10
C12
R31 510
R32 5.1
CR12
Q1 2N2222A
5 ZC1 SAMPLE
R25 26 ±1%
R26 150 ±1%
C7
C8
R27 50 ±1%
R28 261 ±1%
+5V
-5V
R1
R3
TP 95 J1
TP 100 J1
+5V
C3
R5 1K ±1%
CR1
R2 1.2K
R4 4.02K ±1%
A1 14
R16 49.9 ±1%
R29 6.2K
C9
A1 5 6 7
-5V
R15 49.9 ±1%
A1 3 1
TP 98 J1
J1 94 TP
CR5 1N5221B
A2 9 10 11
R17 1K
R18 1K ±10%
A2 4 5 3
C10 510PF 500V ±5%
R7 240
R20 100
A2 14 12 13
TP 93 J1
+5V
R40 510
R35 100
R36 100
A12 2 3 1
R34 240
C15
-5V
CR20
CR19
CR18
R41 510
2K
A1 9 8
CR2 10
CR3
C6
R72 15
CR4
A24 11 10
A24 6 7
A24 8 1
C11
R54 510
-5V
R53 510
-5V
C17
CR14
CR13
C16
A2 5 6 7
-5V
R23 1K
TP 91 J1
C4
R19 150
R42 510
CR3
R43 1.3K
A2 3 2 1
R8 3.9K
-5V
5 ZD2 DATA WINDOW
5 ZD2 /LAMP/
R45 4.7K
R46 240
A12 8 9 10
R10 10K
-5V
R50 1K
CR10 CR11
R38 100
+5V
R52 5.1K
A24 2 1 4 5 3
CR16
R51 240
-5V
R48 560
R49 390
A24 14 12 13
WINDOW SWITCH/ 5 ZD8
TP 99 J1

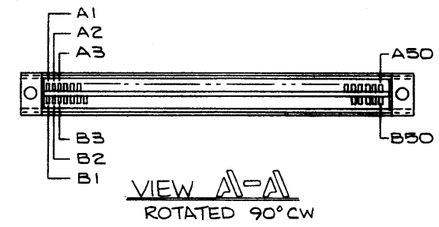
SCALE: NONE	SIZE D	DEPT 13	DRAWING NO. 103178	REV A
SHEET 6 OF 6				

© INTEL 1972

THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.







VIEW A-A
ROTATED 90° CW

8 FORM .5" RADIUS PRIOR TO SHRINKING SLEEVE IN PLACE.

7 PUT TIE WRAP KNOT UNDERNEATH AS SHOWN.

6 SHIELD OF CABLE TO BE ROLLED INTO SINGLE CONDUCTOR AND SLEEVED AS SHOWN.

5 MARK NOMENCLATURE AND/OR REF DES AS SHOWN IN PERMANENT CONTRAST INK.

4 MARK ASSY VENDOR ID WITH CONTRASTING PERM COLOR, .12 HIGH, APPROX WHERE SHOWN.

3 MARK ASSY PART NO. AND REV. LEVEL WITH CONTRASTING PERM COLOR. .12 HIGH, APPROX WHERE SHOWN.

2. WORKMANSHIP PER MCSD QAWS 99-0007-001.

1. ASSY PART NO. IS 4002175-01. ASSY & PL ARE TRACKING DOCUMENTS.

NOTES: UNLESS OTHERWISE SPECIFIED

intel®
3065 BOWERS AVE.
SANTA CLARA
CALIF. 95051

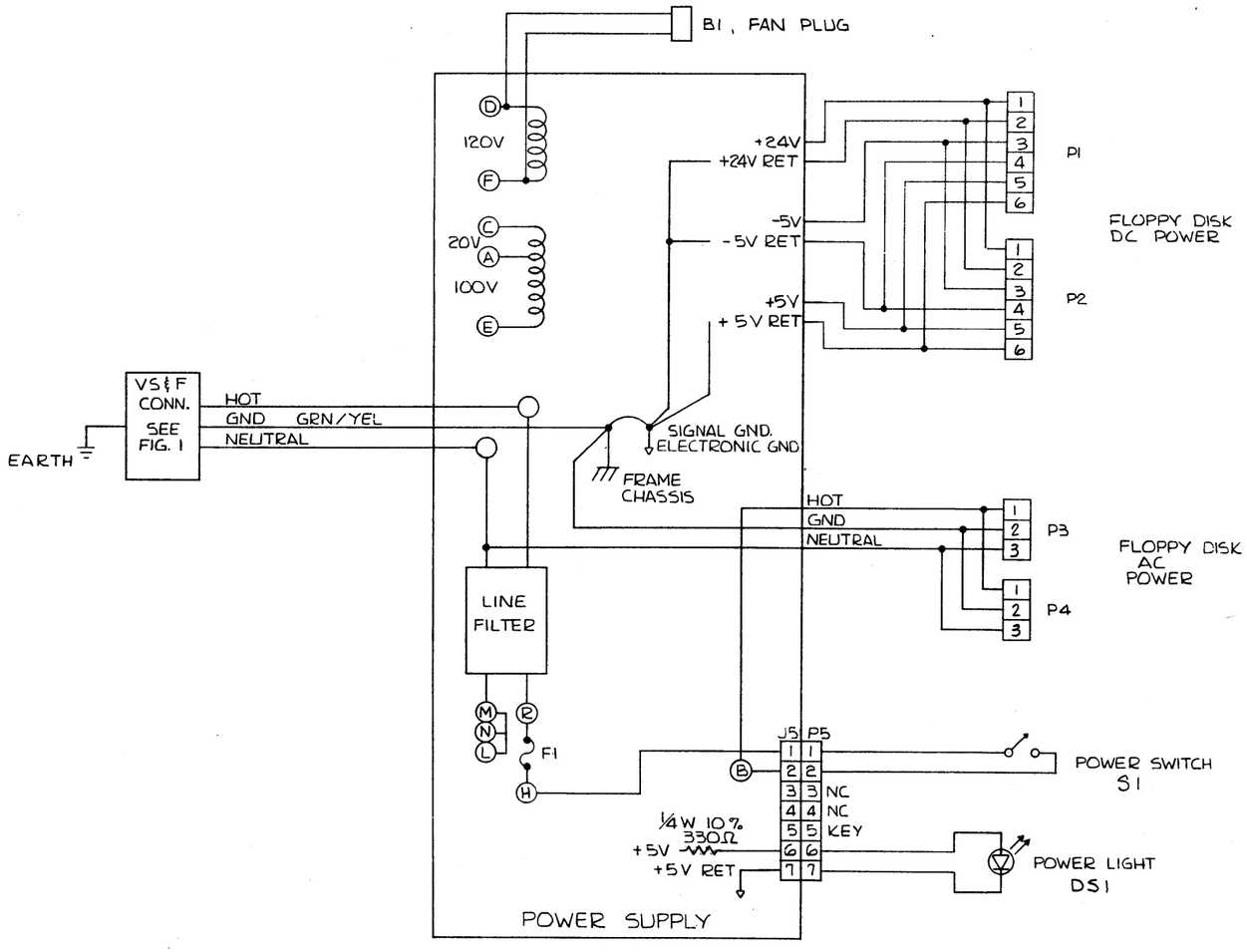
TITLE
CONTROLLER CABLE
DUAL FLOPPY

SIZE	CODE	DWG. NO.	REV
D	MCSD	P4002175	D

SCALE NONE SHEET 1 OF 1

9300021

THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.



1. FUSE: 2 AMP. FAST-BLOW FOR 110 VAC,
1 AMP. FAST-BLOW FOR 240 VAC.

NOTES: UNLESS OTHERWISE SPECIFIED:

98-253A

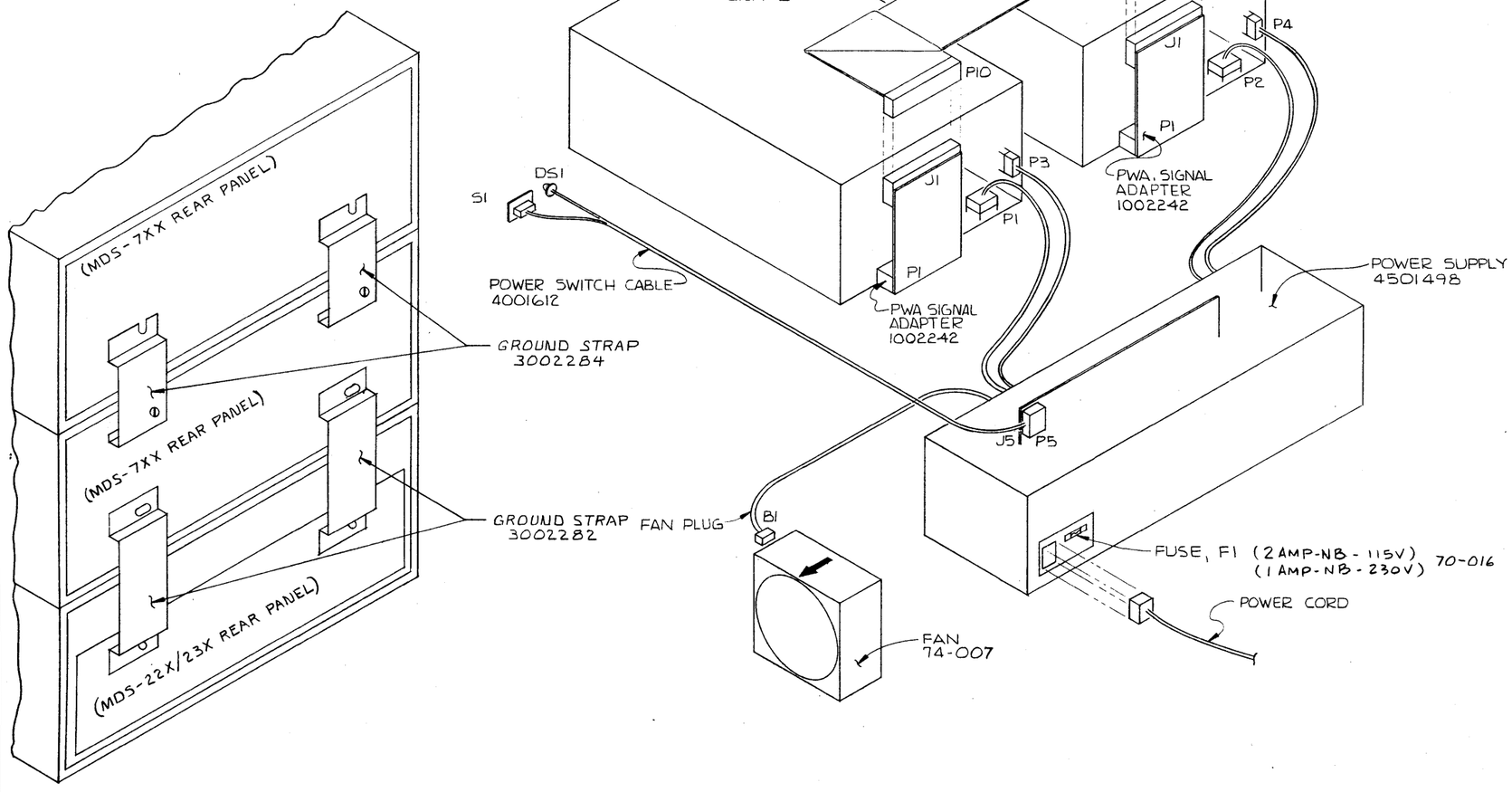
intel 3065 BOWERS AVE. SANTA CLARA CALIF. 95051

TITLE: SYSTEMS INTERCONN. DIAGRAM MDS-7XX

SIZE	DEPT	DRAWING NO.	REV
D	MCSD	L2001926	B

CODE: SHEET 1 OF 2

THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS DISCLOSED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.



SCALE: NONE	SIZE	DEPT	DRAWING NO.	REV
SHEET 2 OF 2	C	MCSD	EL2001926	B

THE INFORMATION CONTAINED HEREIN IS THE EXCLUSIVE PROPERTY OF INTEL CORPORATION. THIS DRAWING IS LOANED TO CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE WRITTEN PERMISSION OF INTEL CORPORATION.

ELECTRICAL SPECS:

1. INPUT: 100, 115, 220, 230 VAC ± 10%, 47-440 Hz.
2. OUTPUT:

2.1 +5VDC NOMINAL ADJUSTABLE ± 5% TO BE SET AT NOMINAL ± 1%
MAX LOAD: AT +5.0V, 3AMP.
LINE LOAD REGULATION COMBINED 1.0%
MAX RIPPLE: 40 MVPP. OR 10 MV RMS.
TRANSIENT RESPONSE: 50 μSEC MAX FOR A 50% LOAD CHANGE.
OVER-VOLTAGE PROTECTION: 5.8V TO 6.6V.
OVER-CURRENT FOLDBACK PROTECTION: 5% TO 50% OVERLOAD

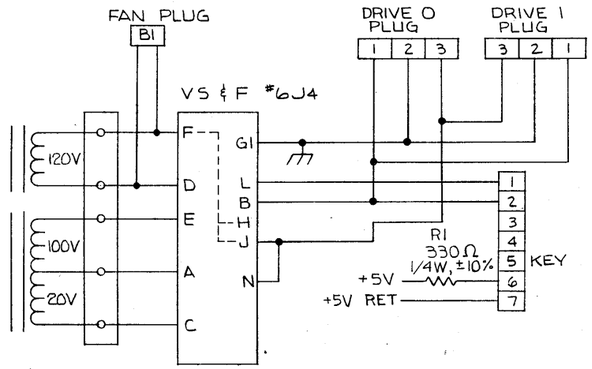
2.2 -5 VDC NOMINAL ADJUSTABLE ± 5% TO BE SET AT NOMINAL ± 1%
MAX LOAD: AT -5.0V, 0.4 AMP
LINE LOAD REGULATION COMBINED 1.0%
MAX RIPPLE: 40 MV PP OR 10 MV RMS
TRANSIENT RESPONSE: 50 μSEC MAX FOR A 50% LOAD CHANGE.
SHORT CIRCUIT CURRENT SHALL NOT EXCEED 2.3 AMPS

2.3 +24 VDC NOMINAL ADJUSTABLE ± 5% TO BE SET AT NOMINAL ± 1%
MAX LOAD AT +24V, 2.5 AMPS.
LINE LOAD REGULATION COMBINED: 1.0%
MAX RIPPLE: 100 MVPP OR 25 MV RMS
OVER-CURRENT FOLDBACK PROTECTION: 5% TO 50% OVERLOAD
SEPARATE GROUND RETURN PROVIDED, CONNECTED TO ELECTRONIC GROUND AT ONE POINT.

3. A SINGLE GREEN WIRE WITH YELLOW STRIPE WILL CONNECT VS & F CONNECTOR FRAME GROUND TO CHASSIS.
4. ALL ELECTRONIC GROUNDS (+5V, -5V, +24V) SHALL BE COMMON AND ISOLATED FROM FRAME GROUND.
5. TEMPERATURE COEFFICIENT: ± .02% PER °C MAX.
6. OVER-VOLTAGE PROTECTION NEED NOT BE ADJUSTABLE.
7. LINE FILTER REQUIRED.
8. ENVIRONMENT:
AMBIENT TEMP. 0°C TO 65° C.
HUMIDITY: 90% WITH NO CONDENSATION.
9. LIFE EXPECTANCY: 10 YEARS.
10. THIS POWER SUPPLY TO PASS ELECTROSTATIC DISCHARGE TESTS PER INTEL SPECIFICATION 9400010 AT A LEVEL OF 15 KILOVOLTS.

ELECTRICAL SPECS (CONT.)

11. EFFICIENCY SHALL BE 30% OR GREATER AT FULL LOAD
12. VOLTAGE ADJUSTMENT POTENTIOMETERS SHALL BE ACCESSIBLE FROM THE TOP OF UNIT.
13. ALL MEASUREMENTS TO BE MADE AT THE END OF THE APPROPRIATE POWER CABLE CONNECTOR.



10. MULTIPLE PIECE CHASSIS CONSTRUCTION ACCEPTABLE.
9. MARK NOMENCLATURE AS SHOWN IN PERMANENT CONTRASTING INK
8. REMOVED
7. PROVIDE 2 AMP, NORMAL BLOW, FUSE, ITEM 11, IN VS & F CONN., ITEM 8.
6. ALL LARGE CAPACITORS MUST BE SECURELY FASTENED TO CHASSIS.
5. 100% BEARING SURFACE REQ'D BEHIND HARDWARE LOCKING DEVICES.
4. STRAIN RELIEF REQ'D ON ALL CABLES EXTENDING BEYOND ENVELOPE.
3. MARK VENDOR I.D. WITH CONTRASTING PERM. COLOR, APPROX. WHERE SHOWN.
2. MARK PART NO. AND REV LEVEL WITH CONTRASTING PERM COLOR, .12 HIGH, APPROX WHERE SHOWN.
1. PART NO. IS 4501498-02. SPEC CONTROL DRAWING AND LIST OF VENDORS ARE TRACKING DOCUMENTS.

NOTES: UNLESS OTHERWISE SPECIFIED;

17. MOUNT ITEM 13 ON PWB SUPPORT PLATE APPROX WHERE SHOWN.
16. INTERNAL AC WIRING FROM TRANSFORMER SECONDARY TO REGULATOR CARD SHALL BE SLEEVED.
15. PROVIDE INSULATING COVER OVER CONNECTOR J5 WITH THE FOLLOWING LABEL: WARNING HIGH VOLTAGE DO NOT TOUCH
14. ALL DIMENSIONS ARE IN INCHES.
13. WORKMANSHIP PER MCSD QAWS 99-0007-001.
12. REMOVE PIN 5, LOCATE AT APPROX POSITION SHOWN.
11. FINISH: ALODINE 1000, CLEAR.

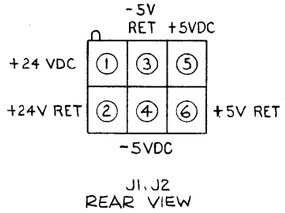
intel 3065 BOWERS AVE. SANTA CLARA CALIF. 95051

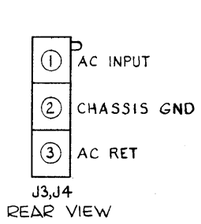
TITLE: POWER SUPPLY MDS-71X/72X/73X

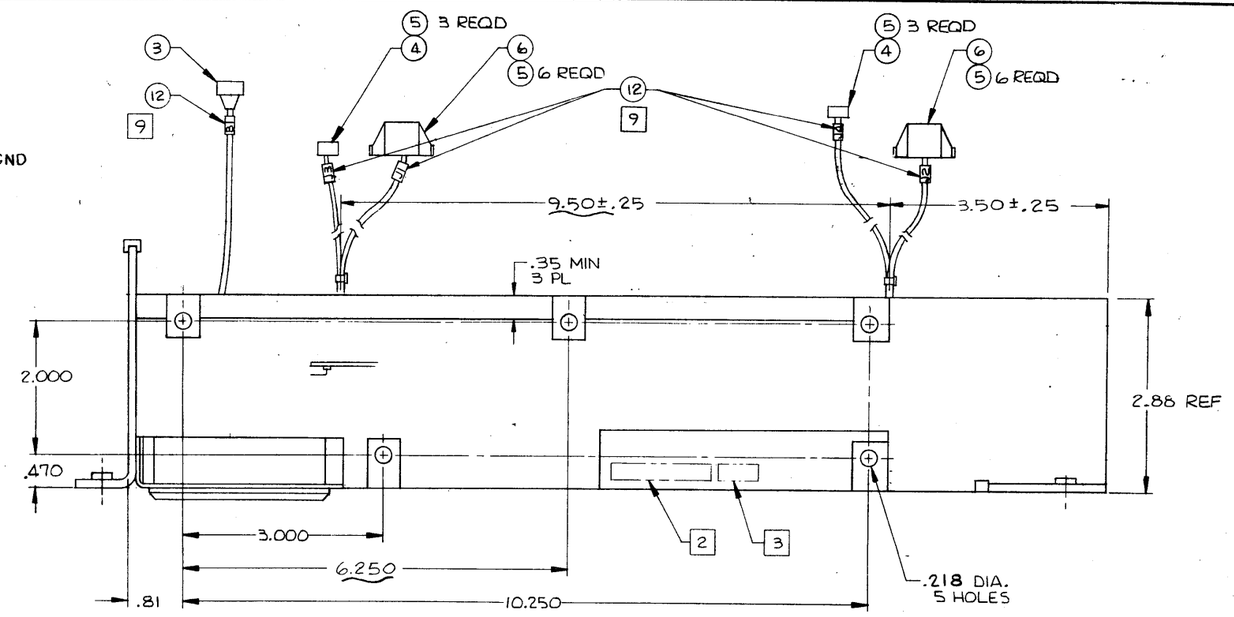
SIZE	DEPT	DRAWING NO.	REV
D	MCSD	L4501498	E

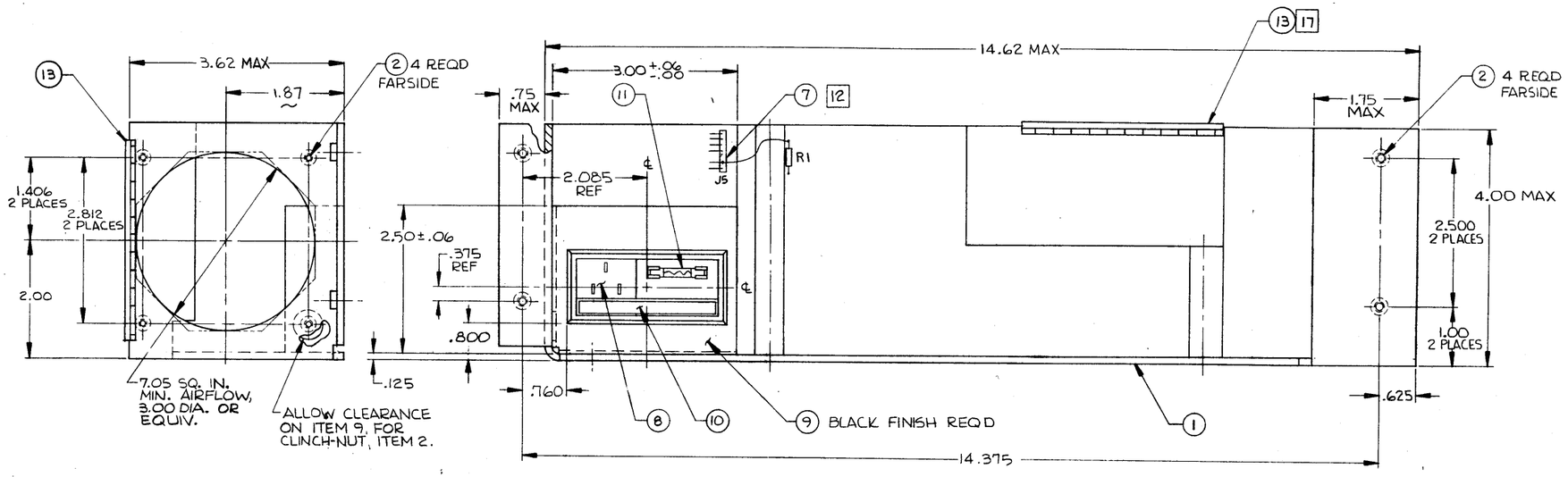
CODE: SHEET 1 OF 3

98-253A



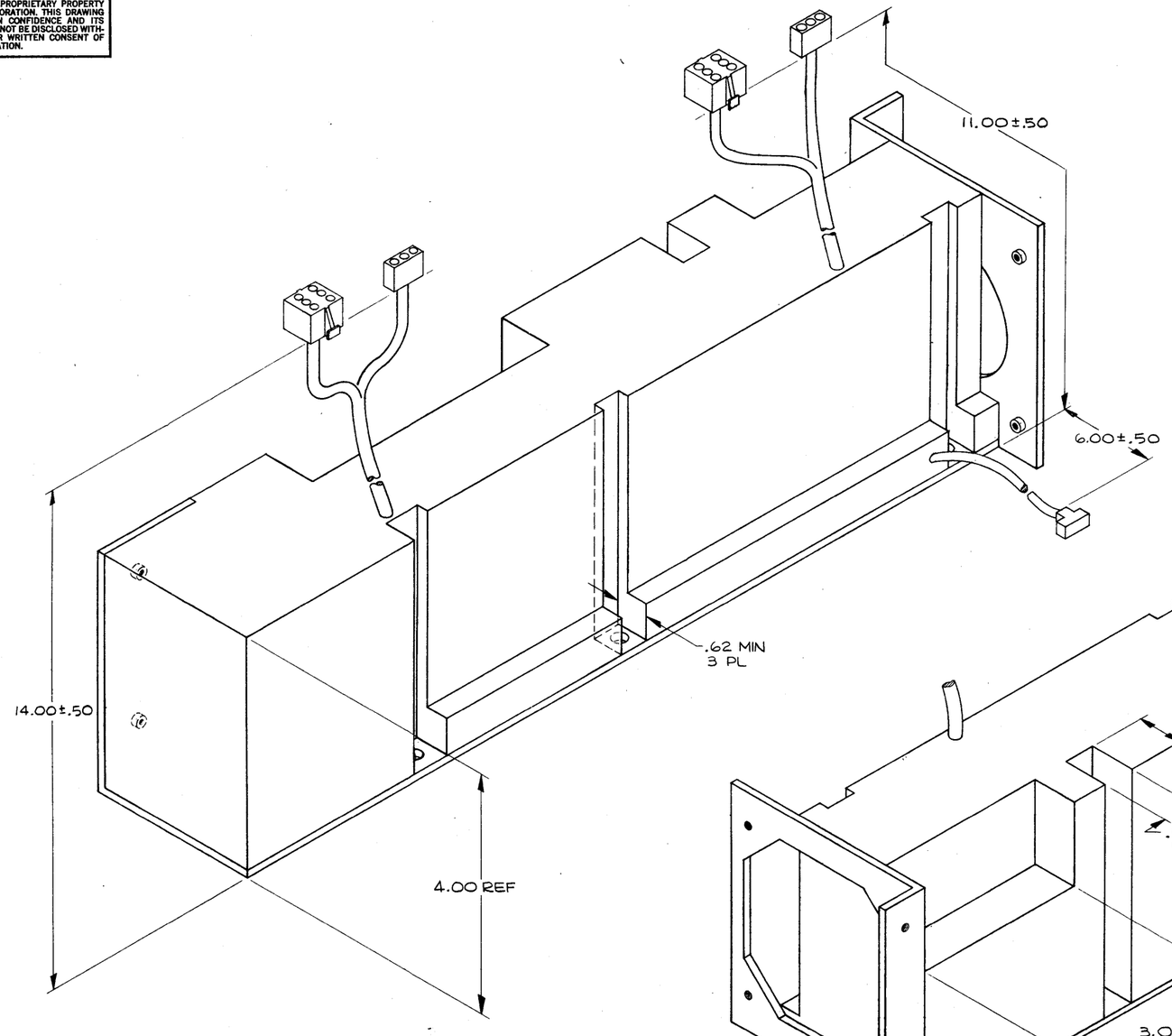


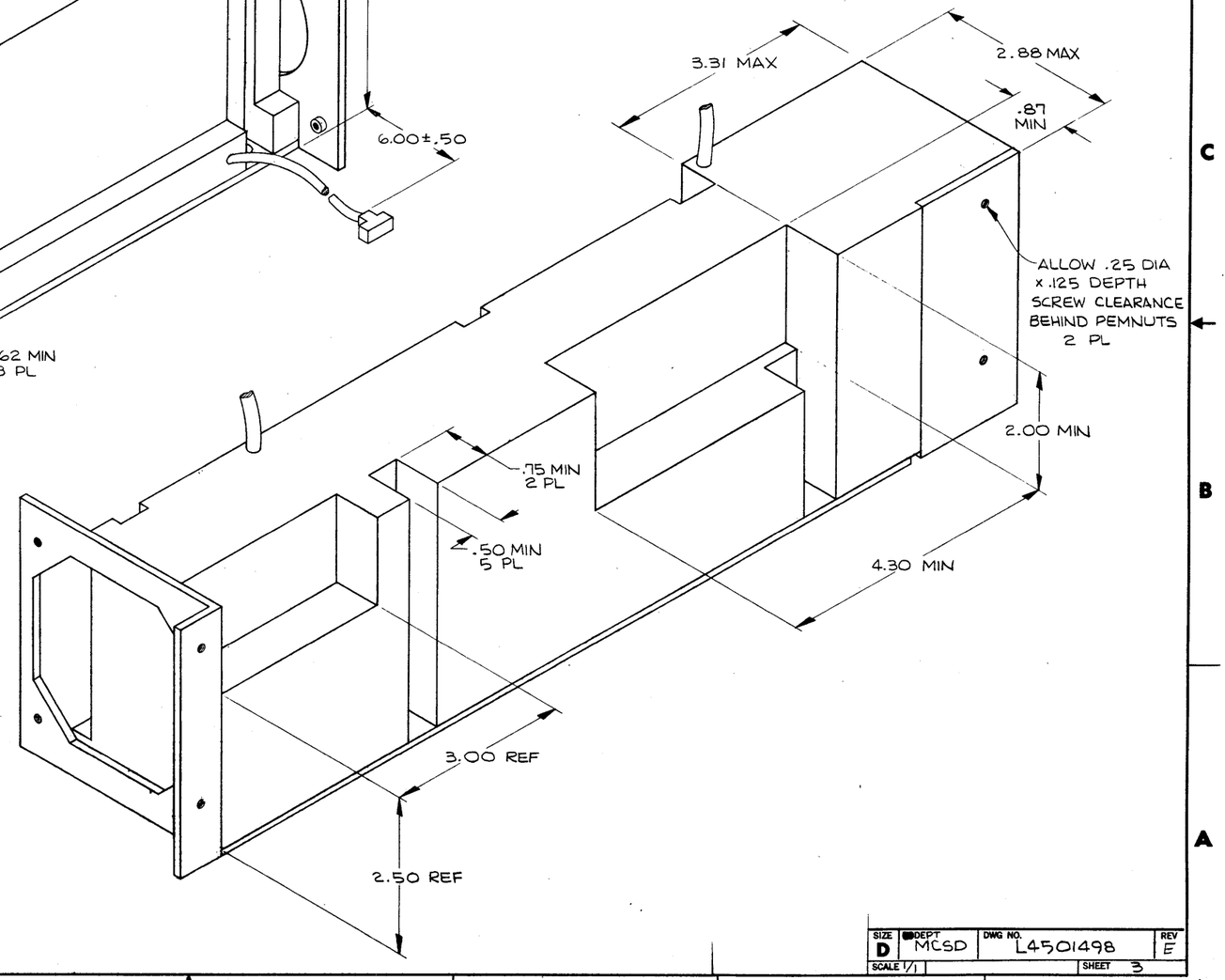




SCALE: 1/1	SIZE	DEPT	DRAWING NO.	REV
SHEET 2 OF	D	MCSD	L4501498	E

THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.

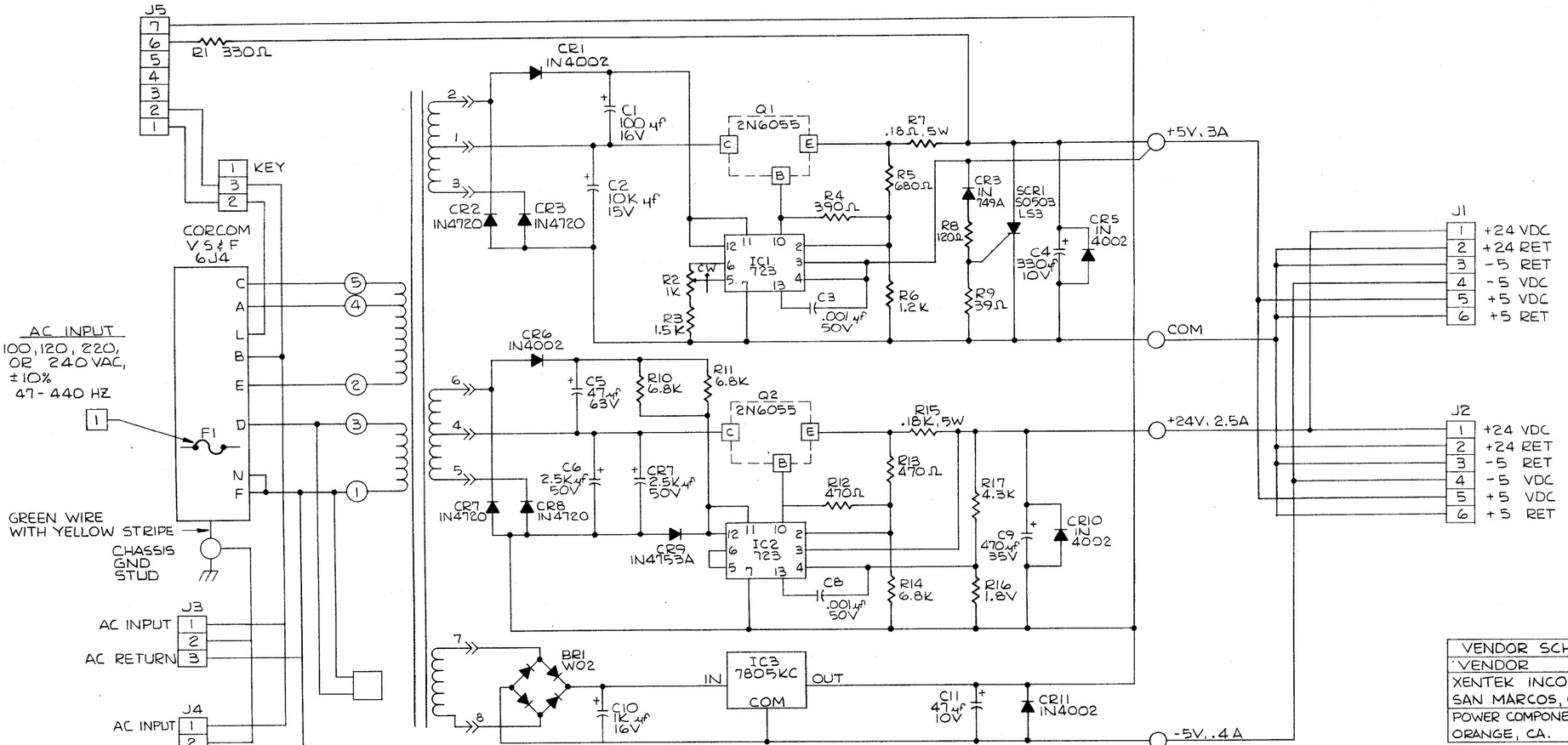




SIZE	DEPT	DWG NO.	REV
D	MCSD	L4501498	E
SCALE 1/1		SHEET 3	

9300022

THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS LOANED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.



[1] F1 IS 2A FOR 100, & 120 OPERATION
F1 IS 1A FOR 220, & 240 OPERATION

NOTES: UNLESS OTHERWISE SPECIFIED;

VENDOR SCHEMATICS	
VENDOR	SHT. NO.
XENTEK INCORP. SAN MARCOS, CA.	1
POWER COMPONENTS CO. ORANGE, CA.	2, 3, & 4

VENDORS SCHEMATIC
XENTEK INCORP.
C2910-501

intel 3065 BOWERS AVE. SANTA CLARA CALIF. 95051

TITLE: PWR. SUPPLY SCHEMATIC MDS-7XX

SIZE	DEPT	DRAWING NO.	REV
D	MCSD	L2002677	A

CODE: SHEET 1 OF 4

98-253A

THIS DRAWING AND SPECIFICATION, EITHER IS THE EXCLUSIVE PROPERTY OF MCS CORPORATION. THIS DRAWING IS SUBMITTED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF MCS CORPORATION.

J3
AC INPUT 1
CHASSIS GND 2
AC RETURN 3

J4
AC INPUT 1
CHASSIS GND 2
AC RETURN 3

B1 - FAN PLUG

VS & F *6J4
HOT
GND
GI
NEUTRAL
C
A
E
D
F
L B N J
1 2 3 4 5 6

A1
04-653-01
+24 VDC @ 2.5 AMP
3ZD7
10 E1
11 E3
+OUT
+ SENSE
- SENSE
- OUT

A2
04-653-02
-5VDC @ 0.4 AMP
3ZB6
12 E1
13 E2
+ OUT
+ SENSE
- SENSE
- OUT

A3
04-653-03
+5VDC @ 3 AMP
4ZD7
7 E1
8 E2
9 E3
+OUT
+SENSE
- SENSE
- OUT

A4
4ZB4
+OUT
-OUT

A5
J5
1 2 3 4 5 6 7
R1
6

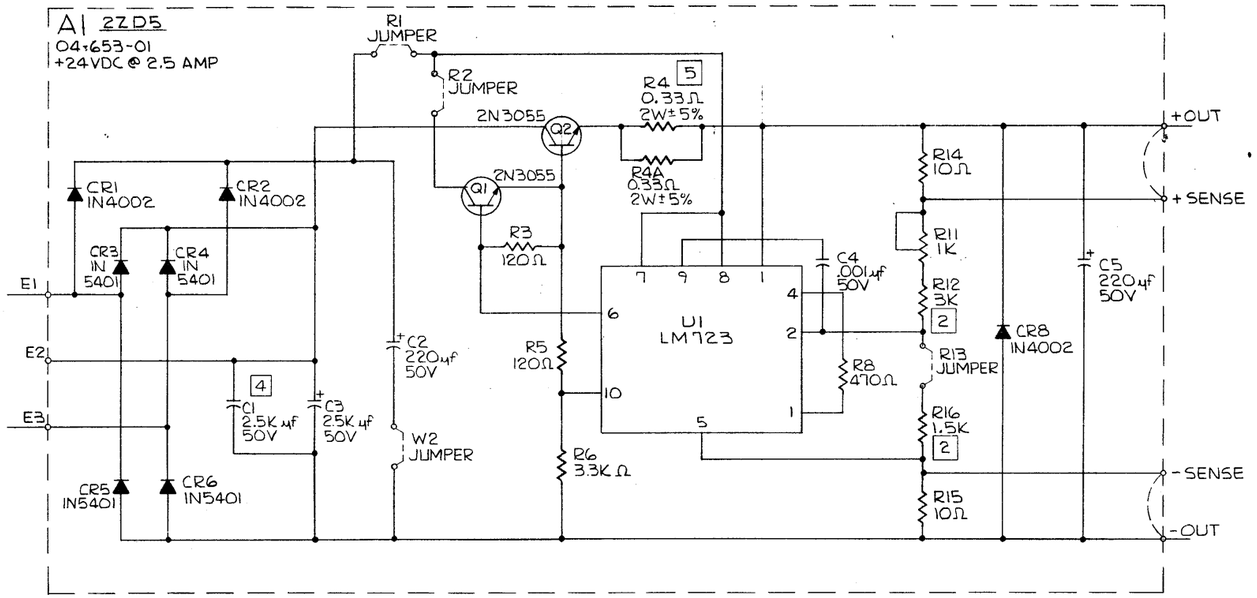
J1
1 +24 VDC
2 +24V RET
3 +5 VDC
4 -5V RET
5 +5 VDC
6 +5V RET

J2
1 +24 VDC
2 +24V RET
3 - 5 VDC
4 -5V RET
5 +5VDC
6 +5V RET

7 VALUE SELECTED IN TEST FOR OVP TO FIRE 6.2V ± 0.4 VDC.
6 RESISTOR R1 IS 330Ω 1/4W ± 5%
5 R4 & R4A ARE MOUNTED PIGGYBACK ON THE BOARD
4 CAPACITOR C1 IS MOUNTED OFF THE BOARD
3 TRANSISTOR Q2 IS MOUNTED OFF THE BOARD.
2 RESISTORS ARE IN OHMS 1/2W ± 2%
1. RESISTORS ARE IN OHMS 1/2 W ± 5%
NOTES: UNLESS OTHERWISE SPECIFIED;

VENDORS SCHEMATIC
POWER COMPONENTS CO.
04-653-00

SCALE:	SIZE	DEPT	DRAWING NO.	REV
SHEET 2 OF 4	D	MCSD	L2002677	A



VENDORS SCHEMATIC
POWER COMPONENTS
04-653-00 REV A

SCALE: —	SIZE D	DEPT MCSD	DRAWING NO. L2002677	REV A
SHEET 3 OF 4				

© Intel Corporation 1977

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITH OUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.

A3 2ZB4
04-653-03
+5VDC @ 3AMP

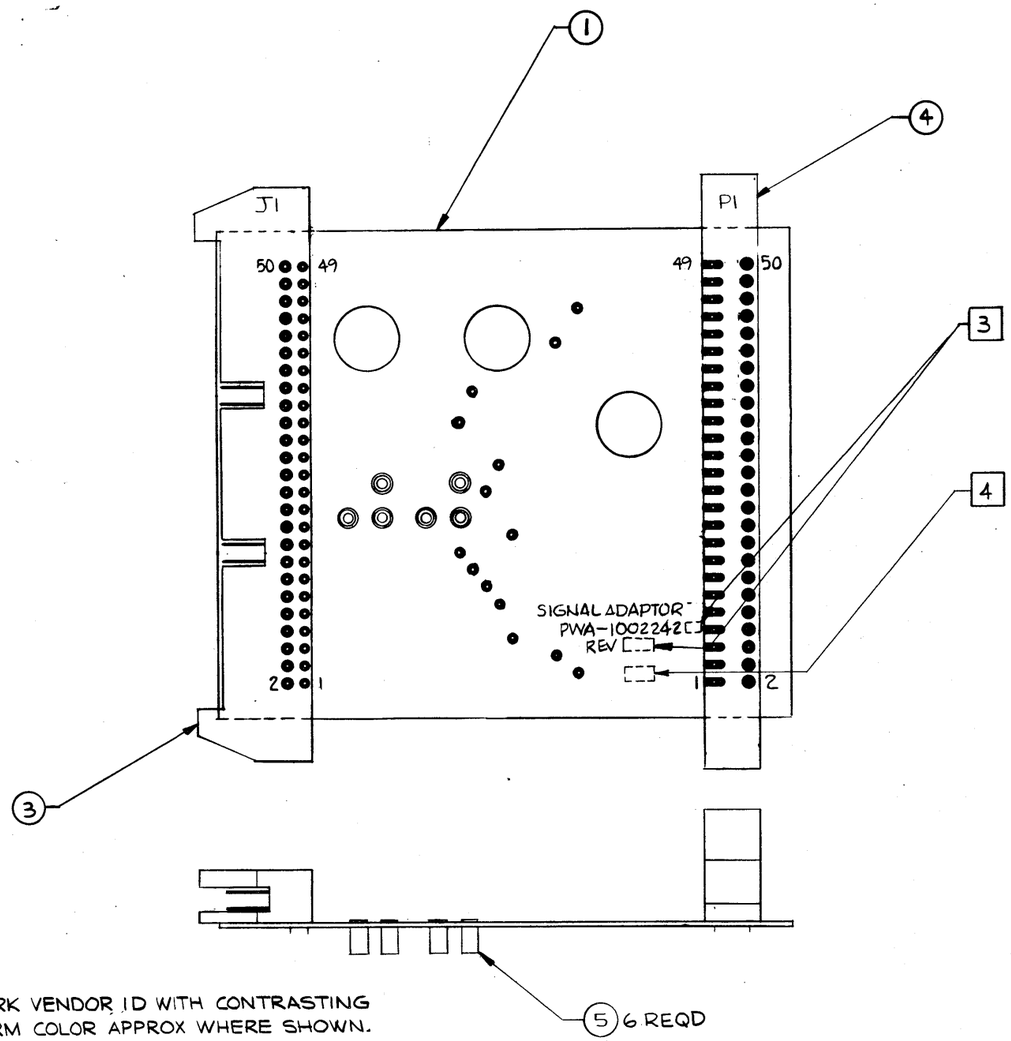
R1 JUMPER
R2 JUMPER
3 2N3055 Q2
R4 0.1Ω 2W±5%
2N3055 Q1
R3 120Ω
C4 .001μf 50V
R14 10Ω
R11 1K
R12 1.5K
2
R13 JUMPER
R16 1.5K 2
R8 5.6K 2
R9 2.4K 2
U1 LM723
R5 120Ω
R6 910K
C2 IN4002
C2 IN4002
C2 220μf 50V
C3 75K μf 15V
W2 JUMPER
CR5 IN5401
CR6 IN5401
CR8 IN4002
C5 220μf 50V
R15 10Ω
E1
E2
E3
+OUT
+ SENSE
-OUT
-SENSE

A4 2ZB4
CR1 IN4734
R1 7
SCR1 2N4441
R2 100Ω
C1 20μf 15V
+OUT
-OUT
OVP-0-5

VENDORS SCHEMATIC
POWER COMPONENTS
04-653-00

SCALE: —	SIZE D	DEPT MCSD	DRAWING NO. L2002677	REV A
SHEET 4 OF 4				

THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.



4 MARK VENDOR ID WITH CONTRASTING PERM COLOR APPROX WHERE SHOWN.

3. MARK PART NO & REV LEVEL WITH CONTRASTING PERM COLOR, .12 HIGH, APPROX WHERE SHOWN.

2. WORKMANSHIP PER MCSD QAWS 99-0007-001.

1. ASSY PART NO. IS 1002242-01. ASSY AND PL ARE TRACKING DOCUMENTS.

NOTES: UNLESS OTHERWISE SPECIFIED

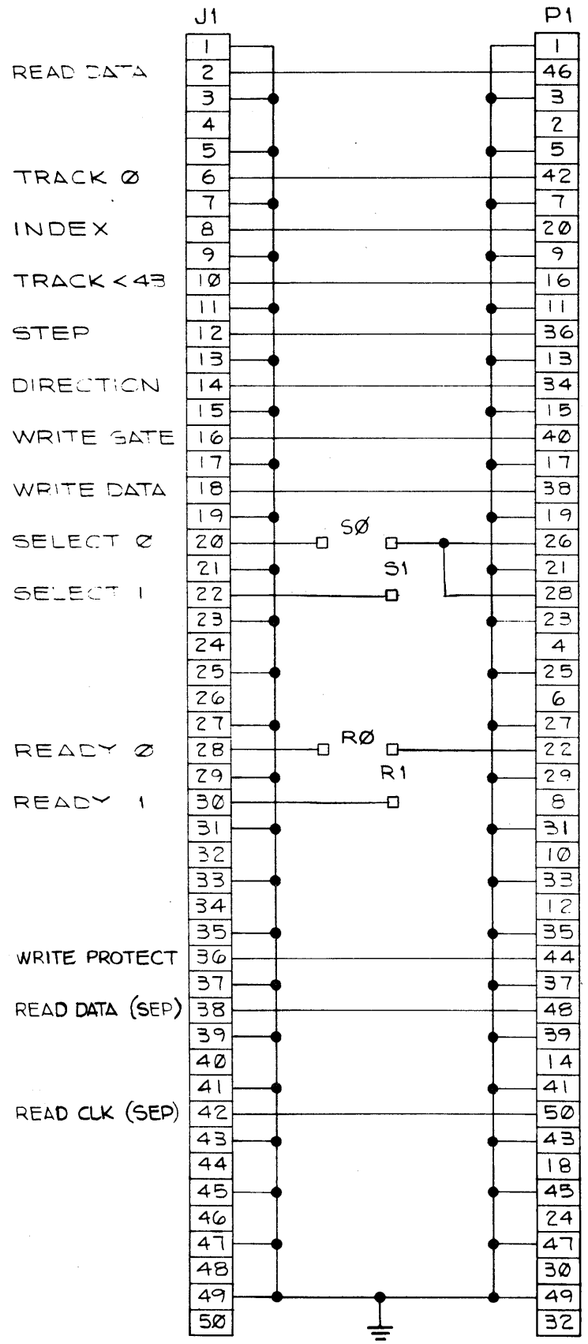
intel
3065 BOWERS AVE.
SANTA CLARA
CALIF. 95051

PRINTED WIRING ASSEMBLY
SIGNAL ADAPTOR

SIZE	DEPT	DRAWING NO	REV
C	MCSD	L1002242	A

SHEET 1 OF 1

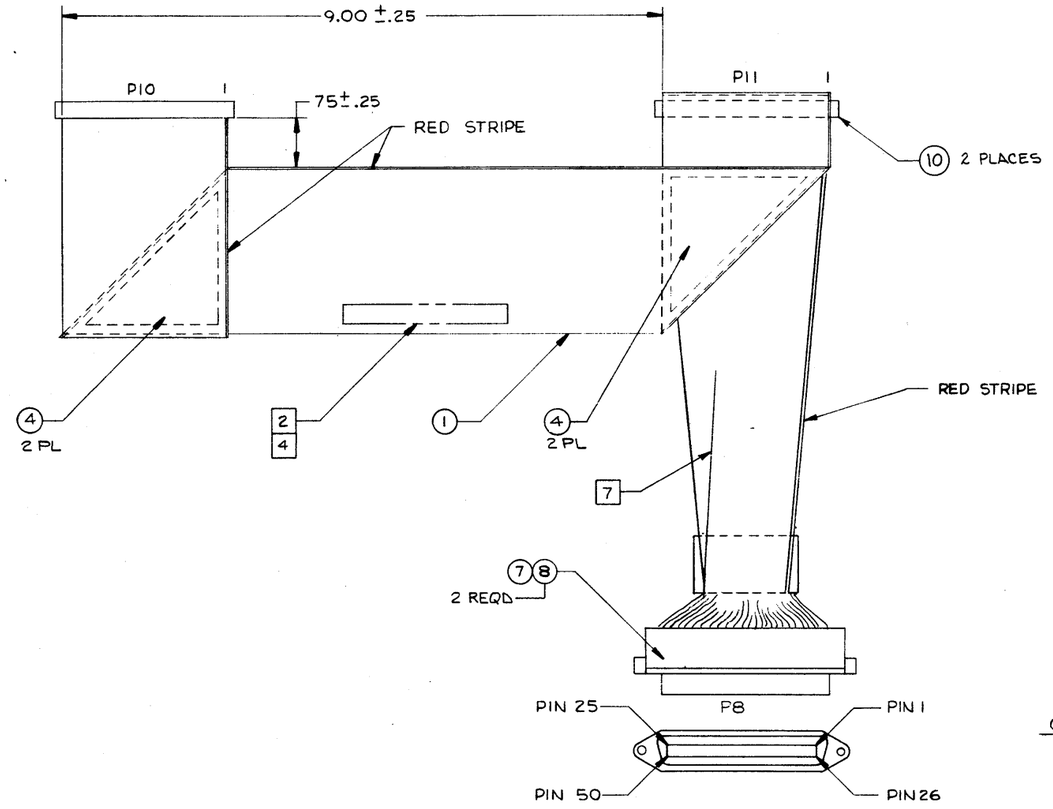
THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.

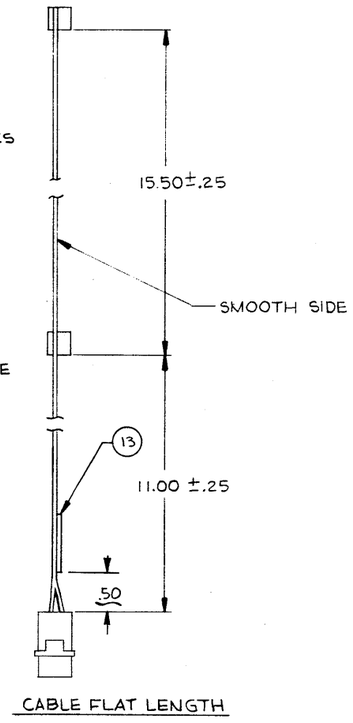


intel®	3065 BOWERS AVE. SANTA CLARA CALIF. 95051		
TITLE	SCHEMATIC SIGNAL ADAPTER		
SIZE C	CODE MCSD	DWG. NO. L2002244	REV A
SCALE NONE		SHEET 1 OF 1	

98-252A

THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.





7 SPLIT CABLE BETWEEN WIRES 25 & 26 APPROX 8" UP CABLE FROM P8 END. SEPARATE EACH WIRE AND INSTALL IN ITEM 7. USE FULL QTY OF ITEM 13 & INSTALL AS SHOWN.

6. WORKMANSHIP PER MCSD QAWS 99-0007-001.

5 REMOVED

4 MARK ASSY VENDOR ID WITH CONTRASTING PERM COLOR, .12 HIGH, APPROX WHERE SHOWN.

3. REMOVED

2 MARK ASSY PART NO. & REV LEVEL WITH CONTRASTING PERM COLOR, .12 HIGH, APPROX WHERE SHOWN.

1. PART NO. IS 4001496-01. ASSY & PL ARE TRACKING DOCUMENTS.

NOTES: UNLESS OTHERWISE SPECIFIED

SEE SEPERATE PART LIST

intel® 3065 BOWERS AVE. SANTA CLARA CALIF. 95051

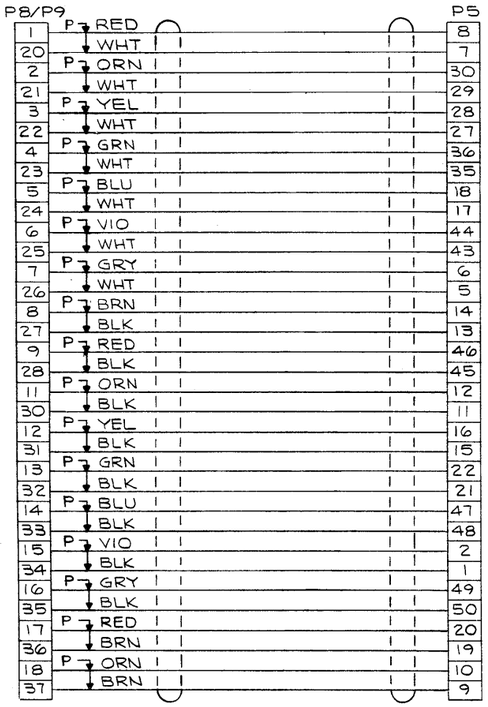
TITLE: DC SIGNAL CABLE FLOPPY DISK

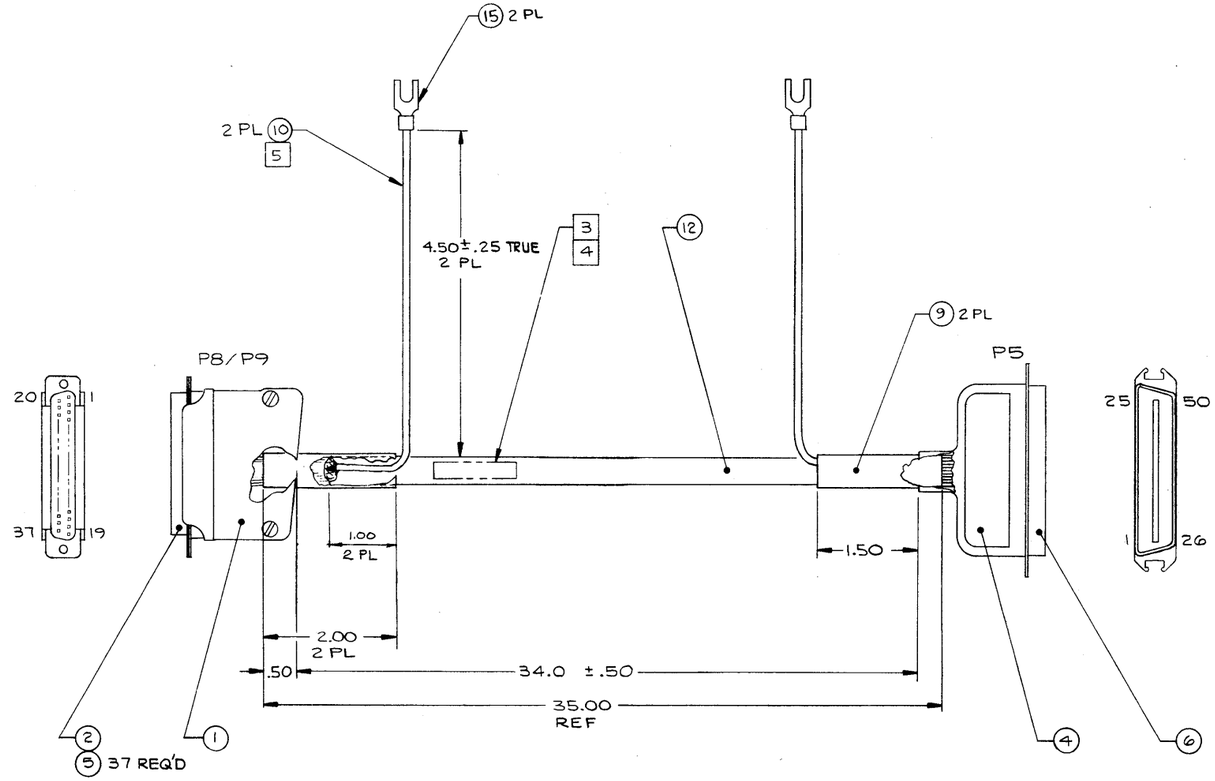
SIZE	CODE	DWG. NO.	REV
D	MCSD	L4001496	D

SCALE 1:1 SHEET 1 OF 1

9300021

THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.





5. SHIELD OF CABLE TO BE ROLLED INTO SINGLE CONDUCTOR AND SLEEVED AS SHOWN.
4. MARK VENDOR ID WITH CONTRASTING PERM COLOR, APPROX WHERE SHOWN.
3. MARK PART NO. AND REV LEVEL WITH CONTRASTING PERM COLOR, .12 HIGH, APPROX WHERE SHOWN.
2. WORKMANSHIP PER MCSD QAWS 99-0007-001.
1. ASSY PART NO. IS 4002176-01.

NOTES: UNLESS OTHERWISE SPECIFIED

intel® 3065 BOWERS AVE. SANTA CLARA CALIF. 95051

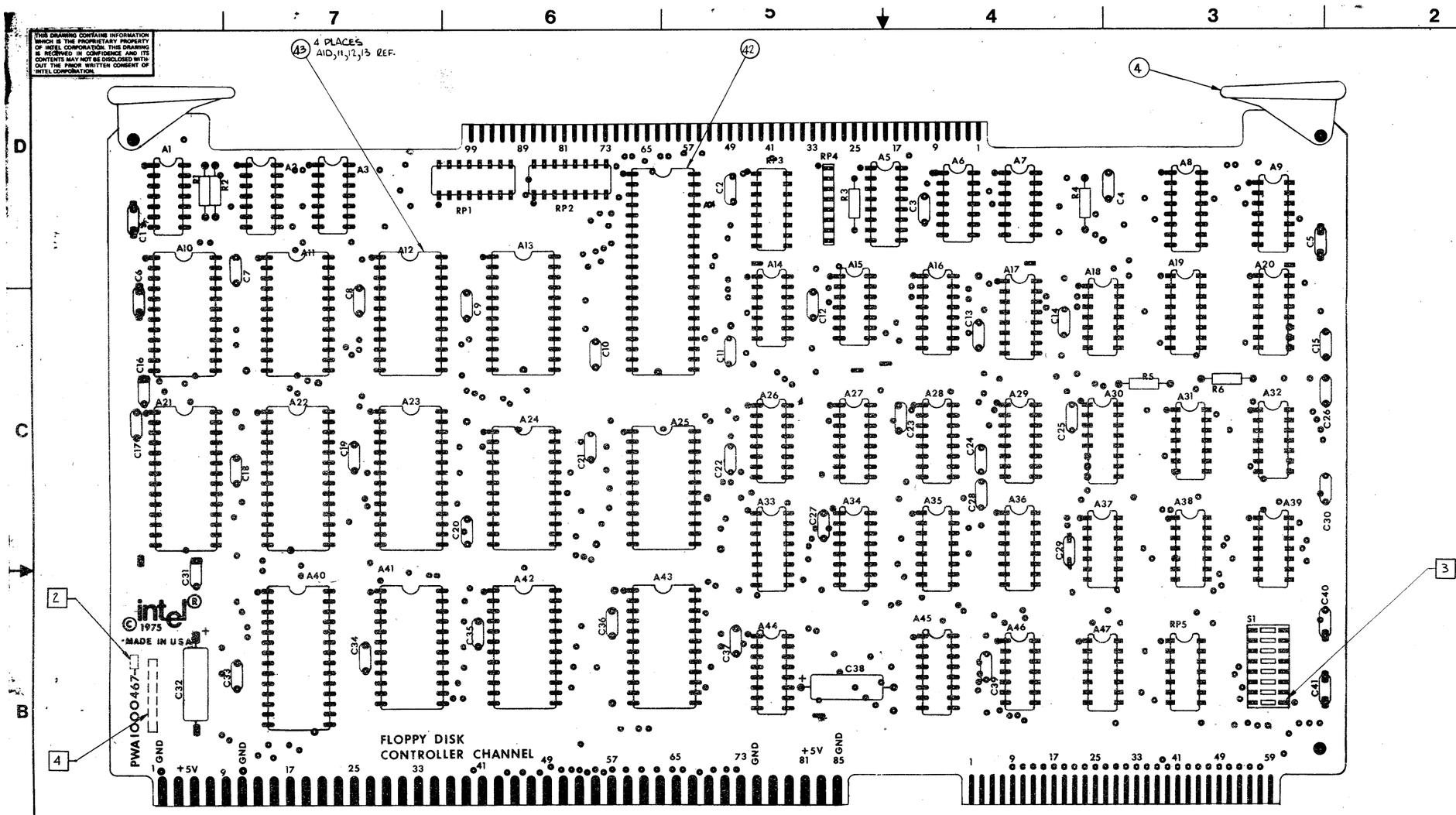
TITLE: PERIPHERAL CABLE INTERCONNECT

SIZE	CODE	DWG. NO.	REV
D	MCSD	L4002176	A

SCALE NONE | SHEET 1 OF 1

9300021

THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.



5. WORKMANSHIP PER MCSD QAWS 99—0007-001.

[4] MARK ASSY VENDOR ID WITH CONTRASTING PERM COLOR NON-CONDUCTIVE, .12 INCH HIGH, APPROX WHERE SHOWN.

[3] INSTALL SWITCH WITH SLIDE POSITION 1 TO BOTTOM OF BOARD.

[2] MARK ASSY DASH No AND REV LEVEL WITH CONTRASTING PERM COLOR, NON-CONDUCTIVE, .12 INCH HIGH APPROX WHERE SHOWN.

1. ASSY PART No IS 1000467-XX. ASSY AND PL ARE TRACKING DOCUMENTS.

NOTES UNLESS OTHERWISE SPECIFIED

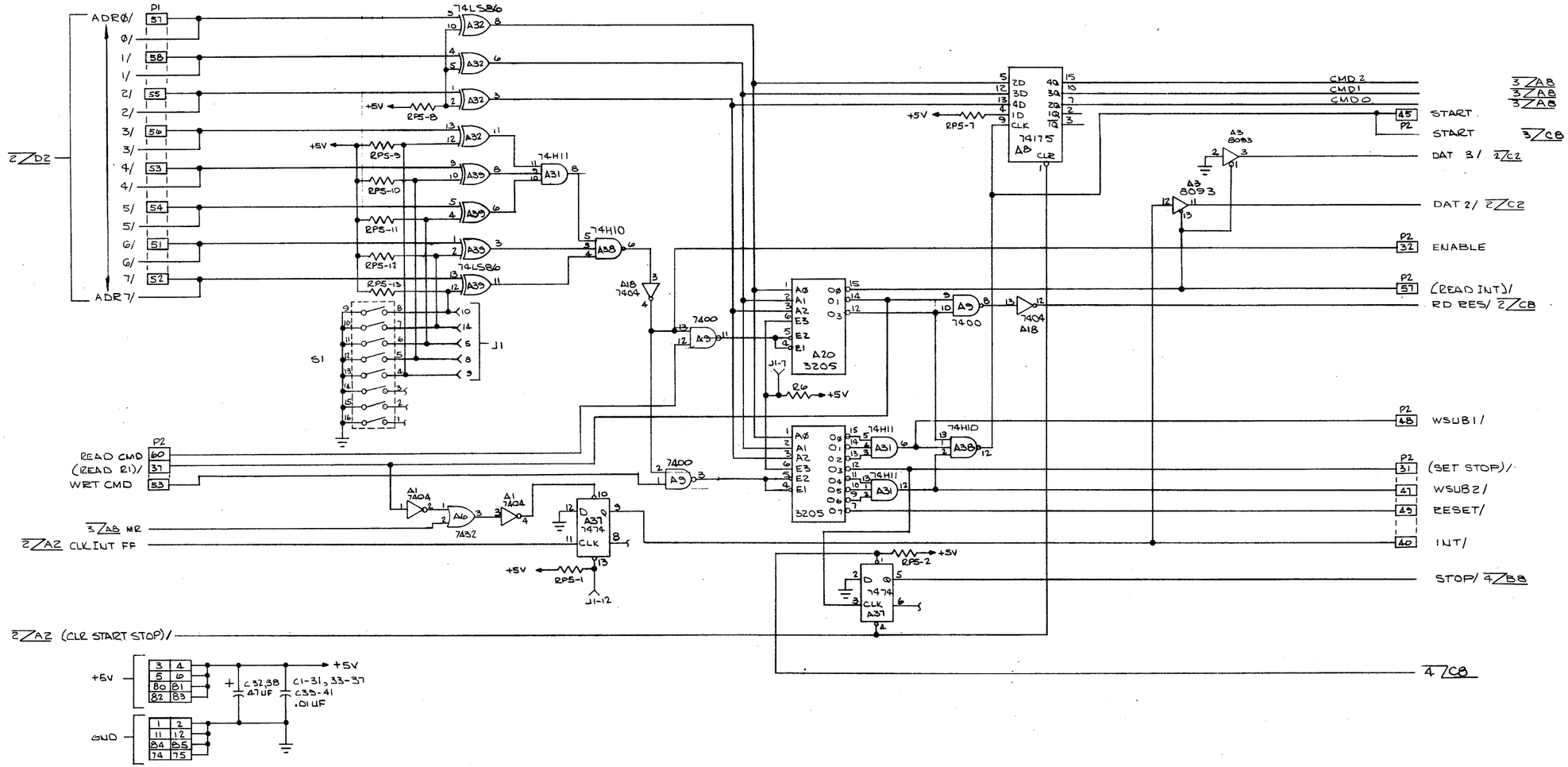
intel® 3065 BOWERS AVE. SANTA CLARA CALIF 95051

PRINTED WIRING ASSEMBLY

FLOPPY DISK CONTROLLER CHANNEL

SIZE	DEPT	DRAWING NO	REV
D	MCSD	P1000467	N

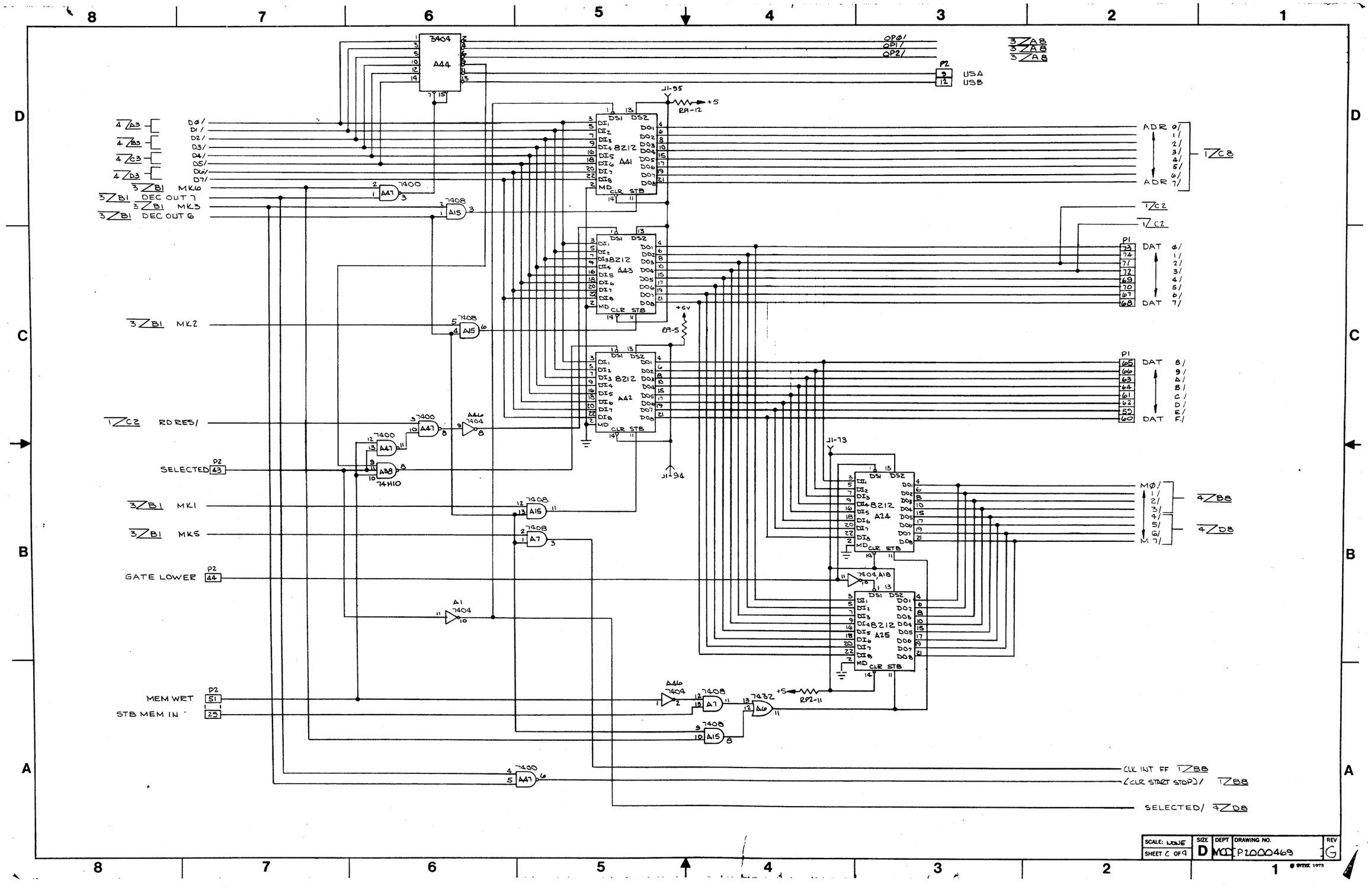
CODE | SHEET 1 OF 1



NOTES: UNLESS OTHERWISE SPECIFIED.

1. THIS DOCUMENT REFLECTS ARTWORK NO. 1000468, REV 'F'.
2. RESISTOR VALUES ARE IN OHMS 1K, ¼W, 5%.
3. CONNECTOR J1 IS USED FOR TEST POINT ONLY.

intel © INTEL 1976	3065 BOWERS AVE. SANTA CLARA CALIF. 95051		
TITLE: SCHEMATIC FLOPPY DISK CONTROLLER CHANNEL			
SIZE: D	DEPT: MCD	DRAWING NO.: P2000469	REV: G
CODE:	SHEET 1 OF 4		


3404
A44
OP0/
OP1/
OP2/
P2
USA
USB
J1-95
+5
RP-12
DS1 DS2
8212
A41
A43
A42
A24
A25
ADR 0/
ADR 7/
1ZC8
1ZC2
P1
DAT 0/
DAT 7/
DAT 8/
DAT F/
+5V
RP-5
J1-73
J1-94
M0/
M7/
4ZB8
4ZD8
7400
7408
7404
7432
74H10
A47
A15
A38
A7
A16
A18
A10
A1
4ZA3
4ZB3
4ZC3
4ZD3
3ZB1 MK10
3ZB1 DEC OUT 7
3ZB1 MK3
3ZB1 DEC OUT 6
3ZB1 MK2
1ZC2 RD RES/
SELECTED 43
3ZB1 MK1
3ZB1 MK5
GATE LOWER 44
MEM WET 51
STB MEM IN 25
RP2-11
CLK INT FF 1ZB8
/CLR START STOP)/ 1ZB8
SELECTED/ 4ZD8
SCALE: NONE
SHEET 2 OF 9
SIZE D
DEPT MCC
DRAWING NO. P2000469
REV G
© SYTEK 1975

3404 A44

OP0/ OP1/ OP2/

P2 USA USB

3 A8 3 A8 3 A8

J1-35 +5 RP-12

4 A3 D0/ D1/ D2/ D3/ D4/ D5/ D6/ D7/

4 B3 4 C3 4 D3

3 B1 MK6

3 B1 DEC OUT 7

3 B1 MK3

3 B1 DEC OUT 6

7400 A47

7408 A15

DS1 DS2 8212 A41 DI1–DI8 DO1–DO8 MD CLR STB

ADR 0/ 1/ 2/ 3/ 4/ 5/ 6/ 7/ — 1 C8

1 C2 1 C2

DS1 DS2 8212 A43

P1 72 74 71 72 69 70 67 68 DAT 0/ 1/ 2/ 3/ 4/ 5/ 6/ 7/ DAT

3 B1 MK2

7408 A15

+6V RP-5

DS1 DS2 8212 A42

P1 65 66 63 64 61 62 59 60 DAT 8/ 9/ A/ B/ C/ D/ E/ F/ DAT

1 C2 RD RES/

7400 A47

A46 7404

7400 A47

7400 A47

P2 43 SELECTED

A38 74H10

3 B1 MK1

3 B1 MK5

7408 A15

7408 A7

J1-94

J1-73

DS1 DS2 8212 A24

M0/ 1/ 2/ 3/ 4/ 5/ 6/ 7/ — 4 B8 — 4 D8

7404 A18

DS1 DS2 8212 A25

GATE LOWER P2 44

A1 7404

A46 7404

7408 A7

7432 A10

+5 RP2-11

7408 A15

P2 51 MEM WRT

25 STB MEM IN

7400 A47

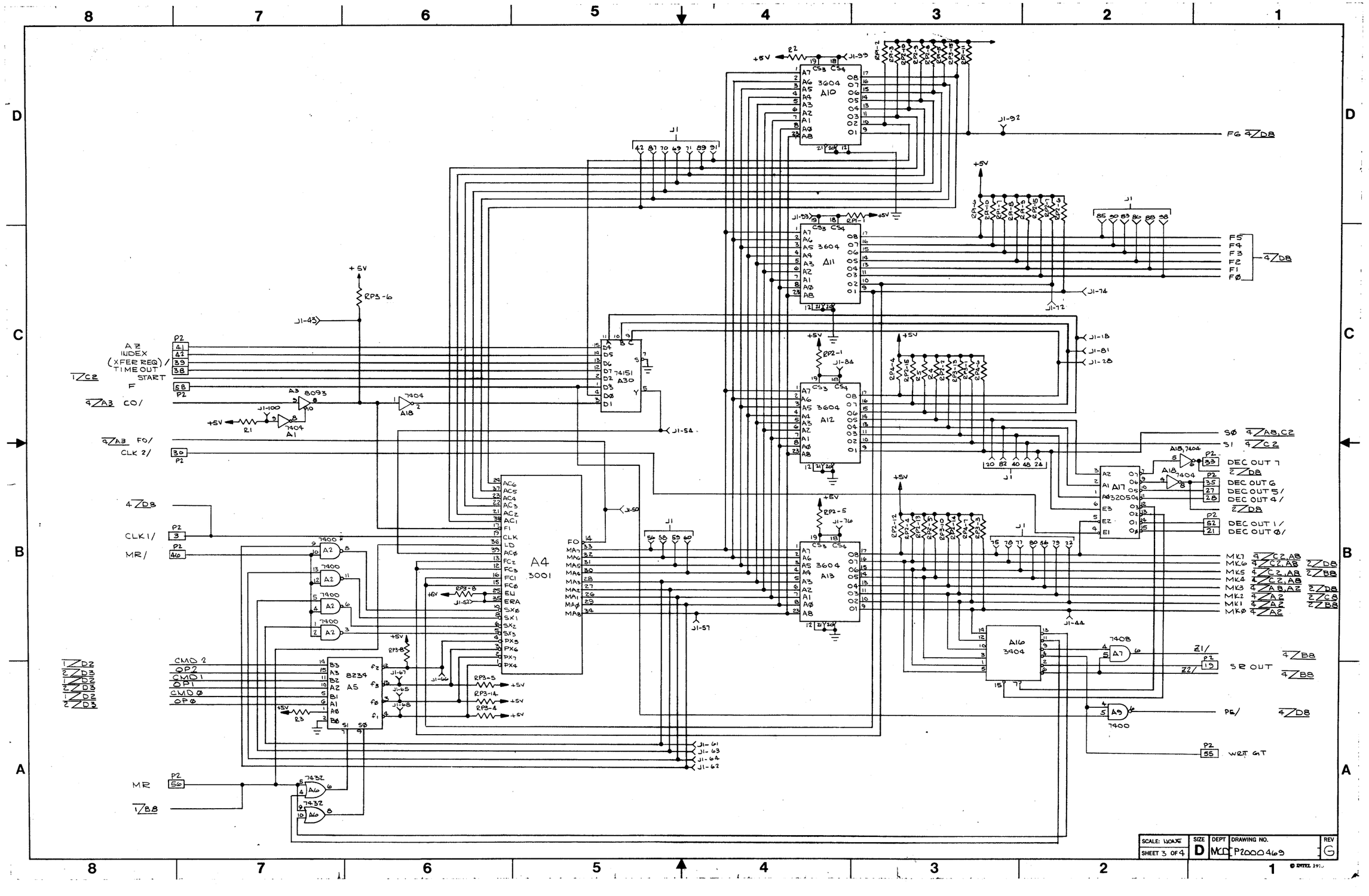
CLK INT FF 1 B8

(CLR START STOP)/ 1 B8

SELECTED/ 4 D8

SCALE: NONE	SIZE	DEPT	DRAWING NO.	REV
SHEET 2 OF 9	D	MCD	P2000469	G

© DIGITAL 1975


A10 3604
A11 3604
A12 3604
A13 3604
A4 3001
A5 8234
A30 74151
A1 7404
A18 7404
A3 8093
A16 3904
A17 32050
A7 7408
A9 7900
A2 7900
A16 7432
+5V
RP3-6
RP2-1
RP2-2
RP2-3
RP2-4
RP2-5
RP2-6
RP2-7
RP2-8
RP2-9
RP2-10
RP2-11
RP2-12
RP3-8
RP3-5
RP3-4
R1
R2
R3
J1-43
J1-54
J1-50
J1-57
J1-92
J1-93
J1-74
J1-72
J1-84
J1-18
J1-81
J1-28
J1-76
J1-44
J1-67
J1-65
J1-68
J1-66
J1-61
J1-63
J1-64
J1-62
FG 4/D8
F5 F4 F3 F2 F1 F0
4/D8
S0 4/A8,C2
S1 4/C2
DEC OUT 7
2/D8
DEC OUT 6
DEC OUT 5/
DEC OUT 4/
2/D8
DEC OUT 1/
DEC OUT 0/
MK7 4/C2,A8
MK6 4/C2,A8
MK5 4/C2,A8
MK4 4/C2,A8
MK3 4/A8,A2
MK2 4/A2
MK1 4/A2
MK0 4/A2
2/D8
2/B8
2/C8
2/B8
Z1/
Z2/
SR OUT
4/B8
4/B8
PE/
4/D8
WRT GT
A7 INDEX
(XFER REQ)/
TIME OUT
START
1/C2
F
4/A3 CO/
4/A3 F0/
CLK 2/
4/D8
CLK 1/
MR/
MR
1/B8
CMD 2
OP2
CMD 1
OP1
CMD 0
OP0
1/D2
2/D3
1/D2
2/D3
1/D2
2/D3
FO
MA7
MA6
MA5
MA4
MA3
MA2
MA1
MA0
MA8
AC6
AC5
AC4
AC3
AC2
AC1
FC2
FC3
FC1
FC0
EU
ERA
SX0
SX1
SX2
SX3
PX5
PX6
PX7
PX4
CLK
LD
AC0
P2
J1
SCALE: NONE
SHEET 3 OF 4
SIZE D
DEPT MCD
DRAWING NO. P2000469
REV G

8 7 6 5 4 3 2 1

M7/ M6/ M5/ M4/ — 2/B2
F6 F5 F4 F3 F2 F1 FØ — 3/D1, 3/C1
CLK I/ SELECTED/ — 3/BB, 2/A2
SR DATA IN/ DATA SR STB — P2 22 24
PE/ — 3/A1
ID Ø/ ID 1/ SR CLK IN/ CLK SR STB — P2 26 23 6 8
1/B1
SR DATAOUT — P2 25
Z1/ Z2/ — 3/A1, 3/A1
SR CLK OUT — P2 10
M3/ M2/ M1/ MØ/ — 2/B2
DOR/ (DSK WRT PROT)/ (WRT ERR)/ (SEL DR URDY)/ DR Ø/ DR 1/ STOP/ (TRACK 00)/ — P2 16 14 18 20 15 17 11
MK7, MK2, MK3, MK6, MK5 — 4/C2, 3/B1 / 3/B1

9300 A36 — 9300 A34 — 9300 A29 — 9300 A27

A35 8233 — 8234 A28 — 8234 A45

RP5-3 1K, RP5-4 1K, RP5-10 1K, RP5-5 1K — +5V

7408 A7 — 7400 A14 ×4

A21 3002 — A40 3002 — A22 3002 — A23 3002

ADRF/ ADRE/ — 44 43
D7/ D6/ — 2/D8, 2/D8
ADRD/ ADRC/ — 46 45
D5/ D4/ — 2/D8, 2/D8
ADRB/ ADRA/ — 48 47
D3/ D2/ — 2/D8, 2/D8
ADR9/ ADR8/ — 50 49
D1/ DØ/ — 2/D8, 2/D8
CO/ — 3/C8
FO/ — 3/BB

RP3-3, RP4-3 — +5
RP3-12 — +5V
MK4 MK5 MK6 MK7 — 3/B1 — P2 2 54 36
A33 8234 — J1-30, J1-34, J1-32, J1-26
RP4-5, RP4-2 — +5
RP3-13, RP4-14 — +5
MKØ MK1 MK2 MK3 — 3/B1 — P2 13 4 50 34
A26 8234 — J1-36, J1-37, J1-46, J1-38
3/C1 S1, 3/B1 SØ
RP3-11 — +5
RP3-2 — +5

SCALE: NONE	SIZE	DEPT	DRAWING NO.	REV
SHEET 4 OF 4	D	MCD	P2000469	G

© DYNEX 1975

INTEL CORPORATION, 3065 Bowers Avenue, Santa Clara, California 95051 • (408) 987-8080

Printed in U.S.A. NCG