User's Manual

Rotator

User's Manual

Multimedia Processor for Mobile Applications
EMMA Mobile ™ EV2

Renesas Electronics
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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the EMMA Mobile EV2. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Data Sheet	Hardware overview and electrical characteristics	EMMA Mobile EV2 Datasheet	R19DS0010EJxxxx
User's manual (1chip)	Hardware whole specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description	EMMA Mobile EV2 User's manual 1chip	R19UH0036EJxxxx
User's manual (module)	Hardware each macro specifications and operation description.	EMMA Mobile EV2 User's manual each module	See below

Document Name	Document No.	Document Name	Document No.
1chip	R19UH0036EJxxxx	DMA Controller	R19UH0043EJxxxx
System Management Unit	R19UH0037EJxxxx	LP-DDR/DDR2 Controller	R19UH0039EJxxxx
Timer	R19UH0054EJxxxx	SD Memory Card Interface	R19UH0061EJxxxx
System Timer	R19UH0055EJxxxx	SDIO Interface	R19UH0042EJxxxx
HD Video Decoder	R19UH0056EJxxxx	CF Card Interface	R19UH0062EJxxxx
Rotator (This manual)	R19UH0057EJxxxx	Unified Serial Interface	R19UH0047EJxxxx
Resizer	R19UH0058EJxxxx	UART interface	R19UH0040EJxxxx
Image Composer	R19UH0038EJxxxx	USB 2.0 Host Controller	R19UH0045EJxxxx
LCD Interface	R19UH0044EJxxxx	USB 2.0 Function Controller	R19UH0034EJxxxx
ITU-R BT.656 Interface	R19UH0059EJxxxx	IIC Interface	R19UH0052EJxxxx
Digital Terrestrial TV Interface	R19UH0048EJxxxx	General Purpose I/O Interface	R19UH0041EJxxxx
Camera Interface	R19UH0060EJxxxx	Pulse Width Modulation Interface	R19UH0063EJxxxx

4 digits of end shows the version.

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names

Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.

Examples the PM03 bit in the PM0 register

P3_5 pin, VCC pin

(2) Notation of Numbers

The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.

Examples Binary: 11b or 11

Hexadecimal: EFA0h

Decimal: 1234

3. Register Notation

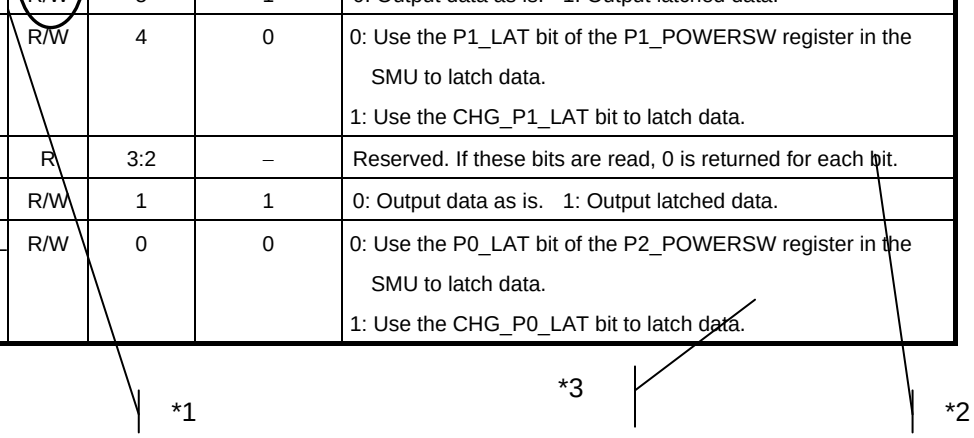
The symbols and terms used in register diagrams are described below.

x.x.x XXX register

This register (XXXXXXX: xxxx_xxxxh) …..

7	6	5	4	3	2	1	0
Reserved		CHG_P1_LAT	LATCH_P1_SEL	Reserved		CHG_P0_LAT	CHG_P0_LAT_SEL

Name	R/W	Bit No.	After Reset	Description
LATCH_P2_SEL	R/W	8	0	0: Use the P2_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P2_LAT bit to latch data.
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P1_LAT	R/W	5	1	0: Output data as is. 1: Output latched data.
LATCH_P1_SEL	R/W	4	0	0: Use the P1_LAT bit of the P1_POWERSW register in the SMU to latch data. 1: Use the CHG_P1_LAT bit to latch data.
Reserved	R	3:2	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P0_LAT	R/W	1	1	0: Output data as is. 1: Output latched data.
CHG_P0_LAT_SEL	R/W	0	0	0: Use the P0_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P0_LAT bit to latch data.



*1

R/W: Read and Write.

R: Read only.

W: Write only.

-: Nothing is assigned.

*2

Reserved bit.

Reserved bit. Set to specified value.

*3

・ Nothing is assigned.

Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.

・ Do not set to a value.

Operation is not guaranteed when a value is set.

・ Function varies according to the operating mode.

The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

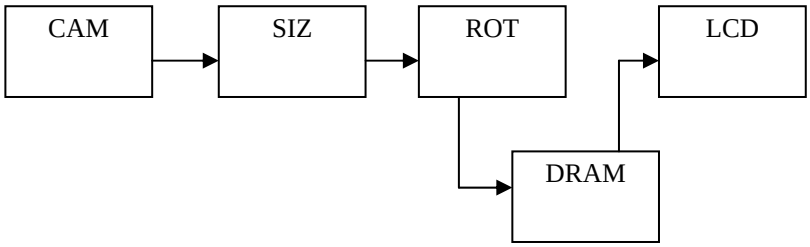
Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Register
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

Table of Contents

1. Overview

The rotator (ROT) is a module used to rotate an image and data can be input directly from components such as the CAM and CPU.
The ROT module has two modes: raster order mode and random mode.
In raster order mode, there are no input address restrictions, but the pixels must be input in raster order.
In random mode, the pixels can be input in any order, but the input line addresses must be aligned with 2^*n*.

Figure 1-1. ROT Data Flow



1.1 Features

(1) Raster order mode

- Rotation: 0°, 90°, 180°, 270°
- Formats: ARGB8888, RGB888/YUV444, RGB565
- Byte lane swapping on the output side

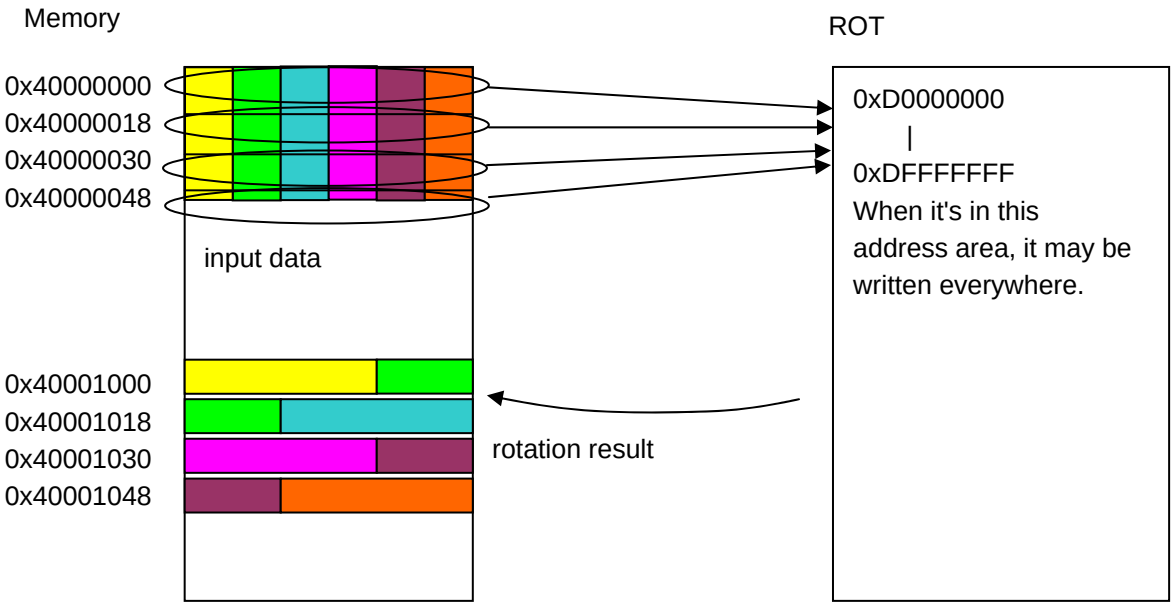
(2) Random mode

- Rotation: 0°, 90°, 180°, 270°
- Rotation in the X or Y direction
- Formats: RGB565, YUV422 (interleaved, semi-planar, and planar), YUV420 (semi-planar and planar)
- Byte lane swapping on the output side

Note

With Raster order mode

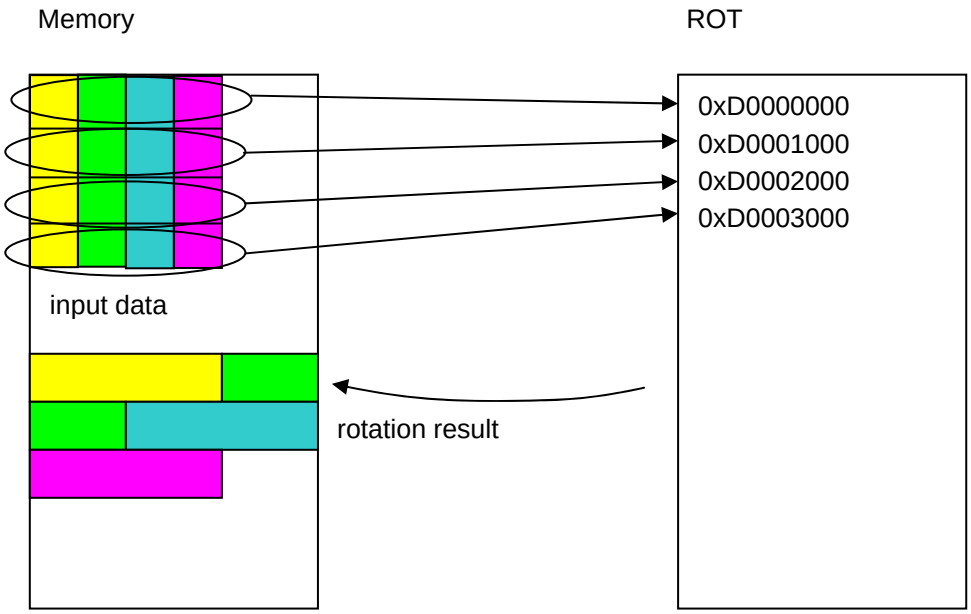
It's the mode to write in the data which continued in the address reach of ROT (from 0xD0000000, 0xDFFFFFFF).
A DSTADDRV register is set in bit[3:0]=0xF to make it Raster Order mode.



The example which is as a result of the revolution the time 90 deg. Output data of ROT is stocked continuously on the memory.

With Random order mode

It's the mode to write in data by the linear unit in the address reach every color of ROT.
The writing in address to ROT is decided according to the setting of bit [5:4] BOUNDARY of a MODE register in the linear unit of the input data. The writing in address to ROT on a figure is the value of the setting of BOUNDARY=00b.

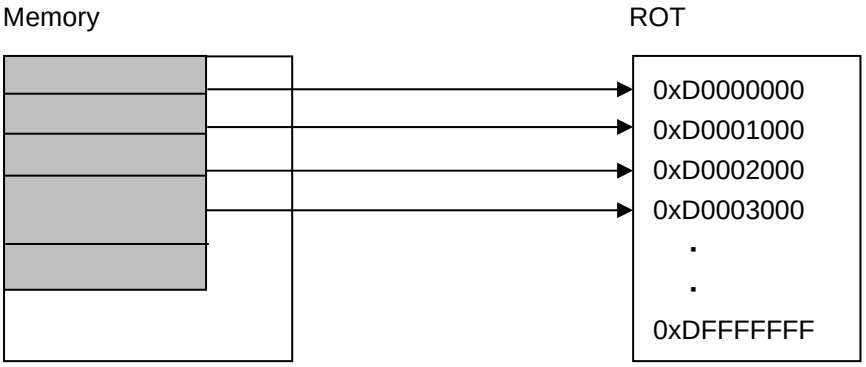


The example which is as a result of the revolution the time 90 deg. Output data of ROT is stocked continuously on the memory.

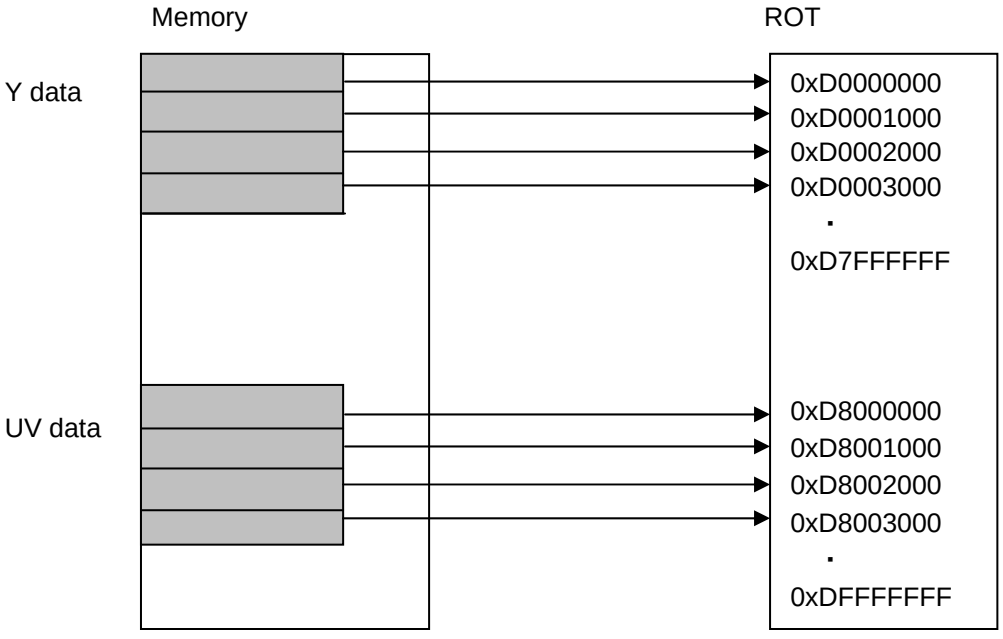
An example of the writing in address to ROT. (BOUNDARY setting)

BOUNDARY=00b	BOUNDARY=01b	BOUNDARY=10b	BOUNDARY=11b
0xD0000000	0xD0000000	0xD0000000	0xD0000000
0xD0001000	0xD0002000	0xD0004000	0xD0008000
0xD0002000	0xD0004000	0xD0008000	0xD0010000
0xD0003000	0xD0006000	0xD000C000	0xD0018000
.	.	.	.
.	.	.	.

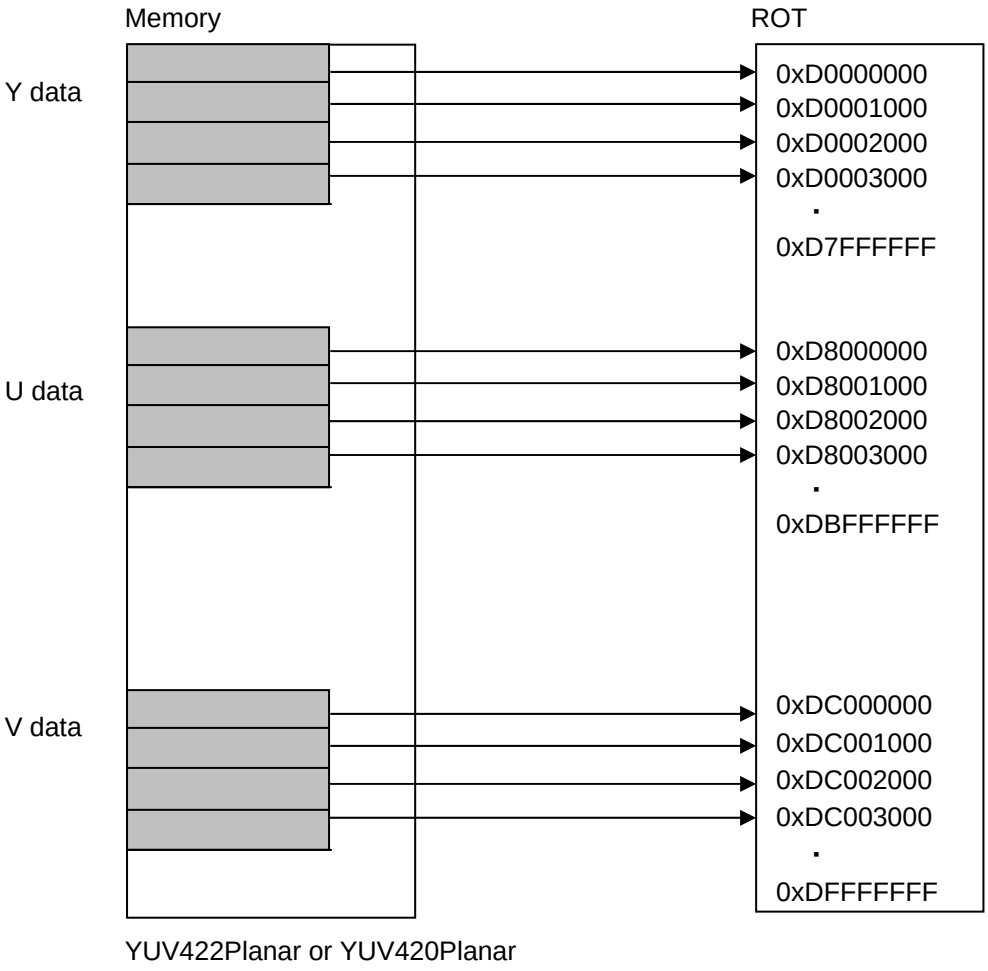
The writing in address to ROT every each color of the input data format. (BOUNDARY=00b setting)



RGB565 or YUV422Interleave



YUV422SemiPlanar or YUV420SemiPlanar


Memory
ROT
Y data
U data
V data
0xD0000000
0xD0001000
0xD0002000
0xD0003000
0xD7FFFFFF
0xD8000000
0xD8001000
0xD8002000
0xD8003000
0xDBFFFFFF
0xDC000000
0xDC001000
0xDC002000
0xDC003000
0xDFFFFFFF
YUV422Planar or YUV420Planar

1.2 Restrictions

1.2.1 Input interface (slave interface)

Writing in bytes or half words is not supported.

1.2.2 Input address for source images

In raster order mode: D000_0000H to DFFF_FFFFH
In random mode:

RGB565, YUV422 interleaved:		D000_0000H to DFFF_FFFFH
YUV422/420 semi-planar:	Y:	D000_0000H to D7FF_FFFFH
	UV:	D800_0000H to DFFF_FFFFH
YUV422/420 planar:	Y:	D000_0000H to D7FF_FFFFH
	U:	D800_0000H to DBFF_FFFFH
	V:	DC00_0000H to DFFF_FFFFH

The horizontal size of input (source) images specified for registers such as IMC_WB_HOFFSET and CAM_LINESIZE_*x* must be 2^*n* bytes.

Bits 5 and 4 of the MODE_CH*x* register = 0: Horizontal size = 2^12 (y = [25:12], x = [11:0]) (default)
Bits 5 and 4 of the MODE_CH*x* register = 1: Horizontal size = 2^13 (y = [26:13], x = [12:0])
Bits 5 and 4 of the MODE_CH*x* register = 2: Horizontal size = 2^14 (y = [27:14], x = [13:0])
Bits 5 and 4 of the MODE_CH*x* register = 3: Horizontal size = 2^15 (y = [27:15], x = [14:0])

In the YUV422/420 planar mode, the U and V components are calculated using 1/2 the horizontal size. (This is also true for the IMC and SIZ modules.)

1.2.3 Input (source) and output (destination) addresses

4byte alignment (8byte alignment is recommended for better performance.)

1.2.4 Input (source) and output (destination) pixel boundaries

RGB565	2 × 1 pixels
YUV422 interleaved	2 × 2 pixels
YUV422/420 semi-planar	4 × 2 pixels
YUV422/420 planar	8 × 2 pixels

2. Registers

The ROT registers can only be accessed in 32-bit units.
Do not write any value other than 0 to reserved bits in each register.

2.1 Register List

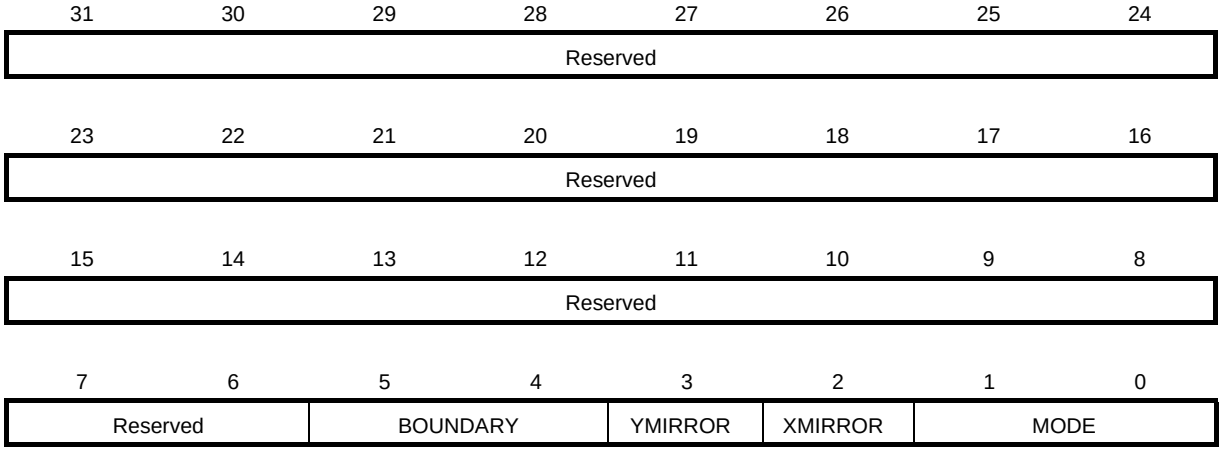
Base address: E122_0000H

Address	Register Name	Symbol	R/W	After Reset
0000H	Rotation setting register (CH0)	MODE_CH0	R/W	0000_0000H
0004H	Horizontal source image size setting register (CH0)	SRCHSIZE_CH0	R/W	0000_0000H
0008H	Vertical source image size setting register (CH0)	SRCVSIZE_CH0	R/W	0000_0000H
000CH	Source format setting register (CH0)	SRCFMT_CH0	R/W	0000_0000H
0010H	Destination address (YRGB) setting register (CH0)	DSTADRYRGB_CH0	R/W	0000_0000H
0014H	Destination address (UV) setting register (CH0)	DSTADRUV_CH0	R/W	0000_0000H
0018H	Destination address (V) setting register (CH0)	DSTADRV_CH0	R/W	0000_0000H
001CH	Destination image byte lane setting register (CH0)	DSTBL_CH0	R/W	0000_00E4H
0020H	Rotation setting register (CH1)	MODE_CH1	R/W	0000_0000H
0024H	Horizontal source image size setting register (CH1)	SRCHSIZE_CH1	R/W	0000_0000H
0028H	Vertical source image size setting register (CH1)	SRCVSIZE_CH1	R/W	0000_0000H
002CH	Source format setting register (CH1)	SRCFMT_CH1	R/W	0000_0000H
0030H	Destination address (YRGB) setting register (CH1)	DSTADRYRGB_CH1	R/W	0000_0000H
0034H	Destination address (UV) setting register (CH1)	DSTADRUV_CH1	R/W	0000_0000H
0038H	Destination address (V) setting register (CH1)	DSTADRUV_CH1	R/W	0000_0000H
003CH	Destination image byte lane setting register (CH1)	DSTBL_CH1	R/W	0000_00E4H
0040H	Histogram control register	HISTCTRL	R/W	–
0044H	Histogram value clear register	HISTCLR	R/W	0000_0000H
0048H	Histogram value count register 0	HIST0	R	0000_0000H
004CH	Histogram value count register 1	HIST1	R	0000_0000H
0050H	Histogram value count register 2	HIST2	R	0000_0000H
0054H	Histogram value count register 3	HIST3	R	0000_0000H
0058H	Histogram value count register 4	HIST4	R	0000_0000H
005CH	Histogram value count register 5	HIST5	R	0000_0000H
0060H	Histogram value count register 6	HIST6	R	0000_0000H
0064H	Histogram value count register 7	HIST7	R	0000_0000H
0068H to FFFCH	Reserved	–	–	–

2.2 Register Details

2.2.1 Rotation setting registers

These registers (MODE_CH0: 0000H, MODE_CH1: 0020H) set up rotation. Flipping in the X or Y direction is executed followed by rotating to output an image.

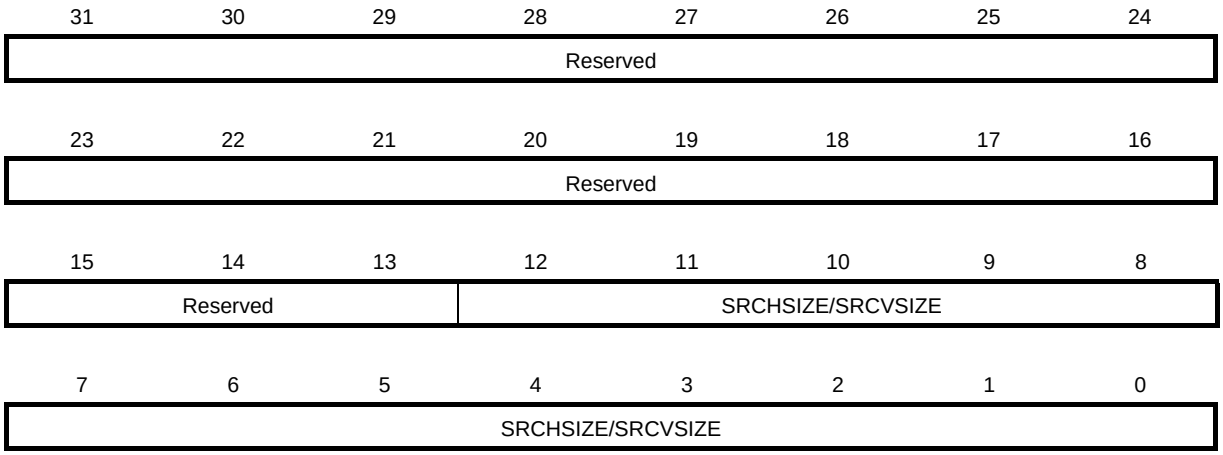


Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:6	000_0000H	Reserved. If these bits are read, 0 is returned for each bit.
BOUNDARY	R/W	5:4	0H	Specify the horizontal size of input (source) images so as to satisfy 2^*n* bytes. 0: 2^12 (y = [25:12], x = [11:0]) 1: 2^13 (y = [26:13], x = [12:0]) 2: 2^14 (y = [27:14], x = [13:0]) 3: 2^15 (y = [27:15], x = [14:0])
YMIRROR	R/W	3	0	Specify whether to mirror images in the Y direction. 0: Without mirror 1: Mirror Set a raster mode as 0.
XMIRROR	R/W	2	0	Specify whether to mirror images in the X direction. 0: Without mirror 1: Mirror Set a raster mode as 0.
MODE	R/W	1:0	00b	Specify the rotation direction. 00: Do not rotate 01: 90° 10: 180° 11: 270°

2.2.2 Horizontal source image size setting registers and vertical source image size setting registers

SRCHSIZE_CH0: 0004H
SRCVSIZE_CH0: 0008H
SRCHSIZE_CH1: 0024H
SRCVSIZE_CH1: 0028H

These registers specify the number of pixels in a source image.

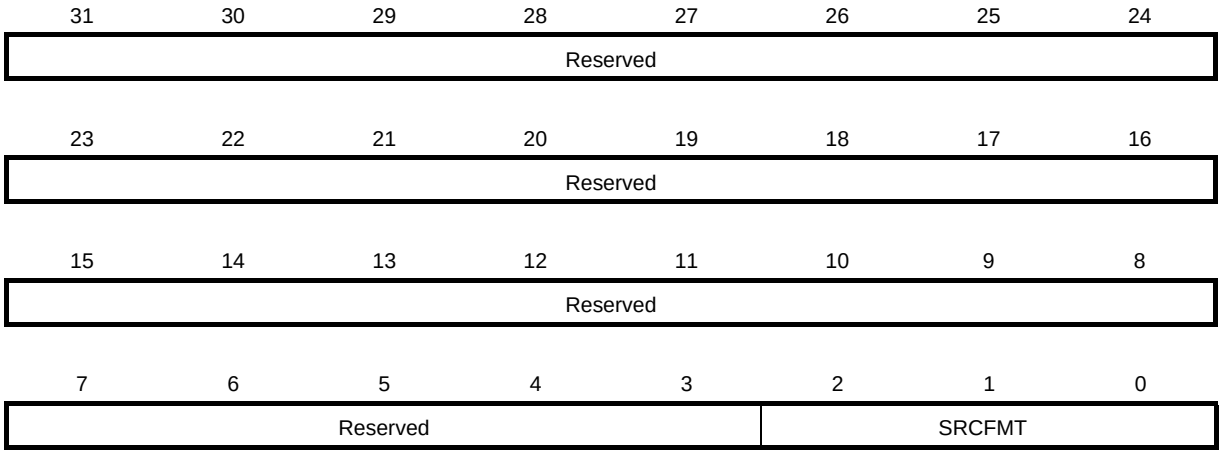


Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:13	0_0000H	Reserved. If these bits are read, 0 is returned for each bit.
SRCHSIZE	R/W	12:0	0000H	Specify the number of pixels in the horizontal direction for images. Specifiable range: 2 to 8,190 pixels

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:13	0_0000H	Reserved. If these bits are read, 0 is returned for each bit.
SRCVSIZE	R/W	12:0	0000H	Specify the number of pixels in the vertical direction for images. Specifiable range: 2 to 8,190 pixels

2.2.3 Source format setting registers

These registers (SRCFMT_CH0: 000CH and SRCFMT_CH1: 002CH) specify the source image format. This format also applies to destination images.

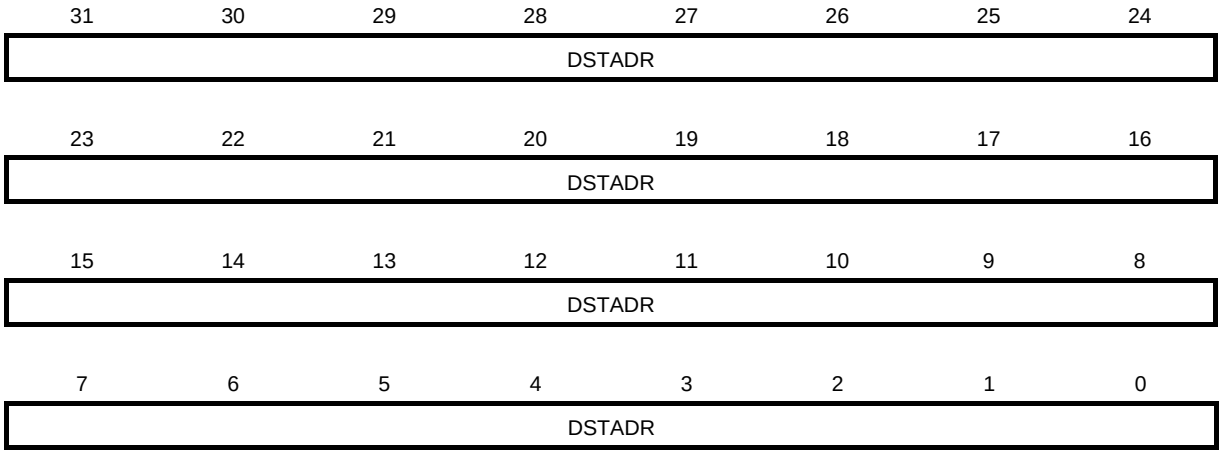


Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:3	0000_0000H	Reserved. If these bits are read, 0 is returned for each bit.
SRCFMT	R/W	2:0	0H	The image format of the input image is designated. For raster order mode: 0: Reserved 1: Reserved 2: 2 bytes (RGB565) 3: 3 bytes (RGB888/YUV444) 4: 4 bytes (ARGB8888) For random mode: 0: Reserved 1: RGB565 2: YUV422 interleaved 3: YUV422 semi-planar 4: YUV422 planar 5: YUV420 semi-planar 6: YUV420 planar

2.2.4 Destination address (YRGB/UV/V) setting registers

DSTADRYRGB_CH0: 0010H
DSTADRUV_CH0: 0014H
DSTADRV_CH0: 0018H
DSTADRYRGB_CH1: 0030H
DSTADRUV_CH1: 0034H
DSTADRV_CH1: 0038H

These registers specify the destination address in bytes.



Name	R/W	Bit No.	After Reset	Description
DSTADR	R/W	31:0	0000_0000H	Destination address Raster order mode is specified by setting bits 3 to 0 to FH.

Set DstAdrYRGB, SrcHsize and SrcVsize as the rotation angle as follows according to SrcFmt in Raster mode.

The value of DstAdrYRGB is calculated and established as follows.
SrcHsize and SrcVsize establish the number of pixels of the horizontal direction of an input picture and the vertical direction respectively.
SrcFmt is as follows by a Raster mode.

2: 2Byte (RGB565)
3: 3Byte (RGB888/YUV444)
4: 4Byte (ARGB8888)

MODE	DstAdrYRGB
00: Without rotate	The start address in which a rotate result is stocked is established.
01: 90 deg	The value which added (SrcVsize-1)* SrcFmt to the start address in which a rotate result is stocked is established.
10: 180 deg	The value which added (SrcHsize* SrcVsize-1)* SrcFmt to the start address in which a rotate result is stocked is established.
11: 270 deg	The value which added (SrcHsize* SrcVsize* SrcVsize)* SrcFmt to the start address in which a rotate result is stocked is established.

Next the value which subtracted 1 from the horizontal direction number of pixels of the input picture and the vertical direction number of pixels respectively is set as the value of SrcHsize and SrcVsize.

SrcHsize	SrcVsize
The number of pixels of the horizontal direction of an input picture- 1.	The number of pixels of the vertical direction of an input picture- 1

Sample code

```
switch(Mode & 3){
    case 0: break;
    case 1: DstAdrYRGB+=(SrcVsize-1)*SrcFmt; break;
    case 2: DstAdrYRGB+=(SrcHsize*SrcVsize-1)*SrcFmt; break;
    case 3: DstAdrYRGB+=(SrcHsize*SrcVsize-SrcVsize)*SrcFmt; break;
}
SrcVsize--;
SrcHsize--;
```

2.2.5 Destination image byte lane setting registers

These registers (DSTBL_CH0: 001CH and DSTBL_CH1: 003CH) specify the byte lane for a destination image.

31	30	29	28	27	26	25	24
Reserved							

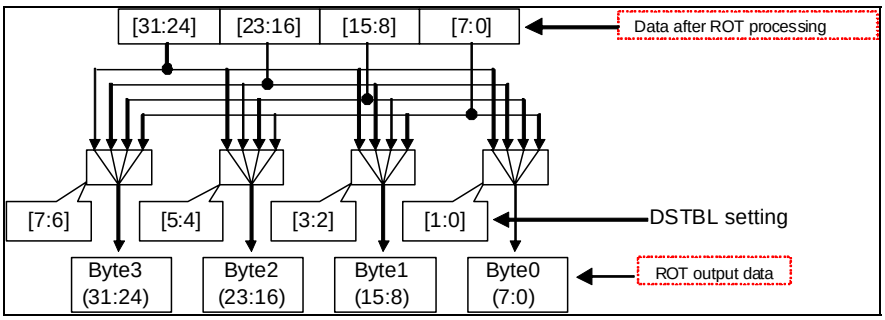
23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
DSTBL							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:8	00_0000H	Reserved. If these bits are read, 0 is returned for each bit.
DSTBL	R/W	7:0	E4H	When writing the data ROT processed on a memory, an output byte is established. A byte gets one of values of 0 to 3. DSTBL[7:6]: It's established in which byte a bit [31:24] of an output data of ROT is output. DSTBL[5:4]: It's established in which byte a bit [23:16] of an output data of ROT is output. DSTBL[2:3]: It's established in which byte a bit [15:8] of an output data of ROT is output. DSTBL[1:0]: It's established in which byte a bit [7:0] of an output data of ROT is output.

Figure 2-1. Relation between DSTBL and a byte



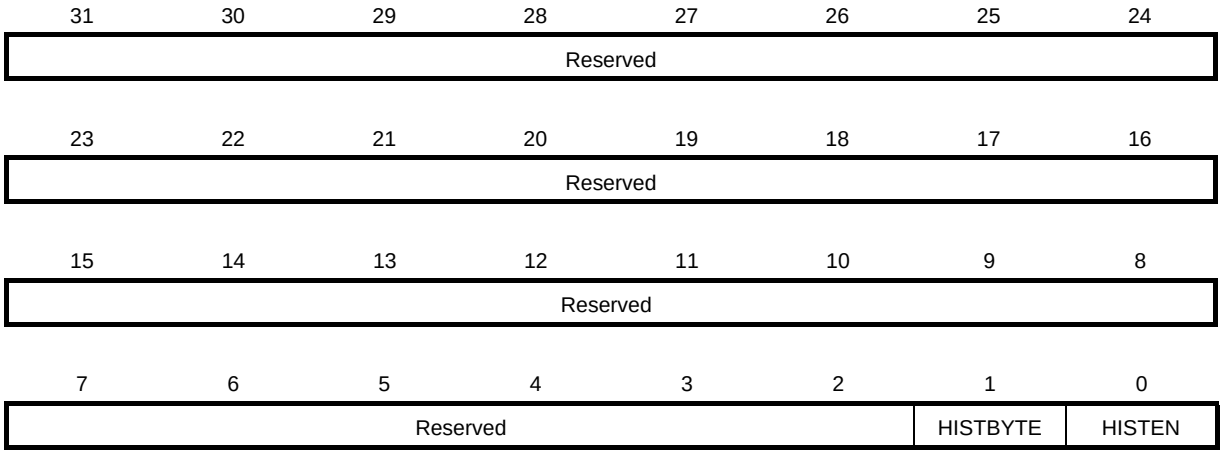
The table below shows the combinations of values that can be specified. If other values are specified, data becomes undefined.

Table 2-1. The combination by which Bytelane setting is possible

DSTBL[31:24]	DSTBL[23:16]	DSTBL[15:8]	DSTBL[7:0]	DSTBL[31:0]
3	2	1	0	E4
3	2	0	1	E1
3	1	2	0	D8
3	1	0	2	D2
3	0	2	1	C9
3	0	1	2	C6
2	3	1	0	B4
2	3	0	1	B1
2	1	3	0	9C
2	1	0	3	93
2	0	3	1	8D
2	0	1	3	87
1	3	2	0	78
1	3	0	2	72
1	2	3	0	6C
1	2	0	3	63
1	0	3	2	4E
1	0	2	3	4B
0	3	2	1	39
0	3	1	2	36
0	2	3	1	2D
0	2	1	3	27
0	1	3	2	1E
0	1	2	3	1B

2.2.6 Histogram control register

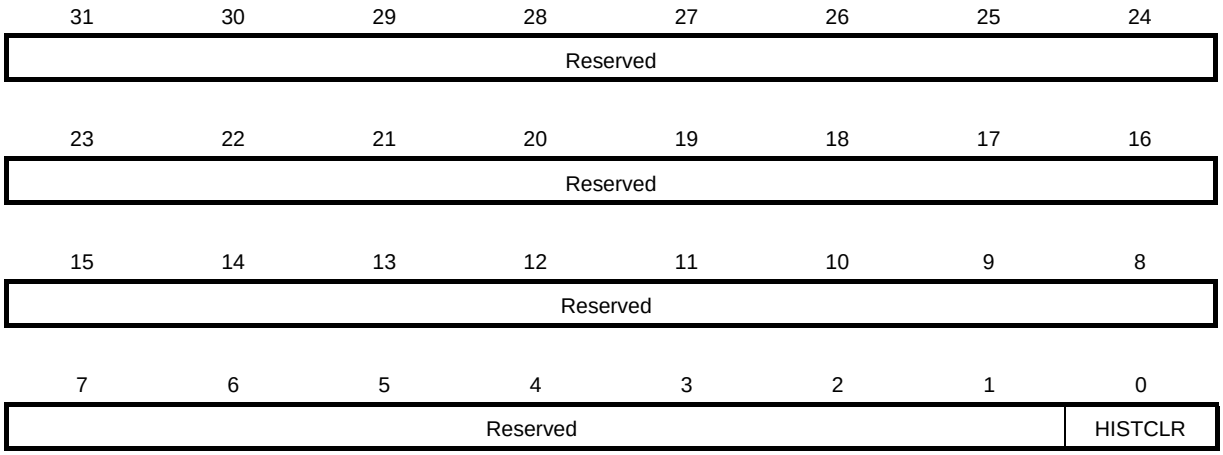
This register (HISTCTRL: 0040H) enables outputting a histogram. The settings specified for this register are valid only for the YUV422 interleaved mode.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	0000_0000H	Reserved. If these bits are read, 0 is returned for each bit.
HISTBYTE	R/W	1	Undefined	Select data from which to create a histogram. 0: Y 1: UV
HISTEN	R/W	0	Undefined	Specify whether to enable outputting a histogram. 0: Disable 1: Enable

2.2.7 Histogram value clear register

This register (HISTCLR: 0044H) is used to reset histogram value count registers 0 to 7 (HIST0 to HIST7).

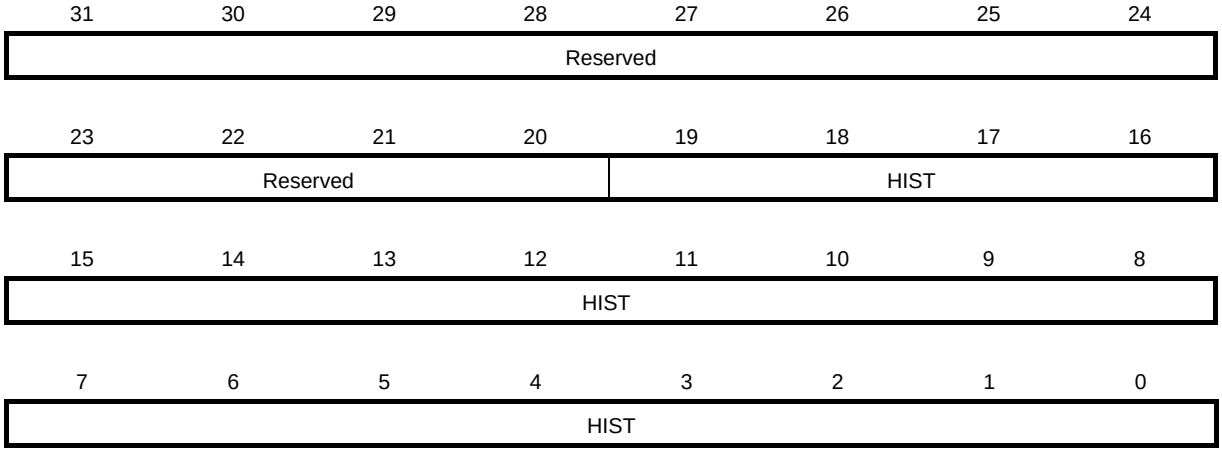


Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	0000_0000H	Reserved. If these bits are read, 0 is returned for each bit.
HISTCLR	R/W	0	0	1: Clear the histogram value count registers.

2.2.8 Histogram value count registers 0 to 7

HIST0: 0048H HIST1: 004CH
HIST2: 0050H HIST3: 0054H
HIST4: 0058H HIST5: 005CH
HIST6: 0060H HIST7: 0064H

These registers are used to count and store the number of data elements (8-bit components) input to the ROT module.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:20	000H	Reserved. If these bits are read, 0 is returned for each bit.
HIST	R	19:0	0_0000H	These bits are used to count and store the number of data elements (8-bit components) input to the ROT module.

3. Description of Functions

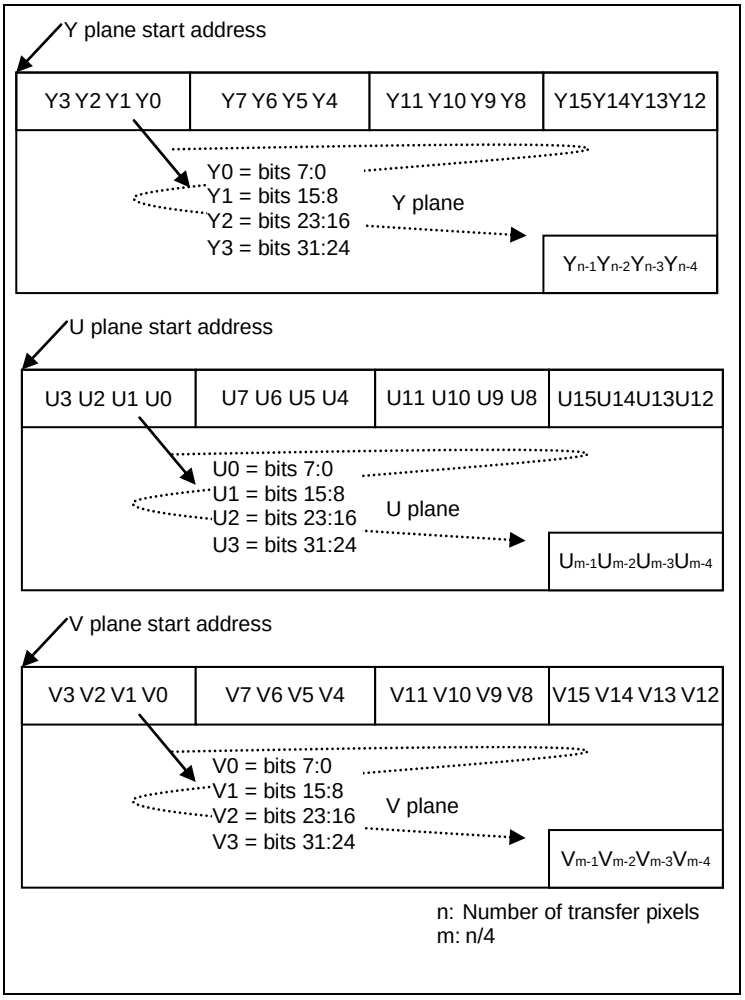
3.1 YUV Formats

3.1.1 YUV420 formats

YUV420 planar

Image data is transferred to the separate areas Y, U, and V in memory. (These areas are respectively referred to as the Y plane, U plane, and V plane in the figure below.) In each plane, any bytes can be replaced in 32-bit units. Figure 3-1 shows the format when little endian is specified.

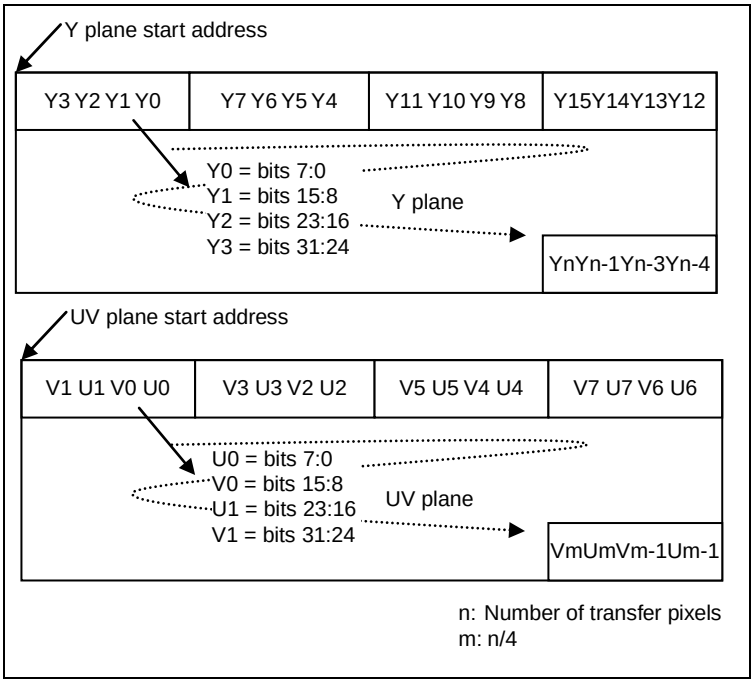
Figure 3-1. YUV420 Planar Format



YUV420 semi-planar

Image data is transferred to separate areas Y and UV in memory. (These areas are respectively referred to as Y plane and UV plane in the figure below.) In each plane, any bytes can be replaced in 32-bit units. Figure 3-2 shows the format when little endian is specified.

Figure 3-2. YUV420 Semi-Planar Format

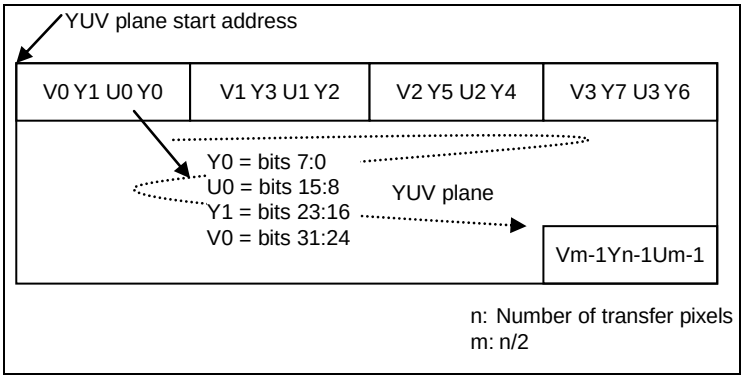


3.1.2 YUV422 formats

YUV422 interleaved

Image data is transferred from the memory area where YUV is interleaved. (This area is referred to as the YUV plane in the figure below.) In the plane, any bytes can be replaced in 32-bit units. Figure 3-3 shows the format when a VYUY data sequence is specified.

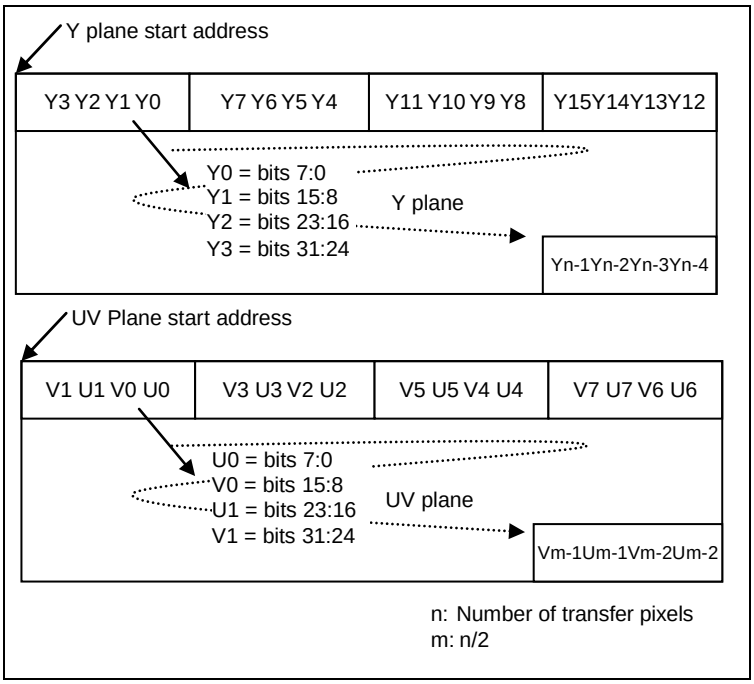
Figure 3-3. YUV422 Interleaved Format



YUV422 semi-planar

Image data Y and UV are transferred from separate memory areas. (These areas are referred to as the Y plane and UV plane in the figure below.) In each plane, any bytes can be replaced in 32-bit units. Figure 3-4 shows the format when little endian is specified.

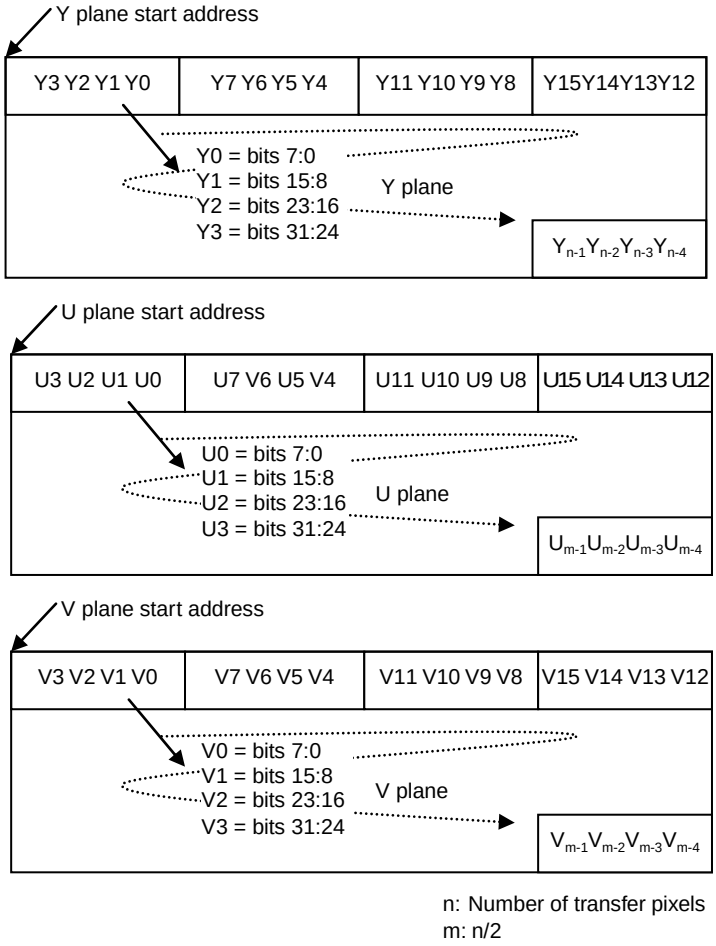
Figure 3-4. YUV422 Semi-Planar Format



YUV422 planar

Image data Y, U and V are transferred from separate memory areas. (These areas are referred to as the Y plane, U plane, and V plane in the figure below.) In each plane, any bytes can be replaced in 32-bit units. Figure 3-5 shows the format when little endian is specified.

Figure 3-5. YUV422 Planar Format



n: Number of transfer pixels
m: n/2

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