User's Manual

USB2.0 Host Controller

User's Manual

Multimedia Processor for Mobile Applications
EMMA Mobile ™ EV2

Renesas Electronics
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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the EMMA Mobile EV2. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Data Sheet	Hardware overview and electrical characteristics	EMMA Mobile EV2 Datasheet	R19DS0010EJxxxx
User's manual (1chip)	Hardware whole specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description	EMMA Mobile EV2 User's manual 1chip	R19UH0036EJxxxx
User's manual (module)	Hardware each macro specifications and operation description.	EMMA Mobile EV2 User's manual each module	See below

Document Name	Document No.	Document Name	Document No.
1chip	R19UH0036EJxxxx	DMA Controller	R19UH0043EJxxxx
System Management Unit	R19UH0037EJxxxx	LP-DDR/DDR2 Controller	R19UH0039EJxxxx
Timer	R19UH0054EJxxxx	SD Memory Card Interface	R19UH0061EJxxxx
System Timer	R19UH0055EJxxxx	SDIO Interface	R19UH0042EJxxxx
HD Video Decoder	R19UH0056EJxxxx	CF Card Interface	R19UH0062EJxxxx
Rotator	R19UH0057EJxxxx	Unified Serial Interface	R19UH0047EJxxxx
Resizer	R19UH0058EJxxxx	UART interface	R19UH0040EJxxxx
Image Composer	R19UH0038EJxxxx	USB 2.0 Host Controller (This manual)	R19UH0045EJxxxx
LCD Interface	R19UH0044EJxxxx	USB 2.0 Function Controller	R19UH0034EJxxxx
ITU-R BT.656 Interface	R19UH0059EJxxxx	IIC Interface	R19UH0052EJxxxx
Digital Terrestrial TV Interface	R19UH0048EJxxxx	General Purpose I/O Interface	R19UH0041EJxxxx
Camera Interface	R19UH0060EJxxxx	Pulse Width Modulation Interface	R19UH0063EJxxxx

4 digits of end shows the version.

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names

Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.

Examples the PM03 bit in the PM0 register

P3_5 pin, VCC pin

(2) Notation of Numbers

The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.

Examples Binary: 11b or 11

Hexadecimal: EFA0h

Decimal: 1234

3. Register Notation

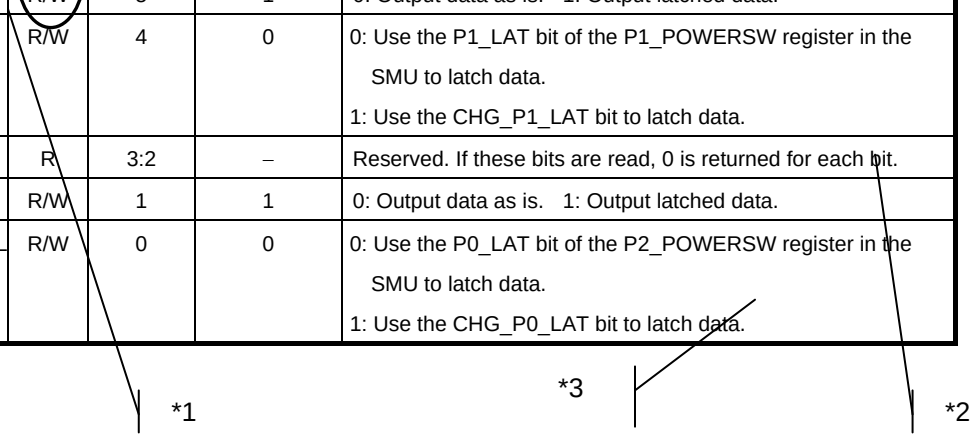
The symbols and terms used in register diagrams are described below.

x.x.x XXX register

This register (XXXXXXX: xxxx_xxxxh) …..

7	6	5	4	3	2	1	0
Reserved		CHG_P1_LAT	LATCH_P1_SEL	Reserved		CHG_P0_LAT	CHG_P0_LAT_SEL

Name	R/W	Bit No.	After Reset	Description
LATCH_P2_SEL	R/W	8	0	0: Use the P2_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P2_LAT bit to latch data.
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P1_LAT	R/W	5	1	0: Output data as is. 1: Output latched data.
LATCH_P1_SEL	R/W	4	0	0: Use the P1_LAT bit of the P1_POWERSW register in the SMU to latch data. 1: Use the CHG_P1_LAT bit to latch data.
Reserved	R	3:2	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P0_LAT	R/W	1	1	0: Output data as is. 1: Output latched data.
CHG_P0_LAT_SEL	R/W	0	0	0: Use the P0_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P0_LAT bit to latch data.



*1

R/W: Read and Write.

R: Read only.

W: Write only.

-: Nothing is assigned.

*2

Reserved bit.

Reserved bit. Set to specified value.

*3

・ Nothing is assigned.

Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.

・ Do not set to a value.

Operation is not guaranteed when a value is set.

・ Function varies according to the operating mode.

The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Register
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

Table of Contents

USB2.0 Host Controller

EMMA Mobile EV2

R19UH0045EJ0400
Rev.4.00
Apr 12, 2012

1. Overview

This specification describes the USB2.0 host function.

1.1 Features

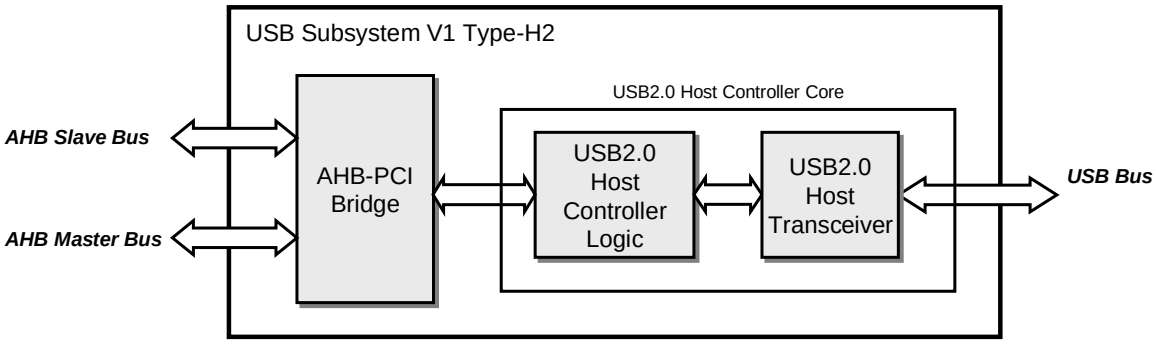
- Universal Serial Bus Specification Revision 2.0 Compliant
- Open Host Controller Interface(OHCI) Specification for USB Rev 1.0a compatible
- Enhanced Host Controller Interface (EHCI) Specification for USB Rev 1.0a compatible
- Supports USB2.0 High-Speed (480 Mbps), Full-Speed (12 Mbps), and Low-Speed (1.5 Mbps) Transfer
- USB System Clock: 24 MHz
- Use general I/O port (GPIO) for overcurrent detection and port power control

※ The Isochronous transfer is unsupported.

1.2 Block Overview

The simplified block diagram of USB Host controller V1 Type- H2 is shown in Figure 1-1.

Figure 1-1. Block Overview



(1) USB2.0 Host Controller Core

A controller core that consists of the USB2.0 Transceiver and USB2.0 Host Controller.

(2) USB2.0 Host Transceiver

A transceiver that includes a regulator, USB I/O, CDR, and PLL.

(3) USB2.0 Host Controller Logic

A EHCI/OHCI standard-compliant USB2.0 host controller core that includes a list transaction circuit, serial-to-parallel converter circuit and host transceiver control circuit and implements the USB high-speed transfer, full-speed transfer, and low-speed transfer.

(4) AHB-PCI Bridge

A module that converts the AHB cycle into the PCI bus cycle to the host controller

The slave I/F is used for register access from the CPU to the bridge inside and the host controller. The master I/F is used for PCI-initiator access transmission from the host controller to the AHB.

1.3 Precautions

This section provides the precautions that must be observed when using this USB host function.

1.4.1 Related to Specifications

(1) To ensure consistency of the whole USB host controller, restrictions are imposed on the setting of registers to the subblocks. These restrictions are written in each register description in Chapter 4. Registers by boldface. Read them carefully before using the USB host function.
(2) Dynamic control of the USB0_CLK, PMCLK, and PCICLK except for clock stop is not supported.
(3) The direct power-down function is supported. For details, refer to Section 9.3.

1.4.2 Related to AHB interface

32-bit register access is used for this USB host controller. 8-bit and 16-bit accesses are not allowed.

1.4.3 Related to Operations

The operation flows are shown in the following chapters.

- Chapter 5 ACCESSING REGISTERS — Mapping method of the AHB space and PCI space
- Chapter 9 POWER MANAGEMENT — Power management control method
- Chapter 10 OPERATING PROCEDURE — Initialization

2. Pin Functions

2.1 System Interface

Table 2-1. System Interface Pins

Pin Name	I/O	Description	Synchronization Clock	Active Level	After Reset	Pin handling when unused
USB0_CLK	Input	AHB clock	–	–	–	0
USB0_RSTZ	Input	AHB reset	Asynchronous	L	–	1
OSC1 clock	Input	USB reference clock	–	–	–	0
PCICLK	Input	Internal PCI clock	–	–	–	0

2.2 Interrupt Interface

Table 2-2. Interrupt Interface Pins

Pin Name	I/O	Description	Synchronization Clock	Active Level	After Reset	Pin handling when unused
USB_INTH	Output	AHB-PCI bridger interrupt (bridge)	USB0_CLK	H	0b	Open
U2H_OHCI_INT	Output	Host controller interrupt (OHCI)	USB0_CLK	H	0b	Open
U2H_EHCI_INT	Output	Host controller interrupt (EHCI)	USB0_CLK	H	0b	Open
U2H_PME_INT	Output	Host controller interrupt (PMEI)	USB0_CLK	H	0b	Open
U2H_BIND_INT	Output	Interrupt OR (bridge + OHCI + EHCI + PME)	USB0_CLK	H	0b	Open

2.3 USB Interface

Table 2-3. USB Interface Pins

Pin Name	I/O	Description	Synchronization Clock	Active Level	After Reset	Pin handling when unused
USB_DP1	I/O	USB bus full/low speed D+ signal Host controller USB bus high speed D + signal	Asynchronous	–	– (IN)	GND (pull down)
USB_DM1	I/O	USB bus full/low speed D- signal Host controller USB bus high speed D - signal	Asynchronous	–	– (IN)	GND (pull down)
USB_RREF1	–	Reference current generation	–	–	–	Open

2.4 Power Interface

Table 2-4. Power Interface Pins

Pin Name	I/O	Description	Pin handling when unused
USB_AVDD1	–	Regulator power supply pin	VDD
USB_AVSS1	–	Regulator ground pin	GND
USB_PVSS1	–	PLL ground pin	GND
USB_VD3311	–	IO power supply pin	VDD
USB_GND11	–	IO ground pin	GND
USB_GND21	–	IO ground pin	GND

3. Register Mapping

The USB Host controller V1 Type-H2 registers are organized into the following three areas.

1. OHCI and EHCI Operation Registers
2. PCI Configuraiton Spac
3. AHB-PCI Bridge PCI Communication

Prior to accessing the PCI Configuration Space, the following AHB-PCI Bridge registers must be enabled.

AHBPCI_WIN1_CTR

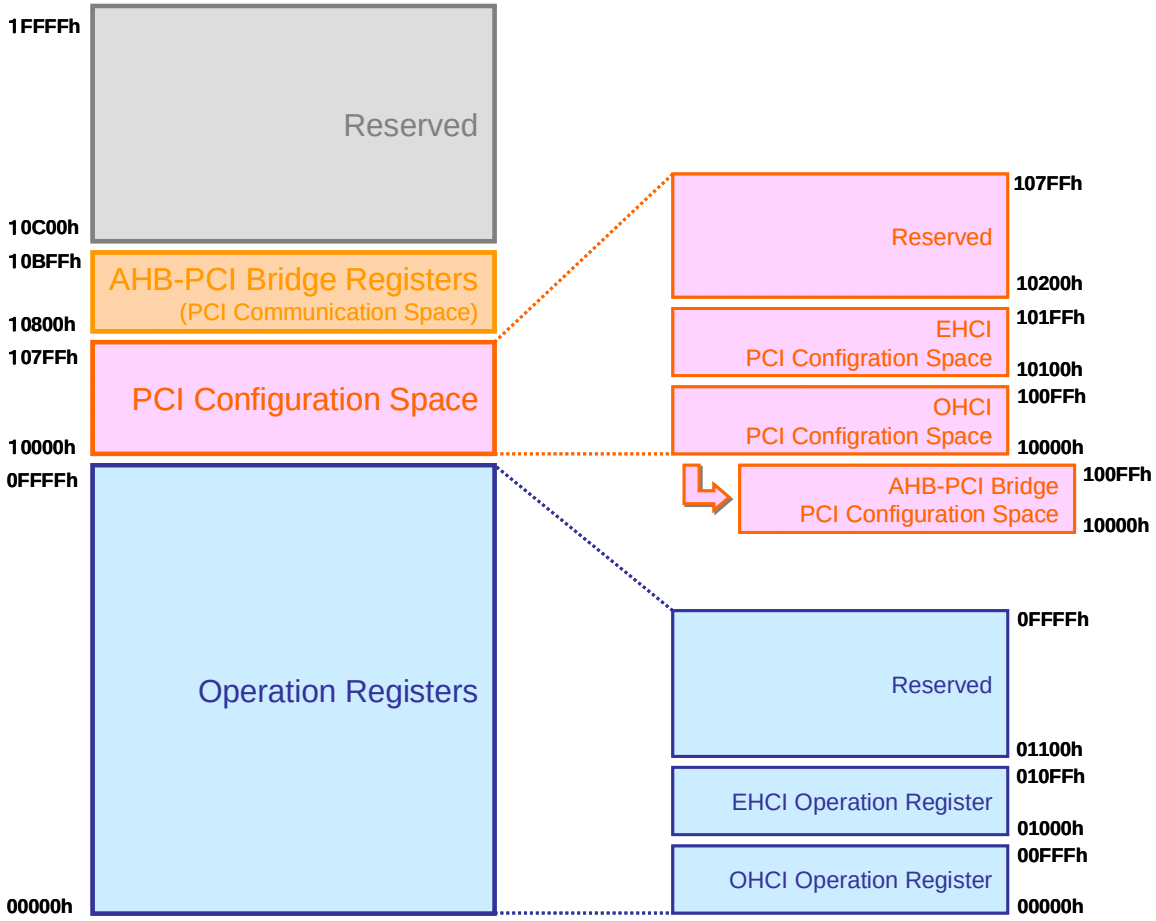
AHBPCI_WIN2_CTR

In addition to the AHB mapping, proper addressing of the OHCI and EHCI Operation Registers and PCI Communication Space in the USB host controller PCI is required.

For how to access to each register and how to perform address mapping, refer to Chapter 5.

Figure 3-1. Register Mapping

Base address : E270_0000H



The request address size : 128KByte

Table 3-1. Register Mapping

Address Offset	Register Name	Symbol
00000h	HcRevision	HcRevision
00004h	HcControl	HcControl
00008h	HcCommandStatus	HcCommandStatus
0000Ch	HcInterruptStatus	HcInterruptStatus
00010h	HcInterruptEnable	HcInterruptEnable
00014h	HcInterruptDisable	HcInterruptDisable
00018h	HcHCCA	HcHCCA
0001Ch	HcPeriodicCurrentED	HcPeriodicCurrentED
00020h	HcControlHeadED	HcControlHeadED
00024h	HcControlCurrentED	HcControlCurrentED
00028h	HcBulkHeadED	HcBulkHeadED
0002Ch	HcBulkCurrentED	HcBulkCurrentED
00030h	HcDoneHead	HcDoneHead
00034h	HcFmInterval	HcFmInterval
00038h	HcFmRemaining	HcFmRemaining
0003Ch	HcFmNumber	HcFmNumber
00040h	HcPeriodicStart	HcPeriodicStart
00044h	HcLSThreshold	HcLSThreshold
00048h	HcRhDescriptorA	HcRhDescriptorA
0004Ch	HcRhDescriptorB	HcRhDescriptorB
00050h	HcRhStatus	HcRhStatus
00054h	HcRhPortStatus1	HcRhPortStatus1
00058h	Reserved	
0005Ch - 00FFCh	Reserved	
01000h	HCIVERSION / CAPLENGTH	CAPL_VERSION
01004h	HCSPARAMS	HCSPARAMS
01008h	HCCPARAMS	HCCPARAMS
0100Ch	HCSP_PORTROUTE	HCSP_PORTROUTE
01010h - 0101Ch	Reserved	
01020h	USBCMD	USBCMD
01024h	USBSTS	USBSTS
01028h	USBINTR	USBINTR
0102Ch	FRINDEX	FRINDEX
01030h	CTRLDSSEGMENT	CTRLDSSEGMENT
01034h	PERIODICLISTBASE	PERIODICLISTBASE
01038h	ASYNCLISTADDR	ASYNCLISTADDR
0103Ch - 0105Ch	Reserved	
01060h	CONFIGFLAG	CONFIGFLAG
01064h	PORTSC1	PORTSC1
01068h	Reserved	
0106Ch - 0FFFCh	Reserved	

Address Offset	Register Name	Symbol
10000h - 107FCh	PCI Configuration Space (AHB-PCI Bridge / OHCI / EHCI)	
10800h	PCIAHB_WIN1_CTR	PCIAHB_WIN1_CTR
10804h	PCIAHB_WIN2_CTR	PCIAHB_WIN2_CTR
10808h	PCIAHB_DCT_CTR	PCIAHB_DCT_CTR
1080Ch	Reserved	
10810h	AHBPCI_WIN1_CTR	AHBPCI_WIN1_CTR
10814h	AHBPCI_WIN2_CTR	AHBPCI_WIN2_CTR
10818h	Reserved	
1081Ch	AHBPCI_DCT_CTR	AHBPCI_DCT_CTR
10820h	PCI_INT_ENABLE	PCI_INT_ENABLE
10824h	PCI_INT_STATUS	PCI_INT_STATUS
10828h - 1082Ch	Reserved	
10830h	AHB_BUS_CTR	AHB_BUS_CTR
10834h	USBCTR	USBCTR
10838h - 1083Ch	Reserved	
10840h	PCI_ARBITER_CTR	PCI_ARBITER_CTR
10844h	Reserved	
10848h	PCI_UNIT_REV	PCI_UNIT_REV
1084Ch - 1FFFCh	Reserved	

3.1 AHB-PCI Bridge PCI Configuration Register

The register map of the PCI Configuration Space for the AHB-PCI Bridge is shown in Table 3-2. AHB-PCI Bridge PCI Configuration Register Map

Table 3-2. AHB-PCI Bridge PCI Configuration Register Map

Offset	31 24	23 16	15 8	7 0	Abbreviation
000h	Device ID		Vendor ID		VID_DID
004h	Status		Command		CMND_STS
008h	Class Code			Revision ID	REVID_CC
00Ch	BIST	Header Type	Latency Timer	Cache Line Size	CLS_LT_HT_BIST
010h	AHB-PCI Bridge Registers Base Address				BASEAD
014h	PCI-AHB Window1 Base Address				WIN1_BASEAD
018h	Reserved				
01Ch					
020h					
024h					
028h					
02Ch	USB host controller ID		USB host controller Vendor ID		SSVID_SSID
030h	Reserved				
034h					
038h					
03Ch	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	INTR_LINE_PIN
040h	Reserved				
…					
7FCh					

3.2 OHCI PCI Configuration Register

The register map of the PCI Configuration Space for the OHCI host controller is shown in Table 3-3. OHCI PCI Configuration Register Map

Table 3-3. OHCI PCI Configuration Register Map

Offset	31 24	23 16	15 8	7 0	Abbreviation
000h	Device ID		Vendor ID		VID_DID
004h	Status		Command		CMND_STS
008h	Class Code			Revision ID	REVID_CC
00Ch	BIST	Header Type	Latency Timer	Cache Line Size	CLS_LT_HT_BIST
010h	OHCI Base Address				BASEAD
014h	Reserved				
018h					
01Ch					
020h					
024h					
028h					
02Ch	USB host controller ID		USB host controller Vendor ID		SSVID_SSID
030h	Reserved				
034h	Reserved			Cap_ptr	CAPPTR
038h	Reserved				
03Ch	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	INTR_LINE_PIN
040h	PMC		Next_Item_Ptr	Cap_ID	CAPID_NIP_PMCAP
044h	Data	PMCSR_BSE	PMCSR		PMC_STS_PMCSR
048h	Reserved				
…					
7FCh					

3.3 EHCI PCI Configuration Register

The register map of the PCI Configuration Space for the EHCI host controller is shown in Table 3-4. EHCI PCI Configuration Register Map

Table 3-4. EHCI PCI Configuration Register Map

Offset	31 24	23 16	15 8	7 0	Abbreviation
100h	Device ID		Vendor ID		VID_DID
104h	Status		Command		CMND_STS
108h	Class Code			Revision ID	REVID_CC
10Ch	BIST	Header Type	Latency Timer	Cache Line Size	CLS_LT_HT_BIST
110h	EHCI Base Address				BASEAD
114h	Reserved				
118h					
11Ch					
120h					
124h					
128h					
12Ch	USB host controller ID		USB host controller Vendor ID		SSVID_SSID
130h	Expansion ROM Base Address				EROM_BASEAD
134h	Reserved			Cap_ptr	CAPPTR
138h	Reserved				
13Ch	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	INTR_LINE_PIN
140h	PMC		Next_Item_Ptr	Cap_ID	CAPID_NIP_PMCAP
144h	Data	PMCSR_BSE	PMCSR		PMC_STS_PMCSR
148h	Reserved				
…					
15Ch					
160h	PORTWAKECAP		FLAD	SBRN	SBRN_FLADJ_PW
164h	Reserved				
…					
7FCh					

4. Registers

This chapter describes the register features in detail. The meaning of the bit assignment table is shown below.

Add	100h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W																														*R*	*R W*	*R W*
Symbol																														SYMBOL_C	SYMBOL_B	SYMBOL_A
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	1	0

Add: Indicates the address offset.

Bit: Indicates the position of the bit in the 32-bit space.

RW: R indicates that the bit can be read, and W indicates that the bit can be written.

Symbol: Indicates the name of the bit.

R: Indicates the initial value after reset.

B: Indicates the value immediately after a USB bus reset signal is received (available in the EPC area only).

Remark The bits whose **Symbol** column is blank are reserved.

4.1 OHCI Operation Registers

4.1.1 HcRevision Regsiter

Add	00000h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W																								R	R	R	R	R	R	R	R	R
Symbol																								Legacy	Revision[7:0]							
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Description
[31:9]	–	Reserved.
8	Legacy	Indicates whether the legacy support register is implemented in the host controller. This bit indicates 0b since this host controller does not support the legacy function.
[7:0]	Revision[7:0]	Indicates the version of the HCI specification implemented in the host controller. This field indicates 10h since this host controller complies with the OHCI standard 1.0a.

4.1.2 HcControl Regiser

Add	00004h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W																						RW	RW	RW	RW	RW	RW	RW		RW	RW	RW
Symbol																						RWE	RWC	IR	HCFS[1:0]		BLE	CLE		PLE	CBSR[1:0]	
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:11]	–	Reserved. (Be sure to write 0b to this field.)
10	RemoteWakeUp Enable (RWE)	Enables the detection of the upstream resume signal. 1: Resume signal is used as a remote wakeup 0: Resume signal is not used as a remote wakeup
9	RemoteWakeUp Connect (RWC)	This bit indicates whether the host controller supports the Remote wakeup. This bit must be set during initialization if the system supports remote wakeup. 1: RemoteWakeUp is supported 0: RemoteWakeUp is NOT supported
8	InterruptRouting (IR)	This bit indicates the interrupt route of the host controller. Interrupt indicated by the HcInterruptStatus register is notified to the system through this route. Do not change the default value ‘0b’ since this USB host controller does not use the SMI. 1: Interrupt occurs via SMI 0: Interrupt occurs via INTA
[7:6]	Host Controller FunctionalState (HCFS)[1:0]	Indicates the operation state of the host controller. Transition to the USB Operational starts management of the frame delimited by 1 ms. This operation state is controlled by the host controller driver, except for transition from USB Suspend to USB Resume by a remote wakeup. After hardware reset, this field indicates USB Reset, but it transitions to USB Suspend after software reset. 00: USB Reset 01: USB Resume 10: USB Operational 11: USB Suspend
5	BulkListEnable (BLE)	Bulk list enable bit This setting becomes valid from the next frame. This bit must be 0b when modifying the bulk list. 1: Bulk list transaction enabled 0: Bulk list transaction disabled
4	ControlListEnable (CLE)	Control list enable bit This setting becomes valid from the next frame. This bit must be 0b when modifying the control list. 1: Control list transaction enabled 0: Control list transaction disabled
3	–	Reserved.
2	PeriodicListEnable	Periodic list enable bit

<table>
<tr><td></td><td>(PLE)</td><td>This setting becomes valid from the next frame.
<table><tr><td>1</td><td>Periodic list transaction enabled</td></tr><tr><td>0</td><td>Periodic list transaction disabled</td></tr></table></td></tr>
<tr><td>[1:0]</td><td>ControlBulk
ServiceRatio
(CBSR)[1:0]</td><td>Specifies the servie ratio of the control transfer and bulk transfer.
This service ratio is maintained on the transfer for periodic list transaction.
<table><tr><th>CBSR</th><th>Bulk ED: Control ED Service Ratio</th></tr><tr><td>00b</td><td>1: 1</td></tr><tr><td>01b</td><td>2: 1</td></tr><tr><td>10b</td><td>3: 1</td></tr><tr><td>11b</td><td>4: 1</td></tr></table></td></tr>
</table>

4.1.3 HcCommandStatus Register

Add	00008h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W															R	R													RW	RW	RW	RW
Symbol															SOC[1:0]														OCR	BLF	CLF	HCR
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:18]	–	Reserved. (Be sure to write 0b to this field.)
[17:16]	Scheduling OverrunCount (SOC)[1:0]	Overrun counter Counts the schedule overruns. The value is incremented by one when an overrun occurs. It keeps counting regardless of the status of the SO bit (HcInterruptStatus Register).
[15:4]	–	Reserved. (Be sure to write 0b to this field.)
3	Ownership ChangeRequest (OCR)	This bit changes the ownership of the host controller.
2	BulkListFilled (BLF)	Indicates whether a bulk list exists. The host controller checks this bit when starting a transaction of the bulk list head. When a TD exists, a list transaction is not started if this bit is 0b. If 1b, it is set to 0b and the bulk ED transaction is started. When a TD is found in the bulk ED, this bit is set to 1b again, and the bulk TD transaction is continued. This bit needs to be set by the driver before the BLE bit (HcCommand Register) is set to start a list transaction.
1	ControlListFilled (CLF)	Indicates whether a control list exists. The host controller checks this bit when starting a transaction of the control list head. When a TD exists, a list transaction is not started if this bit is 0b. If 1b, it is set to 0b and the control ED transaction is started. When a TD is found in the control ED, this bit is set to 1b again, and the control TD transaction is continued. This bit needs to be set by the driver before the CLE bit (HcCommand Register) is set to start a list transaction.
0	Host Controller Reset (HCR)	Initiate a software reset of the host controller. When this bit is set, the host controller transitions to the USB Suspend state. This bit is cleared by the host controller at the completion of the reset.

4.1.4 HcInterruptStatus Register

Add	0000Ch																											
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W																										RW	RW	RW	RW	RW	RW	RW
Symbol																										RHSC	FNO	UE	RD	SF	WDH	SO
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:7]	–	Reserved. (Be sure to write 0b to this field.)
6	RootHubStatusChange (RHSC)	Interrupt bit indicating that the status of the HcRhPortStatus1 register has changed This bit is set when the HcRhPortStatus register is changed in hardware. Writing a 1b to this bit clears the interrupt. 1: RHSC interrupt occurred 0: RHSC interrupt not occurred
5	Frame Number Overflow (FNO)	Interrupt bit indicating that a MSB of the frame number has changed When a MSB of the frame is changed to 1 or to 0, the HcFmNumber register is updated, and then this bit is set. Writing a 1b to this bit clears the interrupt. 1: FNO interrupt occurred 0: FNO interrupt not occurred
4	Unrecoverable Error (UE)	Interrupt bit indicating that a system error has occurred in the PCI bus that is not related to the USB Writing a 1b to this bit clears this interrupt. 1: UE interrupt occurred 0: UE interrupt not occurred
3	ResumeDetected (RD)	Interrupt bit indicating that a resume state has been detected This bit is set when the Resume signal is asserted by a device on the USB bus. This bit is not set when the driver issues a USB Resume. Writing a 1b to this bit clears the interrupt. 1: RD interrupt occurred 0: RD interrupt not occurred
2	StartOfFrame (SF)	Interrupt bit indicating that the HcFmNumber register has been updated The host controller updates the HcFmNumber register when sending a SOF packet. Writing a 1b to this bit clears the interrupt. 1: SF interrupt occurred 0: SF interrupt not occurred
1	Writeback Done Head (WDH)	Interrupt bit indicating that the host controller has updated the content of the HcDoneHead register This bit is set immediately after updating the HcDoneHead register. The HcDoneHead register is not updated until this bit is cleared. Writing a 1b to this bit clears the interrupt. 1: WDH interrupt occurred 0: WDH interrupt not occurred
0	SchedulingOverrun (SO)	Interrupt bit indicating that an USB schedule overrun has occurred When a schedule overrun has occurred, the HcFmNumbe register is updated with the next frame, and then this bit is set. When this bit is set, the SchedulingOverrun bit (HcCommandStatus Register) is also incremented. Writing a 1b to this bit clears the interrupt.

			1	SO interrupt occurred	
			0	SO interrupt not occurred	

4.1.5 HcInterruptEnable Register

Add	00010h																											
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	RW																									RW	RW	RW	RW	RW	RW	RW
Symbol	MIE																									RHSCE	FNOE	UEE	RDE	SFE	WDHE	SOE
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
31	MasterInterruptEnable (MIE)	Enables the setting of the bit[30:0]. When set to 0b, all the interrupts are masked. This bit is cleared when a 1b is written to the corresponding bit in the HcInterruptDisable register. 1: Interrupt setting enabled 0: No change
[30:7]	–	Reserved. (Be sure to write 0b to this field.)
6	RootHubStatusChange Enable (RHSCE)	RHSC interrupt enable Writing a 1b enables the interrupt. This bit is cleared when a 1b is written to its corresponding bit in the HcInterruptDisable register. 1: RHSC interrupt enabled 0: No change
5	FrameNumberOverflow Enable (FNOE)	FNO interrupt enable Writing a 1b enables the interrupt. This bit is cleared when a 1b is written to its corresponding bit in the HcInterruptDisable register. 1: FNO interrupt enabled 0: No change
4	UnrecoverableError Enable (UEE)	UE interrupt enable Writing a 1b enables the interrupt. This bit is cleared when a 1b is written to its corresponding bit in the HcInterruptDisable register. 1: UE interrupt enabled 0: No change
3	ResumeDetectedEnable (RDE)	RD interrupt enable Writing a 1b enables the interrupt. This bit is cleared when a 1b is written to its corresponding bit in the HcInterruptDisable register. 1: RD interrupt enabled 0: No change
2	StartOfFrameEnable (SFE)	SF interrupt enable Writing a 1b enables the interrupt. This bit is cleared when a 1b is written to its corresponding bit in the HcInterruptDisable register. 1: SF interrupt enabled 0: No change
1	WritebackDoneHead Enable (WDHE)	WDH interrupt enable Writing a 1b enables the interrupt. This bit is cleared when a 1b is written to its corresponding bit in the HcInterruptDisable register. 1: WDH interrupt enabled 0: No change
0	SchedulingOverrun	SO interrupt enable

	Enable (SOE)	Writing a 1b enables the interrupt. This bit is cleared when a 1b is written to its corresponding bit in the HcInterruptDisable register. 1 SO interrupt enabled 0 No change

4.1.6 HcInterruptDisable Register

Add	00014h																												
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	RW																									RW	RW	RW	RW	RW	RW	RW
Symbol	MID																									RHSCD	FNOD	UED	RDD	SFD	WDHD	SOD
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
31	MasterInterruptDisable (MID)	Disables the setting of the HcInterruptEnable Register bit[30:0]. When set to 0b, all the interrupts are masked. Writing a 1b clears this bit. This bit is set when its corresponding bit in the HcInterruptEnable register is set to 1b. 1: Interrupt setting disabled 0: No change
[30:7]	–	Reserved. (Be sure to write 0b to this field.)
6	RootHubStatusChange Disable (RHSCD)	Disables the RHSC interrupt. Writing a 1b clears this bit. This bit is set when its corresponding bit in the HcInterruptEnable register is set to 1b. 1: RHSC interrupt disabled 0: No change
5	FrameNumberOverflow Disable (FNOD)	Disables the FNO interrupt. Writing a 1b clears this bit. This bit is set when its corresponding bit in the HcInterruptEnable register is set to 1b. 1: FNO interrupt disabled 0: No change
4	UnrecoverbleError Disable (UED)	Disables the UE interrupt. Writing a 1b clears this bit. This bit is set when its corresponding bit in the HcInterruptEnable register is set to 1b. 1: UE interrupt disabled 0: No change
3	ResumeDetected Disable (RDD)	Disables the RD interrupt. Writing a 1b clears this bit. This bit is set when its corresponding bit in the HcInterruptEnable register is set to 1b. 1: RD interrupt disabled 0: No change
2	StartOfFrame Disable (SFD)	Disables the SF interrupt. Writing a 1b clears this bit. This bit is set when its corresponding bit in the HcInterruptEnable register is set to 1b. 1: SF interrupt disabled 0: No change
1	WritebackDoneHead Disable (WDHD)	Disables the WDH interrupt. Writing a 1b clears this bit. This bit is set when its corresponding bit in the HcInterruptEnable register is set to 1b. 1: WDH interrupt disabled 0: No change

<table>
<tr>
<td>0</td>
<td>SchedulingOverrun
Disable
(SOD)</td>
<td>Disables the SO interrupt.
Writing a 1b clears this bit. This bit is set when its corresponding bit in the HcInterruptEnable register is set to 1b.
<table>
<tr><td>1</td><td>SO interrupt disabled</td></tr>
<tr><td>0</td><td>No change</td></tr>
</table>
</td>
</tr>
</table>

4.1.7 HcHCCA Register

Add	00018h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW								
Symbol	HcHCCA[31:8]																															
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:8]	HcHCCA[31:8]	This field specifies the base address of RAM assigned as the host controller communication area. This must be set at initialization. The host controller requires 256 bytes of HCCA starting from the specified base address.
[7:0]	–	Reserved. (Be sure to write 0b to this field.)

4.1.8 HcPeriodicCurrentED Register

Add	0001Ch																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R				
Symbol	Periodic CurrentED[31:4]																															
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:4]	PeriodicCurrentED [31:4]	This field indicates the address in which a periodic list transaction is currently performed. The host controller updates the pointer of this field when one periodic list transaction terminates.
[3:0]	–	Reserved.

4.1.9 HcControlHeadED Register

Add	00020h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW				
Symbol	ControllHeadED[31:4]																															
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:4]	ControlHeadED [31:4]	This field specifies the header address of the list ED for control transfer. This field must be set before setting the CLE bit of the HcControl register.
[3:0]	–	Reserved. (Be sure to write 0b to this field.)

4.1.10 HcControlCurrentED Register

Add	00024h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW				
Symbol	ControllCurrentED[31:4]																															
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:4]	ControlCurrentED [31:4]	This field indicates the address in which a control list transaction is currently performed. This field is updated by the host controller when a control ED transaction terminates. Set to 00000000h indicating the bottom of the list when newly creating a list. Ensure that the ED pointed by the CCED link pointer exists when a suspended transfer is resumed.
[3:0]	–	Reserved. (Be sure to write 0b to this field.)

4.1.11 HcBulkHeadED Register

Add	00028h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW				
Symbol	BulkHeadED[31:4]																															
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:4]	BulkHeadED[31:4]	This field spedifies the header addres of the list ED for bulk transfer. This must be set before setting the BLE bit of the HcControl register.
[3:0]	–	Reserved. (Be sure to write 0b to this field.)

4.1.12 HcBulkCurrentED Register

Add	0002Ch																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW				
Symbol	BulkCurrentED[31:4]																															
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:4]	BulkCurrentED [31:4]	This field indicates the address in which a bulk list transaction is currently performed. This field is updated by the host controller when a bulk ED transaction terminates. Set to 00000000h indicating the bottom of the list when newly creating a list. Ensure that the ED pointed by the BCED link pointer exists when a suspended transfer is resumed.
[3:0]	–	Reserved. (Be sure to write 0b to this field.)

4.1.13 HcDoneHead Register

Add	00030h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R				
Symbol	DoneHead[31:4]																															
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:4]	DoneHead[31:4]	This field indicates the address of the HcDoneHead of the host controller.
[3:0]	–	Reserved.

4.1.14 HcFmInterval Register

Add	00034h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Symbol	FIT	FSMPS[14:0]																	FI[13:0]													
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	1	1	0	1	1	1	1	1

Bit	Symbol	Description
31	FrameIntervalToggle (FIT)	This bit is used for frame synchronization between the HCD and HC. Toggle this bit when writing the FI field from the HCD. The HC reflects the FIT value to the FRT bit of the HcFmRemaining register when loading the FI field. The HCD can check whether a newly set FI value has been reflected by comparing the FIT and FRT values.
[30:16]	FSLagestDataPacket (FSMPS)[14:0]	This field specifies the maximum data amount that can be transmitted or received without schedule overruns. This value is determined by comparing the current frame position and set value. This field is set from the driver since the value varies depending on the specifications of the system bus.
[15:14]	–	Reserved. (Be sure to write 0b to this field.)
[13:0]	FrameInterval(FI) [13:0]	This field is used to set the frame length that applies to a full-speed mode. To satisfy the USB standard (= 1 ms), this value needs to be set to 2EDFh.

4.1.15 HcFmRemaining Register

Add	00038h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R																		R	R	R	R	R	R	R	R	R	R	R	R	R	R
Symbol	FRT																		FR[13:0]													
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	1	1	0	1	1	1	1	1

Bit	Symbol	Description
31	FrameRemainingToggle (FRT)	This bit is used for frame synchronization between the HCD and HC. When the FR value reaches 0000h, the FI value is reloaded. The HC copies the FIT value into this bit when reloading the FI value. The HCD can check whether the FI value has been reflected to the FR by comparing the FIT and FRT values.
[30:14]	–	Reserved.
[13:0]	FrameRemaining(FR) [13:0]	This field indicates the current value of the frame. This field value is decremented at elapse of time. When this value reaches 0000h, the frame value is reloaded. Copy the FI value into this field to start counting again.

4.1.16 HcFmNumber Register

Add	0003Ch																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W																	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Symbol																	FrameNumber[15:0]															
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:16]	–	Reserved.
[15:0]	FrameNumber[15:0]	This field indicates the number of elapsed frames. When the FR value reaches 0000h, this value is incremented.

4.1.17 HcPeriodicStart Register

Add	00040h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W																			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Symbol																			PeriodicStart[13:0]													
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:14]	–	Reserved. (Be sure to write 0b to this field.)
[13:0]	PeriodicStart [13:0]	This field is used to determine the transfer rate of the periodic list and non-periodic list. This field needs to be set at initialization of the host controller by the HCD. When the FmRemaining value is larger than this value, the non-periodic list is higher priority than the periodic list. The OHCI standard recommends that this value be set to 10 percent of the FmInterval, which is 3E67h.

4.1.18 HcLSThreshold Register

Add	00044h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W																					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Symbol																					HcLSThreshold[11:0]											
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	1	0	0	0

Bit	Symbol	Description
[31:12]	–	Reserved. (Be sure to write 0b to this field.)
[11:0]	HcLSThreshold [11:0]	This field is used to create the threshold of LS transfer. When the FmRemaining value is larger than this value, LS transfer can be started.

4.1.19 HcRhDescriptorA Register

Add	00048h																											
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW												RW	RW	R	RW	RW	R	R	R	R	R	R	R	R
Symbol	POTPGT[7:0]																			NOCP	OCPM	DT	NPS	PSM	NDP[7:0]							
R	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	1	0

Bit	Symbol	Description
[31:24]	PowerOnToPowerGoodTime (POTPGT)[7:0]	This field determines a time to wait before accessing a powered-on root hub. The time is set in 2-ms intervals; therefore, the wait time is POTPGTx2 ms.
[23:13]	–	Reserved. (Be sure to write 0b to this field.)
12	NoOverCurrentProtection (NOCP)	This bit specifies whether to support the overcurrent function of the root hub. 1: Overcurrent state is not supported 0: Overcurrent state is supported
11	OverCurrentProtectionMode (OCPM)	This bit specifies how the root hub overcurrent is notified. This setting must be matched to the PowerSwitchingMode bit. This setting is effective only when NoOverCurrentProtection bit is cleared. 1: Individual port overcurrent protection 0: Global overcurrent protection
10	DeviceType (DT)	Indicates that the root hub is not a compound device. This bit is fixed to 0b since the root hub is not allowed to be a compound device.
9	NoPowerSwitching (NPS)	Determines whether to support a power switching. 1: Powered on when the host controller is in operation 0: Power switching is supported
8	PowerSwitchingMode (PSM)	Determines how to control a port power switching of the root hub. When the PortPowerControlMask bit is set, the port is controlled by the SetPortPower and ClearPortPower. When the PortPowerControlMask bit is cleared, the port is controlled by the SetGlobalPower and ClearGlobalPower. This setting is effective only when NoPowerSwitching is cleared. 1: Individual port power switching 0: Global port power switching
[7:0]	NumberDownstreamPort (NDP)[7:0]	This field specifies the number of downstream ports that the root hub of the host controller supports.

4.1.20 HcRhDescriptorB Register

Add	0004Ch																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	R
Symbol	PPCM[15:0]																DR[15:0]															
R	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:16]	PortPowerControlMask (PPCM)[15:0]	Indicates whether bit is controlled by the SetGlobalPower and Clear GlobalPower. This setting is effective when the PowerSwitichingMode bit is set. Field bit: Description 0: Reserved 1: Port 1 device 2: Port 2 device [15:3]: Reserved Value 1: Port is controlled by SetPortPower and ClearPortPower 0: Port is controlled by SetGlobalPower and ClearGlobalPower
[15:0]	DeviceRemovable (DR)[15:0]	Indicates whether a port of the host controller is removable. Field bit: Description 0: Reserved 1: Port 1 device 2: Port 2 device [15:3]: Reserved Value 1: Device is non-removable 0: Device is removable

4.1.21 HcRhStatus Register

Add	00050h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	W																R W															
Symbol Read																	DRWE															
Symbol Write	CRWE																SRWE															
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	RW	Symbol	Description
31	W	ClearRemote WakeupEnable (CRWE)	This bit clears the DRWE. When this bit is set to 1, the DeviceRemoteWakeupEnable bit is cleared. Writing a 0b has no effect.
[30:16]		–	Reserved. (Be sure to write 0b to this field.)
15	R	DeviceRemote WakeupEnable (DRWE)	ConnectStatusChange interrupt enable bit When set, the ConnectStatusChange event causes a state transition from USB Suspend to USB Resume and triggers a ResumeDetect interrupt. 1 ConnectStatusChange is used as a remote wakeup 0 ConnectStatusChange is used as a remote wakeup
	W	SetRemote WakeupEnable (SRWE)	DRWE enable bit When set, the DeviceRemoteWakeupEnable bit can be set. Writing an ob has no effect.
[14:0]		–	Reserved. (Be sure to write 0b to this field.)

4.1.22 HcRhPortStatus1 Register

Add	00054h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W												R W		R W																	
Symbol												PRSC		PSSC																	
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:21]	–	Reserved. (Be sure to write 0b to this field.)
[20:19]	PortReset StatusChange (PRSC)	This bit indicates that the port reset has been completed. This bit is set when 10-ms hardware reset is terminated. This bit is cleared when a 1b is written from the driver. 1: Port reset is completed 0: PortResetStatus not changed
18	PortSuspend StatusChange (PSSC)	This bit indicates that the resume sequence has been terminated. This bit is set when all the hardware resume processings are terminated. This bit is cleared when a 1b is written from the driver. 1: Resume has been completed 0: PortSuspendStatus not changed
[17:0]	–	Reserved. (Be sure to write 0b to this field.)

4.2 EHCI Operation Registers

4.2.1 HCIVERSION Register and CAPLENGTH Register

Add	01000h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R									R	R	R	R	R	R	R	R
Symbol	Interface Version Number[15:0]																								Capability Registers Length[7:0]							
R	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit	Symbol	Description
[31:16]	Interface Version Number[15:0]	This bit indicates the version of the EHCI that the host controller supports. This bit is set to 0100h since this host controller complies with the EHCI Rev1.0.
[15:8]	–	Reserved
[7:0]	Capability Registers Length[7:0]	This bit indicates the start address of the Operation register of the host controller. This bit indicates 20h since the operation register starts from 20h in this core.

4.2.2 HCSPARAMS Register

Add	01004h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W									R	R	R	R				R	R	R	R	R	R	R	R	R	R			R	R	R	R	R
Symbol									Debug Port Number[3:0]							P_INDICATOR	Number of Companion Controller[3:0] (N_CC)				Number of Ports per Companion Controller[3:0] (N_PCC)				Port Routing Rules			Port Power Control (PPC)	Number of Ports[3:0] (N_PORTS)			
R1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
R2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	1	0	0	1	0

Bit	Symbol	Description
[31:24]	–	Reserved
[23:20]	Debug Port Number[3:0]	This bit indicates 000b since this host controller does not have a debug port.
[19:17]	–	Reserved
16	P_INDICATOR	This bit indicates 0b since this USB host controller does not support the Port Indicator Control.
[15:12]	Number of Companion Controller[3:0] (N_CC)	Indicates the number of companion host controllers. This field indicates 1h since the OHCI is a companion host controller in this USB host controller.
[11:8]	Number of Ports per Companion Controller[3:0] (N_PCC)	Indicates the number of ports per companion host controller. This bit indicates 1h when the NPPFAHBUSB2HOST1PV10 that has one port is used, and indicates 2h when the NPPFAHBUSB2HOST2PV10 that has two ports is used.
7	Port Routing Rules	Indicates how the companion host controller is mapped.
[6:5]	–	Reserved
4	Port Power Control(PPC)	In this USB host controller, the host controller does not support the power supply control, but this bit indicates 1b.
[3:0]	Number of Ports[3:0] (N_PORTS)	Indicates the number of downstream ports.

4.2.3 HCCPARAMS Register

Add	01008h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W																	R	R	R	R	R	R	R	R	R	R	R	R		R	R	R
Symbol																	EHCI Extend Capabilities Pointer[7:0] (EECP)													Asynchronous Schedule Park Capability	Programming Frame List Flag	64-bit Addressing Capability
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0	1	1	0

Bit	Symbol	Description
[31:16]	–	Reserved
[15:8]	EHCI Extend Capabilities Pointer[7:0] (EECP)	A pointer to the address of the extended register of the EHCI. Indicates that the extended register exists in the EHCI Configuration Space E8h. Reading this field has no meaning since this USB host controller does not support the legacy function that is explained in the extended register.
[7:4]	–	Reserved
3	–	Reserved
2	Asynchronous Schedule Park Capability	This field indicates 1b since the host controller supports the asynchronous schedule park mode of the HS.
1	Programming Frame List Flag	This field indicates 1b since the host controller supports the frame list size that is smaller than 4 Kbytes. (USBCMD register bit[3:2] Frame List Size)
0	64-bit Addressing Capability	This field indicates 0b since the host controller does not support the 64-bit addressing.

4.2.4 HCSP_PORTROUTE Register

Add	0100Ch																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Symbol	Companion Port Route[31:0]																															
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:0]	Companion Port Route[31:0]	Indicates the number of ports of the companion host controller.

4.2.5 USBCMD Register

Add	01020h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W									RW	RW	RW	RW	RW	RW	RW	RW					RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Symbol									Interrupt Threshold Control[7:0]												Asynchronous Schedule Park Mode Enable		Asynchronous Schedule Park Mode Count[1:0]		Light Host Controller Reset	Interrupt on Async Advance Doorbell	Asynchronous Schedule Enable	Periodic Schedule Enable	Frame List Size[1:0]		Host Controller Reset(HCRESET)	Run/Stop(RS)
R	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:24]	–	Reserved. (Be sure to write 0b to this field.)
[23:16]	Interrupt Threshold Control[7:0]	Indicates the maximum interrupt rate of the host controller. If a value that is not listed in the following table is set, the operation is not guaranteed. 00h Reserved 01h 1 micro-frame 02h 2 micro-frames 04h 4 micro-frames 08h 8 micro-frames (1 ms) 10h 16 micro-frames (2 ms) 20h 32 micro-frames (4 ms) 40h 64 micro-frames (8 ms)
[15:12]	–	Reserved. (Be sure to write 0b to this field.)
11	Asynchronous Schedule Park Mode Enable	Enables or disables the asynchronous schedule park mode. 1 Enable 0 Disable
10	–	Reserved. (Be sure to write 0b to this field.)
[9:8]	Asynchronous Schedule Park Mode Count[1:0]	Specifies the number of counts for the asynchronous schedule park mode. The valid values are 1h through 3h. This bit is effective when the Asynchronous Schedule Park Mode Enable (bit[11]) = 1b.
7	Light Host Controller Reset	This bit is fixed to 0b since the host controller does not support the Light Host Controller Reset.
6	Interrupt on Async Advance Doorbell	This bit is used to generate an interrupt when the host controller starts the next asynchronous list transaction. At the start of the next asynchronous list transaction, the host controller sets the Interrupt on Async Advance bit (USBSTS register bit[5]) to generate an interrupt, provided that the Interrupt on Async Advance Enable

<table>
<tr><td></td><td></td><td>(USBINTR bit[5]) = 1b .This bit is cleared automatically when the Interrupt on Async Advance bit is set. If this bit is set when Asynchronous Schedule Enable = 0b, the operation is not guaranteed.</td></tr>
<tr><td>5</td><td>Asynchronous Schedule Enable</td><td>This bit determines whether the host controller processes the asynchronous list.<table><tr><td>1</td><td>Asynchronous schedule transaction enabled</td></tr><tr><td>0</td><td>Asynchronous schedule transaction disabled</td></tr></table></td></tr>
<tr><td>4</td><td>Periodic Schedule Enable</td><td>This bit determines whether the host controller processes the periodic list.<table><tr><td>1</td><td>Periodic schedule transaction enabled</td></tr><tr><td>0</td><td>Periodic schedule transaction disabled</td></tr></table></td></tr>
<tr><td>[3:2]</td><td>Frame List Size[1:0]</td><td>Specifies the frame list size. The index of the current frame list can be obtained through the FRINDEX register.<table><tr><td>00b</td><td>1024 components (4096 bytes)</td></tr><tr><td>01b</td><td>512 components (2048 bytes)</td></tr><tr><td>10b</td><td>256 components (1024 bytes)</td></tr><tr><td>11b</td><td>Reserved</td></tr></table></td></tr>
<tr><td>1</td><td>Host Controller Reset (HCRESET)</td><td>When set to 1b, the host controller initializes the internal pipelines and state machine. The USB communication is stopped immediately. In this case, the USB Reset is not issued to the downstream. This reset operation initializes the EHCI operation registers, and the port owner returns to the OHCI. The PCI configuration registers are not initialized. This bit is automatically cleared by the host controller at the completion of the reset operation. This reset cannot be cancelled by writing a 0b by software. Set this bit when the HCHalted bit (USBSTS register bit[12]) is set to 1b.</td></tr>
<tr><td>0</td><td>Run/Stop(RS)</td><td>When set to 1b, the host controller starts the operation. Use the HCHalted bit (USBSTS register bit[12]) to check whether the host controller has completed the transaction and stopped the operation. Set this bit to 1b when the host controller is halted.<table><tr><td>1</td><td>Run (Scheduled transactions are performed)</td></tr><tr><td>0</td><td>Stop (Transactions have completed, and host controller is halted)</td></tr></table></td></tr>
</table>

4.2.6 USBSTS Register

Add	01024h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W																	R	R	R	R							RW	RW	RW	RW	RW	RW
Symbol																	Asynchronous Schedule Status	Periodic Schedule Status	Reclamation	HCHalted							Interrupt on Async Advance	Host System Error	Frame List Rollover	Port Change Detect	USB Error Interrupt(USBERRINT)	USB Interrupt (USBINT)
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:16]	–	Reserved. (Be sure to write 0b to this field.)
15	Asynchronous Schedule Status	Indicates the current status of the asynchronous schedule. 1 Asynchronous schedule enabled 0 Asynchronous schedule disabled
14	Periodic Schedule Status	Indicates the current status of the periodic schedule. 1 Periodic schedule enabled 0 Periodic schedule disabled
13	Reclamation	This bit indicates 0b after reset. This bit is cleared to 0b when the host controller reads the QH of which H is 1. When the host controller executes an asynchronous transaction, this bit is set to 1b. This bit is also set to 1b when a start event has been detected. When this bit is 0b, if the host controller reads the QH of which H is 1, the host controller enters into the asynchronous sleep mode.
12	HCHalted	This bit is set to 0b when the RS bit (USBCMD Register bit[0]) is set to 1b. This bit is set to 1b when the RS bit is cleared to 0b by the host controller to stop the operation due to a software error or internal error. 1 Host controller is halted 0 Host controller is not halted
[11:6]	–	Reserved. (Be sure to write 0b to this field.)
5	Interrupt on Async Advance	The host controller checks the Interrupt on Async Advance Doorbell bit (USBCMD Register bit[6]) after reading the QH. When it is set to 1b, the host controller issues an interrupt at the next interrupt threshold. This bit is cleared when a 1b is written by S/W. Writing a 0b has no effect. 1 Asynchronous list read interrupt occurred 0 Interrupt not occurred
4	Host System Error	This bit is set to 1b when a fatal error (e.g., parity error on the PCI system) occurs in the host controller. When set to 1b, an interrupt is generated. When this error has occurred, the RS bit (USBCMD Register bit[0]) is cleared to 0b to avoid any additional execution of TD.

<table>
<tr><td></td><td></td><td>This bit is cleared when a 1b is written by S/W. Writing a 0b has no effect.
<table><tr><td>1</td><td>System error has occurred</td></tr><tr><td>0</td><td>Interrupt has not been generated</td></tr></table></td></tr>
<tr><td>3</td><td>Frame List Rollover</td><td>This bit is set to 1b by the host controller when the Frame Index field (FRINDEX Register) returns to 000h from the maximum value. The maximum value is specified by the Frame List Size (USBCMD Register bit[3:2]). This bit is cleared when a 1b is written by S/W. Writing a 0b has no effect.
<table><tr><td>1</td><td>Frame list has returned to 000h</td></tr><tr><td>0</td><td>Frame list has not returned to 000h</td></tr></table></td></tr>
<tr><td>2</td><td>Port Change Detect</td><td>This bit is set to 1b by the host controller when the USB bus state of a port in which the Port Owner (PORTSC1 Register bit[13]) is 0b changes (the Force Port Resume bit, Over-Current Change bit, Port Enabled/Disabled Change bit or Connect Status Change bit is set to 1b).
This bit is cleared when a 1b is written by S/W. Writing a 0b has no effect.</td></tr>
<tr><td>1</td><td>USB Error Interrupt (USBERRINT)</td><td>This bit is set to 1b by the host controller. When set, an interrupt occurs. This bit is set when an error occurs during USB transaction (e.g., overflow of the error counter).
This bit is cleared when a 1b is written by S/W. Writing a 0b has no effect.
<table><tr><td>1</td><td>Error has occurred during USB transfer</td></tr><tr><td>0</td><td>Error has not occurred during USB transfer</td></tr></table></td></tr>
<tr><td>0</td><td>USB Interrupt (USBINT)</td><td>This bit is set to 1b when an USB transaction is terminated or when a short packet is received. When set to 1b, an interrupt is generated.
This bit is cleared when a 1b is written by S/W. Writing a 0b has no effect.
<table><tr><td>1</td><td>USB transfer has terminated</td></tr><tr><td>0</td><td>USB transfer has not terminated</td></tr></table></td></tr>
</table>

4.2.7 USBINTR Register

Add	01028h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W																											R/W	R/W	R/W	R/W	R/W	R/W
Symbol																											Interrupt on Async Advance Enable	Host System Error Enable	Frame List Rollover Enable	Port Change Interrupt Enable	USB Error Interrupt Enable	USB Interrupt Enable
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:6]	–	Reserved. (Be sure to write 0b to this field.)
5	Interrupt on Async Advance Enable	Enables or disables the Interrupt on the Async Advance bit (USBSTS Register bit[5]). The interrupt is cleared by the Async Advance bit. 1 Enabled 0 Disabled
4	Host System Error Enable	Enables or disables the Host System Error bit (USBSTS Register bit[4]). The interrupt is cleared by the Host System Error bit. 1 Enabled 0 Disabled
3	Frame List Rollover Enable	Enables or disables the Frame List Rollover bit (USBSTS Register bit{3}). The interrupt is cleared by the Frame List Rollover bit. 1 Enabled 0 Disabled
2	Port Change Interrupt Enable	Enables or disables the Port Change Detect bit (USBSTS Register bit[2].) The interrupt is cleared by the Port Change Detect bit. 1 Enabled 0 Disabled
1	USB Error Interrupt Enable	Enables or disables the USBERRINT bit (SBSTS Register bit[1]). The interrupt is cleared by the USBERRINT bit. 1 Enabled 0 Disabled
0	USB Interrupt Enable	Enables or disables the USBINT bit (USBSTS Register bit[0]). The interrupt is cleared by the USBINT bit. 1 Enabled 0 Disabled

4.2.8 FRINDEX Register

Add	0102Ch																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W																			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Symbol																			Frame Index[13:0]													
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:14]	–	Reserved. (Be sure to write 0b to this field.)
[13:0]	Frame Index[13:0]	This bit is incremented at the end of the microframe. The [N:3] indicates the current number of the frame list. (N is specified by the Frame List Size field (USBCMD Register bit[3:2].) This register can be accessed when the host controller is halted (USBSTS Register bit[12], HCHalted = 1b). The value of this register is reflected to the SOF number that is sent to the USB.

4.2.9 CTRLDSSEGMENT Register

Add	01030h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Symbol	CTRLDSSEGMENT[31:0]																															
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:0]	CTRLDSSEGMENT[31:0]	This register indicates 00000000h since this USB host controller does not support 64-bit addressing. Do not access this register via S/W.

4.2.10 PERIODICLISTBASE Register

Add	01034h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW												
Symbol	BaseAddress(Low)[31:12]																															
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:12]	BaseAddress(Low)[31:12]	The host controller implements a periodic schedule. The first address of a periodic list on the system memory is specified by S/W. The host controller determines a target frame list by this field and Frame Index field (FRINDEX Register). The periodic list address must be 4-kbyte aligned. Do not change this value during operation. If changed, the operation is not guaranteed.
[12:0]	–	Reserved. (Be sure to write 0b to this field.)

4.2.11 ASYNCLISTADDR Register

Add	01038h																															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW					
Symbol	Link Pointer Low[31:5] (LPL)																															
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:5]	Link Pointer Low[31:5] (LPL)	This field contains the memory address of the QH of the next asynchronous list to be processed. The asynchronous list address must be 32-byte aligned.
[4:0]	–	Reserved. (Be sure to write 0b to this field.)

4.2.12 CONFIGFLAG Register

Add	01060h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W																																RW
Symbol																																Configure Flag(CF)
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:1]	–	Reserved. (Be sure to write 0b to this field.)
0	Configure Flag(CF)	This bit is set to 1b by S/W at the end of the configuration of the host controller. This bit is used to control the port assignments. 1 Port assigned to EHCI 0 Port assigned to OHCI

4.2.13 PORTSC1 Register

Add	01064h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W										RW	RW	RW	RW	RW	RW	RW	R	R	RW		R	R		RW	RW	RW	RW		RW	RW	RW	R
Symbol										Wake on Over-current Enable(WKOC_E)	Wake on Disconnect Enable(WKDSCNNT_E)	Wake on Connect Enable(WKCNNT_E)	Port Test Control[3:0]				Port Indicator Control[1:0]		Port Owner		Line Status[1:0]			Port Reset	Suspend	Force Port Resume	Over-current Change		Port Enable/Disable Change	Port Enabled/Disabled	Connect Status Change	Current Connect Status
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:23]	–	Reserved. (Be sure to write 0b to this field.)
22	Wake on Over-current Enable (WKOC_E)	When set to 1b, an overcurrent state is detected as a wakeup event. Setting to this bit has no effect when the host controller is in operation. This bit indicates 0b when PP (bit[12]) = 0b.
21	Wake on Disconnect Enable (WKDSCNNT_E)	When set to 1b, a USB disconnection is detected as a wakeup event. Setting to this bit has no effect when the host controller is in operation. This bit indicates 0b when PP (bit[12]) = 0b.
20	Wake on Connect Enable (WKCNNT_E)	When set to 1b, a USB connection is detected as a wakeup event. The setting to this bit has no effect when the host controller is in operation. This bit indicates 0b when PP (bit[12]) = 0b.
[19:16]	Port Test Control[3:0]	Controls the test mode. For details of the test mode, refer to the USB2.0 Specification Chapter7.
[15:14]	Port Indicator Control[1:0]	Indicates 0b since this USB host controller does not support the Port Indicator Control. Writing to this bit has no effect.
13	Port Owner	This bit is set to 1b when CF = 0b and is cleared when the CF bit (CONFIGFLAG Register bit[0]) is changed from 0b to 1b. S/W sets this bit to 1b and passes the port ownership to OHCI when the connected device is not a HS device.
12	–	Reserved. (Be sure to write 0b to this field.)

Port Test Control[3:0]	Mode
0000b	Normal
0001b	Test_J
0010b	Test_K
0011b	Test_SE0_NAK
0100b	Test_Packet
0101b	Test_Force_Enable
Other	Reserved

<table>
<tr><td>[11:10]</td><td>Line Status[1:0]</td><td>This field indicates the D+/D- state of the USB bus. This bit indicates 0b when PP (bit[12]) = 0b.
When a HS device is connected:
<table>
<tr><th>bit11 (D+)</th><th>bit10 (D-)</th><th>Mode</th></tr>
<tr><td>0b</td><td>0b</td><td>Receiver squelched</td></tr>
<tr><td>0b</td><td>1b</td><td>J-State</td></tr>
<tr><td>1b</td><td>0b</td><td>K-State</td></tr>
<tr><td>1b</td><td>1b</td><td>Undefined</td></tr>
</table>
When a FS/LS device is connected:
<table>
<tr><th>bit11 (D+)</th><th>bit10 (D-)</th><th>Mode</th></tr>
<tr><td>0b</td><td>0b</td><td>SE0 or Open</td></tr>
<tr><td>0b</td><td>1b</td><td>Full-speed Device Attached</td></tr>
<tr><td>1b</td><td>0b</td><td>Low-speed Device Attached</td></tr>
<tr><td>1b</td><td>1b</td><td>Undefined</td></tr>
</table></td></tr>
<tr><td>9</td><td>–</td><td>Reserved. (Be sure to write 0b to this field.)</td></tr>
<tr><td>8</td><td>Port Reset</td><td>This bit is set to 1b from 0b when a 1b is written by S/W. When set to 1b, a reset operation defined by the USB 2.0 standard is started. Writing a 0b to this bit suspends the reset operation. According to the USB 2.0 standard, S/W must hold this bit a 1b until the sequence is completed.
Do not perform the reset operation when HCHalted = 1b (USBSTS Register bit[12]). This bit indicates 0b when PP (bit[12])= 0b.
<table>
<tr><td>1</td><td>Port is being reset</td></tr>
<tr><td>0</td><td>Port is not being reset</td></tr>
</table></td></tr>
<tr><td>7</td><td>Suspend</td><td>The port state is determined by this bit and the Port Enabled/Disabled bit (bit[2]) as shown below.
<table>
<tr><th>PortEnabled/Disabled bit</th><th>Suspend bit</th><th>Port state</th></tr>
<tr><td>0b</td><td>X</td><td>Disabled</td></tr>
<tr><td>1b</td><td>0b</td><td>Enabled</td></tr>
<tr><td>1b</td><td>1b</td><td>Suspend</td></tr>
</table>
In the Suspend state, downstream data transmission to a port is stopped. If this bit is set to 1b during a transfer, the state transition and transmission stop operation are performed after termination of the current transfer.
This bit is cleared to 0b when the Force Port Resume bit (bit[6]) is cleared to 0b by S/W or when the Port Reset bit (bit[8]) is set to 1b by S/W.
This bit indicates 0b when PP (bit[12])= 0b.
<table>
<tr><td>1</td><td>Port is in suspend state</td></tr>
<tr><td>0</td><td>Port is not in suspend state</td></tr>
</table></td></tr>
<tr><td>6</td><td>Force Port Resume</td><td>When a state transition from J to K (RemoteWakeUp) is detected in the Suspend state, the Port Change Detect bit (USBSTS Register, bit[2]) and this bit are set to 1b by the host controller. This bit is also set to 1b by S/W when a resume is notified. In this case, the Port Change Detect bit is not set.
When this bit is 1b, the resume signal (FS-J) is generated on the bus. This bit must be cleared by S/W after a certain period of time.
When this bit is 1b, writing a 0b returns the port to the HS idle state. After return, this bit is cleared to 0b automatically.
This bit indicates 0b when PP (bit[12])= 0b.
<table>
<tr><td>1</td><td>Port has detected/notified a resume</td></tr>
<tr><td>0</td><td>Port has not detected/notified a resume</td></tr>
</table></td></tr>
</table>

<table>
<tr><td>5</td><td>Over-current Change</td><td>This bit is set to 1b when an overcurrent state is detected. This bit is cleared when a 1b is written. Writing a 0b has no effect.<table><tr><td>1</td><td>Port changed to overcurrent state</td></tr><tr><td>0</td><td>No change</td></tr></table></td></tr>
<tr><td>4</td><td></td><td>Reserved (This bit needs to be set to 0b.)</td></tr>
<tr><td>3</td><td>Port Enable/Disable Change</td><td>This bit is set to 1b when the port is disabled by H/W. This bit is cleared when a 1b is written to this bit. Writing a 0b has no effect.
This bit indicates 0b when PP (bit[12])= 0b.<table><tr><td>1</td><td>Port enabled/disabled state changed</td></tr><tr><td>0</td><td>No change</td></tr></table></td></tr>
<tr><td>2</td><td>Port Enabled/Disabled</td><td>The host controller resets a port, enables the port if the connected device is a HS device, and sets this bit to 1b. This bit cannot be set to 1b from S/W.
The host controller disables the port when the port is disconnected or when an error occurs, and clears this bit to 0b. The port is also disabled when a 0b is written to this bit from S/W.
A write to this bit is not reflected until the port state is actually changed. When a port is disabled, downstream data transmission to the port is stopped. This bit indicates 0b when PP (bit[12])= 0b.<table><tr><td>1</td><td>Port enabled</td></tr><tr><td>0</td><td>Port disabled</td></tr></table></td></tr>
<tr><td>1</td><td>Connect Status Change</td><td>This bit indicates that the status of the Current Connect Status bit (bit[0]) has been changed. This bit is cleared when a 1b is written to this bit. Writing a 0b has no effect. This bit indicates 0b when PP (bit[12])= 0b.<table><tr><td>1</td><td>Current Connect Status changed</td></tr><tr><td>0</td><td>No change</td></tr></table></td></tr>
<tr><td>0</td><td>Current Connect Status</td><td>This bit indicates the current connection state of the port.
This bit indicates 0b when PP (bit[12])= 0b.<table><tr><td>1</td><td>Device is connected to the port</td></tr><tr><td>0</td><td>Device is not connected to the port</td></tr></table></td></tr>
</table>

4.3 OHCI PCI Configuration Registers

4.3.1 Offset 00h (Vendor ID, Device ID)

Add	10000h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Symbol	Device ID[15:0]																Vendor ID[15:0]															
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	1	1

Bit	Symbol	Description
[31:16]	DEVICE_ID[15:0]	Indicates the device type. This is used to select a driver that operates the device on PCI standard. This is not necessary for built-in host system.
[15:0]	VENDOR_ID[15:0]	Indicates the vendor of the device. This is used to select a driver that operates the device on PCI standard. This is not needed for the embedded host. When read, this field returns 1033h.

4.3.2 Offset 04h (Command, Status)

Add	10004h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R W	R W	R W	R W	R W	R	R	R W	R			R											R	R W	R	R W	R	R W	R	R W	R W	R
Symbol	Detected Parity Error	Signaled System Error	Received Master Abort	Received Target Abort	Signaled Target Abort	Devsel Timing[1:0]		Data Parity Error Detected	Fast Back to Back Capable			Capabilities List											Fast Back to Back Enable	SERR Enable	Wait Cycle Control	Parity Error Response	VGA Palette Snoop	Memory Write and Invalidate Enable	Special Cycle	Bus Master	Memory Space	I/O Space
R	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
31	Detected Parity Error	Parity error status bit This bit is set when an address error or data parity error occurs. This bit is cleared when a 1b is written from the PCI bus.
30	Signaled System Error	SERR status bit This bit is set when a system error occurs. This bit is cleared when a 1b is written from the PCI bus.
29	Received Master Abort	Master-Master Abort status bit This bit is set when a master operation is terminated by the master abort. This bit is cleared when a 1b is written from the PCI bus.
28	Received Target Abort	Master-Target Abort status bit This bit is set when a master operation is terminated by the target abort. This bit is cleared when a 1b is written from the PCI bus.
27	Signaled Target Abort	Slave-Target Abort status bit This bit is set when a slave operation is terminated by the target abort. This bit is cleared when a 1b is written from the PCI bus.
[26:25]	Devsel Timing[1:0]	Indicates the response time of DEVSEL. This bit is fixed to 01b (middle speed).
24	Data Parity Error Detected	This bit is set when a parity error occurs during a master operation. This bit is cleared when a 1b is written from the PCI bus. When the Parity Error Response bit (Command Register) is set to Disabled, this bit is fixed to 0b.
23	Fast Back to Back Capable	Indicates whether the fast back-to-back is supported. Fixed to 0b since the fast back-to-back is not supported.
[22:21]	–	Reserved. (Be sure to write 0b to this field.)
20	Capabilities List	Indicates that the Power Management mode is supported. Fixed to 1b.
[19:10]	–	Reserved. (Be sure to write 0b to this field.)
9	Fast Back to Back Enable	Fast Back-to-Back Enable bit This bit is fixed to 0b since the host controller does not support the fast back-to-back.

8	SERR Enable	SERR Enable bit When this bit is set to 1, a system error is transmitted by the SERR signal.
7	Wait Cycle Control	Wait Cycle Control Enable bit This bit is fixed to 0b since the host controller does not support the Address/Data Stepping.
6	Parity Error Response	Parity Error Response Enable bit When this bit is set to 1b, parity error check is performed.
5	VGA Palette Snoop	VGA Pallete Snoop Enable bit This bit is fixed to 0b since the host controller does not support the VGA Palette Snoop.
4	Memory Write and Invalidate Enable	Memory Write and Invalidate Enable bit This bit is fixed to 0b since the host controller does not support the Memory Write and Invalidate.
3	Special Cycle	Special Cycle Enable bit This bit is fixed to 0b since the host controller does not support the Special Cycle.
2	Bus Master	Bus Master Enable bit This bit enables a master access to the PCI bus. This bit must be set to 1b when accessing the SRAM of the system bus. This bit must be set at initialization of the host controller.
1	Memory Space	Memory Space Access Enable bit This bit enables a memory access on PCI standard. This bit must be set to 1b when performing a register access. This bit must be set at initialization of the host controller.
0	I/O Space	I/O Space Access Enable bit This bit is fixed to 0b since the host controller does not accept I/O access.

4.3.3 Offset 08h (Revision ID, Class Code)

Add	10008h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Symbol	Class Code																								Revision ID[7:0]							
	Base Class[7:0]								Sub Class[7:0]								Programming I/F[7:0]															
R	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0	1	0

Bit	Symbol	Description
[31:24]	Base Class[7:0]	Identifies the base class on PCI standard. Indicates 0Ch that is a serial peripheral bus controller.
[23:16]	Sub Class[7:0]	Identifies the sub class on PCI standard. Indicates 03h that is a USB device.
[15:8]	Programming I/F[7:0]	Identifies the programming interface on PCI standard. Indicates 10h that is the OHCI.
[7:0]	Revision ID[7:0]	Identifies the revision of the host controller. This field is fixed to 42h.

4.3.4 Offset 0Ch (Cache Line Size, Latency Timer, Header Type, BIST)

Add	1000Ch																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW	RW	RW
Symbol	BIST[7:0]								Header Type[7:0]								Latency Timer[7:0]								Cache Line Size[7:0]							
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0

Bit	Symbol	Description
[31:24]	BIST[7:0]	For self test. Indicates 00h.
[23:16]	Header Type[7:0]	This field is for reporting the header type to the system. The bit[22:16] is fixed to 0 since the header type is Type0, and the bit[23] is fixed to 0 since a multi-function device is not supported.
[15:8]	Latency Timer[7:0]	This field is for reporting the Latency Timer to the system. The lowest two bits are fixed to 00b.
[7:0]	Cache Line Size[7:0]	This field is for reporting the Cache Line Size to the system.

4.3.5 Offset 10h (OHCI Base Address)

Add	10010h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	R	R	R	R	R	R	R	R	R
Symbol	OHCI Base Address[31:4]																												Prefetchable	Type[1:0]		Memory Space Indicator
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:4]	OHCI Base Address [31:4]	The bit[31:12] identifies the address of the Operation register. Set the base address of the Operation register that is predefined by the system at initialization. The bit[11:4] is fixed to 00h.
3	Prefetchable	Indicates that the field specified by the base address is the memory space. This bit is fixed to 0b indicating that this field is not prefetchable.
[2:1]	Type[1:0]	Base address type field Indicates that the OHCI base address is an arbitrary position in the 32-bit space.
0	Memory Space Indicator	Indicates that the field specified by the base address is the memory space. Fixed to 0b.

4.3.6 Offset 2Ch (USB host controller Vendor ID, USB host controller ID)

Add	1002Ch																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Symbol	Subsystem ID[15:0]																Subsystem Vendor ID[15:0]															
R	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1	1	0	0	0	1	0	0	0	0	0	0	1	1	0	0	1	1

Bit	Symbol	Description
[31:16]	Subsystem ID[15:0]	Indicates the device type. This is used to select a driver that operates the device on PCI standard. This is not needed for the embedded host.
[15:0]	Subsystem Vendor ID[15:0]	Indicates the vendor of the device. This is used to select a driver that operates the device on PCI standard. This is not needed for the embedded host.

4.3.7 Offset 34h (Capability Pointer)

Add	10034h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W																									R	R	R	R	R	R	R	R
Symbol																									Capability Pointer[7:0]							
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit	Symbol	Description
[31:8]	–	Reserved.
[7:0]	Capability Pointer[7:0]	Points to the Capability Identifier. Indicates 40h since it is assigned to 40h in this core.

4.3.8 Offset 3Ch (Interrupt Line, Interrupt Pin, Min gnt, Max Latency)

Add	1003Ch																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW
Symbol	Max Latency[7:0]								Min Gnt[7:0]								Interrupt Pin[7:0]								Interrupt Line[7:0]							
R	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:24]	Max Latency[7:0]	Indicates the maximum latency. Fixed to 2Ah.
[23:16]	Min Gnt[7:0]	Indicates the minimum grant time. Fixed to 01h.
[15:8]	Interrupt Pin[7:0]	Indicates the interrupt output pin. Fixed to 01h indicating the INTA.
[7:0]	Interrupt Line[7:0]	Indicates the interrupt line. Do not change the default value ‘00h’.

4.3.9 Offset 40h (Capability Identifier, Next Item Pointer, Power Management Capabilities)

Add	10040h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Symbol	Power Management Capabilities																Next Item Pointer[7:0]								Capability Identifier[7:0]							
	PME Support[4:0]					D2 Support	D1 Support	AUX Current[2:0]			DSI		PME CLK	Version[2:0]																		
R	0	1	1	1	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Description
31	PME Support[4:0]	Indicates whether to support the D3 Cold state. This field is fixed to 0b since the D3 Cold state is not supported.
[30:27]		Indicates that the PME interrupt is supported in all the states (D0-D3) of the PCI power state. Fixed to 1111b.
26	D2 Support	Indicates that the PCI power state D2 is supported. Fixed to 1.
25	D1 Support	Indicates that the PCI power state D1 is supported. Fixed to 1.
[24:22]	Aux Current[2:0]	The PME interrupt from the D3 Cold state is not supported. Fixed to 000b.
21	DSI	Indicates that a specific initialization is not necessary on using power management. Fixed to 0b.
20	–	Reserved.
19	PME CLK	Indicates that the PCICLK is not necessary to generate the U2H_PME_INT interrupt. Fixed to 0b.
[18:16]	Version[2:0]	Indicates the version of the Power Management. This field is fixed to 010b indicating the implemented circuit structure in the host controller.
[15:8]	Next Item Pointer[7:0]	Indicates that the next item does not exist. Fixed to 00h.
[7:0]	Capability Identifier[7:0]	Indicates the Power Management Register ID. Fixed to 01h.

4.3.10 Offset 44h (Power Management Control/Status, PMCSR Bridge Support Extensions)

Add	10044h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	R	R	R	R	R	R	RW	R	R	R	R	R	R	RW	RW
Symbol	Data								PMCSR Bridge Support Extensions								Power Management Control/Status															
	Data[7:0]								BPCC Enable	B2_B3							PME Status	Data Scale[1:0]		Data Select[3:0]				PME Enable							Power State[1:0]	
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:24]	Data[7:0]	Indicates 00h. This field is optional on PCI standard and is not supported by the host controller.
23	BPCC Enable	Indicates 0b. This bit is for Bridge and is not supported by the host controller.
22	B2_B3	Indicates 0b. This bit is for Bridge and is not supported by the host controller.
[21:16]	–	Reserved. (Be sure to write 0b to this field.)
15	PME Status	Indicates the PME interrupt status. This bit is set to 1b when the PME interrupt condition is generated. This bit is cleared to 0b by writing 1b from the PCI bus.
[14:13]	Data Scale[1:0]	Indicates 00b. This field is optional on PCI standard and is not supported by the host controller.
[12:9]	Data Select[3:0]	Indicates 0h. This field is optional on PCI standard and is not supported by the host controller.
8	PME Enable	This bit specifies whether to use the external pin PME. When set to 1b, a PME interrupt is generated by a return from the Power Management.
[7:2]	–	Reserved. (Be sure to write 0b to this field.)
[1:0]	Power State[1:0]	Indicates the power status of the PCI. The corresponding states are as follows. 00b D0 State 01b D1 State 10b D2 State 11b D3 hot State

4.4 EHCI PCI Configuration Registers

4.4.1 Offset 00h (Vendor ID, Device ID)

Add	10100h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Symbol	Device ID[15:0]																Vendor ID[15:0]															
R	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	1	1

Bit	Symbol	Description
[31:16]	Device ID[15:0]	Indicates the devide type. This is used to select a driver that operates the device on PCI standard. This is not needed for the embedded host.
[15:0]	Vendor ID[15:0]	Indicates the vendor of the device. This is used to select a driver that operates the device on PCI standard. This is not needed for the embedded host.

4.4.2 Offset 04h (Command, Status)

Add	10104h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	RW	RW	RW	RW	RW	R	R	RW	R		R	R											R	RW	R	RW	R	RW	R	RW	RW	R
Symbol	Detected Parity Error	Signaled System Error	Received Master Abort	Received Target Abort	Signaled Target Abort	Devsel Timing[1:0]		Data Parity Error Detected	Fast Back to Back Capable		66MHz Capable	Capabilities List											Fast Back to Back Enable	SERR Enable	Wait Cycle Control	Parity Error Response	VGA Palette Snoop	Memory Write and Invalidate Enable	Special Cycle	Bus Master	Memory Space	I/O Space
R	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
31	Detected Parity Error	Parity error status bit This bit is set when an address error or data parity error occurs. This bit is cleared when a 1b is written from the PCI bus.
30	Signaled System Error	SERR status bit This bit is set when a system error occurs. This bit is cleared when a 1b is written from the PCI bus.
29	Received Master Abort	Master-Master Abort status bit This bit is set when a master operation is terminated by the master abort. This bit is cleared when a 1b is written from the PCI bus.
28	Received Target Abort	Master-Target Abort status bit This bit is set when a master operation is terminated by the target abort. This bit is cleared by writing a 1b from the PCI bus.
27	Signaled Target Abort	Slave-Target Abort status bit This bit is set when a slave operation is terminated by the target abort. This bit is cleared when a 1b is written from the PCI bus.
[26:25]	Devsel Timing[1:0]	Indicates the response time of the DEVSEL. This bit is fixed to 01b (middle speed).
24	Data Parity Error Detected	This bit is set when a parity error occurs during a master operation. This bit is cleared when a 1b is written from the PCI bus. When the Parity Error Response bit (Command Register) is set to Disabled, this bit is fixed to 0b.
23	Fast Back to Back Capable	Indicates whether the fast back-to-back is supported. Fixed to 0b since the fast back-to-back is not supported.
22	–	Reserved. (Be sure to write 0b to this field.)
21	66Mhz Capable	Indicates whether to be operatable at 66 MHz. Fixed to 0b since only 33 MHz is supported.
20	Capabilities List	Indicates that the Power Management mode is supported. Fixed to 1b.
[19:10]	–	Reserved. (Be sure to write 0b to this field.)
9	Fast Back to Back	Fast Back-to-Back Enable bit

	Enable	Fixed to 0b since the host controller does not support the fast back-to-back.
8	SERR Enable	SERR Enable bit Set to 1b to enable the SERR signal to report a system error.
7	Wait Cycle Control	Wait Cycle Control Enable bit This bit is fixed to 0b since the host controller does not support the Address/Data Stepping.
6	Parity Error Response	Parity Error Response Enable bit When this bit is set to 1b, parity error check is performed.
5	VGA Palette Snoop	VGA Palette Snoop Enable bit This bit is fixed to 0b since the host controller does not support the VGA Palette Snoop.
4	Memory Write and Invalidate Enable	Memory Write and Invalidate Enable bit This bit is fixed to 0b since the host controller does not support the Memory Write and Invalidate.
3	Special Cycle	Special Cycle Enable bit. This bit is fixed to 0b since the host controller does not support the Special Cycle.
2	Bus Master	Bus Master Enable bit This bit enables a master access to the PCI bus. This bit must be set to 1b when accessing the SRAM of the system bus. This bit must be set at initialization of the host controller.
1	Memory Space	Memory Space Access Enable bit This bit enables a memory access on PCI standard. This bit must be set to 1b when performing a register access. This bit must be set at initialization of the host controller.
0	I/O Space	I/O Space Access Enable bit This bit is fixed to 0b since the host controller does not accept I/O access.

4.4.3 Offset 08h (Revision ID, Class Code)

Add	10108h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Symbol	Class Code																								Revision ID[7:0]							
	Base Class[7:0]								Sub Class[7:0]								Programming I/F[7:0]															
R	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Description
[31:24]	Base Class[7:0]	Identifies the base class on PCI standard. Indicates 0Ch that is a serial peripheral bus controller.
[23:16]	Sub Class[7:0]	Identifies the sub class on PCI standard. Indicates 03h that is a USB device.
[15:8]	Programming I/F[7:0]	Identifies the programming interface on PCI standard. Indicates 20h that is the EHCI.
[7:0]	Revision ID[7:0]	Identifies the revision of the host controller. This field is fixed to 01h.

4.4.4 Offset 0Ch (Cache Line Size, Latency Timer, Header Type, BIST)

Add	1010Ch																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW	RW	RW
Symbol	BIST[7:0]								Header Type[7:0]								Latency Timer[7:0]								Cache Line Size[7:0]							
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:24]	BIST[7:0]	For self test. Indicates 00h.
[23:16]	Header Type[7:0]	This field is for reporting the header type to the system. The bit[22:16] is fixed to 0 since the header type is Type0, and the bit[23] is fixed to 0 since a multi-function device is not supported.
[15:8]	Latency Timer[7:0]	This field is for reporting the Latency Timer to the sytem. The lowest two bits are fixed to 00b.
[7:0]	Cache Line Size[7:0]	This field is for reporting the Cache Line Size to the system.

4.4.5 Offset 10h (EHCI Base Address)

Add	10110h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	R	R	R	R	R	R	R	R	R
Symbol	OHCI Base Address[31:4]																												Prefetchable	Type[1:0]		Memory Space Indicator
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:4]	EHCI Base Address [31:4]	The bit[31:8] identifies the address of the Operation register. Set the base adress of the Operation register that is predefined by the system at initialization. The bit[7:4] is fixed to 0h.
3	Prefetchable	Indicates that the field specified by the base address is the memory space. This bit is fixed to 0b indicating that the field is no prefetchable.
[2:1]	Type[1:0]	Base Address Type field Indicates that the EHCI base address is an arbitrary position in the 32-bit space.
0	Memory Space Indicator	Indicates that the field specified by the base address is the memory space. Fixed to 0b.

4.4.6 Offset 2Ch (USB host controller Vendor ID, USB host controller ID)

Add	1012Ch																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Symbol	Subsystem ID[15:0]																Subsystem Vendor ID[15:0]															
R	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	1	1

Bit	Symbol	Description
[31:16]	Subsystem ID[15:0]	Indicates the device type. This is used to select a driver that operates the device on PCI standard. This is not necessary for the built-in host system.
[15:0]	Subsystem Vendor ID [15:0]	Indicates the vendor of the device. This is used to select a driver that operates the device on PCI standard. This is not necessary for built-in host system.

4.4.7 Offset 30h (Expansion ROM Base Address)

Add	10130h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R										R
Symbol	Expansion ROM Base Address[21:0]																															ROM Decode Enable
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:10]	Expansion ROM Base Address[21:0]	This field always returns 000000h since a decoding of the expansion ROM is prohibited. Write access to this field is not possible.
[9:1]	–	Reserved.
0	ROM Decode Enable	This bit always returns 0b since decoding the expansion ROM is prohibited. Write access to this bit is not possible.

4.4.8 Offset 34h (Capability Pointer)

Add	10134h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W																									R	R	R	R	R	R	R	R
Symbol																									Capability Pointer[7:0]							
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit	Symbol	Description
[31:8]	–	Reserved.
[7:0]	Capability Pointer[7:0]	Points to the Capability Identifier. Indicates 40h since it is assigned to 40h in this core.

4.4.9 Offset 3Ch (Interrupt Line, Interrupt Pin, Min gnt, Max Latency)

Add	1013Ch																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW
Symbol	Max Latency[7:0]								Min Gnt[7:0]								Interrupt Pin[7:0]								Interrupt Line[7:0]							
R	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:24]	Max Latency[7:0]	Indicates the maximum latency. Fixed to 22h.
[23:16]	Min Gnt[7:0]	Indicates the minimum grant time. Fixed to 10h.
[15:8]	Interrupt Pin[7:0]	Indicates the interrupt output pin. Fixed to 02h indicating the INTB.
[7:0]	Interrupt Line[7:0]	Indicates the interrupt line. Do not change the default value ‘00h’.

4.4.10 Offset 40h (Capability Identifier, Next Item Pointer, Power Management Capabilities)

Add	10140h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Symbol	Power Management Capabilities																Next Item Pointer[7:0]								Capability Identifier[7:0]							
	PME Support[4:0]					D2 Support	D1 Support	AUX Current[2:0]			DSI		PME CLK	Version[2:0]																			
R	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Description
31	PME Support[4:0]	Indicates whether to support the D3 Cold state. This field is fixed to 0b since the D3 Cold state is not supported.
[30:27]		Indicates that the PME is supported in all the states (D0-D3) of the PCI power state. Fixed to 1111b.
26	D2 Support	Indicates that the PCI power state D2 is supported. Fixed to 1.
25	D1 Support	Indicates that the PCI power state D1 is supported. Fixed to 1.
[24:22]	Aux Current[2:0]	The PME interrupt from the D3 Cold state is not supported. Fixed to 000b.
21	DSI	Indicates that a specific initialization is not necessary for Power Management. Fixed to 0b.
20		Reserved
19	PME CLK	Indicates that the PCICLK is not necessary to generate the PME interrupt. Fixed to 0b.
[18:16]	Version[2:0]	Indicates the version of the Power Management. This field is fixed to 010b indicating the implemented circuit structure in the host controller.
[15:8]	Next Item Pointer[7:0]	Indicates that the next item does not exist. Fixed to 00h.
[7:0]	Capability Identifier[7:0]	Indicates the Power Management Register ID. Fixed to 01h.

4.4.11 Offset 44h (Power Management Control/Status, PMCSR Bridge Support Extensions)

Add	10144h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	R	R	R	R	R	R	RW	R	R	R	R	R	R	RW	RW
Symbol	Data								PMCSR Bridge Support Extensions								Power Management Control/Status															
	Data[7:0]								BPCC Enable	B2_B3							PME Status	Data Scale[1:0]		Data Select[3:0]				PME Enable							Power State[1:0]	
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:24]	Data[7:0]	Indicates 00h. This field is optional on PCI standard and is not supported by the host controller.
23	BPCC Enable	Indicates 0b. This bit is for Bridge and is not supported by the host controller.
22	B2_B3	Indicates 0b. This bit is for Bridge and is not supported by the host controller.
[21:16]	–	Reserved. (Be sure to write 0b to this field.)
15	PME Status	Indicates the PME interrupt status. This bit is set to 1b when the PME interrupt condition is generated. This bit is cleared to 0b by writing 1b from the PCI bus.
[14:13]	Data Scale[1:0]	Indicates 00b. This field is optional on PCI standard and is not supported by the host controller.
[12:9]	Data Select[3:0]	Indicates 0h. This field is optional on PCI standard and is not supported by the host controller.
8	PME Enable	This bit specifies whether to use the external pin PME. When set to 1b, a PME interrupt is generated by a return from the Power Management.
[7:2]	–	Reserved. (Be sure to write 0b to this field.)
[1:0]	Power State[1:0]	Indicates the power status of the PCI. The corresponding states are as follows. 00b D0 State 01b D1 State 10b D2 State 11b D3 hot State

4.4.12 Offset 60h (SBRN, FLADJ, PORTWAKECAP)

Add	10160h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW	R	R	R	R	R	R	R	R
Symbol	PORTWAKECAP[15:0]																FLADJ[7:0]								SBRN[7:0]							
R	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:16]	PORTWAKECAP[15:0]	This bit masks a port that is used as a wakeup event. This setting does not affect the operation of the host controller.
[15:8]	FLADJ[7:0]	Adjusts the frame length by the unit of 16-bit time. The default is 20h (60000d bit time).
[7:0]	SBRN[7:0]	Indicates the serial bus release number. Fixed to 20h.

4.4.13 Offset E8h (USBLEGSUP)

The host controller does not support the legacy function. Do not access this register.

4.4.13 Offset ECh (USBLEGCTLSTS)

The host controller does not support the legacy function. Do not access this register.

4.5 AHB-PCI Bridge PCI Configuration Registers

4.5.1 Offset 00h (Vendor ID, Device ID)

Add	10000h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Symbol	Device ID[15:0]																Vendor ID[15:0]															
R	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	1	1

Bit	Symbol	Description
[31:16]	Device ID[15:0]	Indicates the devide type. This is used to select a driver that operates the device on PCI standard. This is not needed for the embedded host.
[15:0]	Vendor ID[15:0]	Indicates the vendor of the device. This is used to select a driver that operates the device on PCI standard. This is not needed for the embedded host.

4.5.2 Offset 04h (Command, Status)

Add	10004h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	RW	RW	RW	RW	RW	R	R	RW	R		R	R											R	RW	R	RW	R	RW	R	RW	RW	R
Symbol	DETPERR	SIGSERR	REMABORT	RETABORT	SIGTABORT	DEVTIM[1:0]		MDPERR	FBTBCAP		66MCAP	CAPLIST											FBTBEN	SERREN	STEPCTR	PERREN	VGAPSNP	MWINVEN	SPECIALC	MASTEREN	MEMEN	IOEN
R	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
31	DETPERR	Parity error status bit This bit is set when an address error or data parity error is detected. This bit is cleared when a 1b is written. 1: Parity error detected 0: Parity error not detected
30	SIGSERR	SERR status bit This bit is set when a system error occurs. This bit is cleared when a 1b is written. 1: SERR# asserted 0: SERR# not asserted
29	REMABORT	Master Abort status bit This bit is set when a master abort is received. This bit is cleared when a 1b is written. 1: Master Abort received 0: Master Abort not received
28	RETABORT	Master Target Abort status bit This bit is set when a target abort is received. This bit is cleared when a 1b is written. 1: Target Abort received 0: Target Abort not received
27	SIGTABORT	Slave Target Abort status bit This bit is set when a target abort is sent. This bit is cleared when a 1b is written. 1: Target Abort transmitted 0: Target Abort not transmitted
[26:25]	DEVTIM[1:0]	Indicates the response time of the DEVSEL. This is set to 01b (medium mode).
24	MDPERR	This bit is set if a parity error is detected when acting as a master. This bit is cleared when a 1b is written. 1: Parity error detected 0: Parity error not detected
23	FBTBCAP	Indicates whether the fast back-to-back is supported. This bit is fixed to 0b. (Fast back-to-back is not supported.)
22	–	Reserved. (Be sure to write 0b to this field.)
21	66MCAP	Indicate whether the operation at 66 MHz is supported. This bit is fixed to 0b. (66 MHz operation is not supported.)
20	CAPLIST	Indicates whether the Capabilities List is supported. This bit is fixed to 0b.

		(Capability list is not supported.)
[19:10]	–	Reserved. (Be sure to write 0b to this field.)
9	FBTBEN	Fast Back-to-Back Enable bit This bit is fixed to 0b.
8	SERREN	Specifies the action to be taken when a system error occurs. Set this bit to 1b at initialization. 1: SERR# is asserted. 0: Error is ignored (default)
7	STEPCTR	Address Stepping Control bit This bit is fixed to 0b (Address Stepping not performed).
6	PERREN	Specifies the action to be taken when a parity error occurs. Set this bit to 1b at initialization. 1: Asserts the PERR#. 0: Ignores (default)
5	VGAPSNP	VGA Palette Snoop Enable bit This bit is fixed to 0b.
4	MWINVEN	Memory Write and Invalidate Enable bit This bit is fixed to 0b.
3	SPECIALC	Special Cycle Enable bit This bit is fixed to 0b.
2	MASTEREN	PCI Master Enable bit Set this bit to 1b at initialization. 1: Master operation enabled 0: Master operation disabled (default)
1	MEMEN	PCI Slave Enable bit Set this bit to 1b at initialization. 1: Memory cycle reception enabled 0: Memory cycle reception disabled (default)
0	IOEN	I/O Space Access Enable bit This bit is fixed to 0b.

4.5.3 Offset 08h (Revision ID, Class Code)

Add	10008h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Symbol	CLASS_CODE[23:0]																								REVISION_ID[7:0]							
R	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Description
[31:8]	CLASS_CODE[23:0]	Indicates 060000h.
[7:0]	REVISION_ID[7:0]	Indicates 01h.

4.5.4 Offset 0Ch (Cache Line Size, Latency Timer, Header Type, BIST)

Add	1000Ch																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	R	R	R	R	R
Symbol	BIST[7:0]								Header Type[7:0]								Latency Timer[7:0]								Cache Line Size[7:0]							
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:24]	BIST[7:0]	Indicates 00h (BIST not implemented).
[23:16]	HEADER_TYPE[7:0]	Indicates 00h (single function device).
[15:8]	LATENCY_TIMER[7:0]	This field is used to notify the system of the latency timer. Do not change the default value ‘00h’ (Latency timer not used).
[7:0]	CACHE_LINE_SIZE[7:0]	Indicates 00h (Cache not supported).

4.5.5 Offset 10h (AHB-PCI Bridge Base Address)

Add	10010h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW							R	R	R	R
Symbol	PCICOM_BASEADR[31:10]																												PREFETCH	TYPE[1:0]		MEM
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:10]	PCICOM_ BASEADR[31:10]	Specifies the base address of the AHB-PCI Bridge PCI Communication Register area. 1-Kbyte space is required. The upper 24 bits are the base address.
[9:4]	–	Reserved. (Be sure to write 0b to this field.)
3	PREFETCH	Enables or disables the data prefetch. This bit is fixed to 0b (data prefetch disabled).
[2:1]	TYPE[1:0]	Indicates the base address type. This bit indicates 00b (can be assigned to an arbitrary area in 4-Gbyte space).
0	MEM	Indicates that the field specified by the base address is memory space. This bit is fixed to 0b.

4.5.6 Offset 14h (PCI-AHB WIN1 Base Address)

Add	10010h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	RW	RW	RW	RW																									R	R	R	R
Symbol	PCI_WIN1_ BASEADR [31:28]																												PREFETCH	TYPE[1:0]		MEM
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit	Symbol	Description
[31:28]	PCI_WIN1_ BASEADR[31:28]	Specifies the base address of the PCI-AHB Window1. The upper 4 bits are the base address since a 256-Mbyte space is required.
[27:4]	–	Reserved. (Be sure to write 0b to this field.)
3	PREFETCH	Indicates whether prefetching is enabled or disabled. This bit is fixed to 1b (Prefetching enabled).
[2:1]	TYPE[1:0]	Indicates the Base Address Type. This bit is fixed to 00b (can be allocated to an arbitrary area in 4-Gbyte space).
0	MEM	Indicates that the field specified by the PCI_WIN1_BASEADR is a memory space. This bit is fixed to 0b.

4.5.7 Offset 2Ch (USB host controller Vendor ID, USB host controller ID)

Add	1002Ch																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Symbol	Subsystem ID[15:0]																Subsystem Vendor ID[15:0]															
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	1	1

Bit	Symbol	Description
[31:16]	SUBSYS_ID[15:0]	Indicates 0000h.
[15:0]	SUBSYS_VENDOR_ID[15:0]	Indicates 1033h.

4.5.8 Offset 3Ch (Interrupt Line, Interrupt Pin, Min gnt, Max Latency)

Add	1003Ch																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW
Symbol	Max Latency[7:0]								Min Gnt[7:0]								Interrupt Pin[7:0]								Interrupt Line[7:0]							
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:24]	MAX_LAT[7:0]	Indicates 00h (no request for frequency the bus use).
[23:16]	MIN_GNT[7:0]	Indicates 02h (latency timer request 16 burst).
[15:8]	INT_PIN[7:0]	Indicates 01h (INTA#).
[7:0]	INT_LINE[7:0]	Specifies the interrupt line. Do not change the default value ‘00h’.

4.6 AHB-PCI Bridge PCI Communication Registers

4.6.1 PCIAHB_WIN1_CTR Register

This register configures the settings necessary for the host controller to access the AHB.

Add	10800h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	RW	RW																						RW	RW	RW					RW	RW
Symbol	AHB_BASEADR[31:30]																							ENDIAN_CTR[2:0]							PREFETCH[1:0]	
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:30]	AHB_BASEADR[31:30]	Specifies a base address of the AHB side, which is used for the host controller to access the PCI-AHB Window1. The PCI-AHB Window1 is a 1-Gbyte area, and its upper 2 bits are the base address. For how to set the registers, refer to Chapter 5.
[29:9]	–	Reserved. (Be sure to write 0b to this field.)
[8:6]	ENDIAN_CTR[2:0]	Specifies the endian conversion method for the AHB side. In little-endian mode, do not change the default value '000b'. In big-endian mode, set to 010b at initialization, and do not change the value after that. 000b: No conversion 001b: Access type data swap 010b: Byte data swap 011b: Half word swap 100b: Address conversion other: Prohibited
[5:2]	–	Reserved. (Be sure to write 0b to this field.)
[1:0]	PREFETCH[1:0]	Enables or disables prefetching of the AHB, in response to a read request from the host controller. Set to 11b at initialization, and do not change the value after that. 00b: Prefetch disabled 01b: Prefetch enabled (Max 4 burst) 10b: Prefetch enabled (Max 8 burst) 11b: Prefetch enabled (Max 16 burst)

4.6.2 PCIAHB_WIN2_CTR Register

This register configures the settings necessary for the host controller to access the AHB.

Add	10804h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	RW	RW	RW	RW																				RW	RW	RW					RW	RW
Symbol	AHB_BASEADR[31:28]																							ENDIAN_CTR[2:0]							PREFETCH[1:0]	
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:28]	AHB_BASEADR[31:28]	Specifies a base address of the AHB side, which is used for the host controller to access the PCI-AHB Window1. The PCI-AHB Window1 is a 2-Gbyte area, and its upper 4 bits are the base address. For how to set the registers, refer to Chapter 5.
[27:9]	–	Reserved. (Be sure to write 0b to this field.)
[8:6]	ENDIAN_CTR[2:0]	Specifies the endian conversion method for the AHB side. In little-endian mode, do not change the default value '000b'. In big-endian mode, set to 010b at initialization, and do not change the value after that. 000b: No conversion 001b: Access type data swap 010b: Byte data swap 011b: Half word swap 100b: Address conversion other: Prohibited
[5:2]	–	Reserved. (Be sure to write 0b to this field.)
[1:0]	PREFETCH[1:0]	Enables or disables prefetching of the AHB, in response to a read request from the host controller. Set to 11b at initialization, and do not change the value after that. 00b: Prefetch disabled 01b: Prefetch enabled (Max 4 burst) 10b: Prefetch enabled (Max 8 burst) 11b: Prefetch enabled (Max 16 burst)

4.6.3 PCIAHB_DCT_CTR Register

This register configures the Discard timer for read access to the PCI-AHB Window1.

Add	10808h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W																	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW				RW
Symbol																	PCIAHB_DISCARD_TIMER[11:0]															DISCARD_EN
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bit	Symbol	Description
[31:16]	–	Reserved. (Be sure to write 0b to this field.)
[15:4]	PCIAHB_ DISCARD_TIMER[11:0]	Specifies a time to generate a timeout of the Discard timer. Do not change the default value ‘00Fh’ (256 times).
[3:1]	–	Reserved. (Be sure to write 0b to this field.)
0	DISCARD_EN	Enables or disables the Discard timer. Do not change the default value ‘0b’. 1 Discard timer enabled 0 Discard timer disabled

4.6.4 AHBPCI_WIN1_CTR Register

This register configures the settings necessary for access to the PCI Configuration Space.

Add	10810h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW			RW	RW	RW		RW	RW	RW	RW	
Symbol	PCIWIN1_BASEADR[31:11]																							ENDIAN_CTR[2:0]				CFGTYPE	PCICMD[2:0]			
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:11]	PCIWIN1_ BASEADR[31:11]	Specifies a base address of the PCI side, which is used for the AHB to access the AHB-PCI Window1 area. This setting is required for access to the PCI Configuration Space of the host controller and AHB-PCI Bridge. For how to set the resgister, refer to Chapter 5.
[10:9]	–	Reserved. (Be sure to write 0b to this field.)
[8:6]	ENDIAN_CTR[2:0]	Specifies the endian conversion method for the PCI side. Do not change the default value ‘000b’. 000b: No conversion 001b: Access type data swap 010b: Byte data swap 011b: Half word swap 100b: Address conversion Others: Prohibited
5	–	Reserved. (Be sure to write 0b to this field.)
4	CFGTYPE	Specifies the type of the PCI configuration cycle. Do not change the defalut value ’0b’. 1: TYPE1 0: TYPE0
[3:1]	PCICMD[2:0]	Specifies the PCI bus cycle type. Set to 101b at initialization, and do not change the value after that. 000b: Interrupt Acknowledge / Special Cycle 001b: IO Read / IO Write 011b: Memory Read / Memory Write 101b: Configuration Read / Configuration Write 110b: Memory Read Multiple / Memory Write 111b: Memory Read Line / Memory Write Others: Prohibited
0	–	Reserved. (Be sure to write 0b to this field.)

4.6.5 AHBPCI_WIN2_CTR Register

This register configures the settings necessary for access to the OHCI Operation Registers.

Add	10814h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW								RW	RW	RW	RW		RW	RW	RW	RW
Symbol	PCIWIN2_BASEADR[31:16]																							ENDIAN_CTR[2:0]			BURST_EN		PCICMD[2:0]			PREFETCH
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit	Symbol	Description
[31:16]	PCIWIN2_ BASEADR[31:16]	Specifies a base address of the PCI side, which is used for the AHB to access the AHB-PCI Window2 area. This register is used to access the OHCI Operation register area. For how to set the registers, refer to Chapter 5.
[15:9]	–	Reserved. (Be sure to write 0b to this field.)
[8:6]	ENDIAN_CTR[2:0]	Specifies the endian conversion method for the PCI side. Do not change the default value ‘000b’. 000b: No conversion 001b: Access type data swap 010b: Byte data swap 011b: Half word swap 100b: Address conversion Others: Prohibited
5	BURST_EN	Enables a burst transfer to the PCI bus. Set to 0b at initialization, and do not change the value after that. 1: Burst enabled 0: Burst disabled
4	–	Reserved. (Be sure to write 0b to this field.)
[3:1]	PCICMD[2:0]	Specifies the PCI bus cycle type. Set to 011b at initialization, and do not change the value after that. 001b: IO Read / IO Write 011b: Memory Read / Memory Write 110b: Memory Read Multiple / Memory Write 111b: Memory Read Line / Memory Write Others: Prohibited
0	PREFETCH	Enables or disables the prefetching to a burst read transfer request of the AHB side. Do not change the default value ’0b’. 1: Prefetch enabled 0: Prefetch disabled

4.6.6 AHBPCI_DCT_CTR Register

This register configures the Discard timer on the PCI bus for access to the AHB-PCI Window1 and 2.

Add	1081Ch																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W																	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW				RW
Symbol																	AHBPCI_DISCARD_TIMER[11:0]															DISCARD_EN
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bit	Symbol	Description
[31:16]	–	Reserved. (Be sure to write 0b to this field.)
[15:4]	AHBPCI_ DISCARD_TIMER[11:0]	Specifies a retry time to generate a timeout of the Discard timer. Do not change the default value ‘00Fh’ (256 times).
[3:1]	–	Reserved. (Be sure to write 0b to this field.)
0	DISCARD_EN	Enables or disables the Discard timer. Do not change the default value ’0b’. 1 Discard timer enabled 0 Discard timer disabled

4.6.7 PCI_INT_ENABLE Register

This register enables or disables the interrupts of the PCI_INT_STATUS register individually. When disabled the interrupt signal is not asserted when the interrupt occurs and its corresponding bit of the PCI_INT_STATUS register is set to 1b.

Add	10820h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W													RW		RW	RW		RW	RW	RW			RW	RW			RW	RW	RW	RW	RW	RW
Symbol													USBH_PMEEN		USBH_INTBEN	USBH_INTAEN		AHBPCI_WIN_INTEN	PCIAHB_WIN2_INTEN	PCIAHB_WIN1_INTEN			DMA_AHBPCI_INTEN	DMA_PCIAHB_INTEN			RESERR_INTEN	SIGSERR_INTEN	PERR_INTEN	REMABORT_INTEN	RETABORT_INTEN	SIGTABORT_INTEN
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:20]	–	Reserved. (Be sure to write 0b to this field.)
19	USBH_PMEEN	PCI_INT_STATUS bit19 USBH_PME interrupt enable 1 Interrupt enabled 0 Interrupt disabled
18	–	Reserved. (Be sure to write 0b to this field.)
17	USBH_INTBEN	PCI_INT_STATUS bit17 USBH_INTB interrupt enable 1 Interrupt enabled 0 Interrupt disabled
16	USBH_INTAEN	PCI_INT_STATUS bit16 USBH_INTA interrupt enable 1 Interrupt enabled 0 Interrupt disabled
15	–	Reserved. (Be sure to write 0b to this field.)
14	AHBPCI_WIN_INTEN	PCI_INT_STATUS bit14 AHBPCI_WIN_INT interrupt enable Do not change the default value '0b'. 1 Interrupt enabled 0 Interrupt disabled
13	PCIAHB_WIN2_INTEN	PCI_INT_STATUS bit13 PCIAHB_WIN2_INT interrupt enable Do not change the default value '0b'. 1 Interrupt enabled 0 Interrupt disabled
12	PCIAHB_WIN1_INTEN	PCI_INT_STATUS bit12 PCIAHB_WIN1_INT interrupt enable 1 Interrupt enabled 0 Interrupt disabled
[11:10]	–	Reserved. (Be sure to write 0b to this field.)
9	DMA_AHBPCI_INTEN	PCI_INT_STATUS bit9 DMA_AHBPCI_INT interrupt enable Do not change the default value '0b'. 1 Interrupt enabled

		0 Interrupt disabled
8	DMA_PCIAHB_INTEN	PCI_INT_STATUS bit8 DMA_PCIAHB_INT interrupt enable Do not change the default value '0b'. 1 Interrupt enabled 0 Interrupt disabled
[7:6]	–	Reserved. (Be sure to write 0b to this field.)
5	RESERR_INTEN	PCI_INT_STATUS bit5 RESERR_INT interrupt enable 1 Interrupt enabled 0 Interrupt disabled
4	SIGSERR_INTEN	PCI_INT_STATUS bit4 SIGSERR_INT interrupt enable 1 Interrupt enabled 0 Interrupt disabled
3	PERR_INTEN	PCI_INT_STATUS bit3 PERR_INT interrupt enable 1 Interrupt enabled 0 Interrupt disabled
2	REMABORT_INTEN	PCI_INT_STATUS bit2 REMABORT_INT interrupt enable 1 Interrupt enabled 0 Interrupt disabled
1	RETABORT_INTEN	PCI_INT_STATUS bit1 RETABORT_INT interrupt enable 1 Interrupt enabled 0 Interrupt disabled
0	SIGTABORT_INTEN	PCI_INT_STATUS bit0 SIGTABORT_INT interrupt enable 1 Interrupt enabled 0 Interrupt disabled

4.6.8 PCI_INT_STATUS Register

This register indicates the status of the interrupt source of the AHB-PCI Bridge. It also indicates the status of the interrupt signals from the host controller.

Add	10824h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W													R		R	R		RW	RW	RW			RW	RW			RW	RW	RW	RW	RW	RW
Symbol													USBH_PME		USBH_INTB	USBH_INTA		AHBPCI_WIN_INT	PCIAHB_WIN2_INT	PCIAHB_WIN1_INT			DMA_AHBPCI_INT	DMA_PCIAHB_INT			RESERR_INT	SIGSERR_INT	PERR_INT	REMABORT_INT	RETABORT_INT	SIGTABORT_INT
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:20]	–	Reserved. (Be sure to write 0b to this field.)
19	USBH_PME	Indicates the status of the PME interrupt that is generated by the host controller. Clear the interrupt on the host controller side. 1: PME interrupt occurred 0: PME interrupt not occurred
18	–	Reserved. (Be sure to write 0b to this field.)
17	USBH_INTB	Indicates the status of the INTB interrupt that is generated by the host controller. Clear the interrupt on the host controller side. 1: INTB interrupt occurred 0: INTB interrupt not occurred
16	USBH_INTA	Indicates the status of the INTA interrupt that is generated by the host controller. Clear the interrupt on the host controller side. 1: INTA interrupt occurred 0: INTA interrupt not occurred
15	–	Reserved. (Be sure to write 0b to this field.)
14	AHBPCI_WIN_INT	Interrupt is not generated by this function.
13	PCIAHB_WIN2_INT	Indicates that the AHB error has occurred in the PCIAHB_Window2. This bit is cleared when a 1b is written. 1: AHB error has occurred 0: AHB error has not occurred
12	PCIAHB_WIN1_INT	Indicates that the AHB error has occurred in the PCIAHB_Window1. This bit is cleared when a 1b is written. 1: AHB error has occurred 0: AHB error has not occurred
[11:10]	–	Reserved. (Be sure to write 0b to this field.)
9	DMA_AHBPCI_INT	Interrupt is not generated by this function.
8	DMA_PCIAHB_INT	Interrupt is not generated by this function.
[7:6]	–	Reserved. (Be sure to write 0b to this field.)

5	RESERR_INT	Indicates the status of the interrupt that is generated by the SERR# input. This bit is cleared when a 1b is written. 1: SERR# is asserted 0: SERR# is not asserted
4	SIGSERR_INT	Indicates the status of the interrupt that is generated by the SERR# output. This bit is cleared when a 1b is written. 1: SERR# is asserted 0: SERR# is not asserted
3	PERR_INT	Indicates the status of the interrupt that is generated by the PERR# input/output. This bit is cleared when a 1b is written. 1: PERR# is asserted 0: PERR# is not asserted
2	REMABORT_INT	Indicates a master abort has been received during operation as a PCI master. This bit is cleared when a 1b is written. 1: Master abort received 0: Master abort not received
1	RETABORT_INT	Indicates that a target abort has been received during operation as a PCI master. This bit is cleared when a 1b is written. 1: Target abort received 0: Target abort not received
0	SIGTABORT_INT	Indicates that a target abort has been notified during operation as a PCI target. This bit is cleared when a 1b is written. 1: Target abort notified 0: Target abort not notified

4.6.9 AHB_BUS_CTR Register

This register configures the AHB Master/Slave function.

Add	10830h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W															R W	R W									R W	R W	R W	R W	R W	R W	R W	R W
Symbol															SMODE_READY_CTR	SMODE_READ_BURST									MMODE_HBUSREQ	MMODE_BOUNDARY[1:0]		MMODE_BURST_WIDTH[1:0]		MMODE_WR_INCR	MMODE_BYTE_BURST	MMODE_HTRANS
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:18]	–	Reserved. (Be sure to write 0b to this field.)
17	SMODE_READY_CTR	Controls the wait operation of the AHB slave. Set this bit to 0b when the Retry/Sprit is used. Do not change the value after initialization. 1: Wait control is performed by SHREADY = 0b 0: Wait control is performed by SHRESP = RETRY
16	SMODE_READ_BURST	Determines whether the data are retained when the cycle is divided during a fixed-length burst transfer in AHB slave read cycles. Do not change the default value ‘0b’. 1: Data are discarded 0: Data are retained
[15:8]	–	Reserved. (Be sure to write 0b to this field.)
7	MMODE_HBUSREQ	Specifies the deasserting timing of the MHBUSREQ when operating as an AHB master. Set to 1b at initialization, and do not change the value after that. 1: Deasserted at the first MHGRANT = 1b and MHREADY = 1b 0: Deasserted at the last address phase of the cycle
[6:5]	MMODE_BOUNDARY[1:0]	Specifies a boundary of burst transfer when operating as an AHB master. Set to 00b at initialization, and do not change the value after that. 00b: 1 Kbyte 01b: Address = 3Fh 10b: Address = 7Fh 11b: Prohibited
[4:3]	MMODE_ BURST_WIDTH [1:0]	Specifies the maximum number of beat count in burst transfer when operating as an AHB master. Do not change the default value ‘00b’. 00b: Max 16 beat transfer 01b: Max 8 beat transfer 10b: Max 4 beat transfer

		11b: Single transfer
2	MMODE_WR_INCR	Specifies the condition of the undefined length burst transfer in a write transfer when operating as an AHB master. Set to 1b at initialization, and do not change the value after that. 1: INCR is used when the remaining is 2 to 3 beat. INCR4, 8, or 16 is used. 0: INCR is used except for 4-, 8-, and 16-beat transfer
1	MMODE_BYTE_BURST	Enables or disables the 16-bit/8-bit burst transfer of the AHB master. Set to 1b at initialization, and do not change the value after that. 1: 16-bit/8-bit burst transfer disabled 0: 16-bit/8-bit burst transfer enabled
0	MMODE_HTRANS	Specifies the operation mode of the MHTRANS signal in the operation of AHB master. Set to 1b at initialization, and do not change the value after that. 1: When cycle is divided, add IDLE and request a bus with MHBUSREQ 0: When cycle is divided, output NONSEQ consecutively

4.6.10 USBCTR Register

This register configures the USB host controller.

Add	10834h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W																					RW	RW	RW	RW					RW	RW	RW	RW
Symbol																					TEMP0[2:0]			DIRPD					TEMP1[1:0]		PCICLK_MASK	USBH_RST
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1

Bit	Symbol	Description
[31:12]	–	Reserved. (Be sure to write 0b to this field.)
[11:9]	TEMP0[2:0]	Temporary register. The default is 0b. Do not change the default value.
8	DIRPD	When set to 1b, the direct power-down state is selected. The direct power-down can be also enabled from the DIRPD input pin. 1: Direct powerdown state 0: Normal operation
[7:4]	–	Reserved. (Be sure to write 0b to this field.)
[3:2]	TEMP1[1:0]	Temporary register. The default is 1b. Do not change the default value.
1	PCICLK_MASK	When set to 1, the PCI clock output is stopped. Note that the host controller becomes inaccessible when this bit is set to 1b. 1: PCI clock stopped 0: PCI clock supplied
0	USBH_RST	Controls the reset signal that is supplied to the host controller. Access to the host controller becomes effective in 3CLK@PCICLK after reset cancel. 1: Host contoller reset 0: Host contoller reset cancel

4.6.11 PCI_ARBITER_CTR Register

This register configures the arbitration function of the PCI bus.

Add	10840h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W									RW	RW	RW	RW	RW	RW	RW	RW				RW					RW	RW	RW	RW	RW	RW	RW	RW
Symbol									PCIBUS_PARK_TIMER [7:0]											PCIBP_MODE					PCIREQ7	PCIREQ6	PCIREQ5	PCIREQ4	PCIREQ3	PCIREQ2	PCIREQ1	PCIREQ0
R	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Description
[31:24]	–	Reserved. (Be sure to write 0b to this field.)
[23:16]	PCIBUS_ PARK_TIMER[7:0]	Specifies the Parking timer value of the PCI bus. Do not change the default value ‘07h’.
[15:13]	–	Reserved. (Be sure to write 0b to this field.)
12	PCIBP_MODE	Specifies the PCI bus parking master. Set this bit to 1b at initialization, and do not change the value after that. 1: Last accessed master is the bus parking master 0: This unit is the bus parking master
[11:8]	–	Reserved. (Be sure to write 0b to this field.)
7	PCIREQ7	This function is not used. Do not change the default value ‘0b’.
6	PCIREQ6	This function is not used. Do not change the default value ‘0b’.
5	PCIREQ5	This function is not used. Do not change the default value ‘0b’.
4	PCIREQ4	This function is not used. Do not change the default value ‘0b’.
3	PCIREQ3	This function is not used. Do not change the default value ‘0b’.
2	PCIREQ2	This function is not used. Do not change the default value ‘0b’.
1	PCIREQ1	Enables or disables the PCI bus request signal from the host controller. Set to 1b at initialization, and do not change the value after that. 1: Request signal enabled 0: Request signal disabled
0	PCIREQ0	Enables or disables the PCI bus request signal of this unit. Set to 1b at initialization, and do not change the value after that. 1: Request signal enabled 0: Request signal disabled

4.6.12 PCI_UNIT_REV Register

This register indicates the version of the AHB-PCI Bridge macro.

Add	10848h																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Symbol	Major Revision ID[15:0]																Minor Revision ID[15:0]															
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1

Bit	Symbol	Description
[31:16]	Major Revision ID [15:0]	Indicates the Major Revision ID of this unit.
[15:0]	Minor Revision ID [15:0]	Indicates the Minor Revision ID of this unit.

5. Accessing Registers

Access to the host controller is performed via the internal PCI bus. To perform the access properly, the AHB memory space and the PCI memory space need to be mapped into the USB host controller correctly.
The PCI has a PCI Configuration Space and a PCI Memory Space. The PCI configuration space configures the PCI transfer and defines the PCI base address, and the PCI memory space performs data transfer.

Access from the AHB to the host and master access from the host to the AHB are performed through the window areas of the AHBPCI Bridge. The relation between the register area and window area is described in Figure 5-1. AHB and PCI Space Mappingand Table 5-1. AHB Area Description

Figure 5-1. AHB and PCI Space Mapping

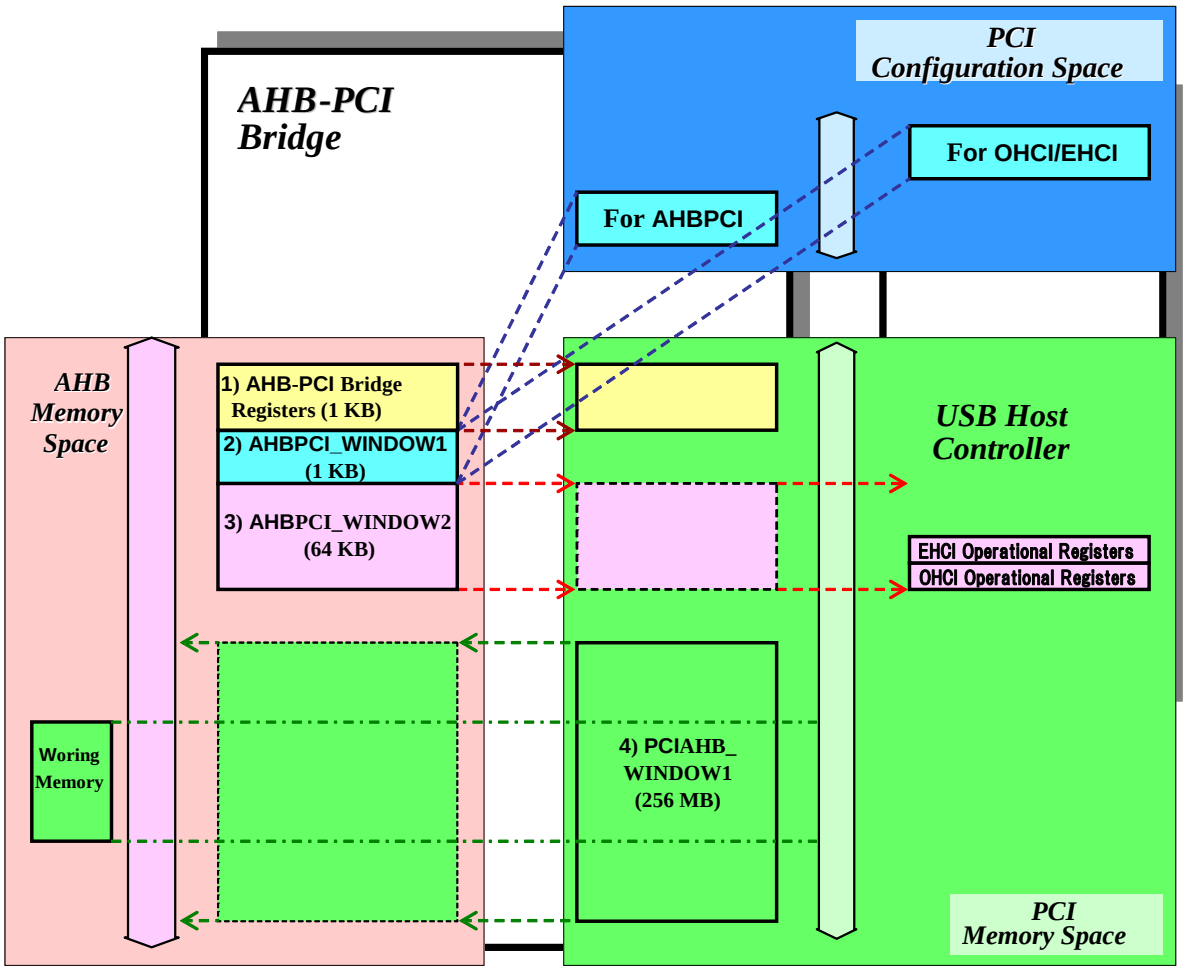


Table 5-1. AHB Area Description

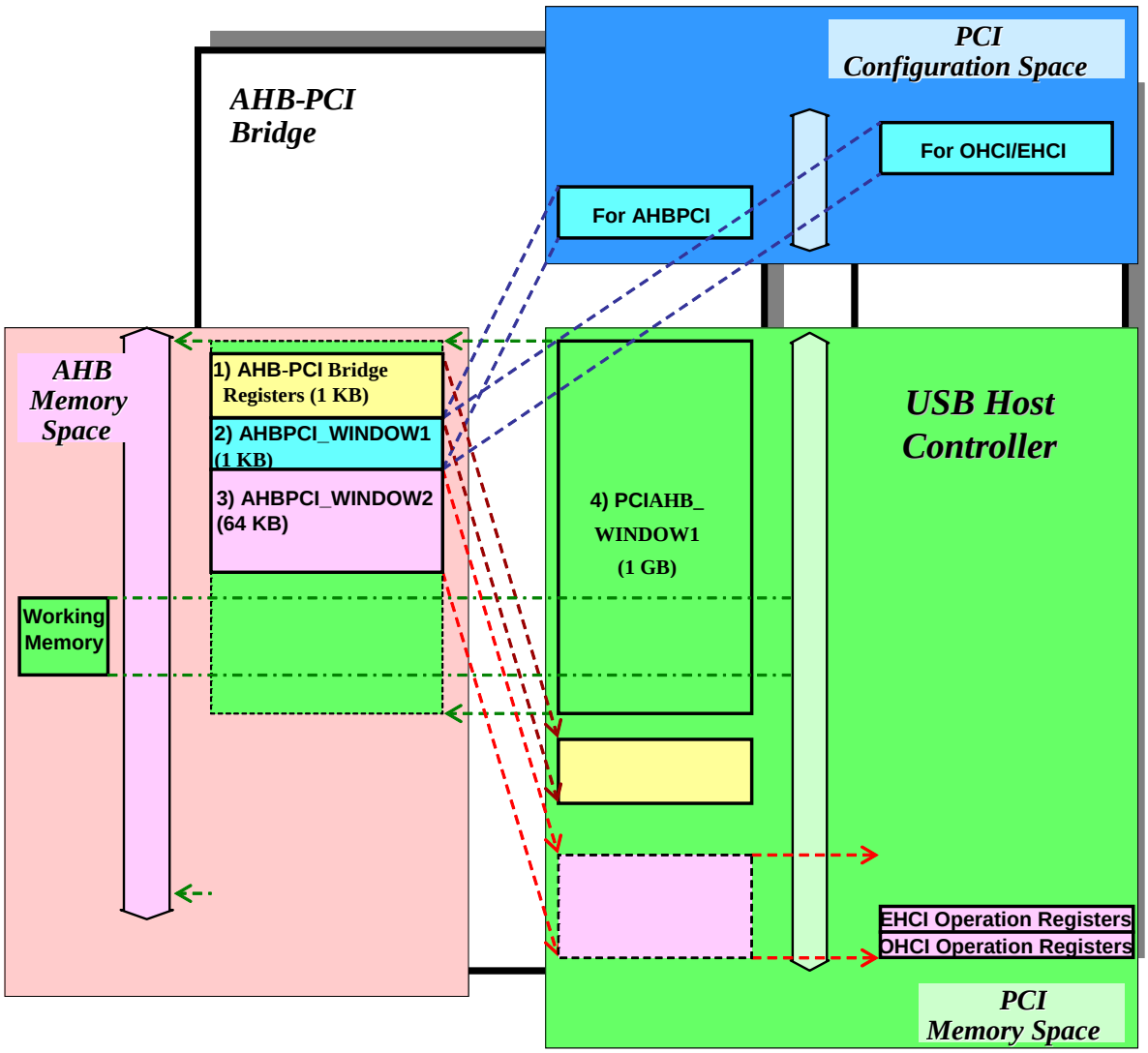
AHB area name	Size	Description
1) AHBPCI Communication Registers	1 KB	Used for various settings for AHB, including the base address of each Window area. This area is also mapped into the PCI memory space. Care should be taken not to overlap this area and other areas when mapping.
2) AHBPCI_WINDOW1	1 KB	Access to the PCI Configuration Space is performed through this area. The access is allocated to the OHCI Configuration Register, EHCI PCI Configuration Register, or AHB-PCI Bridge PCI Configuration Register by the AHBPCI_WIN1_CTR register.
3) AHBPCI _WINDOW2	64 KB	Access to the OHCI Operation Register and EHCI Operation Register is performed through this area.
4) PCIAHB_WINDOW1	1 GB	The host controller accesses the AHB working memory through this area.
5) PCIAHB_WINDOW2	256 MB	The host controller accesses the AHB working memory through this area.

Care should be taken not to overlap the following areas on the PCI memory space when mapping.

- PCIAHB_WINDOW1 (1 GB) and PCIAHB_WINDOW2 (256 MB)
- OHCI Operation Register, EHCI Operation Register, and AHB-PCI Bridge PCI Communication Register

The AHB memory space and PCI memory space are mapped in the same address in general. If the above overlapping occurs, use the PCI configuration register (OHCI Base Address, EHCI Base Address, AHB-PCI Bridge Base Address) to define the base address, avoiding overlapping of the the PCIAHB_WINDOW1 and PCIAHB_WINDOW2. Figure 5-2. AHB and PCI Space Mapping (Area Overlapped)shows the mapping image of overlapped memory space.

Figure 5-2. AHB and PCI Space Mapping (Area Overlapped)



The registers required for mapping the AHB space and PCI space are listed in Table 5-2. Address Setting Registers Table 5-3. Example of Addressingshows the relation of those registers and AHB and PCI space.

Figure 5-3. Relation of Address Registers and AHB/PCI Space Mapping

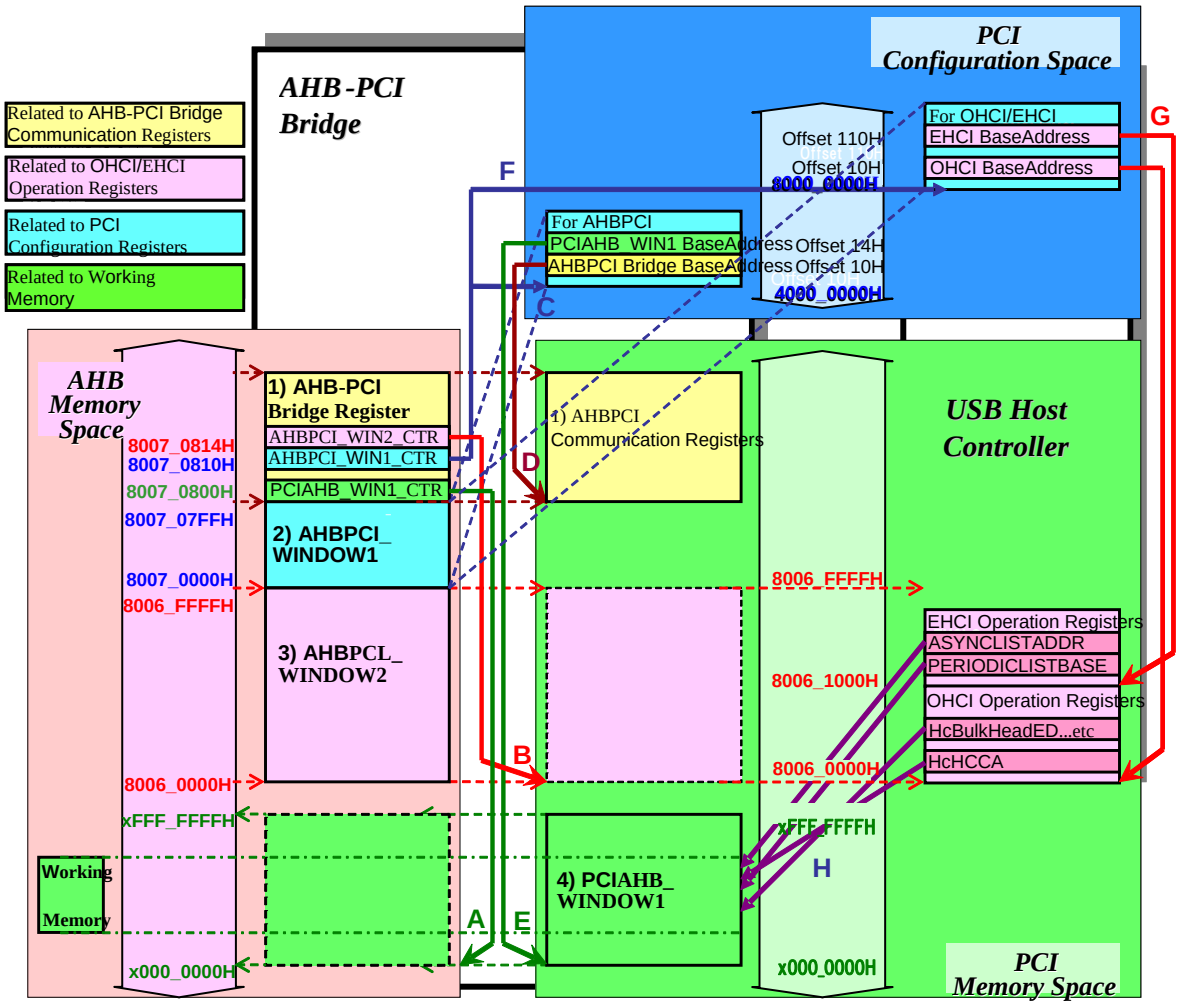


Table 5-2. Address Setting Registers

AHB area name	Description
A: PCIAHB_WIN1_CTR	When the host controller accesses the PCIAHB_WINDOW1 as a master, AHB address is converted into the base address defined by this register. The working memory to use is included in general.
B: AHBPCI_WIN2_CTR	When the AHBPCI_WINDOW2 is accessed, PCI address is converted into the base address defined by this register. The same value as the AHBPCI_WINDOW2 can be set in general. Avoid overlapping of the area (256 MB including a working memory) that is set by A.
C: AHBPCI_WIN1_CTR	When the base address is set to 4000_0000h in this register, access to the AHB-PCI Bridge PCI configuration register is performed.
D: AHBPCI Bridge Base Address	Sets the base address of the AHB-PCI Bridge on the PCI space. This register is not accessed from PCI side; however, avoid overlapping of other areas.
E: PCIAHB_WIN1 Base Address	Sets the base address of the PCIAHB_WINDOW1 area on thePCI space. The same base address as A is set in general.
F: AHBPCI_WIN1_CTR	When the base address is set to 8000_0000h in this register, access to the OHCI/EHCI PCI configuration register is performed.
G: OHCI Base Address and EHCI Base Address	Sets the base address of the OHCI and EHCI operation registers on the PCI space. The base address of the OHCI operation register is the same as B in general, and the base address of the EHCI operation register is the base address of B + offset 1000h.
H: Various OHCI/EHCI operation registers	When the settings A to G are complete, the host controller can access the data (e.g., descriptor) in the AHB working memory via PCI. The addresses of data that reside in the working memory are specified by the following registers. OHCI/EHCI Operation Register - HcHCCA Register - HcPeriodicCurrentED Register - HcControlHeadED Register - HcControlCurrentED Register - HcBulkHeadED Register - HcBulkCurrentED Register - HcDoneHead Register EHCI Operation Register - PERIODICLISTBASE Register - ASYNCLISTADDR Register

Table 5-3. Example of Addressing

AHB area name	Description
PCIAHB_WIN1_CTR	0x40000003
PCIAHB_WIN2_CTR	0xF0000003
AHBPCI_WIN2_CTR	0xE2700006
AHBPCI_WIN1_CTR	0x4000000A
PA_BASEAD	0xE2710800
PA_WIN1_BASEAD	0x40000000
PA_WIN2_BASEAD	0xF0000000
AHBPCI_WIN1_CTR	0x8000000A
PO_BASEAD	0xE2700000
PE_BASEAD	0xE2701000

5.1 Access to PCI Configuration Space

Prior to accessing the PCI configuration space, the AHBPCI_WIN1_CTR register must be set properly. For the parameters, refer to the table below. Access to the PCI configuration space is performed through the AHB-PCI Window1 area (10000h to 107FFh, 2 Kbytes).

Table 5-4. Parameter Setting for Access to PCI Configuration Space

Targer area	AHBPCI_WIN1_CTR Register		
	PCIWIN1_BASEADR [31:11]	PCICMD[2:0]	CFGTYPE
OHCI PCI Configuration Register EHCI PCI Configuration Register	bit[31] = 1b	101b	0b
AHB-PCI BridgePCI Configuration Register	bit[30] = 1b		

5.2 Access to OHCI and EHCI Operation Registers

Prior to accessing the OHCI Operation and EHCI Operation Registers, the following registers must be set in addition to mapping PCI address spaces. For the parameters, refer to the table below.

- OHCI PCI Configuration Register
- EHCI PCI Configuratin Fegister
- AHBPCI_WIN2_CTR Register

Table 5-5. Parameter Setting for Access to OHCI/EHCI Operation Registers

Register	Description
OHCI/EHCI PCI Configuration Register, Offset 04h, PCI Command	Memory Space (bit[1]) = 1b
AHBPCI_WIN2_CTR Register	PCICMD [2:0] = 011b (Memory Read/Memory Write)

6. Clock System

6.1 Externally Supplied Clocks

The USB function controller requires the following clocks to be supplied externally:

Table 6-1. Externally Supplied Clocks

Clock Signal	Description	Restriction on Frequency
USB0_CLK	AHB clock	Durin communication: PCICLK < USB0_CLK ≦133 MHz During non-communication: 0 ≦ USB0_CLK ≦133 MHz
PMCLK	AHB clock for power management	PMCLK = USB0_CLK
OSC1_CLK	USB reference clock	24 MHz
PCICLK	Subsysten internal PCI clock	33.33 MHz ≧ PCICLK ≧ 25 MHz

The clocks are described below.

- USB0_CLK

The USB0_CLK is a clock signal that is supplied to the AHB-PCI briedge. The AHB clock is connected. When the USB function is not used, the USB0_CLK clock can be stopped to lower power consumption. Dynamic control of the USB0_CLK except for clock stop is not supported.

- OSC1_CLK

The OSC1_CLK is a reference clock that is used to generate clock for USB transfer. 24-MHz clock is used.

- PCICLK

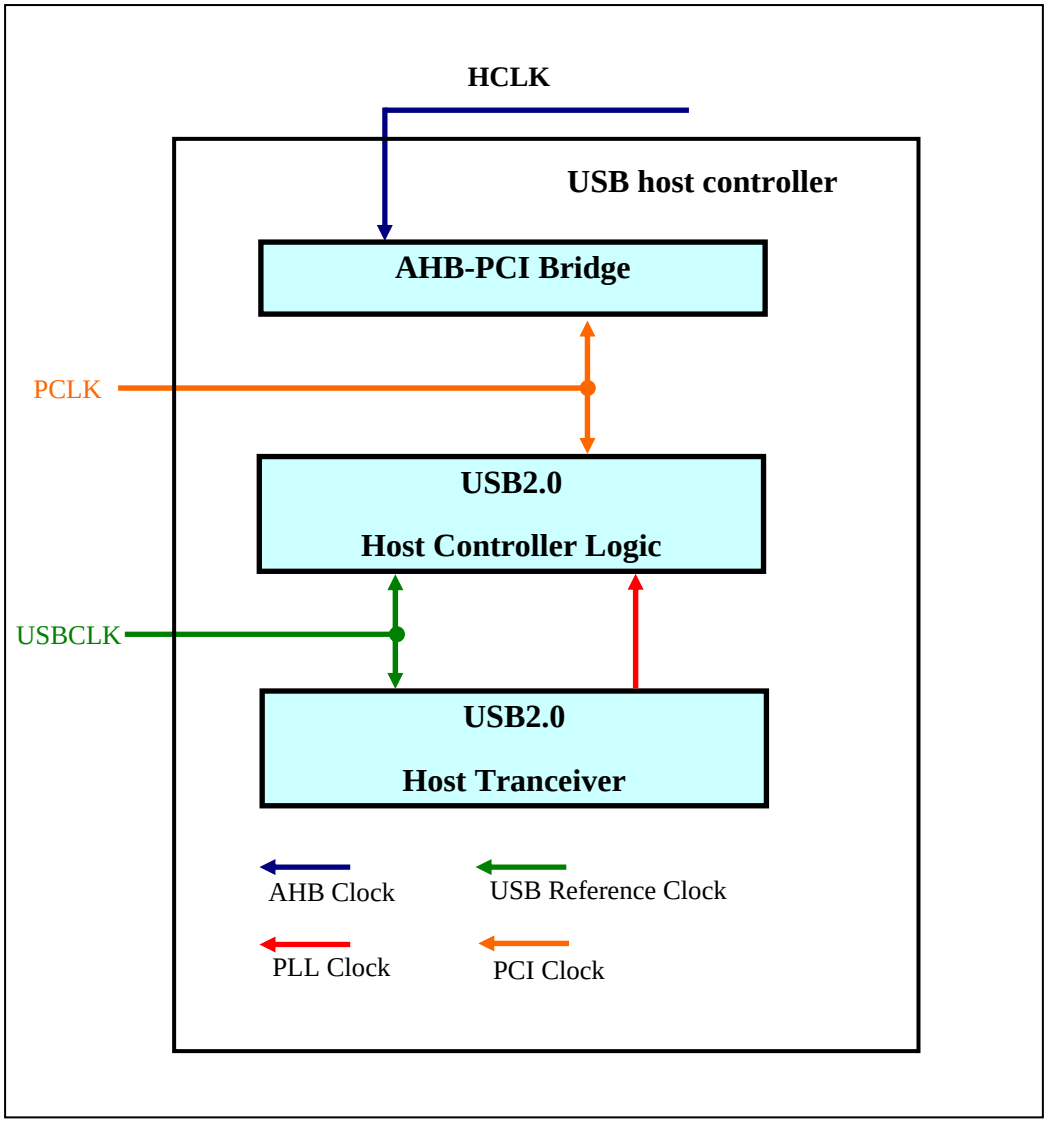
The PCICLK is a PCI bus clock that is supplied to the host controller and the AHB-PCI Bridge.

The frequency is limited to the range from 25 MHz to 33 MHz due to the specification of the host controller. When the USB host function is not used, the clock gating can be enabled for this clock internally from the AHB-PCI Bridge register. Dynamic control of the PCICLK except for clock stop is not supported.

6.2 Clock System Diagram

Figure 6-1 shows the clock system of the USB function controller.

Figure 6-1. Clock System Diagram



7. Reset System

7.1 Reset Configuration

This USB host controller is reset by the USB0_RSTZ signal. When the USB0_RSTZ signal is asserted, all the circuits within the USB host controller are reset. The USB0_RSTZ is a power-on reset, and assumes that the USB0_RSTZ signal of the AHB is connected. The reset signal of this USB host controller is an asynchronous reset that is directly connected to the F/F reset signal. The table lists the reset signals of this USB host controller.
Table 7-1 lists the reset signals for the USB function controller.

Table 7-1. Reset Signals

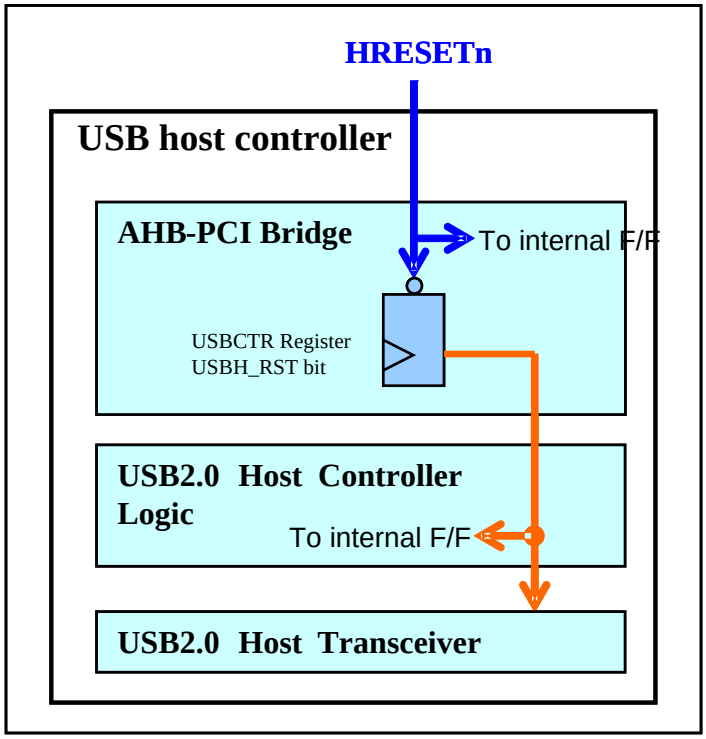
Reset Signal	Supplied From	Description
USB0_RSTZ	External	Power-on Reset Signal of the USB host controller Resets the entire USB host controller.
USBH_RST	Internal	USB Host Controller Reset Signal

When the USB0_RSTZ is asserted, the USBH_RST is also asserted. The internal reset can be operated from the AHB-PCI Bridge register. After the USB0_RSTZ assertion, use the same register to cancel the reset state. For the reset sequence, refer to section 0.

7.2 Reset System Diagram

Figure 7-1 shows the reset system in the USB function controller.

Figure 7-1. Reset System Diagram



8. Interrupts

8.1 Interrupt Signals

This USB host controller has the interrupt signals listed below. These signals are used as level-triggered interrupts. The interrupt lines can be reduced by the U2H_BIND_INT register if required (e.g., due to insufficient system resources). The U2H_BIND_INT register is not used when these interrupts are used individually.

Table 8-1. Interrupt Signals

Interrupt Signals	Synchronization Clock	Active Level	Description
USB_INTH	USB0_CLK	High	Interrupt signal generated from the AHB-PCI Bridge
U2H_OHCI_INT	USB0_CLK	High	INTA interrupt signal generated from the host controller
U2H_EHCI_INT	USB0_CLK	High	INTB interrupt signal generated from the host controller
U2H_PME_INT	PMCLK	High	PME interrupt signal generated from the host controller
U2H_BIND_INT	USB0_CLK/PMCLK	High	OR of the intererupt signals (Bridge+OHCI+EHCI+PME)

8.2 Interrupt Control Registers

8.2.1 USB_INTH control register

USB_INTH is an interrupt that is generated by the AHB-PCI Bridge. The status check, interrupt clear, and interrupt enable are performed by the AHB-PCI Bridge registers.

Table 8-2. USB_INTH Control Register

Function	Register
Interrupt status check and clear	PCI_INT_STATUS Register
Interrupt enable	PCI_INT_ENABLE Register

8.2.2 U2H_OHCI_INT Control Register

U2H_OHCI_INT is an INTA interrupt that is generated by the host controller. This interrupt is controlled by the host controller registers; however, for this interrupt signal assertion, the interrupt enable bit of the AHB-PCI Bridge must be set to Enabled.

Table 8-3. U2H_OHCI_INT Control Register

Function	Register
Interrupt status check and clear	HcInterruptStatus Register
Interrupt enable	HcInterruptEnable Register HcInterruptDisable Register PCI_INT_ENABLE Register (bit[16] USBH_INTAEN)

8.2.3 U2H_EHCI_INT Control Register

U2H_EHCI_INT is an INTB interrupt that is generated by the host controller. This interrupt is controlled by the host controller register. To assert this interrupt signal, the interrupt enable bit of the AHB-PCI Bridge must be valid.

Table 8-4. U2H_EHCI_INT Control Register

Function	Register
Interrupt status check and clear	USBSTS Register
Interrupt enable	USBINTR Register PCI_INT_ENABLE Register (bit[17] USBH_INTBEN)

8.2.4 U2H_PME_INT Control Register

U2H_PME_INT is a PME interrupt that is generated by the host controller. This interrupt is controlled by the host controller register. To assert this interrupt signal, the interrupt enable bit of the AHB-PCI Bridge must be valid.

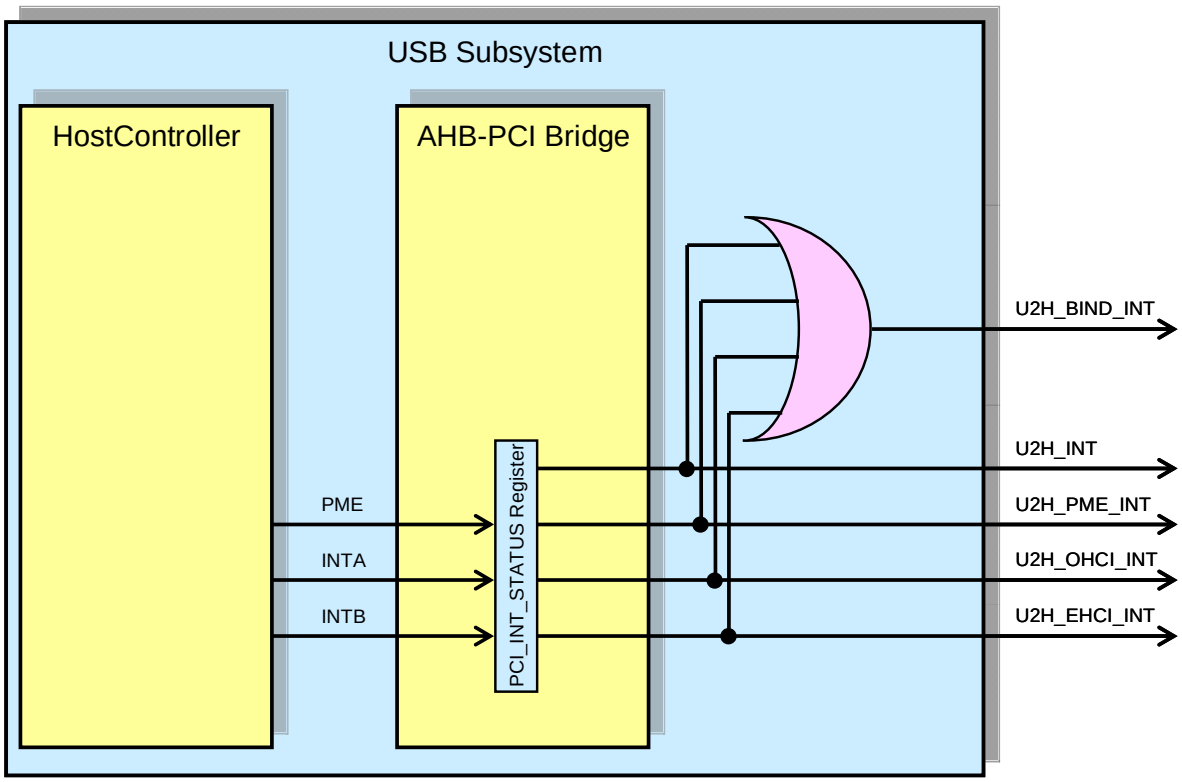
Table 8-5. U2H_PME_INT Control Register

Function	Register
Interrupt status check and clear	PCI Configuration Register for OHCI/EHCI offset 44h
Interrupt enable	PCI Configuration Register for OHCI/EHCI offset 44h PCI_INT_ENABLE Register (bit[19] USBH_PMEEN)

8.3 U2H_BIND_INT

The U2H_BIND_INT interrupt signal is generated by an OR of the interrupt source signals (USB_INTH, U2H_OHCI_INT, U2H_EHCI_INT, and U2H_PME_INT). The signal states of the U2H_PME_INT, U2H_OHCI_INT and U2H_EHCI_INT are reflected to the PCI_INT_STATUS register. Reading the PCI_INT_STATUS register enables the user to check the interrupt source.

Figure 8-1. Interrupt Signals Aggregation Image

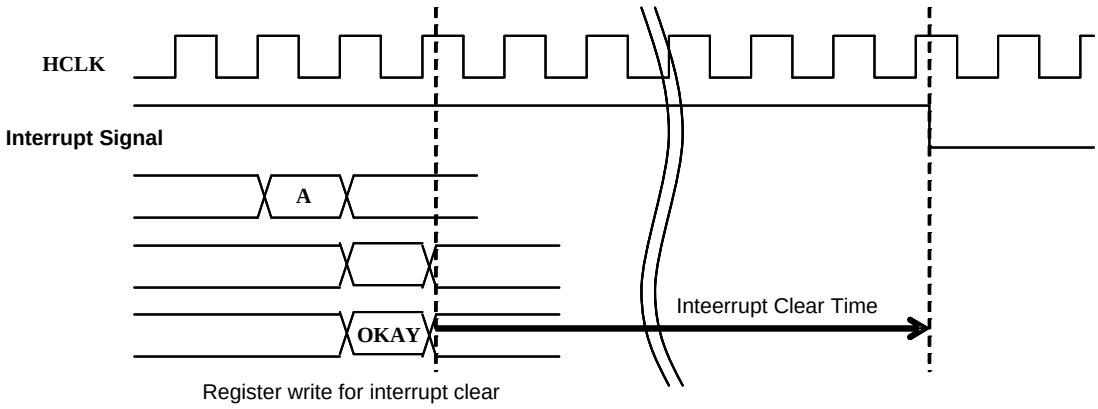


8.4 Interrupt Signal Clear Time

The AHB-PCI Bridge implements a posted write; therefore, an interrupt generated by the host controller may not be cleared soon after setting the clear register and same interrupt state may be recognized many times. (See the Fig. 8-2.) The user must take a countermeasure to avoid such false recognition.
For example; access to the host controller register (2) after accessing to an Interrupt Clear Register (1). The operation of (2) is waited (SHREADY = 0 or Retry response) until the operation of (1) is completed. As the result, the interrupt is cleared without fail at the completion of the access of (2).

The U2H_OHCI_INT, U2H_EHCI_INT, and U2H_PME_INT may not be cleared soon after setting the clear register. When USB0_CLK = 150MHz and PCICLK = 25MHz, the interrupt is cleared in about 300 ns after setting the clear register. When the host controller is executing a transfer as a master on the internal PCI-bus, it takes about 1.6 us (35CLK@PCICLK+3CLK@USB0_CLK +2CLK@12MHz) at worst to clear the interrupt.

Figure 8-2. Interrupt Clear Time



9. Power Management

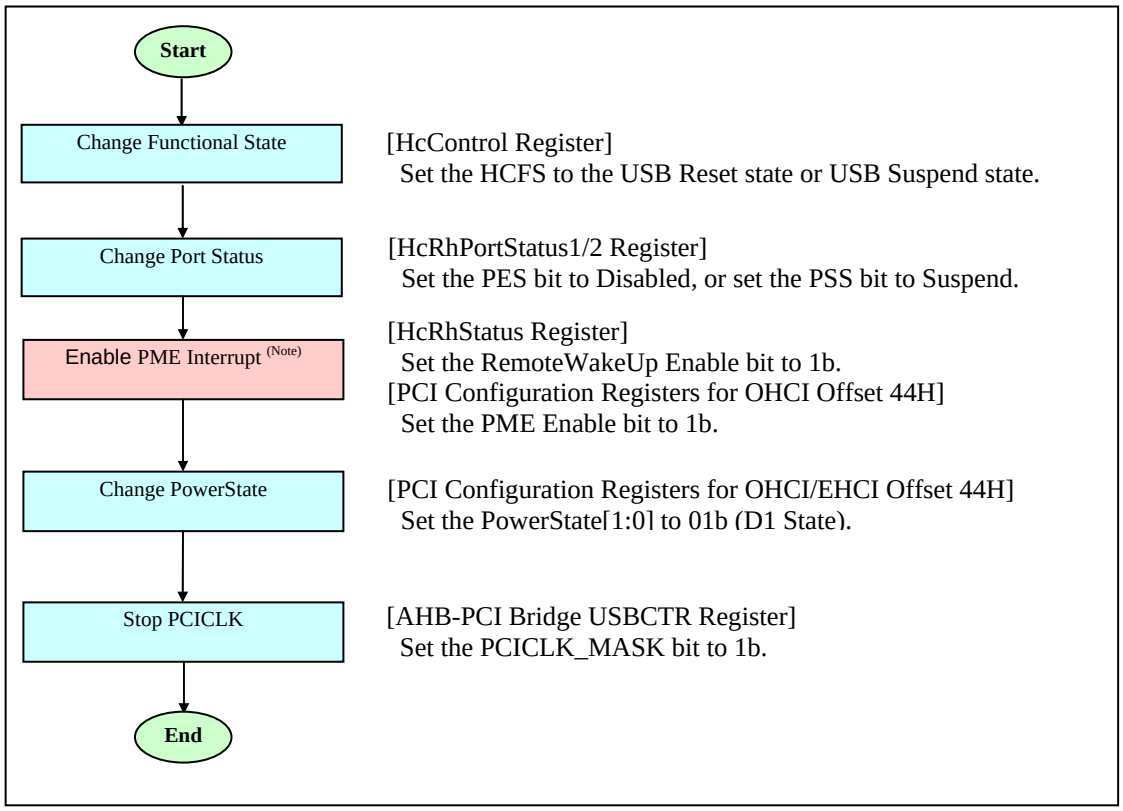
This chapter describes the power management function of the USB Host controller V1 Type-H2.
When the USB is not used, hold the power state in a reset state after cancellation of the AHB bus reset (USBCTR Register, USBH_RST = 1b). The subsequent sections describe a power-off operation that temporarily powers down (suspend) the USB host.

9.1 Power-Off Sequence

When the USB Host function is temporarily stopped, the power consumption can be reduced by powering down the host controller and stopping the internal PCI bus clock (PCICLK) of the USB host controller.
The USB host controller has a gating circuit for the PCICLK, and the circuit can be controlled from the AHB-PCI Bridge register. The following figure shows the power-off sequence.

(1) OHCI Mode

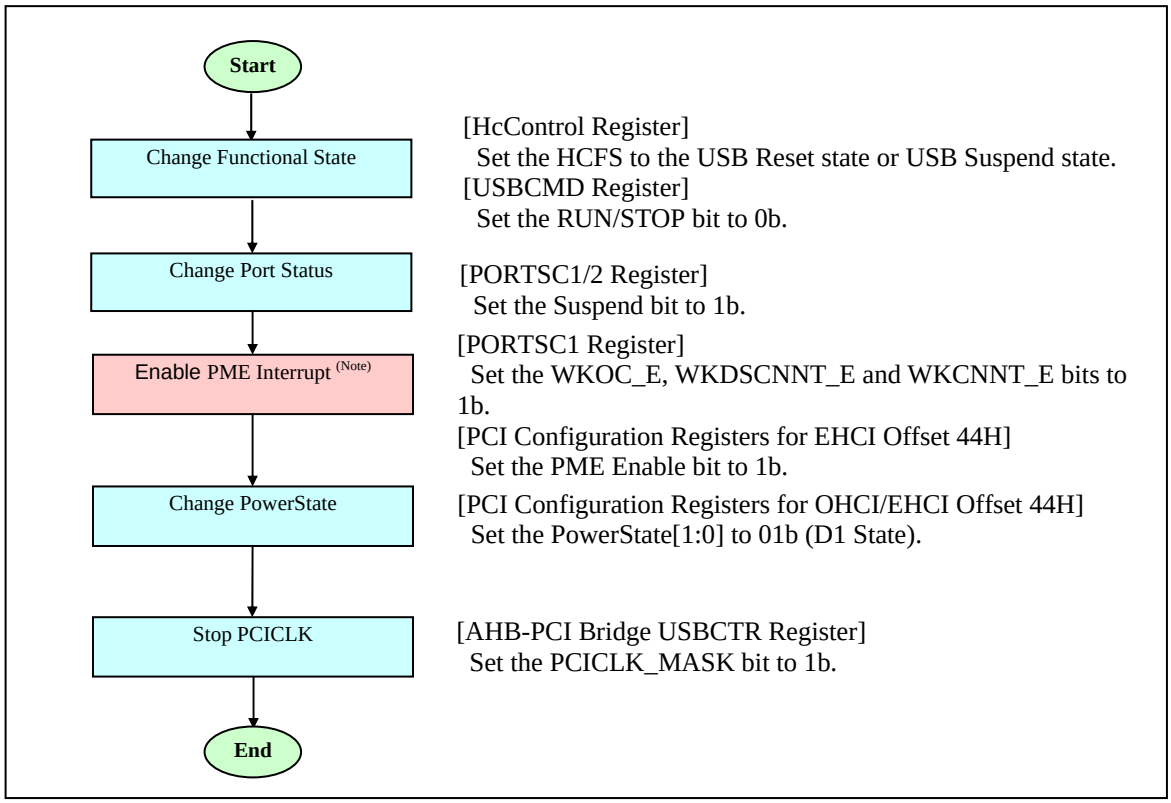
Figure 9-1. Power-Off Sequence



Note To detect the event (e.g., connected, disconnected or resumed) that occurs on the USB bus during the power-down operation, the PME interrupt must be enabled.

(2) EHCI Mode

Figure 9-2. Power-Off Sequence



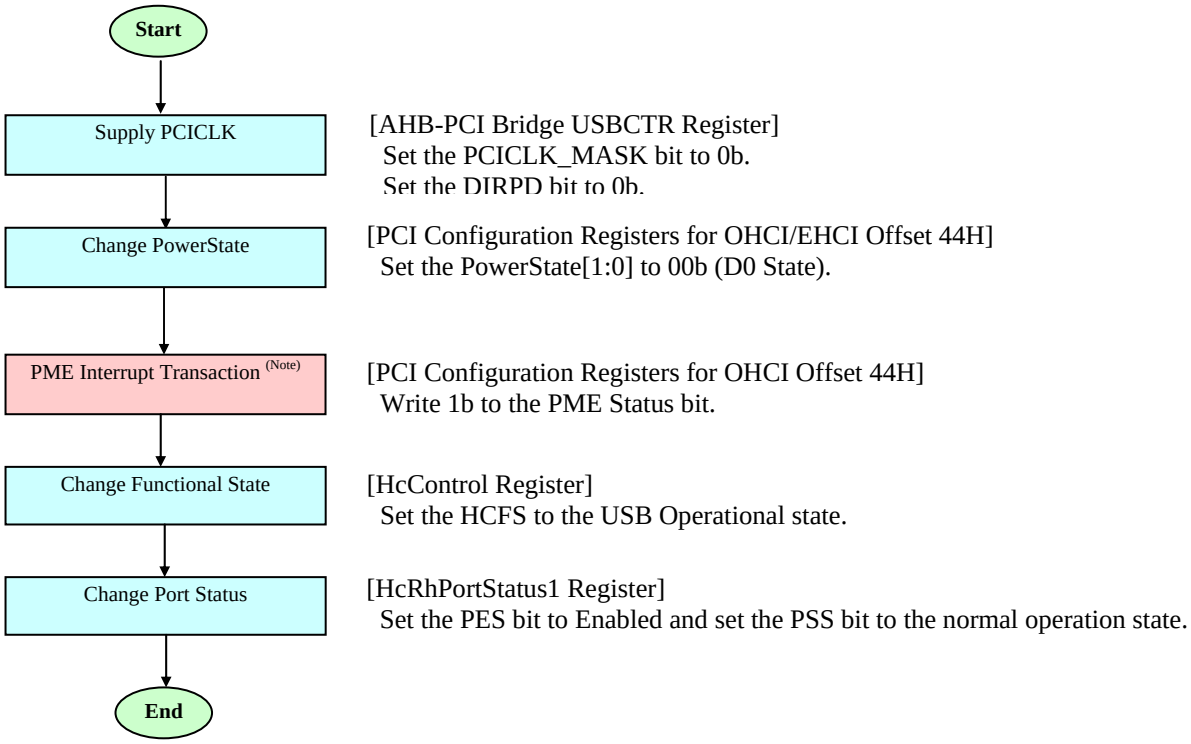
Note To detect the event (e.g., connected, disconnected or resumed) that occurs on the USB bus during the power-down operation, the PME interrupt must be enabled.

9.2 Power On Sequence

The recovery from the power-down state is performed in the opposite procedure of the power-down operation.

(1) OHCI Mode

Figure 9-3. Power-On Sequence

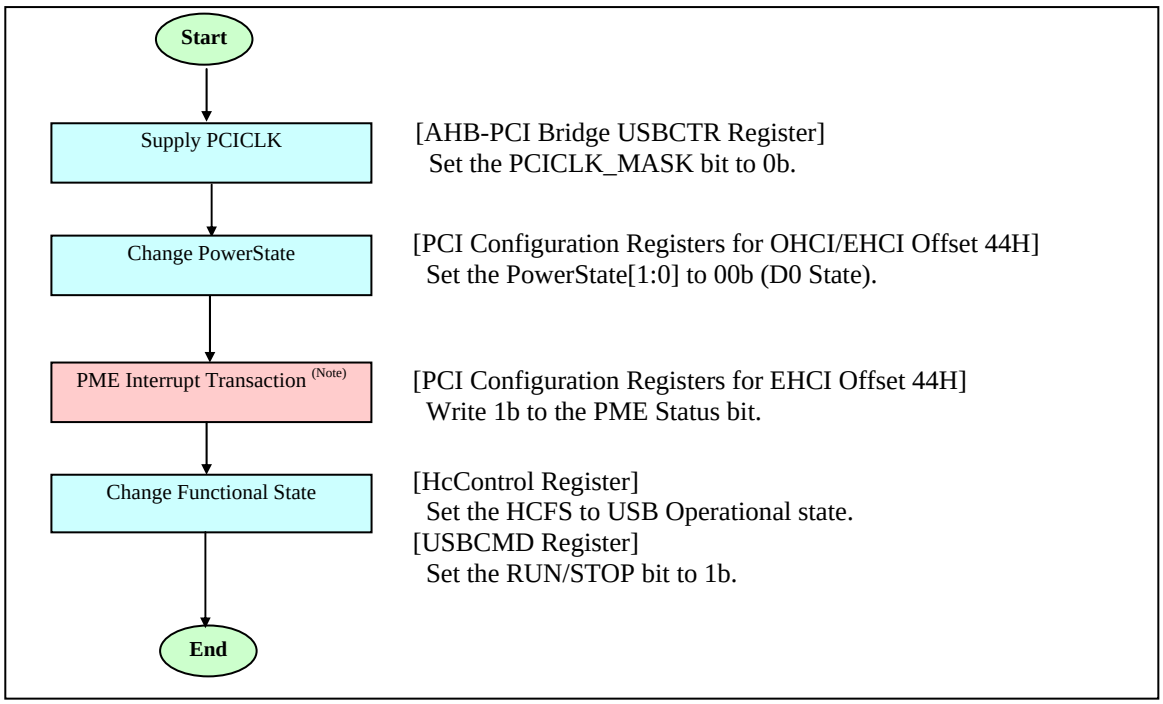


The interrupt source can be checked from the HcRhPortStatus1 register.

When an interrupt is detected, supply the PCICLK, and then clear the interrupt.

(2) EHCI Mode

Figure 9-4. Power-On Sequence



The interrupt source can be checked from the PORTSC1 register.

When an interrupt is detected, supply the PCICLK, and then clear the interrupt.

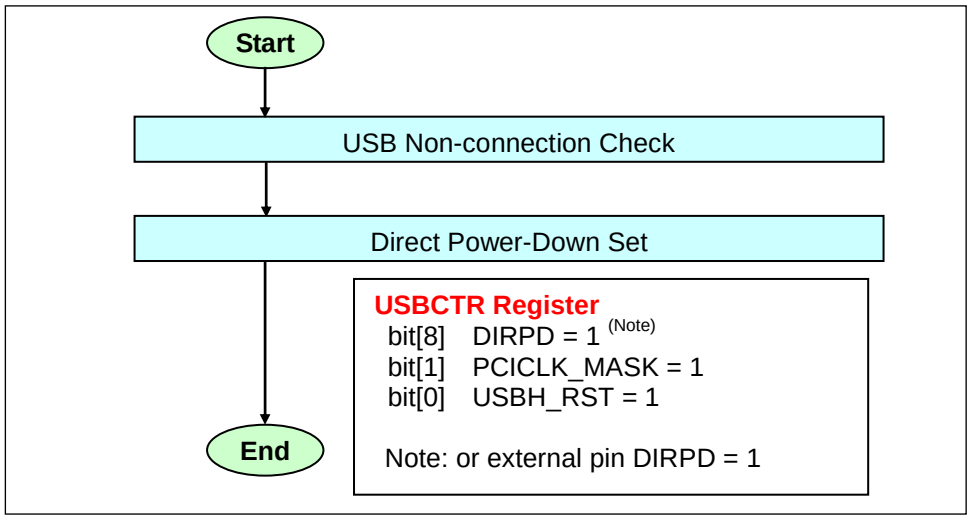
9.3 Direct Power-Down Feature

When the whole USB host controller is not used, power consumption of the USB host controller can be reduced using the direct power-down function. Recovery from the direct power-down state is not performed in this USB host controller.

9.3.1 Direct Power-Down Setting

The figure below shows how to set the direct power-down mode. It is recommended that the PCICLK be masked from the PCICLK_MASK register to minimize power consumption.

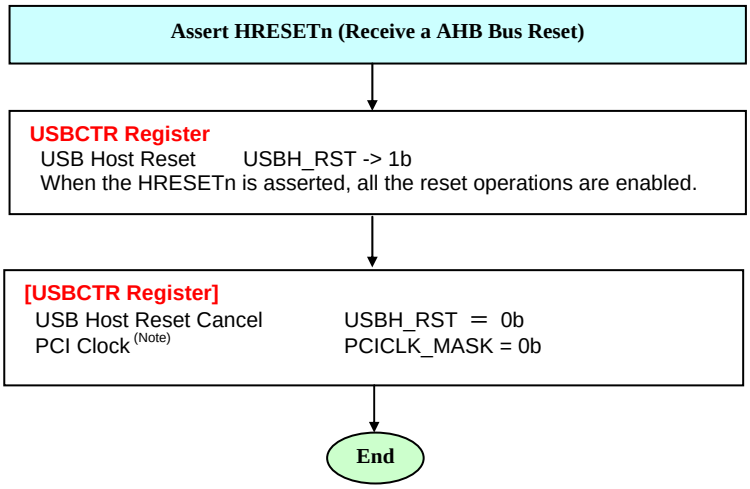
Figure 9-5. Direct Power-Down Setting



10. Operating Procedures

10.1 Reset Sequence

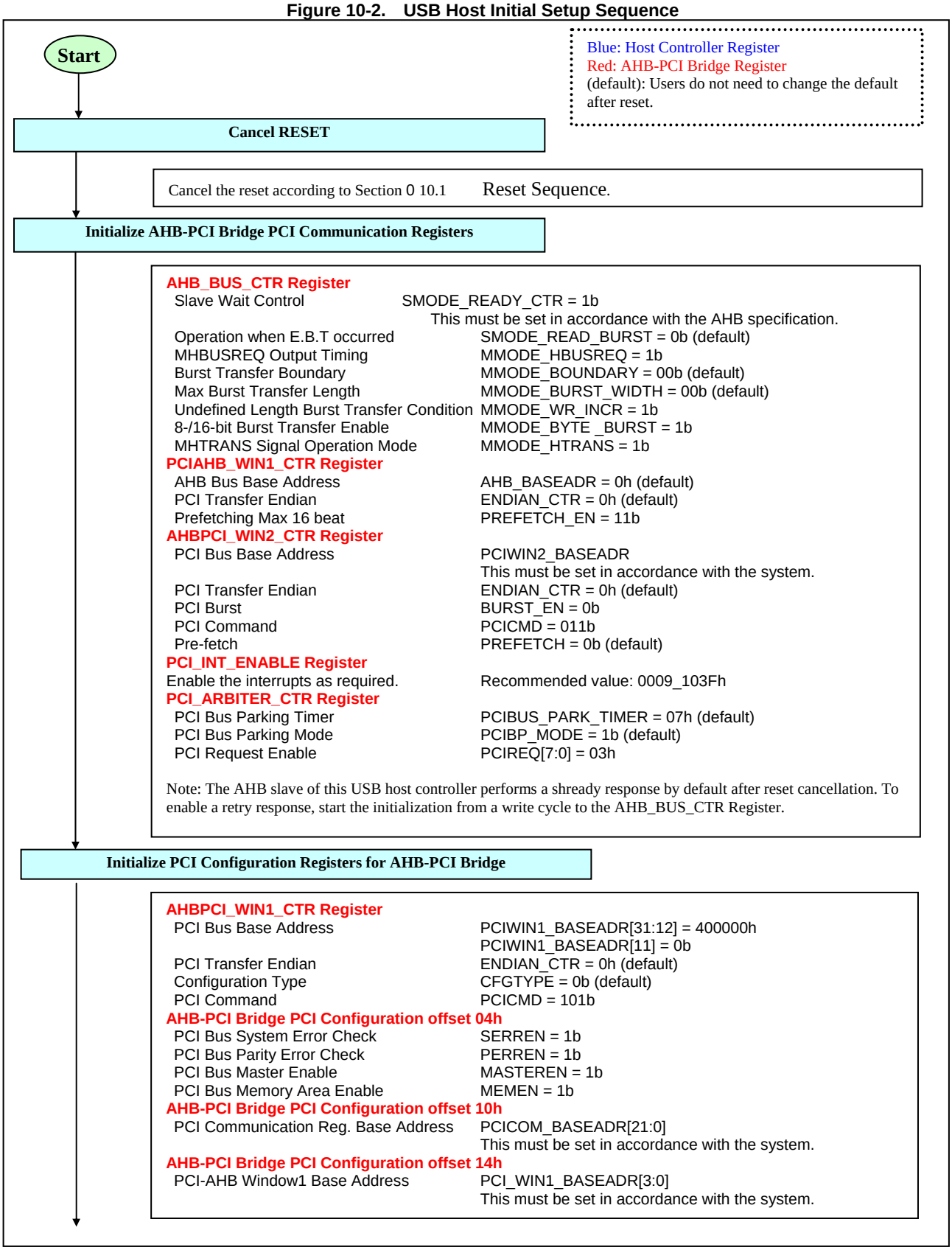
Figure 10-1. Reset Sequence

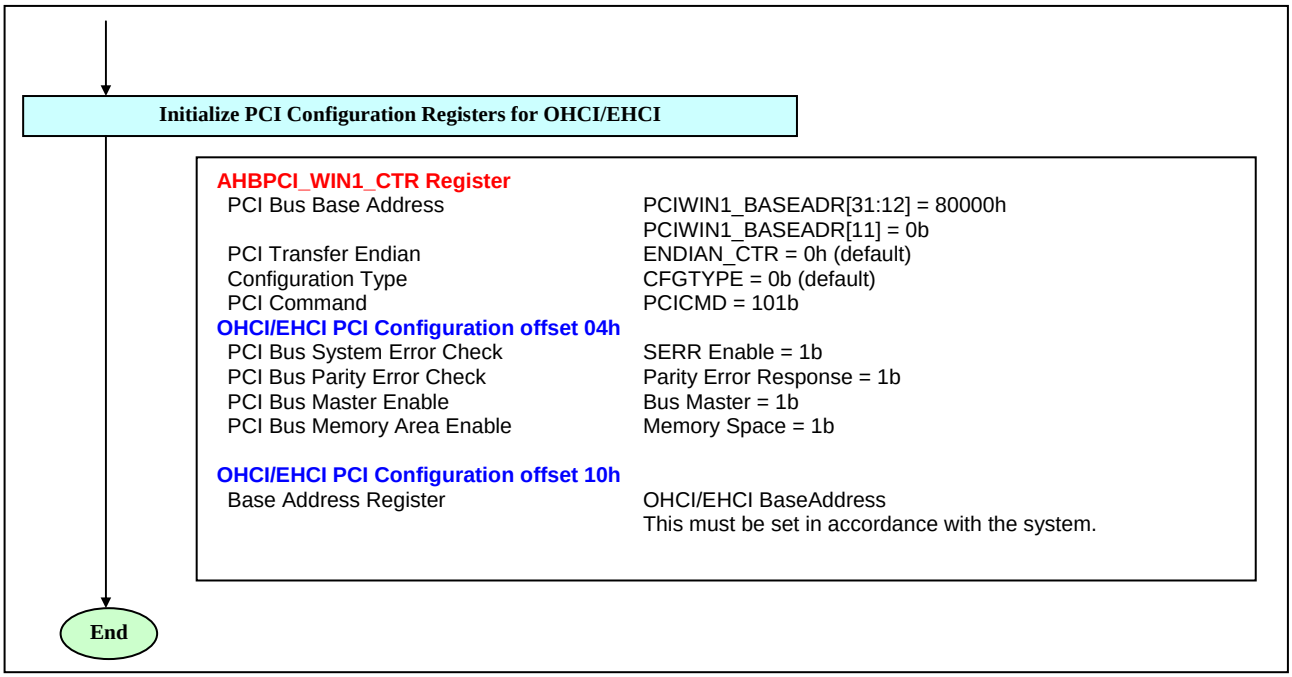


Note Access to the host controller is enabled in 3CLK@PCICLK after reset cancellation.

10.2 Initial Setup Sequence

Figure 10-2. USB Host Initial Setup Sequence





The above settings enable the following operations.

- Access to the OHCI and EHCI Operation Registers via the AHB-PCI Window2 register
- Data transfer to the AHB from the host controller

10.3 Transfer Overview

Transfer by the host controller must be performed in compliance with the following OHCI and EHCI specifications.

- Open Host Controller Interface Specification for USB Rev 1.0a
- Enhanced Host Controller Interface Specification for Universal Serial Bus Revision 1.0

This section provides supplementary note about the DMA stop.

10.3.1 DMA Transfer Stop

The AHB-PCI Bridge does not have a control bit that turns on or off DMA mode. When the host controller initiates a PCI bus cycle as a master, the AHB-PCI Bridge performs DMA transfer to the AHB. DMA transfer of the host controller is performed: (1) to write the current frame number into memory; and (2) to write or read the descriptor and data loaded into memory to perform a list transaction.

Writing of the frame number (1) is performed per frame cycle when the USB is in the Operational state; therefore, the USB must be put into the Suspend or Reset state before stopping the DMA transfer. In this case, the list transaction of (2) is stopped at the same time.

The list transaction of (2) is stopped when the enable bit (HcControl Register, BLE bit, CLE bit, PLE bit) of the list transaction is cleared. The transaction is stopped from the next frame when the bit is cleared. In this case, a writing of the frame number of (1) is not stopped.

REVISION HISTORY	EMMA Mobile EV2 User's Manual: USB 2.0 Host Controller

Rev.	Date	Description	
		Page	Summary
1.00	Oct 20, 2010	—	1st revision release
2.00	May 31, 2011	—	Incremental update from comments to the 1.0.
3.00	Mar 30, 2012	—	Isochronous transfer related description deleted.
4.00	Apr 12, 2012	1	Chapter 1.1 corrected. (OHCI specification Rev 1.0a compliant→OHCI specification Rev 1.0a compatible) (EHCI specification Rev 1.0a compliant→EHCI specification Rev 1.0a compatible) Isochronous transfer unsupported added.

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