User's Manual

CF Card Interface

User's Manual

Multimedia Processor for Mobile Applications
EMMA Mobile ™ EV2

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the EMMA Mobile EV2. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Data Sheet	Hardware overview and electrical characteristics	EMMA Mobile EV2 Datasheet	R19DS0010EJxxxx
User's manual (1chip)	Hardware whole specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description	EMMA Mobile EV2 User's manual 1chip	R19UH0036EJxxxx
User's manual (module)	Hardware each macro specifications and operation description.	EMMA Mobile EV2 User's manual each module	See below

Document Name	Document No.	Document Name	Document No.
1chip	R19UH0036EJxxxx	DMA Controller	R19UH0043EJxxxx
System Management Unit	R19UH0037EJxxxx	LP-DDR/DDR2 Controller	R19UH0039EJxxxx
Timer	R19UH0054EJxxxx	SD Memory Card Interface	R19UH0061EJxxxx
System Timer	R19UH0055EJxxxx	SDIO Interface	R19UH0042EJxxxx
HD Video Decoder	R19UH0056EJxxxx	CF Card Interface (This manual)	R19UH0062EJxxxx
Rotator	R19UH0057EJxxxx	Unified Serial Interface	R19UH0047EJxxxx
Resizer	R19UH0058EJxxxx	UART interface	R19UH0040EJxxxx
Image Composer	R19UH0038EJxxxx	USB 2.0 Host Controller	R19UH0045EJxxxx
LCD Interface	R19UH0044EJxxxx	USB 2.0 Function Controller	R19UH0034EJxxxx
ITU-R BT.656 Interface	R19UH0059EJxxxx	IIC Interface	R19UH0052EJxxxx
Digital Terrestrial TV Interface	R19UH0048EJxxxx	General Purpose I/O Interface	R19UH0041EJxxxx
Camera Interface	R19UH0060EJxxxx	Pulse Width Modulation Interface	R19UH0063EJxxxx

4 digits of end shows the version.

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names

Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.

Examples the PM03 bit in the PM0 register

P3_5 pin, VCC pin

(2) Notation of Numbers

The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.

Examples Binary: 11b or 11

Hexadecimal: EFA0h

Decimal: 1234

3. Register Notation

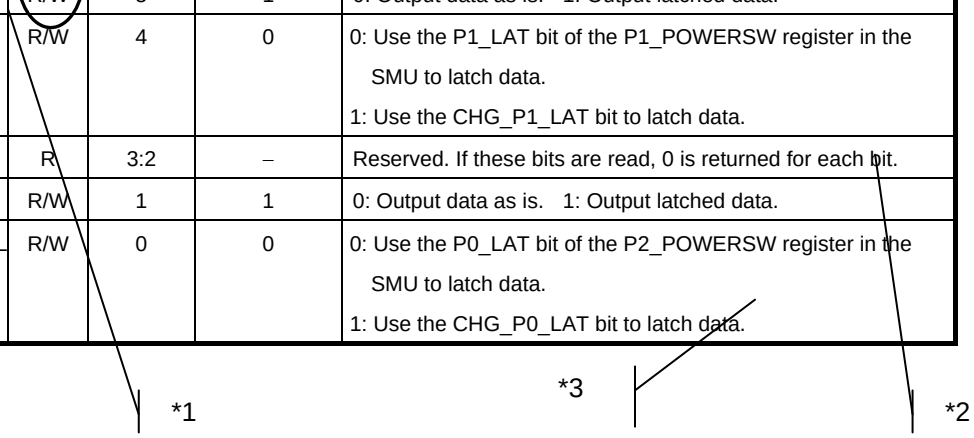
The symbols and terms used in register diagrams are described below.

x.x.x XXX register

This register (XXXXXXX: xxxx_xxxxh) …..

7	6	5	4	3	2	1	0
Reserved		CHG_P1_LAT	LATCH_P1_SEL	Reserved		CHG_P0_LAT	CHG_P0_LAT_SEL

Name	R/W	Bit No.	After Reset	Description
LATCH_P2_SEL	R/W	8	0	0: Use the P2_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P2_LAT bit to latch data.
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P1_LAT	R/W	5	1	0: Output data as is. 1: Output latched data.
LATCH_P1_SEL	R/W	4	0	0: Use the P1_LAT bit of the P1_POWERSW register in the SMU to latch data. 1: Use the CHG_P1_LAT bit to latch data.
Reserved	R	3:2	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P0_LAT	R/W	1	1	0: Output data as is. 1: Output latched data.
CHG_P0_LAT_SEL	R/W	0	0	0: Use the P0_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P0_LAT bit to latch data.



*1

R/W: Read and Write.

R: Read only.

W: Write only.

-: Nothing is assigned.

*2

Reserved bit.

Reserved bit. Set to specified value.

*3

・ Nothing is assigned.

Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.

・ Do not set to a value.

Operation is not guaranteed when a value is set.

・ Function varies according to the operating mode.

The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Register
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

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Table of Contents

1. Overview

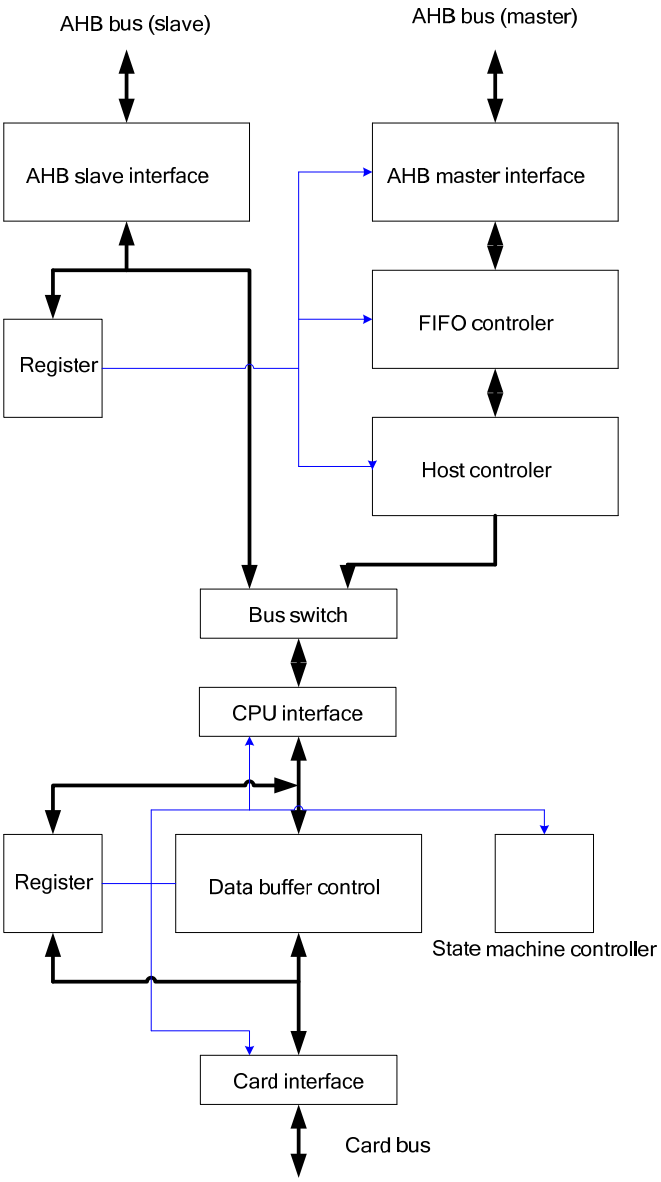
1.1 Features

The CFI (compact flash interface) module provides host controller features for a peripheral interface using compact flash memory devices compliant with the CompactFlash® specifications, which are standardized by the CompactFlash Association (CFA).
The major features of the CFI module are as follows:

- Compliant with CF+ (CompactFlash Plus) and CompactFlash Specification Revision 3.0 released by the CFA
- Supports CF+ and CF (CompactFlash).
- Supports the True IDE PIO mode as the CompactFlash operating mode
- Supports True IDE PIO modes 0 to 6
- Timing to access cards can be specified using a register.
- 32 bits × 16 words of internal RAM provided for data transmission and reception
- Generates an interrupt request signal to the interrupt controller (INTA) when any of the following is detected:
  - Card insertion or removal
  - A change of the card status
  - A change of the RDY signal status (a data transfer completion interrupt in the True IDE mode)
  - Illegal access
- Supports automatic clock control, outputs a clock request signal to the SMU when a clock is necessary, and outputs an advance clock request signal to the SMU and bus bridge DDR controller
- A reset signal output from outside the macro is asserted asynchronously, and deasserted synchronously
- Restriction
  CF+ and CompactFlash Specification Revision 4.x are not supported.

1.2 Function Block Diagram

Figure 1-1. Function Block Diagram



2. Pin functions

3.3V system

Pin Name	IO Type	Function	Alternate Pin Function
CF_D15	I/O	CF data bit 15	AB_AD15, SDI2_DATA3, GPIO_092
CF_D14	I/O	CF data bit 14	AB_AD14, SDI2_DATA2, GPIO_091
CF_D13	I/O	CF data bit 13	AB_AD13, SDI2_DATA1, USI5_CS2, GPIO_090
CF_D12	I/O	CF data bit 12	AB_AD12, SDI2_DATA0, USI5_CS1, GPIO_089
CF_D11	I/O	CF data bit 11	AB_AD11, DTV_DATA, USI5_CS0, GPIO_088
CF_D10	I/O	CF data bit 10	AB_AD10, DTV_VALID, USI5_DO, GPIO_087
CF_D09	I/O	CF data bit 9	AB_AD9, DTV_PSYNC, USI5_DI, GPIO_086
CF_D08	I/O	CF data bit 8	AB_AD8, DTV_BCLK, USI5_CLK, GPIO_085
CF_D07	I/O	CF data bit 7	AB_AD7, GPIO_084
CF_D06	I/O	CF data bit 6	AB_AD6, GPIO_083
CF_D05	I/O	CF data bit 5	AB_AD5, GPIO_082
CF_D04	I/O	CF data bit 4	AB_AD4, GPIO_081
CF_D03	I/O	CF data bit 3	AB_AD3, GPIO_080
CF_D02	I/O	CF data bit 2	AB_AD2, GPIO_079
CF_D01	I/O	CF data bit 1	AB_AD1, GPIO_078
CF_D00	I/O	CF data bit 0	AB_AD0, GPIO_077
CF_CSB1	Output	CF chip select 1	AB_CSB3, GPIO_072
CF_CSB0	Output	CF chip select 0	AB_CSB2, GPIO_071
CF_RESET	Output	CF reset output	AB_ADV, GPIO_076
CF_A02	Output	CF address bit 2	AB_A19, GPIO_095
CF_A01	Output	CF address bit 1	AB_A18, GPIO_094
CF_A00	Output	CF address bit 0	AB_A17, GPIO_093
CF_IOWRB	Output	CF write strobe	AB_WRB, GPIO_074
CF_IORDB	Output	CF read strobe	AB_RDB, GPIO_073
CF_IORDY	Input	CF I/O ready	AB_WAIT, GPIO_075
CF_INTRQ	Input	CF interrupt request	AB_A21, SDI2_CKO, GPIO_097
CF_INPACKB	Input	IO read reply input (asynchronous)	AB_A24, GPIO_100
CF_CDB1	Input	CF card detection 1	AB_A25, GPIO_101
CF_CDB2	Input	CF card detection 2	AB_A26, GPIO_102

3. Registers

3.1 Register List

The CFI registers are accessed via the AHB bus in 32-bit, 16-bit, and 8-bit units.
Base address: E220_0000H

CF-ATA register list (Card internal ATA register)
(Refer to CF+ and Compact Flash Specification Revision 4.1 6.1.5 for details.)

Address	Register Name
01F0H	Data register
01F1H	Feature register
01F2H	Sector count register
01F3H	Sector number
01F4H	Cylinder low
01F5H	Cylinder high
01F6H	Drive/Head
01F7H	Status & Alternate status register
03F6H	Device control register
03F7H	Card (drive) address register
8000H to BFFFH	Reserved

CFI internal register

Address	Register Name	Symbol	R/W	After Reset
C000H	Control register 0	Control-0	R/W	0000_8000H
C004H	Control register 1	Control-1	R/W	0000_0000H
0008H	Reserved	–	–	–
C00CH	Interrupt register	Interrupt	R/W	0000_0000H
C010H	Status register	Status	R	0000_07FEH
C014H	Reserved	–	–	–
C018H	Timing register 1	Timing-1	R/W	0000_0000H
C01CH to C020H	Reserved	–	–	–
C024H	Version register 0	Version-0	R	0000_2007H
C028H	Version register 1	Version-1	R	0000_0222H
C02CH	Data register	DATA	R/W	0000_0000H
C030H	Reserved	–	–	–
C034H	Extension register 0	Extension-0	R/W	0000_0000H
C038H	Extension register 1	Extension-1	R	0000_0002H
C03CH to E000H	Reserved	–	–	–
E004H	Bus interface control register	BUSIF_CTRL	R/W	0000_0000H
E008H	TXMEM address register	TXMEM_ADDR	R/W	3000_8000H

E00CH	RXMEM address register	RXMEM_ADDR	R/W	3000_C000H
E010H	PIO address register	PIO_ADDR	R/W	0000_0000H
E014H	Reserved	–	–	–
E018H	Sector length register	SECTOR_LENGTH	R/W	0000_0000H
E01CH	Block length register	BLOCK_LENGTH	R/W	0000_0001H
E020H	Block index register	BLOCK_INDEX	R/W	0000_0000H
E024H	Transfer start register	TRANS_START	R/W	0000_0000H
E028H, E02CH	Reserved	–	–	–
E034H	Interrupt raw status register	INT_RAW	R	0000_0001H
E038H	Interrupt report register	INT_ORG	R	0000_0000H
E03CH	Interrupt clear register	INT_CLR	W	0000_0000H

3.2 Register Details

3.2.1 Control register 0

This register (Control-0: C000H) is used to control the CFI module operation.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
HRST	IOEN	Reserved					
7	6	5	4	3	2	1	0
Reserved			IDE	IDEM[1:0]		Reserved	

Name	R/W	Bit No.	After Reset	Description
Reserved	–	31:16	0000H	Reserved. If these bits are read, 0 is returned for each bit.
HRST	R/W	15	1	Select the level of the hardware reset signal (RESET) output to the card. RESET is high active in the PC card (memory, I/O) mode. RESET is low active in the True IDE mode 0: Low level 1: High level
IOEN	R/W	14	0	Select the level of the I/O buffer output enable signal (CARDENB). 0: Output H (inactive) 1: Output L (active) If bit 7 (PCNT) is 0, the CARDENB signal level changes according to the CD1B/CD2B signal level. If CD1B and CD2B are low: Level specified for the IOEN bit If CD1B and CD2B are not low: High level If bit 7 (PCNT) is 1, the level specified for the IOEN bit is output.
Reserved	–	13:5	00H	Reserved. If these bits are read, 0 is returned for each bit.
IDE	R/W	4	0	Select the card mode. 0: Setting prohibited 1: True IDE mode
IDEM[1:0]	R/W	3:2	00b	Select the access type in the True IDE mode. 00: PIO mode 01, 10, 11: Setting prohibited
Reserved	–	1:0	0H	Reserved. If these bits are read, 0 is returned for each bit.

3.2.2 Control register 1

This register (Control-1: C004H) is used to control the CFI module operation.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
SRST	Reserved					RINTA	RINTB
7	6	5	4	3	2	1	0
AINTE	Reserved		BINTE	CINTE	RINTE	DINTE	EINTE

(1/2)

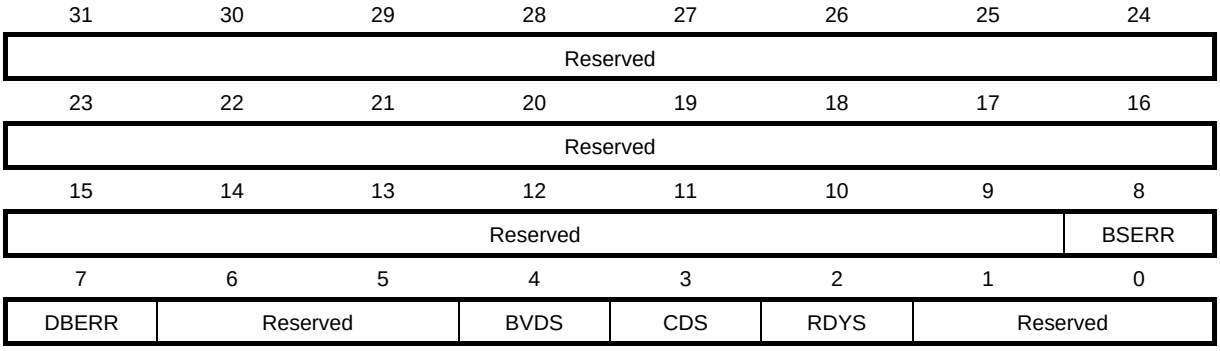
Name	R/W	Bit No.	After Reset	Description
Reserved	–	31:16	0000H	Reserved. If these bits are read, 0 is returned for each bit.
SRST	R/W	15	0	This bit is used to execute a software reset[Note]. 0: Cancel a reset. (CFI registers are not reset.) 1: Reset (All the CFI registers are reset.) **Note** The internal circuit must be reset by setting this bit to 1 in such cases as when a busy state is not canceled by the card or when the card is removed or inserted during a transfer, making the transfer invalid.
Reserved	–	14:10	00H	Reserved. If these bits are read, 0 is returned for each bit.
RINTA	R/W	9	0	Specify the timing for detecting an interrupt caused by changing the level of the ready signal (RDY) output from the card. 0: When the RDY level changes (L to H or H to L) 1: When the RDY level becomes the level shown in bit 8 (RINTB).
RINTB	R/W	8	0	Specify the timing for detecting an interrupt based on the level of the RDY signal output from the card. 0: When RDY becomes high 1: When RDY becomes low
AINTE	R/W	7	0	Specify whether to enable outputting an interrupt upon illegal CPU access[Note]. 0: Disable 1: Enable **Note** Access other than that shown in *4.3 Bus Sizing* or access to the DATA register (2CH)
Reserved	–	6:5	0H	Reserved. If these bits are read, 0 is returned for each bit.
BINTE	R/W	4	0	Specify whether to enable outputting an interrupt when the level of the battery voltage detection signal (BVD1 or BVD2) output from the card changes. 0: Disable 1: Enable

(2/2)

Name	R/W	Bit No.	After Reset	Description
CINTE	R/W	3	0	Specify whether to enable outputting an interrupt when the level of the card detection signal (CD1B or CD2B) output from the card changes. 0: Disable 1: Enable
RINTE	R/W	2	0	Specify whether to enable outputting an interrupt when the level of the ready signal (RDY) output from the card changes. 0: Disable 1: Enable
DINTE	R/W	1	0	Specify whether to enable outputting an interrupt when a transfer does not finish normally[Note]. 0: Disable 1: Enable **Note** During post-writing, this interrupt means the data buffer has available space and the specified number of transfers has not been reached. During prefetching, this interrupt means data exists in the data buffer and the specified number of transfers has not been reached.
EINTE	R/W	0	0	Specify whether to enable outputting an interrupt when post-writing or prefetching finishes. 0: Disable 1: Enable

3.2.3 Interrupt register

This register (Interrupt: C00CH) indicates the sources of the interrupts to the CPU.
The bits in this register are cleared when 1 is written to them.



Name	R/W	Bit No.	After Reset	Description
Reserved	–	31:9	00_0000H	Reserved. If these bits are read, 0 is returned for each bit.
BSERR	R/W	8	0	Indicates whether access for which the CPU cannot change the bus size occurred. 0: Did not occur 1: Occurred
DBERR	R/W	7	0	Indicates whether the data buffer is used to access the DATA register. 0: The data buffer is used. 1: The data buffer is not used.
Reserved	–	6:5	0H	Reserved. If these bits are read, 0 is returned for each bit.
BVDS	R/W	4	0	Indicates whether the level of the battery voltage detection signal (BVD1 or BVD2) output from the card has changed. 0: Not changed (for battery status and card status information) 1: Changed (for battery status and card status information) For the memory card interface, the fall of BVD1 or BVD2 is detected (which means the battery operation is disabled). For the I/O card interface, the change of the BVD1 level is detected (which shows the change in card status information).
CDS	R/W	3	0	Indicates whether the level of the card detection signal (CD1B or CD2B) output from the card has changed. 0: Not changed (No card has been inserted or removed.) 1: Changed (A card has been inserted or removed.)
RDYS	R/W	2	0	Indicates whether the level of the ready signal (RDY) output from the card has changed. 0: Not changed 1: Changed
Reserved	–	1:0	0H	Reserved. If these bits are read, 0 is returned for each bit.

3.2.4 Status register

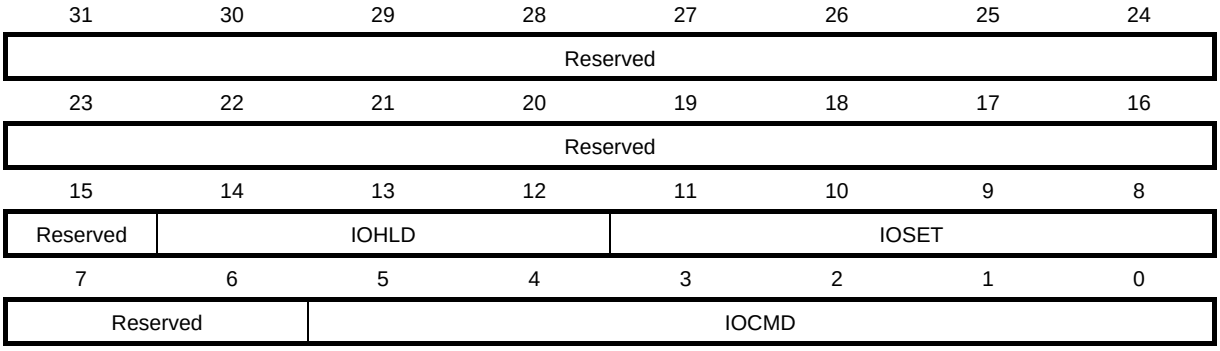
This register (Status: C010H) indicates the card status.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved					RDY	Reserved	CD2
7	6	5	4	3	2	1	0
CD1	VS2	VS1	IPK	Reserved	BVD1	CVCC	CDV

Name	R/W	Bit No.	After Reset	Description
Reserved	–	31:11	00_0000H	Reserved. If these bits are read, 0 is returned for each bit.
RDY	R	10	1	Indicates the RDY value output from the card.
Reserved	–	9	0	Reserved. If this bit is read, 0 is returned.
CD2	R	8	1	Indicates the CD2B value output from the card.
CD1	R	7	1	Indicates the CD1B value output from the card.
VS2	R	6	1	Indicates the VS2B value output from the card.
VS1	R	5	1	Indicates the VS1B value output from the card.
IPK	R	4	1	Indicates the INPACKB value output from the card.
Reserved	–	3	0	Reserved. If this bit is read, 0 is returned.
BVD1	R	2	1	Indicates the BVD1 value output from the card.
CVCC	R	1	1	Indicates the CVCC value output from the card.
CDV	R	0	0	Indicates whether a card has been inserted based on the detection of CD1B and CD2B being at the low level. 0: Not inserted 1: Inserted

3.2.5 Timing register 1

This register (Timing-1: C018H) is used to specify the number of wait cycles in the PC card (I/O) and True IDE PIO modes.



Name	R/W	Bit No.	After Reset	Description
Reserved	–	31:15	0_0000H	Reserved. If these bits are read, 0 is returned for each bit.
IOHLD	R/W	14:12	000b	Specify the number of wait cycles for data to be held in True IDE PIO mode.
IOSET	R/W	11:8	0000b	Specify the number of wait cycles for data to be set up in True IDE PIO mode.
Reserved	–	7:6	0H	Reserved. If these bits are read, 0 is returned for each bit.
IOCMD	R/W	5:0	00H	Specify the number of wait cycles for a command to be sent in True IDE PIO mode.

The actual number of wait cycles is *specified value* + 1.
Examples of settings when transfers are executed with a 50 MHz clock are shown on the following page.

Notes on specifying each timing parameter:

- A reference clock is CFI_CLK (CFI_HCLK). • To guarantee the cycle time IORDY
  For access other than the following:
  - I/O access (cycle time: 80 ns)
  - True IDE PIO access (modes 5 and 6)

  Because the WAITB (IORDY) signal output from a card is internally synchronized in the CFI module, specify the IOCMD bits so that the value is greater than the value of ({`twIOWR` or `twIORD` or `t2`}/clock cycles) + 2.
- To guarantee the cycle time `t0`
  Specify the IOCMD bits so that the total of the IOSET, IOCMD, and IOHLD bit values is greater than `t0`/clock cycles.

Examples of settings when transfers are executed with a 50 MHz clock (clock cycle: 20 ns)

The **Correction Value** column in the table below shows the delay value that must be added to guarantee the card specifications for the following parameters:

`tdfWT` (IORD) (max.), `tdfWT` (IOWR) (max.), `t0` (min.), and `ta` (max.)

○ Read or write in True IDE PIO mode

	Mode 0			Mode 1			Mode 2			Mode 3			
	600 ns			383 ns			240 ns			180 ns			
	Rating (ns)	Correction Value (ns)	Setting (No. of Cycles)	Rating (ns)	Correction Value (ns)	Setting (No. of Cycles)	Rating (ns)	Correction Value (ns)	Setting (No. of Cycles)	Rating (ns)	Correction Value (ns)	Setting (No. of Cycles)	
IOSET (min.)	70	0	3	50	0	2	30	0	1	30	0	1	Guaranteed delay for `t1`
IOCMD (min.)	165	345	25	125	193	15	100	100	10	80	0	4	Guaranteed delay for `t2`
IOHLD (min.)	20	0	1	15	0	0	10	0	0	70	0	3	Guaranteed delay for `t9` or `t2i`

	Mode 4			Mode 5			Mode 6			
	120 ns			100 ns			80 ns			
	Rating (ns)	Correction Value (ns)	Setting (No. of Cycles)	Rating (ns)	Correction Value (ns)	Setting (No. of Cycles)	Rating (ns)	Correction Value (ns)	Setting (No. of Cycles)	
IOSET (min.)	25	0	1	15	0	0	10	0	0	Guaranteed delay for `t1`
IOCMD (min.)	70	10	4	65	0	3	55	0	2	Guaranteed delay for `t2`
IOHLD (min.)	25	0	1	25	0	1	20	0	1	Guaranteed delay for `t9` or `t2i`

3.2.6 Version register 0

This register (Version-0: C024H) indicates information that makes up the module version.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
YEAR							
7	6	5	4	3	2	1	0
YEAR							

Name	R/W	Bit No.	After Reset	Description
Reserved	–	31:16	0000H	Reserved. If these bits are read, 0 is returned for each bit.
YEAR	R	15:0	2007H	Indicates the year of production.

3.2.7 Version register 1

This register (Version-1: C028H) indicates information that makes up the module version.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
MONTH							
7	6	5	4	3	2	1	0
DAY							

Name	R/W	Bit No.	After Reset	Description
Reserved	–	31:16	0000H	Reserved. If these bits are read, 0 is returned for each bit.
MONTH	R	15:8	02H	Indicates the month of production.
DAY	R	7:0	22H	Indicates the day of production.

3.2.8 Data register

This register (DATA: C02CH) is used to read or write the data buffer.

31	30	29	28	27	26	25	24
DATA							
23	22	21	20	19	18	17	16
DATA							
15	14	13	12	11	10	9	8
DATA							
7	6	5	4	3	2	1	0
DATA							

Name	R/W	Bit No.	After Reset	Description
DATA	R/W	31:0	0000_0000H	These bits are used to read data from or write data to the internal data buffer during a transfer between the CPU and a card. These bits can only be accessed in 2 or 4-byte units. Before using these bits, set bit 3 (DBEN) of the Extension-0 register (34H). [Read] It's used for the reading of the data buffer inside this core from CPU. [Write] Writing in data on a card is used for data buffer writing in inside this core from CPU.

3.2.9 Extension register 0

This register (Extension-0: C034H) is used to control DMA.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
DCNT							
7	6	5	4	3	2	1	0
Reserved			DBCR	DBEN	RWSL	DMAR	DMAE

Name	R/W	Bit No.	After Reset	Description
Reserved	–	31:16	0000H	Reserved. If these bits are read, 0 is returned for each bit.
DCNT	R/W	15:8	00H	Specify the number of times to execute a DMA transfer when using the data buffer. 00H: 256 times (2 bytes × the specified number of times)
Reserved	–	7:5	0H	Reserved. If these bits are read, 0 is returned for each bit.
DBCR	R/W	4	0	Specify whether to clear the data buffer. 0: Do not clear the data buffer. 1: Clear the data buffer.
DBEN	R/W	3	0	Specify whether to use the data buffer. 0: Do not use the data buffer. 1: Use the data buffer. This bit is cleared when a post-write or prefetch read operation finishes.
RWSL	R/W	2	0	Specify the timing to use the data buffer when the data buffer is used. 0: Post-write 1: Prefetch
DMAR	R/W	1	0	Specify the direction of DMA transfers. 0: Write 1: Read
DMAE	R/W	0	0	Specify whether to execute a DMA transfer. This bit is cleared when a DMA transfer finishes. 0: Do not execute 1: Execute

3.2.10 Extension register 1

This register (Extension-1: C038H) indicates the data buffer status.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
RDCNT							
7	6	5	4	3	2	1	0
Reserved						DBEMP	DBFUL

Name	R/W	Bit No.	After Reset	Description
Reserved	–	31:16	0000H	Reserved. If these bits are read, 0 is returned for each bit.
RDCNT	R	15:8	00H	Indicates the number of data bytes read during DMA read operation (in 2-byte units), or written during DMA write operation (in 2-byte units).
Reserved	–	7:2	00H	Reserved. If these bits are read, 0 is returned for each bit.
DBEMP	R	1	1	Indicates whether the data buffer is empty. 0: Not empty. 1: Empty
DBFUL	R	0	0	Indicates whether the data buffer is full. 0: Not full. 1: Full

3.2.11 Bus interface control register

This register (BUSIF_CTRL: E004H) is used to control the bus.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
FIFO USE	Reserved						
7	6	5	4	3	2	1	0
Reserved	PIO MODE	PIO_16_8B	BURST MODE		TXRXB	DMAEN	Reserved

Name	R/W	Bit No.	After Reset	Description
Reserved	–	31:16	0000H	Reserved. If these bits are read, 0 is returned for each bit.
FIFO USE	R/W	15	0	Specify whether to use the internal FIFO buffer for DMA master operation. 0: The internal FIFO buffer is not used for the bus. 1: Setting prohibited
Reserved	–	14:7	00H	Reserved. If these bits are read, 0 is returned for each bit.
PIO MODE	R/W	6	0	Select the PIO mode. 0: Setting prohibited 1: PIO mode
PIO_16_8B	R/W	5	0	Specify the width of data output to the card. 0: 8 bits 1: 16 bits
BURST MODE	R/W	4:3	00b	Specify the burst size for DMA master operation. 00: Single burst 01: Incremental 4 burst 10: Incremental 8 burst 11: Incremental 16 burst
TXRXB	R/W	2	0	Select the transfer mode for AHB master operation. 0: Reception mode 1: Transmission mode
DMAEN	R/W	1	0	Specify whether to enable DMA transfers for AHB master operation. 0: Disable 1: Enable
Reserved	–	0	0	Reserved. If this bit is read, 0 is returned.

3.2.12 TXMEM address register

This register (TXMEM_ADDR: E008H) specifies the DMA transfer address.

31	30	29	28	27	26	25	24
TXMEM ADDR							
23	22	21	20	19	18	17	16
TXMEM ADDR							
15	14	13	12	11	10	9	8
TXMEM ADDR							
7	6	5	4	3	2	1	0
TXMEM ADDR							

Name	R/W	Bit No.	After Reset	Description
TXMEM ADDR	R/W	31:0	3000_8000H	Destination to which data is transferred from the host to a card when the CFI module serves as the DMA master.

3.2.13 RXMEM address register

This register (RXMEM_ADDR: E00CH) specifies the DMA transfer address.

31	30	29	28	27	26	25	24
RXMEM ADDR							
23	22	21	20	19	18	17	16
RXMEM ADDR							
15	14	13	12	11	10	9	8
RXMEM ADDR							
7	6	5	4	3	2	1	0
RXMEM ADDR							

Name	R/W	Bit No.	After Reset	Description
RXMEM ADDR	R/W	31:0	3000_C000H	Destination to which data is transferred from a card to the host when the CFI module serves as the DMA master.

3.2.14 PIO address register

This register (PIO_ADDR: E010H) is used to specify the PIO transfer address.

31	30	29	28	27	26	25	24
PIO ADDR							
23	22	21	20	19	18	17	16
PIO ADDR							
15	14	13	12	11	10	9	8
PIO ADDR							
7	6	5	4	3	2	1	0
PIO ADDR							

Name	R/W	Bit No.	After Reset	Description
PIO ADDR	R/W	31:0	0000_0000H	Specify the True IDE PIO transfer address when the CFI module serves as the DMA master. Be sure to set bit 9 to 1 if using the secondary area in the True IDE PIO mode.

3.2.15 Sector length register

This register (SECTOR_LENGTH: E018H) specifies the transfer sector length.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved						Sector length	
7	6	5	4	3	2	1	0
Sector length							

Name	R/W	Bit No.	After Reset	Description
Reserved	–	31:10	00_0000H	Reserved. If these bits are read, 0 is returned for each bit.
Block length	R/W	9:0	000H	Specify the transfer sector length when the CFI module serves as the DMA master.

3.2.16 Block length register

This register (BLOCK_LENGTH: E01CH) specifies the transfer block length.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved						Block length	
7	6	5	4	3	2	1	0
Block length							

Name	R/W	Bit No.	After Reset	Description
Reserved	–	31:10	0C_0000H	Reserved.
Block length	R/W	9:0	00CH	Specify the transfer block length when the CFI module serves as the DMA master.

3.2.17 Block index register

This register (BLOCK_INDEX: E020H) specifies the transfer block index.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved						Block index	
7	6	5	4	3	2	1	0
Block index							

Name	R/W	Bit No.	After Reset	Description
Reserved	–	31:10	0C_0000H	Reserved.
Block index	R/W	9:0	00CH	Specify the transfer block index.

3.2.18 Transfer start register

This register (TRANS_START: E024H) controls DMA transfers.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							Trans start

Name	R/W	Bit No.	After Reset	Description
Reserved	–	31:1	1800_0006H	Reserved.
Trans start	R/W	0	0	This bit is used to trigger the start of a DMA transfer when the CFI module serves as the DMA master. This bit is cleared when the DMA transfer finishes.

3.2.19 Interrupt raw status register

This register (INT_RAW: E034H) indicates the interrupt raw status.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						ERR ADDR LATCH	DMA COMP

Name	R/W	Bit No.	After Reset	Description
Reserved	–	31:2	0C00_0003H	Reserved.
ERR ADDR LATCH	R	1	0	Indicates whether a DMA transfer error raw interrupt occurred when the CFI module serves as the DMA master. 0: Did not occur 1: Occurred
DMA COMP	R	0	0	Indicates whether a DMA transfer raw interrupt occurred when the CFI module serves as the DMA master. 0: Did not occur 1: Occurred

3.2.20 Interrupt original register

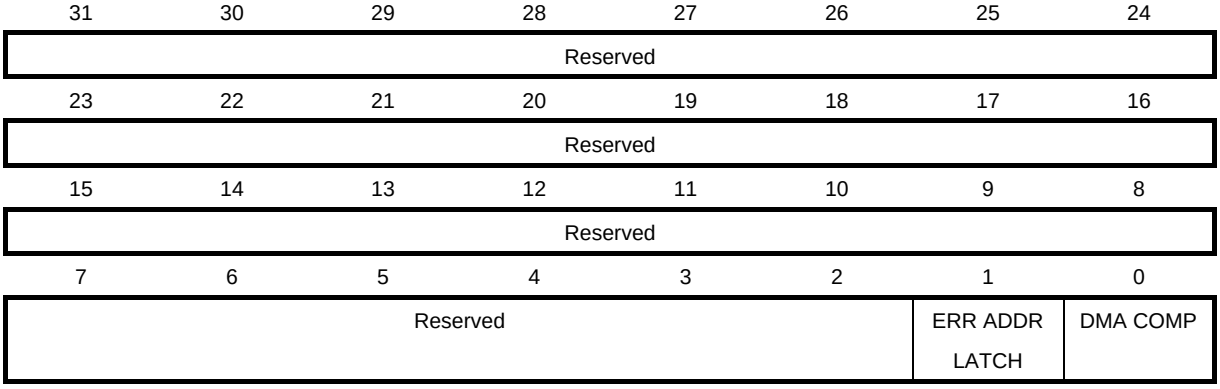
This register (INT_ORG: E038H) indicates whether an interrupt occurred or clearing the interrupt masking was reported.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						ERR ADDR LATCH	DMA COMP

Name	R/W	Bit No.	After Reset	Description
Reserved	–	31:2	0C00_0003H	Reserved.
ERR ADDR LATCH	R	1	0	Indicates whether a DMA transfer error interrupt occurred when the CFI module serves as the DMA master. Indicates also whether the interrupt masking was cancelled. 0: Did not occur 1: Occurred
DMA COMP	R	0	0	Indicates whether a DMA transfer raw interrupt occurred when the CFI module serves as the DMA master. Indicates also whether cancelling the interrupt masking was reported. 0: Did not occur 1: Occurred

3.2.21 Interrupt clear register

This register (INT_CLR: E03CH) is used to clear the interrupt issued.



Name	R/W	Bit No.	After Reset	Description
Reserved	–	31:2	0C00_0003H	Reserved.
ERR ADDR LATCH	W	1	0	Clear the DMA transfer error interrupt when the CFI module serves as the DMA master. 0: No operation 1: Clear the interrupt.
DMA COMP	W	0	0	Clear the DMA transfer raw interrupt when the CFI module serves as the DMA master. 0: No operation 1: Clear the interrupt.

4. Description of Functions

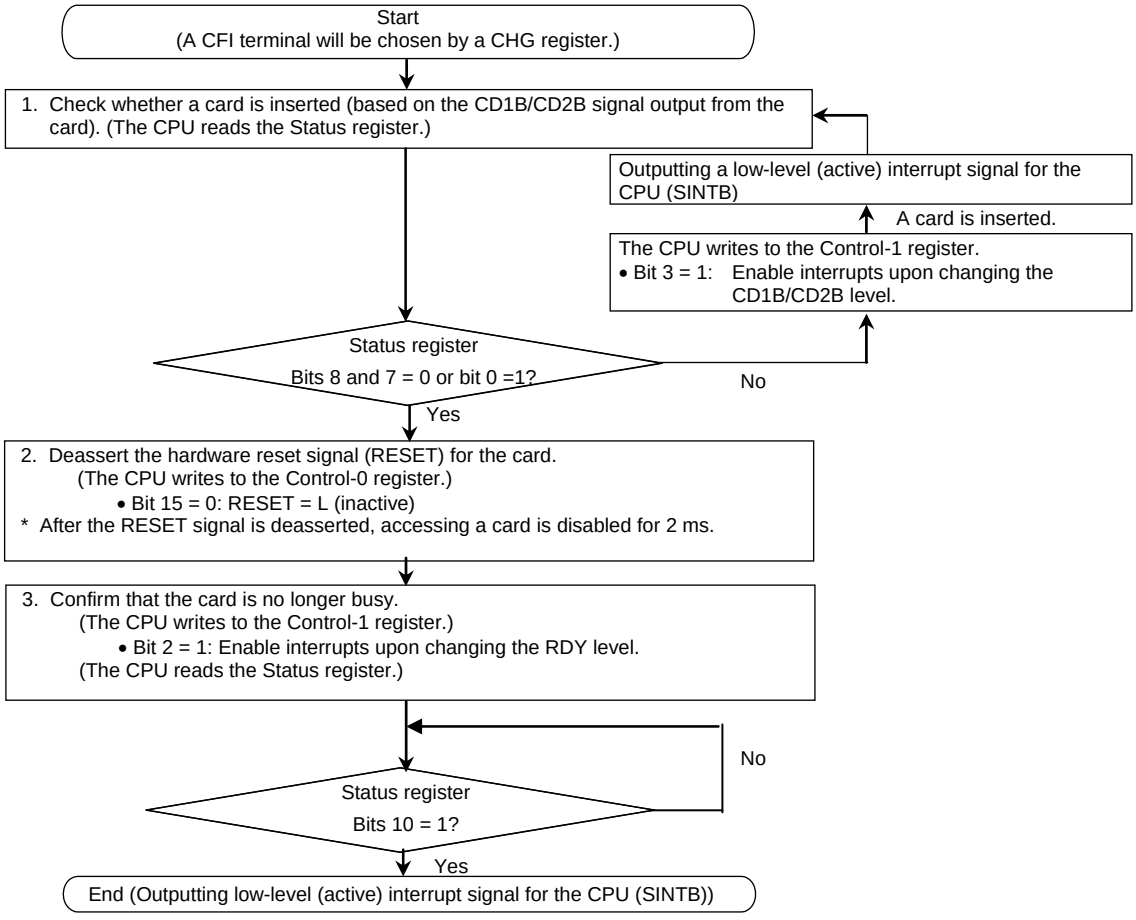
4.1 Accessing a Card

4.1.1 Initializing a card

To initialize a card, perform the procedure below.

1. Read the Status register to check whether a card is inserted.
2. Write to the Control-0 register to deassert the hardware reset signal (RESET) for the card.
3. Read the Status register to confirm that the card is no longer busy.

• Overview of card initialization



4.1.2 Accessing a card

1. Write to the Control-0 register to set up the card access interface.
   Combinations of settings other than the following are prohibited:
   • Bits [4:0] = 1000X: True IDE PIO mode

2. Specify the card access timing.
   • For the I/O or True IDE PIO access mode: Change the Timing-1 register setting.

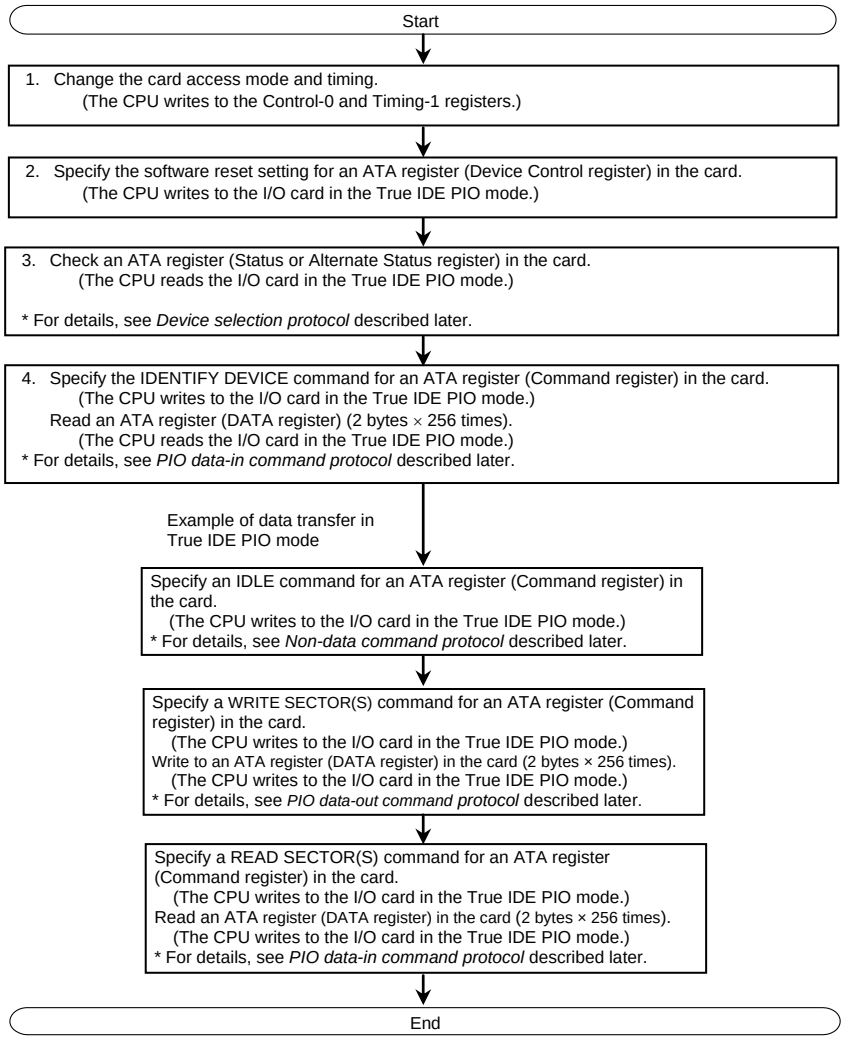
3. Set up the ATA registers in the card (the device control register, for example, that specifies the settings such as for a software reset).

Remark Each card contains a collection of data (CIS information) that provides information such as the manufacturer, product name, serial number, and features. Tuples are data structures contained in the card.

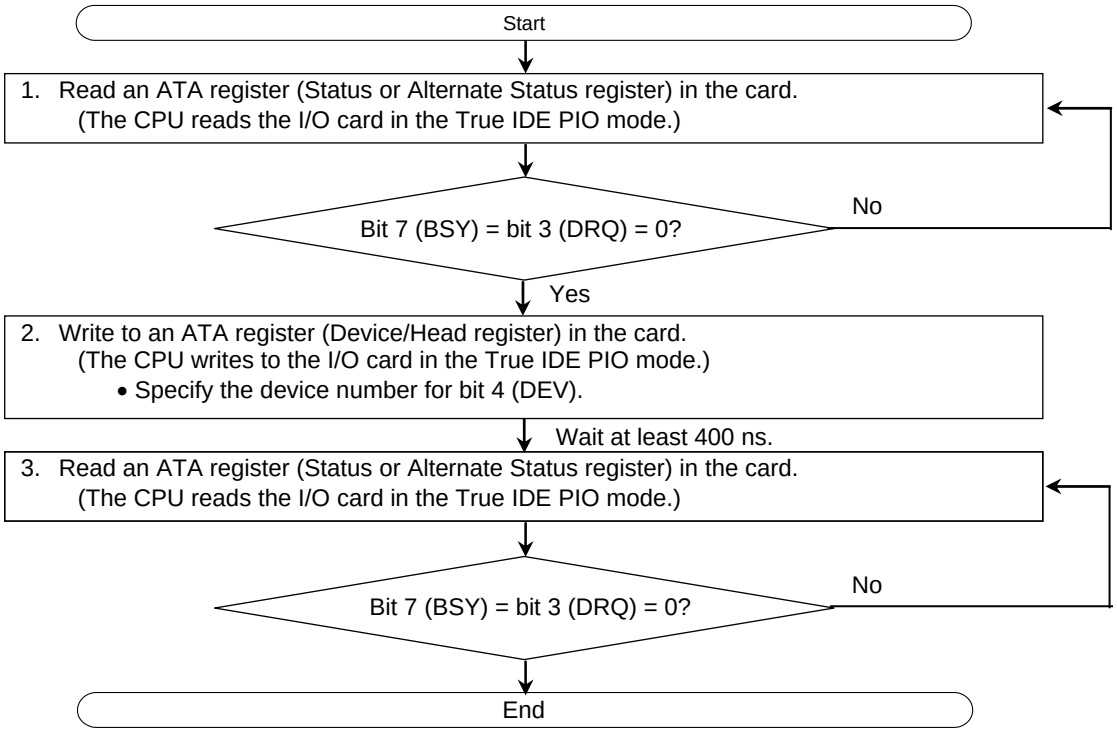
The following shows the settings and procedure for accessing each card.

- When using a CF card: Access in the True IDE PIO mode
  After the Control-0 or Timing-1 register settings are changed, the card can be read or written by the CPU.
  1. Read an ATA register (Status or Alternate Status register) in the card by using the CPU in the True IDE PIO mode.
  2. Write to an ATA register (Command register) in the card to specify the IDENTIFY DEVICE command by using the CPU in the True IDE PIO mode.
  3. Read an ATA register (DATA register) in the card by using the CPU in the True IDE PIO mode (2 bytes × 256 times).
  4. Specify a DMA command for the card.
     • Write to an ATA register (Command register) in the card to specify the READ DMA or WRITE DMA command by using the CPU in the True IDE PIO mode.

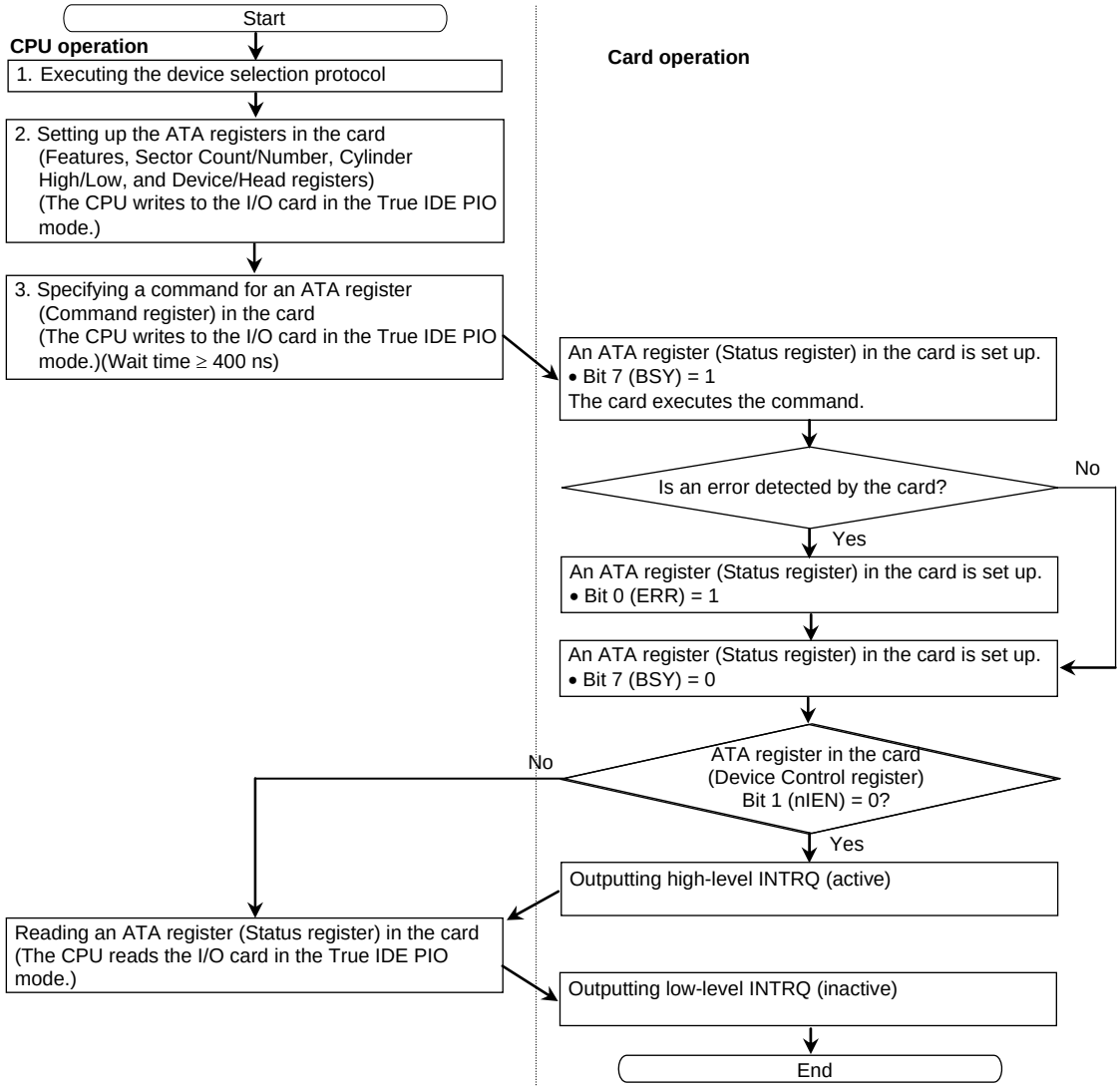
◎ Overview of accessing a card



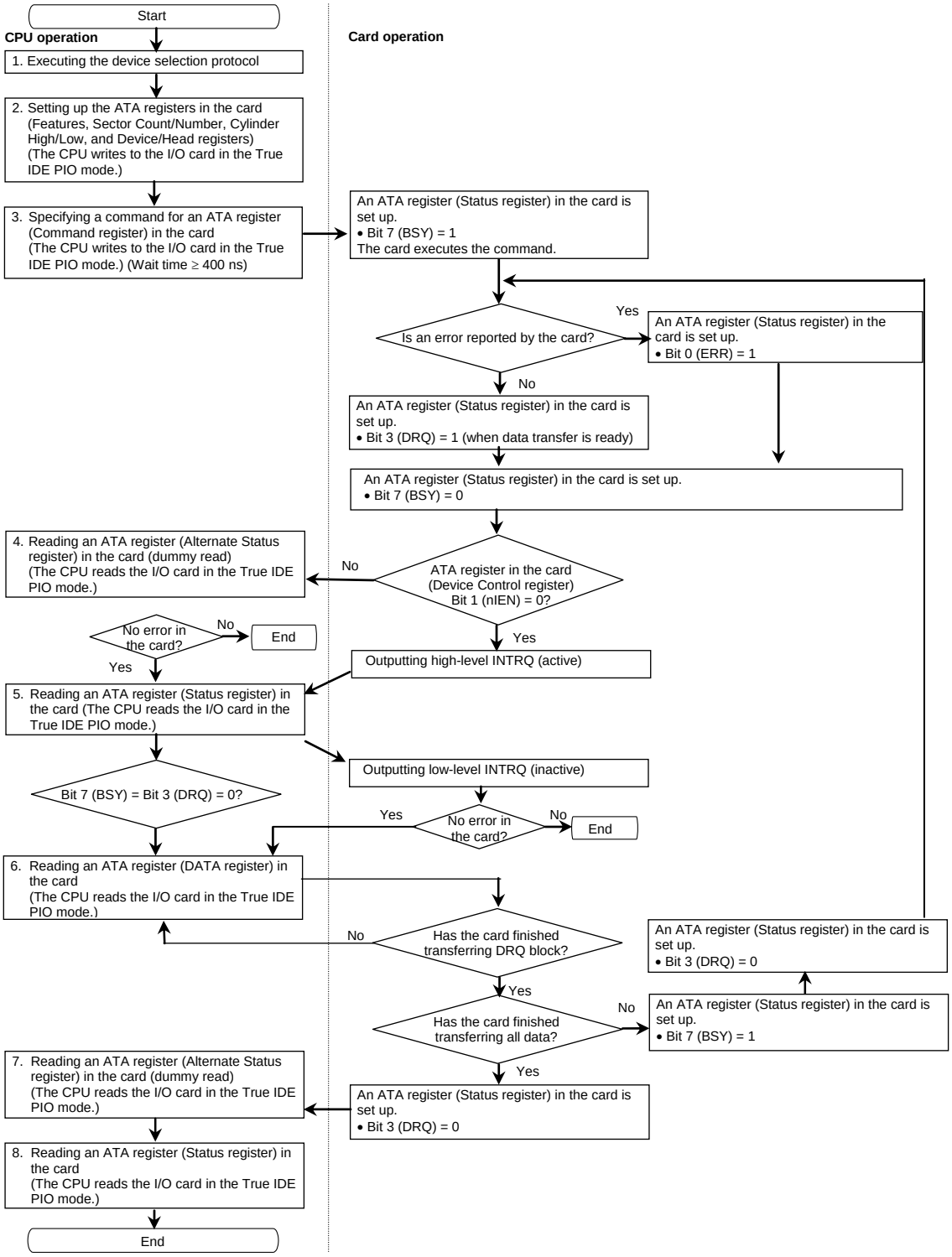
- Device selection protocol



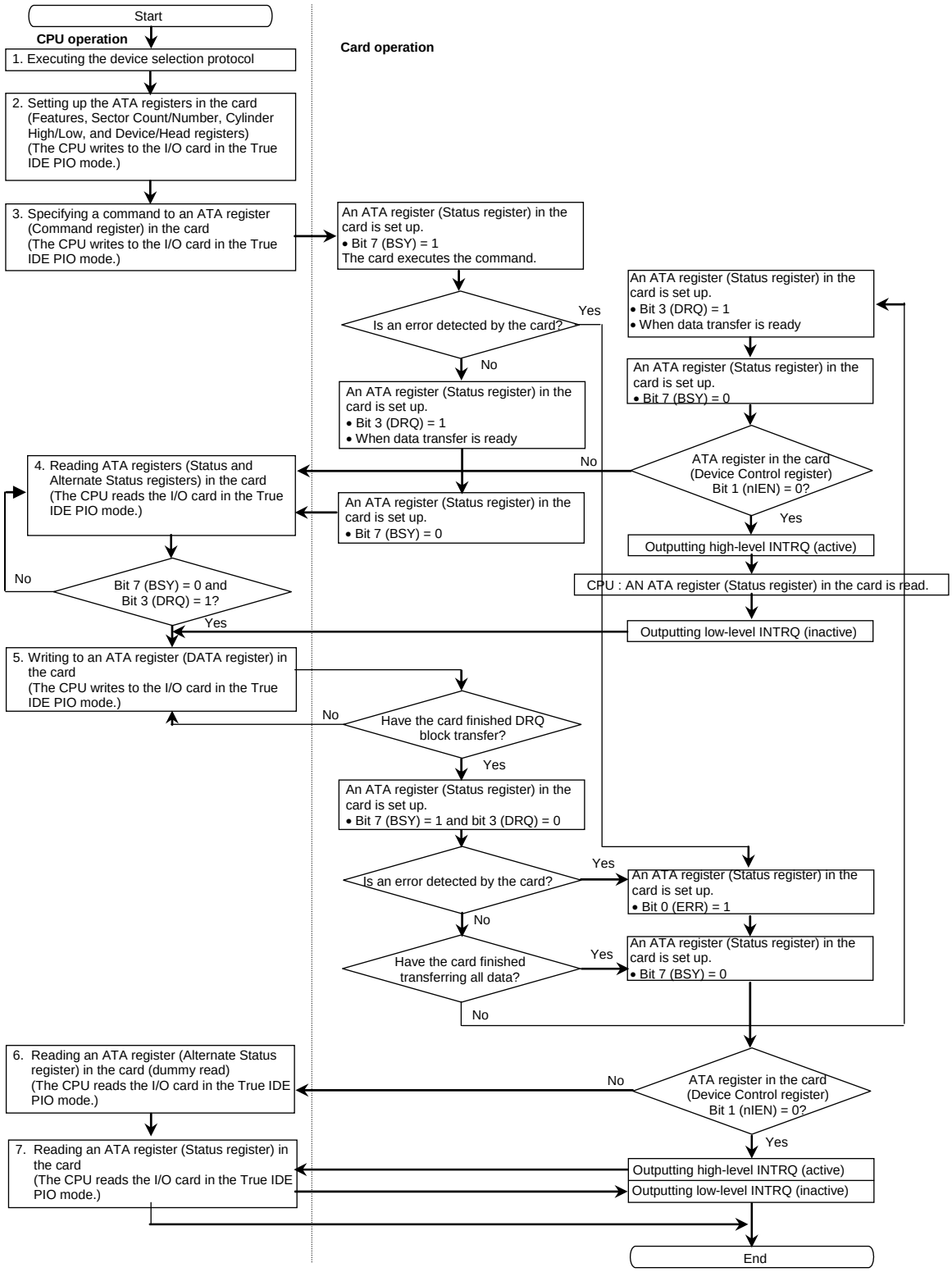
- Non-data command protocol



- PIO data-in command protocol



- PIO data-out command protocol



4.2 Bus Sizing

The primary I/O addresses prescribed by the CF specifications are 1F0H to 1F7H, 3F6H, and 3F7H, and the secondary ones are 170H to 177H, 376H, and 377H, each of which has registers in two I/O spaces. The CFI module switches the I/O spaces based on the address SA9 indicated by the CPU.

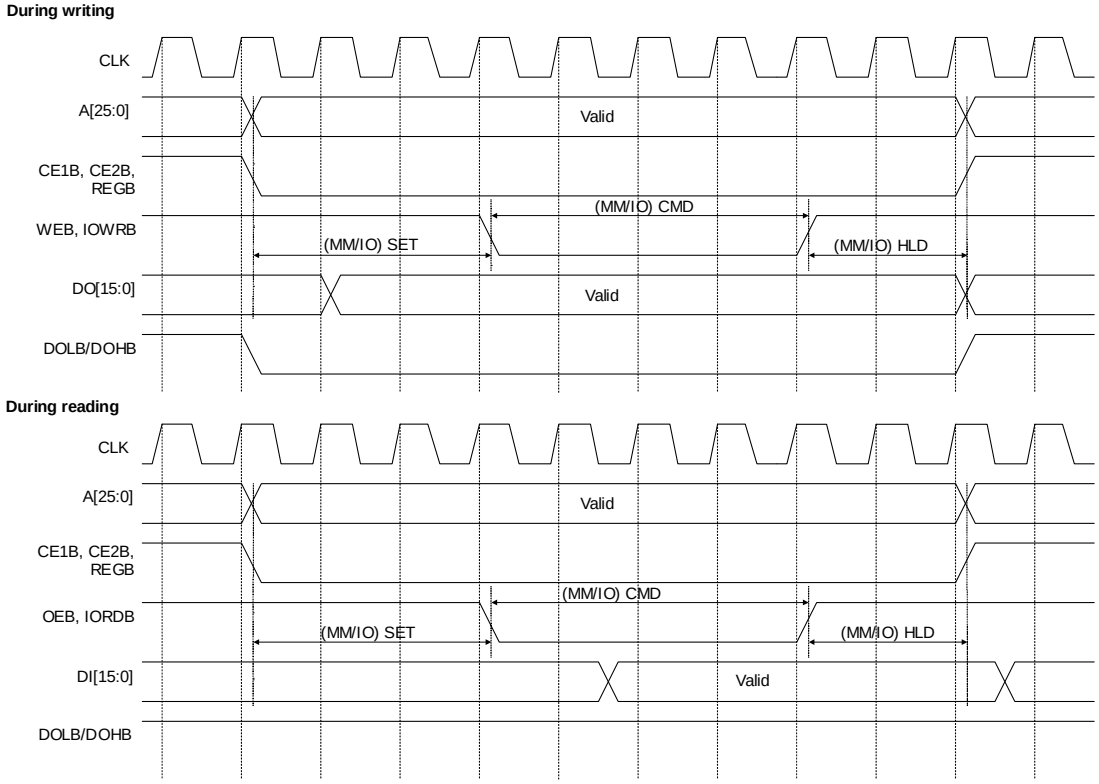
(Access in 32-bit units from the CPU is not supported.)

When accessing in 16Bit from CPU, bus sizing is performed according to the data width on the card side.

4.3 Card Access Timing

The timing registers must be set up according to the card access specifications.
The clock cycles required for the setup (SET), command (CMD), and hold (HLD) times are (*register value* + 1) × clock cycles.

- In the True IDE PIO access modes



4.4 Interrupts

The CFI module supports the following interrupt sources:

1. Inserting or removing a card (change of the CD1B and CD2B levels)
2. Change of the battery level (when using a memory card: fall of BVD1 or BVD2)
3. Change of the card status (when using an I/O card: change of the BVD1 level)
4. Change of the RDY (INTRQ) data transfer completion signal in the True IDE mode) level
5. Completion of a write by DMA
6. Completion of a read by DMA
7. Detecting the end of post-writing before the specified number of transfers is reached
8. Detecting the end of prefetching before the specified number of transfers is reached
9. Illegal access

Individual interrupts can be enabled by using the interrupt register (0CH).
The interrupt signals generated by the above sources and output to SINTB are asserted at low level.

4.5 When an error occurs during a transfer

If any of the events shown below occur during a data transfer to or from a card, the transfer becomes invalid and therefore must be restarted by resetting the CFI module[Note 1] and the card[Note 2].

1. The card is removed or inserted
   When bit 3 (CINTE) of the Control-1 register is 1 (which means that interrupts are enabled), the CFI module asserts an interrupt signal (SINTB) for the CPU. Therefore, read the Interrupt register to confirm that bit 3 (CDS) is 1.

2. The card is busy. (Card side: memory interface)
   Read the Status register to confirm that bit 10 (RDY) is 0.

Notes **1.** Set bit 15 (SRST) of the Control-1 register to 1.
2. In modes other than the True IDE mode: Set bit 15 (HRST) of the Control-0 register to 1.
In the True IDE mode: Clear bit 15 (HRST) of the Control-0 register to 0.

REVISION HISTORY	EMMA Mobile EV2 User's Manual: CF Card Interface

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		Page	Summary
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2.00	May 31, 2010	—	Incremental update from comments to the 1.0.
3.00	May 31, 2011	—	Incremental update from comments to the 2.0.

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