User's Manual

SDIO Interface

User's Manual

Multimedia Processor for Mobile Applications
EMMA Mobile ™ EV2

Renesas Electronics
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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the EMMA Mobile EV2. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Data Sheet	Hardware overview and electrical characteristics	EMMA Mobile EV2 Datasheet	R19DS0010EJxxxx
User's manual (1chip)	Hardware whole specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description	EMMA Mobile EV2 User's manual 1chip	R19UH0036EJxxxx
User's manual (module)	Hardware each macro specifications and operation description.	EMMA Mobile EV2 User's manual each module	See below

Document Name	Document No.	Document Name	Document No.
1chip	R19UH0036EJxxxx	DMA Controller	R19UH0043EJxxxx
System Management Unit	R19UH0037EJxxxx	LP-DDR/DDR2 Controller	R19UH0039EJxxxx
Timer	R19UH0054EJxxxx	SD Memory Card Interface	R19UH0061EJxxxx
System Timer	R19UH0055EJxxxx	SDIO Interface (This manual)	R19UH0042EJxxxx
HD Video Decoder	R19UH0056EJxxxx	CF Card Interface	R19UH0062EJxxxx
Rotator	R19UH0057EJxxxx	Unified Serial Interface	R19UH0047EJxxxx
Resizer	R19UH0058EJxxxx	UART interface	R19UH0040EJxxxx
Image Composer	R19UH0038EJxxxx	USB 2.0 Host Controller	R19UH0045EJxxxx
LCD Interface	R19UH0044EJxxxx	USB 2.0 Function Controller	R19UH0034EJxxxx
ITU-R BT.656 Interface	R19UH0059EJxxxx	IIC Interface	R19UH0052EJxxxx
Digital Terrestrial TV Interface	R19UH0048EJxxxx	General Purpose I/O Interface	R19UH0041EJxxxx
Camera Interface	R19UH0060EJxxxx	Pulse Width Modulation Interface	R19UH0063EJxxxx

4 digits of end shows the version.

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names

Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.

Examples the PM03 bit in the PM0 register

P3_5 pin, VCC pin

(2) Notation of Numbers

The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.

Examples Binary: 11b or 11

Hexadecimal: EFA0h

Decimal: 1234

3. Register Notation

The symbols and terms used in register diagrams are described below.

x.x.x XXX register

This register (XXXXXXX: xxxx_xxxxh) …..

7	6	5	4	3	2	1	0
Reserved		CHG_P1_LAT	LATCH_P1_SEL	Reserved		CHG_P0_LAT	CHG_P0_LAT_SEL

Name	R/W	Bit No.	After Reset	Description
LATCH_P2_SEL	R/W	8	0	0: Use the P2_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P2_LAT bit to latch data.
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P1_LAT	R/W	5	1	0: Output data as is. 1: Output latched data.
LATCH_P1_SEL	R/W	4	0	0: Use the P1_LAT bit of the P1_POWERSW register in the SMU to latch data. 1: Use the CHG_P1_LAT bit to latch data.
Reserved	R	3:2	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P0_LAT	R/W	1	1	0: Output data as is. 1: Output latched data.
CHG_P0_LAT_SEL	R/W	0	0	0: Use the P0_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P0_LAT bit to latch data.

*1 *3 *2

*1

R/W: Read and Write.

R: Read only.

W: Write only.

-: Nothing is assigned.

*2

Reserved bit.

Reserved bit. Set to specified value.

*3

・ Nothing is assigned.

Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.

・ Do not set to a value.

Operation is not guaranteed when a value is set.

・ Function varies according to the operating mode.

The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Register
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

Abbreviation	Full Form
AHB	Advanced High-performance Bus
ATA	Advanced Technology Attachment
eMMC	Embedded Multi Media Card
FIFO	First In, First Out
GPIO	General Purpose I/O
I/O	Input/Output
MMC	Multi Media Card
SDHC	SD High Capacity
SMU	System Management Unit

Table of Contents

1. Overview

This module (SDIO) is an SD card interface that complies with SD card interface Physical Layer Version 2.00. In addition to performing I/O with a card, this module can also be used as a CE-ATA drive, SDIO card, or MMC/eMMC (4.2 or equivalent) host controller.

SDIO1, 2 is MMC non-correspondence.

1.1 Features

The main features of the SDIO module are as follows:

- SD card Specification Physical Layer Specification Ver. 2.0
- SDIO card Specification Ver. 2.0
- MMC System Specification Ver. 4.2
- SD cards, SDIO cards, SDIO multifunction cards, and combo cards can be connected
- 1-bit or 4-bit SD bus
- Supports high-speed SD cards (up to 50 MHz)
  SD transfer clock does division (1-512) in the SDC as a SDC_SCLK source clock and uses.
  SDC_SCLK makes divide PLL3/PLL4/OSC0/OSC1 as a source clock, and is generated.
  Example) When choosing PLL3 (229.376MHz), it'll be 229.376/6 = 38.229MHz.
  The maximum of the clock frequency which can be chosen as a SD clock in EM/EV will be 49MHz.
  Maximum 50MHz of SD transfer clock is covered as a SDIO module element.
- Supports SDHC cards
- Supports the SDIO suspend/resume function
- Supports the SDIO read wait function
- Includes 4 KB, 3 KB, 1 KB, or 0.5 KB two-port RAM
- Includes a DMA controller
- Implements ADMA features
- Supports CE-ATA Digital Protocol 1.1
- MMC-HS (up to 52 MHz)
  SD transfer clock does division (1-512) in the SDC as a SDC_SCLK source clock and uses.
  SDC_SCLK makes divide PLL3/PLL4/OSC0/OSC1 as a source clock, and is generated.
  Example) When choosing PLL3 (229.376MHz), it'll be 229.376/6 = 38.229MHz.
  The maximum of the clock frequency which can be chosen as a SD clock in EM/EV will be 49MHz.
  Maximum 52MHz of MMC transfer clock is covered as a SDIO module element.
- Supports MMC-HC
- 1-bit, 4-bit, or 8-bit MMC bus
- Implements an AMBA 2.0 AHB master interface as the DMA interface
- Implements an AMBA 2.0 AHB slave interface as the control interface
- Supports the big endian and little endian modes
- Supplies an SD, SDIO, MMC, or CE-ATA transfer clock (0 to 52 MHz)
- Prevents FIFO buffer overruns and underruns due to the transfer clock stopping
- Supports automatic clock control, and outputs a clock request signal to the SMU when a clock is necessary

2. Pin Functions

Pin Name	I/O	Function	IO Voltage	Alternate Pin Function
SDI0_CKO	Output	SDI0 clock output	VDD33	GPIO_050
SDI0_CKI	Input	SDI0 clock output	VDD33	GPIO_051
SDI0_CMD	I/O	SDI0 command	VDD33	GPIO_052
SDI0_DATA0	I/O	SDI0 data bit 0	VDD33	GPIO_053
SDI0_DATA1	I/O	SDI0 data bit 1	VDD33	GPIO_054
SDI0_DATA2	I/O	SDI0 data bit 2	VDD33	GPIO_055
SDI0_DATA3	I/O	SDI0 data bit 3	VDD33	GPIO_056
SDI0_DATA4	I/O	SDI0 data bit 4	VDD33	GPIO_057
SDI0_DATA5	I/O	SDI0 data bit 5	VDD33	GPIO_058
SDI0_DATA6	I/O	SDI0 data bit 6	VDD33	GPIO_059
SDI0_DATA7	I/O	SDI0 data bit 7	VDD33	GPIO_060
SDI1_CKO	Output	SDI1 clock output	VDD33	GPIO_061
SDI1_CKI	Input	SDI1 clock output	VDD33	GPIO_062
SDI1_CMD	I/O	SDI1 command	VDD33	GPIO_063
SDI1_DATA0	I/O	SDI1 data bit 0	VDD33	GPIO_064
SDI1_DATA1	I/O	SDI1 data bit 1	VDD33	GPIO_065
SDI1_DATA2	I/O	SDI1 data bit 2	VDD33	GPIO_066
SDI1_DATA3	I/O	SDI1 data bit 3	VDD33	GPIO_067
SDI2_CKO	Output	SDI2 clock output	VDD33	AB_A21/GPIO_097/CF_INTRQ
SDI2_CKI	Input	SDI2 clock output	VDD33	AB_A22/GPIO_098
SDI2_CMD	I/O	SDI2 command	VDD33	AB_A23/GPIO_099
SDI2_DATA0	I/O	SDI2 data bit 0	VDD33	AB_AD12/GPIO_089/CF_D12/USI5_CS1
SDI2_DATA1	I/O	SDI2 data bit 1	VDD33	AB_AD13/GPIO_090/CF_D13/USI5_CS2
SDI2_DATA2	I/O	SDI2 data bit 2	VDD33	AB_AD14/GPIO_091/CF_D14
SDI2_DATA3	I/O	SDI2 data bit 3	VDD33	AB_AD15/GPIO_092/CF_D15

Note : Use GPIO for a CD (Card Detect) and a WP (Write Protect).

3. Registers

3.1 Register List

The SDIO registers can only be accessed by way of the AHB slave devices, and only in 32-bit units.
If register access in 16-bit or 8-bit units is attempted, it is handled as 32-bit access.

Base addresses: SDIO0: E290_0000H
SDIO1: E2A0_0000H
SDIO1: E2B0_0000H

(1/2)

Address	Register Name	Register Symbol	R/W	Reset
0000H to 0002H	Reserved	–	–	–
0004H	Block size register	SDIO_BLKSIZE	R/W	0000H
0006H	Block count register	SDIO_BLKCOUNT	R/W	0000H
0008H	Argument setting register 0	SDIO_ARG0	R/W	0000H
000AH	Argument setting register 1	SDIO_ARG1	R/W	0000H
000CH	Transfer mode setting register	SDIO_MODE	R/W	0000H
000EH	Command setting register	SDIO_CMD	R/W	0000H
0010H	Response register 0	SDIO_RSP0	R	0000H
0012H	Response register 1	SDIO_RSP1	R	0000H
0014H	Response register 2	SDIO_RSP2	R	0000H
0016H	Response register 3	SDIO_RSP3	R	0000H
0018H	Response register 4	SDIO_RSP4	R	0000H
001AH	Response register 5	SDIO_RSP5	R	0000H
001CH	Response register 6	SDIO_RSP6	R	0000H
001EH	Response register 7	SDIO_RSP7	R	00H
0020H	Buffer data port register 0	SDIO_BUF0	R/W	–
0022H	Buffer data port register 1	SDIO_BUF1	R/W	–
0024H	State register 0	SDIO_STATE0	R	0000H
0026H	State register 1	SDIO_STATE1	R	000AH
0028H	Host control setting register	SDIO_HOST	R/W	00H
0029H	Power control setting register	SDIO_POWER	R/W	00H
002AH	Block gap control setting register	SDIO_BLKGAP	R/W	00H
002BH	Wakeup control setting register	SDIO_WAKEUP	R/W	00H
002CH	Clock control setting register	SDIO_CLKCTRL	R/W	0002H
002EH	Timeout setting register	SDIO_TIMEOUT	R/W	00H
002FH	Software reset setting register	SDIO_SOFTRST	R/W	00H
0030H	Normal interrupt status register	SDIO_NRMINT_STS	R, R/W	0000H
0032H	Error interrupt status register	SDIO_ERRINT_STS	R/W	0000H
0034H	Normal interrupt status enable register	SDIO_NRMINT_STSEN	R/W	0000H
0036H	Error interrupt status enable register	SDIO_ERRINT_STSEN	R/W	0000H

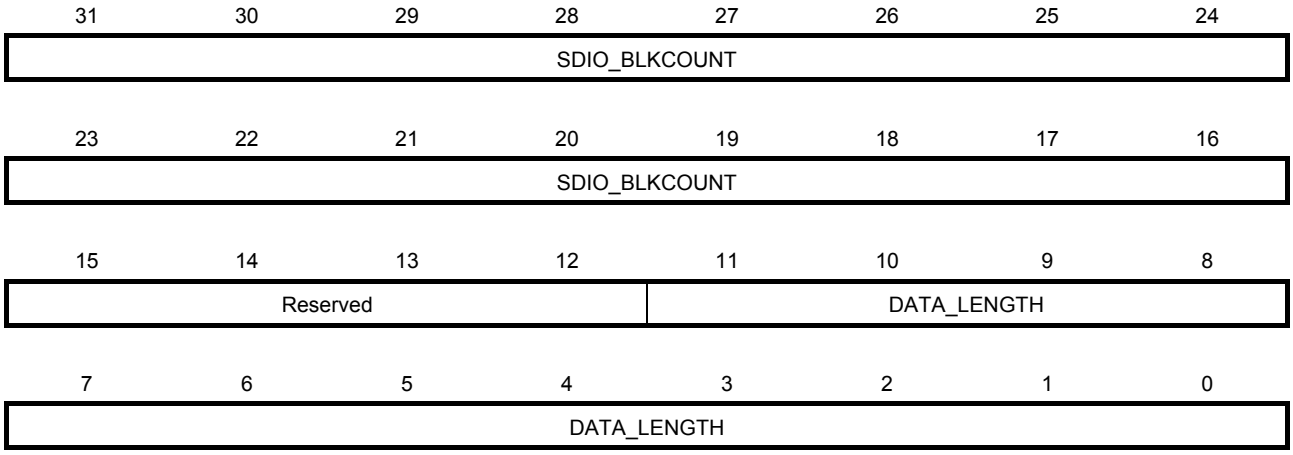
(2/2)

Address	Register Name	Register Symbol	R/W	Reset
0038H	Normal interrupt signal enable register	SDIO_NRMINT_SIGEN	R/W	0000H
003AH	Error interrupt signal enable register	SDIO_ERRINT_SIGEN	R/W	0000H
003CH	Automatic CMD12 issuance error register	SDIO_CMD12_ERR	R	0000_0000H
003EH	Reserved	–	–	–
0040H	Capability register 0	SDIO_CAP0	R	32B2H
0042H	Capability register 1	SDIO_CAP1	R	07FDH
0044H to 004EH	Reserved	–	–	–
0050H	CMD12 error interrupt force event register	SDIO_CMD12ERR_FORCE	R	0000H
0052H	Error interrupt force event register	SDIO_ERRINT_FORCE	R	0000H
0054H	ADMA1/2 error status register	SDIO_ADMA_ERR	R	0000H
0056H	Reserved	–	–	–
0058H	ADMA1/2 system address register 0 (lower 16 bits)	SDIO_ADMA_SYSADD0	R/W	0000_0000H
005AH	ADMA1/2 system address register 1 (higher 16 bits)	SDIO_ADMA_SYSADD1	R/W	0000_0000H
005CH to 007EH	Reserved	–	–	–
0080H	CE-ATA control register	SDIO_CEATA	R, R/W	0000_0010H
0082H to 00FAH	Reserved	–	–	–
00FCH	Slot interrupt status register	SDIO_SLOTINT_STS	R	00FFH
00FEH	Host controller version register	SDIO_HOSTVER	R	E101H
0100H	AHB IF control register 0	SDIO_AMBA0	R/W	0000_0000H
0102H	Reserved	–	–	–
0104H	AHB IF control register 1	SDIO_AMBA1	R/W	0000_0000H
0106H to DFFEH	Reserved	–	–	–
E000H	Clock delay setting register	SDIO_DLYCYRL	R/W	0000_0000H
E002H	Reserved	–	–	–
E004H	Module port setting register0	SDIO_GPIO0	R/W	0000_8000H
E006H	Reserved	–	–	–
E008H	Module port setting register1	SDIO_GPIO1	R/W	4000_0000H
E00AH to EFFCH	Reserved	–	–	–
F000H	Module enable register	SDIO_MODEN	R/W	0000_0000H
F002H to FFFEH	Reserved	–	–	–

3.2 Register Details

3.2.1 Block size register and block count register

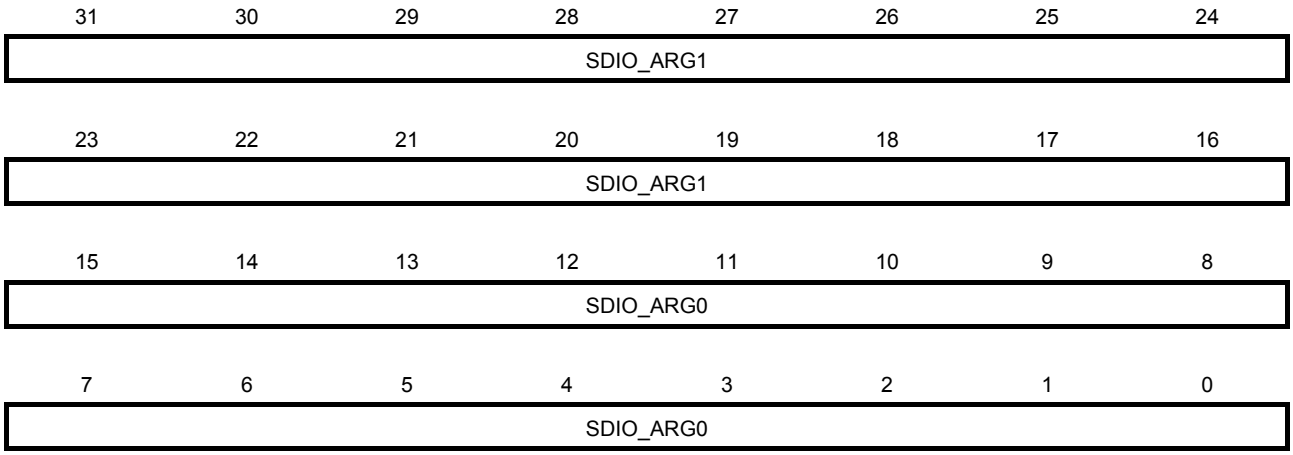
These registers (SDIO_BLKSIZE: 0004H and SDIO_BLKCOUNT: 0006H) specify the transfer data length.



Name	R/W	Bit No.	After Reset	Description
SDIO_BLKCOUNT	R/W	31:16	0000H	These bits are used to count the blocks sent by performing a multiple block transfer.
Reserved	R	15:12	0H	Reserved. If these bits are read, 0 is returned for each bit.
DATA_LENGTH	R/W	11:0	000H	Specify the transfer data length.

3.2.2 Argument setting registers 0 and 1

These registers (SDIO_ARG0: 0008H and SDIO_ARG1: 000AH) specify command arguments.



Name	R/W	Bit No.	After Reset	Description
SDIO_ARG1	R/W	31:16	0000H	Specify command arguments (in the higher 16 bits).
SDIO_ARG0	R/W	15:0	0000H	Specify command arguments (in the lower 16 bits).

ex) When setting 0x1234_5678 as an argument, 0x1234 is set as SDIO_ARG1 and 0x5678 is set as SDIO_ARG0.

3.2.3 Transfer mode setting register and command setting register

These registers (SDIO_MODE: 000CH and SDIO_CMD: 000EH) specify the transfer mode and the command to transfer.

31	30	29	28	27	26	25	24
Reserved		CMD_INDEX					

23	22	21	20	19	18	17	16
CMD_TYPE		DATA_ PRESENT	CMD_INDEX_ CHK	CMD_CRC_ CHK	Reserved	RESP_TYPE	

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved		MULTI	TRANS_DIR	Reserved	AUTO_ CMD12_EN	BLK_COUNT_ EN	DMA_EN

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:30	0H	Reserved. If these bits are read, 0 is returned for each bit.
CMD_INDEX	R/W	29:24	00H	Specify the command to transfer. If the command completion signal disable (CCSD) signal is issued while bits 5 and 3 of the SDIO_CEATA register are 1, the setting of these bits is invalid.
CMD_TYPE	R	23:22	01b	Indicates the command type. 00: Normal command 01: Suspend (CMD52 to write to the BR bit of the bus suspend register) 10: Resume (CMD52 to select a function) 11: Abort (CMD12 or CMD52 to abort IO)
DATA_PRESENT	R/W	21	0	Specify whether to send data. 0: Do not send data 1: Send data
CMD_INDEX_CHK	R/W	20	0	Specify whether to enable checking command indexes. 0: Disable 1: Enable
CMD_CRC_CHK	R/W	19	0	Specify whether to enable checking CRC7 in commands. 0: Disable 1: Enable
Reserved	R	18	0	Reserved. If this bit is read, 0 is returned.

(2/2)

Name	R/W	Bit No.	After Reset	Description
RESP_TYPE	R/W	17:16	00b	Specify the expected response type. 00: No response 01: 136-bit response 10: 48-bit response without a busy status 11: 48-bit response with a busy status
Reserved	R	15:6	000H	Reserved. If these bits are read, 0 is returned for each bit.
MULTI	R/W	5	0	Specify the transfer type. 0: Single transfer 1: Multiple block transfer
TRANS_DIR	R/W	4	0	Specify the direction to transfer data. 0: Write transfer 1: Read transfer
Reserved	R	3	0	Reserved. If this bit is read, 0 is returned.
AUTO_CMD12_EN	R/W	2	0	Specify whether to enable automatic CMD12 transfers. 0: Disable 1: Enable
BLK_COUNT_EN	R/W	1	0	Specify whether to enable block counting. 0: Disable 1: Enable
DMA_EN	R/W	0	0	Specify whether to enable DMA transfers. 0: Disable 1: Enable

3.2.4 Response registers 0 and 1

These registers (SDIO_RSP0: 0010H and SDIO_RSP1: 0012H) are used to store response data.

31	30	29	28	27	26	25	24
SDIO_RSP1							

23	22	21	20	19	18	17	16
SDIO_RSP1							

15	14	13	12	11	10	9	8
SDIO_RSP0							

7	6	5	4	3	2	1	0
SDIO_RSP0							

Name	R/W	Bit No.	After Reset	Description
SDIO_RSP1	R	31:16	0000H	Store response data R39 to R24 in these bits.
SDIO_RSP0	R	15:0	0000H	Store response data R23 to R8 in these bits.

3.2.5 Response registers 2 and 3

These registers (SDIO_RSP2: 0014H and SDIO_RSP3: 0016H) are used to store response data.

31	30	29	28	27	26	25	24
SDIO_RSP3							

23	22	21	20	19	18	17	16
SDIO_RSP3							

15	14	13	12	11	10	9	8
SDIO_RSP2							

7	6	5	4	3	2	1	0
SDIO_RSP2							

Name	R/W	Bit No.	After Reset	Description
SDIO_RSP3	R	31:16	0000H	Store response data R71 to R56 in these bits.
SDIO_RSP2	R	15:0	0000H	Store response data R55 to R40 in these bits.

3.2.6 Response registers 4 and 5

These registers (SDIO_RSP4: 0018H and SDIO_RSP5: 001AH) are used to store response data.

31	30	29	28	27	26	25	24
SDIO_RSP5							

23	22	21	20	19	18	17	16
SDIO_RSP5							

15	14	13	12	11	10	9	8
SDIO_RSP4							

7	6	5	4	3	2	1	0
SDIO_RSP4							

Name	R/W	Bit No.	After Reset	Description
SDIO_RSP5	R	31:16	0000H	Store response data R103 to R88 in these bits.
SDIO_RSP4	R	15:0	0000H	Store response data R87 to R72 in these bits.

3.2.7 Response registers 6 and 7

These registers (SDIO_RSP6: 001CH and SDIO_RSP7: 001EH) are used to store response data.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
SDIO_RSP7							

15	14	13	12	11	10	9	8
SDIO_RSP6							

7	6	5	4	3	2	1	0
SDIO_RSP6							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:24	00H	Reserved. If these bits are read, 0 is returned for each bit.
SDIO_RSP7	R	23:16	00H	Store response data R127 to R120 or automatically-issued CMD12 command response data R39 to R24 in these bits.
SDIO_RSP6	R	15:0	0000H	Store response data R119 to R104 or automatically-issued CMD12 command response data R23 to R8 in these bits.

3.2.8 Buffer data port registers 0 and 1

These registers (SDIO_BUF0: 0020H and SDIO_BUF1: 0022H) are used to store buffer data.

31	30	29	28	27	26	25	24
SDIO_BUF1							

23	22	21	20	19	18	17	16
SDIO_BUF1							

15	14	13	12	11	10	9	8
SDIO_BUF0							

7	6	5	4	3	2	1	0
SDIO_BUF0							

Name	R/W	Bit No.	After Reset	Description
SDIO_BUF1	R/W	31:16	–	Store buffer data in the higher 16 bits.
SDIO_BUF0	R/W	15:0	–	Store buffer data in the lower 16 bits.

3.2.9 State registers 0 and 1

These registers (SDIO_STATE0: 0024H and SDIO_STATE1: 0026H) indicate various statuses.

31	30	29	28	27	26	25	24
DAT7	DAT6	DAT5	DAT4	Reserved			CMD

23	22	21	20	19	18	17	16
DAT3	DAT2	DAT1	DAT0	Reserved			

15	14	13	12	11	10	9	8
Reserved				RDEN	WREN	RD_ACTIVE	WR_ACTIVE

7	6	5	4	3	2	1	0
Reserved					DAT_ACTIVE	DAT_INHIBIT	CMD_INHIBIT

(1/2)

Name	R/W	Bit No.	After Reset	Description
DAT7	R	31	0	Indicates the DAT7 line level.
DAT6	R	30	0	Indicates the DAT6 line level.
DAT5	R	29	0	Indicates the DAT5 line level.
DAT4	R	28	0	Indicates the DAT4 line level.
Reserved	R	27:25	000b	Reserved. If these bits are read, 0 is returned for each bit.
CMD	R	24	1	Indicates the CMD line level.
DAT3	R	23	1	Indicates the DAT3 line level.
DAT2	R	22	1	Indicates the DAT2 line level.
DAT1	R	21	1	Indicates the DAT1 line level.
DAT0	R	20	1	Indicates the DAT0 line level.
Reserved	R	19:12	10100000b	Reserved. If these bits are read, 0 is returned for each bit.
RDEN	R	11	0	Indicates whether reading the data buffer is enabled. 0: Disabled 1: Enabled
WREN	R	10	0	Indicates whether writing the data buffer is enabled. 0: Disabled 1: Enabled
RD_ACTIVE	R	9	0	Indicates the read transfer status. 0: Inactive 1: Active
WR_ACTIVE	R	8	0	Indicates the write transfer status. 0: Inactive 1: Active
Reserved	R	7:3	00H	Reserved. If these bits are read, 0 is returned for each bit.
DAT_ACTIVE	R	2	0	Indicates the DAT line status. 0: Inactive 1: Active

(2/2)

Name	R/W	Bit No.	After Reset	Description
DAT_INHIBIT	R	1	0	Indicates whether issuing commands for data transfer is enabled. 0: Enabled (DAT line enabled) 1: Disabled
CMD_INHIBIT	R	0	0	Indicates whether issuing commands is enabled. 0: Enabled 1: Disabled

3.2.10 Host control setting, power control, block gap control, and wakeup control setting registers

These registers (SDIO_HOST: 0028H, SDIO_POWER: 0029H, SDIO_BLKGAP: 002AH, and SDIO_WAKEUP: 002BH) specify the settings for the host controller, power, block gap, and wakeup signal.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved				BLKGAP_INT_EN	READ_WAIT	CONTINU_REQ	STOP_AT_BG_REQ

15	14	13	12	11	10	9	8
Reserved				VOLT			Reserved

7	6	5	4	3	2	1	0
Reserved		MMC8B	DMASEL		HS	WIDTH	Reserved

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:20	000H	Reserved. If these bits are read, 0 is returned for each bit.
BLKGAP_INT_EN	R/W	19	0	Specify whether to enable block gap interrupts. 0: Disable 1: Enable
READ_WAIT	R/W	18	0	Specify whether to enable keeping the read operation waiting. 0: Disable 1: Enable
CONTINU_REQ	R/W	17	0	Specify whether to enable resuming interrupted data transfers. 0: Disable 1: Enable
STOP_AT_BG_REQ	R/W	16	0	Specify whether to enable stopping data transfers at block gaps. 0: Disable 1: Enable If this bit is set to 1, be sure to set the READ_WAIT bit to 1. If this bit is set to 1, CMD12 is not issued automatically even if such issuance is specified.
Reserved	R	15:12	0H	Reserved. If these bits are read, 0 is returned for each bit.
VOLT	R/W	11:9	000b	The voltage value of the SD bus is indicated. (The function to which the IO voltage is changed isn't being supported.) 101: 1.8 V 110: 3.0 V 111: 3.3 V

(2/2)

Name	R/W	Bit No.	After Reset	Description
POWER	R/W	8	0	Specify the SD bus power status. 0: Power on 1: Power off
Reserved	R	7:6	0H	Reserved. If these bits are read, 0 is returned for each bit.
MMC8B	R/W	5	0	Specify whether to enable wider MMC data (8 bits). 0: Disable. The width specified for the WIDTH bit is used. 1: Enable. The width is 8 bits.
DMASEL	R/W	4:3	00b	Specify the DMA type. 00: No selection 01: 32-bit ADMA1 10: 32-bit ADMA2 11: 64-bit ADMA2
HS	R/W	2	0	Specify the SD card interface mode. 0: Normal mode (The signal is output at falling edges.) 1: High-speed mode (The signal is output at rising edges.)
WIDTH	R/W	1	0	Specify the data bus width. 0: 1 bit 1: 4 bits
Reserved	R	0	0	Reserved. If this bit is read, 0 is returned.

3.2.11 Clock control, timeout, and software reset setting registers

These registers (SDIO_CLKCTRL: 002CH, SDIO_TIMEOUT: 002EH, and SDIO_SOFTRST: 002EH) are used to reset control blocks and specify the clock settings.

31	30	29	28	27	26	25	24
Reserved					SRST_DAT	SRST_CMD	SRST_ALL

23	22	21	20	19	18	17	16
Reserved				TOUT_COUNT			

15	14	13	12	11	10	9	8
SDIOLKDIV							

7	6	5	4	3	2	1	0
Reserved					SDIOLKEN	CLKSTA	CLKEN

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:27	00H	Reserved. If these bits are read, 0 is returned for each bit.
SRST_DAT	R/W	26	0	This bit is used to reset the following data control blocks: • Buffer data port registers 0 and 1 • State registers 0 and 1 • Block gap control setting register • Normal interrupt status register 0: Cancels a reset 1: Reset
SRST_CMD	R/W	25	0	This bit is used to reset the following command control blocks: • State registers 0 and 1 • Normal interrupt status register 0: Cancels a reset 1: Reset
SRST_ALL	R/W	24	0	This bit is used to reset all control blocks except the following: • DAT[7:0], CMD, WP, CD, STABLE, and INSERT bits of SDIO_STATE1 register • Capability registers 0 and 1 0: Cancels a reset 1: Reset
Reserved	R	23:20	0H	Reserved. If these bits are read, 0 is returned for each bit.

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Name	R/W	Bit No.	After Reset	Description
TOUT_COUNT	R/W	19:16	0000b	Specify the number of SDIO_TCLK cycles before a transfer times out due to no data being sent. 0000: 2^{13} cycles 0001: 2^{14} cycles 0010: 2^{15} cycles 0011: 2^{16} cycles 0100: 2^{17} cycles 0101: 2^{18} cycles 0110: 2^{19} cycles 0111: 2^{20} cycles 1000: 2^{21} cycles 1001: 2^{22} cycles 1010: 2^{23} cycles 1011: 2^{24} cycles 1100: 2^{25} cycles 1101: 2^{26} cycles 1110: 2^{27} cycles 1111: Reserved
SDIOLKDIV	R/W	15:8	00H	Specify the divisor for generating the count clock. 0H: Undivided 1H: Divide by 2 2H: Divide by 4 4H: Divide by 8 8H: Divide by 16 10H: Divide by 32 20H: Divide by 64 40H: Divide by 128 80H: Divide by 256
Reserved	R	7:3	00H	Reserved. If these bits are read, 0 is returned for each bit.
SDIOLKEN	R/W	2	0	Specify whether to start or stop the SD transfer clock. (Terminal control of SDCLK) 0: Stop 1: Start
CLKSTA	R	1	1	Indicates the internal clock status. After setting "1" as CLKEN, when a clock became stable, “1” is set by this bit.. 0: Not stable 1: Stable
CLKEN	R/W	0	0	Specify whether to start or stop the internal clock. **Be sure to set it as "1".** 0: Stop 1: Start

3.2.12 Normal interrupt status register and error interrupt status register

These registers (SDIO_NRMINT_STS: 0030H and SDIO_ERRINT_STS: 0032H) indicate the status of normal interrupts and error interrupts and clear the interrupt sources.

31	30	29	28	27	26	25	24
Reserved						ADMA_ERR	CMD12_ERR

23	22	21	20	19	18	17	16
Reserved	DATA_END	DATA_CRC	DATA_TOUT	CMD_INDEX	CMD_END	CMD_CRC	CMD_TOUT

15	14	13	12	11	10	9	8
ERR	Reserved						CARD

7	6	5	4	3	2	1	0
Reserved		RREADY	WREADY	DMA	BGE	TRANCOMP	CMDCOMP

(1/3)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:26	00H	Reserved. If these bits are read, 0 is returned for each bit.
ADMA_ERR	R/W	25	0	Indicates whether an ADMA1/ADMA2 error interrupt occurred and is used to clear the source. When DMA_ERR was asserted in DMA_EN=1, or a data transfer error was on the SD bus, and occurred, this bit is set by 1. (When ADMA1/2 is an enable.)
CMD12_ERR	R/W	24	0	Indicates whether an automatic CMD12 issuance error interrupt occurred and is used to clear the source. Logical sum of each bit of Auto CMD12 Error Status Register is reflected.
Reserved	R	23	0	Reserved. If this bit is read, 0 is returned.
DATA_END	R/W	22	0	Indicates whether a data end bit error interrupt occurred and is used to clear the source. Indicates whether a data end bit error of read data or a data end bit error of write CRC status.
DATA_CRC	R/W	21	0	Indicates whether a data CRC error interrupt occurred and is used to clear the source. Indicates whether a CRC error of read data or a CRC status error of CRC token.
DATA_TOUT	R/W	20	0	Indicates whether a data timeout error interrupt occurred and is used to clear the source.
CMD_INDEX	R/W	19	0	Indicates whether a command index error interrupt occurred and is used to clear the source. Disagreement of a command index and a response index is indicated.

(2/3)

Name	R/W	Bit No.	After Reset	Description
CMD_END	R/W	18	0	Indicates whether a command end bit error interrupt occurred and is used to clear the source. Indicates whether a data end bit error of command response.
CMD_CRC	R/W	17	0	Indicates whether a command CRC error interrupt occurred and is used to clear the source. Indicates whether a command CRC error or command conflict error.
CMD_TOUT	R/W	16	0	Indicates whether a command timeout error interrupt occurred and is used to clear the source. The command timeout error when the response doesn't return in the 128 SDCLK cycle, or a command conflict error is indicated.
ERR	R	15	0	Indicates whether an error interrupt occurred. Logical sum of each bit of Error Interrupt Status Register is reflected.
Reserved	R	14:9	00H	Reserved. If these bits are read, 0 is returned for each bit.
CARD	R	8	0	Indicates whether an SDIO card interrupt occurred. Even if 1 is written in this register, this bit isn't cleared. An interrupt factor on a SDIO card is cleared to clear this bit. CARD_EN of a normal interrupt status enable register latches the value of this bit internally at 1.
Reserved	R	7:6	0H	Reserved. If these bits are read, 0 is returned for each bit.
RREADY	R/W	5	0	Indicates whether a buffer read ready interrupt occurred and is used to clear the source. When RDEN of State register 0 transferred in 1, this bit is set by 1. When the last block was forwarded when Auto CMD12 was an enable, before this bit is set by 1, Auto CMD12 is issued.
WREADY	R/W	4	0	Indicates whether a buffer write ready interrupt occurred and is used to clear the source. When WREN of State register 0 transferred in 1, this bit is set by 1. Clear this bit before writing in in a buffer.
DMA	R/W	3	0	Indicates whether a block size DMA interrupt occurred and is used to clear the source. When the interior counter reached the designated value in Host DMA Buffer Boundary, it's set. Attributes in Descriptor which refers during transmission Tran and INT When the bit is set, the data transfer established in Data length is to finish, and it's set. When End and the INT bit are set, Attributes will be set immediately. (In case of ADMA)
BGE	R/W	2	0	Indicates whether a block gap event interrupt occurred and is used to clear the source. The next block gap timing requested in Stop At Block Gap Request is indicated.

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Name	R/W	Bit No.	After Reset	Description
TRANCOMP	R/W	1	0	Indicates whether a data transfer completion interrupt occurred and is used to clear the source. It's indicated at the timing of completion of data transaction including completion at a block gap by Stop At Block Gap Request. When an error was detected by the time of data transaction, this bit isn't set. When Auto CMD12 is an enable, before this bit is set by 1, Auto CMD12 is issued.
CMDCOMP	R/W	0	0	Indicates whether a command completion (response reception) interrupt occurred and is used to clear the source. When the last bit of the command response is received, this bit is set by 1. In case of the command which doesn't require the response, this bit is set by 1 just after the command issue.

Remark 0: Did not occur 1: Occurred

Note : It's possible to clear an interrupt factor by writing "1" in each bit.

3.2.13 Normal interrupt status enable register and error interrupt status enable register

These registers (SDIO_NRMINT_STSEN: 0034H and SDIO_ERRINT_STSEN: 0036H) specify whether to enable normal interrupts and error interrupts.

31	30	29	28	27	26	25	24
Reserved		CEATA_ERR_EN	Reserved			ADMA_ERR_EN	CMD12_ERR_EN

23	22	21	20	19	18	17	16
Reserved	DATA_END_EN	DATA_CRC_EN	DATA_TOUT_EN	CMD_INDEX_EN	CMD_END_EN	CMD_CRC_EN	CMD_TOUT_EN

15	14	13	12	11	10	9	8
Reserved							CARD_EN

7	6	5	4	3	2	1	0
Reserved		RREADY_EN	WREADY_EN	DMA_BLKSIZ_EN	BGE_EN	TRANCOMP_EN	CMDCOMP_EN

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:30	0H	Reserved. If these bits are read, 0 is returned for each bit.
CEATA_ERR_EN	R/W	29	0	Specify whether to enable CE-ATA error interrupts.
Reserved	R	28:26	0H	Reserved. If these bits are read, 0 is returned for each bit.
ADMA_ERR_EN	R/W	25	0	Specify whether to enable ADMA1/ADMA2 error interrupts.
CMD12_ERR_EN	R/W	24	0	Specify whether to enable automatic CMD12 issuance error interrupts.
Reserved	R	23	0	Reserved. If this bit is read, 0 is returned.
DATA_END_EN	R/W	22	0	Specify whether to enable data end bit error interrupts.
DATA_CRC_EN	R/W	21	0	Specify whether to enable data CRC error interrupts.
DATA_TOUT_EN	R/W	20	0	Specify whether to enable data timeout error interrupts.
CMD_INDEX_EN	R/W	19	0	Specify whether to enable command index error interrupts.
CMD_END_EN	R/W	18	0	Specify whether to enable command end bit error interrupts.
CMD_CRC_EN	R/W	17	0	Specify whether to enable command CRC error interrupts.
CMD_TOUT_EN	R/W	16	0	Specify whether to enable command timeout error interrupts.
Reserved	R	15:9	00H	Reserved. If these bits are read, 0 is returned for each bit.
CARD_EN	R/W	8	0	Specify whether to enable SDIO card interrupts.
Reserved	R	7:6	0H	Reserved. If these bits are read, 0 is returned for each bit.
RREADY_EN	R/W	5	0	Specify whether to enable buffer read ready interrupts.
WREADY_EN	R/W	4	0	Specify whether to enable buffer write ready interrupts.
DMA_BLKSIZ_EN	R/W	3	0	Specify whether to enable block size DMA interrupts.
BGE_EN	R/W	2	0	Specify whether to enable block gap event interrupts.
TRANCOMP_EN	R/W	1	0	Specify whether to enable data transfer completion interrupts.

(2/2)

Name	R/W	Bit No.	After Reset	Description
CMDCOMP_EN	R/W	0	0	Specify whether to enable command completion (response reception) interrupts.

Remark 0: Disable 1: Enable

Note The factor enable by this register is reflected by SDIO_NRMINT_STS register and SDIO_ERRINT_STS register.. The factor disable isn't reflected.

3.2.14 Normal interrupt signal enable register and error interrupt signal enable register

These registers (SDIO_NRMINT_SIGEN: 0038H and SDIO_ERRINT_SIGEN: 003AH) specify whether to enable normal interrupt and error interrupt signals.

31	30	29	28	27	26	25	24
Reserved		CEATA_ERR_SIGEN	Reserved			ADMA_ERR_SIGEN	CMD12_ERR_SIGEN

23	22	21	20	19	18	17	16
Reserved	DATA_SIGEND_SIGEN	DATA_CRC_SIGEN	DATA_TOUT_SIGEN	CMD_INDEX_SIGEN	CMD_SIGEND_SIGEN	CMD_CRC_SIGEN	CMD_TOUT_SIGEN

15	14	13	12	11	10	9	8
Reserved							CARD_SIGEN

7	6	5	4	3	2	1	0
Reserved		RREADY_SIGEN	WREADY_SIGEN	DMA_SIGEN	BGE_SIGEN	TRANCOMP_SIGEN	CMDCOMP_SIGEN

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:30	0H	Reserved. If these bits are read, 0 is returned for each bit.
CEATA_ERR_SIGEN	R/W	29	0	Specify whether to enable the CE-ATA error interrupt signal.
Reserved	R	28:26	0H	Reserved. If these bits are read, 0 is returned for each bit.
ADMA_ERR_SIGEN	R/W	25	0	Specify whether to enable the ADMA1/ADMA2 error interrupt signal.
CMD12_ERR_SIGEN	R/W	24	0	Specify whether to enable the automatic CMD12 issuance error interrupt signal.
Reserved	R	23	0	Reserved. If this bit is read, 0 is returned.
DATA_SIGEND_SIGEN	R/W	22	0	Specify whether to enable the data end bit error interrupt signal.
DATA_CRC_SIGEN	R/W	21	0	Specify whether to enable the data CRC error interrupt signal.
DATA_TOUT_SIGEN	R/W	20	0	Specify whether to enable the data timeout error interrupt signal.
CMD_INDEX_SIGEN	R/W	19	0	Specify whether to enable the command index error interrupt signal.
CMD_SIGEND_SIGEN	R/W	18	0	Specify whether to enable the command end bit error interrupt signal.
CMD_CRC_SIGEN	R/W	17	0	Specify whether to enable the command CRC error interrupt signal.
CMD_TOUT_SIGEN	R/W	16	0	Specify whether to enable the command timeout error interrupt signal.
Reserved	R	15:9	00H	Reserved. If these bits are read, 0 is returned for each bit.
CARD_SIGEN	R/W	8	0	Specify whether to enable the SDIO card interrupt signal.
Reserved	R	7:6	0H	Reserved. If these bits are read, 0 is returned for each bit.
RREADY_SIGEN	R/W	5	0	Specify whether to enable the buffer read ready interrupt signal.
WREADY_SIGEN	R/W	4	0	Specify whether to enable the buffer write ready interrupt signal.
DMA_SIGEN	R/W	3	0	Specify whether to enable the block size DMA interrupt signal.
BGE_SIGEN	R/W	2	0	Specify whether to enable the block gap event interrupt signal.

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Name	R/W	Bit No.	After Reset	Description
TRANCOMP_SIGEN	R/W	1	0	Specify whether to enable the data transfer completion interrupt signal.
CMDCOMP_SIGEN	R/W	0	0	Specify whether to enable the command completion (response reception) interrupt signal.

Remark 0: Disable 1: Enable

Note : It falls below the interrupt factor made effective at this register and is reflected by a status register. (An invalidated interrupt factor isn't reflected.).
When the interrupt factor made effective here occurs, SDIx_INT active.

3.2.15 Automatic CMD12 issuance error register

This register (SDIO_CMD12_ERR: 003CH) indicates the automatic command issuance status.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
CMD12_NOT_ISSUE	Reserved		CMD12_INDEX_ERR	CMD12_ENDBIT_ERR	CMD12_CRC_ERR	CMD12_TIMEOUT_ERR	CMD12_NOT_EXEC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:8	00_0000H	Reserved. If these bits are read, 0 is returned for each bit.
CMD12_NOT_ISSUE	R	7	0	Indicates whether a data transfer command was issued in response to a CMD12 error occurring for the previous data transfer command. 0: Issued 1: Not issued
Reserved	R	6:5	0H	Reserved. If these bits are read, 0 is returned for each bit.
CMD12_INDEX_ERR	R	4	0	Indicates whether a CMD12 index error occurred. 0: Did not occur 1: Occurred
CMD12_ENDBIT_ERR	R	3	0	Indicates whether a CMD12 end bit error occurred. 0: Did not occur 1: Occurred
CMD12_CRC_ERR	R	2	0	Indicates whether a CMD12 CRC error occurred. 0: Did not occur 1: Occurred
CMD12_TIMEOUT_ERR	R	1	0	Indicates whether a CMD12 timeout error occurred. 0: Did not occur 1: Occurred
CMD12_NOT_EXEC	R	0	0	Indicates whether a CMD12 issuance error occurred. 0: Did not occur 1: Occurred

3.2.16 Capability registers 0 and 1

These registers (SDIO_CAP0: 0040H and SDIO_CAP1: 0042H) indicate various bus interface settings.

31	30	29	28	27	26	25	24
Reserved			B64	Reserved	V18	V30	V33

23	22	21	20	19	18	17	16
SUSREG	DMA	HS	ADMA1	ADMA2	MMC8	MAX_BLEN	

15	14	13	12	11	10	9	8
Reserved		BCLK_FREQ					

7	6	5	4	3	2	1	0
TCLK_UNIT	Reserved	TCLK_FREQ					

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:29	0H	Reserved. If these bits are read, 0 is returned for each bit.
B64	R	28	0	Indicates whether the 64-bit system bus is supported. 0: Not supported 1: Supported
Reserved	R	27	0	Reserved. If this bit is read, 0 is returned.
V18	R	26	1	Indicates whether the 1.8 V SD bus is supported. 0: Not supported 1: Supported
V30	R	25	1	Indicates whether the 3.0 V SD bus is supported. 0: Not supported 1: Supported
V33	R	24	1	Indicates whether the 3.3 V SD bus is supported. 0: Not supported 1: Supported
SUSREG	R	23	1	Indicates whether the suspend/resume function is supported. 0: Not supported 1: Supported
DMA	R	22	1	Indicates whether DMA transfers are supported. 0: Not supported 1: Supported
HS	R	21	1	Indicates whether the high-speed mode is supported. 0: Not supported 1: Supported
ADMA1	R	20	1	Indicates whether ADMA1 is supported. 0: Not supported 1: Supported

(2/2)

Name	R/W	Bit No.	After Reset	Description
ADMA2	R	19	1	Indicates whether ADMA2 is supported. 0: Not supported 1: Supported
MMC8	R	18	1	Indicates whether the 8-bit MMC bus is supported. 0: Not supported 1: Supported
MAX_BLEN	R	17:16	01b	Indicates the maximum block length. The size designated by this bit can be read and written in a buffer in SDIO Controller. (It can be forwarded without wait cycle.) 00: 512 bytes 01: 1,024 bytes 10: 2,048 bytes 11: 4,096 bytes (only when CE-ATA is supported)
Reserved	R	15:14	0	Reserved. If these bits are read, 0 is returned for each bit.
BCLK_FREQ	R	13:8	110010b	Indicates the base clock frequency. Maximum frequency of a SD clock is indicated. The unit = [MHz]
TCLK_UNIT	R	7	1	Indicates the unit of the clock frequency used for determining timeout occurrence. 0: Undefined 1: MHz
Reserved	R	6	0	Reserved. If this bit is read, 0 is returned.
TCLK_FREQ	R	5:0	110010b	Indicates the timeout clock frequency.

3.2.17 CMD12 error interrupt force event register and error interrupt force event register

These registers (SDIO_CMD12ERR_FORCE: 0050H and SDIO_ERRINT_FORCE: 0052H) indicate the forced error interrupt event.

31	30	29	28	27	26	25	24
Reserved		CEATA_ERR	Reserved			ADMA_ERR	CMD12_ERR

23	22	21	20	19	18	17	16
Reserved	DATA_END	DATA_CRC	DATA_TOUT	CMD_INDEX	CMD_END	CMD_CRC	CMD_TOUT

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
CMD12_NOT_ISSUE	Reserved		CMD12_INDEX_ERR	CMD12_ENDBIT_ERR	CMD12_CRC_ERR	CMD12_TIMEOUT_ERR	CMD12_NOT_EXEC

Name	R/W	Bit No.	After Reset	Description
				See the error interrupt status register (described in *3.2.13*) and *3.2.16 Automatic CMD12 issuance error register*.

3.2.18 ADMA1/2 error status register

This register (SDIO_ADMA_ERR: 0054H) indicates the ADMA error status.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved					ADMA_MIS_ERR	ADMA_ERR_STS	

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:3	0000_0000H	Reserved. If these bits are read, 0 is returned for each bit.
ADMA_MIS_ERR	R	2	0	Indicates whether an ADMA error occurred. 0: Did not occur. 1: Occurred.
ADMA_ERR_STS	R	1:0	00b	Indicates the ADMA1/ADMA2 status after an ADMA error occurs. 00: ST_STOP (DMA stopped) The value of the system address register maintains the address next to Error Descriptor. 01: ST_FDS (Description fetched) The value of the system address register maintains the address next to Error Descriptor. 10: SD_CARD (Address changed) 11: ST_TFR (Data transferred) The value of the system address register maintains the address next to Error Descriptor.

Remark An ADMA error occurs under the following conditions:

1. When block counting is enabled and the total data length obtained from the descriptor table differs from the total data length calculated using the number of blocks and data length.
2. When the data length is not an even multiple of the block length.

3.2.19 ADMA1/2 system address registers 0 and 1

These registers (SDIO_ADMA_SYSADD0: 0058H and SDIO_ADMA_SYSADD1: 005AH) specify the system memory address used for ADMA.

31	30	29	28	27	26	25	24
SDIO_ADMA_SYSADD1							

23	22	21	20	19	18	17	16
SDIO_ADMA_SYSADD1							

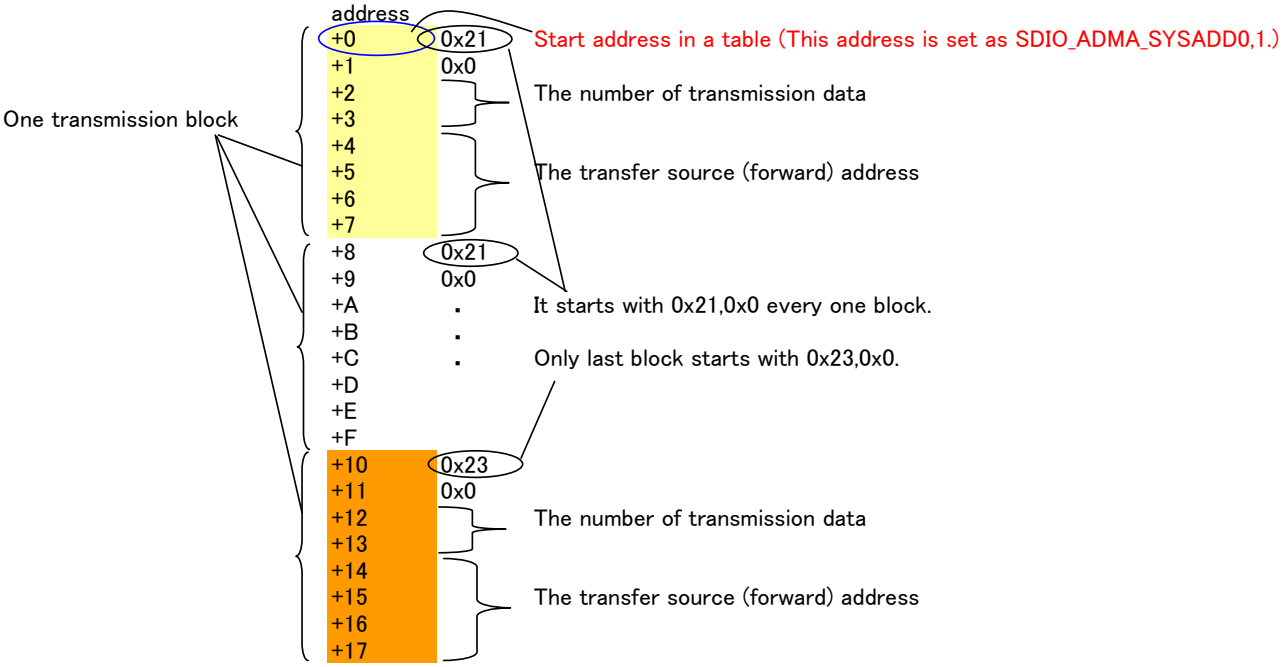
15	14	13	12	11	10	9	8
SDIO_ADMA_SYSADD0							

7	6	5	4	3	2	1	0
SDIO_ADMA_SYSADD0							

Name	R/W	Bit No.	After Reset	Description
ADMA_SYSADD1	R/W	31:16	0000H	Specify the system memory address used for ADMA (in the higher 16 bits).
ADMA_SYSADD0	R/W	15:0	0000H	Specify the system memory address used for ADMA (in the lower 16 bits).

When using ADMA, the following table is made and start address in the table is set as SDIO_ADMA_SYSADD0,1.

The example which hangs ADMA transmission to 3 blocks



3.2.20 CE-ATA control register

This register (SDIO_CEATA: 0080H) sets up the CE-ATA commands.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

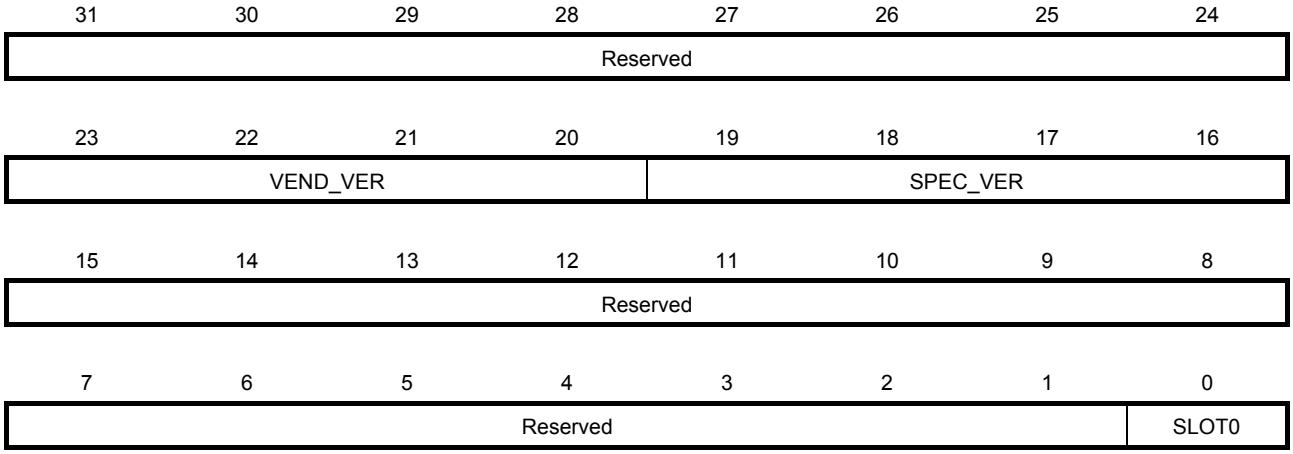
15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved		CMERR_CMP_EN	CE_ATA_MON	CE_ATA_EN	PDRV_DISEN	CM_CMP_DIS_EN	CM_CMP_EM

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:6	000_0000H	Reserved. If these bits are read, 0 is returned for each bit.
CMERR_CMP_EN	R	5	0	Indicates whether issuing the command completion signal disable (CCSD) signal is enabled when a CE-ATA command error occurs. 0: Disabled 1: Enabled
CE_ATA_MON	R	4	1	Indicates whether CE-ATA is supported. 0: Not supported 1: Supported
CE_ATA_EN	R/W	3	0	Specify whether to enable the CE_ATA features. 0: Disable 1: Enable
PDRV_DISEN	R/W	2	0	Specify whether to enable the command line P drive. 0: Enable 1: Disable
CM_CMP_DIS_EN	R/W	1	0	Specify whether to enable the command completion signal disable (CCSD) signal. 0: Disable 1: Enable
CM_CMP_EN	R/W	0	0	Specify whether to enable the command completion signal (CCS). 0: Disable 1: Enable

3.2.21 Slot interrupt status register and host controller version register

These registers (SDIO_SLOTINT_STS: 00FCH and SDIO_HOSTVER: 00FEH) indicate the slot interrupt status, the vendor code, and SD Association specifications supported by the host controller.

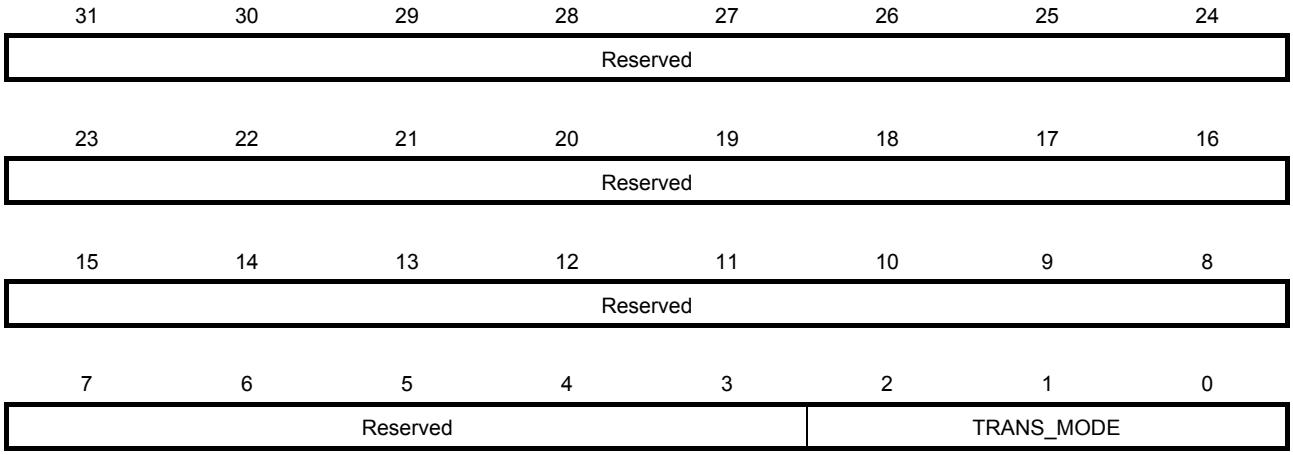


Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:24	00H	Reserved. If these bits are read, E1H is returned for each bit.
VEND_VER	R	23:20	0000b	Indicates the vendor code.
SPEC_VER	R	19:16	0001b	Indicates the version of the SD Association specifications supported by the host controller (Specification Ver. 2.0).
Reserved	R	15:1	000000001111111b	Reserved. If these bits are read, 0 is returned for each bit.
SLOT0	R	0	1	Indicates whether an interrupt from slot 0 occurred. Logical sum of interruption and wake-up 0: Did not occur 1: Occured

Remarks If the interrupt signal or wakeup signal is 1, an interrupt occurred.

3.2.22 AHB IF control register 0

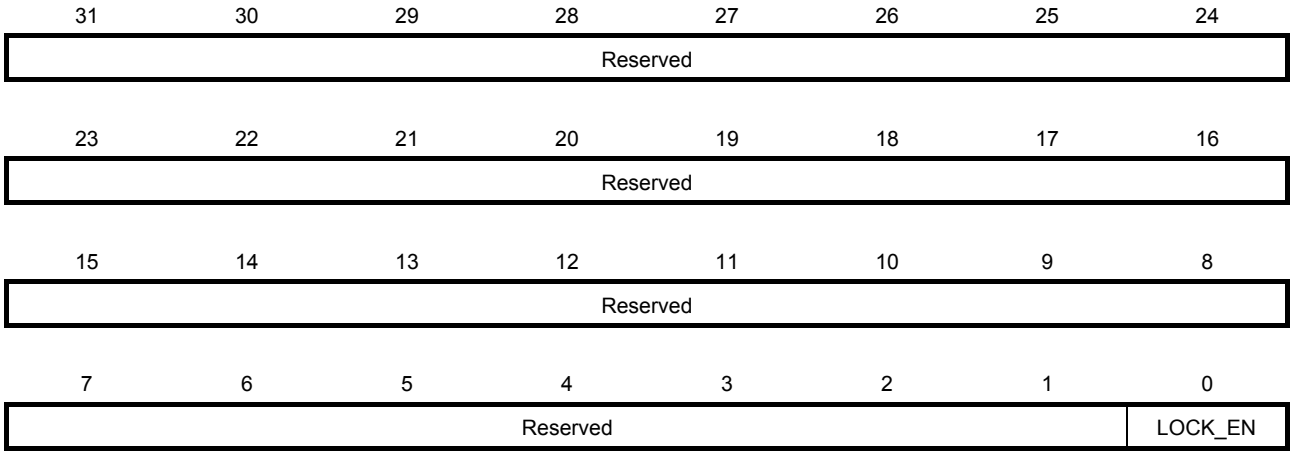
This register (SDIO_AMBA0: 0100H) specifies the AHB transfer protocol.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:3	0000_0000H	Reserved. If these bits are read, 0 is returned for each bit.
TRANS_MODE	R/W	2:0	000b	Specify the AHB transfer protocol. 000: 4-burst incremental transfer 001: 8-burst incremental transfer 010: 16-burst incremental transfer 011: Incremental transfer 1xx: Single transfer

3.2.23 AHB IF control register 1

This register (SDIO_AMBA1: 0104H) enables AHB lock transfers.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	0000_0000H	Reserved. If these bits are read, 0 is returned for each bit.
LOCK_EN	R/W	0	0	Specify whether to enable AHB lock transfers. 0: Disable 1: Enable It may be set as both.

3.2.24 Clock delay setting register

This register (SDIO_DLYCTRL: E000H) specifies the phase and delay for the module clock.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

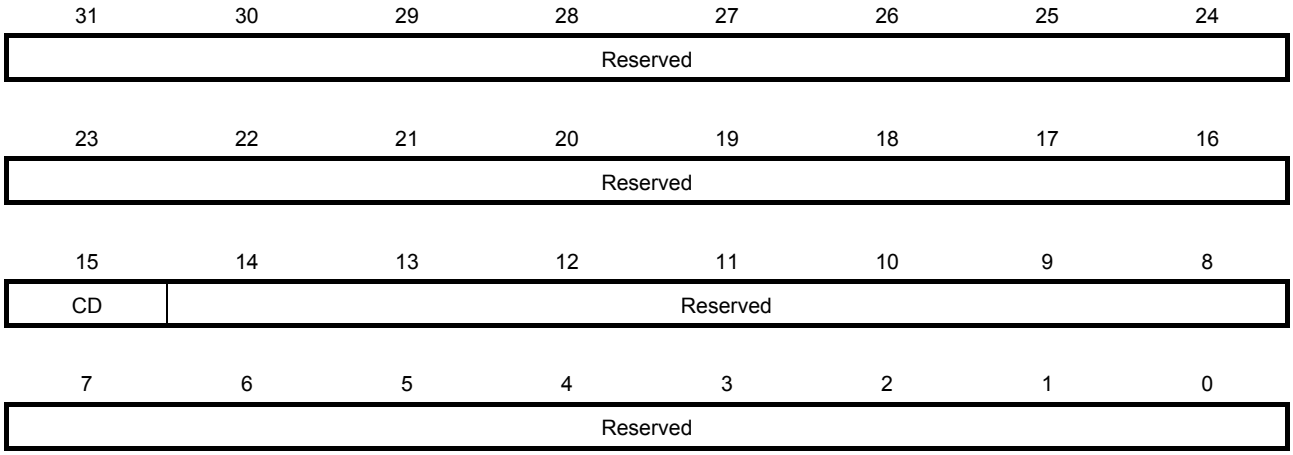
15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved			INV	Reserved			

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:5	000_0000H	Reserved. If these bits are read, 0 is returned for each bit.
INV	R/W	4	0	A clock for latches of an input data (SDIO_SCLK input from outside), a positive logic or a negative logic is chosen. 0: positive logic 1: negative logic
Reserved	R	3:0	0H	Reserved. If these bits are read, 0 is returned for each bit.

3.2.25 Module port setting register 0

This register (SDIO_GPIO0: E004H) specifies the SDIO module port.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:16	0000H	Reserved. If these bits are read, 0 is returned for each bit.
CD	R/W	15	1	Card detect 0 : Detection 1 : Non-detection
Reserved	R	14:0	0000H	The setting can't be changed from defaults.

Note : If card detection is performed, set 0 in a bit [15].

3.2.26 Module port setting register 1

This register (SDIO_GPIO1: E008H) specifies the SDIO module port.

31	30	29	28	27	26	25	24
Reserved		INTSEL	Reserved				

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							

Name	R/W	Bit No.	After Reset	Description
Reserved	R/W	31:30	01b	The setting can't be changed from defaults.
INTSEL	R/W	29	0	Polarity of interrupt 1 : Reverse
Reserved	R	28:0	00_0000H	The setting can't be changed from defaults.

Note : When using SDIx_INT, be sure to set "1" in a bit [29].

3.2.27 Module enable register

This register (SDIO_MODEN: F000H) specifies whether to enable the SDIO module.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

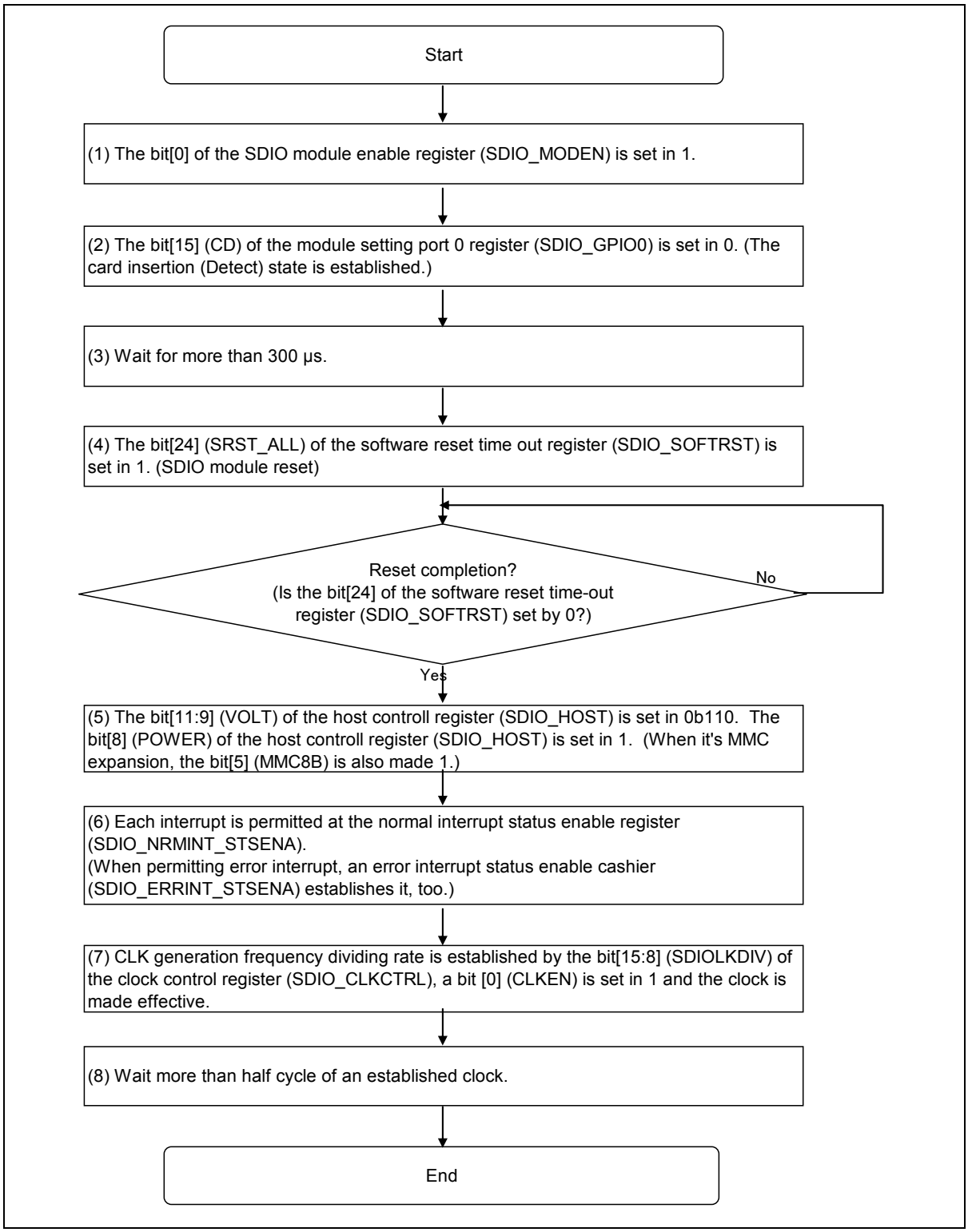
7	6	5	4	3	2	1	0
Reserved							MODEEN

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	0000_0000H	Reserved. If these bits are read, 0 is returned for each bit.
MODEEN	R/W	0	0	Specify whether to enable the SDIO module. 0: Disable 1: Enable

4. Usage

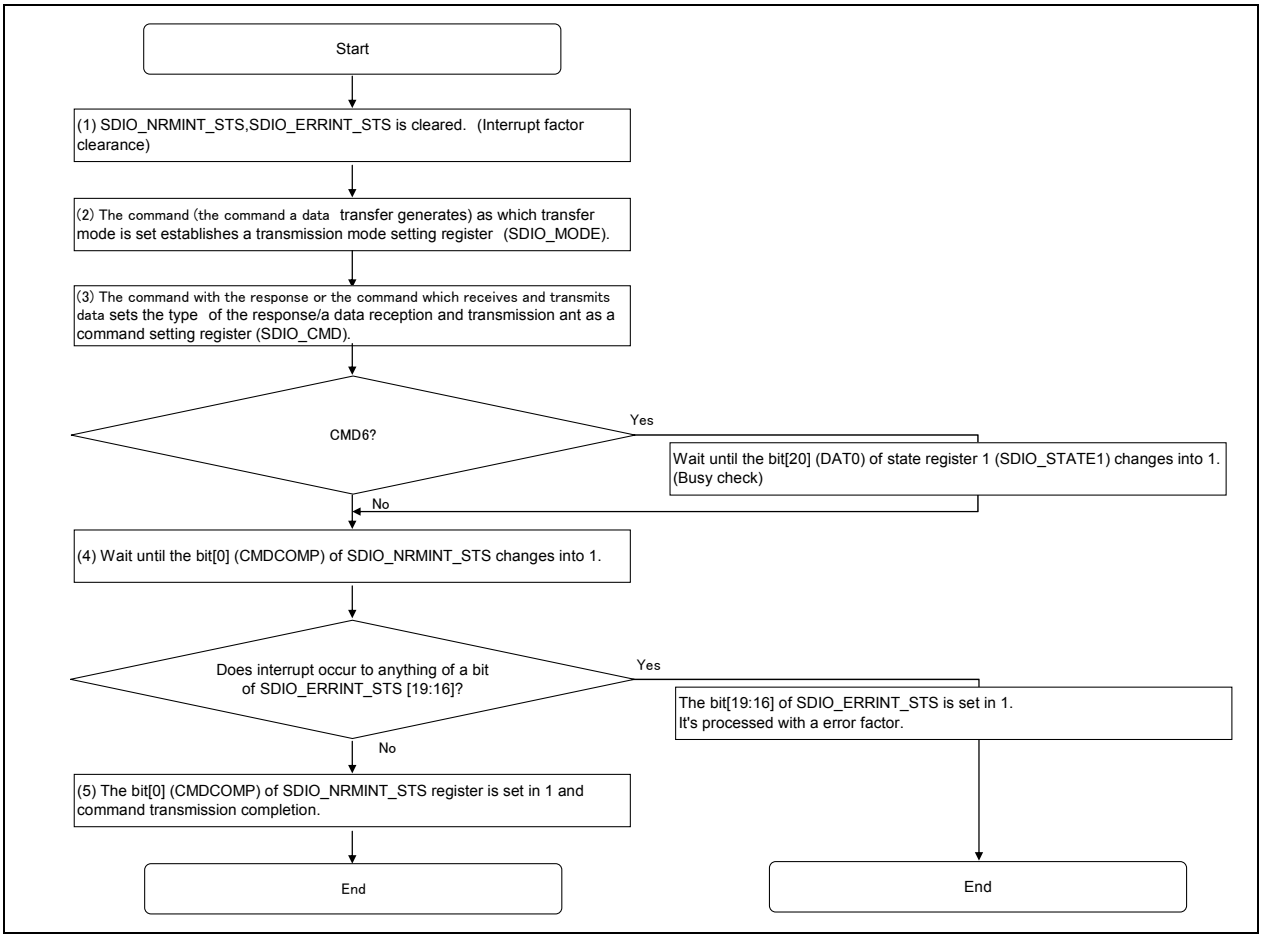
4.1 SDIO module initialization flow

Figure 4-1. SDIO module initialization flow



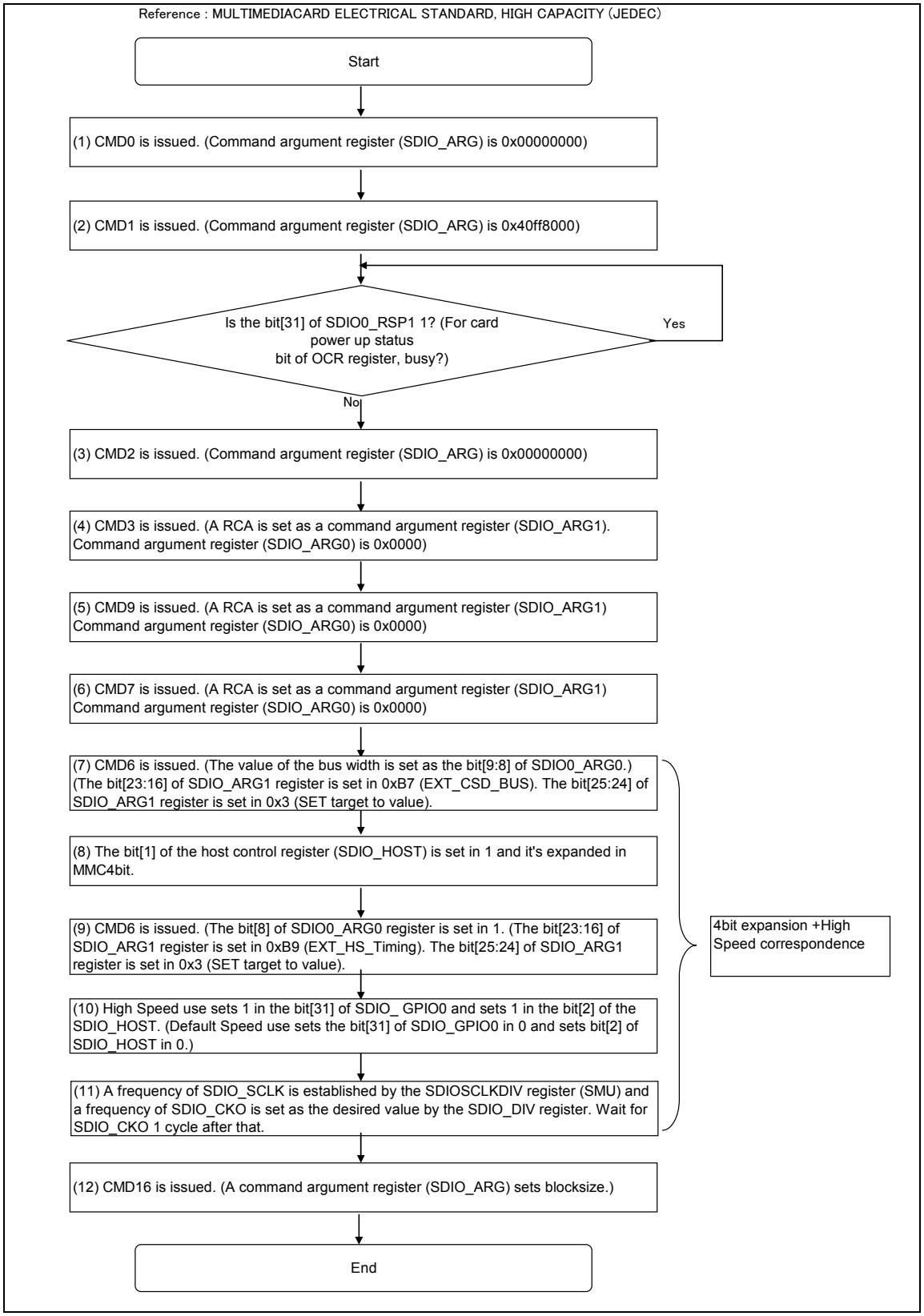
4.2 Command issue flow

Figure 4-2. Command issue flow



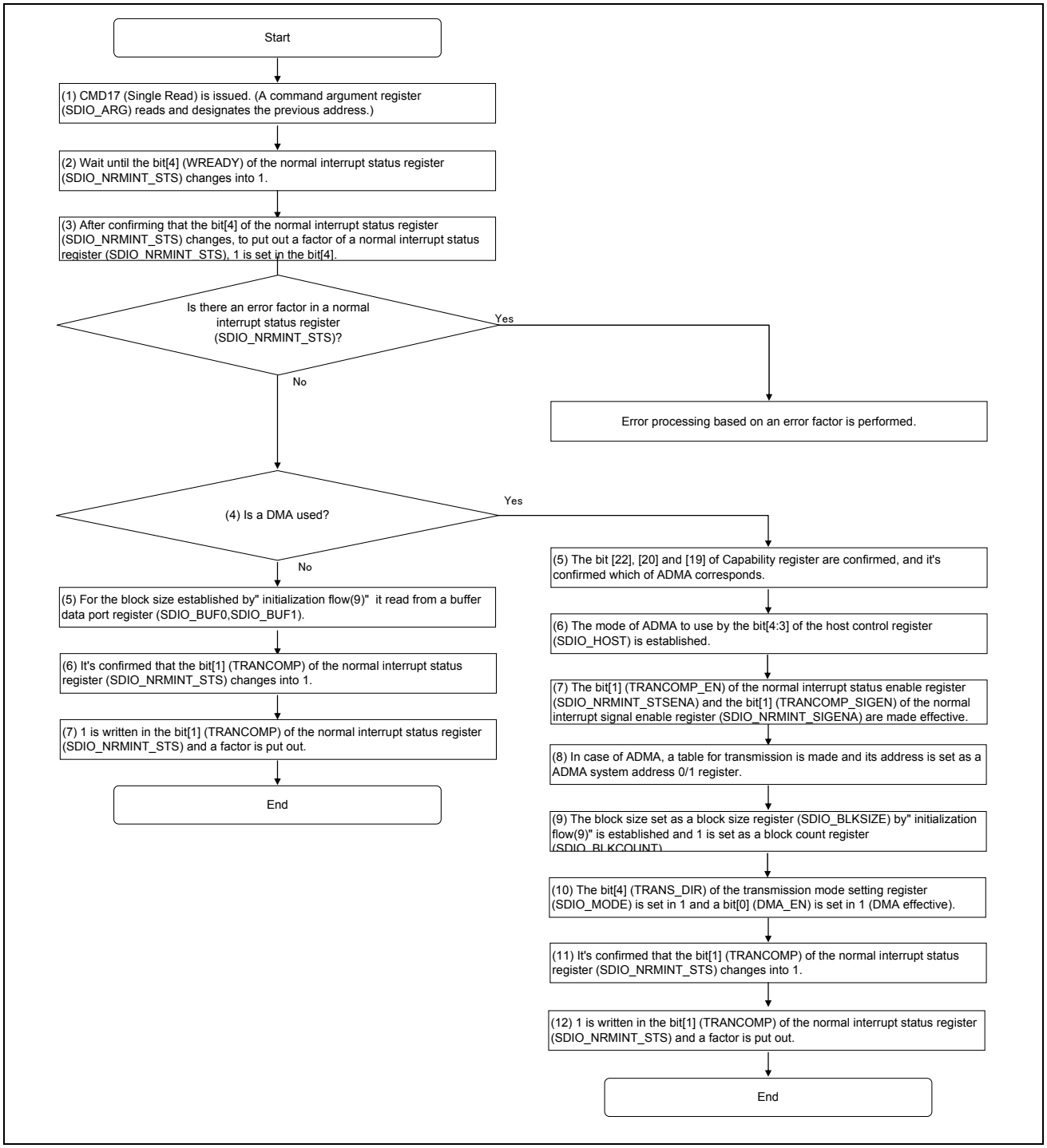
4.3 MMC initialization flow (reference)

Figure 4-3. MMC initialization flow (reference)



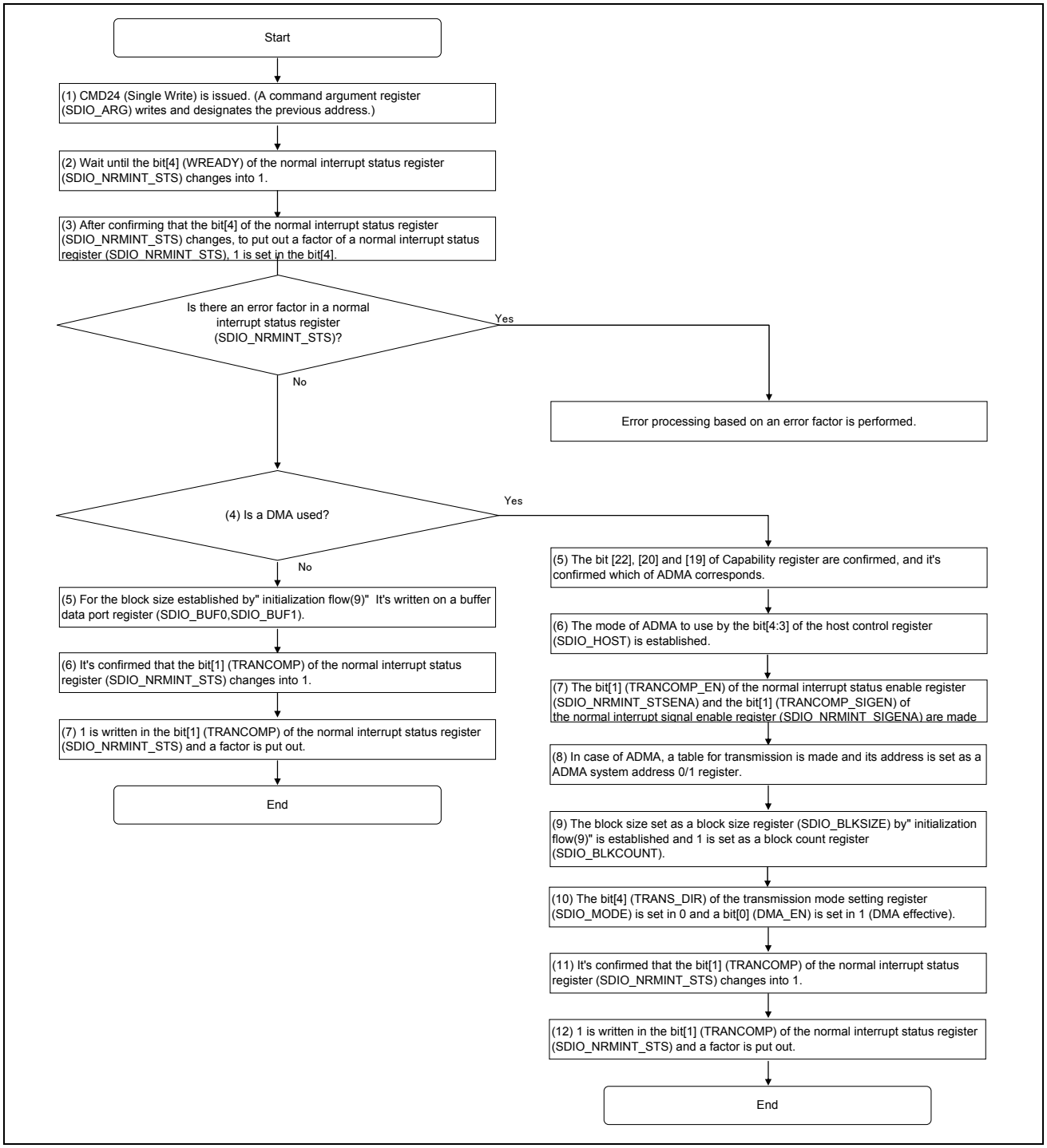
4.4 MMC single read flow (reference)

Figure 4-4. MMC single read flow (reference)



4.5 MMC single write flow (reference)

Figure 4-5. MMC single write flow (reference)



4.6 The DETECT processing performed after return to the Power-On state from The Retention state

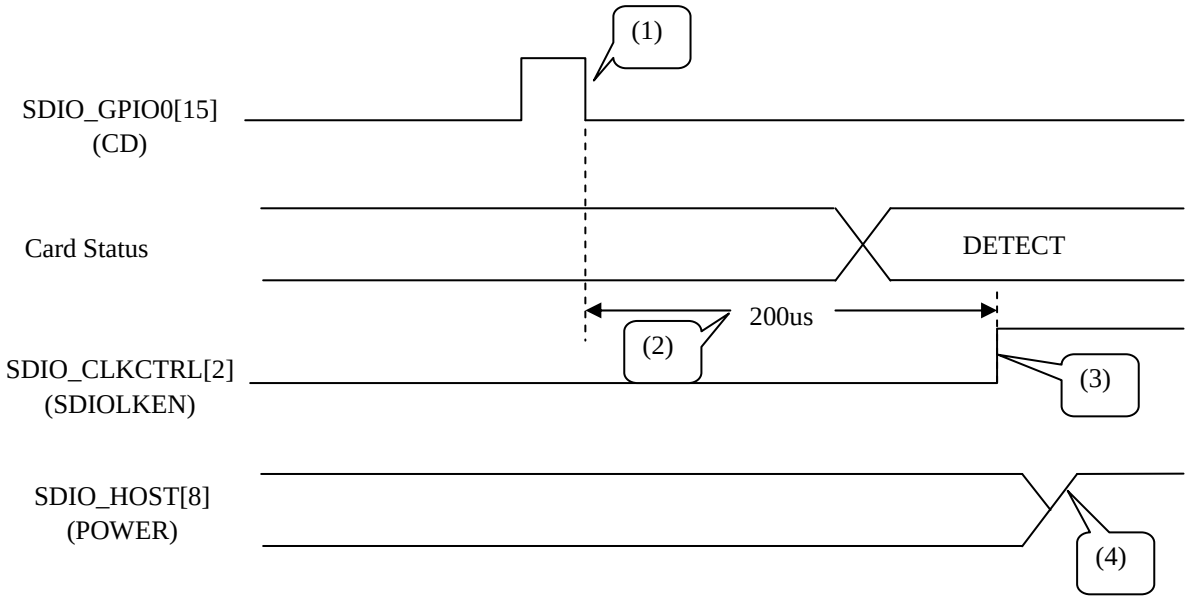
DETECT processing is needed to make them return to the Power-On state from the Retention state.

(1) SDIO_GPIO0 register (E004H) CD bit (bit[15]) : 1→0

(2) After processing of the above “(1)” , and about 200us wait. (SDIO_SCLK, more than for 64 cycles)

(3) SDIO_CLKCTRL register (002CH) SDIOLKEN bit (bit[2]) : 1

(4) SDIO_HOST register (0028H) POWER bit (bit[8]) : 1



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		Page	Summary
1.00	Mar 31, 2010	—	1st revision release
2.00	Jun 7, 2010	—	Incremental update from comments to the 1.0.
3.00	Jun 30, 2010	—	Incremental update from comments to the 2.0. (A change part from the old revision is "★" marked in the page left end.)
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6.00	May 31, 2011	—	Incremental update from comments to the 5.0.
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		19	Chapter 3.2.13 corrected. (bit[7] and [6] Reserved.)
		20	Chapter 3.2.14 corrected. (bit[7] and [6] Reserved.)
		30	Chapter 3.2.24 corrected.
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		13	Chapter 3.2.10 corrected. (bit[8])
		41	Chapter 4.6 added.

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EMMA Mobile EV2

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