User's Manual

LP-DDR/DDR2 Controller

User's Manual

Multimedia Processor for Mobile Applications EMMA Mobile ™ EV2

Renesas Electronics
www.renesas.com

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the EMMA Mobile EV2. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Data Sheet	Hardware overview and electrical characteristics	EMMA Mobile EV2 Datasheet	R19DS0010EJxxxx
User's manual (1chip)	Hardware whole specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description	EMMA Mobile EV2 User's manual 1chip	R19UH0036EJxxxx
User's manual (module)	Hardware each macro specifications and operation description.	EMMA Mobile EV2 User's manual each module	See below

Document Name	Document No.	Document Name	Document No.
1chip	R19UH0036EJxxxx	DMA Controller	R19UH0043EJxxxx
System Management Unit	R19UH0037EJxxxx	LP-DDR/DDR2 Controller (This manual)	R19UH0039EJxxxx
Timer	R19UH0054EJxxxx	SD Memory Card Interface	R19UH0061EJxxxx
System Timer	R19UH0055EJxxxx	SDIO Interface	R19UH0042EJxxxx
HD Video Decoder	R19UH0056EJxxxx	CF Card Interface	R19UH0062EJxxxx
Rotator	R19UH0057EJxxxx	Unified Serial Interface	R19UH0047EJxxxx
Resizer	R19UH0058EJxxxx	UART interface	R19UH0040EJxxxx
Image Composer	R19UH0038EJxxxx	USB 2.0 Host Controller	R19UH0045EJxxxx
LCD Interface	R19UH0044EJxxxx	USB 2.0 Function Controller	R19UH0034EJxxxx
ITU-R BT.656 Interface	R19UH0059EJxxxx	IIC Interface	R19UH0052EJxxxx
Digital Terrestrial TV Interface	R19UH0048EJxxxx	General Purpose I/O Interface	R19UH0041EJxxxx
Camera Interface	R19UH0060EJxxxx	Pulse Width Modulation Interface	R19UH0063EJxxxx

4 digits of end shows the version.

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names

Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.

Examples the PM03 bit in the PM0 register

P3_5 pin, VCC pin

(2) Notation of Numbers

The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.

Examples Binary: 11b or 11

Hexadecimal: EFA0h

Decimal: 1234

3. Register Notation

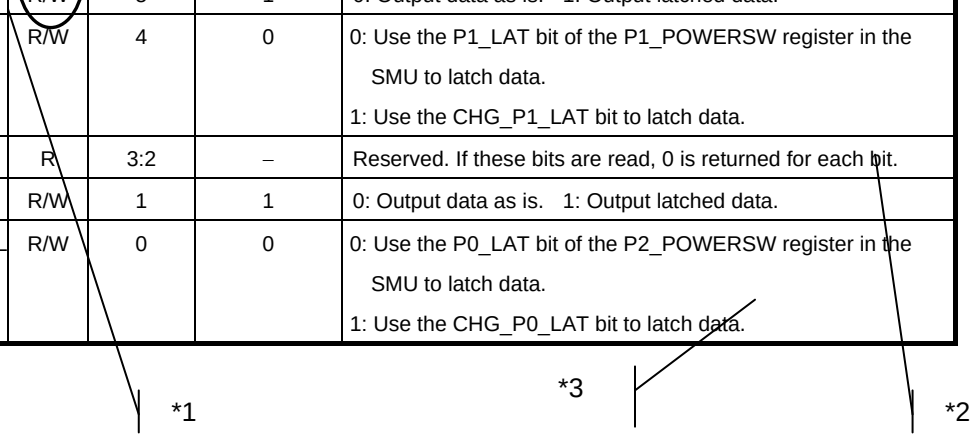
The symbols and terms used in register diagrams are described below.

x.x.x XXX register

This register (XXXXXXX: xxxx_xxxxh) …..

7	6	5	4	3	2	1	0
Reserved		CHG_P1_LAT	LATCH_P1_SEL	Reserved		CHG_P0_LAT	CHG_P0_LAT_SEL

Name	R/W	Bit No.	After Reset	Description
LATCH_P2_SEL	R/W	8	0	0: Use the P2_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P2_LAT bit to latch data.
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P1_LAT	R/W	5	1	0: Output data as is. 1: Output latched data.
LATCH_P1_SEL	R/W	4	0	0: Use the P1_LAT bit of the P1_POWERSW register in the SMU to latch data. 1: Use the CHG_P1_LAT bit to latch data.
Reserved	R	3:2	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P0_LAT	R/W	1	1	0: Output data as is. 1: Output latched data.
CHG_P0_LAT_SEL	R/W	0	0	0: Use the P0_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P0_LAT bit to latch data.



*1

R/W: Read and Write.

R: Read only.

W: Write only.

-: Nothing is assigned.

*2

Reserved bit.

Reserved bit. Set to specified value.

*3

・ Nothing is assigned.

Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.

・ Do not set to a value.

Operation is not guaranteed when a value is set.

・ Function varies according to the operating mode.

The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Register
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

Abbreviation	Full Form
AHB	Advanced High-performance Bus
BL	Burst Length
CAS	Column Address Strobe
CBR	CAS Before RAS
CKE	ClocK Enable
CL	CAS Latency
DDR SDRAM	Double-Data-Rate Synchronous Dynamic Random Access Memory
EMRS	Extended Mode Registers Set
IMC	Image Composer
MRS	Mode Register Set
RAS	Row Address Strobe
SMU	System Management Unit

Table of Contents

LP-DDR/DDR2 Controller

EMMA Mobile EV2

R19UH0039EJ0800
Rev.8.00
Dec 21, 2011

1. Overview

The LP-DDR/DDR2 SDRAM controller (MEMC) controls access to LPDDR/DDR2 SDRAM.

1.1. Features

- External memory access control
  The MEMC has a timing controller for the external memory interface. The usable memory is LPDDR-400/DDR2-533 SDRAM. The maximum operating frequency is 200 MHz (LPDDR-400), 266 MHz (DDR2-533). The MEMC can generate refresh requests to execute refreshes required for DDR SDRAM.

- Supported SDRAM
  - LPDDR SDRAM, DDR2 SDRAM
  - 32-bit data bus connection (one chip that has a 32-bit bus, or two chips that have 16-bit buses connected in parallel)
  - Operating frequency: 200/266 MHz (LP-DDR-400/DDR2-533)
  - Chip select 2 support. (CS0, CS1)
  - CKE 2 support. (CKE0, CKE1)
- Main functions
  - Flexible address mapping
  - Entering and exiting auto self refresh mode
  - Command control via software
  - 4KB read cache
  - BL=8 fixing

2. Pin Functions

Pin Name	I/O	Function	Alternate Pin
DDR_CK	Output	Clock output	–
DDR_CKB	Output	Inverted clock output	–
DDR_CS[1:0]B	Output	Chip select (low active)	–
DDR_CKE[1:0]	Output	Inverted clock enable	–
DDR_CKERSTB	Input	Clock enable reset (low active)	–
DDR_ODT	Output	On-die termination	–
DDR_RASB	Output	Row address strobe (low active)	–
DDR_CASB	Output	Column address strobe (low active)	–
DDR_WEB	Output	Write enable (low active)	–
DDR_BA[2:0]	Output	Bank address	–
DDR_A[14:0]	Output	Address	–
DDR_DM[3:0]	Output	Data mask	–
DDR_DQS[3:0]	I/O	Data strobe	–
DDR_DQS[3:0]B	I/O	Data strobe (low active)	–
DDR_DQ[31:0]	I/O	Data	–

Note : The on die termination function for DDR-ODT is not available.

3. Registers

3.1 Register List

The MEMC registers allow word access only.

Do not access reserved registers. An undefined value is returned for a read access.

Do not write any value other than 0 to reserved bits in each register.

3.1.1 Request control registers and system cache setting registers

Base address: E00A_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Cache disable/prefetch per master register	MEMC_CACHE_MODE	R/W	0000_0000H
0004H	Reserved	–	–	–
0008H	Degrade function register	MEMC_DEGFUN	R/W	0000_0000H
000CH to 0FFCH	Reserved	–	–	–

3.1.2 Memory request scheduler setting registers

Base address: E00A_0000H

Address	Register Name	Register Symbol	R/W	After Reset
1000H	Memory request scheduling mode register	MEMC_REQSCH	R/W	0000_0000H
1004H to 1FFCH	Reserved	–	–	–

3.1.3 External memory control registers

Base address: E00A_0000H (1/2)

Address	Register Name	Register Symbol	R/W	After Reset
2000H	Memory connection setting register	MEMC_DDR_CONFIGF	R/W	0000_0808H
2004H	AC timing setting register 1	MEMC_DDR_CONFIGA1	R/W	5444_3203H
2008H	AC timing setting register 2	MEMC_DDR_CONFIGA2	R/W	00DA_0040H
200CH	Software command issuance register 1	MEMC_DDR_CONFIGC1	R/W	4040_0033H
2010H	Software command issuance register 2	MEMC_DDR_CONFIGC2	R/W	0000_0340H
2014H	Refresh setting register 1	MEMC_DDR_CONFIGR1	R/W	0FFF_0FFFH
2018H	Refresh setting register 2	MEMC_DDR_CONFIGR2	R/W	1F1F_FCFCH
201CH	Refresh setting register 3	MEMC_DDR_CONFIGR3	R/W	0000_FCFCH
2020H	DQS output timing adjustment register 1	MEMC_DDR_CONFIGT1	R/W	0000_0003H
2024H	DQS input timing adjustment register 2	MEMC_DDR_CONFIGT2	R/W	0000_0000H
2028H	Reserved	–	–	–
202CH	Memory status check register	MEMC_DDR_STATE8	R/W	0000_0000H

(2/2)

Address	Register Name	Register Symbol	R/W	After Reset
2030H	IO configuration register	MEMC_DDR_CONFIGD	R/W	0000_8000H
2034H	Reserved	–	–	–
2038H	Drive capability switch register 1	MEMC_DDR_CONFIGZD	R/W	0000_0000H
203CH	Drive capability switch register 2	MEMC_DDR_CONFIGZC	R/W	0000_0000H
2040H	Drive capability switch register 3	MEMC_DDR_CONFIGZA	R/W	0000_0000H
2044H to FFFCH	Reserved	–	–	–

3.2 Register Details

3.2.1 Cache/prefetch setting register

This register (MEMC_CACHE_MODE: E00A_0000H) specifies whether to cache and prefetch data for each master device. Setting is usually unnecessary.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
PRE_A3D	PRE_IMCW	PRE_IMC	PRE_DMA	Reserved	PRE_AHB	PRE_AVE	PRE_CPU

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
DIS_A3D	DIS_IMCW	DIS_IMC	DIS_DMA	Reserved	DIS_AHB	DIS_AHB	DIS_CPU

(1/2)

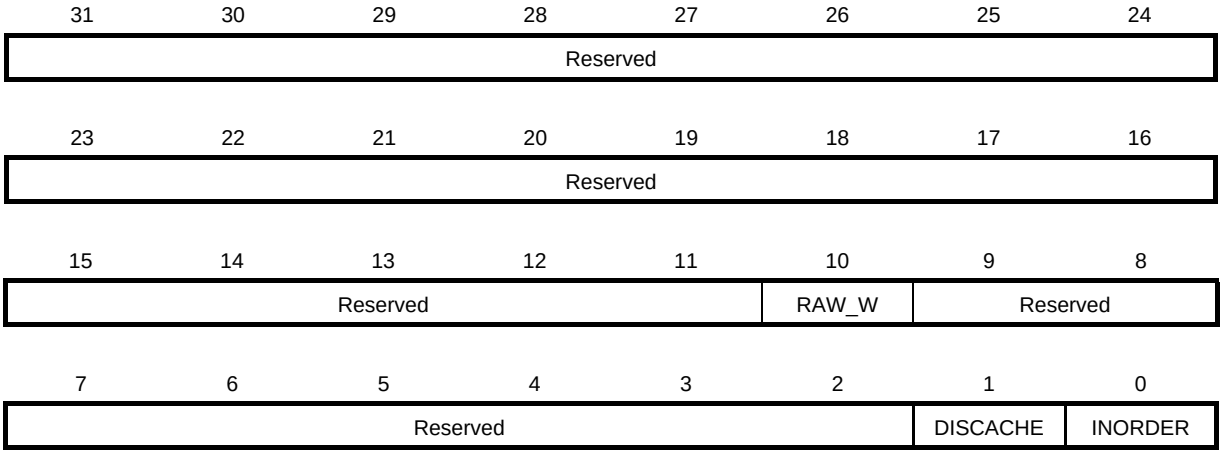
Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:24	00H	Reserved. When these bits are read, 0 is returned for each bit.
PRE_A3D	R/W	23	0	0: Does not prefetch data while reading data from the A3D. 1: Prefetches data while reading data from the A3D.
PRE_IMCW	R/W	22	0	0: Does not prefetch data while reading data from the IMCW. 1: Prefetches data while reading data from the IMCW.
PRE_IMC	R/W	21	0	0: Does not prefetch data while reading data from the IMC. 1: Prefetches data while reading data from the IMC.
PRE_DMA	R/W	20	0	0: Does not prefetch data while reading data from the DMA. 1: Prefetches data while reading data from the DMA.
Reserved	R	19	0	Reserved. When this bit is read, 0 is returned.
PRE_AHB	R/W	18	0	0: Does not prefetch data while reading data from the AHB. 1: Prefetches data while reading data from the AHB.
PRE_AVE	R/W	17	0	0: Does not prefetch data while reading data from the AVE. 1: Prefetches data while reading data from the AVE.
PRE_CPU	R/W	16	0	0: Does not prefetch data while reading data from the CPU. 1: Prefetches data while reading data from the CPU.
Reserved	R	15:8	00H	Reserved. When these bits are read, 0 is returned for each bit.
DIS_A3D	R/W	7	0	0: Cashes data read from the A3D 1: Does not cache data
DIS_IMCW	R/W	6	0	0: Cashes data read from the IMCW 1: Does not cache data
DIS_IMC	R/W	5	0	0: Cashes data read from the IMC 1: Does not cache data

(2/2)

Name	R/W	Bit No.	After Reset	Function
DIS_DMA	R/W	4	0	0: Cashes data read from the DMA 1: Does not cache data
Reserved	R	3	0	Reserved. When this bit is read, 0 is returned.
DIS_AHB	R/W	2	0	0: Cashes data read from the AHB 1: Does not cache data
DIS_AVE	R/W	1	0	0: Cashes data read from the AVE 1: Does not cache data
DIS_CPU	R/W	0	0	0: Cashes data read from the CPU 1: Does not cache data

3.2.2 Function disabling register

This register (MEMC_DEGFUN: E00A_0008H) disables some of the MEMC functions.
Setting is usually unnecessary.



Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:11	00_0000H	Reserved. When these bits are read, 0 is returned for each bit.
RAW_W	R/W	10	0	LCD underrun avoidance function Be sure to set 1.
Reserved	R	9:2	00H	Reserved. When these bits are read, 0 is returned for each bit.
DISCACHE	R/W	1	0	Cash setting for AXI in MEMC. 0: Enables use of the system cache. 1: Disables use of the system cache.
INORDER	R/W	0	0	0: Issues read requests out-of-order. 1: Issues read requests in order.

3.2.3 Memory request scheduling mode register

This register (MEMC_REQSCH: E00A_1000H) specifies the schedule of requests for memory. Setting is usually unnecessary.

31	30	29	28	27	26	25	24
HI_A3D	HI_IMCW	HI_IMC	HI_DMA	Reserved	HI_AHB	HI_AVE	HI_CPU

23	22	21	20	19	18	17	16
RAW_A3D	RAW_IMCW	RAW_IMC	RAW_DMA	Reserved	RAW_AHB	RAW_AVE	RAW_CPU

15	14	13	12	11	10	9	8
Reserved					DPLPRI	MXCSWN	

7	6	5	4	3	2	1	0
MXCASWN		MXWTWN		MXRDWN		WTDNUM	

(1/3)

Name	R/W	Bit No.	After Reset	Function
HI_A3D	R/W	31	0	0: The usual reading order. 1: The reading from A3D is taken high priority.
HI_IMCW	R/W	30	0	0: The usual reading order. 1: The reading from IMCW is taken high priority.
HI_IMC	R/W	29	0	0: The usual reading order. 1: The reading from IMC is taken high priority.
HI_DMA	R/W	28	0	0: The usual reading order. 1: The reading from DMA is taken high priority.
Reserved	R	27	0	Reserved. When this bit is read, 0 is returned.
HI_AHB	R/W	26	0	0: The usual reading order. 1: The reading from AHB is taken high priority.
HI_AVE	R/W	25	0	0: The usual reading order. 1: The reading from AVE is taken high priority.
HI_CPU	R/W	24	0	0: The usual reading order. 1: The reading from CPU is taken high priority.
RAW_A3D	R/W	23	0	0: Normal operation 1: Read command priority. (RAW (Read After Write) is ignored and the Read command is issued.)
RAW_IMCW	R/W	22	0	0: Normal operation 1: Read command priority. (RAW (Read After Write) is ignored and the Read command is issued.)

(2/3)

Name	R/W	Bit No.	After Reset	Function
RAW_IMC	R/W	21	0	0: Normal operation 1: Read command priority. (RAW (Read After Write) is ignored and the Read command is issued.)
RAW_DMA	R/W	20	0	0: Normal operation 1: Read command priority. (RAW (Read After Write) is ignored and the Read command is issued.)
Reserved	R	19	0	Reserved. When this bit is read, 0 is returned.
RAW_AHB	R/W	18	0	0: Normal operation 1: Read command priority. (RAW (Read After Write) is ignored and the Read command is issued.)
RAW_AVE	R/W	17	0	0: Normal operation 1: Read command priority. (RAW (Read After Write) is ignored and the Read command is issued.)
RAW_CPU	R/W	16	0	0: Normal operation 1: Read command priority. (RAW (Read After Write) is ignored and the Read command is issued.)
Reserved	R	15:11	00H	Reserved. When these bits are read, 0 is returned for each bit.

Name	R/W	Bit No.	Act	After Reset	Function
DPLPRI	R/W	10	–	0	0: Direct path request is made the high priority. 1: Direct path request isn't made the high priority.
MXCSWN	R/W	9:8	–	00b	Specifies the maximum number of times the same CS can be selected in a row. 00b: No specification 01b: 2 times 10b: 4 times 11b: 6 times
MXCASWN	R/W	7:6	–	00b	Specifies the maximum number of times a CAS request can be selected in a row. 00b: Once (Performs execution immediately after receiving a CAS request) 01b: 2 times 10b: 4 times 11b: 6 times
MXWTWN	R/W	5:4	–	00b	Specifies the maximum number of times a write request can be selected in a row for a read request during a write drain. 00b: No specification 01b: 2 times 10b: 4 times 11b: 6 times

(3/3)

Name	R/W	Bit No.	Act	After Reset	Function
MXRDWN	R/W	3:2	–	00b	Specifies the maximum number of times a read request can be selected in a row for a write request during a write drain. 00b: No specification 01b: 2 times 10b: 4 times 11b: 6 times
MTDNUM	R/W	1:0	–	00b	Specifies the number of requests for starting a write drain. 00b: 2 01b: 4 10b: 6 11b: 8

3.2.4 Memory connection setting register

This register (MEMC_DDR_CONFIGF: E00A_2000H) specifies the configuration for the external memory.

31	30	29	28	27	26	25	24
DDR2	16BIT	Reserved	tFAW				

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
CS1_BANK_SPLIT		Reserved	CS1_DENSITY				

7	6	5	4	3	2	1	0
CS0_BANK_SPLIT		Reserved	CS0_DENSITY				

Name	R/W	Bit No.	After Reset	Function
DDR2	R/W	31	0	Use DDR2 0: LPDDR 1: DDR2.
16BIT	R/W	30	0	0: 32bit (16bit × 2) 1: Use 16bit × 1 (disable DQ[31:16])
tFAW	R/W	28:24	00H	tFAW (cycle)
Reserved	R	23:16	00H	Reserved. When these bits are read, 0 is returned for each bit.
CS1_BANK_SPLIT	R/W	15:14	00b	Specifies the number of banks for interleaving for CS1 (see **Figure 3-1, 3-2**) 00b: No interleave 01b: 2-bank interleave 10b: 4-bank interleave 11b: Lower two banks interleaved, higher two banks not interleaved
Reserved	R	13	0H	Reserved. When this bit is read, 0 is returned.
CS1_DENSITY	R/W	12:8	8b	CS1 address config (see **Figure 3-1**)
CS0_BANK_SPLIT	R/W	7:6	00b	Specifies the number of banks for interleaving for CS0 (see **Figure 3-1, 3-2**) 00b: No interleave 01b: 2-bank interleave 10b: 4-bank interleave 11b: Lower two banks interleaved, higher two banks not interleaved
Reserved	R	5	0	Reserved. When this bit is read, 0 is returned.
CS0_DENSITY	R/W	4:0	8b	CS0 address config (see **Figure 3-1**)

Bank addressing can be changed individually for CS0 and CS1. DDR SDRAM assigns bank addresses to column addresses consecutively and reads out up to 4 KB of data in succession. However, because memory is separated into banks, data cannot be read consecutively when using the partial refresh function (a function for retaining only specific data in memory) of LPDDR, and consecutiveness in memory areas that must be maintained is not assured. Specify settings by using this register to avoid this problem. Table 3-1 shows an example of address assignment and Figure 3-1 shows an overview of the mapping.

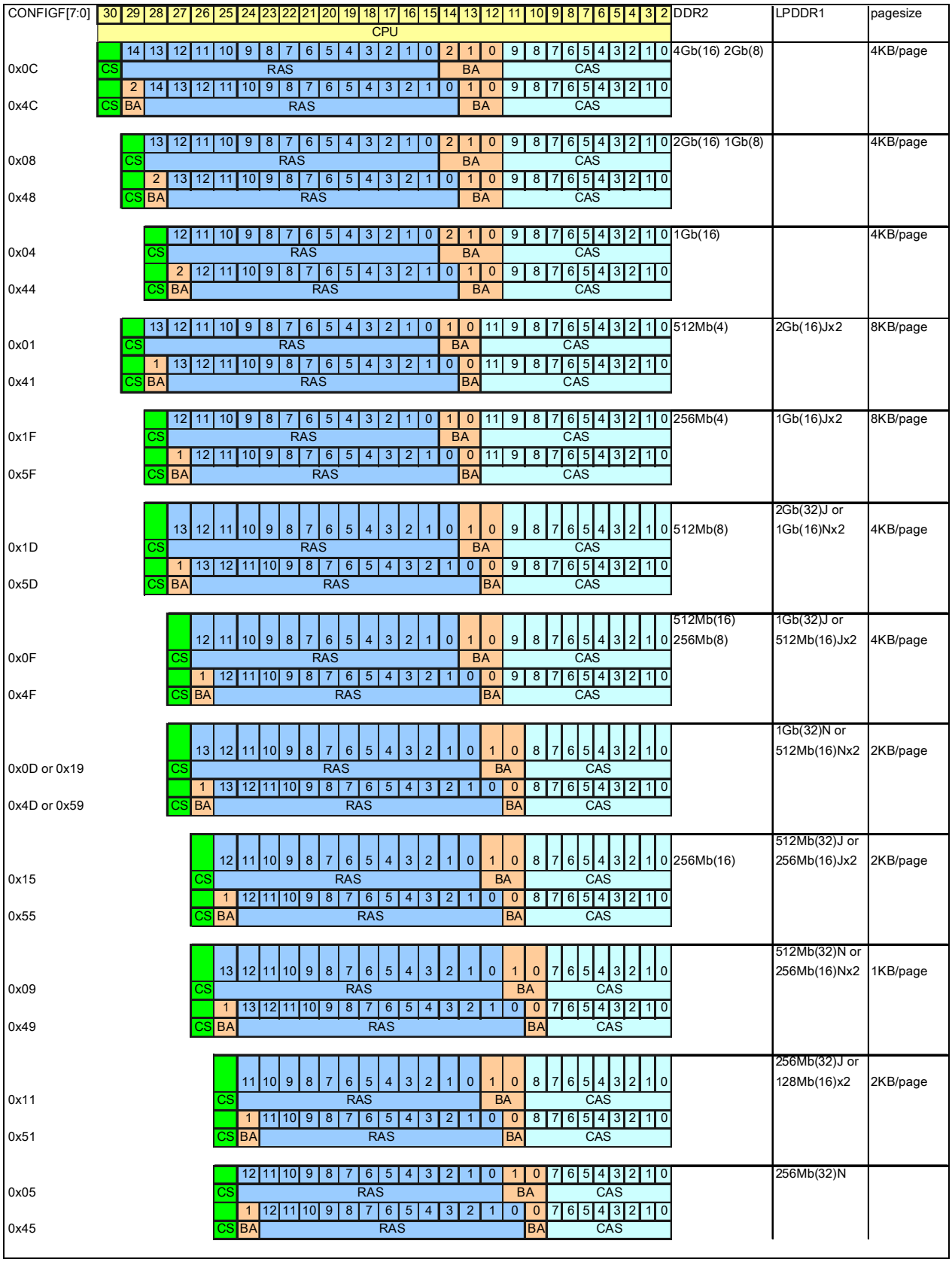


Figure 3-1. CPU address vs External Memory address

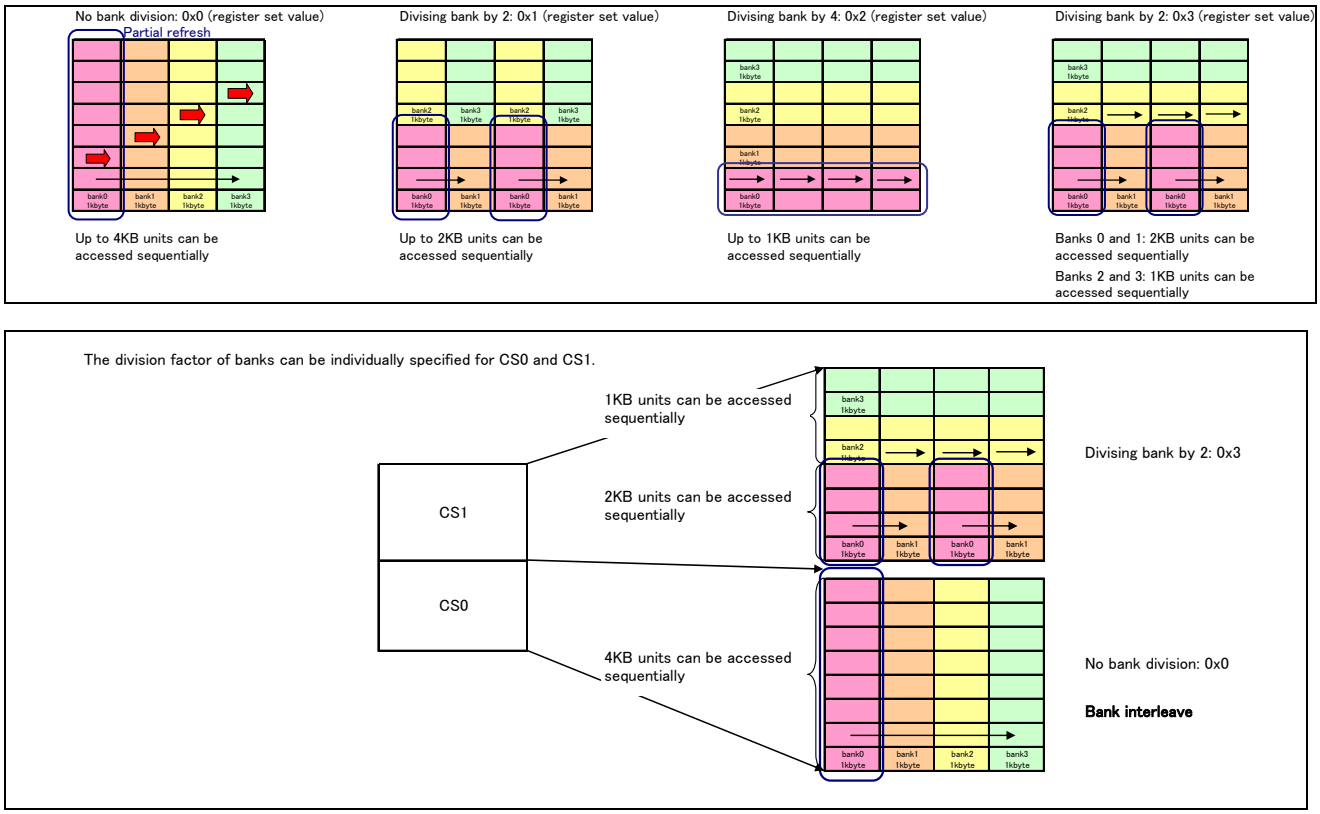


Figure 3-2. External Memory Address Mapping image

DDR SDRAM

Size	Word	Bus Width	Row	Column	BA
256 Mb	8 M	32	A[12:0]	A[7:0]	BA[1:0]
512 Mb	16 M	32	A[13:0]	A[7:0]	BA[1:0]
1 Gb	32 M	32	A[13:0]	A[8:0]	BA[1:0]

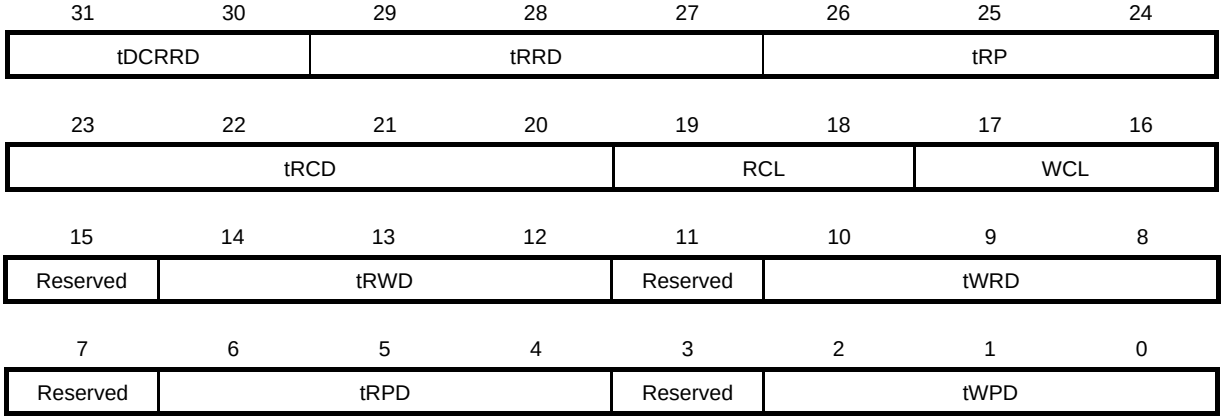
16-bit bus chip × 2

Size	Word	Bus Width	Row	Column	BA
128 Mb	8 M	32	A[11:0]	A[8:0]	BA[1:0]
256 Mb	16 M	32	A[12:0]	A[8:0]	BA[1:0]
512 Mb	32 M	32	A[13:0]	A[8:0]	BA[1:0]
1 Gb	64 M	32	A[13:0]	A[9:0]	BA[1:0]

Table 3-1. LPDDR SDRAM

3.2.5 AC timing setting register 1

This register (MEMC_DDR_CONFIGA1: E00A_2004H) determines the AC timing of external memory.



(1/2)

Name	R/W	Bit No.	Act	After Reset	Function
tDCRRD	R/W	31:30	–	01b	Specifies the number of cycles required from a read (write) command to a read (write) command between chips. Specifying 0 is prohibited.
tRRD	R/W	29:27	–	010b	Specifies the reference clock cycles between bank activating commands.
tRP	R/W	26:24	–	100b	Specifies the reference clock cycles from a precharge command to a bank activating command.
tRCD	R/W	23:20	–	0100b	Specifies the period from a bank activating command to a read command and a bank activating command to a write command. 0x3 at 166 MHz, 0x2 at 133 MHz, 0x1 at 100 MHz → RL = tRCD + RCL, W L = tRCD + WCL – 1[Note 2]
RCL	R/W	19:18	–	01b	Specifies the read CAS latency. 00b: CL = 2 01b: CL = 3 10b: CL = 4 11b: CL = 5
WCL	R/W	17:16	–	00b	Specifies the write CAS latency. 00b: CL = 1 01b: CL = 2 10b: CL = 3 11b: CL = 4
Reserved	R	15	–	0	Reserved. When this bit is read, 0 is returned.
tRWD	R/W	14:12	–	011b	Specifies the period from a read command to a write command. *tRWD* + *4* clock cycles
Reserved	R	11	–	0	Reserved. When this bit is read, 0 is returned.
tWRD	R/W	10:8	–	010b	Specifies the period from a write command to a read command. *tWRD* + *4* clock cycles

(2/2)

Name	R/W	Bit No.	Act	After Reset	Function
Reserved	R	7	–	0	Reserved. When this bit is read, 0 is returned.
tRPD	R/W	6:4	–	000b	Specifies the period from a read command to a precharge command. *tRPD + 4* clock cycles
Reserved	R	3	–	0	Reserved. When this bit is read, 0 is returned.
tWPD	R/W	2:0	–	011b	Specifies the period from a write command to a precharge command. *tWPD + 4* clock cycles

Note tRCDR = tRCDW + 1, RL = tRCDW + RCL, WL = tRCDW + WCL – 1
Because the same AC parameters are applied to CS0 and CS1, devices whose AC timing specifications differ cannot be connected to CS0 and CS1 at the same time.

3.2.6 AC timing setting register 2

This register (MEMC_DDR_CONFIGA2: E00A_2008H) specifies the AC timing parameters for external memory and is used to expand some functions.

31	30	29	28	27	26	25	24
DDR2/LPDDR	Reserved			CS1H	CS0H	ADD_HZ	CMD_HZ

23	22	21	20	19	18	17	16
tSREX				tRFC			

15	14	13	12	11	10	9	8
tRAS			LowFrqTyp	DQS_mask_Ext	DQS_mask		DQM_HZ

7	6	5	4	3	2	1	0
IO_HZ	AutoPre	CLK_MODE		PstamblExt	PreamblExt	DBParkEna	Reserved

(1/2)

Name	R/W	Bit No.	Act	After Reset	Function
DDR2/LPDDR	R/W	31	–	0	DDR2/LPDDR selected 0: LPDDR 1: DDR2
Reserved	R	30:28	–	0H	Reserved. When these bits are read, 0 is returned for each bit.
CS1H	R/W	27	1	0	Forcibly sets CS1 to high level. 0: Active 1: High level
CS0H	R/W	26	1	0	Forcibly sets CS0 to high level. 0: Active 1: High level
ADD_HZ	R/W	25	1	0	Specifies the state of the I/O buffer for address signals. 0: Active 1: Hi-Z
CMD_HZ	R/W	24	1	0	Specifies the state of the I/O buffer for command signals. 0: Active 1: Hi-Z
tSREX	R/W	23:20	–	DH	Specifies the period until returning from a self refresh. [*(tSREX + 8) – 1)*] clock cycles
tRFC	R/W	19:16	–	AH	Specifies the period until returning from an auto refresh. *tRFC + 8* clock cycles
tRAS	R/W	15:13	0	0H	tRAS *tRAS + 7* clock cycles
LowFrqTyp	R/W	12	0	0	Switches the frequency range in the low-frequency mode. 0: 30 MHz or less 1: 30 MHz to 60 MHz

(2/2)

Name	R/W	Bit No.	Act	After Reset	Function
DQS_mask_Ext	R/W	11	–	0	Specifies whether to delay the input DQS mask timing by 0.5 clock cycles. 0: Does not delay the timing. 1: Delays the period.
DQS_mask	R/W	10:9	–	00b	Specifies how much the input DQS mask timing is delayed. 00b: 2 clock cycles 01b: 2.5 clock cycles 10b: 3 clock cycles, 11b: Reserved
DQM_HZ	R/W	8	1	0	Specifies the state of the DQM signal for the I/O buffer. 0: Active 1: Hi-Z
IO_HZ	R/W	7	1	0	Specifies the state of the signal for the I/O buffer. 0: Active 1: Hi-Z
AutoPre	R/W	6	1	1	Specifies whether to enable auto precharge. 0: Does not enable auto precharge 1: Enables auto precharge
CLK_MODE	R/W	5:4	–	00b	Specifies the timing at which read data is received. 00b: 2-clock cycle mode 01b: 3-clock cycle mode, 10b: 1-clock cycle mode 11b: Reserved
PstamblExt	R/W	3	1	0	Specifies whether to extend the period for which the DQS postamble is output during a write by 0.5 clock cycles. 0: Does not extend the period 1: Extend the period
PreamblExt	R/W	2	1	0	Specifies whether to extend the period for which the DQS preamble is output during a write by 0.5 clock cycles. 0: Does not extend the period 1: Extend the period
DBParkEna	R/W	1	1	0	Specifies whether to drive DQ or DQS to low level while DDR SDRAM is in the Hi-Z state. 0: Hi-Z control 1: Drive to low level for periods other than the period when data is valid.
Reserved	R	0	–	0	Reserved. When this bit is read, 0 is returned.

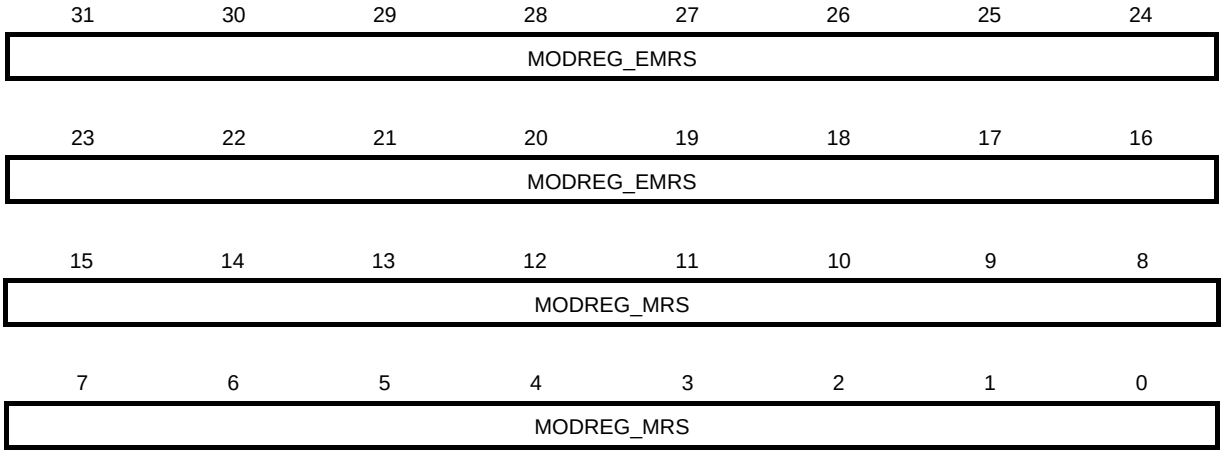
Note tRCDR = tRCDW + 1, RL = tRCDW + RCL, WL = tRCDW + WCL – 1

Remark Because the same AC parameters are applied to CS0 and CS1, devices whose AC timing specifications differ cannot be connected to CS0 and CS1 at the same time.

There is also a bit of the identical name in CONFIGR3 register, but when the price besides 0 is set as tSREX and tRFC of CONFIGR3 register, tSREX and tRFC aren't used for the set value to tSREX and tRFC of this register, and tSREX and tRFC of CONFIGR3 register become effective.

3.2.7 Software command issuance register 1

This register (MEMC_DDR_CONFIGC1: E00A_200CH) specifies addresses and data when the extended mode register is set up for external memory.



Name	R/W	Bit No.	Act	After Reset	Function
MODREG_EMRS	R/W	31:16	–	4040H	Data for mode register issue. Data of [31:16] is output by BA1,BA0 and A[13:0].
MODREG_MRS	R/W	15:0	–	0033H	Data for mode register issue. Data of [15:0] is output by BA1,BA0 and A[13:0].

When it's set as MEMC_DDR_CONFIGC2 [3:0]= F and the command is issued, the data set as bit [31:16] MODEREG_EMRS of this register is output in the address to the memory (BA1 BA0 A [13:0]).
Establish this register as follows at the time of each command put out of MRS/EMRS.

MRS command issue
MODREG_EMRS = {2'b00, MRS setting}
MODREG_MRS = {2'b00, don't care}

EMRS command issue
MODREG_EMRS = {2'b01, EMRS setting}
(Change the part of 2'b01 according to the specification of EMRS of a used memory.)
MODREG_MRS = {2'b00, don't care}

When it's set as MEMC_DDR_CONFIGC2 [3:0]= 9/A/B and the command is issued, the data set as bit [15:0] MODEREG_MRS of this register is output in the address to the memory (BA1 BA0 A [13:0]).
Establish this register as follows at the time of each command put out of MRS/EMRS.

When issuing precharge commands, set up this register as follows:

All bank precharge	MODREG_MRS[10] = 1'b1	Other bits are don't care.
Bank precharge	MODREG_MRS[15:14] = Target bank address, MODREG_MRS[10] = 1'b0	Other bits are don't care.
Auto refresh	MODREG_MRS[15:0] = don't care	

Self refresh MODREG_MRS[15:0] = don’t care

Restriction and caution on command issuance:

- Requests to issue commands are ignored when the CMD_STATE bit of the MEMC_DDR_CONFIGC2 register is set to 0 (busy).

The register set value and correspondence of a terminal

At the time of MEMC_DDR_CONFIGC2 [3:0] =F setting.
Upper : MEMC_DDR_CONFIGC1 register [31:16] Bit.
Lower : DRAM Terminals

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

At the time of MEMC_DDR_CONFIGC2 [3:0] =9/A/B setting.
Upper : MEMC_DDR_CONFIGC1 register [15:0] Bit.
Lower : DRAM Terminals

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

CMD_SET and DRAM signal status

	MEMC_DDR_CONFIGC2 register bit[3:0] CMD_SET			
DRAM signals	**9 :pre charge**	**a :auto refresh**	**f :MRS**	**b :self refresh**
CKE	H	H	H	L
/CS	L	L	L	L
/RAS	L	L	L	L
/CAS	H	L	L	L
/WE	L	H	L	H
BA[1:0]	CONFIGC1 bit[15:14]	CONFIGC1 bit[15:14]	CONFIGC1 bit[31:30]	CONFIGC1 bit[15:14]
A[13:0]	CONFIGC1 bit[13:0]	CONFIGC1 bit[13:0]	CONFIGC1 bit[29:16]	CONFIGC1 bit[13:0]

3.2.8 Software command issuance register 2

This register (MEMC_DDR_CONFIGC2: E00A_2010H) specifies the settings for controlling command issuance for external memory.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved						CMD_STATE (CS1)	CMD_STATE (CS0)

7	6	5	4	3	2	1	0
CMD_REQ_ LOCK	CMD_ ENABLE	CS1_TARGET	CS0_TARGET	CMD_SET			

(1/2)

Name	R/W	Bit No.	Act	After Reset	Function
Reserved	R	31:10	–	00_0000H	Reserved. When these bits are read, 0 is returned for each bit.
CMD_STATE(CS1)	R	9	– Note1	1	Indicates the execution status of a command requested by CS. 0: Busy 1: Standby
CMD_STATE(CS0)	R	8	– Note1	1	Indicates the execution status of a command requested by CS. 0: Busy 1: Standby
CMD_REQ_LOCK	R/W	7	0	0	Specifies the signal to lock any request other than for command issuance. 0: Lock 1: Unlock
CMD_ENABLE	R/W	6	0 Note2	1	Specifies whether to issue a command request. 0: Requests command issuance. This bit is automatically set to 1 during the next clock cycle.
CS1_TARGET	R/W	5	1	0	Sets the command request flag for CS1. 0: Does not set the flag. 1: Sets the flag.
CS0_TARGET	R/W	4	1	0	Sets the command request flag for CS0. 0: Does not set the flag. 1: Sets the flag.

(2/2)

Name	R/W	Bit No.	Act	After Reset	Function
CMD_SET	R/W	3:0	–	0H	Specifies the control command. 0111: Disables the CKE signal. 1000: Reserved 1001: Precharges all banks. Precharge all Banks/Single Bank Precharge changes with setting it as MODEREG_MRS[10],[15:14]. 1010: Executes a CBR refresh. 1011: Shifts to the self refresh mode. 1100: Reserved 1101: Enables the CKE signal. 1110: Reserved 1111: Writes to the (extended) mode register.

Note1 Read only

Note2 When writing in 0, the register value returns to 1 automatically by the next clock.

The command specified by the CMD_SET bit can be issued if a command code is specified for the target memory at the same time as the CMD_ENABLE bit is set to 0 in this register.

The memory assigned to CS0 and CS1 can be specified as target memory at the same time.

Before setting the CMD_ENABLE bit, make sure that the CMD_STATE bit is set to 1.

No command requests are accepted if the CMD_STATE bit is set to 0 (busy) upon command issuance. After a command request is issued while the CMD_REQ_LOCK bit is set to 0 (locked), only requests for software commands are accepted.

When the deep power down mode is entered, cancel the auto self refresh and CBR refresh for the target CS.

3.2.9 Refresh setting register 1

This register (MEMC_DDR_CONFIGR1: E00A_2014H) individually specifies refresh cycles in external memory for CS0 and CS1.

31	30	29	28	27	26	25	24
CS1_REF_OVER	CS1_REF_STOCK			CS1_CBR_SREF	CS1_REF_COUNT		

23	22	21	20	19	18	17	16
CS1_REF_COUNT							

15	14	13	12	11	10	9	8
CS0_REF_OVER	CS0_REF_STOCK			CS0_CBR_SREF	CS0_REF_COUNT		

7	6	5	4	3	2	1	0
CS0_REF_COUNT							

Name	R/W	Bit No.	Act	After Reset	Function
CS1_REF_OVER	R	31	– Note	0	Indicates whether the number of times refreshes for CS1 still needs to be executed exceeds the maximum.
CS1_REF_STOCK	R	30:28	– Note	0H	Indicates the number of times refreshes for CS1 still needs to be executed.
CS1_CBR_SREF	R/W	27	1	1	Specifies whether to forcibly execute a CBR refresh at least once when CS1 is in the self refresh mode.
CS1_REF_COUNT	R/W	26:16	–	FFFH	Specifies the CS1 refresh timer counter value. Default frequency is 38.229MHz. It's possible to change the frequency in REFCLKDIV (E011_068CH) in SMU.
CS0_REF_OVER	R	15	– Note	0	Indicates whether the number of times refreshes for CS0 still needs to be executed exceeds the maximum.
CS0_REF_STOCK	R	14:12	– Note	0H	Indicates the number of times refreshes for CS0 still needs to be executed
CS0_CBR_SREF	R/W	11	1	1	Specifies whether to forcibly execute a CBR refresh at least once when CS0 is in the self refresh mode.
CS0_REF_COUNT	R/W	10:0	–	FFFH	Specifies the CS0 refresh timer count value. Default frequency is 38.229MHz. It's possible to change the frequency in MEMCRCLKDIV (E011_062CH) in SMU.

Note Read only

The refresh counter is incremented during each refresh cycle by the REF_STOCK counter. A refresh is executed when the self refresh mode is entered or when the refresh counter reaches the threshold.

3.2.10 Refresh setting register 2

This register (MEMC_DDR_CONFIGR2: E00A_2018H) specifies the settings for a refresh in external memory.

31	30	29	28	27	26	25	24
Reserved	STOCK_ DRAIN_TYP	CS1_STOCK_DRAIN		CS1_STOCK_MAX			CS1_TIMER _RST

23	22	21	20	19	18	17	16
Reserved	COUNT_ COMMON	CS0_STOCK_DRAIN		CS0_STOCK_MAX			CS0_TIMER _RST

15	14	13	12	11	10	9	8
CS1_SREF_COUNT						CS1_SREF_ AUTO	CS1_REF_ AUTO

7	6	5	4	3	2	1	0
CS0_SREF_COUNT						CS0_SREF_ AUTO	CS0_REF_ AUTO

(1/2)

Name	R/W	Bit No.	Act	After Reset	Function
Reserved	R	31	–	0	Reserved. When this bit is read, 0 is returned.
STOCK_DRAIN_TYP	R/W	30	–	0	Specifies whether to decrement the refresh counter (whether to execute CBR) when no read request is being received and the number of write requests is the write buffer drain threshold value or lower.
CS1_STOCK_DRAIN	R/W	29:28	–	01b	Specifies how many times a refresh is executed before CS1 enters the self refresh mode. Specifiable range: 1 to 3 (Specifying 0 is prohibited.)
CS1_STOCK_MAX	R/W	27:25	–	7H	Specifies the maximum number of refreshes for CS1. Specifiable range: 1 to 7 (Specifying 0 is prohibited.)
CS1_TIMER_RST	R/W	24	0 Note	1	Specifies whether to reset CS1_REF_COUNT, CS1_REF_STOCK, and CS1_REF_OVER. 0: Reset This bit is automatically set to 1 during the next clock cycle.
Reserved	R	23	–	0	Reserved. When this bit is read, 0 is returned.
COUNT_COMMON	R/W	22	1	0	Specifies whether to apply the auto refresh cycle. 0: CS0 counter→CS0,CS1 refresh cycle (CS1 counter stops.) 1: CS0 counter→CS0 refresh cycle, CS1 counter→CS1 refresh cycle
CS0_STOCK_DRAIN	R/W	21:20	–	01b	Specifies how many times a refresh is executed before CS0 enters the self refresh mode. Specifiable range: 1 to 3 (Specifying 0 is prohibited.)

(2/2)

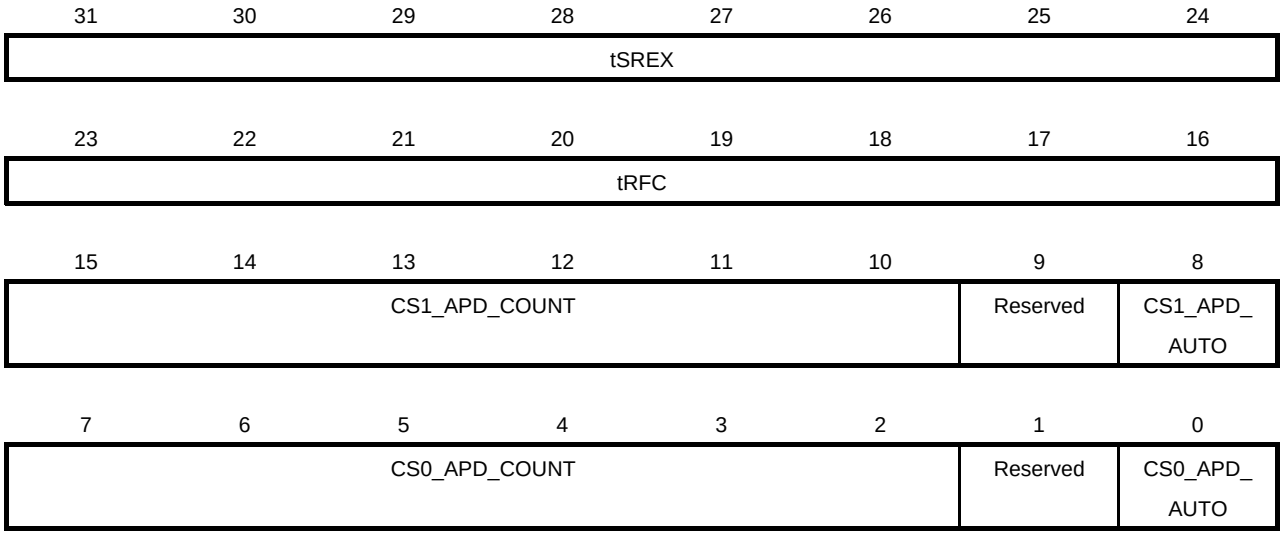
Name	R/W	Bit No.	Act	After Reset	Function
CS0_STOCK_MAX	R/W	19:17	–	7H	Specifies the maximum number of refreshes for CS0. Specifiable range: 1 to 7 (Specifying 0 is prohibited.)
CS0_TIMER_RST	R/W	16	0 Note	1	Specifies whether to reset CS0_REF_COUNT, CS0_REF_STOCK, and CS0_REF_OVER. 0: Reset This bit is automatically set to 1 during the next clock cycle.
CS1_SREF_COUNT	R/W	15:10	–	3FH	Specifies CS1 self refresh counter values. Auto self refresh entry idle counter set value multiplied by 16.
CS1_SREF_AUTO	R/W	9	1	0	Specifies whether to enable issuance of CS1 auto self refresh requests (SREF). 0: Disable 1: Enable
CS1_REF_AUTO	R/W	8	1	0	Specifies whether to enable issuance of CS1 auto refresh requests (CBR). 0: Disable 1: Enable
CS0_SREF_COUNT	R/W	7:2	–	3FH	Specifies CS0 self refresh counter values. Auto self refresh entry idle counter set value multiplied by 16.
CS0_SREF_AUTO	R/W	1	1	0	Specifies whether to enable issuance of CS0 auto self refresh requests (SREF). 0: Disable 1: Enable
CS0_REF_AUTO	R/W	0	1	0	Specifies whether to enable issuance of CS0 auto refresh requests (CBR). 0: Disable 1: Enable

Note When writing in 0, the register value returns to 1 automatically by the next clock.

The refresh counter is incremented during each refresh cycle by the REF_STOCK counter. A refresh is executed when the self refresh mode is entered or when the refresh counter reaches the threshold. When the REF_STOCK counter exceeds the maximum value, the CS0/1_REF_OVER bits of the MEMC_DDR_CONFIGR1 register are set to 1.

3.2.11 Refresh setting register 3

This register (MEMC_DDR_CONFIGR3: E00A_201CH) specifies the settings for a refresh in external memory.



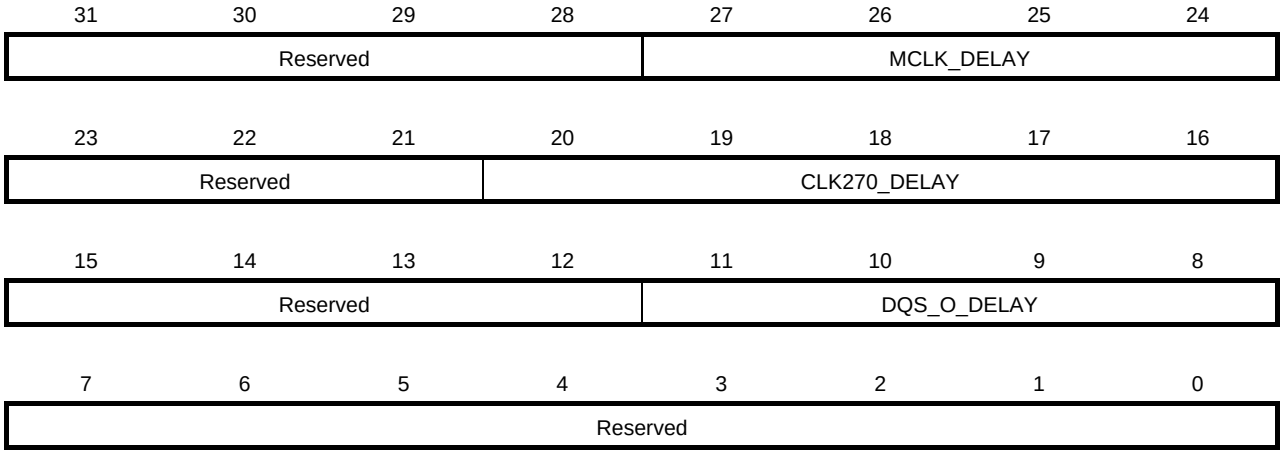
Name	R/W	Bit No.	Act	After Reset	Function
tSREX	R/W	31:24	–	00H	Self-refresh return period ([tSREX + 8] – 1) cycle.
tRFC	R/W	23:16	–	00H	Auto-refresh return period. [tRFC + 8] cycle
CS1_APD_COUNT	R/W	15:10	–	3FH	Specifies the automatic CS1 power down counter value (the idle counter value).
Reserved	R	9	–	0	Reserved. When this bit is read, 0 is returned.
CS1_APD_AUTO	R/W	8	1	0	Specifies whether to request an automatic CS1 power down. 0: Normal operation 1: Requested
CS0_APD_COUNT	R/W	7:2	–	3FH	Specifies the automatic CS0 power down counter value (the idle counter value).
Reserved	R	1	–	0	Reserved. When this bit is read, 0 is returned.
CS0_APD_AUTO	R/W	0	1	0	Specifies whether to request an automatic CS0 power down. 0: Normal operation 1: Requested

When no received requests remain in the request queue, the counter is incremented up to the value set to the CS0/1_APD_COUNT bits and then the corresponding CS automatically enters the power down mode (CKE = low level).

There is also a bit of the identical name in CONFIGA2 register, but when the value besides 0 is set as tSREX and tRFC of this register, tSREX and tRFC aren't used for the set value to tSREX of CONFIGA2 register and tRFC, and tSREX and tRFC of this register become effective.

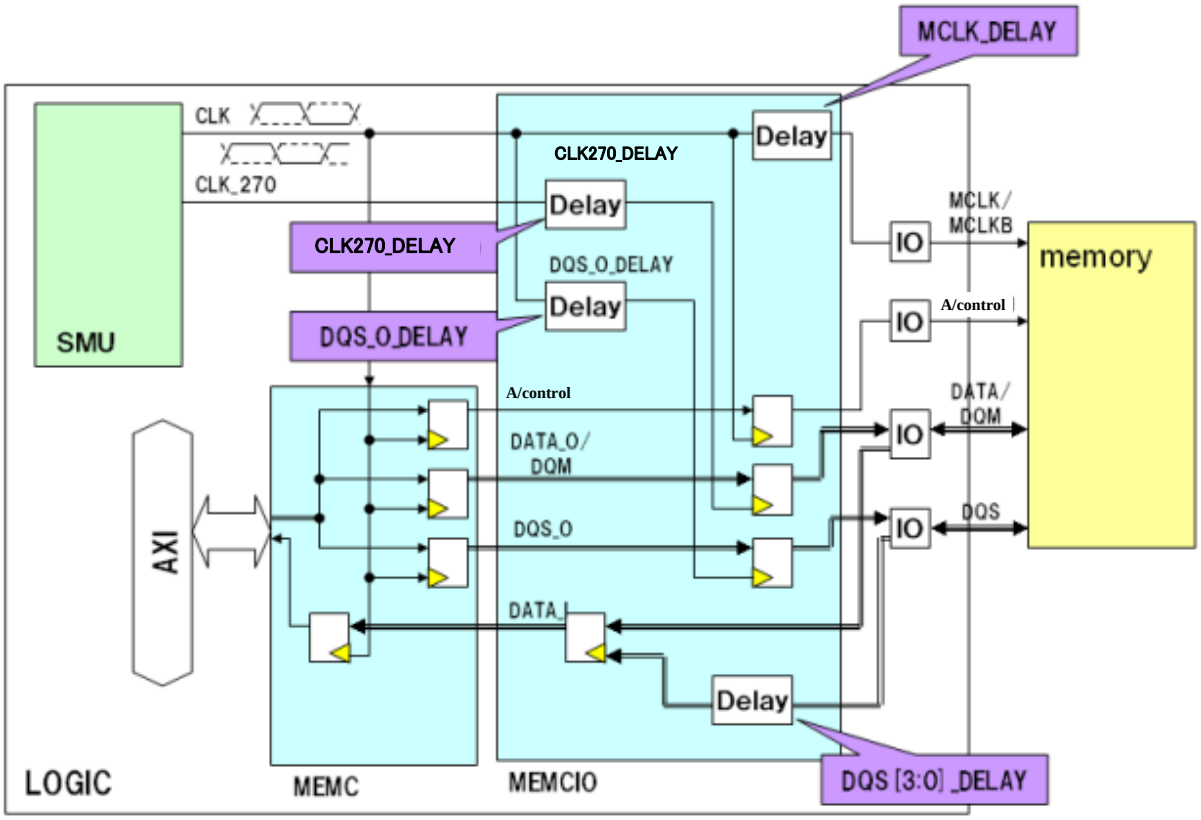
3.2.12 DQS output timing adjustment register 1

This register (MEMC_DDR_CONFIGT1: E00A_2020H) specifies adjustment of output delays in external memory.



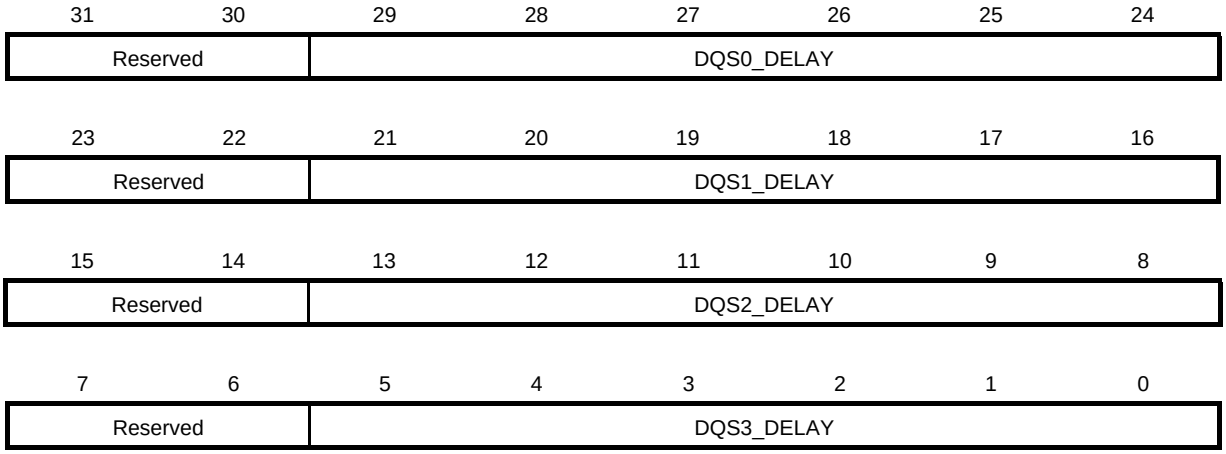
Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:28	0H	Reserved. When these bits are read, 0 is returned for each bit.
MCLK_DELAY	R/W	27:24	0H	Adjusts the MCLK delay.
Reserved	R	23:21	0H	Reserved. When these bits are read, 0 is returned for each bit.
CLK270_DELAY	R/W	20:16	00H	Adjusts the CLK270 delay.
Reserved	R	15:12	0H	Reserved. When these bits are read, 0 is returned for each bit.
DQS_O_DELAY	R/W	11:8	0H	Adjusts the delay of DQS output.
Reserved	R	7:0	03H	Reserved. When these bits are read, 0 is returned for each bit.

Delays can be added to each output DQS signal line by setting up this register. It's about 50 ps of delayed amount per set value 1.


MCLK_DELAY
CLK
CLK_270
CLK270_DELAY
Delay
Delay
CLK270_DELAY
DQS_O_DELAY
Delay
DQS_O_DELAY
SMU
A/control
DATA_O/
DQM
DQS_O
DATA_I
AXI
Delay
LOGIC
MEMC
MEMCIO
DQS [3:0] _DELAY
IO
IO
IO
IO
MCLK/
MCLKB
A/control
DATA/
DQM
DQS
memory

3.2.13 DQS input timing adjustment register 2

This register (MEMC_DDR_CONFIGT2: E00A_2024H) specifies adjustment of input delays in external memory.

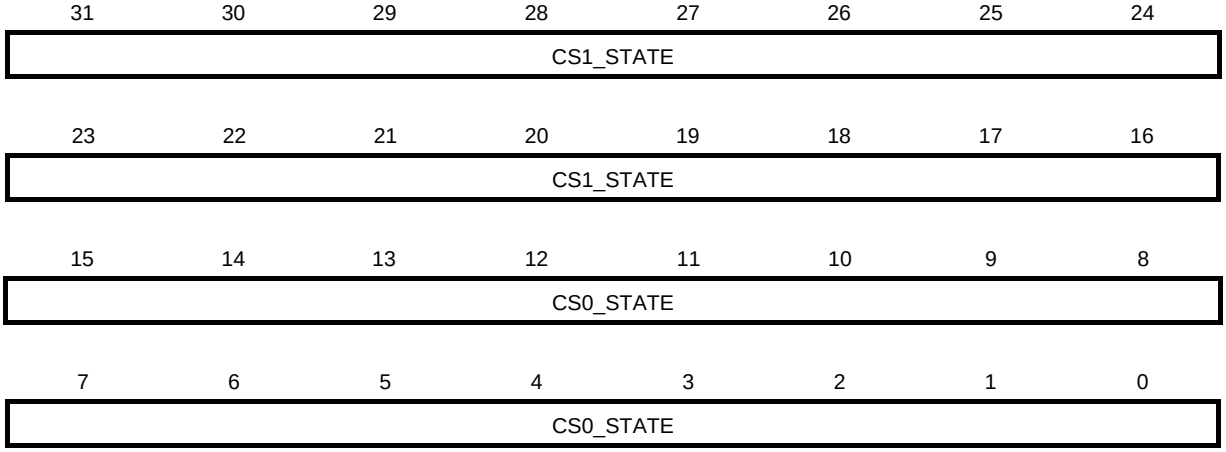


Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:30	0H	Reserved. When these bits are read, 0 is returned for each bit.
DQS0_DELAY	R/W	29:24	00H	Optimizes the DQS0 delay.
Reserved	R	23:22	0H	Reserved. When these bits are read, 0 is returned for each bit.
DQS1_DELAY	R/W	21:16	00H	Optimizes the DQS1 delay.
Reserved	R	15:14	0H	Reserved. When these bits are read, 0 is returned for each bit.
DQS2_DELAY	R/W	13:8	00H	Optimizes the DQS2 delay.
Reserved	R	7:6	0H	Reserved. When these bits are read, 0 is returned for each bit.
DQS3_DELAY	R/W	5:0	00H	Optimizes the DQS3 delay.

Delays can be added to each input DQS signal line by setting up this register. It's about 50 ps of delayed amount per set value 1.

3.2.14 Memory status check register

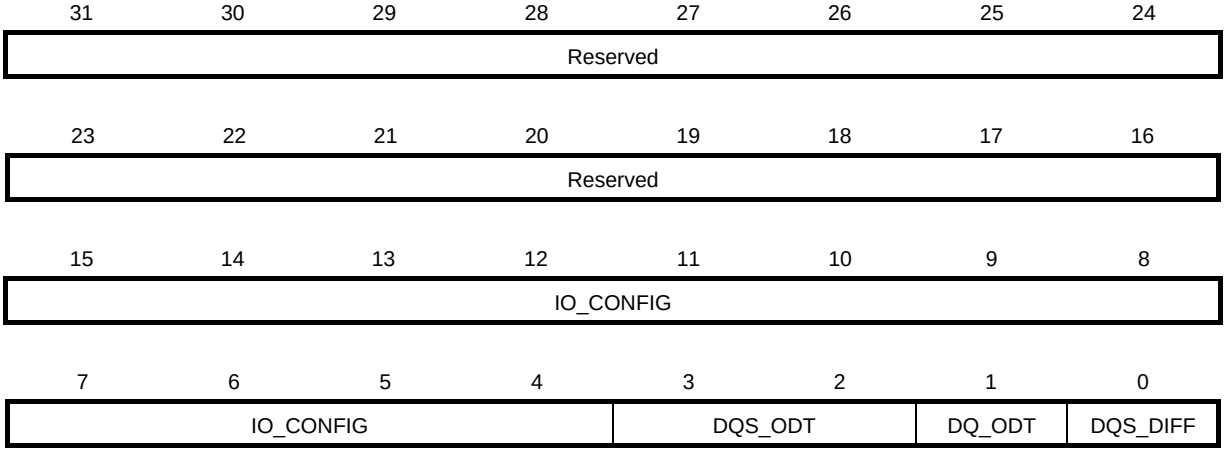
This register (MEMC_DDR_STATE8: E00A_202CH) is used to monitor the status of CS0 and CS1.



Name	R/W	Bit No.	After Reset	Function
CS1_STATE	R	31:16	0000H	Indicates the status of the memory connected to CS1. 0x0: Idle 0x1: Extended mode register setting 0x3: Self refresh 0x5: Auto power down 0x6: Self refresh end 0x7: Deep power down 0x8: Bank precharge/all bank precharge 0xA: Read/write 0xC: Forced CBR1 refresh 0xE: CBR2 refresh 0xF: Mode register setting
CS0_STATE	R	15:0	0000H	Indicates the status of the memory connected to CS0. 0x0: Idle 0x1: Extended mode register setting 0x3: Self refresh 0x5: Auto power down 0x6: Self refresh end 0x7: Deep power down 0x8: Bank precharge/all bank precharge 0xA: Read/write 0xC: Forced CBR1 refresh 0xE: CBR2 refresh 0xF: Mode register setting

3.2.15 IO configuration register

This register (MEMC_DDR_CONFIGD: E00A_2030H) specifies the settings for various in external memory.



Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:16	0000H	Reserved. When these bits are read, 0 is returned for each bit.
IO_CONFIG	R/W	15:4	800H	Configuration setting of IO buffer The recommendation set value when using DDR2 : 913H
DQS_ODT	R/W	3:2	00b	Built-in ODT setting (input for DDR_DQS[3:0], DDR_DQS [3:0]B) 00b: Disable 11b: Enable
DQ_ODT	R/W	1	0	Built-in ODT setting (input for DDR_DQ[31:0]) 0: Disable 1: Enable
DQS_DIFF	R/W	0	0	Differential/Single switched 0: Single 1: Differential (DDR_DQSB valid)

The recommendation set value of DDR2

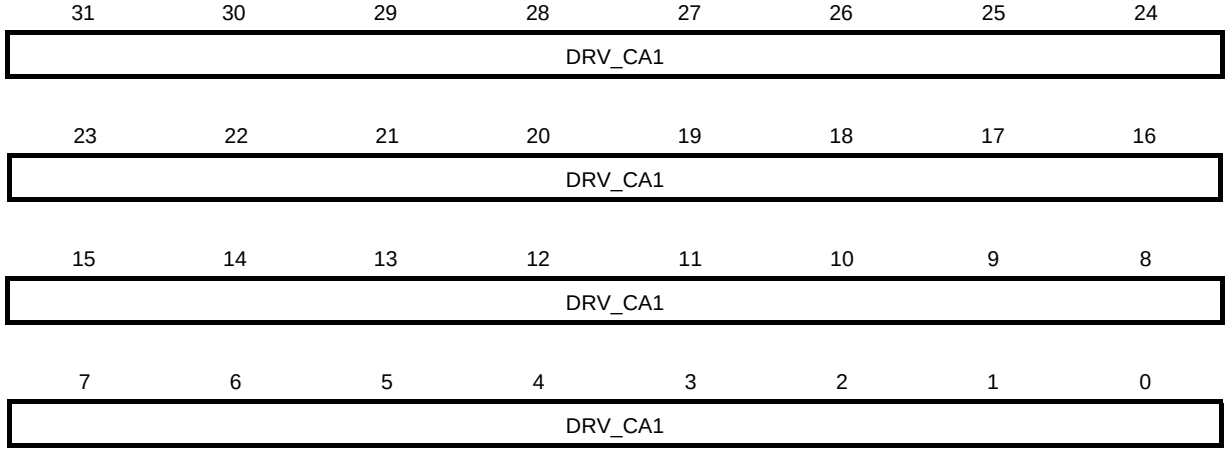
Setting value	Description
0000_9131H	DDR2, DDR_DQS differential (DDR_DQSB valid), Built-in ODT invalidity of DDR_DQ, DDR_DQS/DQSB.

The recommendation set value of LP-DDR

Setting value	Description
0000_9030H	LP-DDR, DDR_DQS differential (DDR_DQSB valid), Built-in ODT invalidity of DDR_DQ, DDR_DQS/DQSB.

3.2.16 Drive capability switch register 1

This register (MEMC_DDR_CONFIGZD: E00A_2038H) switches the I/O buffer drive capability.



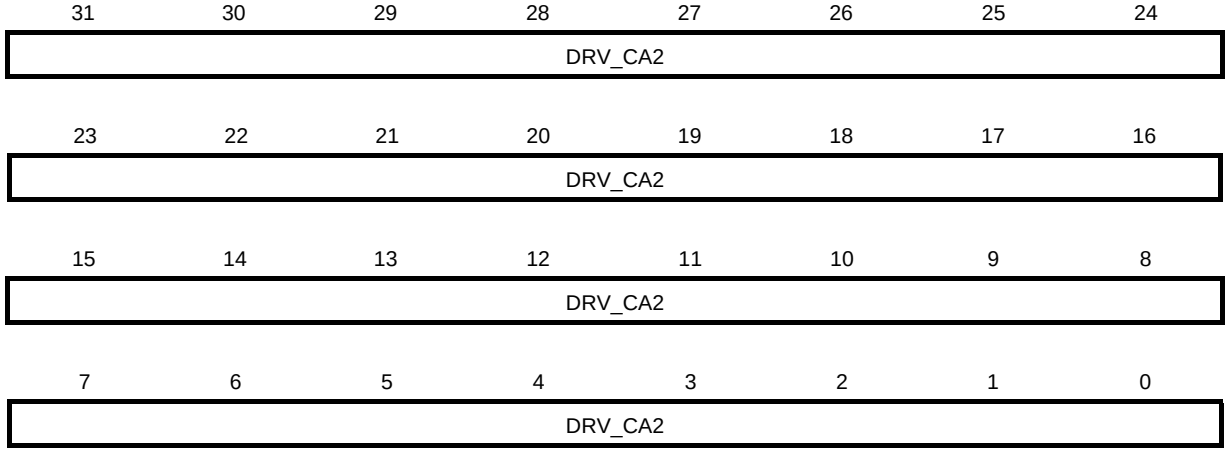
Name	R/W	Bit No.	After Reset	Function
DRV_CA1	R/W	31:0	0000_0000H	Switches the driving capability of the DDR_DQ[31:0], DDR_DQS[3:0], DDR_DQS[3:0]B, and DDR_DM[3:0] signals.

DRV_CA1	Unit (mA)	DRV_CA1	Unit (mA)
01FF_01FFH	6.3	00FF_00FFH	20.7
01FE_01FEH	7.2	00FE_00FEH	21.6
01FD_01FDH	8.1	00FD_00FDH	22.5
01FC_01FCH	9.0	00FC_00FCH	23.4
01F9_01F9H	9.9	00F9_00F9H	24.3
01F8_01F8H	10.8	00F8_00F8H	25.2
01F1_01F1H	11.7	00F1_00F1H	26.1
01F0_01F0H	12.6	00F0_00F0H	27.0
01E1_01E1H	13.5	00E1_00E1H	27.9
01E0_01E0H	14.4	00E0_00E0H	28.8
01C1_01C1H	15.3	00C1_00C1H	29.7
01C0_01C0H	16.2	00C0_00C0H	30.6
0181_0181H	17.1	0081_0081H	31.5
0180_0180H	18.0	0080_0080H	32.4
0101_0101H	18.9	0001_0001H	33.3
0100_0100H	19.8	0000_0000H	34.2

Even if the value of the other than above is established, it's invalid.

3.2.17 Drive capability switch register 2

This register (MEMC_DDR_CONFIGZC: E00A_203CH) switches the I/O buffer drive capability.



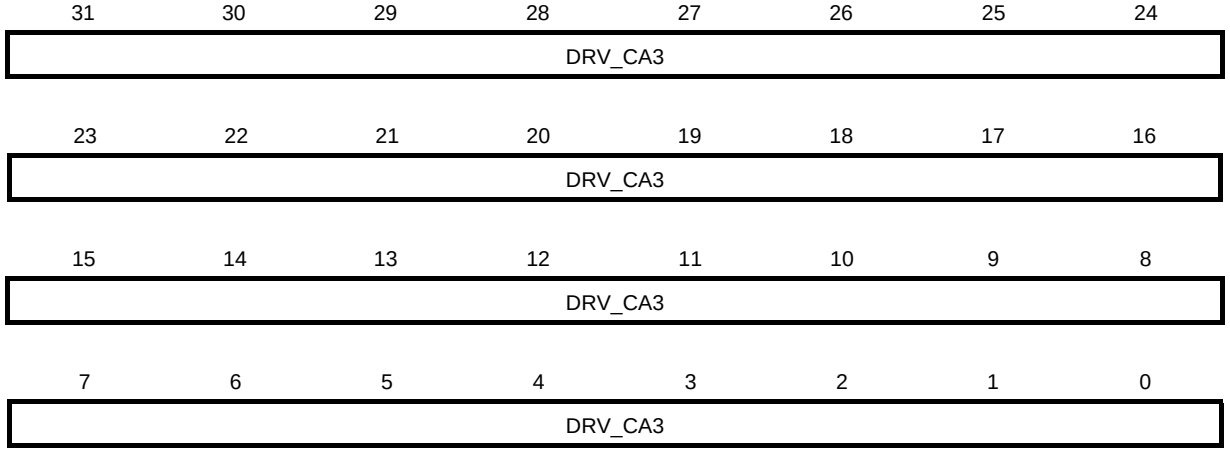
Name	R/W	Bit No.	After Reset	Function
DRV_CA2	R/W	31:0	0000_0000H	Switches the driving capability of the DDR_CK and DDR_CKB signals.

DRV_CA1	Unit (mA)	DRV_CA1	Unit (mA)
01FF_01FFH	6.3	00FF_00FFH	20.7
01FE_01FEH	7.2	00FE_00FEH	21.6
01FD_01FDH	8.1	00FD_00FDH	22.5
01FC_01FCH	9.0	00FC_00FCH	23.4
01F9_01F9H	9.9	00F9_00F9H	24.3
01F8_01F8H	10.8	00F8_00F8H	25.2
01F1_01F1H	11.7	00F1_00F1H	26.1
01F0_01F0H	12.6	00F0_00F0H	27.0
01E1_01E1H	13.5	00E1_00E1H	27.9
01E0_01E0H	14.4	00E0_00E0H	28.8
01C1_01C1H	15.3	00C1_00C1H	29.7
01C0_01C0H	16.2	00C0_00C0H	30.6
0181_0181H	17.1	0081_0081H	31.5
0180_0180H	18.0	0080_0080H	32.4
0101_0101H	18.9	0001_0001H	33.3
0100_0100H	19.8	0000_0000H	34.2

Even if the value of the other than above is established, it's invalid.

3.2.18 Drive capability switch register 3

This register (MEMC_DDR_CONFIGZA: E00A_2040H) switches the I/O buffer drive capability.



Name	R/W	Bit No.	After Reset	Function
DRV_CA3	R/W	31:0	0000_0000H	Switches the driving capability of the DDR_CS[1:0]B, DDR_BA[2:0], DDR_A[14:0], DDR_RASB, DDR_CASB, DDR_WEB and DDR_CKE[1:0] signals.

DRV_CA1	Unit (mA)	DRV_CA1	Unit (mA)
01FF_01FFH	6.3	00FF_00FFH	20.7
01FE_01FEH	7.2	00FE_00FEH	21.6
01FD_01FDH	8.1	00FD_00FDH	22.5
01FC_01FCH	9.0	00FC_00FCH	23.4
01F9_01F9H	9.9	00F9_00F9H	24.3
01F8_01F8H	10.8	00F8_00F8H	25.2
01F1_01F1H	11.7	00F1_00F1H	26.1
01F0_01F0H	12.6	00F0_00F0H	27.0
01E1_01E1H	13.5	00E1_00E1H	27.9
01E0_01E0H	14.4	00E0_00E0H	28.8
01C1_01C1H	15.3	00C1_00C1H	29.7
01C0_01C0H	16.2	00C0_00C0H	30.6
0181_0181H	17.1	0081_0081H	31.5
0180_0180H	18.0	0080_0080H	32.4
0101_0101H	18.9	0001_0001H	33.3
0100_0100H	19.8	0000_0000H	34.2

Even if the value of the other than above is established, it's invalid.

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Rev.	Date	Description	
		Page	Summary
1.00	Mar 31, 2010	—	1st revision release
2.00	Jun 7, 2010	—	Incremental update from comments to the 1.0.
3.00	Jun 30, 2010	—	Incremental update from comments to the 2.0. (A change part from the old version is "★" marked in the page left end.)
4.00	Sep 30, 2010	—	Incremental update from comments to the 3.0. (A change part from the old version is "★" marked in the page left end.)
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6.00	May 31, 2011	—	Incremental update from comments to the 5.0.
7.00	Sep 30, 2011	—	Incremental update from comments to the 6.0.
		4	Chapter 3.1.3 corrected. (After reset value of 2030H)
		22	Chapter 3.2.10 corrected. (Function of bit[22].)
8.00	Dec 21, 2011	21	Chapter 3.2.9 corrected. (bit[10:0] Function)

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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