User's Manual

Pulse Width Modulation Interface

User's Manual

Multimedia Processor for Mobile Applications
EMMA Mobile ™ EV2

Renesas Electronics
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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the EMMA Mobile EV2. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Data Sheet	Hardware overview and electrical characteristics	EMMA Mobile EV2 Datasheet	R19DS0010EJxxxx
User's manual (1chip)	Hardware whole specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description	EMMA Mobile EV2 User's manual 1chip	R19UH0036EJxxxx
User's manual (module)	Hardware each macro specifications and operation description.	EMMA Mobile EV2 User's manual each module	See below

Document Name	Document No.	Document Name	Document No.
1chip	R19UH0036EJxxxx	DMA Controller	R19UH0043EJxxxx
System Management Unit	R19UH0037EJxxxx	LP-DDR/DDR2 Controller	R19UH0039EJxxxx
Timer	R19UH0054EJxxxx	SD Memory Card Interface	R19UH0061EJxxxx
System Timer	R19UH0055EJxxxx	SDIO Interface	R19UH0042EJxxxx
HD Video Decoder	R19UH0056EJxxxx	CF Card Interface	R19UH0062EJxxxx
Rotator	R19UH0057EJxxxx	Unified Serial Interface	R19UH0047EJxxxx
Resizer	R19UH0058EJxxxx	UART interface	R19UH0040EJxxxx
Image Composer	R19UH0038EJxxxx	USB 2.0 Host Controller	R19UH0045EJxxxx
LCD Interface	R19UH0044EJxxxx	USB 2.0 Function Controller	R19UH0034EJxxxx
ITU-R BT.656 Interface	R19UH0059EJxxxx	IIC Interface	R19UH0052EJxxxx
Digital Terrestrial TV Interface	R19UH0048EJxxxx	General Purpose I/O Interface	R19UH0041EJxxxx
Camera Interface	R19UH0060EJxxxx	Pulse Width Modulation Interface (This manual)	R19UH0063EJxxxx

4 digits of end shows the version.

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names

Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.

Examples the PM03 bit in the PM0 register

P3_5 pin, VCC pin

(2) Notation of Numbers

The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.

Examples Binary: 11b or 11

Hexadecimal: EFA0h

Decimal: 1234

3. Register Notation

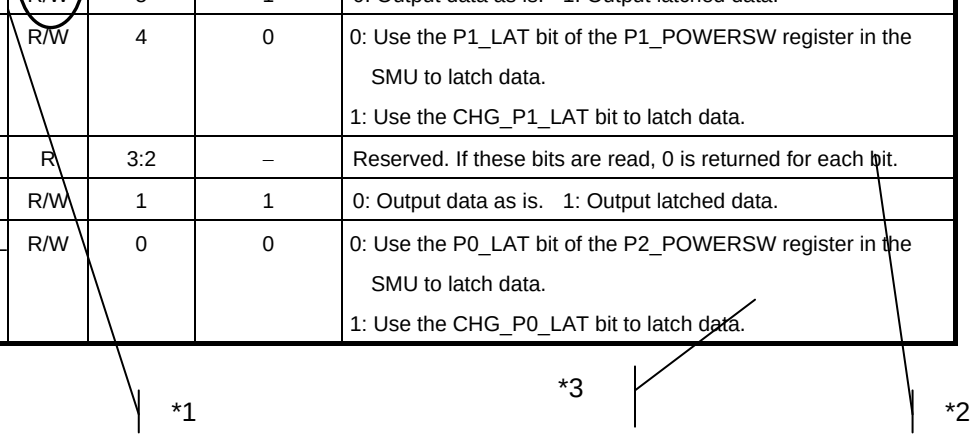
The symbols and terms used in register diagrams are described below.

x.x.x XXX register

This register (XXXXXXX: xxxx_xxxxh) …..

7	6	5	4	3	2	1	0
Reserved		CHG_P1_LAT	LATCH_P1_SEL	Reserved		CHG_P0_LAT	CHG_P0_LAT_SEL

Name	R/W	Bit No.	After Reset	Description
LATCH_P2_SEL	R/W	8	0	0: Use the P2_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P2_LAT bit to latch data.
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P1_LAT	R/W	5	1	0: Output data as is. 1: Output latched data.
LATCH_P1_SEL	R/W	4	0	0: Use the P1_LAT bit of the P1_POWERSW register in the SMU to latch data. 1: Use the CHG_P1_LAT bit to latch data.
Reserved	R	3:2	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P0_LAT	R/W	1	1	0: Output data as is. 1: Output latched data.
CHG_P0_LAT_SEL	R/W	0	0	0: Use the P0_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P0_LAT bit to latch data.



*1

R/W: Read and Write.

R: Read only.

W: Write only.

-: Nothing is assigned.

*2

Reserved bit.

Reserved bit. Set to specified value.

*3

・ Nothing is assigned.

Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.

・ Do not set to a value.

Operation is not guaranteed when a value is set.

・ Function varies according to the operating mode.

The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Register
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

Abbreviation	Full Form
APB	Advanced Peripheral Bus
GPIO	General Purpose I/O
INT	Interrupt
SMU	System Management Unit
TIM	Timer Module

Table of Contents

1. Overview

1.1 Features

The major features of the PWM interface are listed below.

The PWM interface outputs pulse-width-modulated signals. It is mainly used for the beep sound generator, motor control, and LCD modulation control.

- ○ 2-channel PWM output
- ○ Waveform generation
  - Three 32-bit counters per channel
  - Delay (DELAY), leading edge (LEDGE), trailing edge (TEDGE), and total cycle (TOTAL) can be defined separately.
  - Modulation by logic operators between counters (AND, OR, XOR) and for each counter (NOT)
- ○ The number of repetitions can be specified per counter (managed by 16-bit counters).
- ○ Independent counter clock (clock for generating PWM waveform)

1.2 Function Block Diagram

Figure 1-1. Function Block Diagram

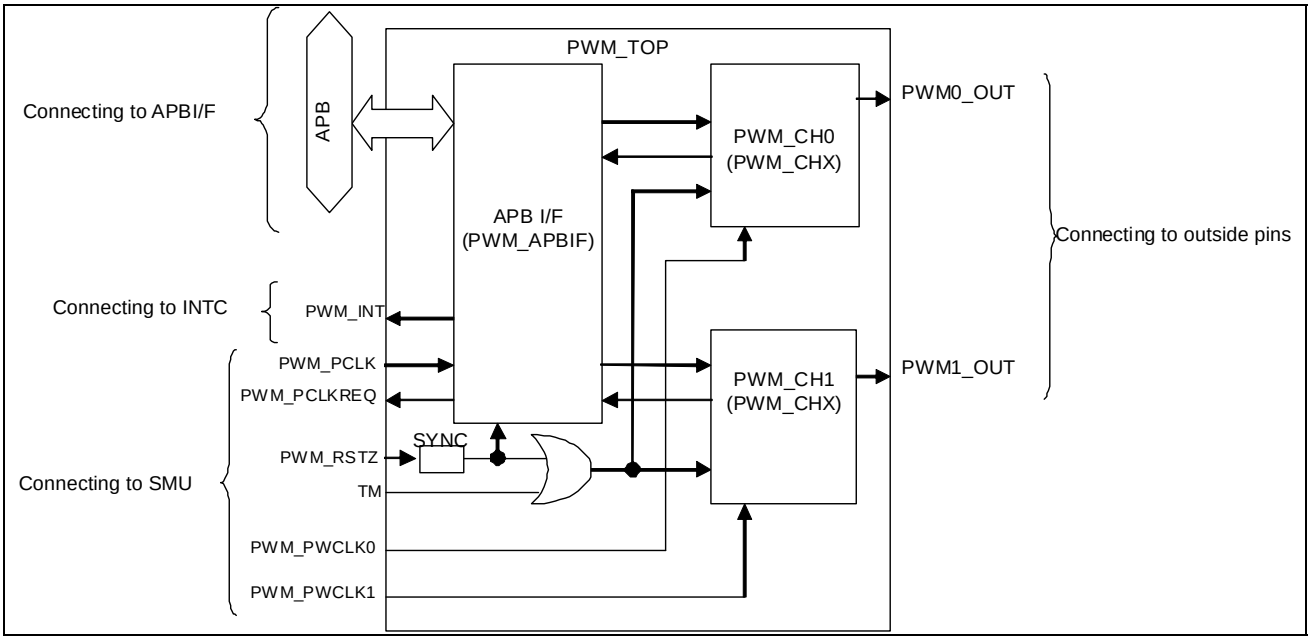
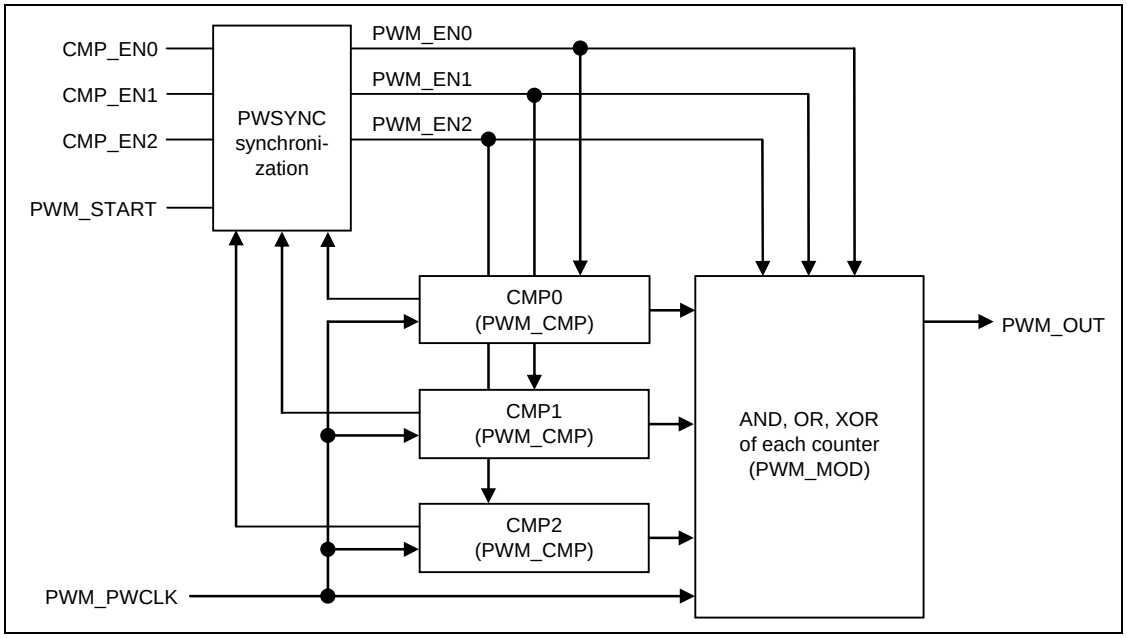


Figure 1-2. Function Block Diagram (One channel)



2. Pin functions

Pin Name	I/O	After Reset	Function	Alternate Pin Function
PWM0	Output	0	PWM output	USI4_DI, GPIO_120
PWM1	Output	0	PWM output	USI4_DO, GPIO_121

3. Registers

3.1 Register List

The registers of the audio/voice and PWM interface allow word access only.
Operation is not guaranteed if an attempt is made to execute halfword or byte access.
Do not access the reserved registers.

Base address: E113_0000H

Table 3-1. PWM Channel 0 Registers

Address	Register Name	Register Symbol	R/W	After Reset
0000H	PWM operation start/stop register	PWM_CH0_CTRL	R/W	0000_0000H
0004H	PWM0 mode control register	PWM_CH0_MODE	R/W	0000_0000H
0008H to 000CH	Reserved	–	–	–
0010H	Channel 0 counter 0 delay setting register	PWM_CH0_DELAY0	R/W	0000_0000H
0014H	Channel 0 counter 0 leading edge setting register	PWM_CH0_LEDGE0	R/W	0000_0000H
0018H	Channel 0 counter 0 trailing edge setting register	PWM_CH0_TEDGE0	R/W	0000_0000H Note
001CH	Channel 0 counter 0 total cycle setting register	PWM_CH0_TOTAL0	R/W	0000_0000H Note
0020H	Channel 0 counter 0 loop count setting register	PWM_CH0_LOOP0	R/W	0000_0001H Note
0024H to 003CH	Reserved	–	–	–
0040H	Channel 0 counter 1 delay setting register	PWM_CH0_DELAY1	R/W	0000_0000H
0044H	Channel 0 counter 1 leading edge setting register	PWM_CH0_LEDGE1	R/W	0000_0000H
0048H	Channel 0 counter 1 trailing edge setting register	PWM_CH0_TEDGE1	R/W	0000_0000H Note
004CH	Channel 0 counter 1 total cycle setting register	PWM_CH0_TOTAL1	R/W	0000_0000H Note
0050H	Channel 0 counter 1 loop count setting register	PWM_CH0_LOOP1	R/W	0000_0001H Note
0054H to 007CH	Reserved	–	–	–
0080H	Channel 0 counter 2 delay setting register	PWM_CH0_DELAY2	R/W	0000_0000H
0084H	Channel 0 counter 2 leading edge setting register	PWM_CH0_LEDGE2	R/W	0000_0000H
0088H	Channel 0 counter 2 trailing edge setting register	PWM_CH0_TEDGE2	R/W	0000_0000H Note
008CH	Channel 0 counter 2 total cycle setting register	PWM_CH0_TOTAL2	R/W	0000_0000H Note
0090H	Channel 0 counter 2 loop count setting register	PWM_CH0_LOOP2	R/W	0000_0001H Note
0094H to 00FCH	Reserved	–	–	–

Note Do not set PWM_CH0_TEDGEn, PWM_CH0_TOTALn, and PWM_CH0_LOOPn to the After Reset value (0000_0000H). Be sure to use the updated values.

Remark The addresses in the above table are relative values from the start address of the areas assigned to PWM control.

Table 3-2. PWM Channel 1 Registers

Address	Register Name	Register Symbol	R/W	After Reset
0100H	PWM operation start/stop register	PWM_CH1_CTRL	R/W	0000_0000H
0104H	PWM0 mode control register	PWM_CH1_MODE	R/W	0000_0000H
0108H to 010CH	Reserved	–	–	–
0110H	Channel 1 counter 0 delay setting register	PWM_CH1_DELAY0	R/W	0000_0000H
0114H	Channel 1 counter 0 leading edge setting register	PWM_CH1_LEDGE0	R/W	0000_0000H
0118H	Channel 1 counter 0 trailing edge setting register	PWM_CH1_TEDGE0	R/W	0000_0000H Note
011CH	Channel 1 counter 0 total cycle setting register	PWM_CH1_TOTAL0	R/W	0000_0000H Note
0120H	Channel 1 counter 0 loop count setting register	PWM_CH1_LOOP0	R/W	0000_0001H Note
0124H to 013CH	Reserved	–	–	–
0140H	Channel 1 counter 1 delay setting register	PWM_CH1_DELAY1	R/W	0000_0000H
0144H	Channel 1 counter 1 leading edge setting register	PWM_CH1_LEDGE1	R/W	0000_0000H
0148H	Channel 1 counter 1 trailing edge setting register	PWM_CH1_TEDGE1	R/W	0000_0000H Note
014CH	Channel 1 counter 1 total cycle setting register	PWM_CH1_TOTAL1	R/W	0000_0000H Note
0150H	Channel 1 counter 1 loop count setting register	PWM_CH1_LOOP1	R/W	0000_0001H Note
0154H to 017CH	Reserved	–	–	–
0180H	Channel 1 counter 2 delay setting register	PWM_CH1_DELAY2	R/W	0000_0000H
0184H	Channel 1 counter 2 leading edge setting register	PWM_CH1_LEDGE2	R/W	0000_0000H
0188H	Channel 1 counter 2 trailing edge setting register	PWM_CH1_TEDGE2	R/W	0000_0000H Note
018CH	Channel 1 counter 2 total cycle setting register	PWM_CH1_TOTAL2	R/W	0000_0000H Note
0190H	Channel 1 counter 2 loop count setting register	PWM_CH1_LOOP2	R/W	0000_0001H Note
0194H to 03FCH	Reserved	–	–	–

Note Do not set PWM_CH1_TEDGEn, PWM_CH1_TOTALn, and PWM_CH1_LOOPn to the After Reset value (0000_0000H). Be sure to use the updated values.

Table 3-3. PWM Interrupt Registers

Address	Register Name	Register Symbol	R/W	After Reset
0400H	PWM interrupt status register	PWM_INTSTATUS	R	0000_0000H
0404H	PWM interrupt raw status register	PWM_INTRAWSTATUS	R	0000_0000H
0408H	PWM interrupt enable set register	PWM_INTENSET	R/W	0000_0000H
040CH	PWM interrupt enable clear register	PWM_INTENCLR	W	0000_0000H
0410H	PWM interrupt source clear register	PWM_INTFFCLR	W	0000_0000H
0414H to FFFCH	Reserved	–	–	–

3.2 Register Details

In the register descriptions, *x* indicates a channel number and *n* indicates a counter number. Here, x = 0 or 1 and n = 0 to 2.

3.2.1 PWM control registers

(1) PWM operation start/stop register

These registers (PWM_CH0_CTRL: E113_0000H, PWM_CH1_CTRL: E113_0100H) starts PWM.
The counter operation starts if the PWM_START bit is set to 1 after the CMP_ENn bit (CMP enable) of the PWM_CHx_MODE register is set to 1. The counter does not start if the PWM_START bit is set to 0 even if the CMP_ENn bit of the PWM_CHx_MODE register is set to 1.
If the PWM_START bit is set to 0 during counter operation, the counter stops after synchronization with PWM_PWCLKx and PWM_OUT becomes 0.
The operation status of each counter can be read by using the PWM_ENn bit.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved	PWM_EN2	PWM_EN1	PWM_EN0	Reserved			PWM_START

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:7	000_0000H	Reserved. When these bits are read, 0 is returned for each bit.
PWM_EN2[Note 1]	R	6	0	Status of CMP2 counter 0: Counter has stopped 1: Counter is running
PWM_EN1[Note 1]	R	5	0	Status of CMP1 counter 0: Counter has stopped 1: Counter is running
PWM_EN0[Note 1]	R	4	0	Status of CMP0 counter 0: Counter has stopped 1: Counter is running
Reserved	R	3:1	0H	Reserved. When these bits are read, 0 is returned.
PWM_START[Note 2]	R/W	0	0	0: Counter stops 1: Counter starts

Notes 1. Since the PWM_ENn bit does not synchronize with the system clock, the value of each status may deviate at the point the signals change.

2. If restarting the counter, set the PWM_START bit to 0 and then wait for at least three PWM_PWCLKx clocks.

3.2.2 PWM setting registers

(1) PWM mode control register

These registers (PWM_CH0_MODE: E113_0004H, PWM_CH1_MODE: E113_0104H) specify the PWM operation mode.

By setting the PWM_START bit of the PWM_CTRL register to 1 after enabling the CMP_ENn bit, the corresponding CMPn starts operating.

Caution Setting this register is prohibited while the counter is running. The operation is not guaranteed if this register is set when the PWM_START bit of the PWM_Chx_CTRL register is set to 1.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved						MOD	

15	14	13	12	11	10	9	8
Reserved					CMP_INV2	CMP_ATST2	CMP_EN2

7	6	5	4	3	2	1	0
Reserved	CMP_INV1	CMP_ATST1	CMP_EN1	Reserved	CMP_INV0	CMP_ATST0	CMP_EN0

(1/2)

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:18	0000H	Reserved. When these bits are read, 0 is returned for each bit.
MOD	R/W	17:16	00b	00b: OR for compare value signals of CMP0 to CMP2 01b: AND for compare value signals of CMP0 to CMP2 10b: XOR for compare value signals of CMP0 to CMP2
Reserved	R	15:11	00H	Reserved. When these bits are read, 0 is returned for each bit.
CMP_INV2	R/W	10	0	0: Output of CMP2 compare result 1: Inverted output of CMP2 compare result
CMP_ATST2	R/W	9	0	0: Infinite loop of CMP2 (does not terminate automatically) 1: CMP2 automatically terminates after looping the number of times set in PWM_CHx_LOOP2.
CMP_EN2	R/W	8	0	0: CMP2 disable 1: CMP2 operation enable If CMP_ATST2 is set to 1, the value automatically becomes 0 after looping.
Reserved	R	7	0	Reserved. When this bit is read, 0 is returned.
CMP_INV1	R/W	6	0	0: Output of CMP1 compare result 1: Inverted output of CMP1 compare result
CMP_ATST1	R/W	5	0	0: Infinite loop of CMP1 (does not terminate automatically) 1: CMP1 automatically terminates after looping the number of times set in PWM_CHx_LOOP1.

(2/2)

Name	R/W	Bit No.	After Reset	Function
CMP_EN1	R/W	4	0	0: CMP1 disable 1: CMP1 operation enable If CMP_ATST1 is set to 1, the value automatically becomes 0 after looping.
Reserved	R	3	0	Reserved. When this bit is read, 0 is returned.
CMP_INV0	R/W	2	0	0: Output of CMP0 compare result 1: Inverted output of CMP0 compare result
CMP_ATST0	R/W	1	0	0: Infinite loop of CMP0 (does not terminate automatically) 1: CMP0 automatically terminates after looping the number of times set in PWM_CHx_LOOP0.
CMP_EN0	R/W	0	0	0: CMP0 disable 1: CMP0 operation enable If CMP_ATST0 is set to 1, the value automatically becomes 0 after looping.

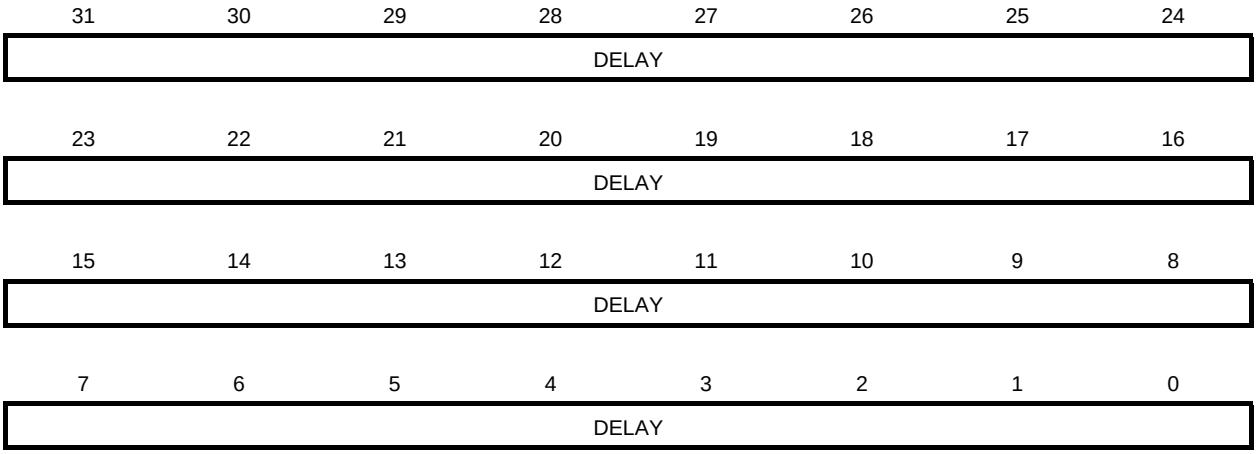
The PWM output is as follows, depending on the setting of the MOD bit of the PWM_CHx_MODE register and the CMP0_ENn bit of the PWM_CHx_MODE register.

	OR Specification MOD = 00b	AND Specification MOD = 01b	XOR Specification MOD = 10b	Setting Prohibited MOD = 11b
CMP0 to CMP2 disable CMP_EN = 000b	0	0	0	–
Only CMP0 enable CMP_EN = 001b	CMP0	CMP0	CMP0	–
CMP0 and CMP1 enable CMP_EN = 011b	CMP0 | CMP1	CMP0 & CMP1	CMP0 ^ CMP1	–
CMP0 to CMP2 enable CMP_EN = 111b	CMP0 | CMP1 | CMP2	CMP0 & CMP1 & CMP2	CMP0 ^ CMP1 ^ CMP2	–

(2) Channel x counter n delay setting registers

These registers specify the delay after CMPn starts operating. The starting time of the counter can be delayed for PWM_PWCLKn cycles × DELAY.

- PWM_CH0_DELAY0: E113_0010H
- PWM_CH0_DELAY1: E113_0040H
- PWM_CH0_DELAY2: E113_0080H
- PWM_CH1_DELAY0: E113_0110H
- PWM_CH1_DELAY1: E113_0140H
- PWM_CH1_DELAY2: E113_0180H



Name	R/W	Bit No.	After Reset	Function
DELAY	R/W	31:0	0000_0000H	Delay value setting bit 0000_0000H: No delay. No delay period is set. 0000_0001H: Delays PWM_PWCLK × 1 cycle from the reference time (delays for 83.3 ns). 0000_0002H: Delays PWM_PWCLK × 2 cycles from the reference time (delays for 166.6 ns). : 0000_FFFFH: Delays PWM_PWCLK × 66,535 cycles from the reference time (delays for 5.5423 ms). : FFFF_FFFFH: Delays PWM_PWCLK × 4,294,967,295 cycles from the reference time (delays for 357.7707757 s).

Remark The values in parentheses refer to when the frequency of PWM_PWCLKx is 12 MHz.

(3) Channel x counter n leading edge setting registers

These registers specify the leading edge of counter n. A low level (high level if inverted) is output from CMPn for the period of PWM_PWCLKn cycles × LEDGE from the next cycle after the delay period has finished. See **Figure 4-1 Timing When Only Counter 0 Runs.**

- PWM_CH0_LEDGE0: E113_0014H
- PWM_CH0_LEDGE1: E113_0044H
- PWM_CH0_LEDGE2: E113_0084H
- PWM_CH1_LEDGE0: E113_0114H
- PWM_CH1_LEDGE1: E113_0144H
- PWM_CH1_LEDGE2: E113_0184H

31	30	29	28	27	26	25	24
LEDGE							

23	22	21	20	19	18	17	16
LEDGE							

15	14	13	12	11	10	9	8
LEDGE							

7	6	5	4	3	2	1	0
LEDGE							

Name	R/W	Bit No.	After Reset	Function
LEDGE[Note]	R/W	31:0	0000_0000H	Leading edge period setting bit 0000_0000H: No LEDGE period when this value is set. 0000_0001H: Outputs low level for PWM_PWCLK × 1 cycle (83.3 ns). 0000_0002H: Outputs low level for PWM_PWCLK × 2 cycles (166.6 ns). : 0000_FFFFH: Outputs low level for PWM_PWCLK × 66,535 cycles (5.5423 ms). : FFFF_FFFFH: Outputs low level for PWM_PWCLK × 4,294,967,295 cycles (357.7707757 s).

Note The following restriction applies: PWM_CHx_LEDGEn < PWM_CHx_TEDGEn ≤ PWM_CHx_TOTALn.

Remark The values in the parentheses refer to when the frequency of PWM_PWCLKx is 12 MHz.

(4) Channel x counter n trailing edge setting registers

These registers specify the trailing edge of counter n. A high level (low level if inverted) is output from CMPn for the period specified by TEDGE from the next cycle after the LEDGE period has finished.
The pulse width is the period of the PWM_PWCLK cycles × (TEDGE – LEDGE). See **Figure 4-1 Timing When Only Counter 0 Runs**.

- PWM_CH0_TEDGE0: E113_0018H
- PWM_CH0_TEDGE1: E113_0048H
- PWM_CH0_TEDGE2: E113_0088H
- PWM_CH1_TEDGE0: E113_0118H
- PWM_CH1_TEDGE1: E113_0148H
- PWM_CH1_TEDGE2: E113_0188H

31	30	29	28	27	26	25	24
TEDGE							

23	22	21	20	19	18	17	16
TEDGE							

15	14	13	12	11	10	9	8
TEDGE							

7	6	5	4	3	2	1	0
TEDGE							

Name	R/W	Bit No.	After Reset	Function
TEDGE[Note 1]	R/W	31:0	0000_0000H[Note 2]	Trailing edge period setting bit The following is output when LEDGE = 0. 0000_0000H: Setting prohibited[Note 2] 0000_0001H: Outputs high level for PWM_PWCLK × 1 cycle (83.3 ns). 0000_0002H: Outputs high level for PWM_PWCLK × 2 cycles (166.6 ns). : 0000_FFFFH: Outputs high level for PWM_PWCLK × 66,535 cycles (5.5423 ms). : FFFF_FFFFH: Outputs high level for PWM_PWCLK × 4,294,967,295 cycles (357.7707757 s).

Notes 1. The following restriction applies: PWM_CHx_LEDGEn < PWM_CHx_TEDGEn ≤ PWM_CHx_TOTALn.

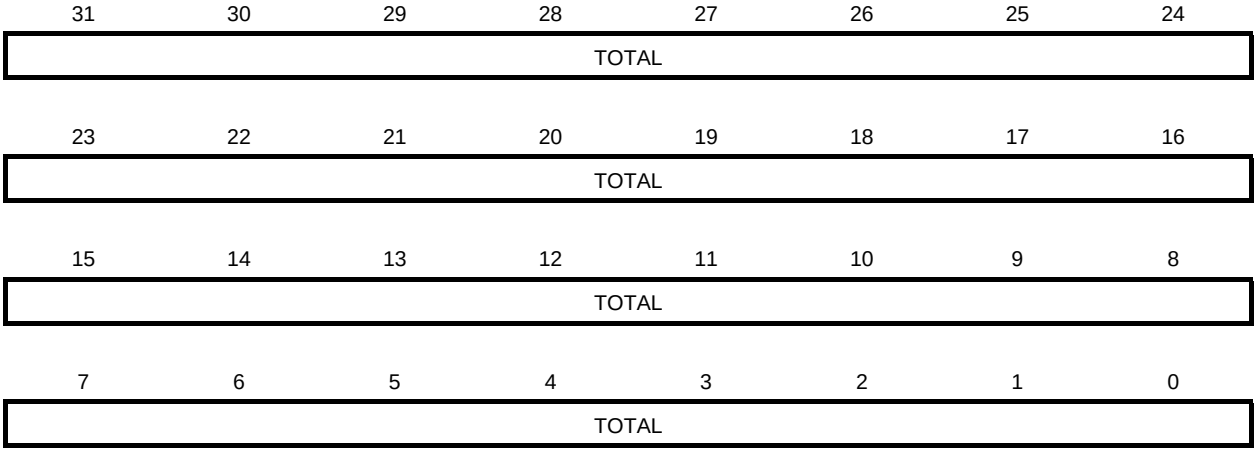
2. Setting of After Reset value (0000_0000H) is prohibited if PWM_CHx_LEDGEn is set to 0. Be sure to use the updated value.

Remark The values in the parentheses refer to when the frequency of PWM_PWCLKx is 12 MHz.

(5) Channel x counter n total cycle setting registers

These registers specify one cycle of counter n. The length of one cycle is PWM_PWCLK cycles × TOTAL. Setting 0000_0000H is prohibited. The operation is not guaranteed if this value is set.

- PWM_CH0_TOTAL0: E113_001CH
- PWM_CH0_TOTAL1: E113_004CH
- PWM_CH0_TOTAL2: E113_008CH
- PWM_CH1_TOTAL0: E113_011CH
- PWM_CH1_TOTAL1: E113_014CH
- PWM_CH1_TOTAL2: E113_018CH



Name	R/W	Bit No.	After Reset	Function
TOTAL[Note 1]	R/W	31:0	0000_0000H[Note 2]	Total cycle setting bit 0000_0000H: Setting prohibited[Note 2] 0000_0001H: The cycle is PWM_PWCLK × 1 cycle (83.3 ns) 0000_0002H: The cycle is PWM_PWCLK × 2 cycles (166.6 ns) : 0000_FFFFH: The cycle is PWM_PWCLK × 66,535 cycles (5.5423 ms) : FFFF_FFFFH: The cycle is PWM_PWCLK × 4,294,967,295 cycles (357.7707757 s)

Notes 1. The following restriction applies: PWM_CHx_LEDGEn < PWM_CHx_TEDGEn ≤ PWM_CHx_TOTALn.

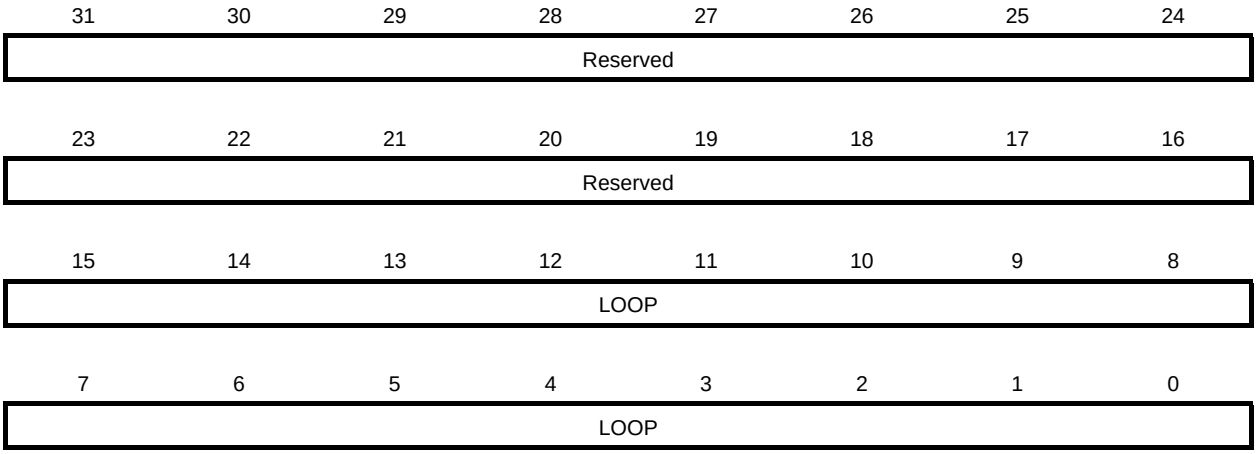
2. Setting of After Reset value (0000_0000H) is prohibited. Be sure to use the updated value.

Remark The values in the parentheses refer to when the frequency of PWM_PWCLKx is 12 MHz.

(6) Channel x counter n loop count setting register

These registers specify the number of cycles to be repeated. The counter automatically stops after repetition is over.

- PWM_CH0_LOOP0: E113_0020H
- PWM_CH0_LOOP1: E113_0050H
- PWM_CH0_LOOP2: E113_0090H
- PWM_CH1_LOOP0: E113_0120H
- PWM_CH1_LOOP1: E113_0150H
- PWM_CH1_LOOP2: E113_0190H



Name	R/W	Bit No.	After Reset	Function
Reserved	R/W	31:16	0000H	Reserved. When these bits are read, 0 is returned for each bit.
LOOP[Note 1]	R/W	15:0	0001H[Note 2]	0000H: Setting prohibited[Note 2] 0001H: The counter stops after one count. 0002H: The counter stops after two repetitions. : FFFFH: The cycle counter stops after 66,535 repetitions.

Notes 1. The counter does not automatically stop if the CMP_ATSTn bit of the PWM_CHx_MODE register is set to 0 even if a value is set. If the CMP_ATSTn bit is set to 1, setting 0000H is prohibited. Be sure to set a value of 1 or more.

2. Setting of the value after reset (0000_0000H) is prohibited. Be sure to use the updated value.

3.2.3 PWM interrupt registers

The PWM interface has two interrupts for each counter.

- Count completion interrupt: Generated for each count until the counter reaches the total cycle.
- Loop completion interrupt: Generated when the specified number of loops are complete when loops are specified.

The PWM_INT pin outputs each ORed interrupt status (PWM_INTSTATUS) signal.

(1) PWM interrupt status register

This register (PWM_INTSTATUS: E113_0400H) indicates the status of the interrupt sources that are enabled in the PWM_INTENSET register.

If a source is disabled, 0 is read.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved		Ch1_CMP2_ LENDSTATUS	Ch1_CMP2_ CENDSTATUS	Ch1_CMP1_ LENDSTATUS	Ch1_CMP1_ CENDSTATUS	Ch1_CMP0_ LENDSTATUS	Ch1_CMP0_ CENDSTATUS

7	6	5	4	3	2	1	0
Reserved		Ch0_CMP2_ LENDSTATUS	Ch0_CMP2_ CENDSTATUS	Ch0_CMP1_ LENDSTATUS	Ch0_CMP1_ CENDSTAUS	Ch0_CMP0_ LENDSTATUS	Ch0_CMP0_ CENDSTATUS

(1/2)

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:14	0_0000H	Reserved. When these bits are read, 0 is returned for each bit.
Ch1_CMP2_LENDSTATUS	R	13	0	Indicates the status of the loop completion interrupt for CMP2 on channel 1.
Ch1_CMP2_CENDSTATUS	R	12	0	Indicates the status of the count completion interrupt for CMP2 on channel 1.
Ch1_CMP1_LENDSTATUS	R	11	0	Indicates the status of the loop completion interrupt for CMP1 on channel 1.
Ch1_CMP1_CENDSTATUS	R	10	0	Indicates the status of the count completion interrupt for CMP1 on channel 1.
Ch1_CMP0_LENDSTATUS	R	9	0	Indicates the status of the loop completion interrupt for CMP0 on channel 1.
Ch1_CMP0_CENDSTATUS	R	8	0	Indicates the status of the count completion interrupt for CMP0 on channel 1.

(2/2)

Name	R/W	Bit No.	After Reset	Function
Reserved	R	7:6	0H	Reserved. When these bits are read, 0 is returned for each bit.
Ch0_CMP2_LENDSTATUS	R	5	0	Indicates the status of the loop completion interrupt for CMP2 on channel 0.
Ch0_CMP2_CENDSTATUS	R	4	0	Indicates the status of the count completion interrupt for CMP2 on channel 0.
Ch0_CMP1_LENDSTATUS	R	3	0	Indicates the status of the loop completion interrupt for CMP1 on channel 0.
Ch0_CMP1_CENDSTAUS	R	2	0	Indicates the status of the count completion interrupt for CMP1 on channel 0.
Ch0_CMP0_LENDSTATUS	R	1	0	Indicates the status of the loop completion interrupt for CMP0 on channel 0.
Ch0_CMP0_CENDSTATUS	R	0	0	Indicates the status of the count completion interrupt for CMP0 on channel 0.

Remark 0: No interrupt request was issued.
1: An interrupt request was issued.

(2) PWM interrupt raw status register

This register (PWM_INTRAWSTATUS: E113_0404H) indicates the interrupt source, regardless of whether the interrupt source is enabled in PWM_INTENSET.

A pending interrupt source can be monitored by reading this register.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved		CH1_CMP2_LEND_RAWSTATUS	CH1_CMP2_CEND_RAWSTATUS	CH1_CMP1_LEND_RAWSTATUS	CH1_CMP1_CEND_RAWSTATUS	CH1_CMP0_LEND_RAWSTATUS	CH1_CMP0_CEND_RAWSTATUS

7	6	5	4	3	2	1	0
Reserved		CH0_CMP2_LEND_RAWSTATUS	CH0_CMP2_CEND_RAWSTATUS	CH0_CMP1_LEND_RAWSTATUS	CH0_CMP1_CEND_RAWSTATUS	CH0_CMP0_LEND_RAWSTATUS	CH0_CMP0_CEND_RAWSTATUS

(1/2)

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:14	0_0000H	Reserved. When these bits are read, 0 is returned for each bit.
CH1_CMP2_LEND_RAWSTATUS	R	13	0	Indicates the raw status of the loop completion interrupt for CMP2 on channel 1.
CH1_CMP2_CEND_RAWSTATUS	R	12	0	Indicates the raw status of the count completion interrupt for CMP2 on channel 1.
CH1_CMP1_LEND_RAWSTATUS	R	11	0	Indicates the raw status of the loop completion interrupt for CMP1 on channel 1.
CH1_CMP1_CEND_RAWSTATUS	R	10	0	Indicates the raw status of the count completion interrupt for CMP1 on channel 1.
CH1_CMP0_LEND_RAWSTATUS	R	9	0	Indicates the raw status of the loop completion interrupt for CMP0 on channel 1.
CH1_CMP0_CEND_RAWSTATUS	R	8	0	Indicates the raw status of the count completion interrupt for CMP0 on channel 1.
Reserved	R	7:6	0H	Reserved. When these bits are read, 0 is returned for each bit.
CH0_CMP2_LEND_RAWSTATUS	R	5	0	Indicates the raw status of the loop completion interrupt for CMP2 on channel 0.
CH0_CMP2_CEND_RAWSTATUS	R	4	0	Indicates the raw status of the count completion interrupt for CMP2 on channel 0.
CH0_CMP1_LEND_RAWSTATUS	R	3	0	Indicates the raw status of the loop completion interrupt for CMP1 on channel 0.
CH0_CMP1_CEND_RAWSTATUS	R	2	0	Indicates the raw status of the count completion interrupt for CMP1 on channel 0.

(2/2)

Name	R/W	Bit No.	After Reset	Function
CH0_CMP0_LEND_RAWSTATUS	R	1	0	Indicates the raw status of the loop completion interrupt for CMP0 on channel 0.
CH0_CMP0_CEND_RAWSTATUS	R	0	0	Indicates the raw status of the count completion interrupt for CMP0 on channel 0.

Caution If an interrupt source is set and cleared at the same time, setting takes precedence. However, if the setting interval for the same source is "PWM_PCLK cycle × 4 + PWM_PWCLKx cycle × 4" or shorter, the source may not be set after the source is cleared. In this case, the source is set at the next source setting timing.

Remark 0: No interrupt request was issued.
1: An interrupt request was issued.

(3) PWM interrupt enable set register

This register (PWM_INTENSET: E113_0408H) enables the interrupts. The register values are updated only for the bits to which 1 is set. The current enable/disable status can be checked by reading this register.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved		CH1_CMP2_LENDSET	CH1_CMP2_CENDSET	CH1_CMP1_LENDSET	CH1_CMP1_CENDSET	CH1_CMP0_LENDSET	CH1_CMP0_CENDSET

7	6	5	4	3	2	1	0
Reserved		CH0_CMP2_LENDSET	CH0_CMP2_CENDSET	CH0_CMP1_LENDSET	CH0_CMP1_CENDSET	CH0_CMP0_LENDSET	CH0_CMP0_CENDSET

(1/2)

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:14	0_0000H	Reserved. When these bits are read, 0 is returned for each bit.
CH1_CMP2_LENDSET	R/W	13	0	Controls whether to enable the loop completion interrupt for CMP2 on channel 1.
CH1_CMP2_CENDSET	R/W	12	0	Controls whether to enable the count completion interrupt for CMP2 on channel 1.
CH1_CMP1_LENDSET	R/W	11	0	Controls whether to enable the loop completion interrupt for CMP1 on channel 1.
CH1_CMP1_CENDSET	R/W	10	0	Controls whether to enable the count completion interrupt for CMP1 on channel 1.
CH1_CMP0_LENDSET	R/W	9	0	Controls whether to enable the loop completion interrupt for CMP0 on channel 1.
CH1_CMP0_CENDSET	R/W	8	0	Controls whether to enable the count completion interrupt for CMP0 on channel 1.
Reserved	R	7:6	0H	Reserved. When these bits are read, 0 is returned for each bit.
CH0_CMP2_LENDSET	R/W	5	0	Controls whether to enable the loop completion interrupt for CMP2 on channel 0.
CH0_CMP2_CENDSET	R/W	4	0	Controls whether to enable the count completion interrupt for CMP2 on channel 0.
CH0_CMP1_LENDSET	R/W	3	0	Controls whether to enable the loop completion interrupt for CMP1 on channel 0.
CH0_CMP1_CENDSET	R/W	2	0	Controls whether to enable the count completion interrupt for CMP1 on channel 0.
CH0_CMP0_LENDSET	R/W	1	0	Controls whether to enable the loop completion interrupt for CMP0 on channel 0.

(2/2)

Name	R/W	Bit No.	After Reset	Function
CH0_CMP0_CENDSET	R/W	0	0	Controls whether to enable the count completion interrupt for CMP0 on channel 0.

Remark When written: The interrupt enable bit is set or retained.
1: The interrupt enable bit is set.
0: The interrupt enable bit is retained.
When read: The status of the interrupt enable bit is indicated.
1: Interrupt request issuance is enabled.
0: Interrupt request issuance is disabled.

(4) PWM interrupt enable clear register

This register (PWM_INTENCLR: E113_040CH) clears the interrupt source enable bits. The register values are updated only for the bits to which 1 is set. 0 is returned when this register is read since it is write-only.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved		CH1_CMP2_LEND_ENCLR	CH1_CMP2_CEND_ENCLR	CH1_CMP1_LEND_ENCLR	CH1_CMP1_CEND_ENCLR	CH1_CMP0_LEND_ENCLR	CH1_CMP0_CEND_ENCLR

7	6	5	4	3	2	1	0
Reserved		CH0_CMP2_LEND_ENCLR	CH0_CMP2_CEND_ENCLR	CH0_CMP1_LEND_ENCLR	CH0_CMP1_CEND_ENCLR	CH0_CMP0_LEND_ENCLR	CH0_CMP0_CEND_ENCLR

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:14	0_0000H	Reserved. When these bits are read, 0 is returned for each bit.
CH1_CMP2_LEND_ENCLR	W	13	0	Clears the loop completion interrupt enable bit for CMP2 on channel 1.
CH1_CMP2_CEND_ENCLR	W	12	0	Clears the count completion interrupt enable bit for CMP2 on channel 1.
CH1_CMP1_LEND_ENCLR	W	11	0	Clears the loop completion interrupt enable bit for CMP1 on channel 1.
CH1_CMP1_CEND_ENCLR	W	10	0	Clears the count completion interrupt enable bit for CMP1 on channel 1.
CH1_CMP0_LEND_ENCLR	W	9	0	Clears the loop completion interrupt enable bit for CMP0 on channel 1.
CH1_CMP0_CEND_ENCLR	W	8	0	Clears the count completion interrupt enable bit for CMP0 on channel 1.
Reserved	R	7:6	0H	Reserved. When these bits are read, 0 is returned for each bit.
CH0_CMP2_LEND_ENCLR	W	5	0	Clears the loop completion interrupt enable bit for CMP2 on channel 0.
CH0_CMP2_CEND_ENCLR	W	4	0	Clears the count completion interrupt enable bit for CMP2 on channel 0.
CH0_CMP1_LEND_ENCLR	W	3	0	Clears the loop completion interrupt enable bit for CMP1 on channel 0.
CH0_CMP1_CEND_ENCLR	W	2	0	Clears the count completion interrupt enable bit for CMP1 on channel 0.
CH0_CMP0_LEND_ENCLR	W	1	0	Clears the loop completion interrupt enable bit for CMP0 on channel 0.
CH0_CMP0_CEND_ENCLR	W	0	0	Clears the count completion interrupt enable bit for CMP0 on channel 0.

Remark 1: The interrupt enable bit is cleared (interrupt masked).
0: The interrupt enable bit is retained.

(5) PWM interrupt source clear register

This register (PWM_INTFFCLR: E113_0410H) clears the generated interrupt sources. The register values are updated only for the bits to which 1 is set. 0 is returned when this register is read since it is write-only.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved		CH1_CMP2_LEND_FFCLR	CH1_CMP2_CEND_FFCLR	CH1_CMP1_LEND_FFCLR	CH1_CMP1_CEND_FFCLR	CH1_CMP0_LEND_FFCLR	CH1_CMP0_CEND_FFCLR

7	6	5	4	3	2	1	0
Reserved		CH0_CMP2_LEND_FFCLR	CH0_CMP2_CEND_FFCLR	CH0_CMP1_LEND_FFCLR	CH0_CMP1_CEND_FFCLR	CH0_CMP0_LEND_FFCLR	CH0_CMP0_CEND_FFCLR

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:14	0_0000H	Reserved. When these bits are read, 0 is returned for each bit.
CH1_CMP2_LEND_FFCLR	W	13	0	Clears the loop completion interrupt source bit for CMP2 on channel 1.
CH1_CMP2_CEND_FFCLR	W	12	0	Clears the count completion interrupt source bit for CMP2 on channel 1.
CH1_CMP1_LEND_FFCLR	W	11	0	Clears the loop completion interrupt source bit for CMP1 on channel 1.
CH1_CMP1_CEND_FFCLR	W	10	0	Clears the count completion interrupt source bit for CMP1 on channel 1.
CH1_CMP0_LEND_FFCLR	W	9	0	Clears the loop completion interrupt source bit for CMP0 on channel 1.
CH1_CMP0_CEND_FFCLR	W	8	0	Clears the count completion interrupt source bit for CMP0 on channel 1.
Reserved	R	7:6	0H	Reserved. When these bits are read, 0 is returned for each bit.
CH0_CMP2_LEND_FFCLR	W	5	0	Clears the loop completion interrupt source bit for CMP2 on channel 0.
CH0_CMP2_CEND_FFCLR	W	4	0	Clears the count completion interrupt source bit for CMP2 on channel 0.
CH0_CMP1_LEND_FFCLR	W	3	0	Clears the loop completion interrupt source bit for CMP1 on channel 0.
CH0_CMP1_CEND_FFCLR	W	2	0	Clears the count completion interrupt source bit for CMP1 on channel 0.
CH0_CMP0_LEND_FFCLR	W	1	0	Clears the loop completion interrupt source bit for CMP0 on channel 0.
CH0_CMP0_CEND_FFCLR	W	0	0	Clears the count completion interrupt source bit for CMP0 on channel 0.

Remark 1: The interrupt source is cleared.
0: The interrupt source is retained.

4. Description of Functions

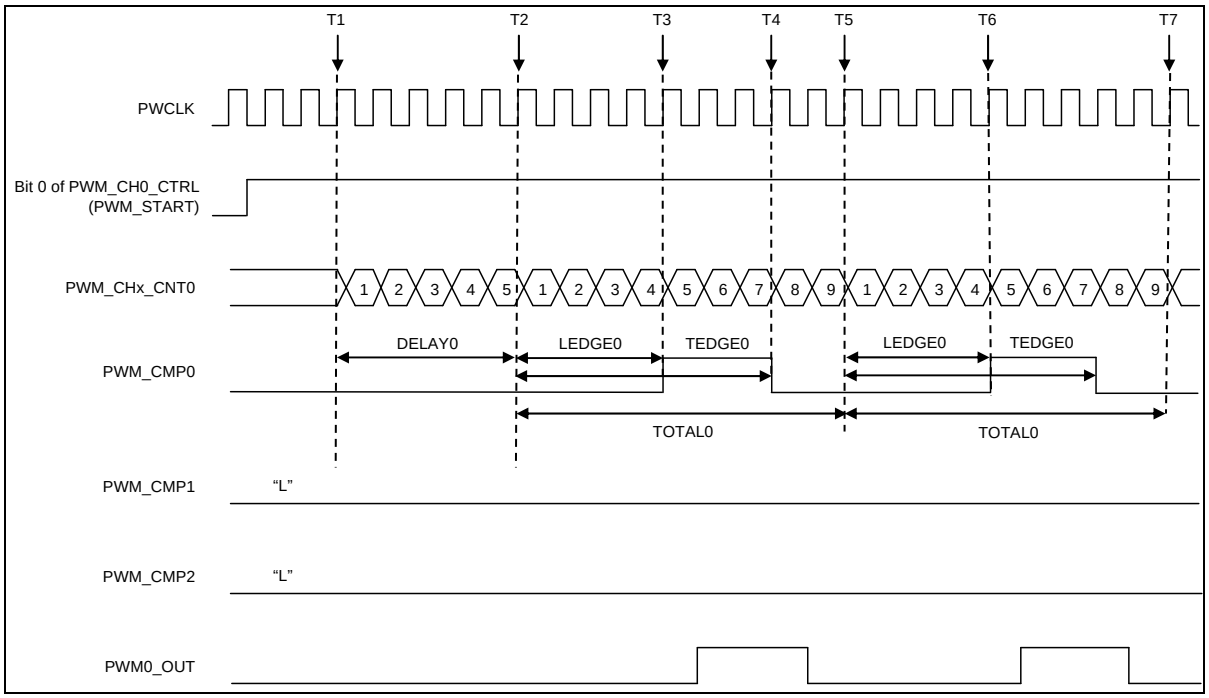
4.1 PWM Operation

4.1.1 When one counter is started

The following shows an example of when only counter 0 of channel 0 (counter 0; PWM_CH0_CNT0) is started.

- PWM_CH0_TOTAL0 = 0000_0009H: Total cycle: PWM_PWCLK × 9 cycles
- PWM_CH0_DELAY0 = 0000_0005H: Delay value: PWM_PWCLK × 5 cycles
- PWM_CH0_LEDGE0 = 0000_0004H: Leading edge setting: 4 cycles
- PWM_CH0_TEDGE0 = 0000_0007H: Trailing edge setting: 7 cycles
- PWM_CH0_MODE = 0000_0001H: Automatic stop disabled (repeat mode set) and inversion of PWM_CMP0 not specified

Figure 4-1. Timing When Only Counter 0 Runs



<1> Counter 0 starts at the rising edge of PWCLK three cycles after the CMP_EN0 bit of the PWM_CH0_MODE register is set to 1 and the PWM_START bit of the PWM_CTRL register is set to 1.

<2> If a delay value is set in the PWM_CH0_DELAY0 register, counter 0 continues counting up to that value. The output from PWM_CMP0 remains low level.

<3> When the counter value matches the value of PWM_CH0_DELAY0, counter 0 is set to 1 in the next cycle (T2 timing).

<4> Counter 0 starts counting at T2 again. When the counter value matches the PWM_CH0_LEDGE0 value, PWM_CMP0 outputs a high level at the next cycle.

<5> In the next cycle after the value of counter 0 matches TEDGE0 (T4 timing), the PWM_CMP0 output becomes low level. PWM_CMP0 continues outputting a low level until the values of TOTAL0 and counter 0 match.

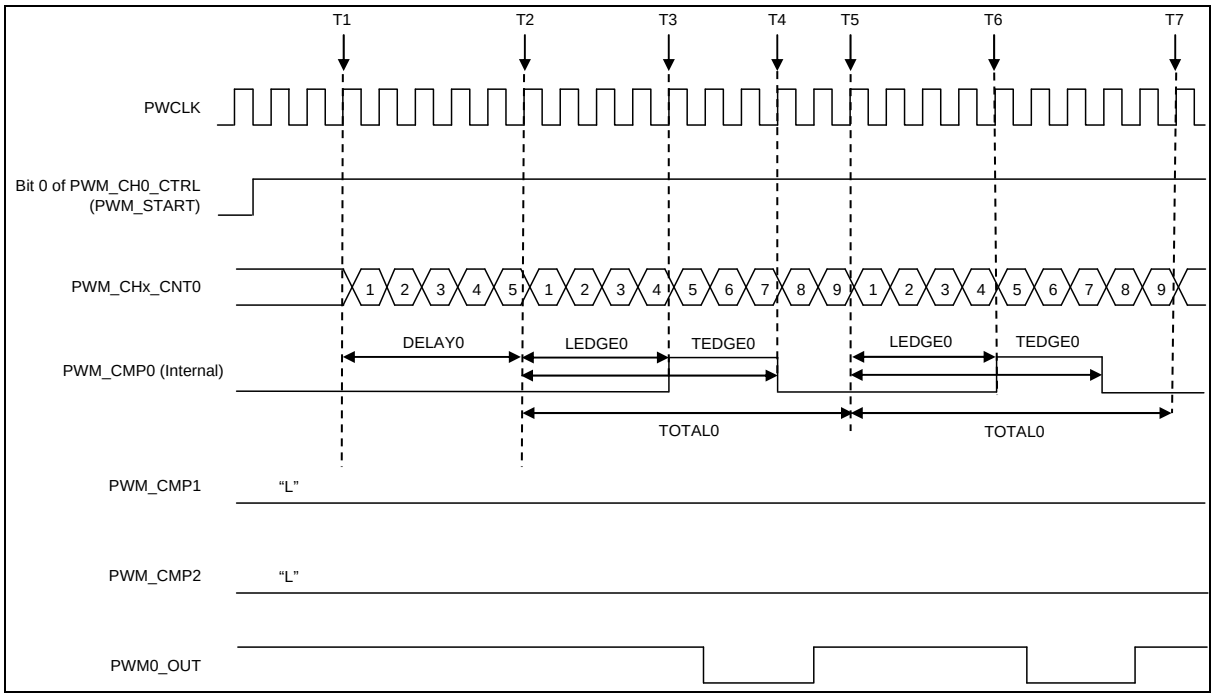
<6>If the values of counter 0 and TOTAL0 match, counter 0 is set to 1 in the next cycle (T5 timing).

<7> After the T5 timing, the operation of T2 to T5 is repeated.

4.1.2 When one counter is started and output is inverted at PWM_CNT0

- PWM_CH0_TOTAL0 = 0000_0009H: Total cycle: PWM_PWCLK × 9 cycles
- PWM_CH0_DELAY0 = 0000_0005H: Delay value: PWM_PWCLK × 5 cycles
- PWM_CH0_LEDGE0 = 0000_0004H: Leading edge setting: 4 cycles
- PWM_CH0_TEDGE0 = 0000_0007H: Trailing edge setting: 7 cycles
- PWM_CH0_MODE = 0000_0005H: Automatic stop disabled (repeat mode set) and inversion of PWM_CMP0 specified

Figure 4-2. Only Counter 0 Runs and PWM_CMP0 Value Is Inverted



The waveform generated in CMP0 (CMP0 internal waveform) is inverted when PWM_CMP0 is output if inversion is specified.

4.1.3 When looping is enabled

The following describes the operation when looping is specified for counter 0 of channel 0.
If looping is specified, counter 0 automatically stops after loop repeats the specified number of times.
This example applies when counter 0 of channel 0 is set as follows.

- PWM_CH0_TOTAL0 = 0000_0009H
- PWM_CH0_DELAY0 = 0000_0006H
- PWM_CH0_LEDGE0 = 0000_0004H
- PWM_CH0_TEDGE0 = 0000_0007H
- PWM_CH0_MODE = 0000_0003H: Automatic stop enabled and counter 0 enabled

Figure 4-3. Start Operation When Looping Is Enabled

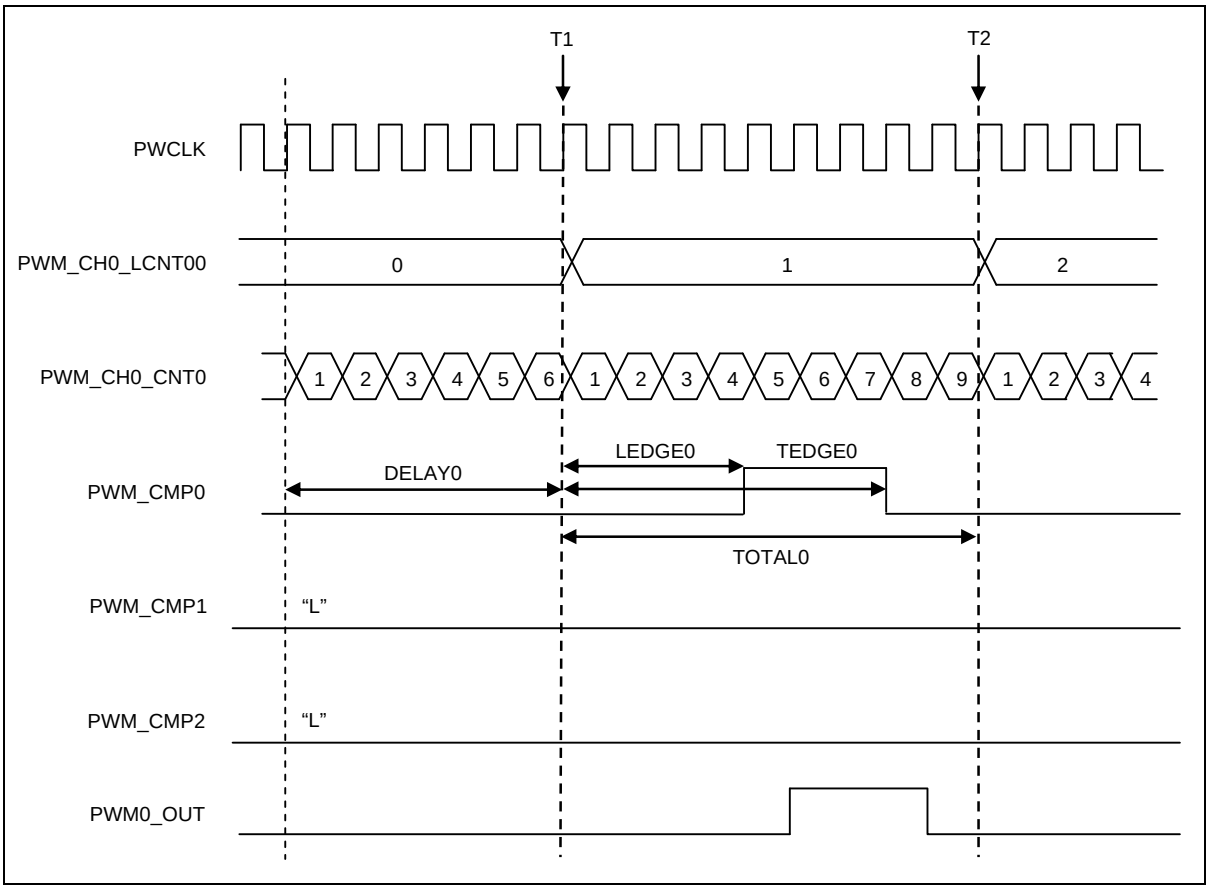
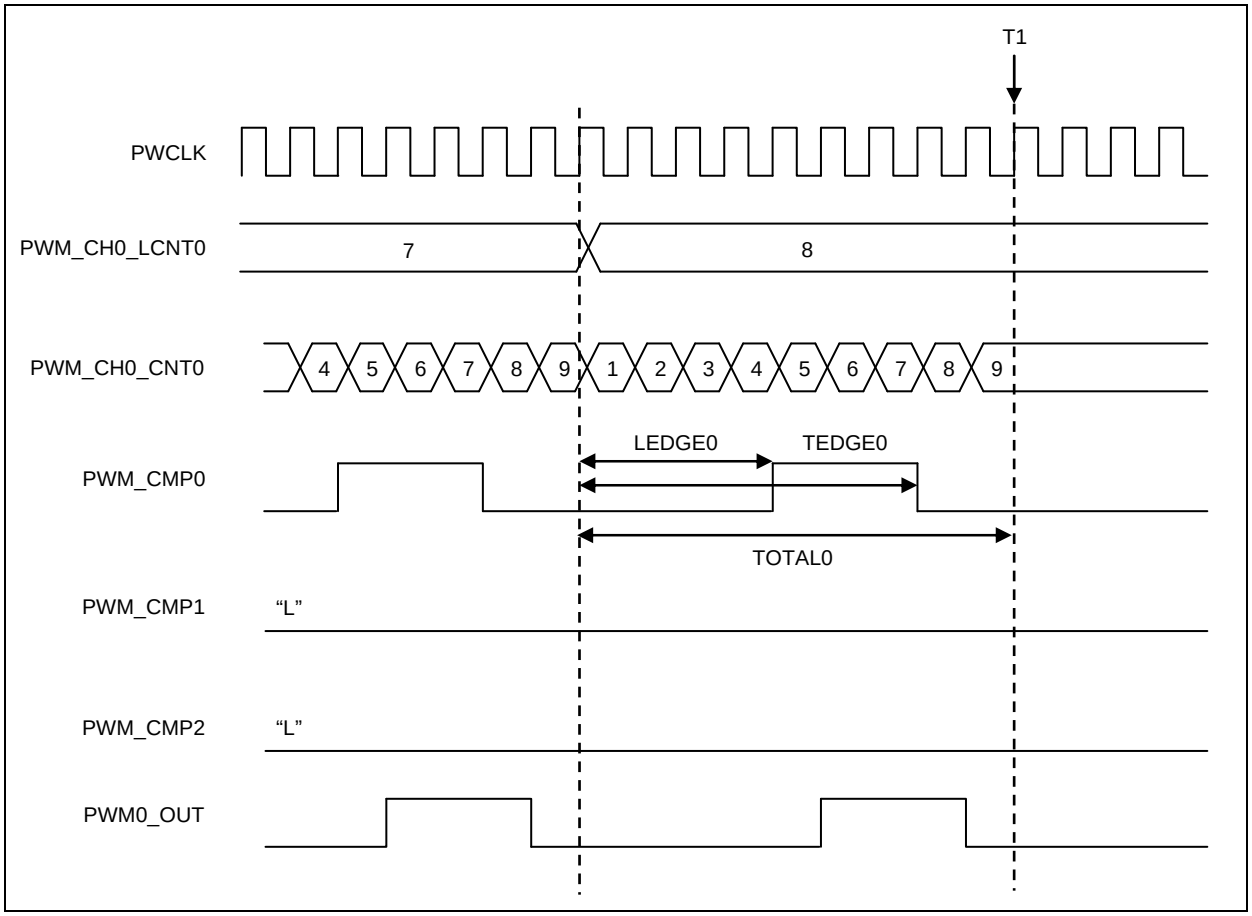


Figure 4-4. Termination Operation When Looping Is Enabled



PWM_CH0_CNT0 and PWM_CH0_LCNT0 stop at the next cycle after loop counter 0 matches the specified value. The PWM0_OUT output remains low level.

4.1.4 When three counters are started (AND specified)

The following shows an example when counters 0 to 2 are set and started as follows.

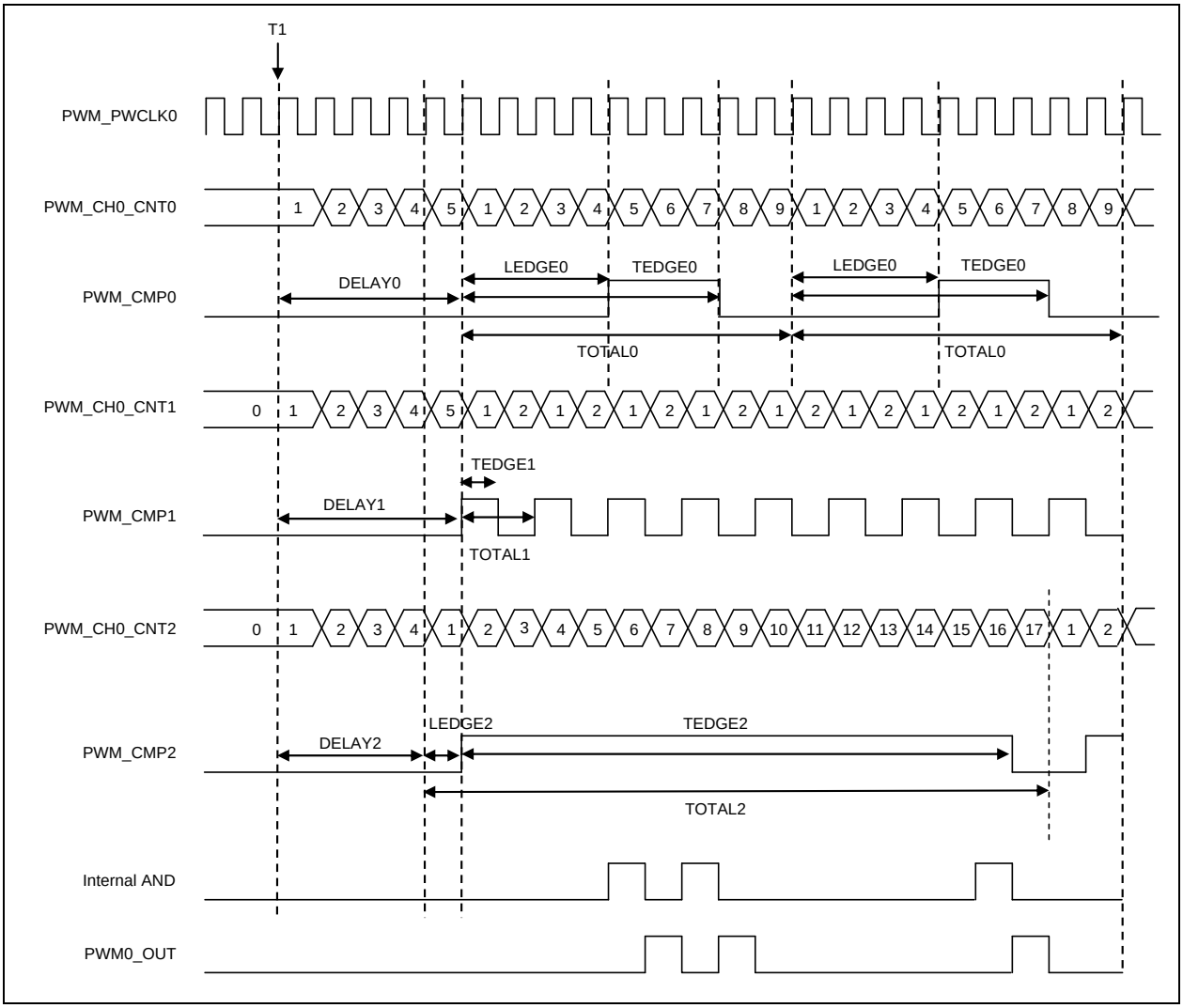
- PWM_CH0_TOTAL0 = 0000_0009H: Counter 0 total cycle: PWM_PWCLK × 9 cycles
- PWM_CH0_DELAY0 = 0000_0005H: Counter 0 delay value: PWM_PWCLK × 5 cycles
- PWM_CH0_LEDGE0 = 0000_0004H: Counter 0 leading edge setting: 4 cycles
- PWM_CH0_TEDGE0 = 0000_0003H: Counter 0 trailing edge setting: 3 cycles

- PWM_CH0_TOTAL1 = 0000_0002H: Counter 1 total cycle: PWM_PWCLK × 2 cycles
- PWM_CH0_DELAY1 = 0000_0005H: Counter 1 delay value: PWM_PWCLK × 5 cycles
- PWM_CH0_LEDGE1 = 0000_0000H: Counter 1 leading edge setting: 0 cycles
- PWM_CH0_TEDGE1 = 0000_0001H: Counter 1 trailing edge setting: 1 cycle

- PWM_CH0_TOTAL2 = 0000_0011H: Counter 2 total cycle: PWM_PWCLK × 17 cycles
- PWM_CH0_DELAY2 = 0000_0004H: Counter 2 delay value: PWM_PWCLK × 4 cycles
- PWM_CH0_LEDGE2 = 0000_0001H: Counter 2 leading edge setting: 1 cycle
- PWM_CH0_TEDGE2 = 0000_0010H: Counter 2 trailing edge setting: 16 cycles

- PWM_CH0_MODE = 0001_0111H: The operation of CMP_EN0 to CMP_EN2 is enabled.
  The output of CMP0 to CMP2 is not inverted.
  Automatic stop is not enabled.
  ANDing of each counter output is specified by the MOD bit.

Figure 4-5. Operation of Counters 0 to 2: With AND Specified



The values generated by PWM_CMP0 to PWM_CMP2 are internally ANDed and output from PWM0_OUT.

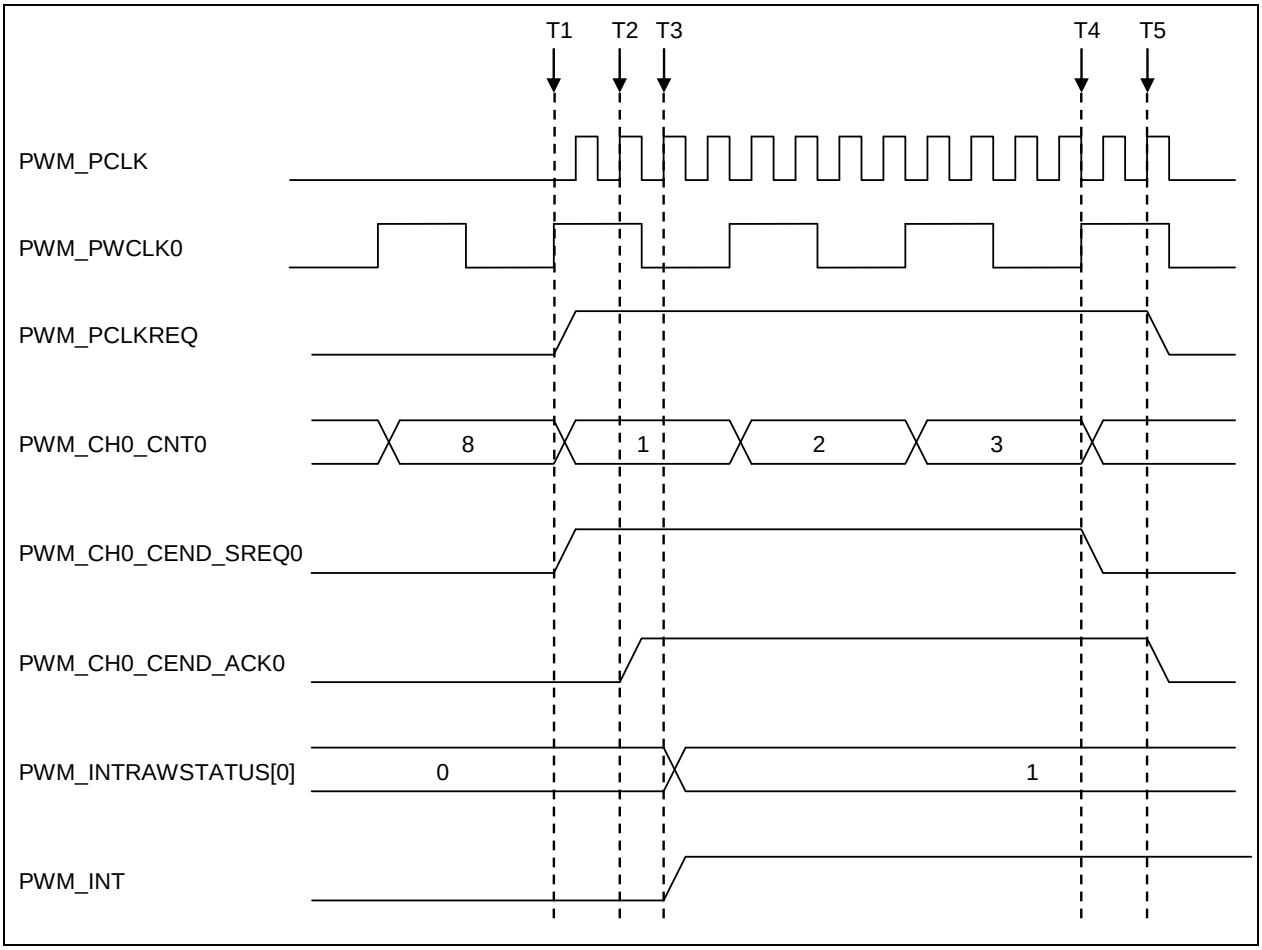
4.2 Interrupt Timing

There are interrupts for each counter in the PWM interface and an interrupt source is generated when the counter reaches the total cycle value. An interrupt source is also generated when the loop count terminates.
When an enabled interrupt source is generated, the source is set to PWM_INTSTATUS and the ORed interrupt signal is output. The interrupt source is cleared by using the PWM_INTFFCLR register.

An example is shown below.

- Only CMP0 of channel 0 operates
- Interrupt output of CMP0 of channel 0 is enabled by setting INT_ENSET to 0000_0001H
- PWM_CH0_TOTAL0 = 8

Figure 4-6. Interrupt Timing (Clock Control)



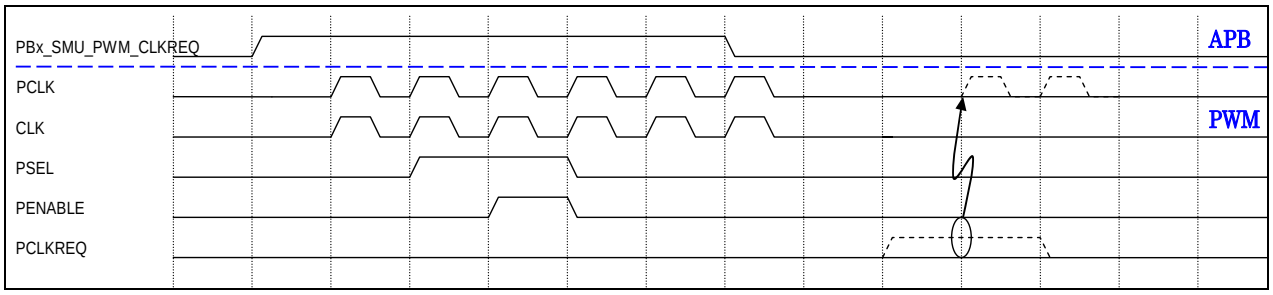
If the value of counter 0 matches the specified value (T1 in Figure 4-6), the internal signal becomes active in the second PWM_PCLK cycle (T2 in Figure 4-6) and the interrupt source is reflected in the PWM_INTRAWSTATUS register in the next PWM_PCLK cycle (T3 in Figure 4-6). If an interrupt source is enabled, the interrupt output signal PWM_INT also becomes active.
The internal signal becomes inactive in the third PWM_PWCLK cycle or later after T3 (T4 in Figure 4-6) and in the second PWM_PCLK cycle after that (T5 in Figure 4-6).

4.3 Clock/Reset

4.3.1 Clock

While REQ signal and ACK signal are an activist, a PWM clock request signal also makes PCLKREQ active, and controls so that PWM_PCLK may be supplied.
An example of timing of clock supply of APB is indicated in the following figure.

Figure 4-7. PCLKREQ



4.3.2 Reset

An asynchronous reset signal of PWM will be 2CLK need until a reset of PWM is released after an asynchronous clock is released.

5. Usage

5.1 Procedure for Generating Waveform in PWM Interface

5.1.1 Procedure of setting

A procedure of basic setting of PWM is below. Something of the same number is inconsecutive by order.

Table 5-1. Procedure of setting

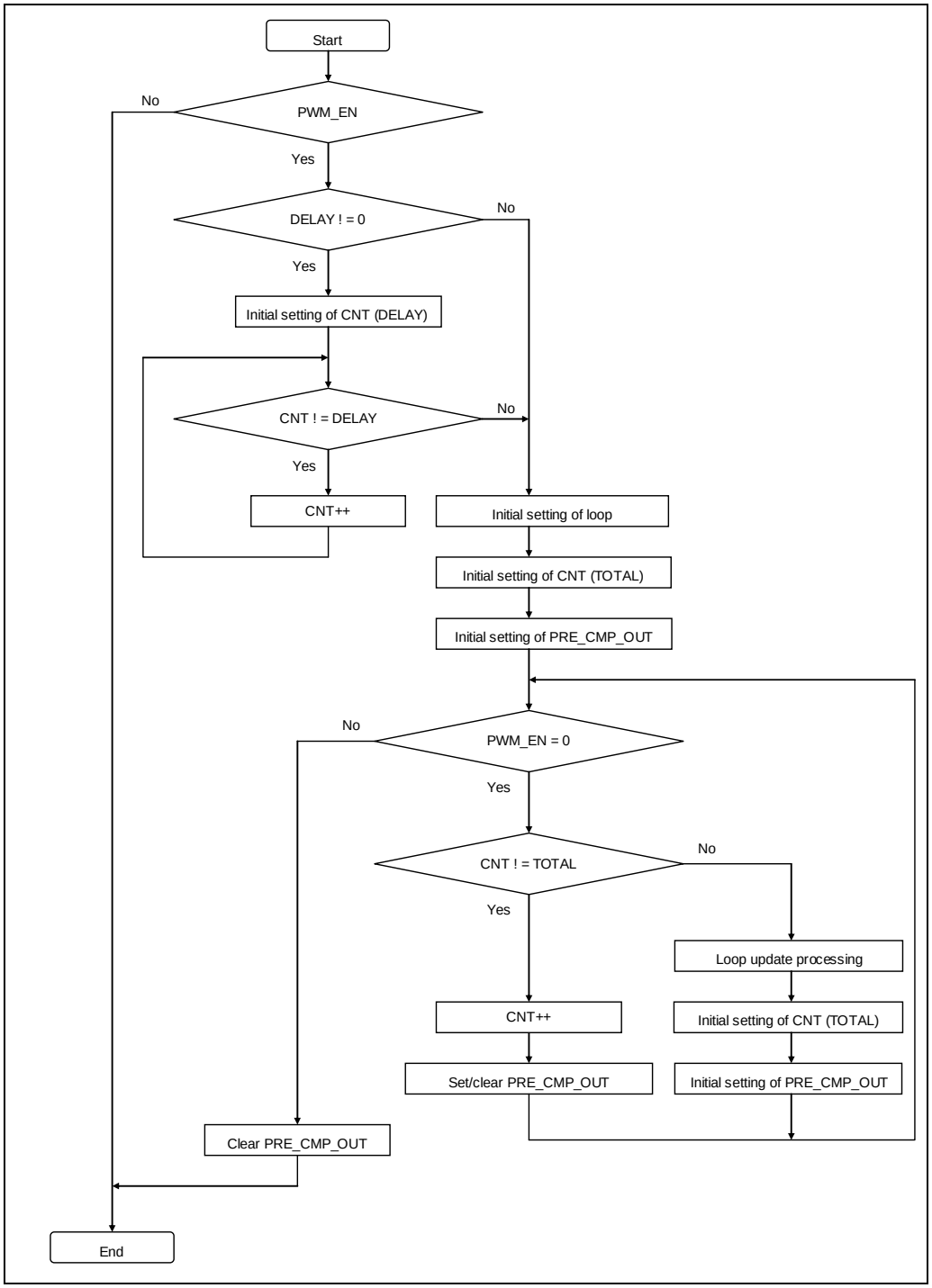
Order of the setting	Register	contents
1	PWM_CHx_DELAYn	Delay value setting
1	PWM_CHx_TOTALn	General cycle setting
1	PWM_CHx_LEDGEn	Leading edge setting
1	PWM_CHx_TEDGEn	Trading edge setting
1	PWM_CHx_LOOPn	Loop count setting (Only when the loop count of times is designated.)
1	PWM_INTENSET	Interrupt enable setting
1	PWM_CHx_MODE	Mode setting
4	PWM_CTRL	PWM_START is set as counter operation starting.

Caution Setting this register is prohibited while the counter is running. The operation is not guaranteed if this register is set when the PWM_START bit of the PWM_Chx_CTRL register is set to 1.

5.1.2 Processing flow

The following figure shows the processing flow of PWM_CHx_CMPn waveform generation.

Figure 5-1. Waveform Generation Flow



5.2 Cautions and Restrictions

<1> The PWM interface uses only rising edges. It does not use falling edges.

<2> PWM_PCLK is not synchronized with PWM_PWCLK0 or PWM_PWCLK1.

<3> The PWM interface is initialized by PWM_RSTZ. Since PWM_RSTZ is synchronized with the system clock, the APB interface is synchronously reset and PWM channels 0 and 1 are asynchronously reset.

<4> Though one channel has three counters, starting these counters separately (for example, starting counter 1 after starting counter 0) is prohibited. If they are started separately, the phase between the counters cannot be guaranteed. Change the settings after making PWM_START inactive.

<5> Due to the PWM interface circuit configuration, the following restrictions apply to the settings of PWM_CHx_LEDGEn (leading edge), PWM_Chx_TEDGEn (trailing edge), and PWM_CHx_TOTALn (total).

- Keep the following relationship for the setting values: LEDGE < TEDGE ≤ TOTAL
- Setting PWM_CHx_TOTALn to 0000_0000H is prohibited.
- The counter remains at 1 if PWM_CHx_TOTALn is set to 0000_0001H.
- No LEDGE period is given if PWM_CHx_LEDGEn is set to 0000_0000H.
- Setting PWM_CHx_TEDGEn to 0000_0000H is prohibited.

<6> If the setting interval for the same source is “PWM_PCLK cycle × 4 + PWM_PWCLKx cycle × 4” or shorter, the source may not be set correctly after the source is cleared. In this case, the source is set at the next source setting timing.

<7> When restarting a counter, set the PWM_START bit to 0 and wait for at least three PWM_PWCLKx cycles.

Remark x = 0 or 1
n = 0 to 2

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		Page	Summary
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2.00	Jun 7, 2010	—	Incremental update from comments to the 1.0.
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