User's Manual

IIC Interface

User's Manual

Multimedia Processor for Mobile Applications
EMMA Mobile ™ EV2

Renesas Electronics
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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the EMMA Mobile EV2. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Data Sheet	Hardware overview and electrical characteristics	EMMA Mobile EV2 Datasheet	R19DS0010EJxxxx
User's manual (1chip)	Hardware whole specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description	EMMA Mobile EV2 User's manual 1chip	R19UH0036EJxxxx
User's manual (module)	Hardware each macro specifications and operation description.	EMMA Mobile EV2 User's manual each module	See below

Document Name	Document No.	Document Name	Document No.
1chip	R19UH0036EJxxxx	DMA Controller	R19UH0043EJxxxx
System Management Unit	R19UH0037EJxxxx	LP-DDR/DDR2 Controller	R19UH0039EJxxxx
Timer	R19UH0054EJxxxx	SD Memory Card Interface	R19UH0061EJxxxx
System Timer	R19UH0055EJxxxx	SDIO Interface	R19UH0042EJxxxx
HD Video Decoder	R19UH0056EJxxxx	CF Card Interface	R19UH0062EJxxxx
Rotator	R19UH0057EJxxxx	Unified Serial Interface	R19UH0047EJxxxx
Resizer	R19UH0058EJxxxx	UART interface	R19UH0040EJxxxx
Image Composer	R19UH0038EJxxxx	USB 2.0 Host Controller	R19UH0045EJxxxx
LCD Interface	R19UH0044EJxxxx	USB 2.0 Function Controller	R19UH0034EJxxxx
ITU-R BT.656 Interface	R19UH0059EJxxxx	IIC Interface (This manual)	R19UH0052EJxxxx
Digital Terrestrial TV Interface	R19UH0048EJxxxx	General Purpose I/O Interface	R19UH0041EJxxxx
Camera Interface	R19UH0060EJxxxx	Pulse Width Modulation Interface	R19UH0063EJxxxx

4 digits of end shows the version.

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names

Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.

Examples the PM03 bit in the PM0 register

P3_5 pin, VCC pin

(2) Notation of Numbers

The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.

Examples Binary: 11b or 11

Hexadecimal: EFA0h

Decimal: 1234

3. Register Notation

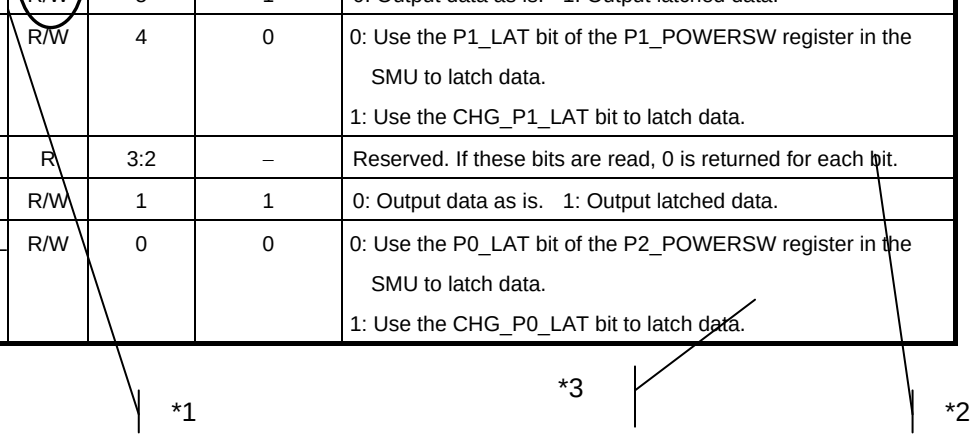
The symbols and terms used in register diagrams are described below.

x.x.x XXX register

This register (XXXXXXX: xxxx_xxxxh) …..

7	6	5	4	3	2	1	0
Reserved		CHG_P1_LAT	LATCH_P1_SEL	Reserved		CHG_P0_LAT	CHG_P0_LAT_SEL

Name	R/W	Bit No.	After Reset	Description
LATCH_P2_SEL	R/W	8	0	0: Use the P2_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P2_LAT bit to latch data.
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P1_LAT	R/W	5	1	0: Output data as is. 1: Output latched data.
LATCH_P1_SEL	R/W	4	0	0: Use the P1_LAT bit of the P1_POWERSW register in the SMU to latch data. 1: Use the CHG_P1_LAT bit to latch data.
Reserved	R	3:2	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P0_LAT	R/W	1	1	0: Output data as is. 1: Output latched data.
CHG_P0_LAT_SEL	R/W	0	0	0: Use the P0_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P0_LAT bit to latch data.



*1

R/W: Read and Write.

R: Read only.

W: Write only.

-: Nothing is assigned.

*2

Reserved bit.

Reserved bit. Set to specified value.

*3

・ Nothing is assigned.

Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.

・ Do not set to a value.

Operation is not guaranteed when a value is set.

・ Function varies according to the operating mode.

The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Register
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

Table of Contents

1. Overview

1.1 Features

The main features of the I^2C interface are as follows.

- Two channels: IIC0 and IIC1

- Conformance to the I^2C bus format (1995 updated version of Philips specification)
  Data length: 8 bits (data 8bit + ACK 1bit.) The standard mode (transfer rate: 97 kbps maximum) and fast mode (transfer rate: 383 kbps maximum) are supported.

- Automatic serial data identification
  A start condition, , and stop condition on the serial data bus are automatically detected.

- Address-based chip selection

- Wake-up operation

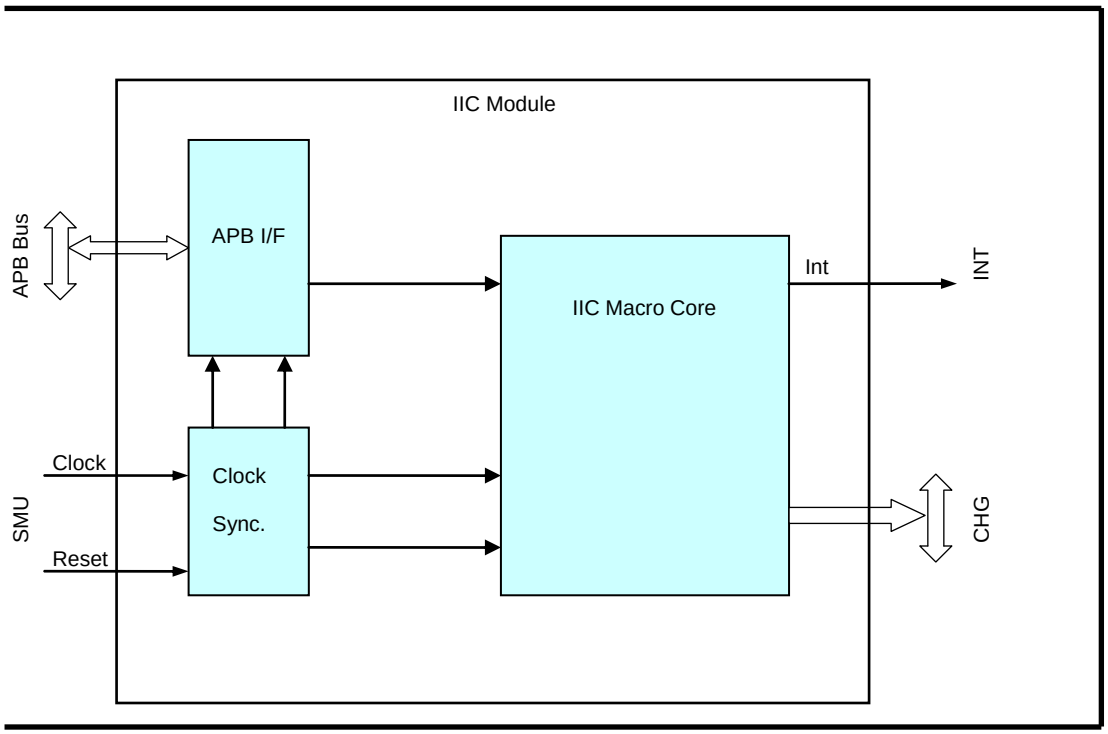
- Acknowledge (ACK) transmission
  The ACK signal is sent to confirm that serial communication has been executed normally.

- Wait (WAIT) notification
  A wait signal is sent to report that the device is waiting.

- Arbitration notification
  When more than one master device generated the start condition "at the same time ", the control which does level comparison of a serial data bus (SDA) terminal after zero in of serial clock (SCL) and chooses a master device can be performed.

1.2 Function Block Diagram

Figure 1-1. Function Block Diagram



1.3 Limitation

○About the input clock frequency to this macro.

Transfer clock of IIC is chosen at IICx transfer clock choice register (IIC_IICCLx). Refer to the explanation of a IIC transfer clock choice register for details about clock choice. Be sure to input a clock to PCLK and IIC_SCLK in the reach of following frequency.

PCLK frequency must be higher than 18.4MHz.

IIC_SCLK frequency range 2MHz to 9.2MHz.

○About a reset of this macro.

A reset of this macro is released behind 2 clocks of IIC_SCLK after release of PRESETZ.

○About supply of a clock.

Always supply IIC_CLK and IIC_SCLK to this macro while using this macro.

2. Pin functions

Pin Name	I/O	Function	Alternate Pin Function
IIC0_SCL	I/O	Serial clock input	GPIO_044
IIC0_SDA	I/O	Serial data input	GPIO_045
IIC1_SCL	I/O	Serial clock input	UART3_RX, GPIO_046
IIC1_SDA	I/O	Serial data input	UART3_TX, GPIO_047

3. Registers

3.1 Register List

The I^2C interface registers allow 32bit access only. (Access of 16bit and 8bit is also processed as 32bit access.)
Do not access reserved registers.
Do not write any value other than 0 to reserved bits in each register.

Base address: E007_0000H (IIC0)

Address	Register Name	Symbol	R/W	After Reset
0000H	IIC0 enable operation register	IIC_IICACT0	R/W	0000_0000H
0004H	IIC0 shift register	IIC_IIC0	R/W	0000_0000H
0008H	IIC0 control register	IIC_IICC0	R/W	0000_0000H
000CH	Slave address register	IIC_SVA0	R/W	0000_0000H
0010H	IIC0 transfer clock selection register	IIC_IICCL0	R/W	0000_0004H
0014H	IIC0 function extension register	IIC_IICX0	R/W	0000_0000H
0018H	IIC0 state register	IIC_IICS0	R	0000_0000H
001CH	IIC0 state register (Read-only register for emulation)	IIC_IICSE0	R	0000_0000H
0020H	IIC0 flag register	IIC_IICF0	R/W	0000_0000H
0024H-0028H	Reserved	–	–	–

Base address: E10A_0000H (IIC1)

Address	Register Name	Symbol	R/W	After Reset
0000H	IIC1 enable operation register	IIC_IICACT1	R/W	0000_0000H
0004H	IIC1 shift register	IIC_IIC1	R/W	0000_0000H
0008H	IIC1 control register	IIC_IICC1	R/W	0000_0000H
000CH	Slave address register	IIC_SVA1	R/W	0000_0000H
0010H	IIC1 clock selection register	IIC_IICCL1	R/W	0000_0004H
0014H	IIC1 function extension register	IIC_IICX1	R/W	0000_0000H
0018H	IIC1 state register	IIC_IICS1	R	0000_0000H
001CH	IIC1 state register (Read-only register for emulation)	IIC_IICSE1	R	0000_0000H
0020H	IIC1 flag register	IIC_IICF1	R/W	0000_0000H
0024H-0028H	Reserved	–	–	–

3.2 Register Details (x: 0 or 1)

3.2.1 IICx enable operation register

This register (IIC_IICACTx: E007_0000H (IIC0), E10A_0000H (IIC1)) specifies the settings for I^2C operations such as enabling/disabling. Other register setting is done after it's confirmed that it's the value designated certainly when setting this register. When making this bit 0, after confirming that macro operation has ended completely. For example when writing 0 in this bit by the following cycle written in the STP bit of IICC0, the stop condition isn't sometimes issued.

7	6	5	4	3	2	1	0
Reserved							IICE0

Name	R/W	Bit No.	After Reset	Function
Reserved	R	7:1	00H	Reserved.
IICE0	R/W	0	0	IIC enable operation bit 0: State register is reset and the inner operation is also suspended. 1: Enabled The data written in won't be reflected by the difference in the frequency bands of sampling clock inside PCLK and IIC immediately as reading data of this register.

3.2.2 IICx shift register

This register (IIC_IICx: E007_0004H (IIC0), E10A_0004H (IIC1)) is used to perform serial transmission/reception (shift operation) in synchronization with the serial clock. Data is transferred, starting with the most significant bit (MSB).
Operation is not guaranteed if this register is accessed during data transfer.
The writing in when being IICE=0, is invalid.
If this register is written to during a wait period, the wait state is canceled and data transfer starts.

7	6	5	4	3	2	1	0
Transmit/receive data							

Name	R/W	Bit No.	After Reset	Function
Transmit/receive data	R/W	7:0	00H	Transmit/receive data is read/written.

3.2.3 IICx control register

This register (IIC_IICCx: E007_0008H (IIC0), E10A_0008H (IIC1)) specifies the settings for I^2C interface operations such as enabling/disabling the I^2C interface and specifying the wait timing.

7	6	5	4	3	2	1	0
Reserved	LREL0	WREL0	SPIE0	WTIM0	ACKE0	STT0	SPT0

(1/2)

Name	R/W	Bit No.	After Reset	Function
Reserved	R	7	0	Reserved
LREL0	R/W	6	0	Ends the communication state and sets the wait state. This bit is used, for example, when an extension code irrelevant to this device is received. When this bit is set to 1, the SCL/SDA line is placed in the Hi-Z state, and the STT0 and SPT0 bits of this register and the MSTS0, EXC0, COI0, TRC0, ACKD0, and STD0 bits of the IIC_IICSEx register are cleared. After this bit is set to 1, it is automatically reset to 0 (one-shot operation). When this bit is read, 0 is returned. 0: Normal operation 1: When communication ends, the operation enters the wait state.
WREL0	R/W	5	0	Cancels the wait state. After this bit is set to 1, it is automatically reset to 0 (one-shot operation). If the wait state is canceled by setting the WREL0 bit when the wait period is set to 9th clocks and when the TRC0 bit of the IIC_IICSEx register is set to 1, the TRC0 bit is cleared to release the SDA line (Hi-Z). When this bit is read, 0 is returned. 0: The wait state is preserved. 1: The wait state is canceled.
SPIE0	R/W	4	0	Enables/disables a stop condition interrupt. 0: Disables issuance of stop condition interrupt requests. 1: Enables issuance of stop condition interrupt requests.
WTIM0 Note1	R/W	3	0	Specifies the timing of interrupt request generation. In master operation, the clock output is pulled low to wait after the specified number of clock cycles are output. In slave operation, the clock output is pulled low to make the master wait when the specified number of clock cycles are input. 0: Interrupt is generated at the 8th falling edge of the clock. 1: Interrupt is generated at the 9th falling edge of the clock.

(2/2)

Name	R/W	Bit No.	After Reset	Function
ACKE0 Note2	R/W	2	0	Controls the acknowledge signal (ACK). "1" is set in this bit because it's receive-enable state when the TRC bit of the IIC register is "0". When not needing the next data, "0" is set in this bit. 0: Disables ACK. 1: Enables ACK. (Sets the SDA line to low during the 9th clock cycle.)
STT0 Note3	R/W	1	0	Issues a start condition. The operation differs depending on what the state was before this bit was set. When this bit is read, 0 is returned. 0: No operation is performed. 1: A start condition is issued. Remark This bit is automatically cleared when any of the following conditions occurs: • When a start condition is detected by the master • When a master loses arbitration • When the LREL0 bit is set to 1 • When the IICE0 bit is set to 0 • When a reset is input
SPT0	R/W	0	0	Issues a stop condition (ends transfer operation as the master). When this bit is set, the SDA line is pulled low, then the SCL line is pulled high or the system waits for the SCL line to be pulled high. Next, a specified time is secured and then the SDA line is pulled high to issue a stop condition. By setting this bit in the wait state, the wait state can be canceled to issue a stop condition. When this bit is read, 0 is returned. 0: No operation is performed. 1: A stop condition is issued. Remark This bit is automatically cleared when any of the following conditions occurs: • When a stop condition is detected • When a master loses arbitration • When the LREL0 bit is set to 1 • When the IICE0 bit is set to 0 • When a reset is input

Notes1. During address transfer, the following operations are performed:

- On the master side, a wait or interrupt request is issued at the 9th falling edge of the clock, regardless of the value of the WTIM0 bit.
- When the address being transferred matches an address input on the slave side (COI0 = 1), a wait or

interrupt request is issued at the 9th falling edge of the clock, regardless of the value of the WTIM0 bit.

- When an extension code is received (EXC0 = 1) on the slave side, a wait or interrupt request is issued at the 8th falling edge of the clock, regardless of the value of the WTIM0 bit. If the WTIM0 bit is set to 1, another wait or interrupt request is issued at the 9th falling edge of the clock.

2. Observe the following order when setting the WREL0 and ACKE0 bits.

- Be sure to set the ACKE0 bit and then set the WREL0 bit because the timing at which the setting is applied differs between the WREL0 and ACKE0 bits.

3. When the STT0 bit is set to 1, the following operations are performed according to the state the system was in before the bit was set:

- If the bus is released (communication is stopped), a master device pulls the SDA line low to issue a start condition (to serve as the master). Next, the master secures the specified time and then pulls the SCL line low.
- If there is no participation on the bus and communication reservation is enabled (the IICRSV bit of the IIC_IICFx register is set to 0 (default)), the start condition can be reserved. After the bus is released, a start condition is automatically issued.
- If there is no participation on the bus and communication cannot be reserved (the IICRSV bit of the IIC_IICFx register is set to 1), the STCF bit of the IIC_IICFx register is set to 1. No start condition is issued.
- If the master is in the wait state, the wait state is released and a start condition is issued again.

3.2.4 Slave address register

This register (IIC_SVAx: E007_000CH (IIC0), E10A_000CH (IIC1)) stores the address of a slave device when a device is connected to the serial bus as a slave device. 7 bits of slave address is set as 1 bit from 7 bits of this register. Bit 0 of this register always establishes 0.

7	6	5	4	3	2	1	0
Slave address							

Name	R/W	Bit No.	After Reset	Function
Slave address	R/W	7:0	00H	Stores a slave address. ex) slave address =0x16 It's set as IIC_SVA0 = 0x2C.

3.2.5 IICx transfer clock selection register

This register (IIC_IICCLx: E007_0010H (IIC0), E10A_0010H (IIC1)) specifies the transfer clock for the I^2C interface. Specify the transfer clock by using this register before setting the IICE0 bit of the IIC_IICCx register.

7	6	5	4	3	2	1	0
Reserved		CLD0	DAD0	SMC0	DFC0	CL01	CL00

Name	R/W	Bit No.	After Reset	Function
Reserved	R	7:6	0H	Reserved.
CLD0 Note1	R	5	0	Detects the level of the SCL line. 0: The level of the SCL line is low. 1: The level of the SCL line is high.
DAD0 Note1	R	4	0	Detects the level of the SDA line. 0: The level of the SDA line is low. 1: The level of the SDA line is high.
SMC0	R/W	3	0	Specifies the operating mode. 0: Standard mode (Maximum transfer rate: 100 kbps) 1: Fast mode (Maximum transfer rate: 400 kbps)
DFC0	R/W	2	0	Enables/disables digital filtering. " 0" setting is prohibited. 0: Digital filtering is disabled. 1: Digital filtering is enabled. Filtering is applied to input to SCLI, SDAI and noise is removed.
CL01 Note2	R/W	1	0	Selects the transfer clock frequency.
CL00 Note2	R/W	0	0	

CL01	CL00	Standard mode	Fast mode
0	0	fXX/44	fXX/24
0	1	fXX/86	fXX/24
1	0	Setting prohibited	Setting prohibited
1	1	Setting prohibited	Setting prohibited

Remark f_{XX}: Frequency of internal system clock
The internal system clock (IIC_CLK) is output from the system management unit (SMU).

Notes 1. The CLD0 and DAD0 bits are valid only when the IICE0 bit of the IIC_IICCx register is set to 1. If the CLD0 and DAD0 bits are read when the IICE0 bit is set to 0, 0 is returned, regardless of the state of the SCL/SDA line.

2. Set the CL01 and CL00 bits so that the frequency of the I^2C interface internal system clock (IIC_CLK) satisfies the condition indicated below. The same operation is performed, regardless of whether 01b or 10b is set. In the fast mode, the same operation is performed when 01b or 10b is set.

CL01	CL00	Standard Mode	Fast Mode
0	0	2.00 MHz ≤ f_{XX} ≤ 4.19 MHz	4.19 MHz ≤ f_{XX} ≤ 9.2 MHz
0	1	4.19 MHz ≤ f_{XX} ≤ 8.38 MHz	4.19 MHz ≤ f_{XX} ≤ 9.2 MHz
1	0	Setting prohibited	Setting prohibited
1	1	Setting prohibited	Setting prohibited

Notes Before setting the IICE bit of IIC_IICACTx register, transfer clock is established certainly.

3.2.6 IICx function extension register

This register (IIC_IICXx: E007_0014H (IIC0), E10A_0014H (IIC1)) chooses transfer clock at the time of a fast mode.

7	6	5	4	3	2	1	0
Reserved							CLX

Name	R/W	Bit No.	After Reset	Function
Reserved	R	7:1	00H	Reserved
CLX	R/W	0	0	Fast mode transfer clock select bit. 0: The transfer speed is the value set as the SMC bit of IICx_IICCLx register. 1: The transmission frequency which is at the time of single master will be 1/12 of a reference clock (It's chosen by the CL bit of IICx clock selection register.).

Notes. A frequency of a chosen clock is used between the 4MHz-4.6MHz..

3.2.7 IICx state register

This read-only register (IIC_IICSEx: E007_0018H (IIC0), E10A_0018H (IIC1)) indicates the state of the I^2C interface. If this register is read, one retry will always occur.

7	6	5	4	3	2	1	0
MSTS0	ALD0	EXC0	COI0	TRC0	ACKD0	STD0	SPD0

(1/4)

Name	R/W	Bit No.	After Reset	Function
MSTS0	R	7	0	Flag for indicating the master communication state. 0: Serving as a slave or communication is enabled 1: Serving as a master [Condition for setting this bit] • When a start condition is issued [Condition for clearing this bit] • When a stop condition is detected • When a master loses arbitration • When the LREL0 bit is set to 1 • When the IICE0 bit is set to 0 • When a reset is input
ALD0	R	6	0	Flag for indicating arbitration loss. 0: No arbitration has occurred or a master won arbitration 1: A master lost arbitration [Condition for setting this bit] • When a master loses arbitration [Condition for clearing this bit] • When the IICE0 bit is set to 0 • When a reset is input When this register is read, this bit is cleared, but it won't be reflected by reading data immediately. Without intending even when arbitration loss has happened when this register is read during a transmission period, one during a transmission period clears an arbitration flag in the macro, and to malfunction, uses IICSE0 certainly.

(2/4)

Name	R/W	Bit No.	After Reset	Function
EXC0	R	5	0	Flag for indicating whether an extension code has been received. 0: No extension code has been received. 1: An extension code has been received. [Condition for setting this bit] • When the higher 4 bits of the received address data are 0000b or 1111b (at the 8th rising edge of the SCL clock) [Condition for clearing this bit] • When a start condition is detected • When a stop condition is detected • When the LREL0 bit is set to 1 • When the IICE0 bit is set to 0 • When a reset is input
COI0	R	4	0	Flag for indicating an address match. 0: No address match was detected. 1: An address match was detected. [Condition for setting this bit] • When the received address data matches the slave address (IIC_SVAx register) of this device (at the 8th rising edge of the SCL clock) [Condition for clearing this bit] • When a start condition is detected • When a stop condition is detected • When the LREL0 bit is set to 1 • When the IICE0 bit is set to 0 • When a reset is input

Note For the wait period, see **4.1.6 Wait signal (WAIT).**

(3/4)

Name	R/W	Bit No.	After Reset	Function
TRC0	R	3	0	Flag for indicating the transmission/reception state. 0: Reception mode (or other than transmission mode) The SDA line is placed in the Hi-Z state. 1: Transmission mode Setting this bit to 1 enables serial data to be output to the SDA line. This setting is valid at the 9th falling edge or later of the SCL clock for the first byte. [Condition for setting this bit] For the master: • When a start condition is issued (STD0 = 1 and MSTS0 = 1) • When 0 is output as the LSB of the first byte of transmit/receive data For the slave: • When 1 is input as the LSB of the first byte of transmit/receive data [Condition for clearing this bit] • When a stop condition is detected • When a master loses arbitration • When the LREL0 bit is set to 1 • When the IICE0 bit is set to 0 • When the WREL0 bit is set to 1 during a wait period. Note • When a reset is input For the master: • When 1 is output as the LSB of the first byte of transmit/receive data For the slave: • When a start condition is detected (STD0 = 1 and MSTS0 = 0) • When 0 is input as the LSB of the first byte of transmit/receive data
ACKD0	R	2	0	Flag for indicating whether an ACK signal has been detected. 0: No ACK signal was detected. 1: An ACK signal was detected. [Condition for setting this bit] • When the level of the SDA line is low at the 9th rising edge of the SCL clock [Condition for clearing this bit] • First rising edge of the SCL clock for the next byte • When a stop condition is detected • When the LREL0 bit is set to 1 • When the IICE0 bit is set to 0 • When a reset is input

(4/4)

Name	R/W	Bit No.	After Reset	Function
STD0	R	1	0	Flag for indicating whether a start condition has been detected. 0: No start condition was detected. 1: A start condition was detected. A setting of 1 indicates that an address is being transferred. [Condition for setting this bit] • When a start condition is detected [Condition for clearing this bit] • First rising edge of the SCL clock for the address transfer byte following the detection of a start condition after this bit is set • When a stop condition is detected • When the IICE0 bit is set to 0 • When a reset is input
SPD0	R	0	0	Flag for indicating whether a stop condition has been detected. 0: No stop condition was detected. 1: A stop condition was detected. A setting of 1 setting indicates that communication by a master has ended and the bus is released. [Condition for setting this bit] • When a stop condition is detected [Condition for clearing this bit] • First rising edge of the SCL clock for the address transfer byte following the detection of a start condition after this bit is set • When the IICE0 bit is set to 0 • When a reset is input

3.2.8 IICx state register

This read-only register (IIC_IICSEx: E007_001CH (IIC0), E10A_001CH (IIC1)) indicates the state of the I^2C interface and is used during emulation. When this register is used, without clearing the ALD bit, it's possible to read the same status bit as IIC0 state register (IICS0). If this register is read, one retry will always occur.

7	6	5	4	3	2	1	0
MSTS0	ALD0	EXC0	COI0	TRC0	ACKD0	STD0	SPD0

3.2.9 IICx flag register

This register (IIC_IICFx: E007_0020H (IIC0), E10A_0020H (IIC1)) controls the I^2C interface.
Operation is not guaranteed if this register is written when the IICE0 bit of the IIC_IICCx register is set to 1.

7	6	5	4	3	2	1	0
STCF	IICBSY	0	0	0	0	STCEN	IICRSV

Name	R/W	Bit No.	After Reset	Function
STCF	R	7	0	Flag for indicating whether the STT0 bit of the IIC_IICCx register has cleared. 0: A start condition was issued. 1: The STT0 bit has been cleared. [Condition for setting this bit] • When the STT0 bit is cleared while communication reservation is disabled (IICRSV = 1) [Condition for clearing this bit] • When the STT0 bit is set to 1 • When the IICE0 bit is set to 0 • When a reset is input
IICBSY Note1	R	6	0	Flag for indicating the I2C bus state. 0: The bus is released. 1: The bus is occupied. [Condition for setting this bit] • When a start condition is detected • When the IICE0 bit is set to 0 while the STCEN bit is set to 0 [Condition for clearing this bit] • When the IICE0 bit is set to 0 • When a reset is input
0	R	5:2	0H	Fix these bits to 0.
STCENNote2	R/W	1	0	By setting this bit to 1 after enabling operation (IICE0 = 1), a start condition can be issued without detecting a stop condition. 0: No start condition can be issued without detecting a stop condition. 1: A start condition can be issued without detecting a stop condition. Remark This bit is automatically cleared when any of the following conditions occurs: • Start condition detection • Reset input
IICRSV	R/W	0	0	Enables/disables communication reservation. 0: Enables communication reservation. 1: Disables communication reservation.

Note 1 At least 2 clocks of busy status (IICBSY) is need by the internal system clock before the state of the bus is reflected after IIC is made enable. There is a possibility that a difference for 1 clocks occurs by a simultaneous change in the condition, so check it after wait for 3 clocks.

2 When setting the STCEN bit to 1, ensure that other I^2C devices on the I^2C bus are not engaged in communication. If the STCEN bit is set to 1 and the STT0 bit of the IIC_IICC0 register is set to 1 while other I^2C devices are engaged in communication, a start condition is issued and data being sent is lost.

3.3 Notice about register access

Register	bit	Notice
IICACT0	IICE	After writing, time for the max. 3 clocks is needed until it's reflected as read data. (By a sampling clock inside IIC.) After writing, read certainly, and confirm that it was expected data. After it's confirmed that macro operation has ended perfectly when setting this bit in 0. For example when writing 0 in this bit by the following cycle written in the STP bit of IICC0, the stop condition isn't sometimes issued.
IIC0	–	Don't access until transmission ends. During forwarding, don't do setting change of transfer mode.
IICC0	LREL	After writing in 1, it's borrowed whether it's max. 3 clocks by a sampling clock inside IIC until it's cleared automatically. After writing in 1, confirm that I read and was cleared.
	WREL	
SVA0	–	Before permitting operation in IICACT0, it's established.
IICCL0	CL[1:0]	
IICS0	ALD	It's borrowed whether it's at most 1 clock by a sampling clock inside IIC until it's cleared automatically after reading. During a transfer operation doesn't read this register.
IICF0	STCEN	After setting the STCEN bit in 1, don't make the value of the STCEN bit 0 until the start condition is generated. After writing 1 in the STT0 bit of IICC0, this bit is set as 1, and when it make the start condition occur, malfunctions.

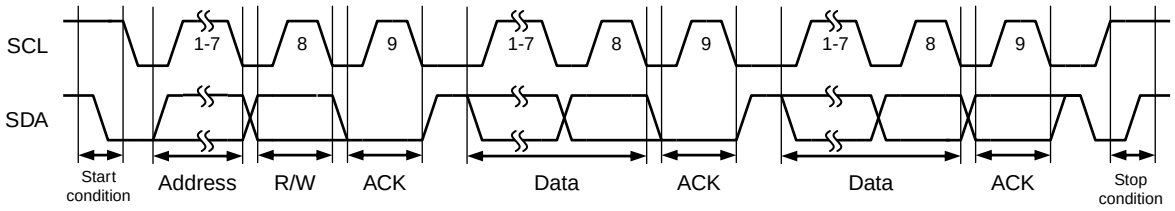
4. Description of Functions

4.1 IIC Bus Operations

This section describes the serial data communication format of the I^2C bus and explains the meanings of the signals used.

Figure 4-1 shows the timing of transferring a start condition, slave address, data, and stop condition output on the SDA line of the I^2C bus.

Figure 4-1. Timing of I^2C Bus Serial Data Transfer



A start condition, slave address, and stop condition are output by the master device.

The acknowledge signal (ACK) can be output by either the master device or slave device. (Usually, the receiver of 8-bit data outputs the ACK signal.)

The serial clock (SCL) is output by the master device.

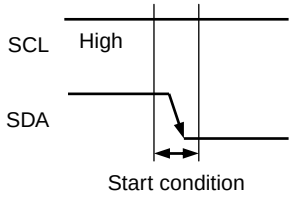
4.1.1 Start condition

A start condition is issued when the SCL line is high (when the serial clock is not output) and the SDA line is pulled low.

A start condition is a signal output by the master device when it starts a serial transfer to a slave device.

The I^2C interface incorporates hardware for detecting a start condition in slave operation.

Figure 4-2. Start Condition

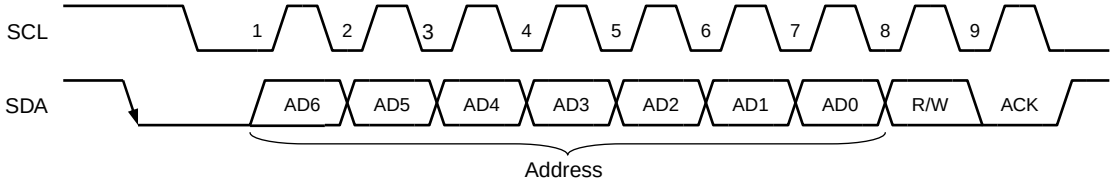


A serial transfer ends with a stop condition. If a start condition is issued again before the stop condition for the current transaction is issued, this start condition is called a restart condition.

4.1.2 Address

The 7-bit data following a start condition is defined as the address.
The address is 7-bit data output by the master device to select a particular slave from multiple slave devices on the bus line. This means that a unique address needs to be assigned to each slave on the bus line.
A slave device detects, by hardware, that data on the SDA line is an address then checks if the 7-bit data matches the value of the slave address register (SVA0). If the 7-bit data matches the value of the SVA0 register, the slave device is selected. The slave device communicates with the master device until the master device transmits a restart condition or a stop condition.

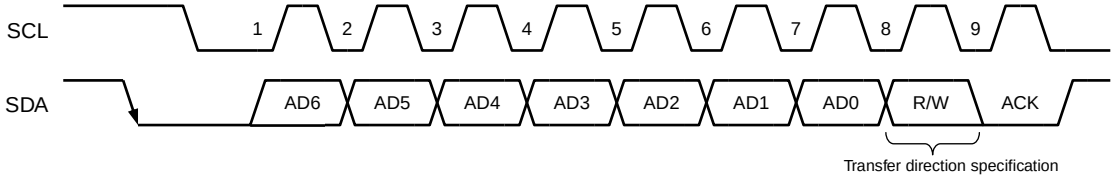
Figure 4-3. Address



4.1.3 Transfer direction specification

The master device transmits 1-bit data for specifying the transfer direction after the 7-bit address data. If the transfer direction bit is set to 0, it means that the master device is transmitting data to a slave device. If the transfer direction bit is set to 1, it means that the master device is receiving data from a slave device.

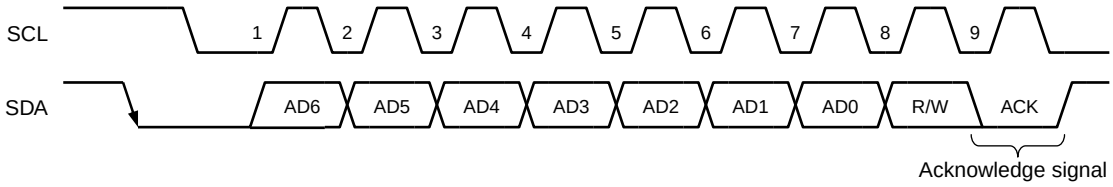
Figure 4-4. Transfer Direction Specification



4.1.4 Acknowledge signal (ACK)

The ACK signal is used by the receiving side to notify the transmitting side of the reception of serial data.
The receiving side returns an ACK signal each time 8-bit data is received. An ACK signal is generated by pulling the SDA line low during the 9th high-level period of the clock on the SCL line.
After transmitting 8-bit data, the transmitting side checks if an ACK signal has been returned from the receiving side.
If an ACK signal is returned, the master device proceeds to the next processing, assuming that the data has been received normally. If no ACK signal has been returned from the slave device, the data is not received normally. In this case, the master device outputs a stop condition to stop transmission.

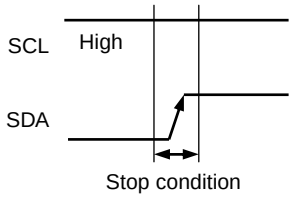
Figure 4-5. Acknowledge Signal



4.1.5 Stop condition

A stop condition is issued when the SCL line is high (when serial transfer ends and the serial clock is not output) and the SDA line is pulled high.
A stop condition is a signal output by the master device to a slave device when a serial transfer ends.
The I^2C interface incorporates hardware for detecting a stop condition in slave operation.

Figure 4-6. Stop Condition

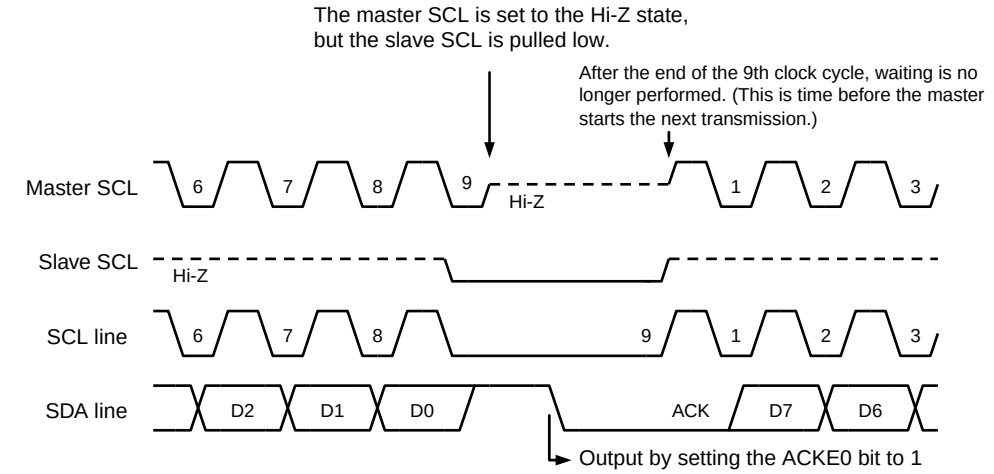


4.1.6 Wait signal (WAIT)

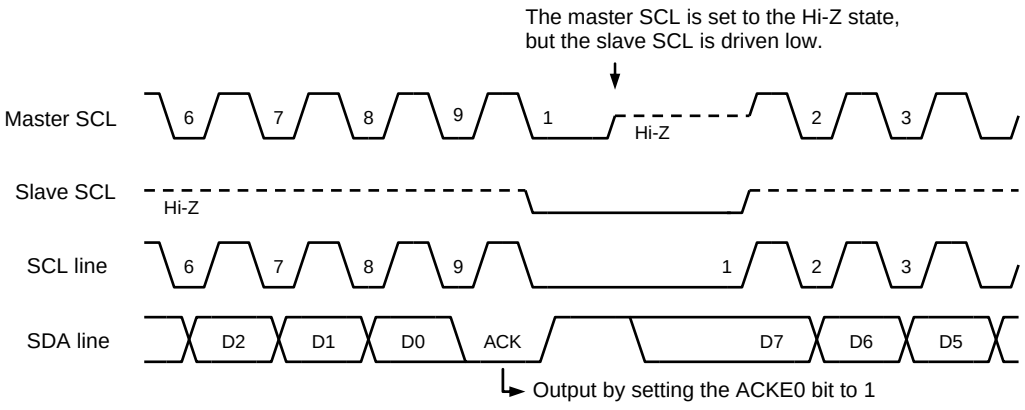
The wait signal is used by the master/slave device to notify the communication destination that the master/slave device is preparing for data transmission/reception (that is, the device is in the wait state).
By pulling the SCL line low, the master/slave device reports its wait state to the communication destination.
When the WAIT signal is canceled, the master device can start the next transfer operation.

Figure 4-7. Wait Signal

(a) Waiting for 8 clock cycles



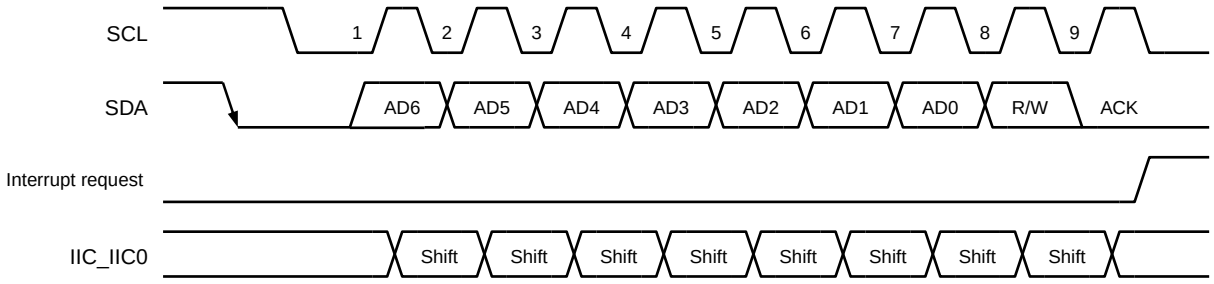
(b) Waiting for 9 clock cycles



4.2 Shift Register (IIC_IIC0) Operation

The shift register (IIC_IIC0) performs a shift operation at the rising edge of the serial clock (SCL). At the rising edge of the SCL line, the register shifts one bit toward the MSB, and the value of the SDA line is read into the LSB. Figure 4-8 shows an example of the IIC_IIC0 register shift operation.

Figure 4-8. Example of Shift Register Operation (During Address Transfer with a 9-Clock-Cycle Wait)



4.3 Extension Code

When the higher 4 bits of a received address are 0000b or 1111b, the extension code reception flag (EXC0) is set to 1 and an interrupt request signal is sent at the 8th falling edge of the clock, assuming the reception of an extension code. The address stored in the SVA0 register is not affected.

For example, if 111110xxb is set in the SVA0 register and 111110xxb is transferred from the master device in a 10-bit address transfer, the EXC0 bit of the IIC_IICSE0 register is set to 1 because the higher 4 bits of data matches, and the COI0 bit of the IIC_IICSE0 register is set to 1 because the higher 7 bits of data matches.

Note, however, that an interrupt request signal is sent at the 8th falling edge of the clock.

The processing performed after an interrupt request signal is sent depends on the data that follows the extension code. This data should be processed by using software.

To disable slave operation after reception of an extension code, set the LREL0 bit of the IIC_IICC0 register to 1. This sets the communication standby state.

Table 4-1. Extension Code Bit Definition

Slave Address	R/W Bit	Explanation
0000000b	0	General call address
0000000b	1	Start byte
0000001b	x	CBUS address
0000010b	x	Address reserved for a different bus format
0000011b	x	Address reserved for future use
00001xxb	x	
11111xxb	x	
11110xxb	x	10-bit slave address specification

Remark x: Undefined

4.4 Arbitration

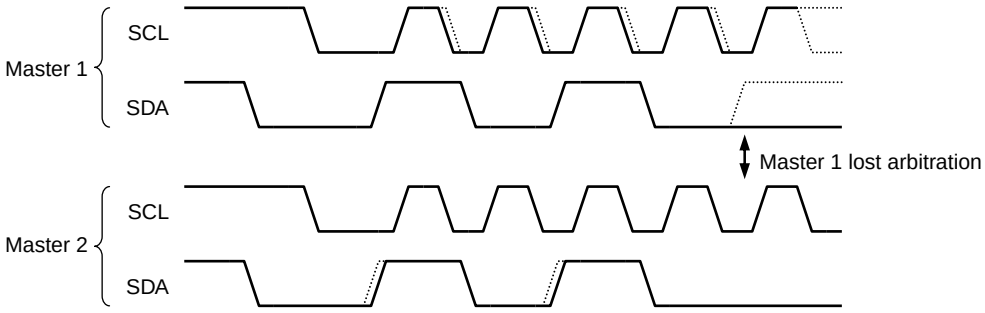
When multiple master devices issue a start condition at the same time, the I^2C interface compares the 7-bit address output from each master device with the SDA value, and grants the bus to the master device whose address matches the SDA line. This operation is called arbitration, and if a device is not granted the bus as a result of arbitration, such state is called arbitration loss.

The master that lost arbitration sets the ALD0 flag to 1 when the loss is determined, and waits as a slave with the SCL and SDA lines kept in the Hi-Z state.

The ALD0 flag must be detected by using software when the next interrupt request is issued.

For the interrupt generation timing, see **4.5 Interrupts.**

Figure 4-9. Example of Arbitration



Arbitration occurs under the following conditions:

<1> During address transfer
<2> During R/W information transfer after address transfer
<3> During extension code transfer
<4> During R/W information transfer after extension code transfer
<5> During data transfer
<6> During ACK transfer after data reception
<7> If a restart condition is detected during data transfer.
<8> If a stop condition is detected during data transfer.
<9> If the SDL line is low level when a master attempts to issue a restart condition.
<10> If a stop condition is detected when a master attempts to issue a restart condition.
<11> If the SDL line is low level when a master attempts to issue a stop condition.
<12> If the SCL line is pulled low when a master attempts to issue a restart condition.

Remark In the case of <1> to <7>, <9>, <11>, and <12>, an interrupt request is issued at the basic timing (at the 8th falling edge or the 9th rising edge of the clock after byte transfer).
In the case of <8> and <10>, an interrupt request is issued when a stop condition interrupt is generated while the SPIE0 bit of the IIC_IICC0 register is set to 1. Be sure to set the SPIE0 bit to 1 if arbitration might occur during master operation.

4.5 Interrupts

This section describes the timing at which an interrupt request is issued by the I^2C interface and indicates the value of the IIC_IICSE0 register when the interrupt is generated.
An interrupt signal is generated at the following timing:

<1> At the 8th or 9th falling edge of the serial clock (IIC_SCLK) (controlled by the WTIM0 bit of the IIC_IICC0 register)
<2> When a stop condition is detected (controlled by the SPIE0 bit of the IIC_IICC0 register)

Remarks 1. △ and ▲ show the timing at which an interrupt occurs.
An interrupt might not occur at △, depending on the state of the SPIE0 bit.

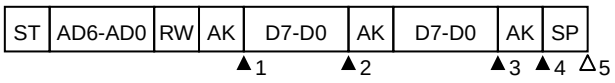
2. A value of "x" in the IIC_IICSE0 register does not represent an undefined value, but means that either 1 or 0 may be assumed.

3. The following symbols are used:
- ST: Start condition
- AD6-AD0: Address data
- RW: Transfer direction specification (R/W)
- AK: Acknowledge signal (ACK)
- D7-D0: Transfer data
- SP: Stop condition

4.5.1 Master operation

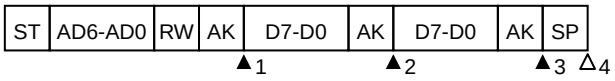
Figure 4-10. Timing for Master Operation

(1) Start → Address → Data → Data → ⋯ → Stop (when WTIM0 = 0)



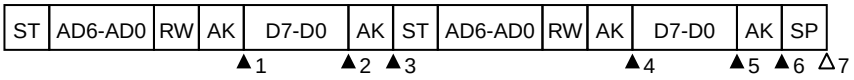
▲1: IIC_IICSE0 = 1000x110
▲2: IIC_IICSE0 = 1000x000
▲3: IIC_IICSE0 = 1000x000 (The WTIM0 bit is set to 1.)
▲4: IIC_IICSE0 = 1000xx00 (The SPT0 bit is set to 1.)
△5: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(2) Start → Address → Data → Data → ⋯ → Stop (when WTIM0 = 1)



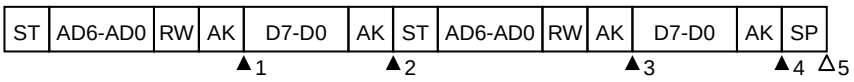
▲1: IIC_IICSE0 = 1000x110
▲2: IIC_IICSE0 = 1000x100
▲3: IIC_IICSE0 = 1000xx00 (The SPT0 bit is set to 1.)
△4: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(3) Start → Address → Data → ⋯ → Start → Address → Data → ⋯ → Stop (when WTIM0 = 0)



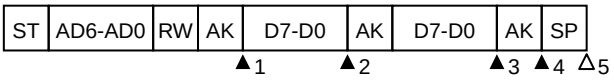
▲1: IIC_IICSE0 = 1000x110
▲2: IIC_IICSE0 = 1000x000 (The WTIM0 bit is set to 1.)
▲3: IIC_IICSE0 = 1000xx00 (The WTIM0 bit is cleared and the STT0 bit is set to 1.)
▲4: IIC_IICSE0 = 1000x110
▲5: IIC_IICSE0 = 1000x000 (The WTIM0 bit is set to 1.)
▲6: IIC_IICSE0 = 1000xx00 (The SPT0 bit is set to 1.)
△7: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(4) Start → Address → Data → ⋯ → Start → Address → Data → ⋯ → Stop (when WTIM0 = 1)



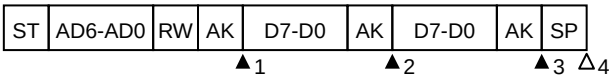
▲1: IIC_IICSE0 = 1000x110
▲2: IIC_IICSE0 = 1000xx00
▲3: IIC_IICSE0 = 1000x110
▲4: IIC_IICSE0 = 1000xx00 (The SPT0 bit is set to 1.)
△5: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(5) Start → Code → Data → Data → ⋯ → Stop (when WTIM0 = 0)



▲1: IIC_IICSE0 = 1010x110
▲2: IIC_IICSE0 = 1010x000
▲3: IIC_IICSE0 = 1010x000 (The WTIM0 bit is set to 1.)
▲4: IIC_IICSE0 = 1010xx00 (The SPT0 bit is set to 1.)
△5: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(6) Start → Code → Data → Data → ⋯ → Stop (when WTIM0 = 1)



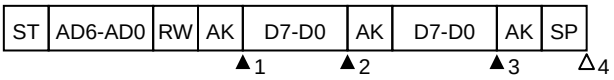
▲1: IIC_IICSE0 = 1010x110
▲2: IIC_IICSE0 = 1010x100
▲3: IIC_IICSE0 = 1010xx00 (The SPT0 bit is set to 1.)
△4: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

4.5.2 Slave operation

(1) When slave address data is received (match with SVA0)

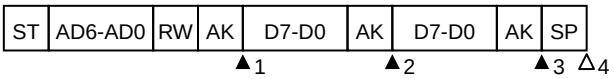
Figure 4-11. Timing for Slave Address Data Reception

(a) Start → Address → Data → Data → ⋯ → Stop (when WTIM0 = 0)



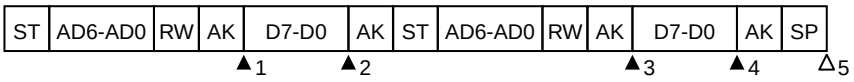
▲1: IIC_IICSE0 = 0001x110
▲2: IIC_IICSE0 = 0001x000
▲3: IIC_IICSE0 = 0001x000
△4: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(b) Start → Address → Data → Data → ⋯ → Stop (when WTIM0 = 1)



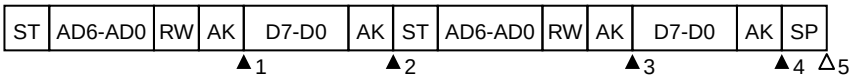
▲1: IIC_IICSE0 = 0001x110
▲2: IIC_IICSE0 = 0001x100
▲3: IIC_IICSE0 = 0001xx00
△4: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(c) Start → Address → Data → ⋯ → Start → Address → Data → ⋯ → Stop (when WTIM0 = 0)
After restart, match with SVA0



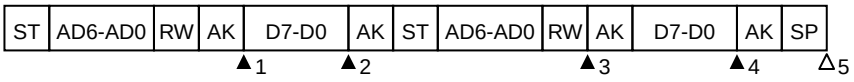
▲1: IIC_IICSE0 = 0001x110
▲2: IIC_IICSE0 = 0001x000
▲3: IIC_IICSE0 = 0001x110
▲4: IIC_IICSE0 = 0001x000
△5: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(d) Start → Address → Data → ⋯ → Start → Address → Data → ⋯ → Stop (when WTIM0 = 1)
After restart, match with SVA0



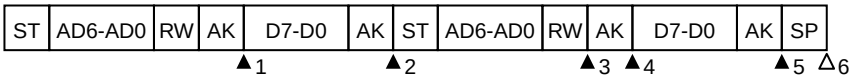
▲1: IIC_IICSE0 = 0001x110
▲2: IIC_IICSE0 = 0001xx00
▲3: IIC_IICSE0 = 0001x110
▲4: IIC_IICSE0 = 0001xx00
△5: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(e) Start → Address → Data → ⋯ → Start → Code → Data → ⋯ → Stop (when WTIM0 = 0)
After restart, extension code reception



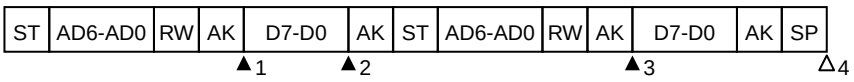
▲1: IIC_IICSE0 = 0001x110
▲2: IIC_IICSE0 = 0001x000
▲3: IIC_IICSE0 = 0010x010
▲4: IIC_IICSE0 = 0010x000
△5: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(f) Start → Address → Data → ⋯ → Start → Code → Data → ⋯ → Stop (when WTIM0 = 1)
After restart, extension code reception



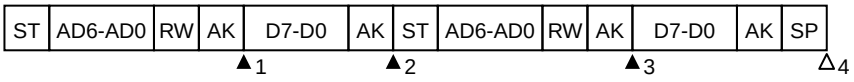
▲1: IIC_IICSE0 = 0001x110
▲2: IIC_IICSE0 = 0001xx00
▲3: IIC_IICSE0 = 0010x010
▲4: IIC_IICSE0 = 0010x110
▲5: IIC_IICSE0 = 0010xx00
△6: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(g) Start → Address → Data → ⋯ → Start → Address → Data → ⋯ → Stop (when WTIM0 = 0)
After re start, address mismatch (other than extension code)



▲1: IIC_IICSE0 = 0001x110
▲2: IIC_IICSE0 = 0001x000
▲3: IIC_IICSE0 = 00000x10
△4: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(h) Start → Address → Data → ⋯ → Start → Address → Data → ⋯ → Stop (when WTIM0 = 1)
After re start, address mismatch (other than extension code)

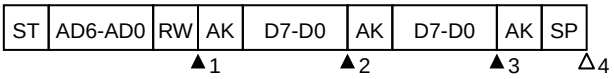


▲1: IIC_IICSE0 = 0001x110
▲2: IIC_IICSE0 = 0001xx00
▲3: IIC_IICSE0 = 00000x10
△4: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(2) When an extension code is received

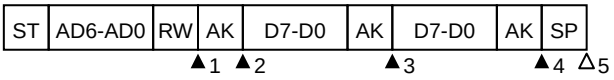
Figure 4-12. Timing for Extension Code Reception

(a) Start → Code → Data → Data → ⋯ → Stop (when WTIM0 = 0)



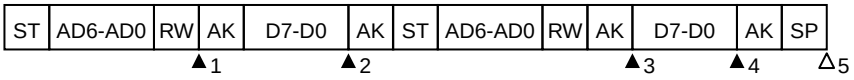
▲1: IIC_IICSE0 = 0010x010
▲2: IIC_IICSE0 = 0010x000
▲3: IIC_IICSE0 = 0010x000
△4: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(b) Start → Code → Data → Data → ⋯ → Stop (when WTIM0 = 1)



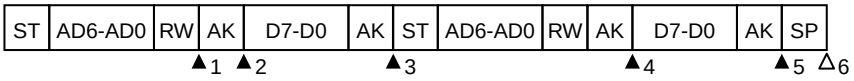
▲1: IIC_IICSE0 = 0010x010
▲2: IIC_IICSE0 = 0010x110
▲3: IIC_IICSE0 = 0010x100
▲4: IIC_IICSE0 = 0010xx00
△5: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(c) Start → Code → Data → ⋯ → Start → Address → Data → ⋯ → Stop (when WTIM0 = 0)
After restart, match with SVA0



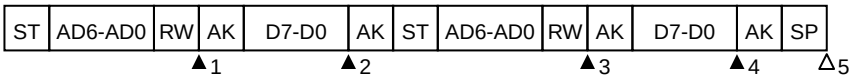
▲1: IIC_IICSE0 = 0010x010
▲2: IIC_IICSE0 = 0010x000
▲3: IIC_IICSE0 = 0001x110
▲4: IIC_IICSE0 = 0001x000
△5: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(d) Start → Code → Data → ⋯ → Start → Address → Data → ⋯ → Stop (when WTIM0 = 1)
After restart, match with SVA0



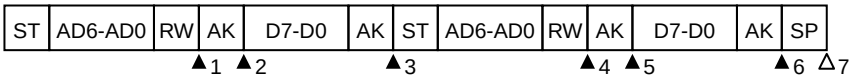
▲1: IIC_IICSE0 = 0010x010
▲2: IIC_IICSE0 = 0010x110
▲3: IIC_IICSE0 = 0010xx00
▲4: IIC_IICSE0 = 0001x110
▲5: IIC_IICSE0 = 0001xx00
△6: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(e) Start → Code → Data → ⋯ → Start → Code → Data → ⋯ → Stop (when WTIM0 = 0)
After restart, extension code reception



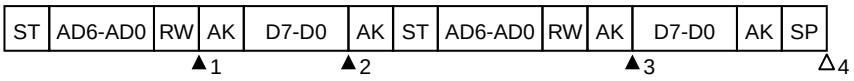
▲1: IIC_IICSE0 = 0010x010
▲2: IIC_IICSE0 = 0010x000
▲3: IIC_IICSE0 = 0010x010
▲4: IIC_IICSE0 = 0010x000
△5: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(f) Start → Code → Data → ⋯ → Start → Code → Data → ⋯ → Stop (when WTIM0 = 1)
After restart, extension code reception



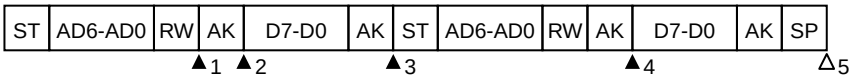
▲1: IIC_IICSE0 = 0010x010
▲2: IIC_IICSE0 = 0010x110
▲3: IIC_IICSE0 = 0010xx00
▲4: IIC_IICSE0 = 0010x010
▲5: IIC_IICSE0 = 0010x110
▲6: IIC_IICSE0 = 0010xx00
△7: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(g) Start → Code → Data → ⋯ → Start → Address → Data → ⋯ → Stop (when WTIM0 = 0)
After restart, address mismatch (other than extension code)



▲1: IIC_IICSE0 = 0010x010
▲2: IIC_IICSE0 = 0010x000
▲3: IIC_IICSE0 = 00000x10
△4: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(h) Start → Code → Data → ⋯ → Start → Address → Data → ⋯ → Stop (when WTIM0 = 1)
After restart, address mismatch (other than extension code)

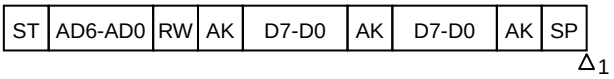


▲1: IIC_IICSE0 = 0010x010
▲2: IIC_IICSE0 = 0010x110
▲3: IIC_IICSE0 = 0010xx00
▲4: IIC_IICSE0 = 00000x10
△5: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

4.5.3 Operation at the time of an address mismatch

Figure 4-13. Timing in Address Mismatch

Start → Code → Data → Data → ⋯ → Stop



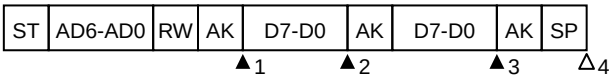
△1: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

4.5.4 Arbitration loss

(1) Operation as a slave after arbitration loss

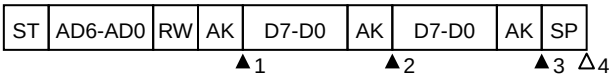
Figure 4-14. Timing for Operation as a Slave After Arbitration Loss

(a) When arbitration is lost during slave address data transmission (when WTIM0 = 0)



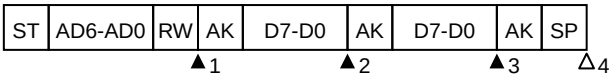
▲1: IIC_IICSE0 = 0101x110
(Example: The ALD0 bit is read during interrupt servicing.)
▲2: IIC_IICSE0 = 0001x000
▲3: IIC_IICSE0 = 0001x000
△4: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(b) When arbitration is lost during slave address data transmission (when WTIM0 = 1)



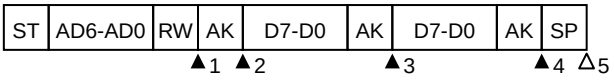
▲1: IIC_IICSE0 = 0101x110
(Example: The ALD0 bit is read during interrupt servicing.)
▲2: IIC_IICSE0 = 0001x100
▲3: IIC_IICSE0 = 0001xx00
△4: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(c) When arbitration is lost during extension code transmission (when WTIM0 = 0)



▲1: IIC_IICSE0 = 0110x010 (Example: The ALD0 bit is read during interrupt servicing.)
▲2: IIC_IICSE0 = 0010x000
▲3: IIC_IICSE0 = 0010x000
△4: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(d) When arbitration is lost during extension code transmission (when WTIM0 = 1)

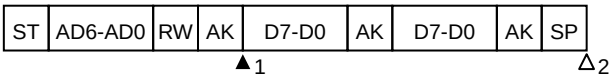


▲1: IIC_IIICSE0 = 0110x010
(Example: The ALD0 bit is read during interrupt servicing.)
▲2: IIC_IICSE0 = 0010x110
▲3: IIC_IICSE0 = 0010x100
▲4: IIC_IICSE0 = 0010xx00
△5: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(2) When participation in communication is disabled after arbitration loss

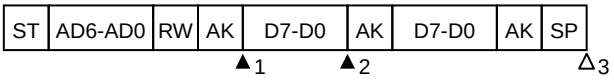
Figure 4-15. Timing When Participation in Communication Is Disabled After Arbitration Loss

(a) When arbitration is lost during slave address data transmission (when WTIM0 = 1)



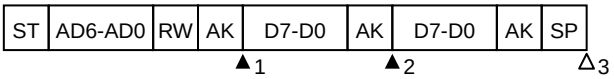
▲1: IIC_IICSE0 = 01000110
(Example: The ALD0 bit is read during interrupt servicing.)
△2: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(b) When arbitration is lost during data transfer (when WTIM0 = 0)



▲1: IIC_IICSE0 = 10001110
▲2: IIC_IICSE0 = 01000000
(Example: The ALD0 bit is read during interrupt servicing.)
△3: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

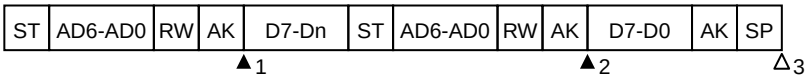
(c) When arbitration is lost during data transfer (when WTIM0 = 1)



▲1: IIC_IICSE0 = 10001110
▲2: IIC_IICSE0 = 01000100
(Example: The ALD0 bit is read during interrupt servicing.)
△3: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(d) When arbitration of a restart condition is lost during data transfer

Other than extension code (Example: Mismatch with SVA0, WTIM0 = 1)



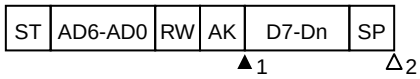
▲1: IIC_IICSE0 = 1000x110

▲2: IIC_IICSE0 = 01000110

(Example: The ALD0 bit is read during interrupt servicing.)

△3: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

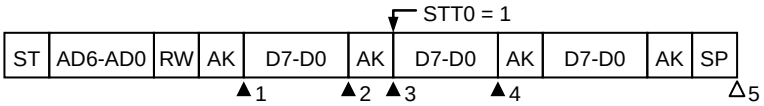
(e) When arbitration of a stop condition is lost during data transfer



▲1: IIC_IICSE0 = 1000x110

△2: IIC_IICSE0 = 01000001 (Only when the SPIE0 bit is set to 1.)

(f) When arbitration is lost because a restart condition could not be generated due to a low data level (when WTIM0 = 0)



▲1: IIC_IICSE0 = 1000x110

▲2: IIC_IICSE0 = 1000x000 (The WTIM0 bit is set to 1.)

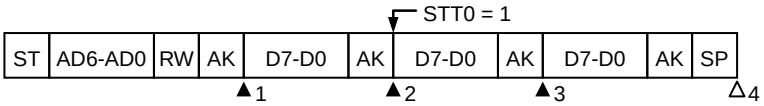
▲3: IIC_IICSE0 = 1000xx00 (The WTIM0 bit is cleared and the STT0 bit is set to 1.)

▲4: IIC_IICSE0 = 01000000

(Example: The ALD0 bit is read during interrupt servicing.)

△5: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(g) When arbitration is lost because a restart condition could not be generated due to a low data level (when WTIM0 = 1)



▲1: IIC_IICSE0 = 1000x110

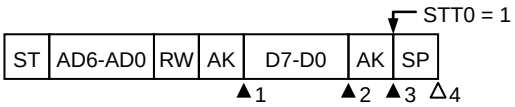
▲2: IIC_IICSE0 = 1000x100 (The STT0 bit is set to 1.)

▲3: IIC_IICSE0 = 01000100

(Example: The ALD0 bit is read during interrupt servicing.)

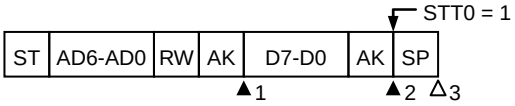
△4: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(h) When arbitration is lost because a restart condition could not be generated due to the generation of a stop condition (when WTIM0 = 0)



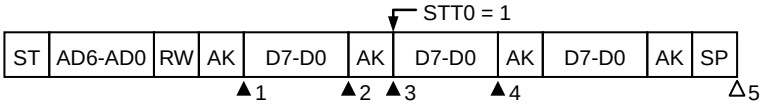
▲1: IIC_IICSE0 = 1000x110
▲2: IIC_IICSE0 = 1000x000 (The WTIM0 bit is set to 1.)
▲3: IIC_IICSE0 = 1000xx00 (The STT0 bit is set to 1.)
△4: IIC_IICSE0 = 01000001 (Only when the SPIE0 bit is set to 1.)

(i) When arbitration is lost because a restart condition could not be generated due to the generation of a stop condition (when WTIM0 = 1)



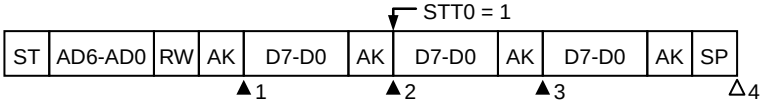
▲1: IIC_IICSE0 = 1000x110
▲2: IIC_IICSE0 = 1000xx00 (The STT0 bit is set to 1.)
△3: IIC_IICSE0 = 01000001 (Only when the SPIE0 bit is set to 1.)

(j) When arbitration is lost because a stop condition could not be generated due to a low data level (when WTIM0 = 0)



▲1: IIC_IICSE0 = 1000x110
▲2: IIC_IICSE0 = 1000x000 (The WTIM0 bit is set to 1.)
▲3: IIC_IICSE0 = 1000xx00 (The WTIM0 bit is cleared and the SPT0 bit is set to 1.)
▲4: IIC_IICSE0 = 01000000
(Example: The ALD0 bit is read during interrupt servicing.)
△5: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(k) When arbitration is lost because a stop condition could not be generated due to a low data level (when WTIM0 = 1)

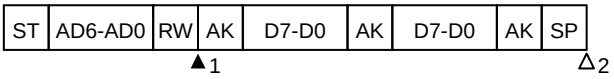


▲1: IIC_IICSE0 = 1000x110
▲2: IIC_IICSE0 = 1000xx00 (The SPT0 bit is set to 1.)
▲3: IIC_IICSE0 = 01000100
(Example: The ALD0 bit is read during interrupt servicing.)
△4: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(3) When participation in communication is not performed after arbitration loss

Figure 4-16. Timing When Participation in Communication Is Not Performed After Arbitration Loss

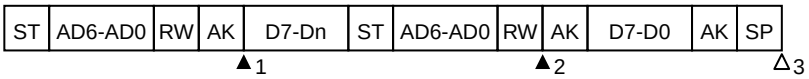
(a) When arbitration is lost during extension code transmission



▲1: IIC_IICSE0 = 0110x010
(Example: The ALD0 bit is read during interrupt servicing.)
The LREL0 bit is set to 1 by software.

△2: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(b) When arbitration of a restart condition is lost during data transfer (extension code)



▲1: IIC_IICSE0 = 1000x110

▲2: IIC_IICSE0 = 0110x010
(Example: The ALD0 bit is read during interrupt servicing.)
The LREL0 bit is set to 0 by software.

△3: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

4.6 Wakeup Operation

In a wake-up operation, an interrupt request signal is generated when the I^2C interface serves as a slave and the slave address and extension code are received.
An unnecessary interrupt is not generated unless the address matches, thus enhancing the efficiency of processing.
The wake-up standby state is set by the detection of a start condition.
Even during master operation (when a start condition has been issued), the master might be switched to a slave due to an arbitration loss. Therefore, the wake-up standby state needs to be set while an address is being transmitted.

Caution The generation of a stop condition interrupt is enabled by setting the SPIE0 bit of the IIC_IICC0 register to 1, independent of the wake-up operation.

4.7 Acknowledge Signal (ACK)

The ACK signal is generated by pulling the SDA line low during the 9th high-level period of the clock on the SCL line.
When the ACKE0 bit of the IIC_IICC0 register is set to 1, generation of an ACK signal is enabled.
The TRC0 bit of the IIC_IICSE0 register is set to 0 or 1 according to the value of the 8th bit (LSB) of the address data. When the TRC0 bit is set to 0 (receiving side), the ACKE0 bit needs to be set to 1.
By setting the ACKE0 bit to 0, the slave receiving side (with the MSTS0 bit and TRC0 bit of the IIC_IICSE0 register set to 0) can request the master side not to start the next transfer if the next data is not required for some reason after the reception of multiple-byte data.
Similarly, by setting the ACKE0 bit to 0 to disable ACK signal generation, the master receiving side (with the MSTS0 bit set to 1 and the TRC0 bit set to 0) needs to warn the slave receiving side not to output MSB data on the SDA line if the next data is not required and a restart condition or stop condition needs to be issued.

4.8 Communication Reservation

If a device has failed to become either a master or a slave as a result of arbitration, or does not operate as a slave after an extension code has been received (if ACK is not returned and the bus is released by setting the LREL0 bit of the IIC_IICC0 register to 1), the device can participate in arbitration to become a master after the end of the current communication by reserving the next communication.
By setting the STT0 bit of the IIC_IICC0 register while the device is in the standby state, a start condition is automatically issued after the bus is released (after detection of a stop condition) and the device enters the wait state.
When a bus release detection (stop condition detection) interrupt is generated, the device starts address transfer as a master by writing to the IIC_IIC0 register.
At this time, the SPIE0 bit of the IIC_IICC0 register needs to be set to 1.
If the IIC_IIC0 register is written to before the stop condition detection interrupt is generated, the data is invalid.

4.9 Communication

4.9.1 Master operation

Figure 4-17 and Figure 4-18 show the communication procedure for master operation.

Figure 4-17. Start with Communication Reservation Enabled and Stop Condition Detected

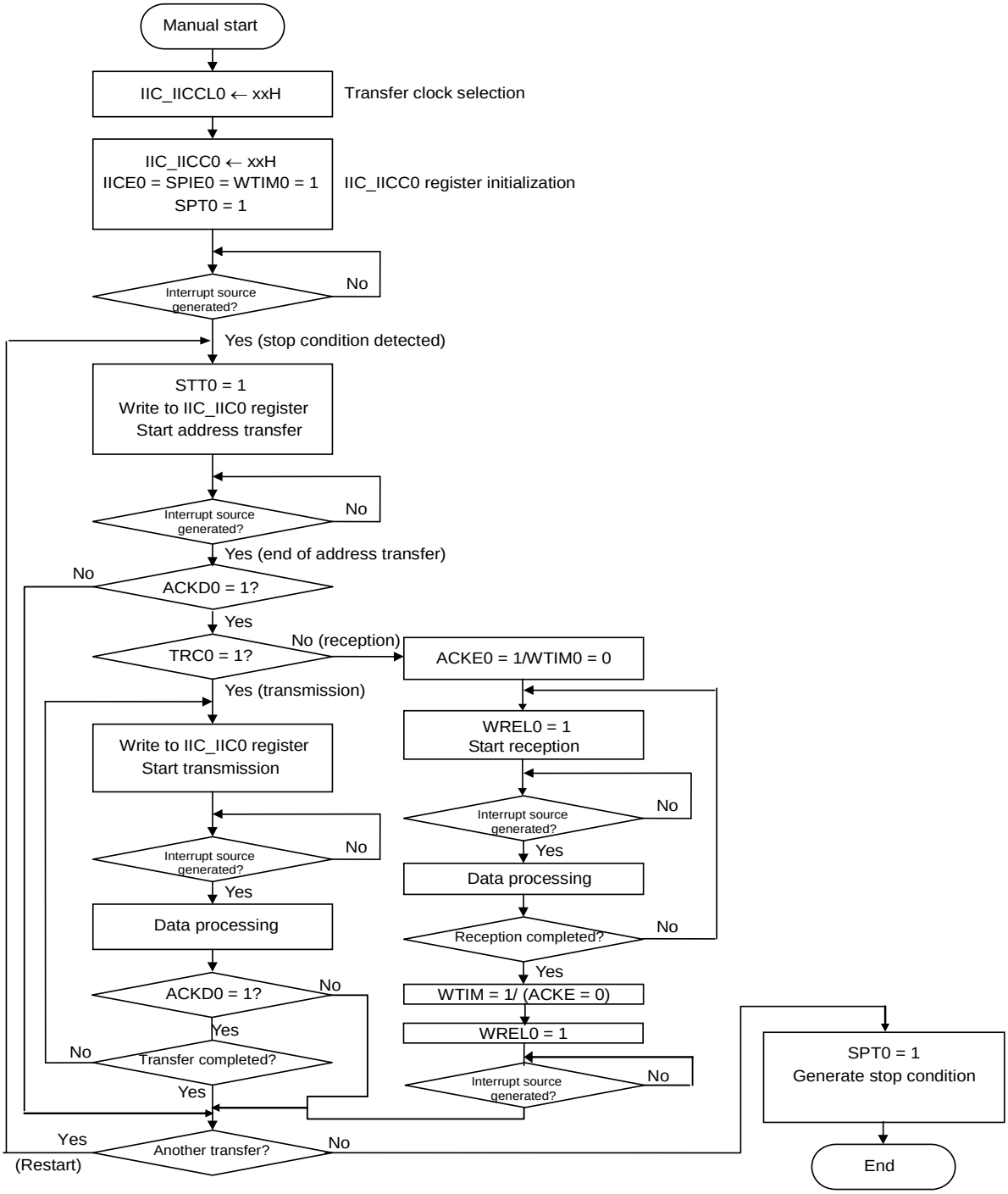
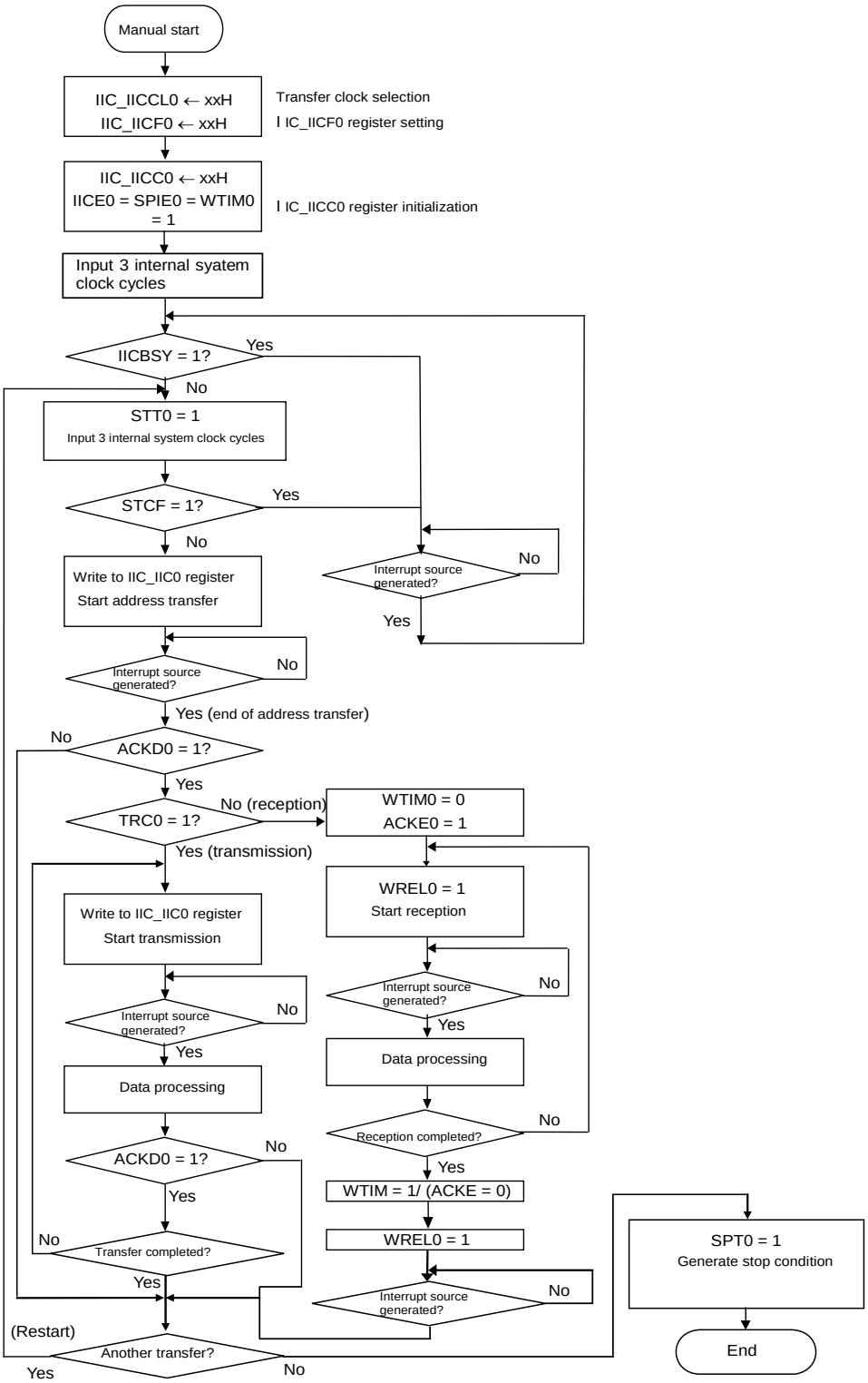


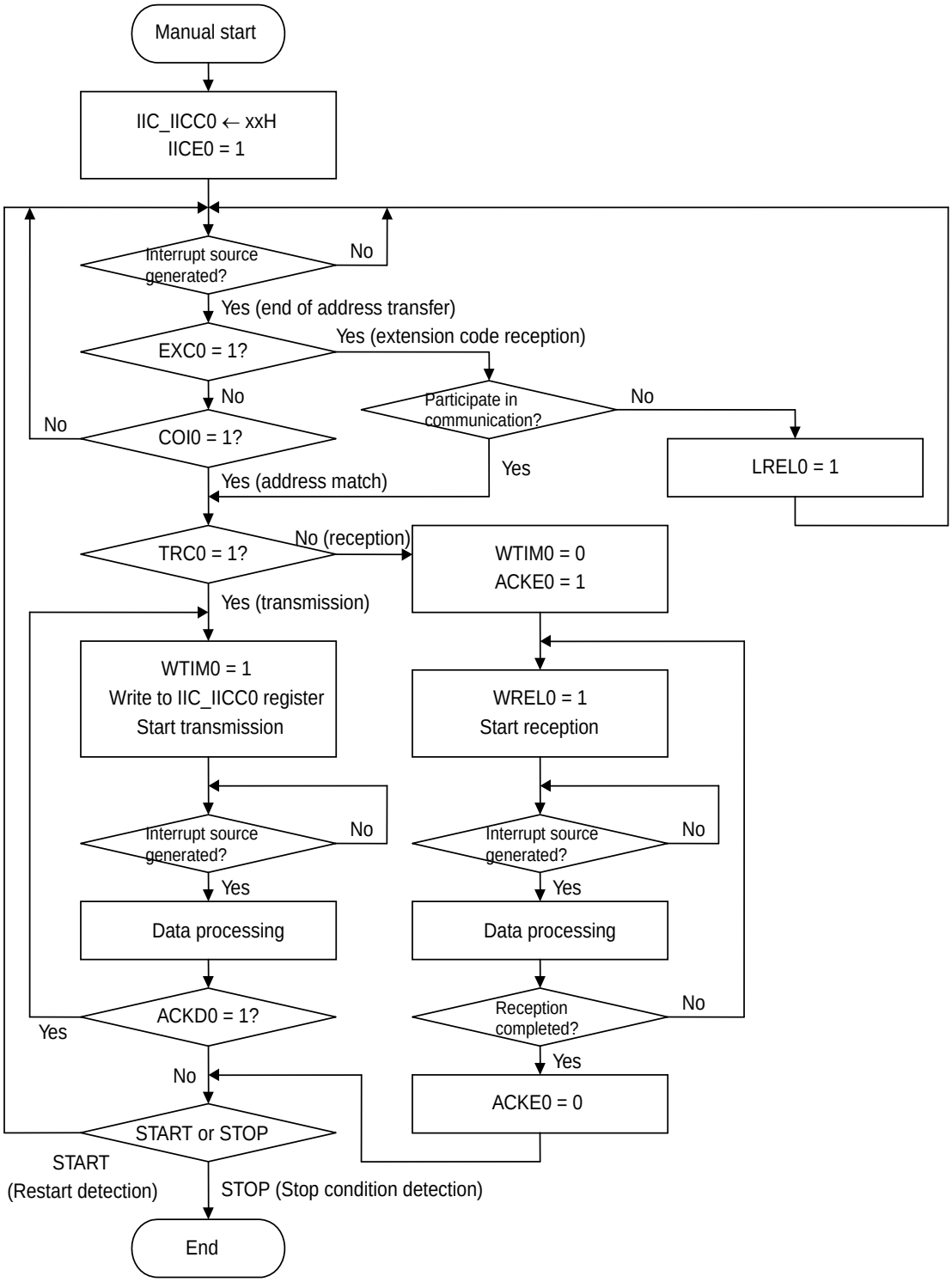
Figure 4-18. Start with Communication Reservation Disabled and Stop Condition Undetected



4.9.2 Slave operation

Figure 4-19 shows the communication procedure for slave operation.

Figure 4-19. Communication Procedure (Slave Operation)



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		Page	Summary
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2.00	Jun 7, 2010	—	Incremental update from comments to the 1.0.
3.00	Dec 28, 2010	—	Incremental update from comments to the 2.0. (A change part from 2.0 is "★" marked in the page left end.)
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Colophon 1.1

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