User's Manual

UART Interface

User's Manual

Multimedia Processor for Mobile Applications
EMMA Mobile ™ EV2

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the EMMA Mobile EV2. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Data Sheet	Hardware overview and electrical characteristics	EMMA Mobile EV2 Datasheet	R19DS0010EJxxxx
User's manual (1chip)	Hardware whole specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description	EMMA Mobile EV2 User's manual 1chip	R19UH0036EJxxxx
User's manual (module)	Hardware each macro specifications and operation description.	EMMA Mobile EV2 User's manual each module	See below

Document Name	Document No.	Document Name	Document No.
1chip	R19UH0036EJxxxx	DMA Controller	R19UH0043EJxxxx
System Management Unit	R19UH0037EJxxxx	LP-DDR/DDR2 Controller	R19UH0039EJxxxx
Timer	R19UH0054EJxxxx	SD Memory Card Interface	R19UH0061EJxxxx
System Timer	R19UH0055EJxxxx	SDIO Interface	R19UH0042EJxxxx
HD Video Decoder	R19UH0056EJxxxx	CF Card Interface	R19UH0062EJxxxx
Rotator	R19UH0057EJxxxx	Unified Serial Interface	R19UH0047EJxxxx
Resizer	R19UH0058EJxxxx	UART interface (This manual)	R19UH0040EJxxxx
Image Composer	R19UH0038EJxxxx	USB 2.0 Host Controller	R19UH0045EJxxxx
LCD Interface	R19UH0044EJxxxx	USB 2.0 Function Controller	R19UH0034EJxxxx
ITU-R BT.656 Interface	R19UH0059EJxxxx	IIC Interface	R19UH0052EJxxxx
Digital Terrestrial TV Interface	R19UH0048EJxxxx	General Purpose I/O Interface	R19UH0041EJxxxx
Camera Interface	R19UH0060EJxxxx	Pulse Width Modulation Interface	R19UH0063EJxxxx

4 digits of end shows the version.

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names

Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.

Examples the PM03 bit in the PM0 register

P3_5 pin, VCC pin

(2) Notation of Numbers

The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.

Examples Binary: 11b or 11

Hexadecimal: EFA0h

Decimal: 1234

3. Register Notation

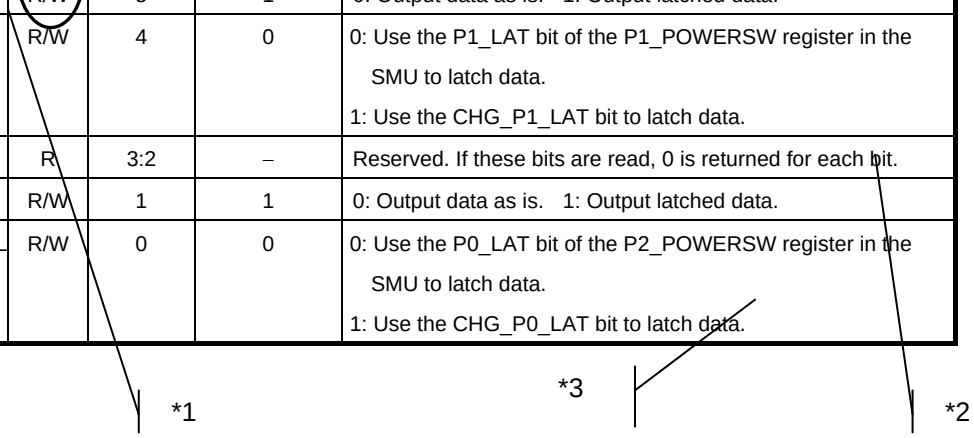
The symbols and terms used in register diagrams are described below.

x.x.x XXX register

This register (XXXXXXX: xxxx_xxxxh) …..

7	6	5	4	3	2	1	0
Reserved		CHG_P1_LAT	LATCH_P1_SEL	Reserved		CHG_P0_LAT	CHG_P0_LAT_SEL

Name	R/W	Bit No.	After Reset	Description
LATCH_P2_SEL	R/W	8	0	0: Use the P2_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P2_LAT bit to latch data.
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P1_LAT	R/W	5	1	0: Output data as is. 1: Output latched data.
LATCH_P1_SEL	R/W	4	0	0: Use the P1_LAT bit of the P1_POWERSW register in the SMU to latch data. 1: Use the CHG_P1_LAT bit to latch data.
Reserved	R	3:2	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P0_LAT	R/W	1	1	0: Output data as is. 1: Output latched data.
CHG_P0_LAT_SEL	R/W	0	0	0: Use the P0_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P0_LAT bit to latch data.



*1

R/W: Read and Write.

R: Read only.

W: Write only.

-: Nothing is assigned.

*2

Reserved bit.

Reserved bit. Set to specified value.

*3

・ Nothing is assigned.

Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.

・ Do not set to a value.

Operation is not guaranteed when a value is set.

・ Function varies according to the operating mode.

The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Register
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

Table of Contents

1. Overview

The UART block incorporated in EM/EV has two 64-byte FIFO buffers, one for transmission and one for reception, and is compatible with TL16C750, a general-purpose UART chip.

1.1 Features

- Four UART blocks: UART0, UART1, UART2 and UART3.
- Two 64-byte FIFO buffers, one for transmission and one for reception
  The following operating modes are available:
  - Non-FIFO mode (16450 mode)
  - 16-byte FIFO mode (16550 mode)
  - 64-byte FIFO mode
- Programmable auto-RTS and auto-CTS
- Standard asynchronous communication control bits (start, stop, and parity bits) can be added to or deleted from transmitted and received serial data. The following items can be specified:
  - Character length: 5, 6, 7 or 8 bits
  - Parity bit: Even parity, odd parity, or no parity bit
  - Stop bit: 1 or 2 bits
  - Baud rate: Reference clock frequency division ratio selectable from 1 to $(2^{16} - 1)$
- Modem control interface (CTS, RTS) (Only UART1 supports flow control.)

1.2 I/O Signals

The following signals are used for UART communication.

- UARTx_SIN: UARTx data input (external pins)
- UARTx_SOUT: UARTx data output (external pins)
- UART1_CTSB: UART1 transmission enable input (low active) (external pins)
- UART1_RTSB: UART1 transmission request output (low active) (external pins)

Remark x = 0 to 3

2. Pin functions

Pin Name	I/O	After Reset	Function	Alternate Pin Function
UART0_RX	Input	–	Serial data	–
UART0_TX	Output	0	Serial data	–
UART1_RX	Input	–	Serial data	GPIO_155
UART1_TX	Output	0	Serial data	GPIO_156
UART1_CTSB	Input	–	Prepared to transmit or receive connected device data	UART2_RX GPIO_157
UART1_RTSB	Output	0	Prepared to transmit or receive data	UART2_TX GPIO_158
UART2_RX	Input	–	Serial data	UART1_CTSB GPIO_157
UART2_TX	Output	0	Serial data	UART1_RTSB GPIO_158
UART3_RX	Input	–	Serial data	GPIO_046
UART3_TX	Output	0	Serial data	GPIO_047

3. Registers

UART register addresses use half-word boundaries.

3.1 Register List

Do not access reserved registers. The value 0000_0000H is returned for a read access.
Do not write any value other than 0 to the reserved bits in each register.

Base addresses: E102_0000H (UART0), E103_0000H (UART1), E104_0000H (UART2) , E105_0000H (UART3)

Address	Register Name	Register Symbol	R/W	Access unit	After Reset
0000H	Receive buffer register	RBR	R	16bit Note3	Undefined
	Transmit hold register	THR	W	16bit Note3	
0004H	Interrupt enable register	IER	R/W	32bit	0000H
0008H	Interrupt identification register	IIR	R	32bit	0001H
000CH	FIFO control register	FCR	R/W	32bit	0000H
0010H	Line control register	LCR	R/W	32bit	0000H
0014H	Modem control register	MCR	R/W	32bit	0000H
0018H	Line status register	LSR	R	32bit	0060H
001CH	Modem status register	MSR	R	32bit	00xxH Note 1
0020H	Scratch register	SCR	R/W	32bit	0000H
0024H	Divisor latch LS byte register	DLL	R/W Note 2	32bit	0000H
0028H	Divisor latch MS byte register	DLM	R/W Note 2	32bit	0000H
002CH	Hardware control register	HCR0	R/W	32bit	0000H
0030H	Hardware status register 2	HCR2	R	32bit	0000H
0034H	Hardware status register 3	HCR3	R	32bit	0000H
0038H to FFFCH	Reserved	–	–	–	–

Notes 1. Differs depending on the condition of the connected device.

2. Bit 7 (DLAB) of the LCR register must be set to 1 before setting up the DLL and DLM registers. The DLAB bit must be set to 0 after writing to the DLL and DLM registers. For details, see **3.2.5 Line control register**.

3. At FIFO mode.

Caution: Refer to following address of the System Management Unit User's Manual (R19UH0037EJ) about reset control.

0x0094 USIAU0_RSTCTRL
0x00AC USIBU1_RSTCTRL
0x00B0 USIBU2_RSTCTRL
0x00B4 USIBU3_RSTCTRL

3.2 Register Details

3.2.1 Receive buffer/ transmit hold register

This register (RBR/THR: E102_0000H (UART0), E103_0000H (UART1), E104_0000H (UART2), E105_0000H (UART3)) is used to read received data and write data to transmit.
This register functions as the receive buffer register (RBR) when read, or as the transmit hold register (THR) when written. In FIFO mode (bit 0 of FCR register = 1), the FIFO buffers are accessed.

15	14	13	12	11	10	9	8
0/D7	0/D6	0/D5	0/D4	0/D3	0/D2	0/D1	0/D0

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Name	R/W	Bit No.	After Reset	Function
0/D[7:0]	R	15:8	Undefined	Reads received data in 2-byte units. These bits are not used for 1-byte access. Zeroes are returned.
	W			Writes data to transmit in 2-byte units. These bits are not used for 1-byte access. Writing is ignored.
D[7:0]	R	7:0	Undefined	Reads received data.
	W			Stores data to transmit.

Operation in non-FIFO mode (bit 0 of FCR register = 0)
Received data is read out by reading this register, and data written to this register is stored as data to transmit.
Data of the lowest bit (D0) is transmitted or received first.
Only the lower bytes (D[7:0]) are used. This register can be accessed in byte units via the host bus interface. If this register is accessed in 2-byte units in non-FIFO mode, the higher bytes (0/D[7:0]) become invalid (all zeros returned when read, ignored when written) and only the lower bytes are used.

Operation in FIFO mode (bit 0 of FCR register = 1)
Received data is read out from the receive FIFO by reading this register, and data written to this register is stored into the transmit FIFO as data to transmit. This register can be accessed in 1- or 2-byte units via the host bus interface. Data of the lowest bit (D0) is transmitted or received first.
If this register is read in byte units, all zeros are returned from the higher bytes (0/D[7:0]) and data in the lower bytes (D[7:0]) becomes valid. If this register is written, the higher bytes become invalid and only the lower bytes are used.

The FIFO capacity is selected by using bit 5 of the FCR register.
The 16-byte FIFO mode is selected (16550 mode) by setting bit 5 of the FCR register to 0, and the 64-byte FIFO mode is selected by setting bit 5 of the FCR register to 1.

Cautions **1. If data is written to the transmit FIFO when it is full or if 2-byte data is written to the transmit FIFO when only 1 byte of space is available, an overrun error occurs and no data is written to the transmit FIFO. When an overrun error occurs, bit 7 of the HCR3 register is set to 1.**

2. When data is read from the empty receive FIFO or if the reading of 2-byte data from the receive FIFO is attempted when only 1 byte of data is stored, an underrun error occurs and data is not read from the receive FIFO. (All zeros are output to the host bus interface.) When an underrun error occurs, bit 7 of the HCR2 register is set to 1.

3. If the number of transmitted or received data bits is 5 to 7 bits, data in the lower bits is transmitted or received and bits exceeding the specified transfer bit count are discarded.

Example When the transfer bit count is set to 5 (bits 1 and 0 (WLS) of LCR register = 00b):
On the transmission side, data of bits 7 to 5 is discarded and data of bits 4 to 0 is transmitted.
On the reception side, “0” is written to bits 7 to 5 and valid data is written to bits 4 to 0.

3.2.2 Interrupt enable register

This register (IER: E102_0004H (UART0), E103_0004H (UART1), E104_0004H (UART2), E105_0004H (UART3)) enables the issuance of interrupt requests. Each interrupt can be set up individually for each interrupt source.

The interrupt sources corresponding to bits to which 1 is written are enabled.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				EDSSI	ELSI	ETBEI	ERBI

Name	R/W	Bit No.	After Reset	Function
Reserved	R	15:8	00H	Reserved. When these bits are read, 0 is returned for each bit.
Reserved	R/W	7:4	0H	Reserved. Written data is ignored.
EDSSI	R/W	3	0	Specifies whether to enable the modem status interrupt. 0: Disables the modem status interrupt. 1: Enables the modem status interrupt.
ELSI	R/W	2	0	Specifies whether to enable the reception error (receiver line status) interrupt. 0: Disables the reception error interrupt. 1: Enables the reception error interrupt.
ETBEI	R/W	1	0	Specifies whether to enable the transmit buffer empty (transmit hold register (THR) empty) interrupt. 0: Disables the transmit buffer empty interrupt. 1: Enables the transmit buffer empty interrupt.
ERBI	R/W	0	0	Specifies whether to enable the reception completion (received data available) and timeout interrupts. 0: Disables the reception completion and timeout interrupts. 1: Enables the reception completion and timeout interrupts.

Caution By setting bit 0 to "0", reception completion and timeouts can be excluded from the interrupt sources. However, when bit 4 of the HCR0 register is set to 1 (receiver timeout DMA REQ disable), a timeout error is added to the interrupt sources, regardless of the setting of bit 0.

Remark A timeout error is detected when either of the following conditions is satisfied while the FIFO stores at least one character:

<1> The most recent serial character is received before at least the four continuous character times.

<2> The host read the FIFO most recently before four continuous character times.

Four continuous character times is equivalent to four characters of a 12-bit received character (start: 1 bit, data: 8 bits, parity: 1 bit, stop: 2 bits), that is, 768 cycles (for a 16× clock) (12 × 4 × 16 = 768 cycles (for a 16× clock)).

3.2.3 Interrupt identification register

This register (IIR: E102_0008H (UART0), E103_0008H (UART1), E104_0008H (UART2), E105_0008H (UART3)) is used to identify interrupt sources.

The FIFO operating mode and interrupt sources can be checked by reading this register.

When multiple interrupts sources are generated, the interrupt source that has the highest priority is output to this register.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
FIFOs Enabled[1:0]		64 Byte FIFO Enabled	Reserved	Interrupt ID[3:0]			

Name	R/W	Bit No.	After Reset	Function
Reserved	R	15:8	00H	Reserved. When these bits are read, 0 is returned for each bit.
FIFOs Enabled[1:0]	R	7:6	00b	Indicates the FIFO operating mode. 00b: Non-FIFO mode (16450 mode) 11b: 16-byte/64-byte FIFO mode (See bit 5.)
64 Byte FIFO Enabled	R	5	0	Indicates the FIFO operating mode. This bit is enabled when bits 7 and 6 are set to 11b. 0: 16-byte FIFO mode (16550 mode) 1: 64-byte FIFO mode
Reserved	R	4	0	Reserved. When this bit is read, 0 is returned.
Interrupt ID[3:0]	R	3:0	0001b	Among the interrupts that have occurred, these bits indicate the ID of the interrupt source that has the highest priority.

Table 3-1. FIFO Operating Mode (Bits 7 to 5)

Bits 7 to 5	FIFO Operating Mode
000	Non-FIFO mode (16450 mode)
110	16-byte FIFO mode (16550 mode)
111	64-byte FIFO mode

Table 3-2. Interrupt Indication and Prioritization of Interrupt Sources (Bits 3 to 0 of IIR)

IIR[3:0]	Priority	Interrupt Type	Interrupt Source	Interrupt Reset Method
0001 (1H)	None	None	None	None
0110 (6H)	1	Reception error (receiver line status)	When at least one of the following occurs: • Overrun • Parity error • Framing error • Break interrupt	When the line status register (LSR) is read
0100 (4H)	2	Reception completion (received data available)	• In non-FIFO mode When data reception in the receive buffer register is completed • In FIFO mode When the amount of data in the receive FIFO exceeds the trigger level	• In non-FIFO mode When the receive buffer register (RBR) is read • In FIFO mode When the receive FIFO is read and the amount of data in the receive FIFO becomes less than the trigger level
1100 (CH)		Timeout	When data reception timed out while the receive FIFO was used	When the receive FIFO is read
0010 (2H)	3	Transmit buffer empty (transmit hold register (THR) empty)	Transmit hold register (THR) or transmit FIFO is empty	When the IIR register is read or data is written in the transmit hold register (THR) or transmit FIFO
0000 (0H)	4	Modem status	When at least one of the following occurs: • △CTS • △DSR (internal signal) • △DCD (internal signal) • Trailing edge RI (internal signal)	When the modem status register (MSR) is read

Caution A transmit buffer empty interrupt (bits 3 to 0 of IIR register = 0010) is canceled by reading the IIR register or writing data to the transmit hold register (THR) or transmit FIFO. Specifically, the following operation is performed for reading the IIR register.

If the transmit buffer is empty when the IIR register is read to check the interrupt source, the read operation masks the transmit buffer empty interrupt and this interrupt no longer occurs. This masking is canceled when data is written to the transmit buffer, and the subsequent transmit buffer empty interrupts are output.

3.2.4 FIFO control register

This register (FCR: E102_000CH (UART0), E103_000CH (UART1), E104_000CH (UART2), E105_000CH (UART3)) controls the transmit/receive FIFO.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Receiver Trigger		64 Byte FIFO Enabled	Reserved	DMA Mode Select	Transmitter FIFO Reset	Receiver FIFO Reset	FIFO Enable

Name	R/W	Bit No.	After Reset	Function
Reserved	R	15:8	00H	Reserved. When these bits are read, 0 is returned for each bit.
Receiver Trigger *	R/W	7:6	00b	Valid only in FIFO mode (bit 0 of FCR register = 1). Specifies the threshold (trigger level) of data stored in the receive FIFO in order to issue an interrupt request or a reception DMA request. • In 16-byte FIFO mode (bit 5 of FCR register = 0) 00: 1 byte 01: 4 bytes 10: 8 bytes 11: 14 bytes • In 64-byte FIFO mode (bit 5 of FCR register = 1) 00: 1 byte 01: 16 bytes 10: 32 bytes 11: 56 bytes
64 Byte FIFO Enable *	R/W	5	0	Valid only in FIFO mode (bit 0 of FCR register = 1). Specifies the FIFO capacity. 0: 16 bytes (16550 mode) 1: 64 bytes
Reserved	R/W	4	0	Reserved. Written data is ignored.
DMA Mode Select *	R/W	3	0	Specifies the DMA mode in FIFO mode. The DMA mode is specified by setting this bit with bits 3 and 2 of the HCR0 register.
Transmitter FIFO Reset	R/W	2	0	Setting this bit to 1 generates a synchronization reset pulse (1 VBCLK cycle) and resets the transmit FIFO and FIFO address counter. This bit is automatically reset to 0. **Caution The transmit shift register (TSR) is not reset. If a reset occurs during transmission, one frame that has only zeros might be transmitted after the data in the TSR register has been transmitted.**
Receiver FIFO Reset	R/W	1	0	Setting this bit to 1 generates a synchronization reset pulse (1 VBCLK cycle) and resets the receive FIFO and FIFO address counter. This bit is automatically reset to 0. **Caution The receive shift register (RSR) is not reset. If a reset occurs during reception, data being received is correctly stored in the receive FIFO after the reset.**
FIFO Enable *	R/W	0	0	Selects the FIFO operating mode. 0: Non-FIFO mode (16450 mode) 1: 16-/64-byte FIFO mode (selected by bit 5 of the FCR register)

* If a register value is changed during operation, normal operation is not guaranteed. In this case, initialize the register.

Table 3-3. Reception Trigger Level Settings (Bits 7 and 6 of FCR)

Bits 7 to 6 of IIR	16-byte FIFO Mode (Bit 5 of FCR Register = 0) Trigger Level (Bytes)	64-byte FIFO Mode (Bit 5 of FCR Register = 1) Trigger Level (Bytes)
00	01	01
01	04	16
10	08	32
11	14	56

Table 3-4. DMA Mode Settings (Bit 3 of FCR and Bits 3 and 2 of HCR0)

Bit 3 of FCR register	Bits 3 and 2 of HCR0	Receive DMA Request	Transmit DMA Request
0	00	Mode 0	
1	00	Mode 1	
0	01	Mode 0	Mode 1
1	10	Mode 1	Mode 0
Others (Setting prohibited)		–	–

Table 3-5. DMA Modes and DMA Request Generation Conditions

Mode		DMA Request Generation Condition	DMA Request Release Condition
When the DMA access data width is one byte (bit 5 of HCR0 = 0)			
Receive DMA request	Mode 0	The receive FIFO stores 1 or more bytes of data.	The receive FIFO is empty.
	Mode 1	The amount of data in the receive FIFO reached the trigger level or a timeout event occurred[Note 1].	The receive FIFO is empty.
Transmit DMA request	Mode 0	The transmit FIFO is empty.	The transmit FIFO stores 1 or more bytes of data.
	Mode 1	The transmit FIFO is empty.	The transmit FIFO is full.
When the DMA access data width is two bytes (bit 5 of HCR0 = 1).			
Receive DMA request	Mode 0	The receive FIFO stores 2 or more bytes of data.	The receive FIFO stores 1 or fewer bytes of data[Note 2].
	Mode 1	The trigger level is reached or a timeout event occurs[Note 1] when the receive FIFO stores 2 or more bytes of data.	The receive FIFO stores 1 or fewer bytes of data[Note 2].
Transmit DMA request	Mode 0	The transmit FIFO is empty.	The transmit FIFO stores 2 or more bytes of data.
	Mode 1	The transmit FIFO is empty.	The transmit FIFO full

Notes **1.** The timeout event can be excluded from the reception DMA request issue conditions by setting bit 4 of the HCR0 register.

Bit 4 = 0: The timeout event is included in the reception DMA request issue conditions.

Bit 4 = 1: The timeout event is excluded from the reception DMA request issue conditions and added to the interrupt sources.

2. If an odd number of data bytes is received in the 2-byte access mode, the reception DMA request is canceled when the amount of data remaining in the receive FIFO becomes 1 byte. When receiving an odd number of data bytes, use 1-byte access or notify the timeout event by using an interrupt (bit 4 of HCR0 register = 1) and read the timeout data by servicing the interrupt.

Caution In the non-FIFO mode, operation equivalent to mode 0 is performed regardless of the settings of bit 3 in the FCR register and bits 3 and 2 in the HCR0 register.

- **A reception DMA request is issued when receiving 1-byte data in the receive buffer register is completed. The request is canceled when the receive buffer register is empty.**
- **A transmission DMA request is issued when the request transmit buffer is empty. The request is canceled when at least 1-byte data is stored in the transmit buffer.**

3.2.5 Line control register

This register (LCR: E102_0010H (UART0), E103_0010H (UART1), E104_0010H (UART2), E105_0010H (UART3)) specifies the transmission/reception data format and enables access to the divisor latch.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
DLAB	Break Control	Stick Parity	EPS	PEN	STB	WLS[1:0]	

(1/2)

Name	R/W	Bit No.	After Reset	Function
Reserved	R	15:8	00H	Reserved. When these bits are read, 0 is returned for each bit.
DLAB *	R/W	7	0	Setting this bit to 1 enables specifying the divisor latch (DLM/DLL registers). When this bit is set to 0 after specifying the divisor latch, access to the divisor latch is prohibited and generation of the 16x clock according to the specified value is started by the baud rate generator. **Caution The 16x clock stops after a master reset. The baud rate generator starts generating the 16x clock when it detects the change of this bit setting (from 1 to 0). After generation starts, the 16x clock will not stop unless a master reset is input.**
Break Control	R/W	6	0	Controls break state generation and transmission. The serial output (UARTx_SOUT) is forcibly set to 0 while this bit is set to 1, and such output is canceled when this bit is set to 0. This bit directly controls the SOUT output level but does not affect the internal circuits. **Caution If this bit is set to 1 during transmission, only framing errors might be detectable on the reception side. To detect breaks for sure, this bit must be set when transmission has completed (the transmit buffer empty).**
Stick Parity *	R/W	5	0	Selects the type of parity bit used to verify transmitted/received data. The setting of this bit is valid only when a parity bit is used (bit 3 = 1). An even, odd, or fixed value (high or low) is set by using bit 4. 0: Parity check using an even or odd parity bit 1: Parity check using a stick parity bit
EPS *	R/W	4	0	Selects the odd or even parity when bit 3 is set to 1 and bit 5 is set to 0. Selects the level of the stick parity when bit 3 and bit 5 are set to 1. 0: Odd parity / Stick High (fixed to 1) 1: Even parity / Stick Low (fixed to 0)
PEN *	R/W	3	0	Specifies whether to enable the parity check. 0: No parity bit. 1: Adds a parity bit on the transmission side. The parity bit is checked on the reception side.

(2/2)

Name	R/W	Bit No.	After Reset	Function
STB *	R/W	2	0	Specifies the number of stop bits to add to data transferred via serial transmission. 0: 1 bit 1: 2 bits Only the first stop bit is checked on the reception side, regardless of this setting.
WLS[1:0] *	R/W	1:0	00b	Specifies the length of data transferred via serial transmission and reception. 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits

* If a register value is changed during operation, normal operation is not guaranteed. In this case, initialize the register.

Table 3-6. Parity Type Settings (Bits 5 to 3 of LCR)

Bits 5 to 3 of LCR	Parity Type
xx0	No parity
001	Odd parity
011	Even parity
101	Stick High (fixed to “1”)
111	Stick Low (fixed to “0”)

xx: Don’t Care

Table 3-7. Settings for Transmission/Reception Data Length (Bits 1 and 0 of LCR)

WLS[1:0] of LCR	Data Length
00	5 bits
01	6 bits
10	7 bits
11	8 bits

3.2.6 Modem control register

This register (MCR: E103_0014H (UART1)) controls the interface with modems (and other peripheral devices).

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved		AFE	Reserved	OUT2	OUT1	RTS	DTR

Name	R/W	Bit No.	After Reset	Function
Reserved	R	15:8	00H	Reserved. When these bits are read, 0 is returned for each bit.
Reserved	R	7:6	0H	Reserved. Written data is ignored.
AFE *	R/W	5	0	Specifies whether to enable auto-flow control (auto-CTS and auto-RTS). 0: Disables auto-flow control. 1: Enables auto-flow control. Auto-flow operation is controlled in detail by using bit 1 of this register and bit 6 of the HCR0 register.
Reserved	R/W	4	0	Reserved.
OUT2	R/W	3	0	Selects the level of the general-purpose output OUT2Z (internal signal). 0: High (inactive). 1: Low (active) In local loopback mode, this bit controls DCDZ (internal signal) input.
OUT1	R/W	2	0	Selects the level of the general-purpose output OUT1Z (internal signal). 0: High (inactive) 1: Low (active) In local loopback mode, this bit controls RIZ (internal signal) input.
RTS	R/W	1	0	Selects the level of UARTx_RTSB pin output (transmission request) when auto-RTS is not used (bit 5 = 0). 0: High (inactive) 1: Low (active) In local loopback mode, this bit controls the UARTx_CTSB input pin.
DTR	R/W	0	0	Selects the level of DTRZ (communication link establishment ready, internal signal) output. 0: High (inactive) 1: Low (active) In local loopback mode, this bit controls DSRZ (internal signal) input.

* If a register value is changed during operation, normal operation is not guaranteed. In this case, initialize the register.

Table 3-8. Auto-Flow Settings (Bits 5 and 1 of MCR and Bit 6 of HCR0)

Bit 5 of MCR Register	Bit 1 of MCR Register	Bit 6 of HCR0 Register	Auto-CTS	Auto-RTS
1	1	0	○	○ (Auto-RTS mode 0)
		1	○	○ (Auto-RTS mode 1)
	0	×	○	– (RTSZ output is fixed to high level.)
0	×	×	–	–

Auto-CTS operation:

While the CTSZ pin is pulled low (requesting transmission), data in the transmit buffer (THR/transmit FIFO) is transmitted. The transmission stops when the pin is pulled high. If the CTSZ pin is pulled high during transmission, data being transmitted (the data that remains in the transmit shift register) is transmitted and transmission stops.

Auto-RTS operation (valid only in the FIFO mode):

Auto-RTS mode 0

When the amount of data in the receive FIFO reaches the trigger level, the RTSZ pin is pulled high (requesting that transmission be stopped). When the data in the receive FIFO is read and the FIFO empties, the pin is pulled low (requesting transmission).

Auto-RTS mode 1

- In the 16-byte FIFO mode, the RTSZ pin is pulled high when the amount of data in the receive FIFO reaches 14 bytes, and the pin is pulled low when the amount of data becomes 13 bytes or less.
- In the 64-byte FIFO mode, the RTSZ pin is pulled high when the amount of data in the receive FIFO reaches 56 bytes, and the pin is pulled low when the amount of data becomes 55 bytes or less.

Caution
- **When auto-flow control is not used, flow control is not performed by hardware. Therefore, CTS monitoring and RTS control must be performed by software to prevent a FIFO overrun.**
- **When auto-flow is not used (bit 5 of MCR register = 0): Bit 1 of the MCR register is used to control the RTSZ output (the value set to bit 1 is reversed and the reversed level is output to RTSZ).**
- **When both a modem status interrupt (bit 3 of IER register = 1) and auto-CTS are set, auto-CTS is disabled.**
- **In the non-FIFO mode, auto-RTS is disabled.**

3.2.7 Line status register

This register (LSR: E102_0018H (UART0), E103_0018H (UART1), E104_0018H (UART2), E105_0018H (UART3)) is used to check the status of transmission and reception.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Error in Receiver FIFO	TEMT	THRE	BI	FE	PE	OE	DR

(1/2)

Name	R/W	Bit No.	After Reset	Function
Reserved	R	15:8	00H	Reserved. When these bits are read, 0 is returned for each bit.
Error in Receiver FIFO	R	7	0	A zero is always read from this bit in non-FIFO mode. This bit is set to "1" when a break interrupt error, parity error, or framing error occurs in data read from the receive FIFO in FIFO mode. Reading this register clears this bit to “0”.
TEMT	R	6	1	This bit is set to "1" when the transmit buffer (the THR register or transmit FIFO) and transmit shift register (TSR) empty. This bit is cleared to "0" when data is written to the transmit buffer or transmit shift register.
THRE	R	5	1	This bit is set to "1" when the transmit buffer (THR register or transmit FIFO) empties. This bit is cleared to "0" when at least 1 byte of data is written to the transmit buffer.
BI *	R	4	0	This bit is set to “1” when a break interrupt occurs. Reading this register clears this bit to “0”. A break interrupt is detected when a low level signal is received for 1 frame or longer (for the total of the start bit, data stop bit, and stop bit). When a start bit (low level) is detected, the receive block assumes that data has been sent, and receives the data. While a break interrupt is being acknowledged (a low level signal is being input), the receive block continues to receive all zeros. (Reception stops when an overrun occurs.) In FIFO mode, the break interrupt information is stored in the receive FIFO with all-0 data. A break interrupt is detected when the data is read. **Caution A framing error always occurs when a break interrupt is detected. A parity error might occur, depending on the settings of bits 5 to 3 of the LCR register.**

(2/2)

Name	R/W	Bit No.	After Reset	Function
FE *	R	3	0	This bit is set to “1” when a framing error is detected in received data. Reading this register clears this bit to “0”. A framing error occurs when the first stop bit following the data bit or parity bit of received data is checked and it is judged to be invalid (low level). In FIFO mode, the framing error information is stored in the receive FIFO with the receive data. A framing error is detected when the data is read.
PE *	R	2	0	This bit is set to “1” when a parity error is detected in received data. Reading this register clears this bit to “0”. In FIFO mode, the parity error information is stored in the receive FIFO with the received data. A parity error is detected when the data is read.
OE *	R	1	0	This bit is set to “1” when a receive overrun error is detected. Reading this register clears this bit to “0”. A receive overrun occurs when the receive buffer register (RBR) or receive FIFO is filled with received data, data is held in the receive shift register (RSR), and the start bit of the following data is detected. When a receive overrun error occurs, received data will no longer be stored in the receive buffer register or receive FIFO. Data held in the receive shift register is stored in the receive buffer when a vacancy becomes available.
DR	R	0	0	This bit is set to "1" when at least 1 byte of received data is stored in the receive buffer register (RBR) or receive FIFO. This bit is cleared to "0" when all of the received data is read and the receive buffer empties.

* Do not poll these bits to check the interrupt source. Instead, check the source after the interrupt is detected.

3.2.8 Modem status register

This register (MSR: E103_001CH (UART1)) is used to check the control signals connected to modems (or other peripheral devices).

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
DCD	RI	DSR	CTS	⊿DCD	TERI	⊿DSR	⊿CTS

Name	R/W	Bit No.	After Reset	Function
Reserved	R	15:8	00H	Reserved. When these bits are read, 0 is returned for each bit.
DCD *	R	7	Undefined	Indicates the inverted level of DCDZ (internal signal) input. 0: High (inactive) 1: Low (active) In local loopback mode, the value set to bit 3 (OUT2) of the MCR register is read.
RI *	R	6	Undefined	Indicates the inverted level of RIZ (internal signal) input. 0: High (inactive) 1: Low (active) In local loopback mode, the value set to bit 2 (OUT1) of the MCR register is read.
DSR *	R	5	Undefined	Indicates the inverted level of DSRZ (internal signal) input. 0: High (inactive) 1: Low (active) In local loopback mode, the value set to bit 0 (DTR : internal signal) of the MCR register is read.
CTS *	R	4	Undefined	Indicates the inverted level of UARTx_CTSB pin input. 0: High (inactive) 1: Low (active) In local loopback mode, the value set to bit 1 (RTS) of the MCR register is read.
⊿DCD *	R	3	Undefined	This bit is set to 1 when the level of the DCDZ (internal signal) input changes (from high to low or low to high). Reading this register clears this bit to “0”.
TERI *	R	2	Undefined	This bit is set to 1 when the RIZ (internal signal) input is pulled high (inactive). Reading this register clears this bit to “0”.
⊿DSR *	R	1	Undefined	This bit is set to 1 when the level of the DSRZ (internal signal) input changes (from high to low or low to high). Reading this register clears this bit to “0”.
⊿CTS *	R	0	Undefined	This bit is set to 1 when the level of the UARTx_CTSB pin input changes (from high to low or low to high). Reading this register clears this bit to “0”.

* Do not poll these bits to check the interrupt source. Instead, check the source after the interrupt is detected.

3.2.9 Scratch register

This register (SCR: E102_0020H (UART0), E103_0020H (UART1), E104_0020H (UART2), E105_0020H (UART3)) can be used freely during programming.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Scratch Register							

Name	R/W	Bit No.	After Reset	Function
Reserved	R	15:8	00H	Reserved. When these bits are read, 0 is returned for each bit.
Scratch Register	R/W	7:0	00H	These bits do not affect the UART operation and can be used freely during programming.

3.2.10 Divisor latch LS byte register

This register (DLL: E102_0024H (UART0), E103_0024H (UART1), E104_0024H (UART2), E105_0024H (UART3)) specifies the lower 8 bits of the divisor for the baud rate generator. Set up this register in combination with the DLM register that specifies the higher 8 bits.

The baud rate generator divides the reference clock (XIN) and generates a 16× baud rate clock for the transmit and receive blocks by using the value specified in this register.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Divisor[7:0]							

Name	R/W	Bit No.	After Reset	Function
Reserved	R	15:8	00H	Reserved. When these bits are read, 0 is returned for each bit.
Divisor[7:0] *	R/W	7:0	00H	Specifies the lower 8 bits of the divisor. (“0” is setting prohibited.)

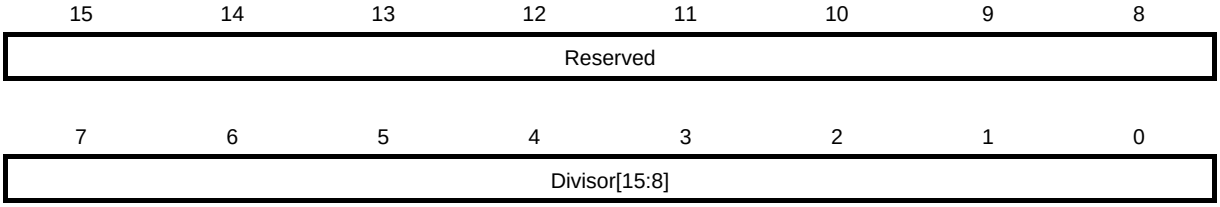
* If a register value is changed during operation, normal operation is not guaranteed. In this case, initialize the register.

Caution When the DLM and DLL registers are set up, bit 7 (DLAB) of the LCR register must be set to 1. The DLAB bit must be set to 0 after the DLM and DLL registers are written. For details, see 3.2.5 Line control register.

3.2.11 Divisor latch MS byte register

This register (DLM: E102_0028H (UART0), E103_0028H (UART1), E104_0028H (UART2), E105_0028H (UART3)) specifies the higher 8 bits of the divisor for the baud rate generator. Set up this register in combination with the DLL register that specifies the lower 8 bits.

The baud rate generator divides the reference clock (XIN) and generates a 16× baud rate clock for the transmit and receive blocks by using the value specified in this register.



Name	R/W	Bit No.	After Reset	Function
Reserved	R	15:8	00H	Reserved. When these bits are read, 0 is returned for each bit.
Divisor[15:8] *	R/W	7:0	00H	Specifies the higher 8 bits of the divisor. (“0” is setting prohibited.)

* If a register value is changed during operation, normal operation is not guaranteed. In this case, initialize the register.

Caution When the DLM and DLL registers are set up, bit 7 (DLAB) of the LCR register must be set to 1. The DLAB bit must be set to 0 after the DLM and DLL registers are written. For details, see 3.2.5 Line control register.

3.2.12 Hardware control register

This additional register (HCR0: E102_002CH (UART0), E103_002CH (UART1), E104_002CH (UART2), E105_002CH (UART3)) controls the DMA controller and other hardware.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
SW Reset	RTS Mode	DMA 2Byte Access Enable	Receiver timeout DMA Disable	Receiver DMA Mode	Transmitter DMA Mode	Receiver DMA Enable	Transmitter DMA Enable

Name	R/W	Bit No.	After Reset	Function
Reserved	R	15:8	00H	Reserved. When these bits are read, 0 is returned for each bit.
SW Reset	R/W	7	0	Setting this bit to 1 resets internal UART registers, except for registers for the transmit and receive FIFOs and baud rate generator (RBR/THR, DLL, and DLM). Setting this bit to 0 cancels the reset. **Caution Before executing a software reset, reset the transmit and receive FIFOs (bits 2 and 1 of FCR register). After that, registers other than the DLL and DLM registers must be set up again.**
RTS Mode	R/W	6	0	Selects the RTS mode when auto-RTS is used. (Only UART1 is effective for a RTS mode.) 0: Auto-RTS mode 0 1: Auto-RTS mode 1
DMA 2Byte Access Enable	R/W	5	0	Selects the width of data to transfer to the transmit and receive FIFOs via DMA. 0: 1 byte 1: 2 bytes This setting affects the conditions for generating DMA request signals.
Receiver timeout DMA Disable	R/W	4	0	Specifies whether to include the timeout event in the reception DMA transfer request sources. 0: Includes the timeout event in the reception DMA transfer request sources. 1: Excludes the timeout event from the reception DMA transfer request sources (and automatically adds it to the interrupt sources).
Receiver DMA Mode	R/W	3	0	Specifies the DMA request mode separately for transmission and reception. These bits are used with bit 3 of the FCR register.
Transmitter DMA Mode	R/W	2	0	
Receiver DMA Enable	R/W	1	0	Specifies whether to enable the reception DMA request output. 0: Disables reception DMA requests. 1: Enables reception DMA requests.
Transmitter DMA Enable	R/W	0	0	Specifies whether to enable the transmission DMA request output. 0: Disables transmission DMA requests. 1: Enables transmission DMA requests.

3.2.13 Hardware status register 2

This additional register (HCR2: E102_0030H (UART0), E103_0030H (UART1), E104_0030H (UART2), E105_0030H (UART3)) is used to check the receive FIFO status.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Receiver FIFO Underrun	Receiver FIFO Data Count[6:0]						

Name	R/W	Bit No.	After Reset	Function
Reserved	R	15:8	00H	Reserved. When these bits are read, 0 is returned for each bit.
Receiver FIFO Underrun	R	7	0	When data is read from the receive FIFO when it is empty or when reading of 2-byte data from the receive FIFO is attempted when only 1 byte is stored, an underrun error occurs and this bit is set to 1. Reading this register clears this bit to “0”. **Caution If an underrun error occurs, the receive FIFO is no longer read and all zeros are output to the host bus interface. No interrupt request is caused by an underrun error.**
Receiver FIFO Data Count[6:0]	R	6:0	0	Indicates the number of data items remaining in the receive FIFO.

3.2.14 Hardware status register 3

This additional register (HCR3: E102_0034H (UART0), E103_0034H (UART1), E104_0034H (UART2), E105_0034H (UART3)) is used to check the transmit FIFO status.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Transmitter FIFO Overrun	Transmitter FIFO Data Count[6:0]						

Name	R/W	Bit No.	After Reset	Function
Reserved	R	15:8	00H	Reserved. When these bits are read, 0 is returned for each bit.
Transmitter FIFO Overrun	R	7	0	When data is written to the transmit FIFO when it is full or when 2-byte data is written to the transmit FIFO when only 1 free byte space is available, an overrun error occurs and this bit is set to 1. Reading this register clears this bit to “0”. **Caution If an overrun error occurs, the transmit FIFO is no longer written. No interrupt request is caused by an overrun error.**
Transmitter FIFO Data Count[6:0]	R	6:0	00H	Indicates the number of data items remaining in the transmit FIFO.

4. Description of Functions

4.1 HCR0 software reset

Almost all UART interface registers are initialized by setting bit 7 of the HCR0 register to 1, except for the FIFOs.

4.2 Error detection when a FIFO is used

A parity error, framing error, and break interrupt are detected during reception and error information is concurrently stored in the FIFO with the data. Next, an interrupt is reported when data 1 byte or 2 bytes before the data that caused the error is read out. No break interrupt occurs when no start bit is detected (such as during frame data reception). However, the break interrupt can be detected in the non-FIFO mode. If the above errors are detected while a FIFO is used, the receive FIFO must be reset by using bit 1 of the FCR register to clear error information in the FIFO.

4.3 Interrupt signal (INTRPT)

After the INTRPT signal related to data transfer is pulled high, it stays at high level until the interrupt source is cleared. However, the transmit buffer empty interrupt is masked by reading the IIR register. The mask is disabled by writing data to transmit. After the transmit buffer empty interrupt is masked, it does not occur even if the transmit buffer is empty, as long as data to transmit is not written.

4.4 Serial clock generation

A serial clock is masked after a reset. The mask is disabled by setting up the baud rate registers (DLL and DLM) and then setting bit 7 (DLAB) of the LCR register to 0. Because the mask is disabled at the falling edge of the output of the DLAB bit setting, disabling the mask is valid only once after a reset. The masking can be specified only when hardware is reset.

4.5 Auto-flow mode is disabled when bit 3 of the IER register is set to 1

When the modem status interrupt is enabled,
auto-CTS : disabled
auto-RTS : enabled
To enable auto-flow mode, the modem status interrupt must therefore be disabled.
In auto-flow mode, the connected devices are also assumed to operate in auto-flow mode. If a connected device does not stop transmission by pulling RTSZ high, an overrun error occurs.

4.6 FIFO's

4.6.1 Operation in FIFO interrupt mode

The following interrupts occur while the receive FIFO interrupt is enabled (when bit 0 of the FCR register, bit 0 of the IER register, and bit 2 of the IER register are set to 1).

- When the amount of data in the receive FIFO reaches the trigger level, a receive data enable interrupt is issued. When the amount of data in the receive FIFO becomes less than the trigger level, the interrupt is cleared.
- The received data available interrupt is indicated in the IIR register when the receive FIFO reaches the trigger level.
- A receiver line status interrupt (IIR = 06H) has a higher priority than the received data available interrupt (IIR = 04H).
- When a character is transmitted to the receive FIFO from the receive shift register (RSR), bit 0 (DR) of the LSR register is set to 1. When the receive FIFO empties, the DR bit is cleared.

4.6.2 Operation in FIFO polled mode

When the FIFO is enabled (bit 0 of the FCR register = 1), bits 3 to 0 of the IER register are set to 0 in FIFO polled mode. Transmission and reception can then be set to FIFO polled mod separately.
In this mode, the user program checks the transmission and reception status by using the LSR register.
The immediately preceding statuses are:

Bit 0 of the LSR register is set to 1 when at least 1 byte is stored in the receive FIFO.
Bits 4 to 1 of the LSR register indicate details about the error occurrence.
Bit 5 of the LSR register indicates that the THR is empty.
Bit 6 of the LSR register indicates that both THR and TSR are empty.
Bit 7 of the LSR register indicates whether the receive FIFO contains some errors.

4.6.3 Read when the receive FIFO is empty

If the receive FIFO is read while it is empty, the read counter is not incremented.
In this case, a receive FIFO underrun error is detected (bit 7 of HCR2 register).

4.7 Interrupt Sources

The UART interface uses four interrupts.

Table 4-1. Interrupt Sources

Interrupt Name	Bit Assignment
Modem status interrupt	Bit 3 (EDSSI) of the IER register
Reception error (receiver line status) interrupt	Bit 2 (ELSI) of the IER register
Transmit buffer empty (transmit hold register (THR) empty) interrupt	Bit 1 (ETBEI) of the IER register
Reception error (received data available)/timeout interrupt	Bit 0 (ERBI) of the IER register

4.8 Clock

The following clock is used for the UART interface:

- USIA_U0_SCLK, USIB_U1_SCLK, USIB_U2_SCLK, USIB_U3_SCLK

5. Usage

5.1 Initialization Method

This section describes initial settings necessary for operating the UART interface.

(1) Baud rate settings and enabling 64-byte FIFO mode

Set bit 7 (DLAB) of the LCR register to 1 and specify a baud rate in the DLM and DLL registers.
After the above settings, LCR [7] is to set it in = 0, and generation of 16× clock is begun.

(2) FIFO mode settings

Specify whether to enable FIFO by using bit 0 of the FCR register.
Select a DMA mode by using bit 3 of the FCR register.
Select the 16- or 64-byte FIFO mode by using bit 5 of the FCR register.
Select the trigger level of the receive FIFO by using bits 7 and 6 of the FCR register. (This setting is not required for the non-FIFO mode.)

(3) Serial interface settings

Specify the length of frame data in bits by using bits 1 and 0 (WLS) of the LCR register.
Specify the number of stop bits by using bit 2 of the LCR register.
Select no parity, even parity, odd parity, or stick parity by using bits 5 to 3 of the LCR register.

(4) Modem interface settings

Set up flow control by using bits 5 and 1 of the MCR register.
When auto-flow control is not used, set bit 1 of the MCR register to 1 to assert the RTSZ output.
Next, set up the IER and HCR0 registers to enable the interrupt and DMA functions.

- Set bits 3 and 2 of the IER register to 1
  Enable the receiver line interrupt.
  Enable the modem status interrupt. (Read the MSR register before enabling this interrupt or the interrupt might be issued immediately.)

- When data is transferred with an interrupt
  Bit 6 of HCR0 = 0 or 1 Set the auto-RTS mode.
  Bits 1 and 0 of IER = 1 Enable the transmit buffer empty interrupt and received data available interrupt.

- When data is transferred by DMA
  Bit 6 of HCR0 = 0 or 1 Set the auto-RTS mode.
  Bits 5 to 2 of HCR0 Specify the settings for the DMA mode.
  Bits 1 and 0 of HCR0 = 1 Enable the transmission/reception DMA request.

5.2 Baud Rate Setting

A baud rate is determined according to the settings for serial clock input and the DLM and DLL registers. EM/EV assumes that the serial clocks below are input.
Clock frequencies can be set individually.

Clock Frequency	[Hz]	Clock Source	Baud Rate (bps)	Error Range	DLMR	DLLR	Actual Baud Rate (bps)	Error (%)
229.376	M	PLL3	2400	±4	23	85	2400.13394	0.0055807
			4800		11	171	4799.46435	–0.011159
			9600		5	213	9602.14334	0.0223264
			19200		2	235	19191.4324	–0.044623
			38400		1	117	38434.3164	0.0893655
			57600		0	249	57574.2972	–0.044623
			115200		0	124	115612.903	0.3584229

Clock Frequency	[Hz]	Clock Source	Baud Rate (bps)	Error Range	DLMR	DLLR	Actual Baud Rate (bps)	Error (%)
7.168	M	PLL3/32	2400	±4	0	187	2395.72193	–0.178253
			4800		0	93	4817.2043	0.3584229
			9600		0	47	9531.91489	–0.70922
			19200		0	23	19478.2609	1.4492754
			38400		0	12	37333.3333	–2.777778
			57600		0	8	56000	–2.777778
			115200		0	4	112000	–2.777778

5.3 Notes on Use of FIFO's

UART and the internal bus communicate via a 2-byte interface, so the FIFOs can be read or written at the same time in 2-byte units, but note the following:

(1) An overrun error occurs when 2-byte data is written in response to a DMA request when only 1 byte of space is available in the transmit FIFO in the DMA mode 1.
(2) When a reception timeout event occurs in DMA mode 1 while the timeout interrupt is enabled (bit 4 of the IER register = 0), the host cannot determine whether the request is issued due to a timeout event or the trigger level. As a result, if 2 bytes are read in response to a DMA request, a FIFO underrun error occurs.

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