User's Manual

General Purpose I/O Interface

User's Manual

Multimedia Processor for Mobile Applications
EMMA Mobile ™ EV2

Renesas Electronics
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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the EMMA Mobile EV2. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Data Sheet	Hardware overview and electrical characteristics	EMMA Mobile EV2 Datasheet	R19DS0010EJxxxx
User's manual (1chip)	Hardware whole specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description	EMMA Mobile EV2 User's manual 1chip	R19UH0036EJxxxx
User's manual (module)	Hardware each macro specifications and operation description.	EMMA Mobile EV2 User's manual each module	See below

Document Name	Document No.	Document Name	Document No.
1chip	R19UH0036EJxxxx	DMA Controller	R19UH0043EJxxxx
System Management Unit	R19UH0037EJxxxx	LP-DDR/DDR2 Controller	R19UH0039EJxxxx
Timer	R19UH0054EJxxxx	SD Memory Card Interface	R19UH0061EJxxxx
System Timer	R19UH0055EJxxxx	SDIO Interface	R19UH0042EJxxxx
HD Video Decoder	R19UH0056EJxxxx	CF Card Interface	R19UH0062EJxxxx
Rotator	R19UH0057EJxxxx	Unified Serial Interface	R19UH0047EJxxxx
Resizer	R19UH0058EJxxxx	UART interface	R19UH0040EJxxxx
Image Composer	R19UH0038EJxxxx	USB 2.0 Host Controller	R19UH0045EJxxxx
LCD Interface	R19UH0044EJxxxx	USB 2.0 Function Controller	R19UH0034EJxxxx
ITU-R BT.656 Interface	R19UH0059EJxxxx	IIC Interface	R19UH0052EJxxxx
Digital Terrestrial TV Interface	R19UH0048EJxxxx	General Purpose I/O Interface (This manual)	R19UH0041EJxxxx
Camera Interface	R19UH0060EJxxxx	Pulse Width Modulation Interface	R19UH0063EJxxxx

4 digits of end shows the version.

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names

Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.

Examples the PM03 bit in the PM0 register

P3_5 pin, VCC pin

(2) Notation of Numbers

The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.

Examples Binary: 11b or 11

Hexadecimal: EFA0h

Decimal: 1234

3. Register Notation

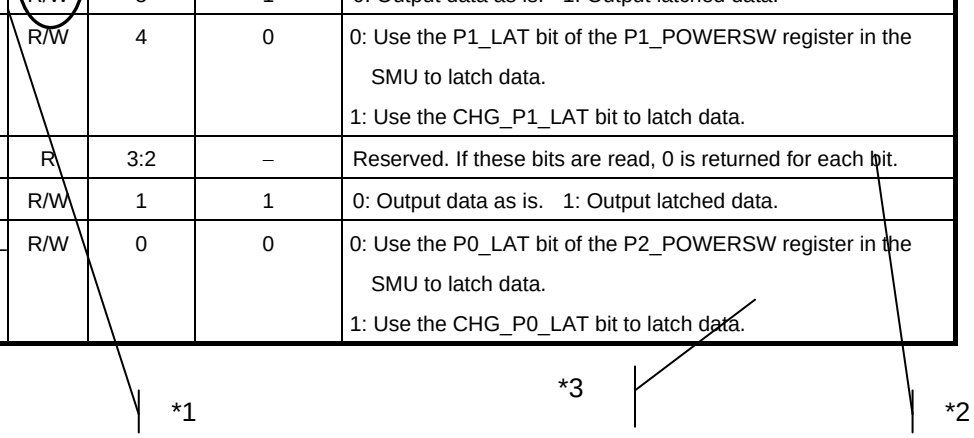
The symbols and terms used in register diagrams are described below.

x.x.x XXX register

This register (XXXXXXX: xxxx_xxxxh) …..

7	6	5	4	3	2	1	0
Reserved		CHG_P1_LAT	LATCH_P1_SEL	Reserved		CHG_P0_LAT	CHG_P0_LAT_SEL

Name	R/W	Bit No.	After Reset	Description
LATCH_P2_SEL	R/W	8	0	0: Use the P2_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P2_LAT bit to latch data.
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P1_LAT	R/W	5	1	0: Output data as is. 1: Output latched data.
LATCH_P1_SEL	R/W	4	0	0: Use the P1_LAT bit of the P1_POWERSW register in the SMU to latch data. 1: Use the CHG_P1_LAT bit to latch data.
Reserved	R	3:2	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P0_LAT	R/W	1	1	0: Output data as is. 1: Output latched data.
CHG_P0_LAT_SEL	R/W	0	0	0: Use the P0_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P0_LAT bit to latch data.



*1

R/W: Read and Write.

R: Read only.

W: Write only.

-: Nothing is assigned.

*2

Reserved bit.

Reserved bit. Set to specified value.

*3

・ Nothing is assigned.

Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.

・ Do not set to a value.

Operation is not guaranteed when a value is set.

・ Function varies according to the operating mode.

The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Register
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

Table of Contents

1. Overview

This user's manual describes the functions of the general-purpose I/O interface (GIO) of EM/EV.

○ GIO is a parallel interface unit with 159 I/O ports.
The GIO port control block operates in synchronization with the rise of GIO_CLK, and the interrupt input detection block operates in synchronization with the rise of GIO_INT_CLK.

○ The internal functions operate at 133 MHz (max).

○ Has interrupt signals to be asserted upon detection of changes of the input signal level. The following can be selected as the change to be detected.
- Synchronous rising edge detection
- Synchronous falling edge detection
- Synchronous high level detection
- Synchronous low level detection
- Synchronous both edge detection
- Asynchronous rising edge detection
- Asynchronous falling edge detection
- Asynchronous high level detection
- Asynchronous low level detection
- Asynchronous both edge detection

○ Has internal registers for controlling the interrupt functions as shown below.
- Whether to enable interrupt functions can be specified for each port.
- Interrupts can be enabled individually for input ports assigned to interrupts.
- Interrupt source statuses can be retained.
- Interrupt sources can be cleared individually by using an interrupt source clear command.
- Whether an interrupt source occurred at a rising or falling edge can be checked in both edge detection mode.
- Interrupt sources that occurred at a rising or falling edge can be cleared individually in both edge detection mode.

○ One GIO_INT signal line is available per 16 GPIO ports. (This macro has 159 GPIO ports, so ten interrupt signal lines are available.)
GIO0_INT: Corresponds to GPIO_000 to GPIO_015 ports
GIO1_INT: Corresponds to GPIO_016 to GPIO_031 ports
GIO2_INT: Corresponds to GPIO_032 to GPIO_047 ports
GIO3_INT: Corresponds to GPIO_048 to GPIO_063 ports
GIO4_INT: Corresponds to GPIO_064 to GPIO_079 ports
GIO5_INT: Corresponds to GPIO_080 to GPIO_095 ports
GIO6_INT: Corresponds to GPIO_096 to GPIO_111 ports
GIO7_INT: Corresponds to GPIO_112 to GPIO_127 ports
GIO8_INT: Corresponds to GPIO_128 to GPIO_143 ports

GIO9_INT: Corresponds to GPIO_144 to GPIO_158 ports

2. Pin Functions

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Pin Name	IO Type	Function	IO Voltage	Alternate Pin Function
GPIO_158	I/O	General-purpose I/O	VDD33/VDD33	UART1_RSTB, UART2_TX
GPIO_157	I/O	General-purpose I/O	VDD18/VDD33	UART1_CTSB, UART2_RX
GPIO_156	I/O	General-purpose I/O	VDD18/VDD33	UART1_TX
GPIO_155	I/O	General-purpose I/O	VDD18/VDD33	UART1_RX
GPIO_154	I/O	General-purpose I/O	VDD18	LOWPWR
GPIO_153	I/O	General-purpose I/O	USB_VD3311	USB_VBUS
GPIO_152	I/O	General-purpose I/O	VDD18	JT_TDOEN
GPIO_151	I/O	General-purpose I/O	VDD18	JT_TDO
GPIO_150	I/O	General-purpose I/O	VDD18	USI5_DI
GPIO_149	I/O	General-purpose I/O	VDD18	USI5_CS4
GPIO_148	I/O	General-purpose I/O	VDD18	USI5_CS3
GPIO_147	I/O	General-purpose I/O	VDD18	USI5_CS2
GPIO_146	I/O	General-purpose I/O	VDD18	USI5_CS1
GPIO_145	I/O	General-purpose I/O	VDD18	USI5_CS0
GPIO_144	I/O	General-purpose I/O	VDD18	USI5_DO
GPIO_143	I/O	General-purpose I/O	VDD18	USI5_CLK
GPIO_142	I/O	General-purpose I/O	VDD33	CAM_YUV7
GPIO_141	I/O	General-purpose I/O	VDD33	CAM_YUV6
GPIO_140	I/O	General-purpose I/O	VDD33	CAM_YUV5
GPIO_139	I/O	General-purpose I/O	VDD33	CAM_YUV4
GPIO_138	I/O	General-purpose I/O	VDD33	CAM_YUV3
GPIO_137	I/O	General-purpose I/O	VDD33	CAM_YUV2
GPIO_136	I/O	General-purpose I/O	VDD33	CAM_YUV1
GPIO_135	I/O	General-purpose I/O	VDD33	CAM_YUV0
GPIO_134	I/O	General-purpose I/O	VDD33	CAM_HS
GPIO_133	I/O	General-purpose I/O	VDD33	CAM_VS
GPIO_132	I/O	General-purpose I/O	VDD33	CAM_CLKI
GPIO_131	I/O	General-purpose I/O	VDD33	CAM_CLKO
GPIO_130	I/O	General-purpose I/O	VDD33	NTSC_DATA7
GPIO_129	I/O	General-purpose I/O	VDD33	NTSC_DATA6
GPIO_128	I/O	General-purpose I/O	VDD33	NTSC_DATA5
GPIO_127	I/O	General-purpose I/O	VDD33	NTSC_DATA4
GPIO_126	I/O	General-purpose I/O	VDD33	NTSC_DATA3
GPIO_125	I/O	General-purpose I/O	VDD33	NTSC_DATA2
GPIO_124	I/O	General-purpose I/O	VDD33	NTSC_DATA1
GPIO_123	I/O	General-purpose I/O	VDD33	NTSC_DATA0
GPIO_122	I/O	General-purpose I/O	VDD33	NTSC_CLK
GPIO_121	I/O	General-purpose I/O	VDD18/VDD33	PWM1, USI4_DI
GPIO_120	I/O	General-purpose I/O	VDD18/VDD33	PWM0, USI4_DI
GPIO_119	I/O	General-purpose I/O	VDD18/VDD33	USI4_CLK

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Pin Name	IO Type	Function	IO Voltage	Alternate Pin Function
GPIO_118	I/O	General-purpose I/O	VDD18/VDD33	USI3_CS0, USI0_CS6
GPIO_117	I/O	General-purpose I/O	VDD18/VDD33	USI3_DO, USI0_CS5
GPIO_116	I/O	General-purpose I/O	VDD18/VDD33	USI3_DI, USI0_CS4
GPIO_115	I/O	General-purpose I/O	VDD18/VDD33	USI3_CLK, USI0_CS3
GPIO_114	I/O	General-purpose I/O	VDD18/VDD33	USI2_CS2, USI4_CS1
GPIO_113	I/O	General-purpose I/O	VDD18/VDD33	USI2_CS1, USI4_CS0
GPIO_112	I/O	General-purpose I/O	VDD18/VDD33	USI2_CS0, DTV_DATA
GPIO_111	I/O	General-purpose I/O	VDD18/VDD33	USI2_DO, DTV_VALID
GPIO_110	I/O	General-purpose I/O	VDD18/VDD33	USI2_DI, DTV_PSYNC
GPIO_109	I/O	General-purpose I/O	VDD18/VDD33	USI2_CLK, DTV_BCLK
GPIO_108	I/O	General-purpose I/O	VDD18/VDD33	USI1_DO
GPIO_107	I/O	General-purpose I/O	VDD18/VDD33	USI1_DI
GPIO_106	I/O	General-purpose I/O	VDD18/VDD33	USI0_CS2
GPIO_105	I/O	General-purpose I/O	VDD18/VDD33	USI0_CS1
GPIO_104	I/O	General-purpose I/O	VDD33	AB_A28, AB_BEN1
GPIO_103	I/O	General-purpose I/O	VDD33	AB_A27, AB_BEN0
GPIO_102	I/O	General-purpose I/O	VDD33	AB_A26, CF_CDB2
GPIO_101	I/O	General-purpose I/O	VDD33	AB_A25, CF_CDB1
GPIO_100	I/O	General-purpose I/O	VDD33	AB_A24, CF_INPACKB
GPIO_099	I/O	General-purpose I/O	VDD33	AB_A23, SDI2_CMD
GPIO_098	I/O	General-purpose I/O	VDD33	AB_A22, SDI2_CKI
GPIO_097	I/O	General-purpose I/O	VDD33	AB_A21, SDI2_CKO, CF_INTRQ
GPIO_096	I/O	General-purpose I/O	VDD33	AB_A20
GPIO_095	I/O	General-purpose I/O	VDD33	AB_A19, CF_A02
GPIO_094	I/O	General-purpose I/O	VDD33	AB_A18, CF_A01
GPIO_093	I/O	General-purpose I/O	VDD33	AB_A17, CF_A00
GPIO_092	I/O	General-purpose I/O	VDD33	AB_AD15, SDI2_DATA3, CF_D15
GPIO_091	I/O	General-purpose I/O	VDD33	AB_AD14, SDI2_DATA2, CF_D14
GPIO_090	I/O	General-purpose I/O	VDD33	AB_AD13, SDI2_DATA1, CF_D13, USI5_CS2
GPIO_089	I/O	General-purpose I/O	VDD33	AB_AD12, SDI2_DATA0, CF_D12, USI5_CS1
GPIO_088	I/O	General-purpose I/O	VDD33	AB_AD11, DTV_DATA, CF_D11, USI5_CS0
GPIO_087	I/O	General-purpose I/O	VDD33	AB_AD10, DTV_VALID, CF_D10, USI5_DO
GPIO_086	I/O	General-purpose I/O	VDD33	AB_AD9, DTV_PSYNC, CF_D09, USI5_DI
GPIO_085	I/O	General-purpose I/O	VDD33	AB_AD8, DTV_BCLK, CF_D08, USI5_CLK
GPIO_084	I/O	General-purpose I/O	VDD33	AB_AD7, CF_D07
GPIO_083	I/O	General-purpose I/O	VDD33	AB_AD6, CF_D06
GPIO_082	I/O	General-purpose I/O	VDD33	AB_AD5, CF_D05
GPIO_081	I/O	General-purpose I/O	VDD33	AB_AD4, CF_D04

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Pin Name	IO Type	Function	IO Voltage	Alternate Pin Function
GPIO_080	I/O	General-purpose I/O	VDD33	AB_AD3, CF_D03
GPIO_079	I/O	General-purpose I/O	VDD33	AB_AD2, CF_D02
GPIO_078	I/O	General-purpose I/O	VDD33	AB_AD1, CF_D01
GPIO_077	I/O	General-purpose I/O	VDD33	AB_AD0, CF_D00
GPIO_076	I/O	General-purpose I/O	VDD33	AB_ADV, CF_RESET
GPIO_075	I/O	General-purpose I/O	VDD33	AB_WAIT, CF_IORDY
GPIO_074	I/O	General-purpose I/O	VDD33	AB_WRB, CF_IOWRB
GPIO_073	I/O	General-purpose I/O	VDD33	AB_RDB, CF_IORDB
GPIO_072	I/O	General-purpose I/O	VDD33	AB_CSB3, CF_CSB1
GPIO_071	I/O	General-purpose I/O	VDD33	AB_CSB2, CF_CSB0
GPIO_070	I/O	General-purpose I/O	VDD33	AB_CSB1
GPIO_069	I/O	General-purpose I/O	VDD33	AB_CSB0
GPIO_068	I/O	General-purpose I/O	VDD33	AB_CLK
GPIO_067	I/O	General-purpose I/O	VDD33	SDI1_DATA3
GPIO_066	I/O	General-purpose I/O	VDD33	SDI1_DATA2
GPIO_065	I/O	General-purpose I/O	VDD33	SDI1_DATA1
GPIO_064	I/O	General-purpose I/O	VDD33	SDI1_DATA0
GPIO_063	I/O	General-purpose I/O	VDD33	SDI1_CMD
GPIO_062	I/O	General-purpose I/O	VDD33	SDI1_CKI
GPIO_061	I/O	General-purpose I/O	VDD33	SDI1_CKO
GPIO_060	I/O	General-purpose I/O	VDD33	SDI0_DATA7
GPIO_059	I/O	General-purpose I/O	VDD33	SDI0_DATA6
GPIO_058	I/O	General-purpose I/O	VDD33	SDI0_DATA5
GPIO_057	I/O	General-purpose I/O	VDD33	SDI0_DATA4
GPIO_056	I/O	General-purpose I/O	VDD33	SDI0_DATA3
GPIO_055	I/O	General-purpose I/O	VDD33	SDI0_DATA2
GPIO_054	I/O	General-purpose I/O	VDD33	SDI0_DATA1
GPIO_053	I/O	General-purpose I/O	VDD33	SDI0_DATA0
GPIO_052	I/O	General-purpose I/O	VDD33	SDI0_CMD
GPIO_051	I/O	General-purpose I/O	VDD33	SDI0_CKI
GPIO_050	I/O	General-purpose I/O	VDD33	SDI0_CKO
GPIO_049	I/O	General-purpose I/O	VDD33	SD_INS
GPIO_048	I/O	General-purpose I/O	VDD33	SD_CKI
GPIO_047	I/O	General-purpose I/O	VDD18/VDD33	IIC1_SDA, UART3_TX
GPIO_046	I/O	General-purpose I/O	VDD18/VDD33	IIC1_SCL, UART3_RX
GPIO_045	I/O	General-purpose I/O	VDD18/VDD33	IIC0_SDA, UART1_RSTB, UART2_TX
GPIO_044	I/O	General-purpose I/O	VDD18/VDD33	IIC0_SCL, UART1_CTSB, UART2_RX
GPIO_043	I/O	General-purpose I/O	VDD33	LCD3_B1, YUV3_D9, TP33_DATA9
GPIO_042	I/O	General-purpose I/O	VDD33	LCD3_B0, YUV3_D8, TP33_DATA8
GPIO_041	I/O	General-purpose I/O	VDD33	LCD3_G1, YUV3_D1, TP33_DATA1
GPIO_040	I/O	General-purpose I/O	VDD33	LCD3_G0, YUV3_D0, TP33_DATA0

(4/4)

Pin Name	IO Type	Function	IO Voltage	Alternate Pin Function
GPIO_039	I/O	General-purpose I/O	VDD33	LCD3_R7, TP33_CTRL
GPIO_038	I/O	General-purpose I/O	VDD33	LCD3_R6, TP33_CLK
GPIO_037	I/O	General-purpose I/O	VDD33	LCD3_R5
GPIO_036	I/O	General-purpose I/O	VDD33	LCD3_R4
GPIO_035	I/O	General-purpose I/O	VDD33	LCD3_R3
GPIO_034	I/O	General-purpose I/O	VDD33	LCD3_R2
GPIO_033	I/O	General-purpose I/O	VDD33	LCD3_R1
GPIO_032	I/O	General-purpose I/O	VDD33	LCD3_R0
GPIO_031	I/O	General-purpose I/O	VDD33	
GPIO_030	I/O	General-purpose I/O	VDD33	
GPIO_029	I/O	General-purpose I/O	VDD33	
GPIO_028	I/O	General-purpose I/O	VDD33	
GPIO_027	I/O	General-purpose I/O	VDD33	
GPIO_026	I/O	General-purpose I/O	VDD33	
GPIO_025	I/O	General-purpose I/O	VDD33	
GPIO_024	I/O	General-purpose I/O	VDD33	
GPIO_023	I/O	General-purpose I/O	VDD33	LCD3_DE, YUV3_DE
GPIO_022	I/O	General-purpose I/O	VDD33	LCD3_VS, YUV3_VS
GPIO_021	I/O	General-purpose I/O	VDD33	LCD3_HS, YUV3_HS
GPIO_020	I/O	General-purpose I/O	VDD33	LCD3_CLK_I, YUV3_CLK_I
GPIO_019	I/O	General-purpose I/O	VDD33	LCD3_PXCLKB
GPIO_018	I/O	General-purpose I/O	VDD33	LCD3_PXCLK
GPIO_017	I/O	General-purpose I/O	VDD33	
GPIO_016	I/O	General-purpose I/O	VDD33	
GPIO_015	I/O	General-purpose I/O	VDD33	
GPIO_014	I/O	General-purpose I/O	VDD33	
GPIO_013	I/O	General-purpose I/O	VDD33	
GPIO_012	I/O	General-purpose I/O	VDD33	
GPIO_011	I/O	General-purpose I/O	VDD33	
GPIO_010	I/O	General-purpose I/O	VDD33	
GPIO_009	I/O	General-purpose I/O	VDD33	
GPIO_008	I/O	General-purpose I/O	VDD33	
GPIO_007	I/O	General-purpose I/O	VDD33	
GPIO_006	I/O	General-purpose I/O	VDD33	
GPIO_005	I/O	General-purpose I/O	VDD18/VDD33	EXT_CLKI
GPIO_004	I/O	General-purpose I/O	VDD18/VDD33	REF_CLKO
GPIO_003	I/O	General-purpose I/O	VDD18/VDD33	
GPIO_002	I/O	General-purpose I/O	VDD18/VDD33	JT_SEL
GPIO_001	I/O	General-purpose I/O	VDD18/VDD33	
GPIO_000	I/O	General-purpose I/O	VDD18/VDD33	

3. Registers

The GIO registers can be accessed only in word (32-bit) units.
Do not write the reserved registers.

The following is a register for GPIO031-GPIO000 ports.
GPIO032-GPIO158 port setting register will be the address which replaced Address line with Table 3-1.

3.1 Register List

Base address: E005_0000H

Address	Register Name	Symbol	R/W	After Reset
0000H	Port switch setting register (output setting)	GIO_000_E1	W	0000_0000H
0004H	Port switch setting register (input setting)	GIO_000_E0	W	0000_0000H
0004H	Port status monitor register	GIO_000_EM	R	0000_0000H
0008H	Output data setting register	GIO_000_OL	W	0000_0000H
000CH	Output data setting register	GIO_000_OH	W	0000_0000H
0010H	Input data read register	GIO_000_I	R	**Note**
0014H	Input port interrupt enable specification register	GIO_000_IIA	R/W	0000_0000H
0018H	Input port interrupt enable register (mask cancel)	GIO_000_IEN	W	0000_0000H
001CH	Input port interrupt disable register (mask setting)	GIO_000_IDS	W	0000_0000H
001CH	Input port interrupt enable monitor register	GIO_000_IIM	R	0000_0000H
0020H	Input port interrupt raw status register	GIO_000_RAW	R	0000_0000H
0024H	Input port interrupt maskable status register	GIO_000_MST	R	0000_0000H
0028H	Input port interrupt source reset register	GIO_000_IIR	W	0000_0000H
002CH-003CH	Reserved	–	–	–
0040H	Input port interrupt detection mode register (7-0 bit)	GIO_000_IDT0	R/W	0000_0000H
0044H	Input port interrupt detection mode register (15-8 bit)	GIO_000_IDT1	R/W	0000_0000H
0048H	Input port interrupt detection mode register (23-16 bit)	GIO_000_IDT2	R/W	0000_0000H
004CH	Input port interrupt detection mode register (32-24 bit)	GIO_000_IDT3	R/W	0000_0000H
0050H	Interrupt status register (in both edge detection mode) (lower 16bit)	GIO_000_RAWBL	R	0000_0000H
0054H	Interrupt status register (in both edge detection mode) (upper 16bit)	GIO_000_RAWBH	R	0000_0000H
0058H	Interrupt source clear register (in both edge detection mode) (lower 16bit)	GIO_000_IRBL	W	0000_0000H
005CH	Interrupt source clear register (in both edge detection mode) (upper 16bit)	GIO_000_IRBH	W	0000_0000H
0060H to FFFCH	Reserved	–	–	–

Note The reset value is determined according to the external pin status.

Table 3-1. The register address every GPIO port

BASE Address E005_0000H	Offset Address				
Register Name	GPIO_031 – 000 GIO_000	GPIO_063 – 032 GIO_032	GPIO_095 – 064 GIO_064	GPIO_127 – 096 GIO_096	GPIO_158 – 128 GIO_128
GIO_XXX_E1	0000H	0080H	0100H	0180H	0200H
GIO_XXX_E0	0004H	0084H	0104H	0184H	0204H
GIO_XXX_EM	0004H	0084H	0104H	0184H	0204H
GIO_XXX_OL	0008H	0088H	0108H	0188H	0208H
GIO_XXX_OH	000CH	008CH	010CH	018CH	020CH
GIO_XXX_I	0010H	0090H	0110H	0190H	0210H
GIO_XXX_INA	0014H	0094H	0114H	0194H	0214H
GIO_XXX_IEN	0018H	0098H	0118H	0198H	0218H
GIO_XXX_IDS	001CH	009CH	011CH	019CH	021CH
GIO_XXX_IIM	001CH	009CH	011CH	019CH	021CH
GIO_XXX_RAW	0020H	00A0H	0120H	01A0H	0220H
GIO_XXX_MST	0024H	00A4H	0124H	01A4H	0224H
GIO_XXX_IIR	0028H	00A8H	0128H	01A8H	0228H
GIO_XXX_IDT0	0040H	00C0H	0140H	01C0H	0240H
GIO_XXX_IDT1	0044H	00C4H	0144H	01C4H	0244H
GIO_XXX_IDT2	0048H	00C8H	0148H	01C8H	0248H
GIO_XXX_IDT3	004CH	00CCH	014CH	01CCH	024CH
GIO_XXX_RAWBL	0050H	00D0H	0150H	01D0H	0250H
GIO_XXX_RAWBH	0054H	00D4H	0154H	01D4H	0254H
GIO_XXX_IRBL	0058H	00D8H	0158H	01D8H	0258H
GIO_XXX_IRBH	005CH	00DCH	015CH	01DCH	025CH

Note XXX : 000, 032, 064, 096, 128

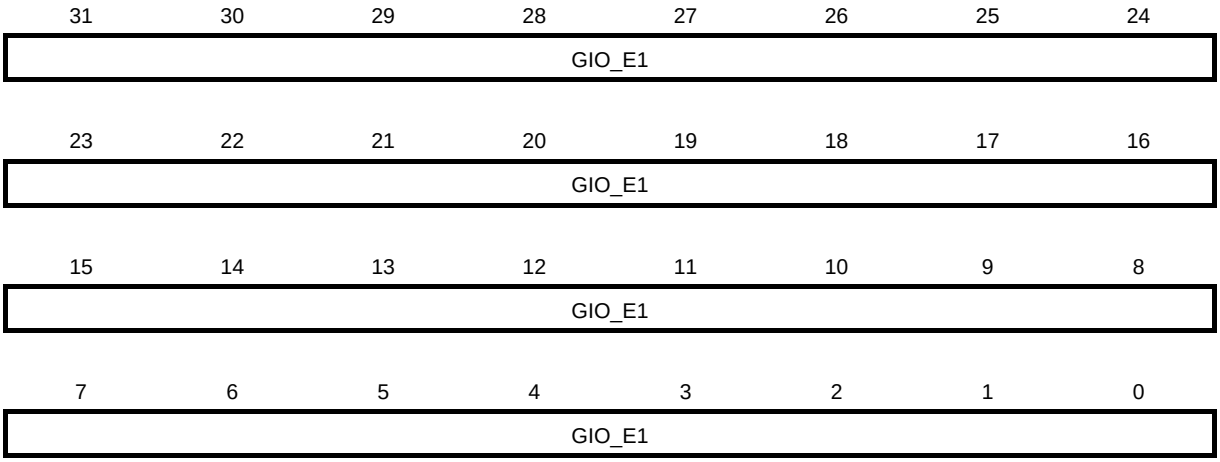
3.2 Register Details

This section describes the registers for GPIO ports 31 to 0.
The structure of the GPIO port [31:0] registers, GPIO port [63:32] registers, GPIO port [95:64] registers, GPIO port [127:96] registers, and GPIO port [158:128] registers is the same.

3.2.1 Port switch setting registers (output setting)

These registers (GIO_E1) specify the GPIO port [31:0] pins to output mode.

GPIO[31:0] port switch setting register (output setting) (GIO_000_E1: E005_0000H)
GPIO[63:32] port switch setting register (output setting) (GIO_032_E1: E005_0080H)
GPIO[95:64] port switch setting register (output setting) (GIO_064_E1: E005_0100H)
GPIO[127:96] port switch setting register (output setting) (GIO_096_E1: E005_0180H)
GPIO[158:128] port switch setting register (output setting) (GIO_128_E1: E005_0200H)



Name	R/W	Bit No.	After Reset	Function
GIO_E1	W	31:0	0000_0000H	Specifies the I/O switching signal of GPIO port [31:0] pins to 1 (output). 0: No operation 1: Sets the I/O switching signal to 1 (output).

Remark For details, see **4.1 I/O control**.

3.2.2 Port switch setting register (input setting)/port status monitor register

These registers (GIO_E0 and GIO_EM) specify the GPIO port [31:0] pins to input mode, and can be used to monitor the GPIO port I/O setting.

GPIO[31:0] port switch setting register (input setting) (GIO_000_E0: E005_0004H)
GPIO[63:32] port switch setting register (input setting) (GIO_032_E0: E005_0084H)
GPIO[95:64] port switch setting register (input setting) (GIO_064_E0: E005_0104H)
GPIO[127:96] port switch setting register (input setting) (GIO_096_E0: E005_0184H)
GPIO[158:128] port switch setting register (input setting) (GIO_128_E0: E005_0204H)

GPIO[31:0] port status monitor register (GIO_000_EM: E005_0004H)
GPIO[63:32] port status monitor register (GIO_032_EM: E005_0084H)
GPIO[95:64] port status monitor register (GIO_064_EM: E005_0104H)
GPIO[127:96] port status monitor register (GIO_096_EM: E005_0184H)
GPIO[158:128] port status monitor register (GIO_128_EM: E005_0204H)

31	30	29	28	27	26	25	24
GIO_E0/GIO_EM							

23	22	21	20	19	18	17	16
GIO_E0/GIO_EM							

15	14	13	12	11	10	9	8
GIO_E0/GIO_EM							

7	6	5	4	3	2	1	0
GIO_E0/GIO_EM							

Name	R/W	Bit No.	After Reset	Function
GIO_E0	W	31:0	0000_0000H	Specifies the I/O switching signal for GPIO port [31:0] pins to 0 (input). 0: No operation 1: Sets the I/O switching signal to 0 (input).
GIO_EM	R			Indicates the GPIO port I/O setting. 0: The I/O switching signal is set to 0 (input). 1: The I/O switching signal is set to 1 (output).

Remark For details, see **4.1 I/O control**.

3.2.3 Output data setting registers

These registers (GIO_OL) specify data output to lower 16bit.

GPIO[15:0] output data setting register (GIO_000_OL: E005_0008H)
GPIO[47:32] output data setting register (GIO_032_OL: E005_0088H)
GPIO[79:64] output data setting register (GIO_064_OL: E005_0108H)
GPIO[111:96] output data setting register (GIO_096_OL: E005_0188H)
GPIO[143:128] output data setting register (GIO_128_OL: E005_0208H)

31	30	29	28	27	26	25	24
GIO_OE[15:8]							

23	22	21	20	19	18	17	16
GIO_OE[7:0]							

15	14	13	12	11	10	9	8
GIO_OD[15:8]							

7	6	5	4	3	2	1	0
GIO_OD[7:0]							

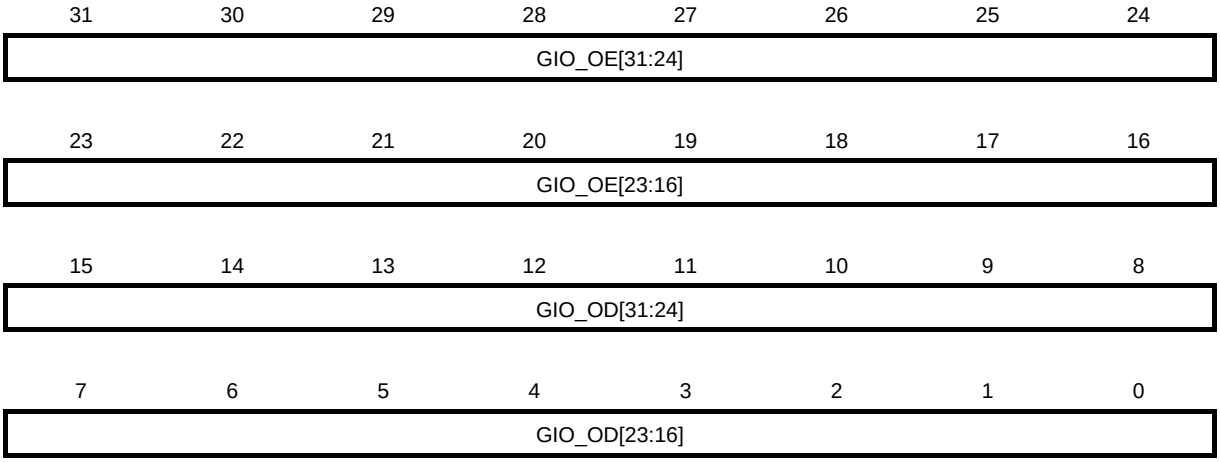
Name	R/W	Bit No.	After Reset	Function
GIO_OE	W	31:16	–	Enables outputting of data to GIO_OD[15:0]. When these bits are read, 0 is returned for each bit.
GIO_OD	R/W	15:0	0000H	Specifies output data. Specifies the values to be output to the ports whose GPIO pins are in the output mode.

Remark For details, see **4.2 Setting of output data and reading of input data**.

3.2.4 Output data setting registers

These registers (GIO_OH) specify data output to upper 16bit.

GPIO[31:16] output data setting register (GIO_000_OH: E005_000CH)
GPIO[63:48] output data setting register (GIO_032_OH: E005_008CH)
GPIO[95:80] output data setting register (GIO_064_OH: E005_010CH)
GPIO[127:112] output data setting register (GIO_096_OH: E005_018CH)
GPIO[158:148] output data setting register (GIO_128_OH: E005_020CH)



Name	R/W	Bit No.	After Reset	Function
GIO_OE	W	31:16	–	Enables outputting of data to GIO_OD[31:16]. When these bits are read, 0 is returned for each bit.
GIO_OD	R/W	15:0	0000H	Specifies output data. Specifies the values to be output to the ports whose GPIO pins are in the output mode.

Remark For details, see **4.2 Setting of output data and reading of input data**.

3.2.5 Input data read registers

These registers (GIO_I) are used to read data input to the GPIO[31:0] ports.

GPIO[31:0] input data read register (GIO_000_I: E005_0010H)
GPIO[63:32] input data read register (GIO_032_I: E005_0090H)
GPIO[95:64] input data read register (GIO_064_I: E005_0110H)
GPIO[127:96] input data read register (GIO_096_I: E005_0190H)
GPIO[158:128] input data read register (GIO_128_I: E005_0210H)

31	30	29	28	27	26	25	24
GIO_I							

23	22	21	20	19	18	17	16
GIO_I							

15	14	13	12	11	10	9	8
GIO_I							

7	6	5	4	3	2	1	0
GIO_I							

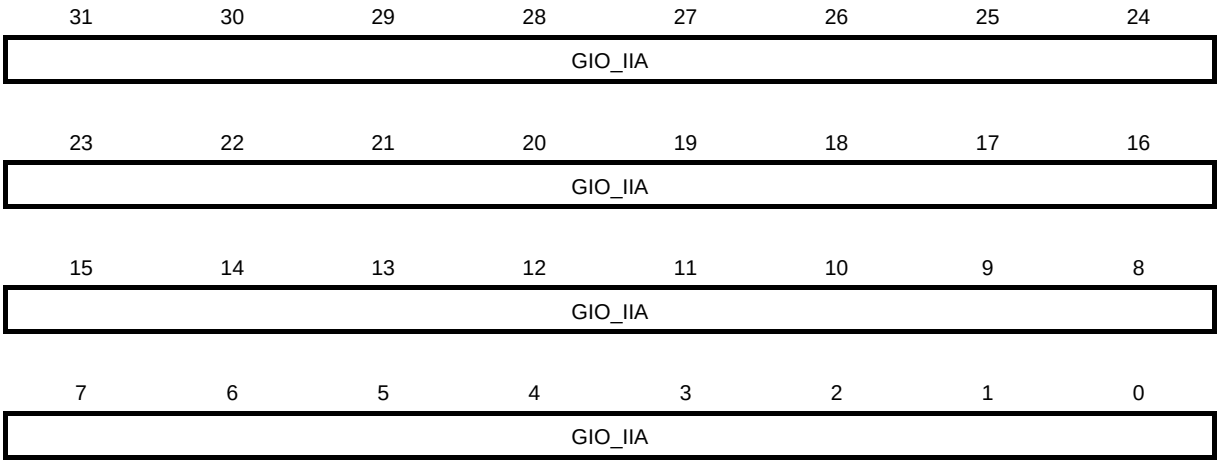
Name	R/W	Bit No.	After Reset	Function
GIO_I	R	31:0	**Note**	Indicates input data. Used to read data input to the external GPIO ports.

Note The reset value is determined according to the external pin status.

3.2.6 Input port interrupt enable specification registers

These registers (GIO_IIA) specify whether to enable interrupt detection in each input port. If “1” is set in these registers, the status of the interrupt sources is reflected in the GIO_RAW and GIO_RAWB registers. If 0 is set in these registers, the interrupt sources are cleared.

GPIO[31:0] input port interrupt enable specification register (GIO_000_IIA: E005_0014H)
GPIO[63:32] input port interrupt enable specification register (GIO_032_IIA: E005_0094H)
GPIO[95:64] input port interrupt enable specification register (GIO_064_IIA: E005_0114H)
GPIO[127:96] input port interrupt enable specification register (GIO_096_IIA: E005_0194H)
GPIO[158:128] input port interrupt enable specification register (GIO_128_IIA: E005_0214H)



Name	R/W	Bit No.	After Reset	Function
GIO_IIA	R/W	31:0	0000_0000H	Specifies whether to enable interrupt detection in each input port. 0: Disables interrupt detection. 1: Enables interrupt detection.

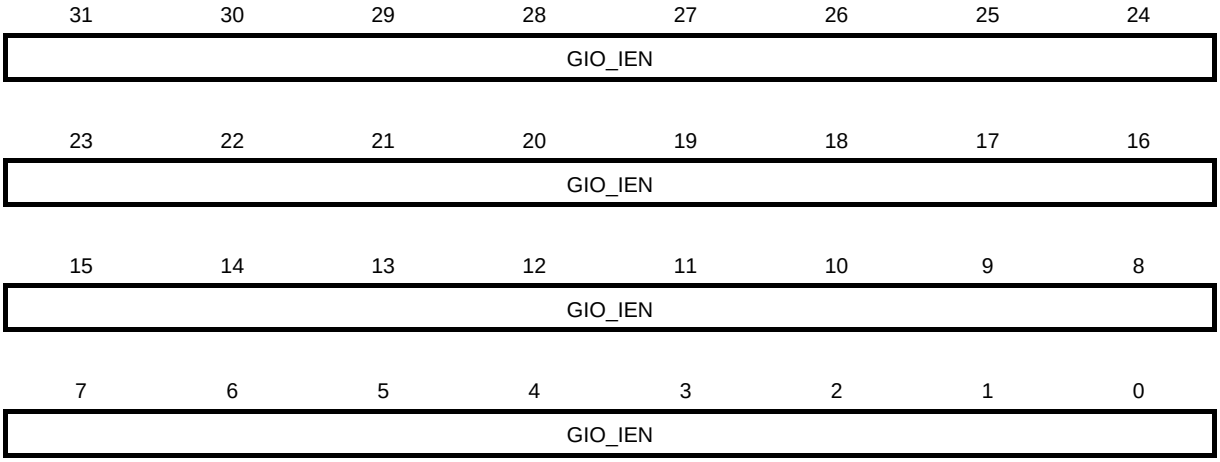
Remarks 1. For details about the interrupt detection sequence, see **5.1 Input port interrupt function setup procedure**.

2. If the setting of this register is changed, wait for three GIO_INT_CLK cycles and then set the interrupt enable register (GIOIIA) to 1.

3.2.7 Input port interrupt enable registers (mask cancel)

These registers (GIO_IEN) enable issuance of interrupt requests in each port.
Setting up these registers enables interrupts enabled in the GIOIIA register. Only data of bits to which 1 is written is updated. If 0 is written, the current value is retained.

GPIO[31:0] input port interrupt enable register (mask cancel) (GIO_000_IEN: E005_0018H)
GPIO[63:32] input port interrupt enable register (mask cancel) (GIO_032_IEN: E005_0098H)
GPIO[95:64] input port interrupt enable register (mask cancel) (GIO_064_IEN: E005_0118H)
GPIO[127:96] input port interrupt enable register (mask cancel) (GIO_096_IEN: E005_0198H)
GPIO[158:128] input port interrupt enable register (mask cancel) (GIO_128_IEN: E005_0218H)



Name	R/W	Bit No.	After Reset	Function
GIO_IEN	W	31:0	0000_0000H	Enables issuance of interrupt requests in each port. 0: No operation 1: Enables interrupts.

Remark For details about the interrupt detection sequence, see **5.1 Input port interrupt function setup procedure**.

3.2.8 Input port interrupt disable registers (mask setting)/input port interrupt enable monitor registers

These registers (GIO_IDS and GIO_IIM) disable GPIO port interrupts, and can be used to monitor the GPIO port interrupt status.

GPIO[31:0] input port interrupt disable register (mask setting) (GIO_000_IDS: E005_001CH)
GPIO[63:32] input port interrupt disable register (mask setting) (GIO_032_IDS: E005_009CH)
GPIO[95:64] input port interrupt disable register (mask setting) (GIO_064_IDS: E005_011CH)
GPIO[127:96] input port interrupt disable register (mask setting) (GIO_096_IDS: E005_019CH)
GPIO[158:128] input port interrupt disable register (mask setting) (GIO_128_IDS: E005_021CH)

GPIO[31:0] input port interrupt enable monitor register (GIO_000_IIM: E005_001CH)
GPIO[63:32] input port interrupt enable monitor register (GIO_032_IIM: E005_009CH)
GPIO[95:64] input port interrupt enable monitor register (GIO_064_IIM: E005_011CH)
GPIO[127:98] input port interrupt enable monitor register (GIO_096_IIM: E005_019CH)
GPIO[158:128] input port interrupt enable monitor register (GIO_128_IIM: E005_021CH)

31	30	29	28	27	26	25	24
GIO_IDS / GIO_IIM							

23	22	21	20	19	18	17	16
GIO_IDS / GIO_IIM							

15	14	13	12	11	10	9	8
GIO_IDS / GIO_IIM							

7	6	5	4	3	2	1	0
GIO_IDS / GIO_IIM							

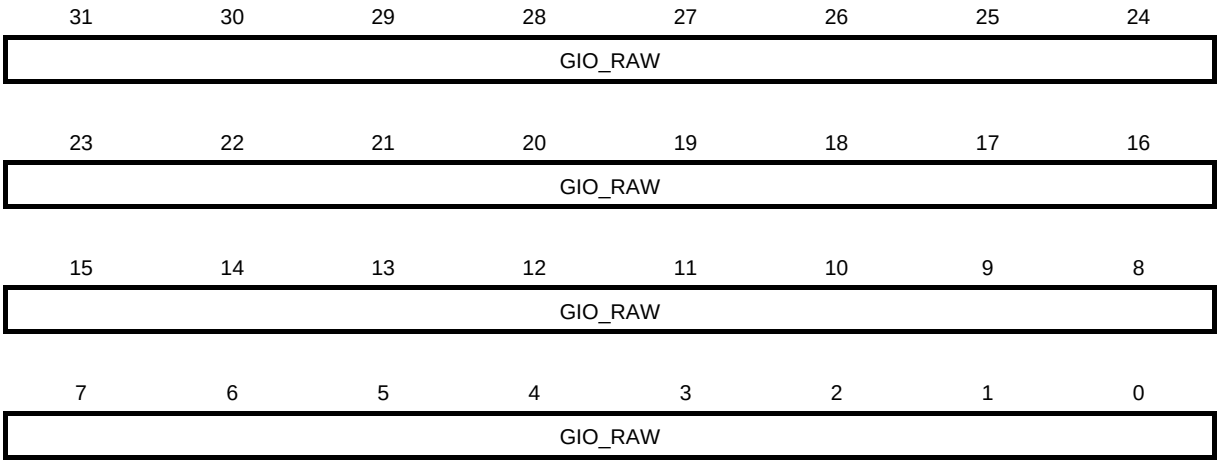
Name	R/W	Bit No.	After Reset	Function
GIO_IDS	W	31:0	0000_0000H	Disables interrupts in each port. 0: No operation 1: Disables interrupts.
GIO_IIM	R			Can be used to monitor the interrupt status in each port. 0: Disables interrupts. 1: Enables interrupts.

Remark For details about the interrupt detection sequence, see **5.1 Input port interrupt function setup procedure**.

3.2.9 Input port interrupt raw status registers

These read-only registers (GIO_RAW) indicate the status of interrupt sources regardless of the settings of the GIO_IEN and GIO_IDS registers.
To clear these registers, write 1 to the corresponding bits of the GIO_IIR register.

GPIO[31:0] input port interrupt source status register (GIO_000_RAW: E005_0020H)
GPIO[63:32] input port interrupt source status register (GIO_032_RAW: E005_00A0H)
GPIO[95:64] input port interrupt source status register (GIO_064_RAW: E005_0120H)
GPIO[127:96] input port interrupt source status register (GIO_096_RAW: E005_01A0H)
GPIO[158:128] input port interrupt source status register (GIO_128_RAW: E005_0220H)



Name	R/W	Bit No.	After Reset	Function
GIO_RAW	R	31:0	0000_0000H	Indicates the status of interrupt sources at each GPIO port. 0: No interrupt source 1: Interrupt source has occurred

Remark For details about the interrupt detection sequence, see **5.1 Input port interrupt function setup procedure**.

3.2.10 Input port interrupt maskable status registers

These registers (GIO_MST) indicate the status of interrupt sources enabled with the interrupt enable registers.

GPIO[31:0] input port interrupt maskable status register (GIO_000_MST: E005_0024H)
GPIO[63:32] input port interrupt maskable status register (GIO_032_MST: E005_00A4H)
GPIO[95:64] input port interrupt maskable status register (GIO_064_MST: E005_0124H)
GPIO[127:96] input port interrupt maskable status register (GIO_096_MST: E005_01A4H)
GPIO[158:128] input port interrupt maskable status register (GIO_128_MST: E005_0224H)

31	30	29	28	27	26	25	24
GIO_MST							

23	22	21	20	19	18	17	16
GIO_MST							

15	14	13	12	11	10	9	8
GIO_MST							

7	6	5	4	3	2	1	0
GIO_MST							

Name	R/W	Bit No.	After Reset	Function
GIO_MST	R	31:0	0000_0000H	Indicates the status of interrupt sources at each GPIO port, only for bits to which interrupts are enabled. 0: No interrupt source 1: Interrupt source has occurred

Remark For details about the interrupt detection sequence, see **5.1 Input port interrupt function setup procedure**.

3.2.11 Input port interrupt source reset registers

These registers (GIO_IIR) clear the interrupt sources being enabled.

GPIO[31:0] input port interrupt source reset register (GIO_000_IIR: E005_0028H)
GPIO[63:32] input port interrupt source reset register (GIO_032_IIR: E005_00A8H)
GPIO[95:64] input port interrupt source reset register (GIO_064_IIR: E005_0128H)
GPIO[127:96] input port interrupt source reset register (GIO_096_IIR: E005_01A8H)
GPIO[158:128] input port interrupt source reset register (GIO_128_IIR: E005_0228H)

Name	R/W	Bit No.	After Reset	Function
GIO_IIR	W	31:0	0000_0000H	Clears interrupt sources. Writing 1 to these bits clears the interrupt sources detected at rising and falling edges, which are retained in the GIO_RAWB register. To clear the interrupt sources detected at rising or falling edges, set up the GIO_IRB register. 0: No operation 1: Clears the interrupt source status registers (GIO_RAW, GIO_MST, GIO_RAWBL and GIO_RAWBH).

Remark For details about the interrupt detection sequence, see **5.1 Input port interrupt function setup procedure**.

3.2.12 Input port interrupt detection mode registers

These registers (GIO_IDT0) specify the interrupt detection mode.

GPIO[7:0] input port interrupt detection mode register (GIO_000_IDT0: E005_0040H)
GPIO[39:32] input port interrupt detection mode register (GIO_032_IDT0: E005_00C0H)
GPIO[71:64] input port interrupt detection mode register (GIO_064_IDT0: E005_0140H)
GPIO[103:96] input port interrupt detection mode register (GIO_096_IDT0: E005_01C0H)
GPIO[135:128] input port interrupt detection mode register (GIO_128_IDT0: E005_00240H)

31	30	29	28	27	26	25	24
GIO_IDT0_7				GIO_IDT0_6			

23	22	21	20	19	18	17	16
GIO_IDT0_5				GIO_IDT0_4			

15	14	13	12	11	10	9	8
GIO_IDT0_3				GIO_IDT0_2			

7	6	5	4	3	2	1	0
GIO_IDT0_1				GIO_IDT0_0			

Name	R/W	Bit No.	After Reset	Function
GIO_IDT0_7	R/W	31:28	0H	Specifies the interrupt detection mode for GPIO port 7.
GIO_IDT0_6	R/W	27:24	0H	Specifies the interrupt detection mode for GPIO port 6.
GIO_IDT0_5	R/W	23:20	0H	Specifies the interrupt detection mode for GPIO port 5 .
GIO_IDT0_4	R/W	19:16	0H	Specifies the interrupt detection mode for GPIO port 4.
GIO_IDT0_3	R/W	15:12	0H	Specifies the interrupt detection mode for GPIO port 3.
GIO_IDT0_2	R/W	11:8	0H	Specifies the interrupt detection mode for GPIO port 2.
GIO_IDT0_1	R/W	7:4	0H	Specifies the interrupt detection mode for GPIO port 1.
GIO_IDT0_0	R/W	3:0	0H	Specifies the interrupt detection mode for GPIO port 0.

Remarks 1. For details about interrupt detection modes, see **4.3 Interrupt detection modes**.

2. For details about the interrupt detection sequence, see **5.1 Input port interrupt function setup procedure**.

3.2.13 Input port interrupt detection mode registers

These registers (GIO_IDT1) specify the interrupt detection mode.

GPIO[15:8] input port interrupt detection mode register (GIO_000_IDT1: E005_0044H)
GPIO[47:40] input port interrupt detection mode register (GIO_032_IDT1: E005_00C4H)
GPIO[79:72] input port interrupt detection mode register (GIO_064_IDT1: E005_0144H)
GPIO[111:104] input port interrupt detection mode register (GIO_096_IDT1: E005_01C4H)
GPIO[143:136] input port interrupt detection mode register (GIO_128_IDT1: E005_0244H)

31	30	29	28	27	26	25	24
GIO_IDT1_15				GIO_IDT1_14			

23	22	21	20	19	18	17	16
GIO_IDT1_13				GIO_IDT1_12			

15	14	13	12	11	10	9	8
GIO_IDT1_11				GIO_IDT1_10			

7	6	5	4	3	2	1	0
GIO_IDT1_9				GIO_IDT1_8			

Name	R/W	Bit No.	After Reset	Function
GIO_IDT1_15	R/W	31:28	0H	Specifies the interrupt detection mode for GPIO port 15.
GIO_IDT1_14	R/W	27:24	0H	Specifies the interrupt detection mode for GPIO port 14.
GIO_IDT1_13	R/W	23:20	0H	Specifies the interrupt detection mode for GPIO port 13.
GIO_IDT1_12	R/W	19:16	0H	Specifies the interrupt detection mode for GPIO port 12
GIO_IDT1_11	R/W	15:12	0H	Specifies the interrupt detection mode for GPIO port 11.
GIO_IDT1_10	R/W	11:8	0H	Specifies the interrupt detection mode for GPIO port 10.
GIO_IDT1_9	R/W	7:4	0H	Specifies the interrupt detection mode for GPIO port 9.
GIO_IDT1_8	R/W	3:0	0H	Specifies the interrupt detection mode for GPIO port 8.

Remarks 1. For details about interrupt detection modes, see **4.3 Interrupt detection modes**.

2. For details about the interrupt detection sequence, see **5.1 Input port interrupt function setup procedure**.

3.2.14 Input port interrupt detection mode registers

These registers (GIO_IDT2) specify the interrupt detection mode.

GPIO[23:16] input port interrupt detection mode register (GIO_000_IDT2: E005_0048H)
GPIO[55:48] input port interrupt detection mode register (GIO_032_IDT2: E005_00C8H)
GPIO[87:80] input port interrupt detection mode register (GIO_064_IDT2: E005_0148H)
GPIO[119:112] input port interrupt detection mode register (GIO_096_IDT2: E005_01C8H)
GPIO[151:144] input port interrupt detection mode register (GIO_128_IDT2: E005_0248H)

31	30	29	28	27	26	25	24
GIO_IDT2_23				GIO_IDT2_22			

23	22	21	20	19	18	17	16
GIO_IDT2_21				GIO_IDT2_20			

15	14	13	12	11	10	9	8
GIO_IDT2_19				GIO_IDT2_18			

7	6	5	4	3	2	1	0
GIO_IDT2_17				GIO_IDT2_16			

Name	R/W	Bit No.	After Reset	Function
GIO_IDT2_23	R/W	31:28	0H	Specifies the interrupt detection mode for GPIO port 23.
GIO_IDT2_22	R/W	27:24	0H	Specifies the interrupt detection mode for GPIO port 22.
GIO_IDT2_21	R/W	23:20	0H	Specifies the interrupt detection mode for GPIO port 21.
GIO_IDT2_20	R/W	19:16	0H	Specifies the interrupt detection mode for GPIO port 20.
GIO_IDT2_19	R/W	15:12	0H	Specifies the interrupt detection mode for GPIO port 19.
GIO_IDT2_18	R/W	11:8	0H	Specifies the interrupt detection mode for GPIO port 18.
GIO_IDT2_17	R/W	7:4	0H	Specifies the interrupt detection mode for GPIO port 17.
GIO_IDT2_16	R/W	3:0	0H	Specifies the interrupt detection mode for GPIO port 16.

Remarks 1. For details about interrupt detection modes, see **4.3 Interrupt detection modes**.

2. For details about the interrupt detection sequence, see **5.1 Input port interrupt function setup procedure**.

3.2.15 Input port interrupt detection mode registers

These registers (GIO_IDT3) specify the interrupt detection mode.

GPIO[31:24] input port interrupt detection mode register (GIO_000_IDT3: E005_004CH)
GPIO[63:56] input port interrupt detection mode register (GIO_032_IDT3: E005_00CCH)
GPIO[95:88] input port interrupt detection mode register (GIO_064_IDT3: E005_014CH)
GPIO[127:120] input port interrupt detection mode register (GIO_096_IDT3: E005_01CCH)
GPIO[158:152] input port interrupt detection mode register (GIO_128_IDT3: E005_024CH)

31	30	29	28	27	26	25	24
GIO_IDT3_31				GIO_IDT3_30			

23	22	21	20	19	18	17	16
GIO_IDT3_29				GIO_IDT3_28			

15	14	13	12	11	10	9	8
GIO_IDT3_27				GIO_IDT3_26			

7	6	5	4	3	2	1	0
GIO_IDT3_25				GIO_IDT3_24			

Name	R/W	Bit No.	After Reset	Function
GIO_IDT3_31	R/W	31:28	0H	Specifies the interrupt detection mode for GPIO port 31.
GIO_IDT3_30	R/W	27:24	0H	Specifies the interrupt detection mode for GPIO port 30.
GIO_IDT3_29	R/W	23:20	0H	Specifies the interrupt detection mode for GPIO port 29.
GIO_IDT3_28	R/W	19:16	0H	Specifies the interrupt detection mode for GPIO port 28.
GIO_IDT3_27	R/W	15:12	0H	Specifies the interrupt detection mode for GPIO port 27.
GIO_IDT3_26	R/W	11:8	0H	Specifies the interrupt detection mode for GPIO port 26.
GIO_IDT3_25	R/W	7:4	0H	Specifies the interrupt detection mode for GPIO port 25.
GIO_IDT3_24	R/W	3:0	0H	Specifies the interrupt detection mode for GPIO port 24.

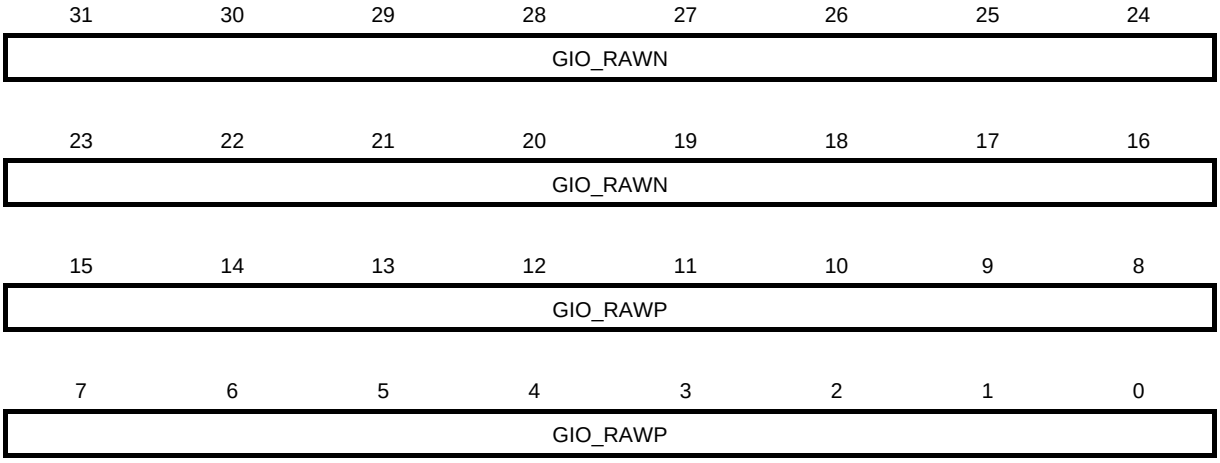
Remarks 1. For details about interrupt detection modes, see **4.3 Interrupt detection modes**.

2. For details about the interrupt detection sequence, see **5.1 Input port interrupt function setup procedure**.

3.2.16 Interrupt status register (in both edge detection mode)

These registers (GIO_RAWBL) indicate whether an interrupt has been detected at a rising or falling edge.

GPIO[15:0] interrupt status register (in both edge detection mode) (GIO_000_RAWBL: E005_0050H)
GPIO[47:32] interrupt status register (in both edge detection mode) (GIO_032_RAWBL: E005_00D0H)
GPIO[79:64] interrupt status register (in both edge detection mode) (GIO_064_RAWBL: E005_0150H)
GPIO[111:96] interrupt status register (in both edge detection mode) (GIO_096_RAWBL: E005_01D0H)
GPIO[143:128] interrupt status register (in both edge detection mode) (GIO_128_RAWBL: E005_0250H)



Name	R/W	Bit No.	After Reset	Function
GIO_RAWN	R	31:16	0000H	Falling edge detection Indicates that an interrupt has been detected at a falling edge in both edge detection mode. These bits are set even if an interrupt has been detected in falling edge detection mode.
GIO_RAWP	R	15:0	0000H	Rising edge detection Indicates that an interrupt has been detected at a rising edge in both edge detection mode. These bits are set even if an interrupt has been detected in rising edge detection mode.

3.2.17 Interrupt status register (in both edge detection mode)

These registers (GIO_RAWBH) indicate whether an interrupt has been detected at a rising or falling edge.

GPIO[31:16] interrupt status register (in both edge detection mode) (GIO_000_RAWBH: E005_0054H)
GPIO[63:48] interrupt status register (in both edge detection mode) (GIO_032_RAWBH: E005_00D4H)
GPIO[95:80] interrupt status register (in both edge detection mode) (GIO_064_RAWBH: E005_0154H)
GPIO[127:112] interrupt status register (in both edge detection mode) (GIO_096_RAWBH: E005_01D4H)
GPIO[158:144] interrupt status register (in both edge detection mode) (GIO_128_RAWBH: E005_0254H)

31	30	29	28	27	26	25	24
GIO_RAWN							

23	22	21	20	19	18	17	16
GIO_RAWN							

15	14	13	12	11	10	9	8
GIO_RAWP							

7	6	5	4	3	2	1	0
GIO_RAWP							

Name	R/W	Bit No.	After Reset	Function
GIO_RAWN	R	31:16	0000H	Falling edge detection Indicates that an interrupt has been detected at a falling edge in both edge detection mode. These bits are set even if an interrupt has been detected in falling edge detection mode.
GIO_RAWP	R	15:0	0000H	Rising edge detection Indicates that an interrupt has been detected at a rising edge in both edge detection mode. These bits are set even if an interrupt has been detected in rising edge detection mode.

3.2.18 Interrupt source clear registers (in both edge detection mode)

These registers (GIO_IRBL) clear an interrupt source that has occurred at a rising or falling edge, in both edge detection mode.

GPIO[15:0] interrupt source clear register (in both edge detection mode) (GIO_000_IRBL: E005_0058H)
GPIO[47:32] interrupt source clear register (in both edge detection mode) (GIO_032_IRBL: E005_00D8H)
GPIO[79:64] interrupt source clear register (in both edge detection mode) (GIO_064_IRBL: E005_0158H)
GPIO[111:96] interrupt source clear register (in both edge detection mode) (GIO_096_IRBL: E005_01D8H)
GPIO[143:128] interrupt source clear register (in both edge detection mode) (GIO_128_IRBL: E005_0258H)

31	30	29	28	27	26	25	24
GIO_IRN							

23	22	21	20	19	18	17	16
GIO_IRN							

15	14	13	12	11	10	9	8
GIO_IRP							

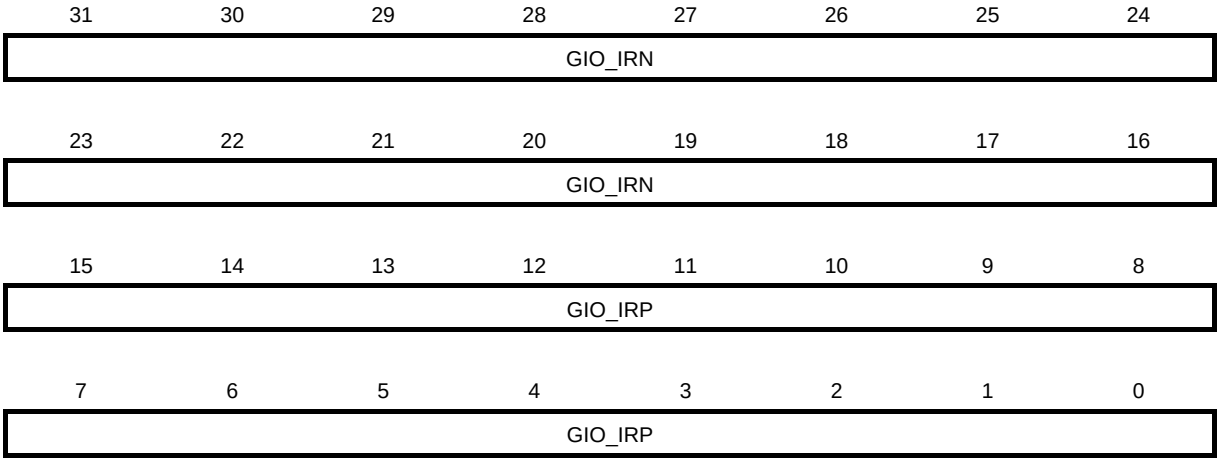
7	6	5	4	3	2	1	0
GIO_IRP							

Name	R/W	Bit No.	After Reset	Function
GIO_IRN	W	31:16	0000H	Clears the interrupt source detected at a falling edge in both edge detection mode. If the interrupt sources are cleared in the GIO_IIR register, interrupt sources that have been detected at either edge are cleared. 0: No operation 1: Clears the GIO_RAWN bits in the GIO_RAWBL and GIO_RAWBH registers.
GIO_IRP	W	15:0	0000H	Clears the interrupt source detected at a rising edge in both edge detection mode. If the interrupt sources are cleared in the GIO_IIR register, interrupt sources that have been detected at either edge are cleared. 0: No operation 1: Clears the GIO_RAWP bits in the GIO_RAWBL and GIO_RAWBH registers.

3.2.19 Interrupt source clear registers (in both edge detection mode)

These registers (GIO_IRBH) clear an interrupt source that has occurred at a rising or falling edge, in both edge detection mode.

GPIO[31:16] interrupt source clear register (in both edge detection mode) (GIO_000_IRBH: E005_005CH)
GPIO[63:48] interrupt source clear register (in both edge detection mode) (GIO_032_IRBH: E005_00DCH)
GPIO[95:80] interrupt source clear register (in both edge detection mode) (GIO_064_IRBH: E005_015CH)
GPIO[127:112] interrupt source clear register (in both edge detection mode) (GIO_096_IRBH: E005_01DCH)
GPIO[158:144] interrupt source clear register (in both edge detection mode) (GIO_128_IRBH: E005_025CH)



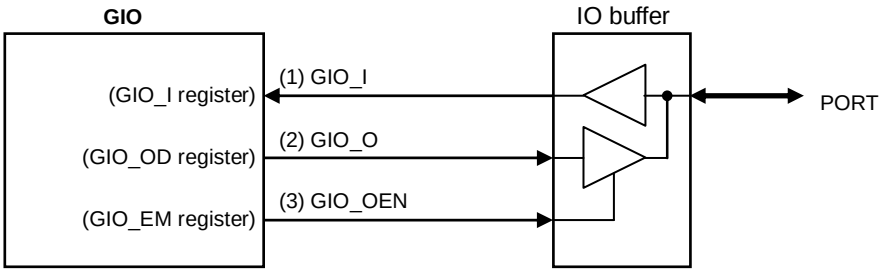
Name	R/W	Bit No.	After Reset	Function
GIO_IRN	W	31:16	0000H	Clears the interrupt source detected at a falling edge in both edge detection mode. If the interrupt sources are cleared in the GIO_IIR register, interrupt sources that have been detected at either edge are cleared. 0: No operation 1: Clears the GIO_RAWN bits in the GIO_RAWBL and GIO_RAWBH registers.
GIO_IRP	W	15:0	0000H	Clears the interrupt source detected at a rising edge in both edge detection mode. If the interrupt sources are cleared in the GIO_IIR register, interrupt sources that have been detected at either edge are cleared. 0: No operation 1: Clears the GIO_RAWP bits in the GIO_RAWBL and GIO_RAWBH registers.

4. Description of Functions

4.1 I/O Control

It is assumed that GIO is connected to a bidirectional buffer, as shown in the following figure.

Figure 4-1. Connection with Bidirectional Buffer



In GIO, a register for specifying the output mode and a register for specifying the input mode are provided so as to enable changing of only the bits subject to I/O switching while other bits can retain the current values.

○ When setting a port to output mode:

Set the relevant bit of the GIO_E1 register to 1. The corresponding bit of the GIO_EM register is then set to 1 (output mode). Bits being set to 0 retain the GIO_EM register settings.

1: Sets to 1 (output).

0: Retains the current value. (No operation)

○ When setting a port to input mode:

Set the relevant bit of the GIO_E0 register to 1. The corresponding bit of the GIO_EM register is then set to 0 (input mode). Bits being set to 0 retain the GIO_EM register settings.

1: Sets to 0 (input).

0: Retains the current value. (No operation)

The setup result (port I/O status) can be checked by reading the GIO_EM register.

Example Initial value 0000_0000_0011_0000

<1> Set GIO_E1 to 0000_0000_0000_0011 (sets bits 0 and 1 to output mode)

→ 0000_0000_0011_0011

Bits 0 and 1 are set to 1 (output port) and other bits retain the current values.

<2> Set GIO_E0 to 0000_0000_ 0000_1010 (sets bits 1 and 3 to input mode)

→ 0000_0000_0011_0001

Bits 1 and 3 are set to 0 (input) and other bits retain the current values.

4.2 Setting of Output Data and Reading of Input Data

4.2.1 Output data setting

In GIO, the GIO_OD bits of the output data setting register (GIO_OL) and the GIO_OE bits of the output data setting enable register (GIO_OH) are provided so as to enable changing of only the bits subject to output data setup while other bits can retain the current values. (See **3.2.3 Output data setting registers** and **3.2.4 Output data setting registers**.)

When writing output data to the GIO_OD bits, the corresponding GIO_OE bits must also be set to 1 at the same time. Only the values of the GIO_OD bits whose corresponding GIO_OE bits are set to 1 are updated; other bits retain the current values.

Example When GIO_OL is set to 00FF_5555H (GIO_OE[15:0] = 00FFH, GIO_OD = 5555H) while GIO_OD is set to 0F0FH before output data is specified, the GIO_OE value is changed to 0F55H. See Table 4-1.

Table 4-1. Output Data Setup Example

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GIO_OD (before setup)	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
GIO_OE	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
GIO_OD (setup value)	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
GIO_OD (after setup)	0	0	0	0	1	1	1	1	0	1	0	1	0	1	0	1

Retained **Reflected**

When the GIO_OD bits are read, the values set to the GIO_OD bits, not the data written to the GIO_OD bits, are read. In the above example, 0F55H is read (not the setup value, 5555H).

4.2.2 Reading input data

Table 4-2 lists the values that can be read via the input data read register (GIO_I), which depend on the GIO_EM register values. Values of the external GPIO pin are read if the GIO_EM bit is set to 0 (input mode), values of the external GPIO pin are read if the GIO_EM bit is set to 1 (output mode).

Table 4-2. Value Read by GIO_I

GIO_EM	External GPIO Pin	GIO_OD	GIO_I
0 (input mode)	0	–	0
0 (input mode)	1	–	1
1 (output mode)	0	0	0
1 (output mode)	1	1	1

4.3 Interrupt Detection Modes

The following modes are available for interrupt detection.

4.3.1 Synchronous rising edge detection

The interrupt source status bits (GIO_RAW and GIO_RAWP) are set at a rising edge of input port GIO_P_IN. Interrupts may not be detected correctly if GIO_P_IN goes into low level again within one cycle of the interrupt monitor clock (GIO_INT_CLK) (high level width is 1T or shorter). To detect such interrupts, use asynchronous high edge detection.

4.3.2 Synchronous falling edge detection

The interrupt source status bits (GIO_RAW and GIO_RAWN) are set at a falling edge of input port GIO_P_IN. Interrupts may not be detected correctly if GIO_P_IN goes into high level again within one cycle of the interrupt monitor clock (GIO_INT_CLK) (low level width is 1T or shorter). To detect such interrupts, use asynchronous falling edge detection.

4.3.3 Synchronous high level detection

The interrupt source status bit (GIO_RAW) is set if input port GIO_P_IN = 1 is detected. When GIO_P_IN goes into low level, the corresponding interrupt source status is automatically cleared. It is not cleared by setting up the interrupt source clear register (GIO_IIR).
Interrupts may not be detected correctly if GIO_P_IN outputs 1 for a period shorter than one cycle of the interrupt monitor clock (GIO_INT_CLK). To detect such inputs, use asynchronous high level detection.

4.3.4 Synchronous low level detection

The interrupt source status bit (GIO_RAW) is set if input port GIO_P_IN = 0 is detected. When GIO_P_IN goes into high level, the corresponding interrupt source status is automatically cleared. It is not cleared by setting up the interrupt source clear register (GIO_IIR).
Interrupts may not be detected correctly if GIO_P_IN outputs 0 for a period shorter than one cycle of the interrupt monitor clock (GIO_INT_CLK). To detect such inputs, use asynchronous low level detection.

4.3.5 Synchronous both edge detection

Interrupts can be detected at both rising and falling edges of input port GIO_P_IN.
If an interrupt is detected, the corresponding interrupt source status bits (GIO_RAW and GIO_RAWP/GIO_RAWN) are set. Interrupts may not be detected correctly if the high or low level width of GIO_P_IN is shorter than one cycle of the interrupt monitor clock (GIO_INT_CLK). To detect such inputs, use asynchronous both edge detection.

4.3.6 Asynchronous rising edge detection

The interrupt source status bits (GIO_RAW and GIO_RAWP) are set at a rising edge of input port GIO_P_IN. Interrupts can be detected correctly even if GIO_P_IN goes into low level again within one cycle of the interrupt

monitor clock (GIO_INT_CLK) (high level width is 1T or shorter), because interrupts are detected asynchronously with the clock.

4.3.7 Asynchronous falling edge detection

The interrupt source status bits (GIO_RAW and GIO_RAWN) are set at a falling edge of input port GIO_P_IN. Interrupts can be detected correctly even if GIO_P_IN goes into high level again within one cycle of the interrupt monitor clock (GIO_INT_CLK) (low level width is 1T or shorter), because interrupts are detected asynchronously with the clock.

4.3.8 Asynchronous high level detection

The interrupt source status bit (GIO_RAW) is set if input port GIO_P_IN = 1 is detected. When the GIO_P_IN output becomes 0, the corresponding interrupt source status is automatically cleared. It is not cleared by setting up the interrupt source clear register (GIO_IIR).
Interrupts can be detected correctly even if GIO_P_IN outputs 1 for a period shorter than one cycle of the interrupt monitor clock (GIO_INT_CLK), because interrupts are detected asynchronously with the clock. If GIO_P_IN outputs 1 for a period shorter than one cycle of INT_CLK, however, the detected interrupt signal may disappear because the detected interrupt signal is synchronized with INT_CLK in the AINT macro.

4.3.9 Asynchronous low level detection

The interrupt source status bit (GIO_RAW) is set if input port GIO_P_IN = 0 is detected. When the GIO_P_IN output becomes 1, the corresponding interrupt source status is automatically cleared. It is not cleared by setting up the interrupt source clear register (GIO_IIR).
Interrupts can be detected correctly even if GIO_P_IN outputs 0 for a period shorter than one cycle of the interrupt monitor clock (GIO_INT_CLK), because interrupts are detected asynchronously with the clock. If GIO_P_IN outputs 0 for a period shorter than one cycle of INT_CLK, however, the detected interrupt signal may disappear because the detected interrupt signal is synchronized with INT_CLK in the AINT macro.

4.3.10 Asynchronous both edge detection

Interrupts can be detected at both rising and falling edges of input port input port GIO_P_IN. If an interrupt is detected, the corresponding interrupt source status bits (GIO_RAW and GIO_RAWP/GIO_RAWN) are set.
Interrupts can be detected correctly even if the high or low level width of GIO_P_IN is shorter than one cycle of the interrupt monitor clock (GIO_INT_CLK), because interrupts are detected asynchronously with the clock.

Table 4-3. Interrupt Detection Settings

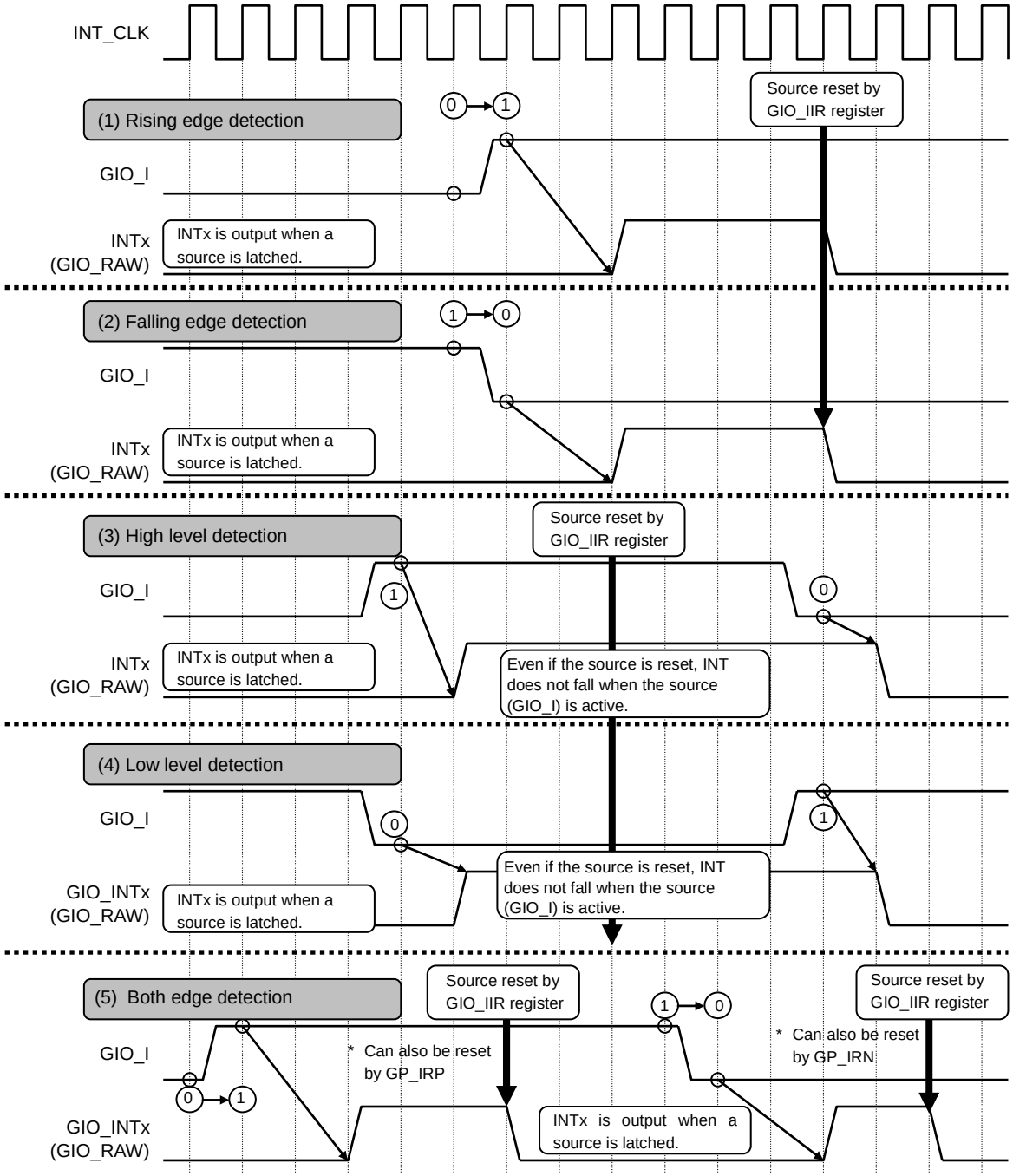
GIO_IDTx(3)	GIO_IDTx(2)	GIO_IDTx(1)	GIO_IDTx(0)	Detection Method
0	0	0	0	Synchronous rising edge detection
0	0	0	1	Synchronous falling edge detection
0	0	1	0	Synchronous high level detection
0	0	1	1	Synchronous low level detection
1	0	0	0	Asynchronous rising edge detection
1	0	0	1	Asynchronous falling edge detection
1	0	1	0	Asynchronous high level detection
1	0	1	1	Asynchronous low level detection
0	1	0	0	Synchronous both edge detection
1	1	0	0	Asynchronous both edge detection
Others				Setting prohibited (operation not guaranteed)
↑	↑	↑	↑	
Synchronous or asynchronous	Both edge of single edge	Edge detection or level detection	Positive/high or negative/low	

Remark If an interrupt is set and reset at the same time by the edge detection setting, reset takes precedence.

4.4 Interrupt Detection Timing (Synchronous Detection)

Figure 4-2 shows interrupt detection timing (synchronous detection).

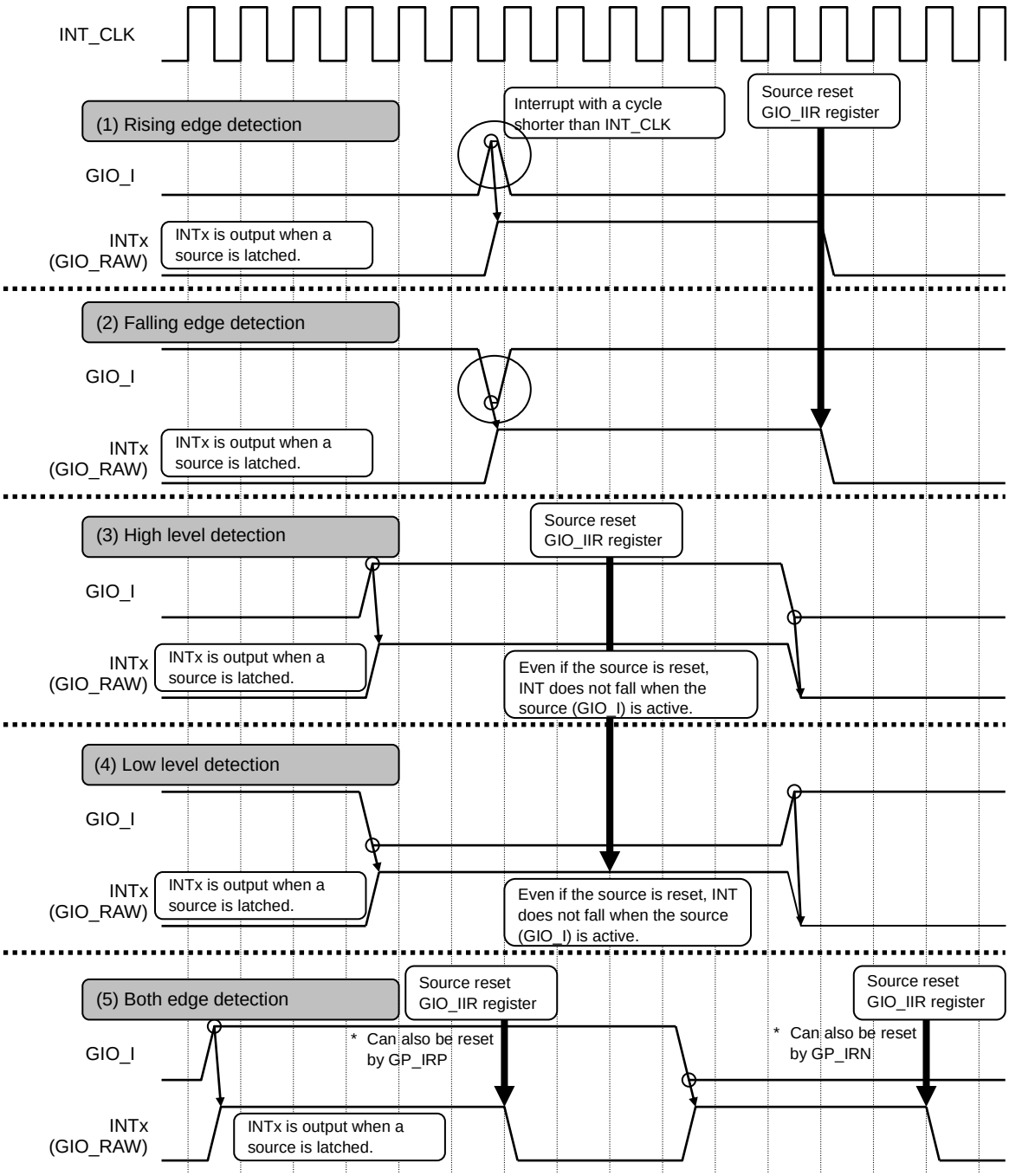
Figure 4-2. Interrupt Detection Timing (Synchronous Detection)



4.5 Interrupt Detection Timing (Asynchronous Detection)

Figure 4-3 shows interrupt detection timing (asynchronous detection).

Figure 4-3. Interrupt Detection Timing (Asynchronous Detection)



5. Usage

5.1 Input Port Interrupt Setup Procedure

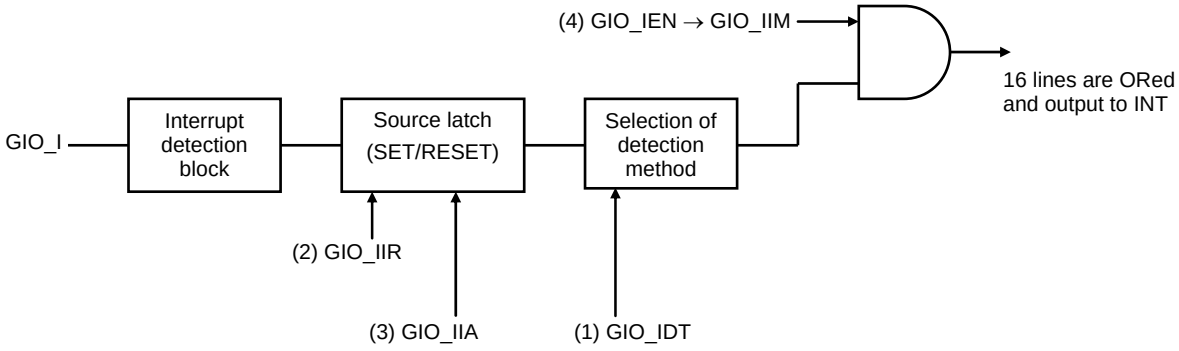
(1) Interrupt detection mode setup: Setting the relevant bits of the GIO_IDT register
(2) Interrupt source clear: Setting the relevant bits of the GIO_IIR register to 1
(3) Interrupt function = ON: Setting the relevant bits of the GIO_IIA register to 1
(4) Interrupt enable setup: Setting the relevant bits of the GIO_IEN register to 1

- The setting made to GIO_IDT takes effect at the relevant input port (interrupt occurs).
- GIOx_INT asserted: 0 → 1
  (x : 0 to 9)

(5) Interrupt source status read: GIO_MST, GIO_RAWBL and GIO_RAWBH registers (interrupt sources detected at rising and falling edges)
(6) Interrupt source clear: Setting of relevant bits of GIO_IIR and GIO_IRB registers (interrupt sources detected at either edge) to 1

- The relevant GIO_RAW, GIO_RAWBL and GIO_RAWBH registers are set to 0.
- GIOx_INT deasserted: 1 → 0
  (x : 0 to 9)

Figure 5-1. Interrupt Detection Overview



5.2 Cautions on Changing Interrupt Detection Mode

Before changing the settings of the input port interrupt detection mode registers (GIO_IDT), clear the GIO_IIA bit of the input port interrupt enable specification register to 0 (disables interrupt detection). The procedure is as follows.

(1) Interrupt function = OFF: Setting the relevant bits of the GIO_IIA register to 0
(2) Interrupt detection mode setup: Changing the setting of relevant bits of the GIO_IDT register
(3) Interrupt source clear: Setting the relevant bits of the GIO_IIR register to 1
(4) Interrupt function = ON: Setting the relevant bits of the GIO_IIA register to 1

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		Page	Summary
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2.00	Jun 7, 2010	—	Incremental update from comments to the 1.0.
3.00	Sep 30, 2010	—	Incremental update from comments to the 2.0. (A change part from the old revision is "★" marked in the page left end.)
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General-Purpose I/O Interface

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