User's Manual

ITU-R BT.656 Interface

User's Manual

Multimedia Processor for Mobile Applications
EMMA Mobile ™ EV2

Renesas Electronics
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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the EMMA Mobile EV2. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Data Sheet	Hardware overview and electrical characteristics	EMMA Mobile EV2 Datasheet	R19DS0010EJxxxx
User's manual (1chip)	Hardware whole specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description	EMMA Mobile EV2 User's manual 1chip	R19UH0036EJxxxx
User's manual (module)	Hardware each macro specifications and operation description.	EMMA Mobile EV2 User's manual each module	See below

Document Name	Document No.	Document Name	Document No.
1chip	R19UH0036EJxxxx	DMA Controller	R19UH0043EJxxxx
System Management Unit	R19UH0037EJxxxx	LP-DDR/DDR2 Controller	R19UH0039EJxxxx
Timer	R19UH0054EJxxxx	SD Memory Card Interface	R19UH0061EJxxxx
System Timer	R19UH0055EJxxxx	SDIO Interface	R19UH0042EJxxxx
HD Video Decoder	R19UH0056EJxxxx	CF Card Interface	R19UH0062EJxxxx
Rotator	R19UH0057EJxxxx	Unified Serial Interface	R19UH0047EJxxxx
Resizer	R19UH0058EJxxxx	UART interface	R19UH0040EJxxxx
Image Composer	R19UH0038EJxxxx	USB 2.0 Host Controller	R19UH0045EJxxxx
LCD Interface	R19UH0044EJxxxx	USB 2.0 Function Controller	R19UH0034EJxxxx
ITU-R BT.656 Interface (This manual)	R19UH0059EJxxxx	IIC Interface	R19UH0052EJxxxx
Digital Terrestrial TV Interface	R19UH0048EJxxxx	General Purpose I/O Interface	R19UH0041EJxxxx
Camera Interface	R19UH0060EJxxxx	Pulse Width Modulation Interface	R19UH0063EJxxxx

4 digits of end shows the version.

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names

Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.

Examples the PM03 bit in the PM0 register

P3_5 pin, VCC pin

(2) Notation of Numbers

The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.

Examples Binary: 11b or 11

Hexadecimal: EFA0h

Decimal: 1234

3. Register Notation

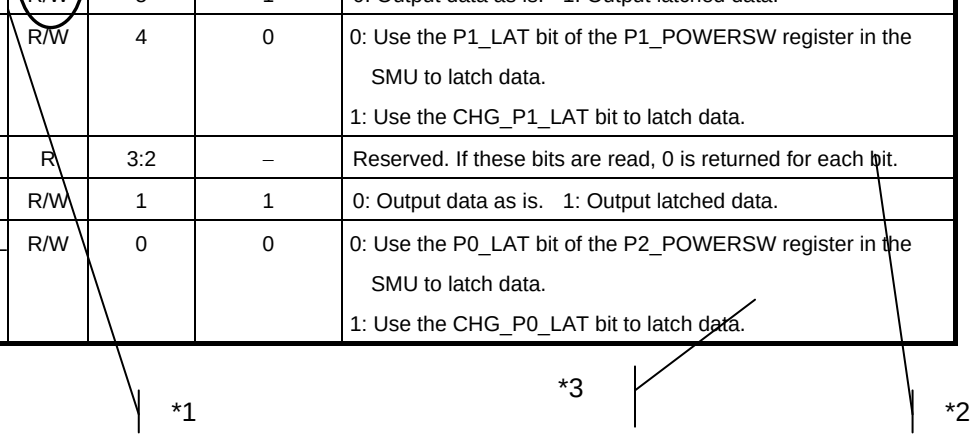
The symbols and terms used in register diagrams are described below.

x.x.x XXX register

This register (XXXXXXX: xxxx_xxxxh) …..

7	6	5	4	3	2	1	0
Reserved		CHG_P1_LAT	LATCH_P1_SEL	Reserved		CHG_P0_LAT	CHG_P0_LAT_SEL

Name	R/W	Bit No.	After Reset	Description
LATCH_P2_SEL	R/W	8	0	0: Use the P2_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P2_LAT bit to latch data.
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P1_LAT	R/W	5	1	0: Output data as is. 1: Output latched data.
LATCH_P1_SEL	R/W	4	0	0: Use the P1_LAT bit of the P1_POWERSW register in the SMU to latch data. 1: Use the CHG_P1_LAT bit to latch data.
Reserved	R	3:2	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P0_LAT	R/W	1	1	0: Output data as is. 1: Output latched data.
CHG_P0_LAT_SEL	R/W	0	0	0: Use the P0_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P0_LAT bit to latch data.



*1

R/W: Read and Write.

R: Read only.

W: Write only.

-: Nothing is assigned.

*2

Reserved bit.

Reserved bit. Set to specified value.

*3

・ Nothing is assigned.

Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.

・ Do not set to a value.

Operation is not guaranteed when a value is set.

・ Function varies according to the operating mode.

The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Register
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

Table of Contents

1. Overview

1.1 Features

NTS fetches YUV422-format image data from a frame buffer memory, converts it to the image to be output to the ITU-R BT.656-compliant parallel interface in synchronization with the internal timing signals, and outputs it to an external NTSC/PAL encoder IC.

(1) Supported standards

NTSC (525/60): Effective pixels: 720 × 486
PAL (625/50): Effective pixels: 720 × 576

(2) Output data format

ITU-R BT.656-compliant parallel data interface for data output

(3) Input image data format

YUV422 image data

(4) Gain adjustment

Internally adjusts the gain of the input YUV data to support ITU-R BT.601.

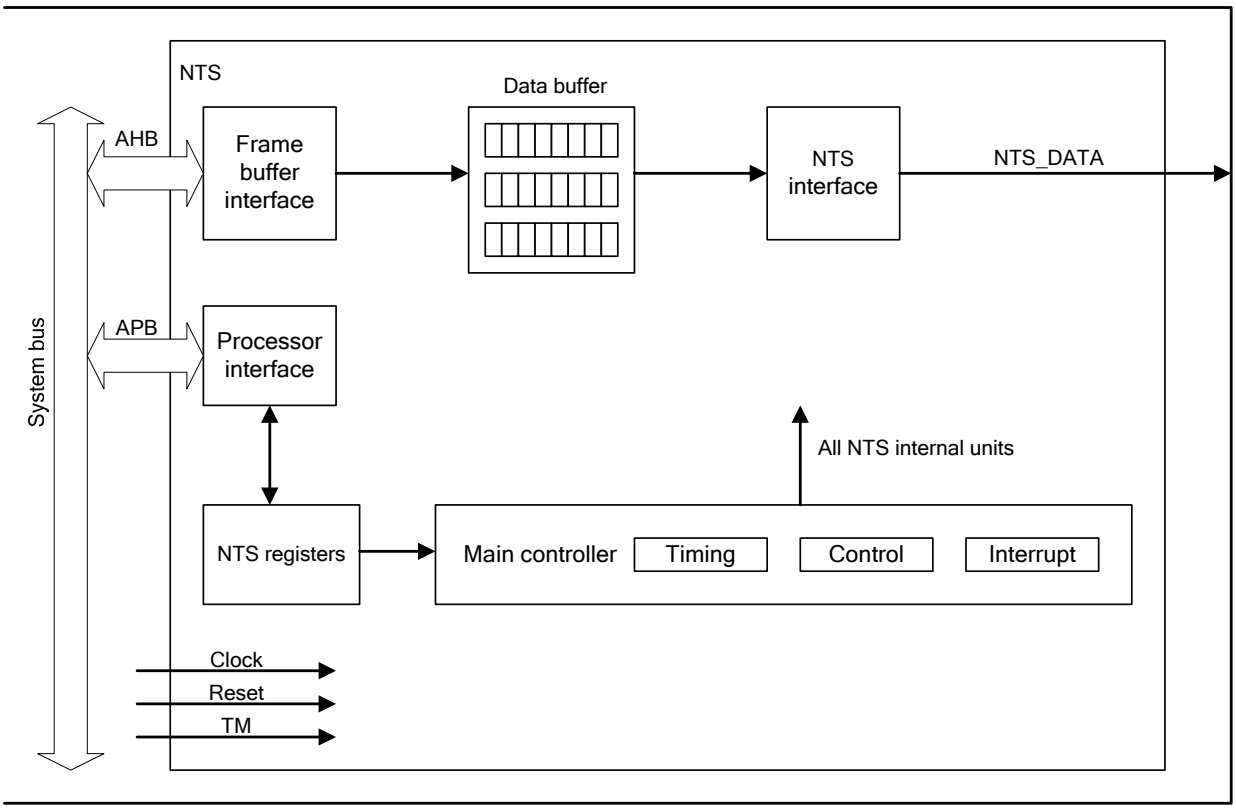
(5) Upscaling

Can double an image vertically and horizontally.

If images need not be expanded to NTSC/PAL size, such as when playing MPEG videos, a small image is generated in the memory and is quadrupled when transferred to the encoder IC. This function reduces internal processing during image generation and memory traffic.

1.2 Function Block Diagram

Figure 1-1. Function Block Diagram



2. Pin Functions

Pin Name	I/O	Function	Alternate Pin Function
NTSC_DATA0	Output	ITU-R BT.656-compliant parallel data Bit 0	GPIO_130
NTSC_DATA1	Output	ITU-R BT.656-compliant parallel data Bit 1	GPIO_129
NTSC_DATA2	Output	ITU-R BT.656-compliant parallel data Bit 2	GPIO_128
NTSC_DATA3	Output	ITU-R BT.656-compliant parallel data Bit 3	GPIO_127
NTSC_DATA4	Output	ITU-R BT.656-compliant parallel data Bit 4	GPIO_126
NTSC_DATA5	Output	ITU-R BT.656-compliant parallel data Bit 5	GPIO_125
NTSC_DATA6	Output	ITU-R BT.656-compliant parallel data Bit 6	GPIO_124
NTSC_DATA7	Output	ITU-R BT.656-compliant parallel data Bit 7	GPIO_123
NTSC_CLK	Input	ITU-R BT.656 interface control clock (27 MHz)	GPIO_122

3. Registers

The NTS registers allow word access only.
Do not access reserved registers.
Any value written to reserved bits in each register is ignored.

3.1 Register List

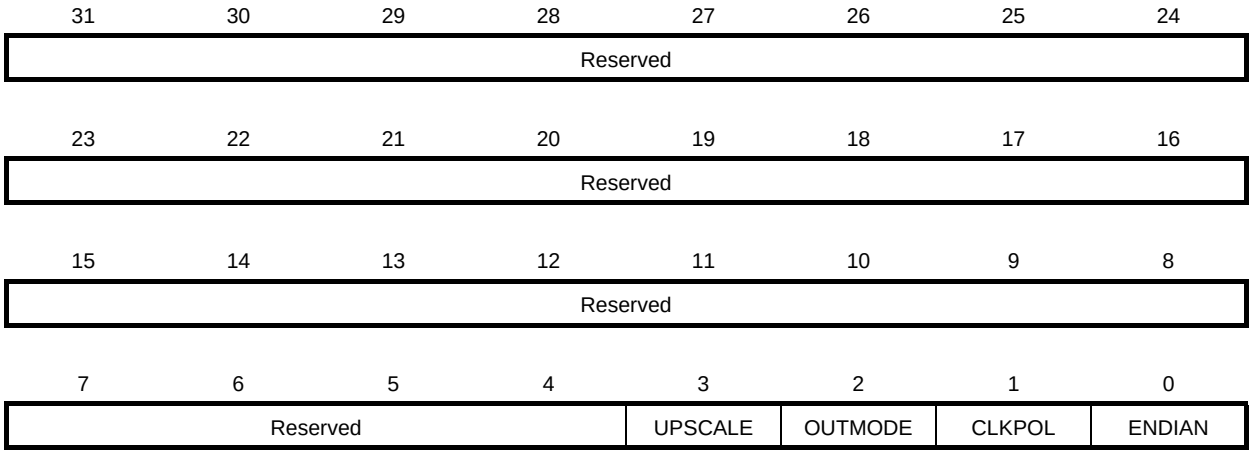
Base address: E121_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Control register	NTS_CONTROL	R/W	0000_0000H
0004H	Display register	NTS_OUT	R/W	0000_0000H
0008H	Status register	NTS_STATUS	R	0000_0000H
000CH	Display area address register YA	NTS_YAREAAD_A	R/W	0000_0000H
0010H	Display area address register YB	NTS_YAREAAD_B	R/W	0000_0000H
0014H	Display area address register YC	NTS_YAREAAD_C	R/W	0000_0000H
0018H	Display area address register UVA	NTS_UVAREAAD_A	R/W	0000_0000H
001CH	Display area address register UVB	NTS_UVAREAAD_B	R/W	0000_0000H
0020H	Display area address register UVC	NTS_UVAREAAD_C	R/W	0000_0000H
0024H	Address addition value register	NTS_HOFFSET	R/W	0000_0000H
0028H	Frame select register	NTS_FRAMESEL	R/W	0000_0001H
002CH-005CH	Reserved	–	–	–
0060H	Interrupt status register	NTS_INTSTATUS	R	0000_0000H
0064H	Interrupt raw status register	NTS_INTRAWSTATUS	R	0000_0000H
0068H	Interrupt enable set register	NTS_INTENSET	R/W	0000_0000H
006CH	Interrupt enable clear register	NTS_INTENCLR	W	0000_0000H
0070H	Interrupt source clear register	NTS_INTFFCLR	W	0000_0000H
0074H	Error address register	NTS_ERRORADR	R/W	0000_0000H
0078H	Software reset register	NTS_SWRESET	R/W	0000_0000H
007CH-FFFCH	Reserved	–	–	–

3.2 Register Details

3.2.1 Control register

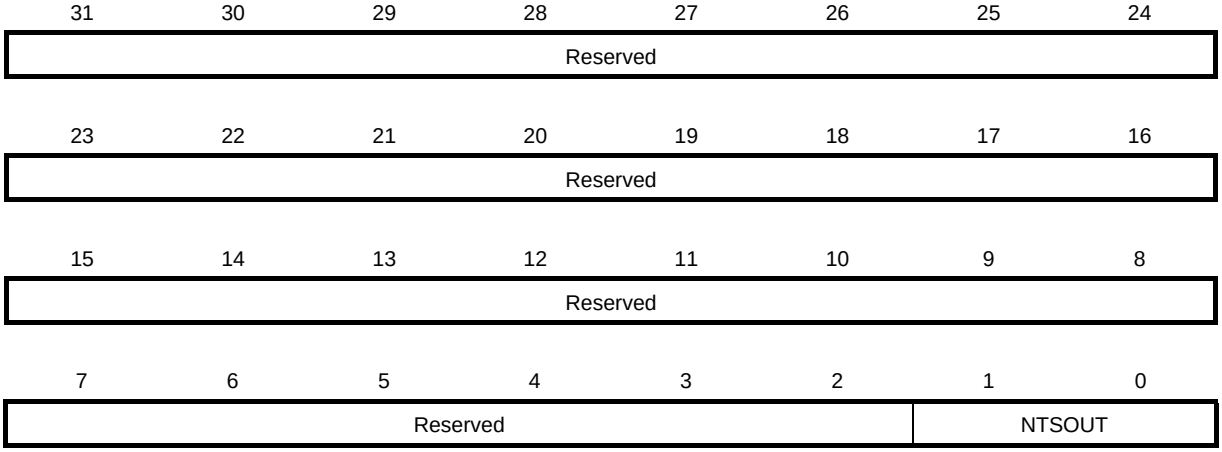
This register (NTS_CONTROL: E121_0000H) control NTS.



Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:4	000_0000H	Reserved. When these bits are read, 0 is returned for each bit.
UPSCALE	R/W	3	0	Specifies whether to enable the upscale (zoom) function. 0: Disable 1: Enable
OUTMODE	R/W	2	0	Selects the NTSC encoder interface output system. 0: NTSC (525/60) 1: PAL (625/60)
CLKPOL	R/W	1	0	Selects the phase of the NTS_CLKI (27 MHz). 0: Rising edge of NTS_CLKI 1: Falling edge of NTS_CLKI
ENDIAN	R/W	0	0	Specifies the endian of the image data being stored in the frame buffer memory. 0: Little endian 1: Big endian

3.2.2 Display register

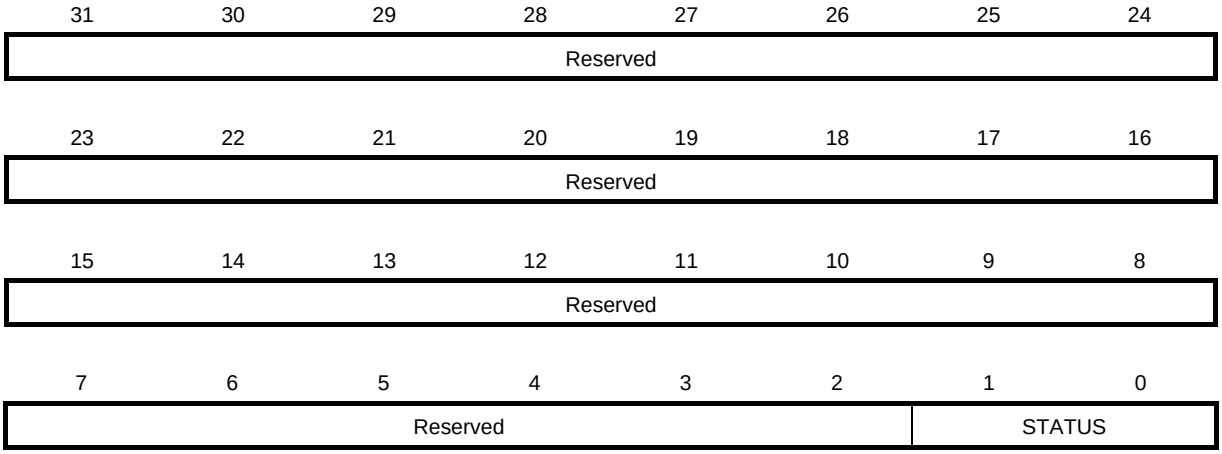
This register (NTS_OUT: E121_0004H) controls the data output to the NTS encoder interface.



Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:2	0000_0000H	Reserved. When these bits are read, 0 is returned for each bit.
NTSOUT	R/W	1:0	00b	Controls the data output to the NTS encoder interface. 00: OFF (all-0 data is output), without synchronization signal output 01: ON (BlackBack output), with synchronization signal output 10: ON (BlueBack output), with synchronization signal output 11: ON (Normal output), with synchronization signal output

3.2.3 Status register

This register (NTS_STATUS: E121_0008H) indicates the status of NTS. The status of the NTS output can be acquired by polling this register.



Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:2	0000_0000H	Reserved. When these bits are read, 0 is returned for each bit.
STATUS	R	1:0	00b	Indicates the NTS output status. 00: OFF (all-0 data is output), without synchronization signal output 01: ON (BlackBack output), with synchronization signal output 10: ON (BlueBack output), with synchronization signal output 11: ON (Normal output), with synchronization signal output

3.2.4 Display area address register

These registers (NTS_YAREAAD_A: E121_000CH, NTS_YAREAAD_B: E121_0010H, NTS_YAREAAD_C: E121_0014H) specify the head address of the Y-layer area in the frame buffer memory to which the YUV422-format image data is stored. A UV layer has three planes (A, B, and C), which have common specifications.

31	30	29	28	27	26	25	24
YAREAADA/B/C							

23	22	21	20	19	18	17	16
YAREAADA/B/C							

15	14	13	12	11	10	9	8
YAREAADA/B/C							

7	6	5	4	3	2	1	0
YAREAADA/B/C						0	0

Name	R/W	Bit No.	After Reset	Function
YAREAADA/B/C	R/W	31:2	0000_0000H	Specifies the head address of the frame buffer memory(Y layer). Specify the address by byte address on a 32-bit boundary.
–	R	1:0	0H	Fixed to 0. When these bits are read, 0 is returned for each bit.

3.2.5 Display area address register UV

These registers (NTS_UVAREAAD_A: E121_0018H, NTS_UVAREAAD_B: E121_001CH, NTS_UVAREAAD_C: E121_0020H) specify the head address of the UV-layer area in the frame buffer memory to which the YUV422-format image data is stored. A UV layer has three planes (A, B, and C), which have common specifications.

31	30	29	28	27	26	25	24
UVAREAADA/B/C							

23	22	21	20	19	18	17	16
UVAREAADA/B/C							

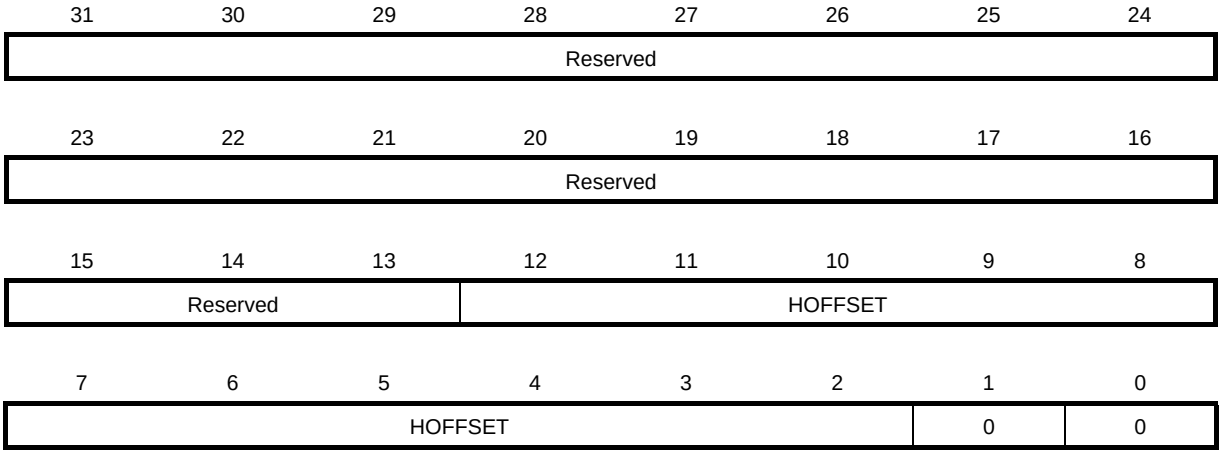
15	14	13	12	11	10	9	8
UVAREAADA/B/C							

7	6	5	4	3	2	1	0
UVAREAADA/B/C						0	0

Name	R/W	Bit No.	After Reset	Function
UVAREAADA/B/C	R/W	31:2	0000_0000H	Specifies the head address of the frame buffer memory (UV layer). Specify the address by byte address on a 32-bit boundary.
–	R	1:0	0H	Fixed to 0. When these bits are read, 0 is returned for each bit.

3.2.6 Address addition value register

This register (NTS_HOFFSET: E121_0024H) specifies the total number of bytes in the horizontal direction of frame buffer areas. The setting is commonly applied to frame buffers A, B and C.



Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:13	0_0000H	Reserved. When these bits are read, 0 is returned for each bit.
HOFFSET	R/W	12:0	0000H	Specifies the total number of bytes in the horizontal direction of the frame buffer areas. (The lower 2 bits are fixed to 0.)

3.2.7 Frame select register

This register (NTS_FRAMESEL: E121_0028H) selects display frame A, B, or C.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				AREASTATUS		AREASEL	

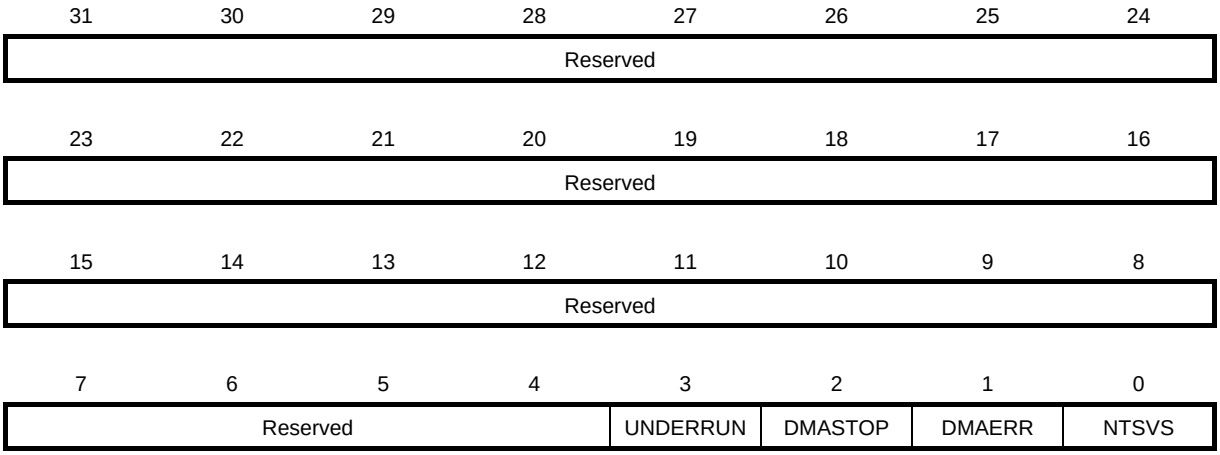
Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:4	000_0000H	Reserved. When these bits are read, 0 is returned for each bit.
AREASTATUS	R	3:2	00b	Indicates the frame currently being displayed. 00: Initial state 01: Frame buffer A 10: Frame buffer B 11: Frame buffer C
AREASEL	R/W	1:0	01b	Selects the frame buffer whose image is to be displayed. 00: Setting prohibited 01: Frame buffer A 10: Frame buffer B 11: Frame buffer C

3.2.8 Interrupt setting registers

These registers are used to specify various interrupt parameters. NTS uses four interrupts.

(1) Interrupt status register

This read-only register (NTS_INTSTATUS: E121_0060H) indicates the status of the interrupt sources. The status of the interrupt sources enabled by the interrupt enable set register can be read.



Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:4	000_0000H	Reserved. When these bits are read, 0 is returned for each bit.
UNDERRUN	R	3	0	Indicates the status of the underrun interrupt. 0: No interrupt source 1: Interrupt source occurred
DMASTOP	R	2	0	Indicates the status of the transfer stop interrupt. 0: No interrupt source 1: Interrupt source occurred
DMAERR	R	1	0	Indicates the status of the transfer error interrupt. 0: No interrupt source 1: Interrupt source occurred
NTSVS	R	0	0	Indicates the status of the NTS frame interrupt. 0: No interrupt source 1: Interrupt source occurred

(2) Interrupt raw status register

This read-only register (NTS_INTRAWSTATUS: E121_0064H) indicates the status of the interrupt sources. The bits corresponding to the interrupt sources are set regardless of the settings of the interrupt enable set register and the interrupt enable clear register.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

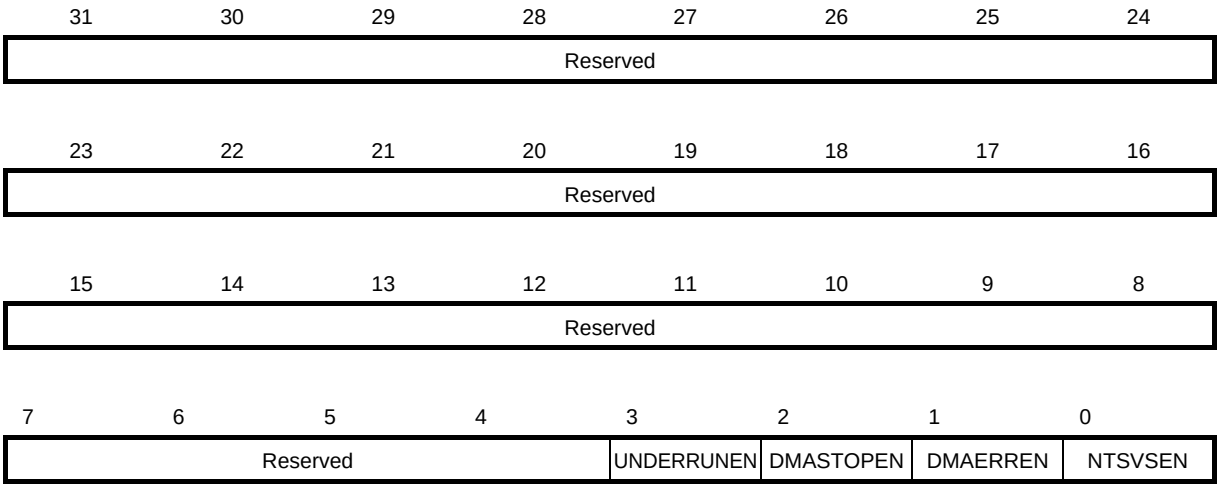
15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				UNDERRUN RAW	DMASTOP RAW	DMAERRRAW	NTSVSRAW

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:4	000_0000H	Reserved. When these bits are read, 0 is returned for each bit.
UNDERRUN RAW	R	3	0	Indicates the status of the underrun interrupt. 0: No interrupt source 1: Interrupt source occurred
DMASTOPRAW	R	2	0	Indicates the status of the transfer stop interrupt. 0: No interrupt source 1: Interrupt source occurred
DMAERRRAW	R	1	0	Indicates the status of the transfer error interrupt. 0: No interrupt source 1: Interrupt source occurred
NTSVSRAW	R	0	0	Indicates the status of the NTS frame interrupt. 0: No interrupt source 1: Interrupt source occurred

(3) Interrupt enable set register

This register (NTS_INTENSET: E121_0068H) enables issuance of interrupt requests. Only data of bits to which 1 is written is updated. When the bit corresponding to an interrupt source in this register is set to 1, the interrupt source is set, request for the interrupt is issued, and the corresponding bit of the interrupt status register is set to 1. If no bits are set to 1 in this register, no interrupt requests are issued even if an interrupt source is set, but the corresponding bit of the interrupt raw status register is set to 1.



Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:4	000_0000H	Reserved. When these bits are read, 0 is returned for each bit.
UNDERRUNEN	R	3	0	Indicates whether issuance of the underrun interrupt request is enabled. 0: Not enabled, 1: Enabled
	W	3	–	Enables issuance of the underrun interrupt request. 0: Ignored, 1: Enable interrupt.
DMASTOPEN	R	2	0	Indicates whether issuance of the transfer stop interrupt request is enabled. 0: Not enabled, 1: Enabled
	W	2	–	Enables issuance of the transfer stop interrupt request. 0: Ignored, 1: Enable interrupt.
DMAERREN	R	1	0	Indicates whether issuance of the transfer stop interrupt request is enabled. 0: Not enabled, 1: Enabled
	W	1	–	Enables issuance of the transfer stop interrupt request. 0: Ignored, 1: Enable interrupt.
NTSVSEN	R	0	0	Indicates whether issuance of the NTS frame interrupt request is enabled. 0: Not enabled, 1: Enabled
	W	0	–	Enables issuance of the NTS frame interrupt request. 0: Ignored, 1: Enable interrupt.

(4) Interrupt enable clear register

This write-only register (NTS_INTENCLR:E121_006CH) disables (masks) issuance of interrupt requests. If the bit corresponding to an interrupt source in this register is set to 1, no interrupt requests are issued even if the interrupt source is generated. The status of the corresponding bit in the interrupt status register also remains unchanged. If no bits are set to 1 in this register, an interrupt request is issued when an interrupt source is set, and the corresponding bit of the interrupt status register is set to 1. Writing 0 to this register does not affect the setting.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				UNDERRUN MASK	DMASTOP MASK	DMAERR MASK	NTSVSMASK

Name	R/W	Bit No.	After Reset	Function
Reserved	–	31:4	000_0000H	Reserved.
UNDERRUN MASK	W	3	0	Disables issuance of the underrun interrupt request. 1: Disable interrupt.
DMASTOPMASK	W	2	0	Disables issuance of the transfer stop interrupt request. 1: Disable interrupt.
DMAERRMASK	W	1	0	Disables issuance of the transfer stop interrupt request. 1: Disable interrupt.
NTSVSMASK	W	0	0	Disables issuance of the NTS frame interrupt request. 1: Disable interrupt.

(5) Interrupt source clear register

This write-only register (NTS_INTFFCLR: E121_0070H) requests clearing of interrupt sources. Setting the bit corresponding to an interrupt source to 1 clears the interrupt source. Writing 0 to this register does not affect the setting.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

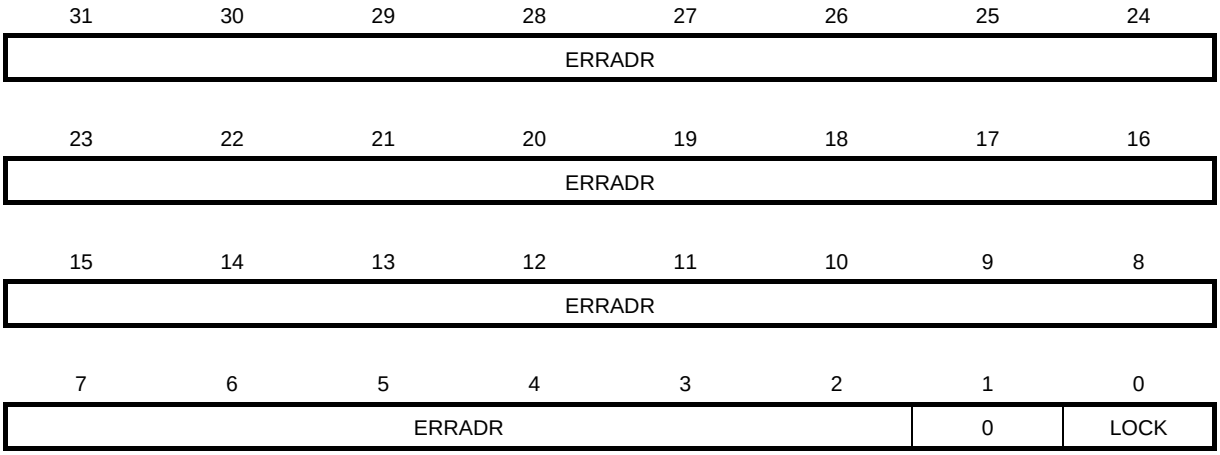
15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				UNDERRUNCLR	DMASTOPCLR	DMAERR CLR	NTSVS CLR

Name	R/W	Bit No.	After Reset	Function
Reserved	–	31:4	000_0000H	Reserved.
UNDERRUN CLR	W	3	0	Requests clearing of the source of the underrun interrupt. 1: Clears the interrupt source.
DMASTOPC LR	W	2	0	Requests clearing of the source of the transfer stop interrupt. 1: Clears the interrupt source.
DMAERRCLR	W	1	0	Requests clearing of the source of the transfer error interrupt. 1: Clears the interrupt source.
NTSVSCLR	W	0	0	Requests clearing of the source of the NTS frame interrupt. 1: Clears the interrupt source.

(6) Error address register

This register (NTS_ERRORADR: E121_0074H) retains the current HADDR status when an internal bus response ERROR, RETRY, or SPLIT is received during DMA transfer.



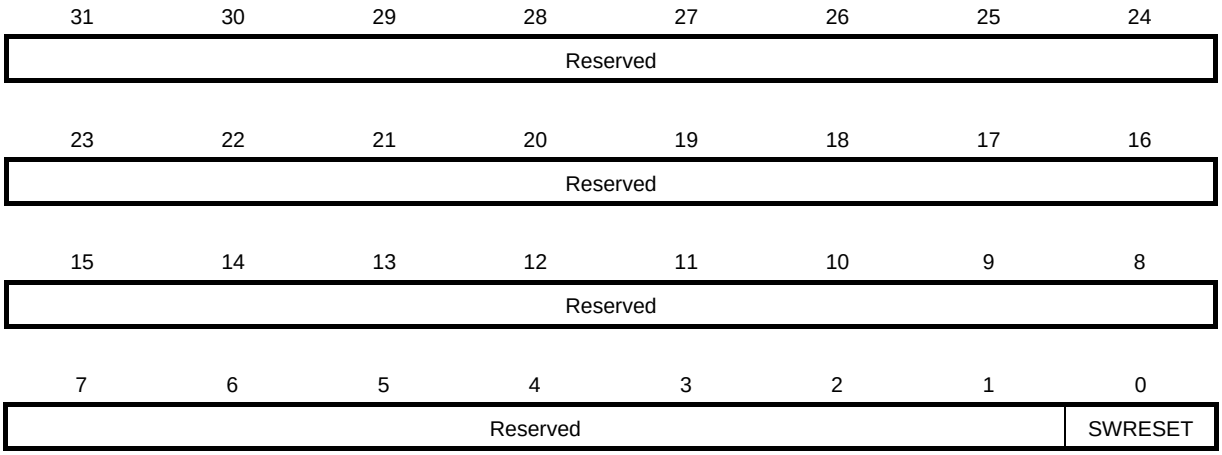
Name	R/W	Bit No.	After Reset	Function
ERRADR	R	31:2	0000_0000H	Stores HADDR upon occurrence of an error response.
Reserved	R	1	0	Reserved. When this bit is read, 0 is returned.
LOCK	R/W	0	0	Error status 0: Stores the address when an error response occurs. 1: An error response occurred and the address was stored.

Caution If an error response occurs when the LOCK bit is 0, the current HADDR status is stored in the ERRADR bit and the LOCK bit is set to 1. To acquire the error status again, set the LOCK bit to 0.
Writing 1 to the LOCK bit does not affect the setting.

(7) Software reset register

This register (NTS_SWRESET: E121_0078H) is used for switching the phase of the NTS_CLKI (27 MHz) clock.

This register resets the circuit operating at 27 MHz before the NTS_CLK phase is switched by using the CLKPOL bit of the control register (NTS_CONTROL). Cancel this setting after changing the phase.



Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:1	0000_0000H	Reserved. When these bits are read, 0 is returned for each bit.
SWRESET	R/W	0	0	Specifies whether to enable software reset. 0: Disables reset. 1: Enables reset.

4. Description of Functions

4.1 NTS Encoder Interface

The ITU-R BT.656-compliant format uses the interlace system where a single screen (frame) consists of two fields. This system does not use the vertical synchronizing (VD) and horizontal synchronizing (HD) signals for synchronizing the image, but recognizes the effective pixel area by using the two timing reference signals SAV (start of active video) and EAV (end of active video), included in the data stream, for the synchronization.
SAV and EAV each consist of 3-byte preamble data (FF/00/00) and 1-byte timing reference data.
The following table lists the timing for the NTSC system and PAL system.

Table 4-1. Video Timing Reference Codes

Data[7:0] Bit Number	1st Word (FF)	2nd Word (00)	3rd Word (00)	4th Word (XY)
7 (MSB)	1	0	0	1
6	1	0	0	F
5	1	0	0	V
4	1	0	0	H
3	1	0	0	P3
2	1	0	0	P2
1	1	0	0	P1
0	1	0	0	P0

F = 0: Field 1 is being accessed F = 1: Field 2 is being accessed
V = 0: Not in a field blanking interval V = 1: In a field blanking interval
H = 0: SAV, H = 1: EAV
P3 to P0: Protection bits
P3 = V EXOR H
P2 = F EXOR H
P1 = F EXOR V
P0 = F EXOR V EXOR H

(1) NTSC system

Figure 4-1. Data Format in NTSC System

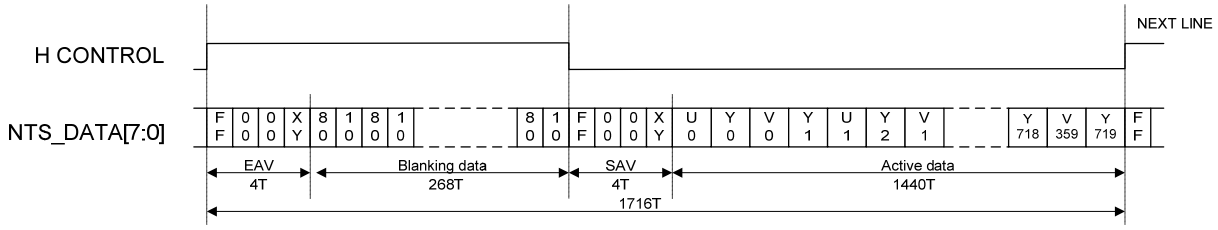
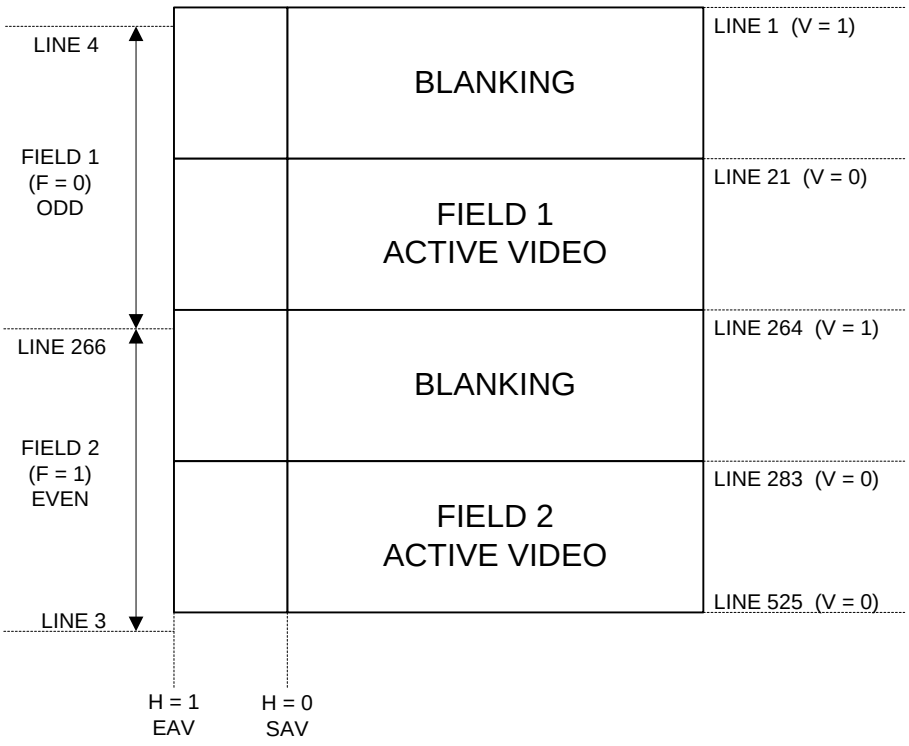


Table 4-2. SAV and EAV Setting Values in NTSC System

Line No.	SAV: XY Value								EAV: XY Value							
NTSC	1	F	V	H	P3	P2	P1	P0	1	F	V	H	P3	P2	P1	P0
1 to 3	1	1	1	0	1	1	0	0	1	1	1	1	0	0	0	1
4 to 19	1	0	1	0	1	0	1	1	1	0	1	1	0	1	1	0
20 to 263	1	0	0	0	0	0	0	0	1	0	0	1	1	1	0	1
264 to 265	1	0	1	0	1	0	1	1	1	0	1	1	0	1	1	0
266 to 282	1	1	1	0	1	1	0	0	1	1	1	1	0	0	0	1
283 to 525	1	1	0	0	0	1	1	1	1	1	0	1	1	0	1	0

Figure 4-2. Vertical Blanking Interval in NTSC System



(2) PAL system

Figure 4-3. Data Format in PAL System

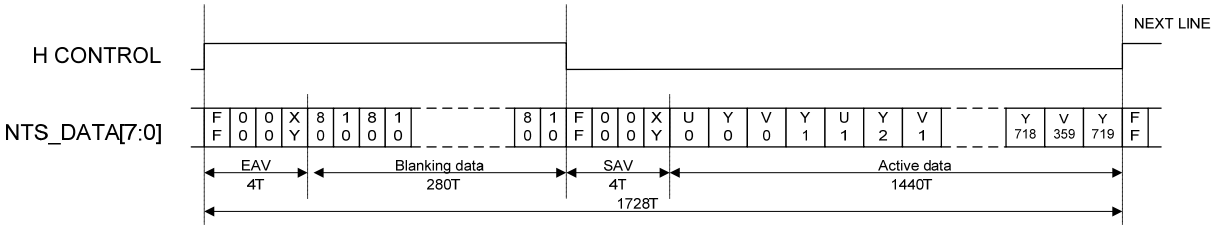
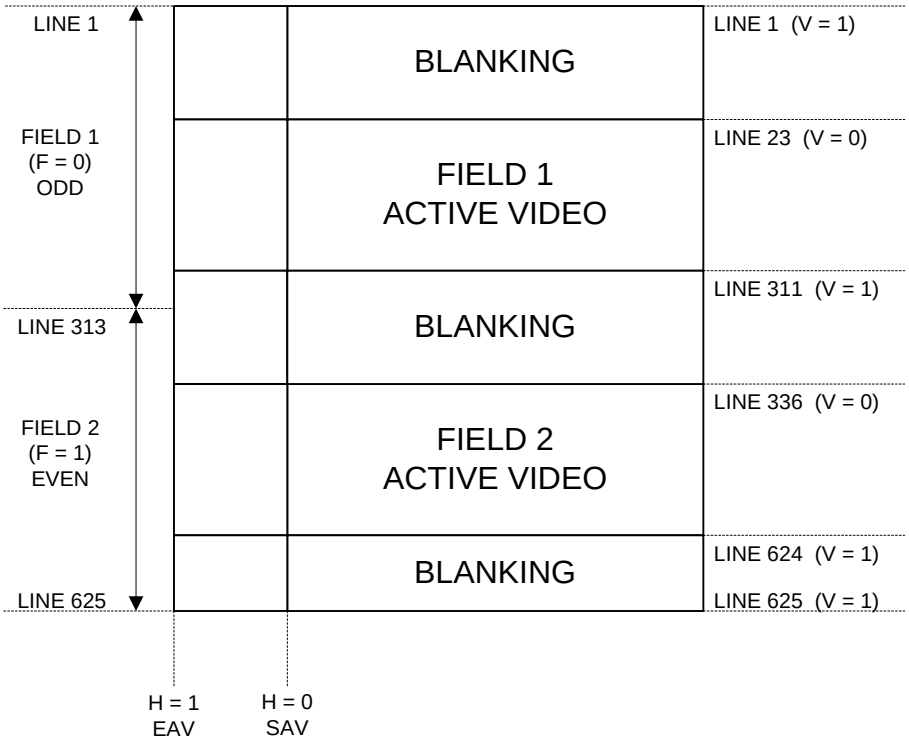


Table 4-3. SAV and EAV Setting Values in PAL System

Line No.	SAV: XY Value								EAV: XY Value							
PAL	1	F	V	H	P3	P2	P1	P0	1	F	V	H	P3	P2	P1	P0
1 to 22	1	0	1	0	1	0	1	1	1	0	1	1	0	1	1	0
23 to 310	1	0	0	0	0	0	0	0	1	0	0	1	1	1	0	1
311 to 312	1	0	1	0	1	0	1	1	1	0	0	1	1	1	1	0
313 to 335	1	1	1	0	1	1	0	0	1	1	1	1	0	0	0	1
336 to 623	1	1	0	0	0	1	1	1	1	1	0	1	1	0	1	0
624 to 625	1	1	1	0	1	1	0	0	1	1	1	1	0	0	0	1

Figure 4-4. Vertical Blanking Interval in PAL System



4.1.1 Generating synchronization signals

The horizontal-direction timing control signal is generated by using an 11-bit counter that operates with the NTS_CLKI clock.

The vertical-direction timing control signal is generated by using a 10-bit counter that operates with the generated horizontal-direction timing control signal.

Figure 4-5. Relationship Between Horizontal- and Vertical-Direction Timing Control Signals in NTSC System

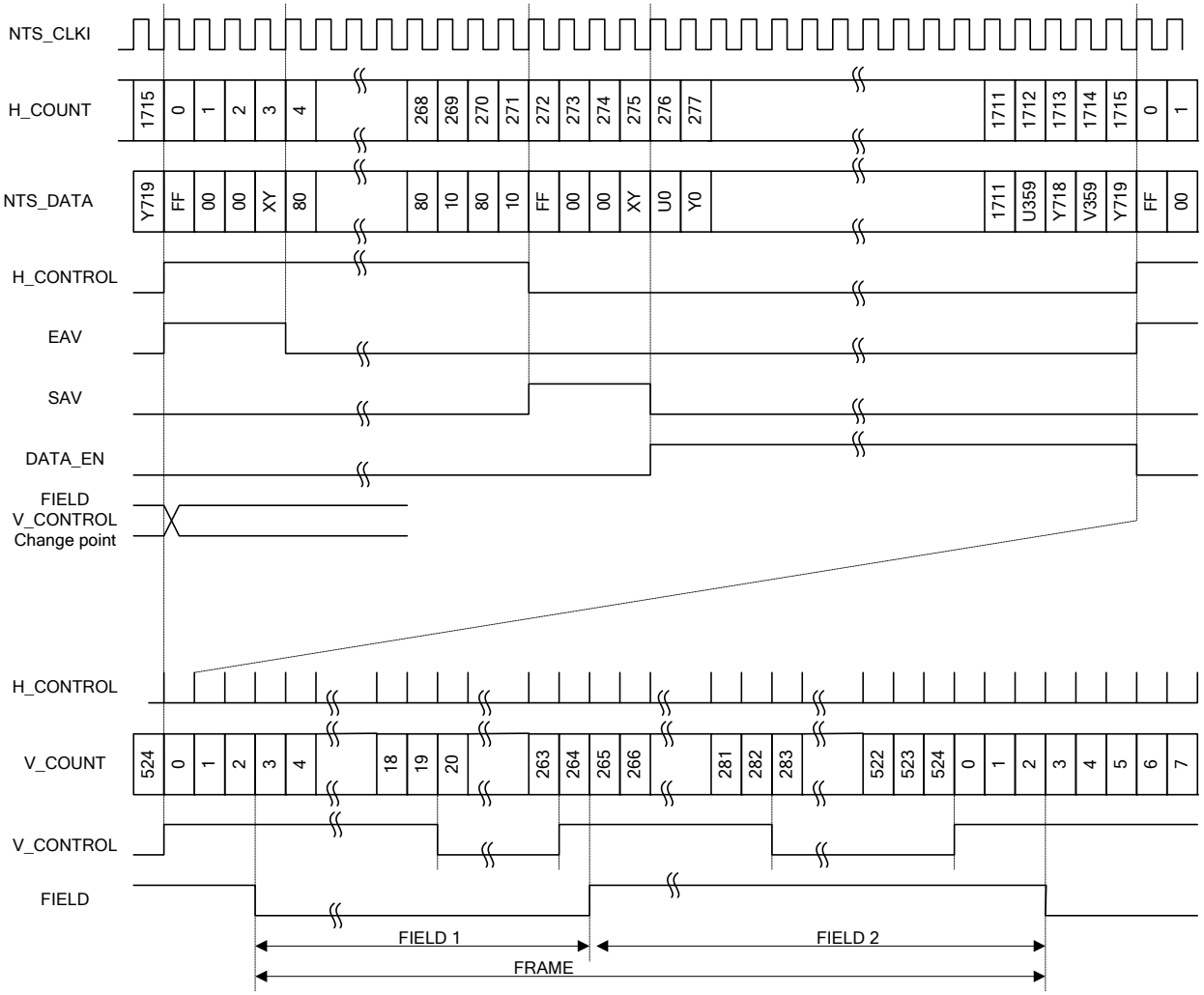
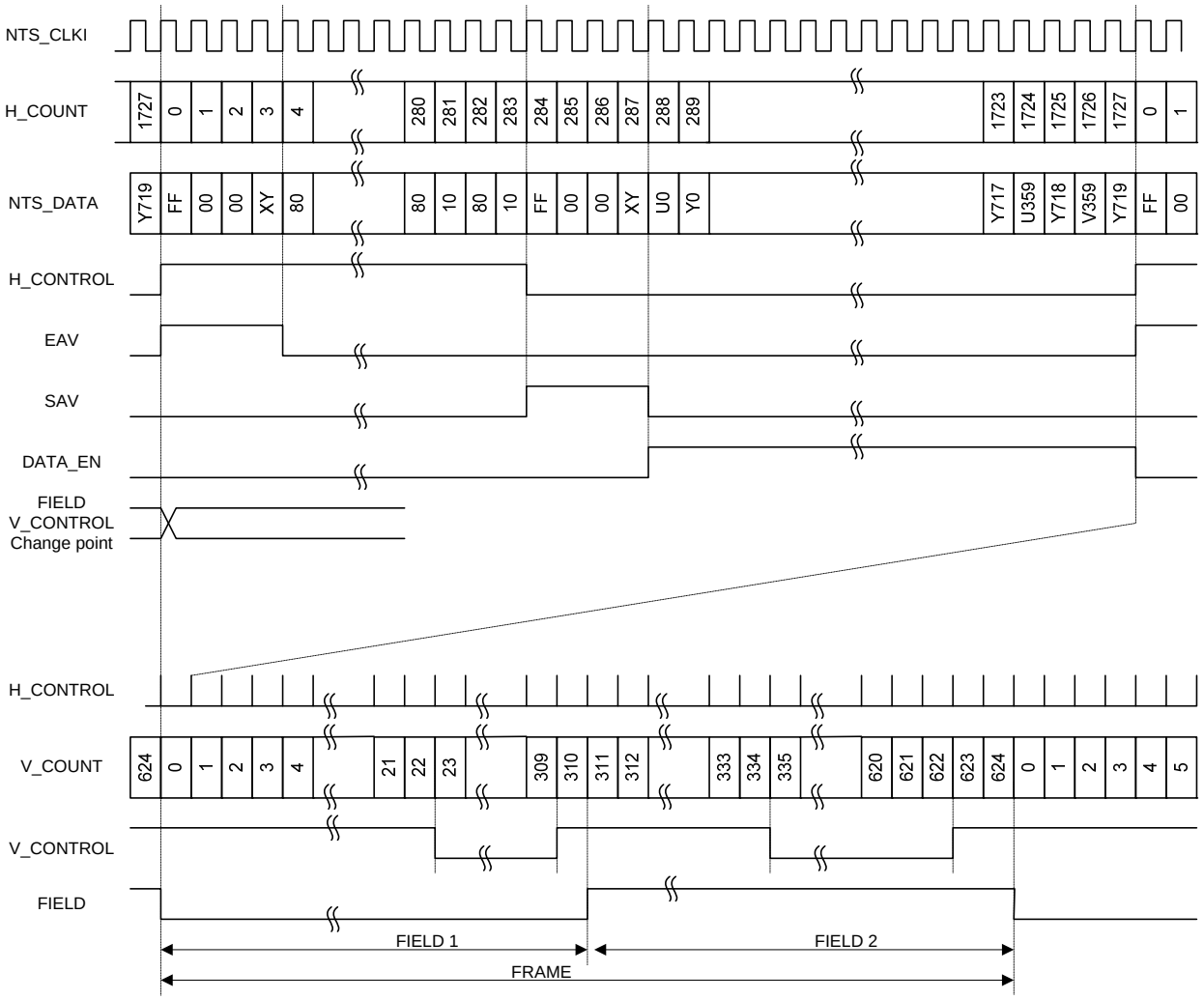


Figure 4-6. Relationship Between Horizontal- and Vertical-Direction Timing Control Signals in PAL System



4.1.2 Adjusting the phase of control clock (NTS_CLKI)

The timing of outputting NTS_DATA can be selected from the rising or falling edge of the NTS_CLKI clock by setting the CLKPOL bit of the NTS_CONTROL register. The NTS_DATA signal is output in synchronization with the rising edge of the NTS_CLKI clock when CLKPOL is set to 0, and with the falling edge when CLKPOL is set to 1.

As a result of this adjustment, the phase of circuits operating at 27 MHz is changed. To prevent the internal circuits from malfunctioning, reset the circuits operating at 27 MHz by using the software reset register (NTS_SWRESET) before phase adjustment, and cancel the reset after adjustment.

Figure 4-7. Synchronization with Rising Edge of NTS_CLKI

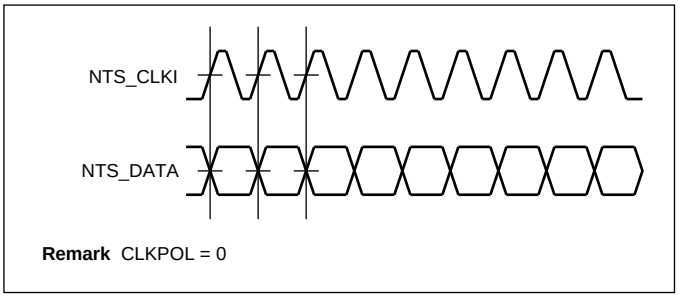
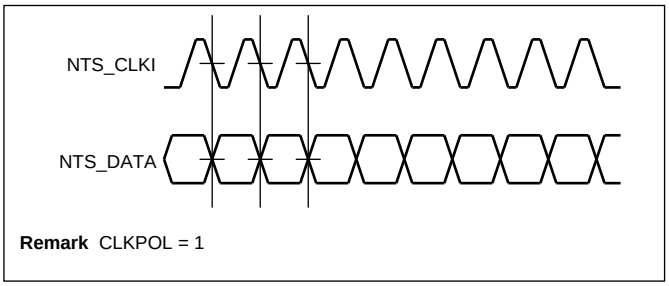


Figure 4-8. Synchronization with Falling Edge of NTS_CLKI



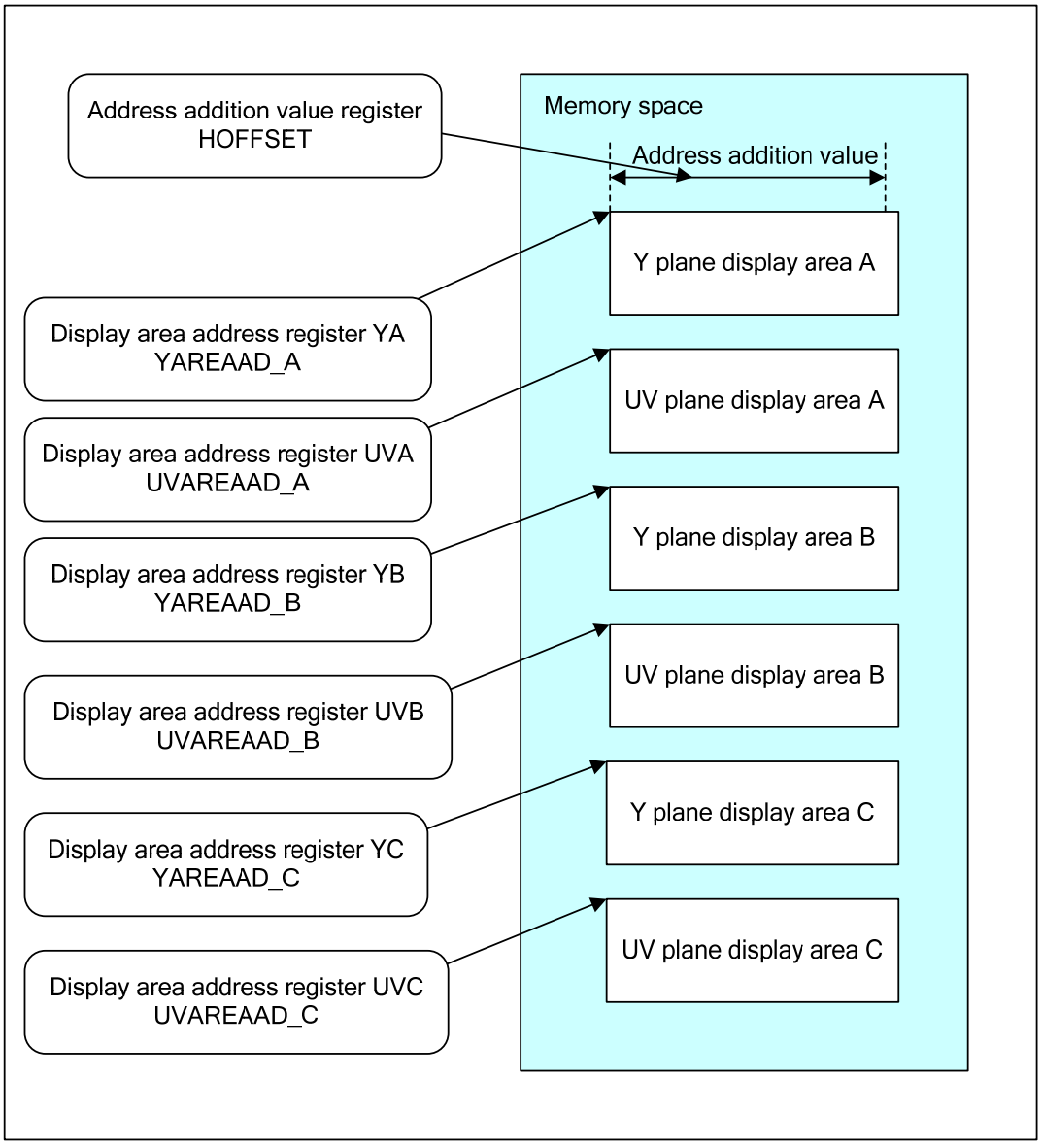
4.2 Frame Buffer and Data Buffer

4.2.1 Frame buffer

Frame buffer is generic term used to refer to a buffer storing a single screen of image data. There are three frame buffers, defined as frame buffers A, B, and C. The display area address registers Y (NTS_YAREAAD_A/B/C) and the display area address registers UV (NTS_UVAREAAD_A/B/C) correspond to frame buffers A, B, and C, respectively, and any address can be set by using these registers. The address addition value register (NTS_HOFFSET) can be used to specify the horizontal size of the frame buffer area in word (2 bytes) units. By this means, a rectangle area clipped from the frame buffer, which has been mapped in a size larger than the display image size, can be output to NTS. (The parameter of address addition value is common to frame buffers A, B, and C.)

Frame buffers A, B, and C are never accessed at the same time. One frame buffer is selected by an order of the processor.

Figure 4-9. Image of Frame Buffer



4.2.2 Frame buffer storage format

Frame buffers store YUV422-format image data. The storage data format is shown below. The endian type for the bus can be specified by using the ENDIAN bit of the NTS_CONTROL register.

Data size: The same size for Y and UV planes.
Y Plane: Data size is X size × Y size bytes for the data at 1 pixel per byte.
UV Plane: Data size is X size × Y size bytes for the data at 2 pixels per byte for UV individually.

The following shows the file images when X size = n, Y size = m, and the number of images is 1.

(1) Little endian

- **Y plane**

Y[0]	Y[1]	Y[2]	Y[3]	Y[4]	Y[5]	.	.	.		Y[14]	Y[15]
Y[16]	Y[17]										
.											
.											
.											
											Y[nxm-1]

- **UV plane**

U[0]	V[0]	U[1]	V[1]	U[2]	V[2]	.	.	.		U[7]	V[7]
U[8]	V[8]										
.											
.											
.											
										U[nxm/2-1]	V[nxm/2-1]

(2) Big endian

- **Y plane**

Y[1]	Y[0]	Y[3]	Y[2]	Y[5]	Y[4]	.	.	.		Y[15]	Y[14]
Y[17]	Y[16]										
.											
.											
.											
										Y[nxm-1]	Y[nxm-2]

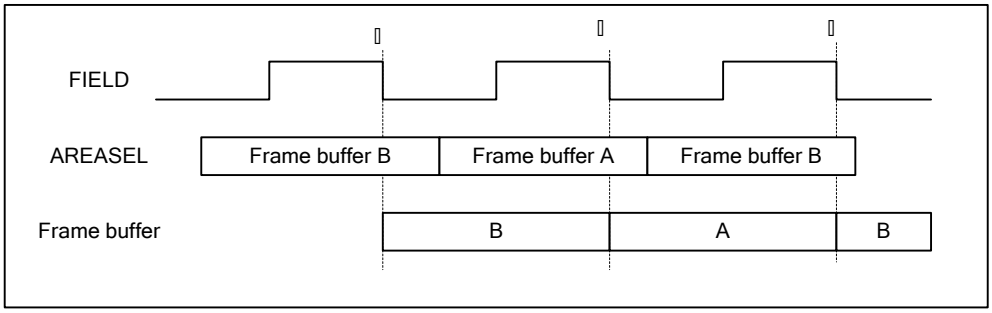
- **UV plane**

V[0]	U[0]	V[1]	U[1]	V[2]	U[2]	.	.	.		V[7]	U[7]
V[8]	U[8]										
.											
.											
.											
										V[nxm/2-1]	U[nxm/2-1]

4.2.3 Switching frame buffers

The AREASEL bit of the frame select register (NTS_FRAMESEL) can be used to switch the frame buffers. The frame buffers are switched at the start of a frame (frame display start signal).

Figure 4-10. Frame Buffer Switching Timing

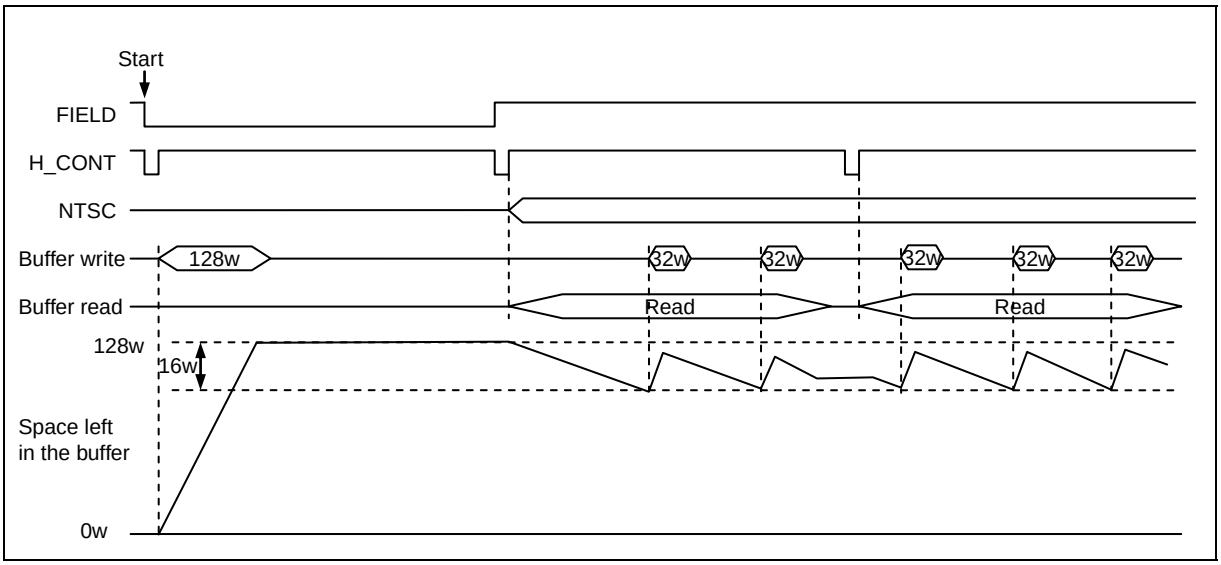


4.2.4 Data buffer

Data buffer is an NTS internal buffer that fetches the image data sent from the frame buffer by burst transfer. The data buffer is a 32-bit × 128- word FIFO buffer with two ports (1R and 1W). If there is an available space of 64 bytes in the data buffer, data is written to the data buffer from the write port via the frame buffer interface. The read port is used to read (display) data from NTS.

The data buffer is accessed as shown in Figure 4-11. First, image data is written to the data buffer via the frame buffer interface. NTS reads the image data from the area where it was written, and displays the image. The image data is written to the frame buffer if the data buffer has an available space of 64 bytes. If the speed of reading the data buffer by NTS is faster than the buffer write speed, an underrun interrupt occurs.

Figure 4-11. Data Buffer Access



Caution If the burst transfer rate is not fast enough in comparison with the NTS image refresh rate, the image data amount is insufficient, which results in a fatal image deterioration.
To avoid this, determine the clock cycle so that the following expression is sufficiently met.
NTS_CLKI clock << AHB clock

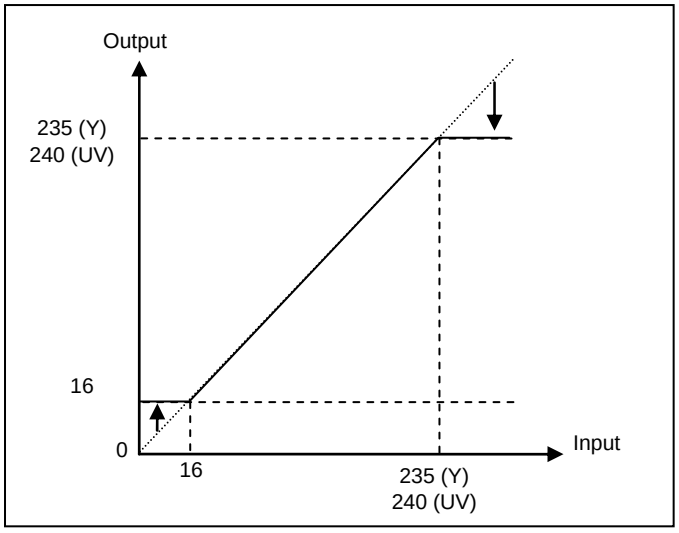
4.2.5 Gain adjustment

To comply with ITU-R BT.601, a gain is internally adjusted for the input YUV data. The following shows the method.

Restrict the image data, which is input with values 0 to 255, to the range of 16 to 240.

Restrict Y data to the range of 16 to 235, and UV data to the range of 16 to 240. The values out of the range are fixed to 0.

Figure 4-12. YUV Data Gain Adjustment



4.3 Interrupt Sources

Control of each interrupt is assigned to each bit of the interrupt setting registers.

Table 4-4. Interrupt Sources

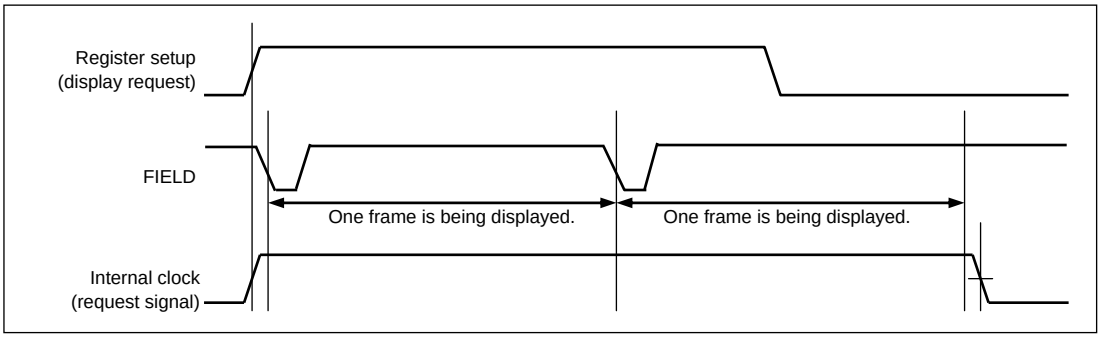
Interrupt Name	Source	Bit Assignment
Underrun interrupt	Generated when an underrun occurs in the NTS internal data buffer.	3
Transfer stop interrupt	Generated when a RETRY or SPLIT response is received during AHB transfer.	2
Transfer error interrupt	Generated when an ERROR response is received during AHB transfer, after a single NTSC image of display data has been output.	1
NTS frame interrupt	Generated when the frame display is started.	0

Generation of an NTS frame interrupt is triggered by the frame display start signal. If register settings are changed immediately after an NTS frame interrupt occurs, the change is enabled from the next and subsequent frames.

4.4 Clock Control

EM/EV0 is designed for low power consumption, so it controls the clock supply on a module basis.
A clock is supplied when a module requests a clock or a register is accessed to request a clock.
For the NTSC system, a clock supply request is issued if the display register (NTS_OUT) is set to 1.
When a display frame ends with no display requests (the NTS_OUT register is 0), the clock supply request is canceled. The following shows the timing of requesting clock supply.

Figure 4-13. Clock Supply Timing



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