User's Manual

Digital Terrestrial TV Interface

User's Manual

Multimedia Processor for Mobile Applications
EMMA Mobile ™ EV2

Renesas Electronics
www.renesas.com

Rev.7.00 Dec 2011

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the EMMA Mobile EV2. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Data Sheet	Hardware overview and electrical characteristics	EMMA Mobile EV2 Datasheet	R19DS0010EJxxxx
User's manual (1chip)	Hardware whole specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description	EMMA Mobile EV2 User's manual 1chip	R19UH0036EJxxxx
User's manual (module)	Hardware each macro specifications and operation description.	EMMA Mobile EV2 User's manual each module	See below

Document Name	Document No.	Document Name	Document No.
1chip	R19UH0036EJxxxx	DMA Controller	R19UH0043EJxxxx
System Management Unit	R19UH0037EJxxxx	LP-DDR/DDR2 Controller	R19UH0039EJxxxx
Timer	R19UH0054EJxxxx	SD Memory Card Interface	R19UH0061EJxxxx
System Timer	R19UH0055EJxxxx	SDIO Interface	R19UH0042EJxxxx
HD Video Decoder	R19UH0056EJxxxx	CF Card Interface	R19UH0062EJxxxx
Rotator	R19UH0057EJxxxx	Unified Serial Interface	R19UH0047EJxxxx
Resizer	R19UH0058EJxxxx	UART interface	R19UH0040EJxxxx
Image Composer	R19UH0038EJxxxx	USB 2.0 Host Controller	R19UH0045EJxxxx
LCD Interface	R19UH0044EJxxxx	USB 2.0 Function Contoller	R19UH0034EJxxxx
ITU-R BT.656 Interface	R19UH0059EJxxxx	IIC Interface	R19UH0052EJxxxx
Digital Terrestrial TV Interface (This manual)	R19UH0048EJxxxx	General Purpose I/O Interface	R19UH0041EJxxxx
Camera Interface	R19UH0060EJxxxx	Pulse Width Modulation Interface	R19UH0063EJxxxx

4 digits of end shows the version.

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names

Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.

Examples the PM03 bit in the PM0 register

P3_5 pin, VCC pin

(2) Notation of Numbers

The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.

Examples Binary: 11b or 11

Hexadecimal: EFA0h

Decimal: 1234

3. Register Notation

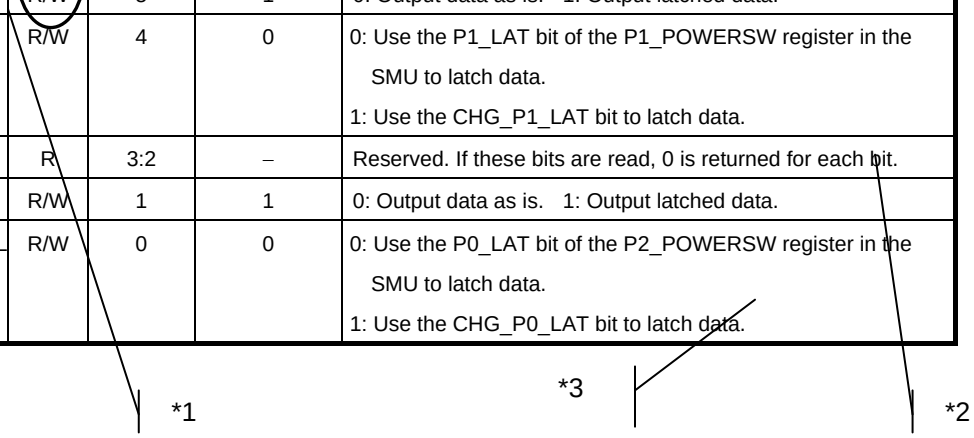
The symbols and terms used in register diagrams are described below.

x.x.x XXX register

This register (XXXXXXX: xxxx_xxxxh) …..

7	6	5	4	3	2	1	0
Reserved		CHG_P1_LAT	LATCH_P1_SEL	Reserved		CHG_P0_LAT	CHG_P0_LAT_SEL

Name	R/W	Bit No.	After Reset	Description
LATCH_P2_SEL	R/W	8	0	0: Use the P2_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P2_LAT bit to latch data.
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P1_LAT	R/W	5	1	0: Output data as is. 1: Output latched data.
LATCH_P1_SEL	R/W	4	0	0: Use the P1_LAT bit of the P1_POWERSW register in the SMU to latch data. 1: Use the CHG_P1_LAT bit to latch data.
Reserved	R	3:2	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P0_LAT	R/W	1	1	0: Output data as is. 1: Output latched data.
CHG_P0_LAT_SEL	R/W	0	0	0: Use the P0_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P0_LAT bit to latch data.



*1

R/W: Read and Write.

R: Read only.

W: Write only.

-: Nothing is assigned.

*2

Reserved bit.

Reserved bit. Set to specified value.

*3

・ Nothing is assigned.

Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.

・ Do not set to a value.

Operation is not guaranteed when a value is set.

・ Function varies according to the operating mode.

The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Register
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

Abbreviation	Full Form
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
CAM	Camera Interface Module
FIFO	First In, First Out
GPIO	General Purpose I/O
USI	Unified Serial Interface

Table of Contents

1. Overview

The digital terrestrial television interface (DTV interface) has a function to transfer stream data sent from an externally connected digital terrestrial TV channel decoder LSI to memory, via DMA. The DTV interface only supports burst output (serial) mode.

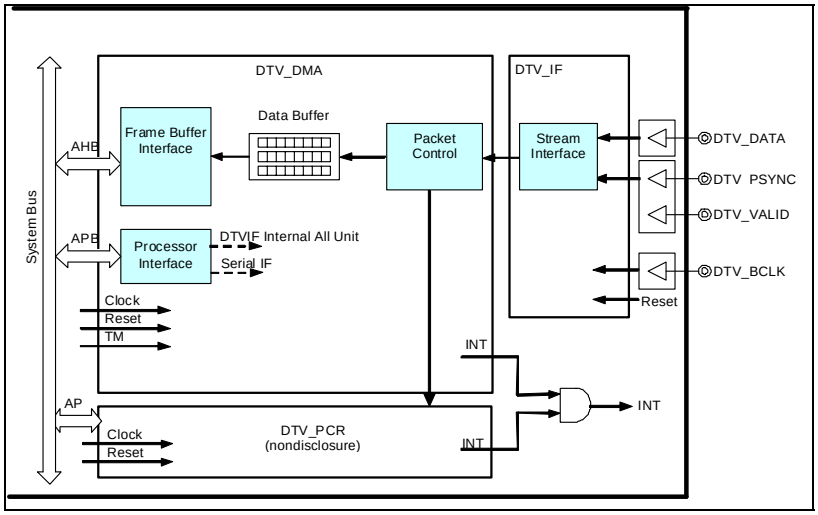
1.1 Features

The main features of DTV are as follows.
The DTV interface only supports serial output.

- ○ DTV interface signals
  - DTV_DATA is used in the serial output mode.
  - Packet synchronization pulse (DTV_PSYNC)
  - Stream data enable signal (DTV_VALID)
  - DTV interface clock (DTV_BCLK)
- ○ DMA transfer destination buffer
  - A ring buffer area can be specified.
- ○ Reception data selection
  - Whether to receive parity fields can be selected.
- ○ Buffer memory
  - A buffer memory of 32 bits × 4 words is incorporated.

1.2 Function Block Diagram

Figure 1-1. Function Block Diagram



2. Pin Functions

Pin Name	I/O	Function	Alternate Pin Function
DTV_BCLK	Input	Clock	AB_AD8, CF_D08, USI5_CLK, GPIO_085
			USI2_CLK, GPIO_109
DTV_PSYNC	Input	Packet synchronization signal	AB_AD9, CF_D09, USI5_DI, GPIO_086
			USI2_DI, GPIO_110
DTV_VALID	Input	Packet data enable	AB_AD10, CF_D10, USI5_DO, GPIO_087
			USI2_DO, GPIO_111
DTV_DATA	Input	Data	AB_AD11, CF_D11, USI5_CS0, GPIO_109
			USI2_CS0, GPIO_112

3. Registers

Do not access reserved registers.
Any value written to reserved bits in each register is ignored.

3.1 Register List

Base address: E115_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Interrupt status register	DT_STATUS	R	0000_0000H
0004H	Interrupt raw status register	DT_RAWSTATUS	R	0000_0000H
0008H	Interrupt enable set register	DT_ENSET	R/W	0000_0000H
000CH	Interrupt enable clear register	DT_ENCLR	W	0000_0000H
0010H	Interrupt source clear register	DT_FFCLR	W	0000_0000H
0014H	Error address register	DT_ERRORADR	R/W	0000_0000H
0018H to 001CH	Reserved	–	–	–
0020H	Transfer control register	DT_DMACNT	R/W	0000_0003H
0024H	Transfer request register	DT_DMAREQ	R/W	0000_0000H
0028H	Transfer request cancellation register	DT_DMASTOP	W	0000_0000H
002CH	Start address register	DT_START	R/W	0000_0000H
0030H	Buffer size register	DT_BUFSIZE	R/W	0000_0000H
0034H	Blank size register	DT_BLANK	R/W	0000_0000H
0038H	Current packet register	DT_CURRENT	R	0000_0000H
003CH	DMA completion interrupt setting register	DT_INTCONT	R/W	0000_0000H
0040H	Module control register	DT_MODULECONT	R/W	0000_0000H
0044H	DTV_PSYNC / DTV_VALID Polarity designation register	DT_SIGNALINVERT	R/W	0000_0000H
0048H	Input pin status monitor register	DT_MONITOR	R	0000_0000H
004CH-FFFCH	Reserved	–	–	–

3.2 Register Details

3.2.1 Interrupt status register

This read-only register (DT_STATUS: E115_0000H) can be used to read the status of the interrupt sources enabled by the interrupt enable set register (DT_ENSET).

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved	DTLP	DTVSP	DTVSYNC	DTVSTOP	DTVOR	DTVDMA	DMAERR

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:7	000_0000H	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTVLP	R	6	0	Indicates the status of the packet length excess. This interrupt is issued when 1 packet exceeded 188byte or 204byte.
DTVSP	R	5	0	Indicates the status of the packet length short. This interrupt is issued when transmission data includes SyncByte and the data transfer volume of the just before packet is 188bytes below or 204bytes below.
DTVSYNC	R	4	0	Indicates the status of the illegal SyncByte. This interrupt is issued when the value of SyncByte is neither 47H nor B8H..
DTVSTOP	R	3	0	Indicates the status of the DMA stop interrupt. This interrupt is issued when DMA stops.
DTVOR	R	2	0	Indicates the status of the packet overrun error interrupt. This interrupt is issued when the internal buffer overruns.
DTVDMA	R	1	0	Indicates the status of the DMA completion interrupt. This interrupt is issued every time the number of packets specified in the DMA completion interrupt setting register (E115_003CH) have been transferred via DMA.
DMAERR	R	0	0	Indicates the status of the transfer error interrupt. This interrupt is issued when an error response is received during internal bus transfer. This interrupt is issued upon a prohibited operation such as writing to the transfer-prohibited area.

3.2.2 Interrupt raw status register

This read-only register (DT_RAWSTATUS: E115_0004H) can be used to read the status of the interrupt sources, regardless of the setting of the interrupt enable set register (DT_ENSET).

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved	DTVLP RAW	DTVSP RAW	DTVSYNC RAW	DTVSTOP RAW	DTVOR RAW	DTVDMA RAW	DMAERR RAW

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:7	000_0000H	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTVLPRAW	R	6	0	Indicates the status of the packet length excess. This interrupt is issued when 1 packet exceeded 188byte or 204byte.
DTVSPRAW	R	5	0	Indicates the status of the packet length short. This interrupt is issued when transmission data includes SyncByte and the data transfer volume of the just before packet is 188bytes below or 204bytes below.
DTVSYNCRAW	R	4	0	Indicates the status of the illegal SyncByte. This interrupt is issued when the value of SyncByte is neither 47H nor B8H.
DTVSTOPRAW	R	3	0	Indicates the status of the DMA stop interrupt. This interrupt is issued when DMA stops.
DTVORRAW	R	2	0	Indicates the status of the packet overrun error interrupt. This interrupt is issued when the internal buffer overruns.
DTVDMARAW	R	1	0	Indicates the status of the DMA completion interrupt. This interrupt is issued every time the number of packets specified in the DMA completion interrupt setting register (E115_003CH) have been transferred via DMA.
DMAERRRAW	R	0	0	Indicates the status of the transfer error interrupt. This interrupt is issued when an error response is received during internal bus transfer. This interrupt is issued upon a prohibited operation such as writing to the transfer-protected area.

3.2.3 Interrupt enable set register

This register (DT_ENSET: E115_0008H) enables issuance of interrupt requests. When the bit corresponding to an interrupt source is set to 1 in this register, if the interrupt source is set, an interrupt request is issued and the corresponding bit of the interrupt status register (DT_STATUS) is set to 1. Writing 0 to this register does not affect the setting. The interrupt request issuance enable status can be checked by reading this register.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved	DTVLP_EN	DTVSP_EN	DTVSYNC_EN	DTVSTOP_EN	DTVOR_EN	DTVDMA_EN	DMAERR_EN

(1/2)

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:7	000_0000H	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTVLP_EN	R	6	0	Indicates whether issuance of packet length excess interrupt request is enabled. 0: Not enabled. 1: Enabled.
	W			Specifies whether to enable issuance of packet length excess interrupt requests. 1: Enable interrupt.
DTVSP_EN	R	5	0	Indicates whether issuance of packet length short interrupt request is enabled. 0: Not enabled. 1: Enabled.
	W			Specifies whether to enable issuance of packet length short interrupt requests. 1: Enable interrupt.
DTVSYNC_EN	R	4	0	Indicates whether issuance of illegal SyncByte interrupt request is enabled. 0: Not enabled. 1: Enabled.
	W			Specifies whether to enable issuance of illegal SyncByte interrupt requests. 1: Enable interrupt.
DTVSTOP_EN	R	3	0	Indicates whether issuance of DMA stop interrupt requests is enabled. 0: Not enabled. 1: Enabled.
	W			Specifies whether to enable issuance of DMA stop interrupt requests. 1: Enable interrupt.

(2/2)

Name	R/W	Bit No.	After Reset	Function
DTVOR_EN	R	2	0	Indicates whether issuance of packet overrun error interrupt requests is enabled. 0: Not enabled. 1: Enabled.
	W			Specifies whether to enable issuance packet overrun error interrupt requests. 1: Enable interrupt.
DTVDMA_EN	R	1	0	Indicates whether issuance of DMA completion interrupt requests is enabled. 0: Not enabled. 1: Enabled.
	W			Specifies whether to enable issuance of DMA completion interrupt requests. 1: Enable interrupt.
DMAERR_EN	R	0	0	Indicates whether issuance of transfer error interrupt requests is enabled. 0: Not enabled. 1: Enabled.
	W			Specifies whether to enable issuance of transfer error interrupt requests. 1: Enable interrupt.

3.2.4 Interrupt enable clear register

This register (DT_ENCLR: E115_000CH) disables issuance of interrupt requests. When the bit corresponding to an interrupt source is set to 1 in this register, an interrupt request is not issued even if an interrupt source occurs. The status of the corresponding bit of the interrupt status register (DT_STATUS) also remains unchanged. Writing 0 to this register does not affect the setting.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved	DTVLP MASK	DTVSP MASK	DTVSYNC MASK	DTVSTOP MASK	DTVOR MASK	DTVDMA MASK	DTVERR MASK

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:7	000_0000H	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTVLPMASK	W	6	0	Disables issuance of packet length excess interrupt requests. 1: Disable
DTVSPMASK	W	5	0	Disables issuance of packet length short interrupt requests. 1: Disable
DTVSYNCMASK	W	4	0	Disables issuance of illegal SyncByte interrupt requests. 1: Disable
DTVSTOPMASK	W	3	0	Disables issuance of DMA stop interrupt requests. 1: Disable
DTVORMASK	W	2	0	Disables issuance of packet overrun error interrupt requests. 1: Disable
DTVDMAMASK	W	1	0	Disables issuance of DMA completion interrupt requests. 1: Disable
DMAERRMASK	W	0	0	Disables issuance of transfer error requests. 1: Disable

3.2.5 Interrupt source clear register

This write-only register (DT_FFCLR: E115_0010H) clears the interrupt source by setting the bit corresponding to the interrupt source to 1. Writing 0 to this register does not affect the setting.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved	DTVLP CLR	DTVSP CLR	DTVSYNC CLR	DTVSTOP CLR	DTVOR CLR	DTVDMA CLR	DMAERR CLR

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:7	000_0000H	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTVLPCLR	W	6	0	Clears the packet length excess interrupt source. 1: Clears the source.
DTVSPCLR	W	5	0	Clears the packet length short interrupt source. 1: Clears the source.
DTVSYNCCLR	W	4	0	Clears the illegal SyncByte interrupt source. 1: Clears the source.
DTVSTOPCLR	W	3	0	Clears the DMA stop interrupt source. 1: Clears the source.
DTVORCLR	W	2	0	Clears the packet overrun error interrupt source. 1: Clears the source.
DTVDMACLR	W	1	0	Clears the DMA completion interrupt source. 1: Clears the source.
DMAERRCLR	W	0	0	Clears the transfer error interrupt source. 1: Clears the source.

3.2.6 Error address register

This register (DT_ERRORADR: E115_0014H) holds the current HADDR status when an internal bus response ERROR, RETRY or SPLIT is received during DMA transfer.

31	30	29	28	27	26	25	24
ERRADR							

23	22	21	20	19	18	17	16
ERRADR							

15	14	13	12	11	10	9	8
ERRADR							

7	6	5	4	3	2	1	0
ERRADR						Reserved	LOCK

Name	R/W	Bit No.	After Reset	Function
ERRADR	R	31:2	0000_0000 H	Stores the HADDR status upon occurrence of an error response.
Reserved	R	1	0	Reserved. Reading returns the unsettled value. Writing in is ignored.
LOCK	R	0	0	Sets error status. 0: Stores the address when an error response occurs. 1: An error response occurred and the address was stored.
	W			Clear error status. 0: Stores the address when an next error response occurs. 1: Nothing action.

Caution If an error response occurs when the LOCK bit is 0, the current HADDR status is stored in the ERRADR bit and the LOCK bit is set to 1.
To acquire the error status again, set the LOCK bit to 0.
Writing 1 to the LOCK bit does not affect the setting.

3.2.7 Transfer control register

This register (DT_DMACNT: E115_0020H) controls data transfer.

Settings can be changed only when DMA transfer is not being performed (DT_DMAREQ register = 0H).

The DTVSP bit must be set to 1.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

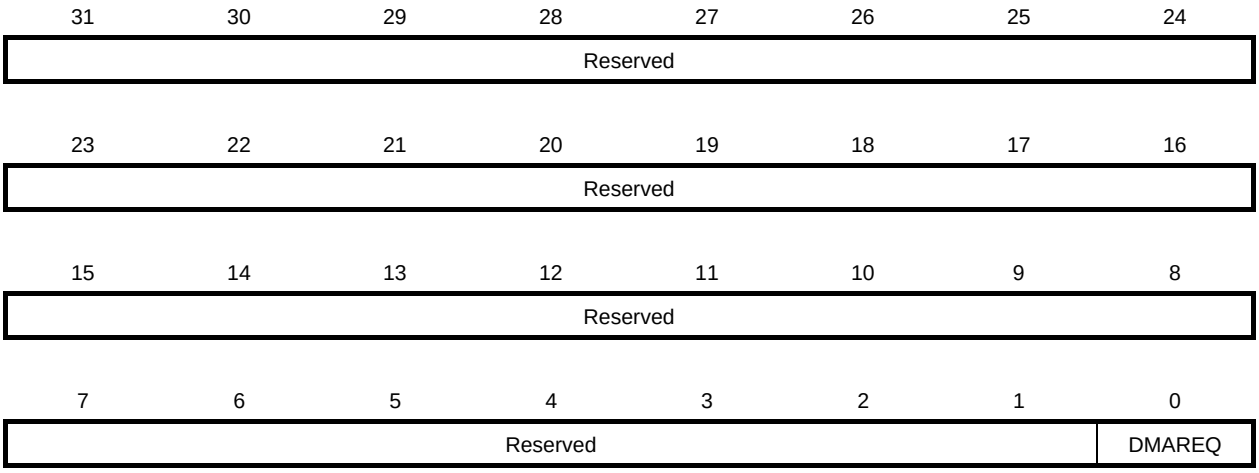
15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved					DTVSP	DTVMODE	DTVENDIAN

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:3	0000_0000H	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTVSP	R/W	2	0	When using, set it as "1".
DTVMODE	R/W	1	1	Specifies the size of a packet. 0: Transfer of synchronization field + data field (188 bytes = 47 words) 1: Transfer of synchronization field + data field + parity field (204 bytes = 51 words)
DTVENDIAN	R/W	0	1	Specifies the DTV stream data format. 0: Big endian 1: Little endian

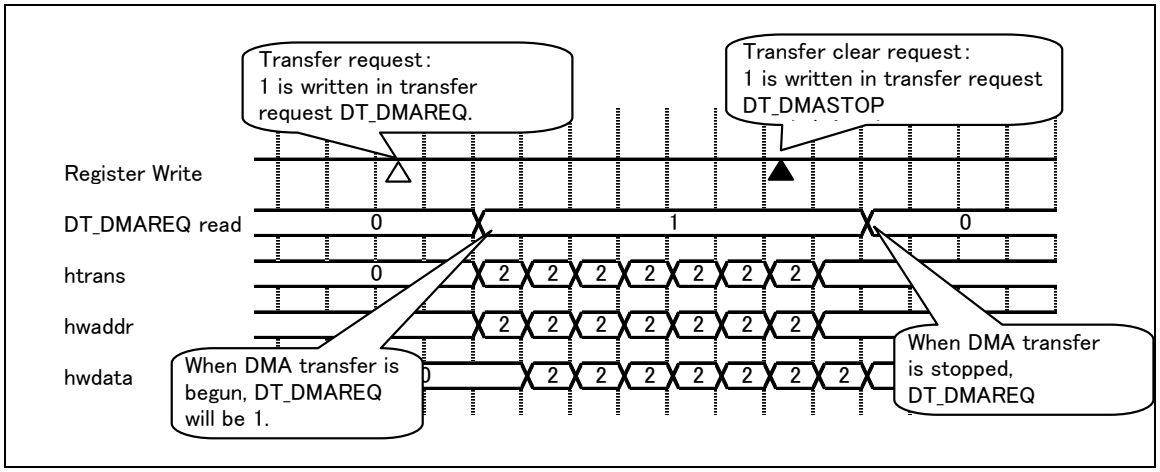
3.2.8 Transfer request register

This register (DT_DMAREQ: E115_0024H) specifies the activation of DMA transfer.
After setting 1 in this register, the read value of this register is 0 until DMA transfer begins. When DMA transfer begins, the read value changes into 1. 1 is set by a transfer release request cashier, and when DMA transfer stops, the read value of this register changes into 0.



Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:1	0000_0000H	Reserved. Reading returns the unsettled value. Writing in is ignored.
DMAREQ	R	0	0	This bit is set to 1 when DMAREQ is acknowledged. This bit is cleared when the transfer request cancellation register (E115_0028H) is set.
	W		–	Writing 1 to this bit issues a DMA transfer request. DMA is repeated until the transfer request cancellation register (E115_0028H) is set. Writing 0 to this bit does not affect the setting.

Figure 3-1. Change of transfer request register value

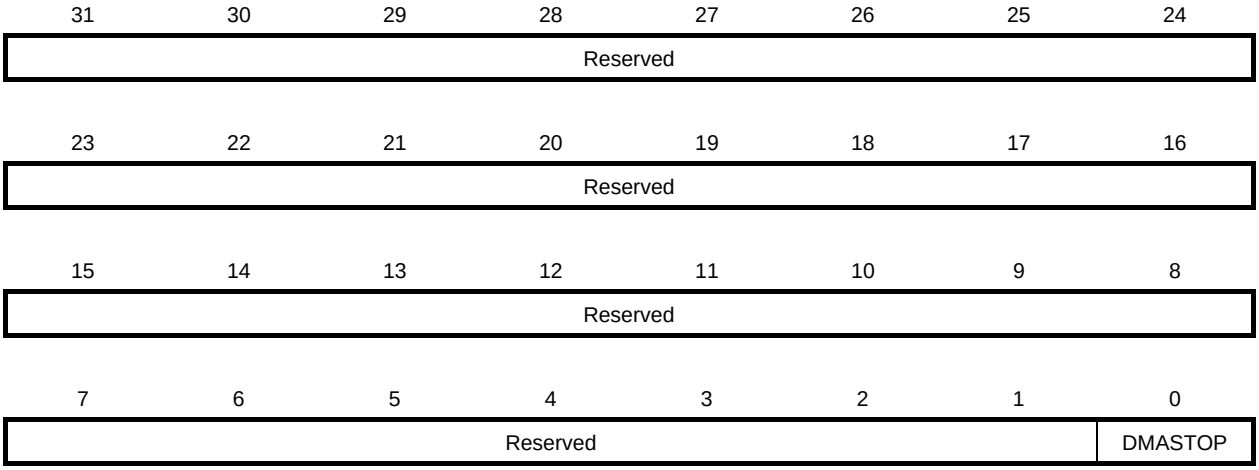


Caution) When requesting DMA transmission, a data transfer is begun from the address which stopped DMA transmission. When doing DMA transmission from the start address, DMA transmission request is done after H/W reset.

3.2.9 Transfer request cancellation register

This register (DT_DMASTOP: E115_0028H) stops DMA transfer. It'll be the stop reservation state by setting this register, and when not forwarding to the occasion during packet transfer after transfer, DMA is stopped immediately . The DMA transfer request status can be checked by reading the transfer request register (DT_DMAREQ). DMA stop interrupt is issued by the time of a fall of status (the read value of the transfer request register).

This is a write-only register. If the register is set to 1, DMA transfer is finished. Writing 0 to this register does not affect the setting.

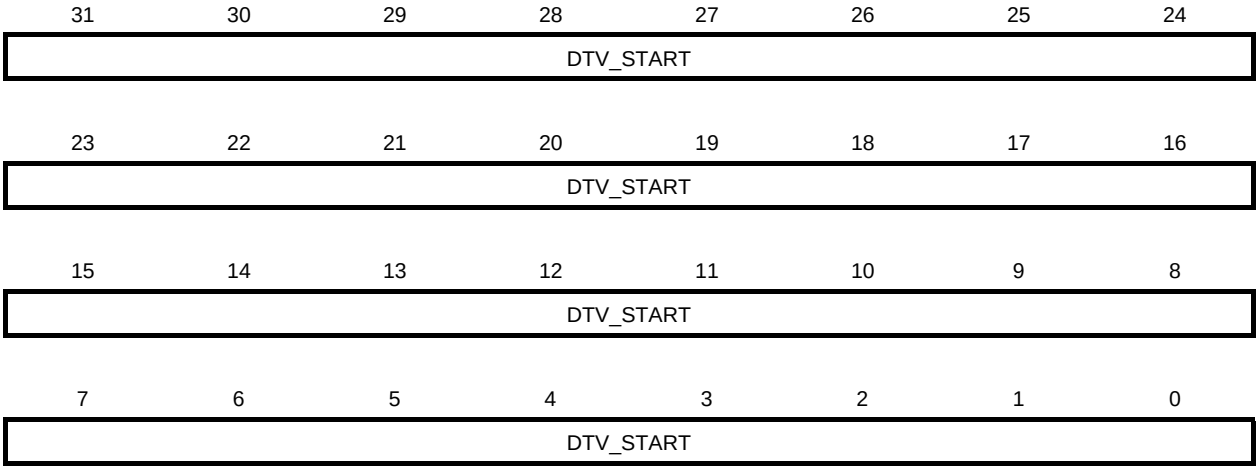


Name	R/W	Bit No.	After Reset	Function
Reserved	W	31:1	0000_0000H	Reserved. Reading returns the unsettled value. Writing in is ignored.
DMASTOP	W	0	0	Stops DMA transfer. 1: Transfer stop When DMA transfer is being performed, the transfer stops after sending the current packet. Otherwise, the transfer immediately stops

Caution) Word data until DMA stop request fixation time is forwarded to a memory. Transfer data was filled in the effective data length of 1 packet (188byte or 204byte), when not having that, even a packet next to the stop request fixation after a while will be unsettled data.

3.2.10 Start address register

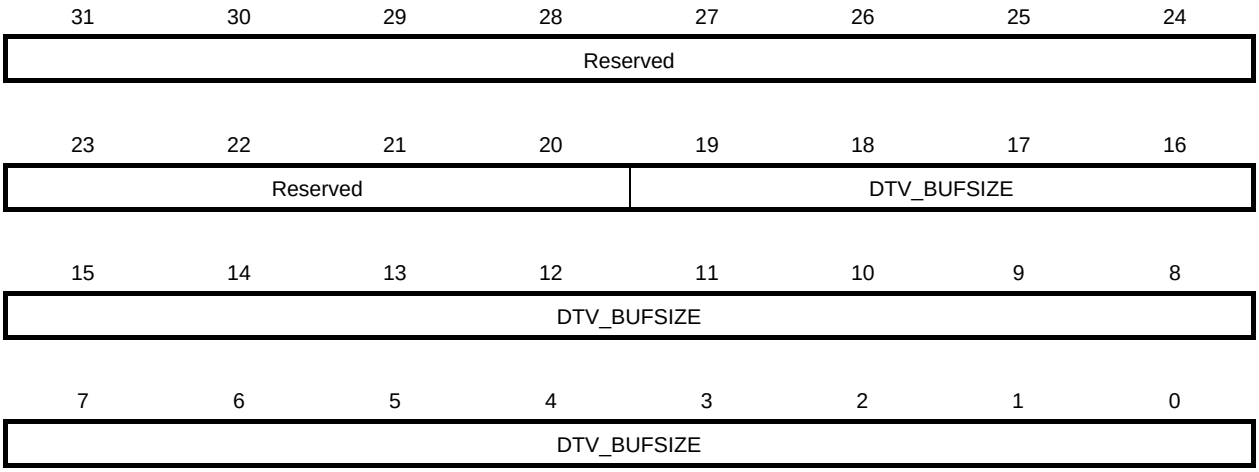
This register (DT_START: E115_002CH) specifies the start address of the DMA transfer destination.
Settings can be changed only when DMA transfer is not being performed (DT_DMAREQ register = 0H).



Name	R/W	Bit No.	After Reset	Function
DTV_START	R/W	31:0	0000_0000H	Specifies the start address of the DMA transfer destination (the lower 2 bits are fixed to 0).

3.2.11 Buffer size register

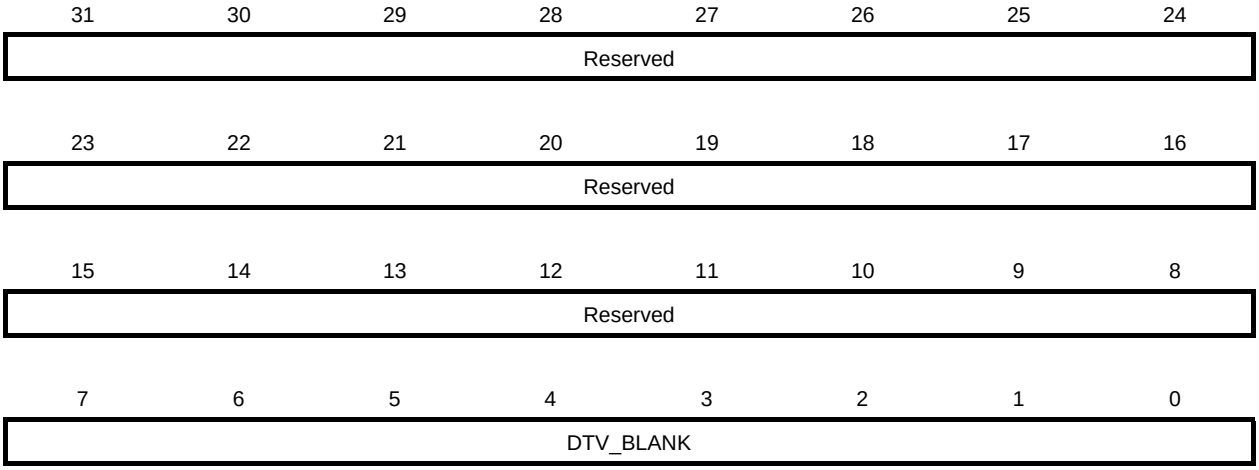
This register (DT_BUFSIZE: E115_0030H) specifies the size of the DMA transfer destination area in units of packets.
Settings can be changed only when DMA transfer is not being performed (DT_DMAREQ register = 0H).



Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:20	000H	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTV_BUFSIZE	R/W	19:0	0_0000H	Specifies the size of the DMA transfer destination area in units of packets (the lower 2 bits are fixed to 0).

3.2.12 Blank size register

This register (DT_BLANK: E115_0034H) specifies the blank size between packets during DMA transfer. Settings can be changed only when DMA transfer is not being performed (DT_DMAREQ register = 0H).



Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:8	00_0000H	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTV_BLANK	R/W	7:0	00H	Specifies the blank size (byte) between packets (the lower 2 bits must be set to 0).

3.2.13 Current packet register

This register (DT_CURRENT: E115_0038H) indicates the number of packets that have been transferred via DMA. This register shows the value from 0 to “DT_BUFSIZE register value – 1”.

31	30	29	28	27	26	25	24
Reserved							

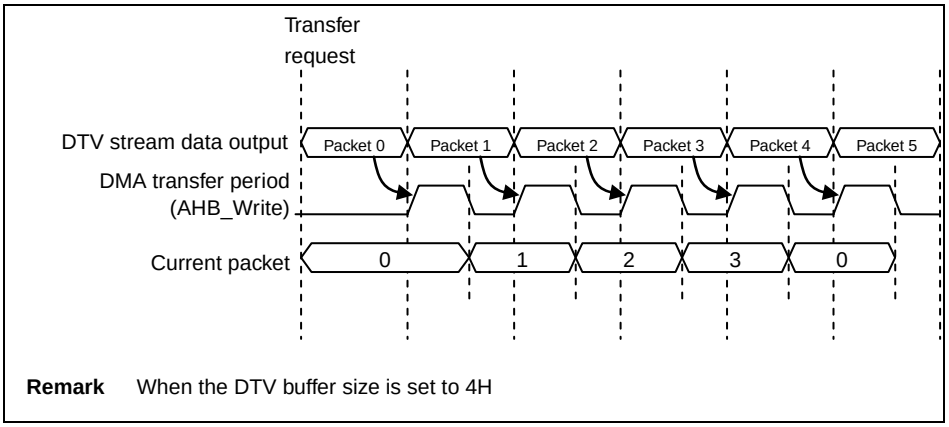
23	22	21	20	19	18	17	16
Reserved				DTV_CURRENT			

15	14	13	12	11	10	9	8
DTV_CURRENT							

7	6	5	4	3	2	1	0
DTV_CURRENT							

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:20	000H	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTV_CURRENT	R	19:0	0_0000H	Stores the number of packets -1, that have been transferred via DMA.

Figure 3-2. Current Packet Register Values



Remark When the DTV buffer size is set to 4H

Caution) The count value is maintained until H/W resets.

3.2.14 DMA completion interrupt setting register

This register (DT_INTCONT: E115_003CH) specifies the interval at which a DMA transfer completion interrupt is issued, in units of packets. A DMA transfer completion interrupt is issued each time DMA transfer of "DT_INTCONT register value + 1" packets is completed.
Settings can be changed only when DMA transfer is not being performed (DT_DMAREQ register = 0H).

31	30	29	28	27	26	25	24
Reserved							

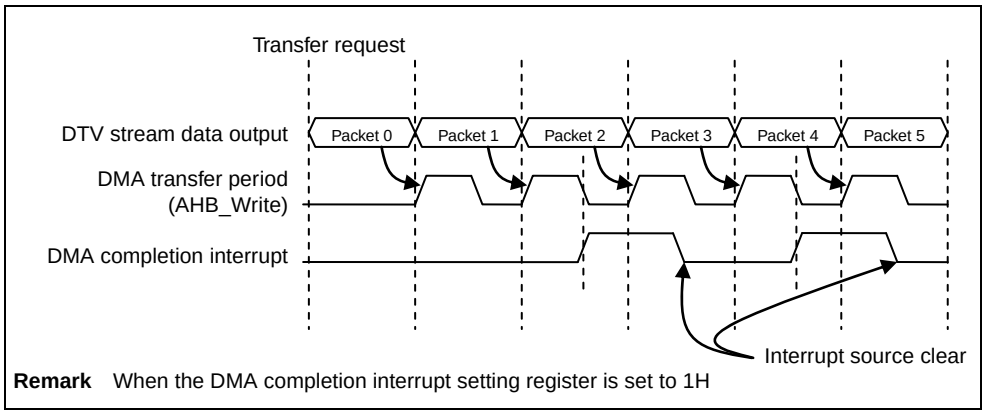
23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
DTV_INTCONT							

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:8	00_0000H	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTV_INTCONT	R/W	7:0	00H	Specifies in units of packets the interval at which a DMA transfer completion interrupt is issued. An interrupt is issued every time the number of packets equal to the set value plus 1 are received.

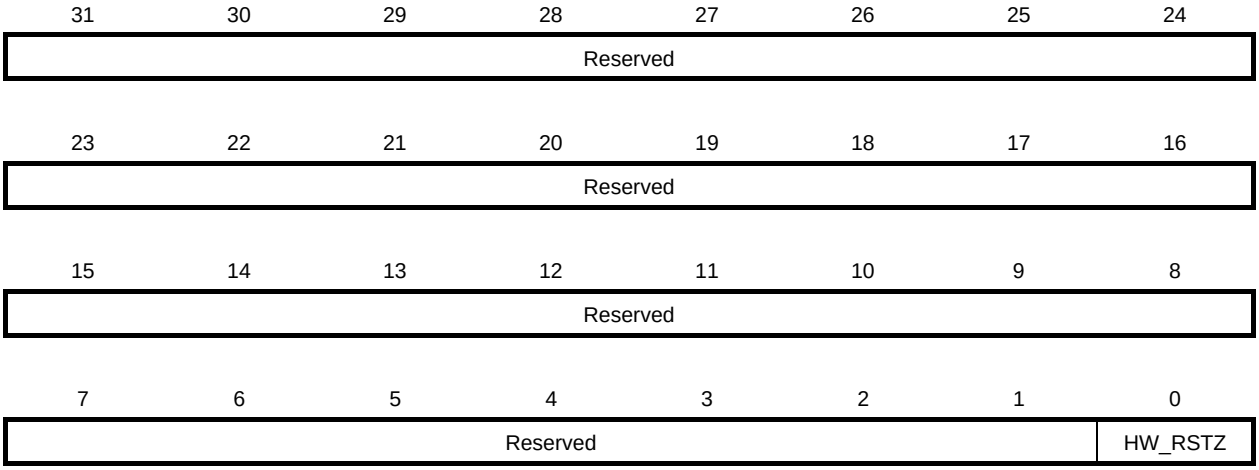
Figure 3-3. DTV Interface DMA Completion Interrupt Set Timing



Remark When the DMA completion interrupt setting register is set to 1H

3.2.15 Module control register

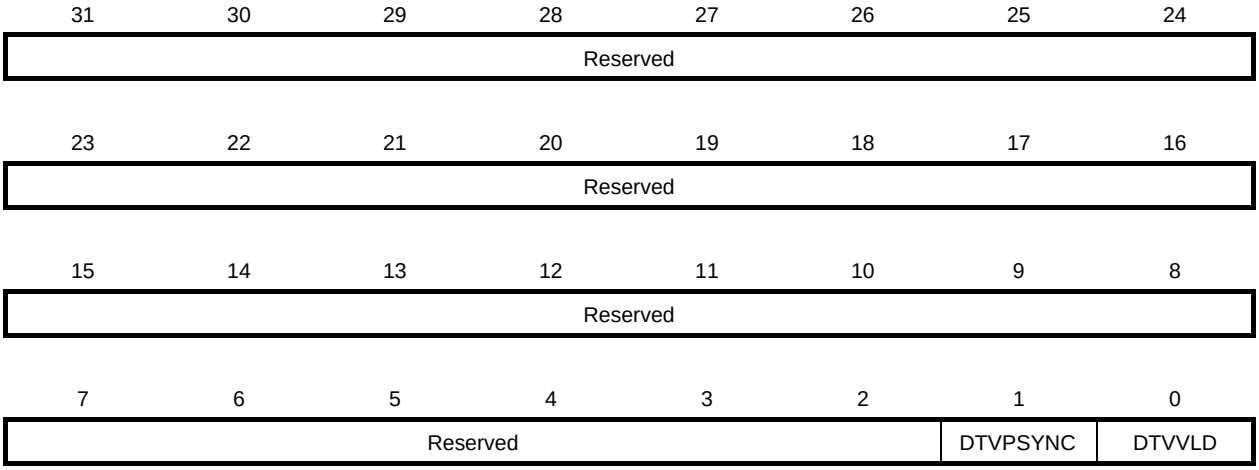
This register (DT_MODULECONT: E115_0040H) initializes the operation of the module that synchronizes with DTV_BCLK.



Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:1	0000_0000H	Reserved. Reading returns the unsettled value. Writing in is ignored.
HW_RSTZ	R/W	0	0	Specifies hardware reset. Specifies whether to initialize the operation of the data capturing circuit that synchronizes with DTV_BCLK. 0: Reset 1: Cancels reset

3.2.16 DTV_PSYNC / DTV_VALID Polarity designation register

This register (DT_SIGNALINVERT: E115_0044H) assign polarity of DTV_PSYNC and DTV_VALID respectively..



Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:2	0000_0000H	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTVPSYNC	R/W	1	0	Polarity of DTV_PSYNC is assigned. 0: not reverse 1: Reverse
DTVVLD	R/W	0	0	Polarity of DTV_VALID is assigned. 0: not reverse 1: Reverse

3.2.17 Input pin status monitor register

This register (DT_MONITOR: E115_0048H) indicates terminal input status of DTV_PSYNC, DTV_VALID, DTV_DATA , and DTV_BCLK.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
DTVDATA	Reserved						

7	6	5	4	3	2	1	0
Reserved					DTVBCLK	DTVPSYNC	DTVVLD

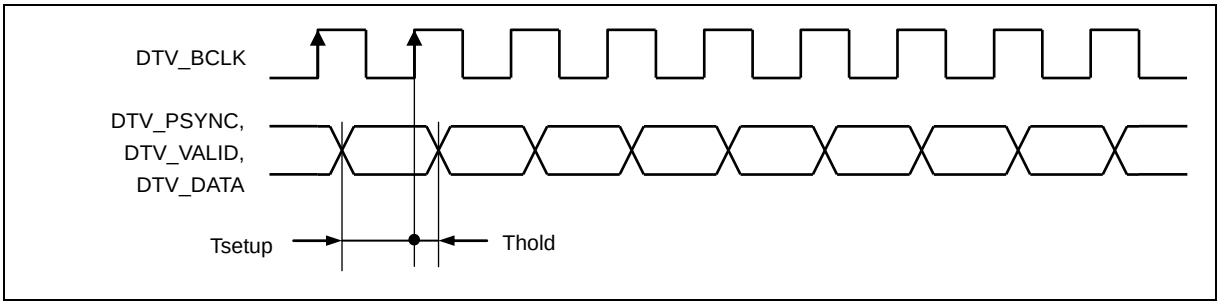
Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:16	0000H	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTVDATA	R	15	0	DTV_DATA is indicated.
Reserved	R	14:3	000H	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTVBCLK	R	2	0	DTV_BCLK is indicated.
DTVPSYNC	R	1	0	DTV_PSYNC is indicated.
DTVVLD	R	0	0	DTV_VALID is indicated.

4. Description of Functions

4.1 Input Signal Timing

4.1.1 DTV interface signal timing

Figure 4-1. DTV Interface Signal Timing



4.1.2 Stream timing

Figure 4-2. Stream Timing (Burst Serial)

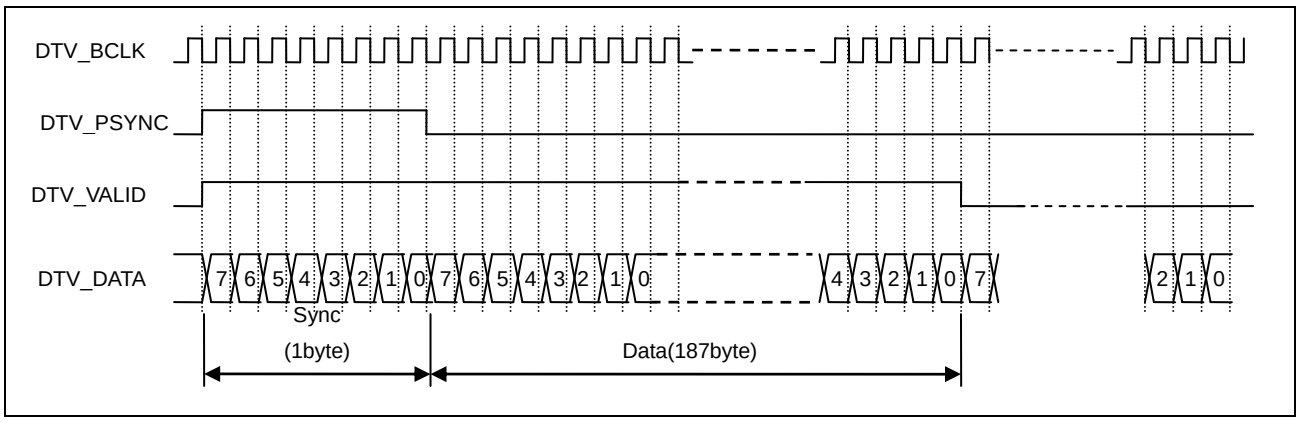
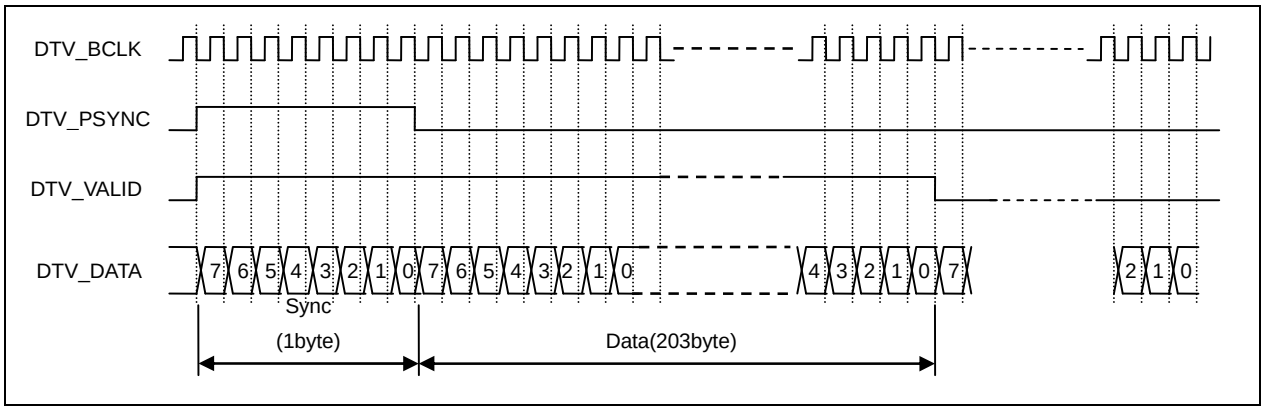


Figure 4-3. Stream Timing (Burst Serial)

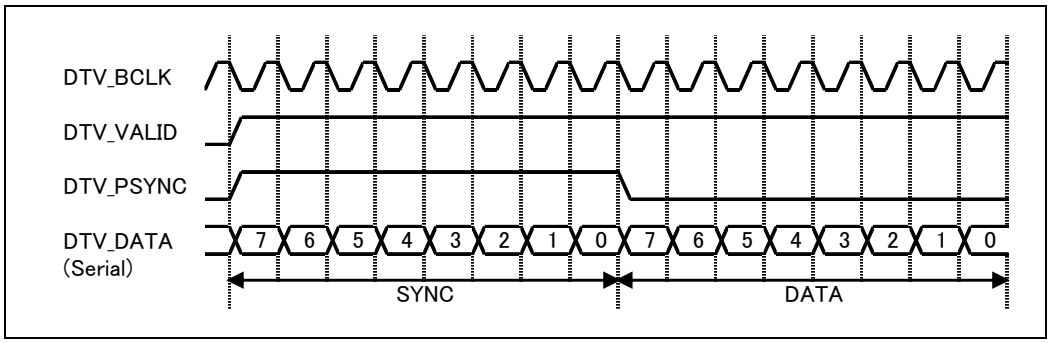


Caution DTVSYNC and DTV_VALID can designate polarity by register setting.

4.1.3 At the timing of a receipt of DTV I/F signal (Burst Serial)

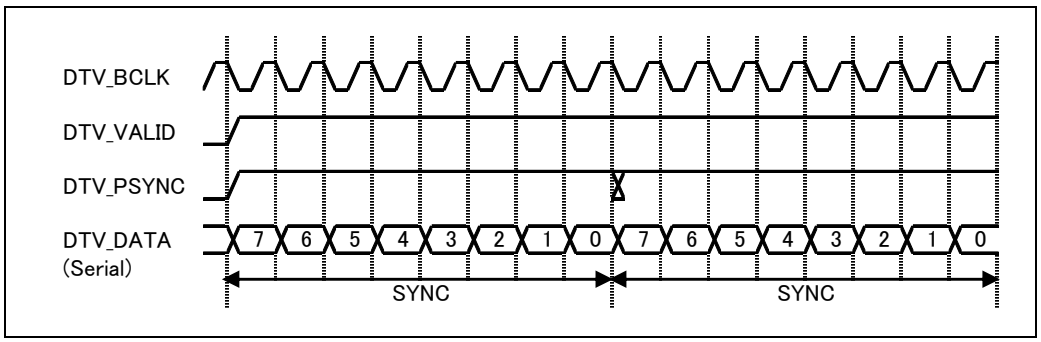
When DTV_VALID=1 and DTV_PSYNC=1 reached for 8 cycles continuously, the 8bits data received at that time is made SYNC. 8 bit data after SYNC is made DATA

Figure 4-4. Judgment of DTV_PSYNC data (Burst Serial)



It's made SYNC continued by the 8bits unit as it indicates on figure 4-5 when DTV_VALID=1 and DTV_PSYNC=1 reached more than 16 cycles continuously.

Figure 4-5. When DTV_PSYNC reaches continuously (Burst Serial)



When it was DTV_VALID==0 during reception, the effective Data bit is made data using 8bits except for DTV_VALID=0 period (figure 4-6). In case of DTV_PSYNC=1, like, it's made SYNC using 8bits except for DTV_VALID=0 period (figure 4-7). But, when changing into DTV_PSYNC=0 during DTV_VALID=0 period, it's made DATA, not SYNC (figure 4-8).

Figure 4-6. When DTV_VALID intermits (Burst Serial)

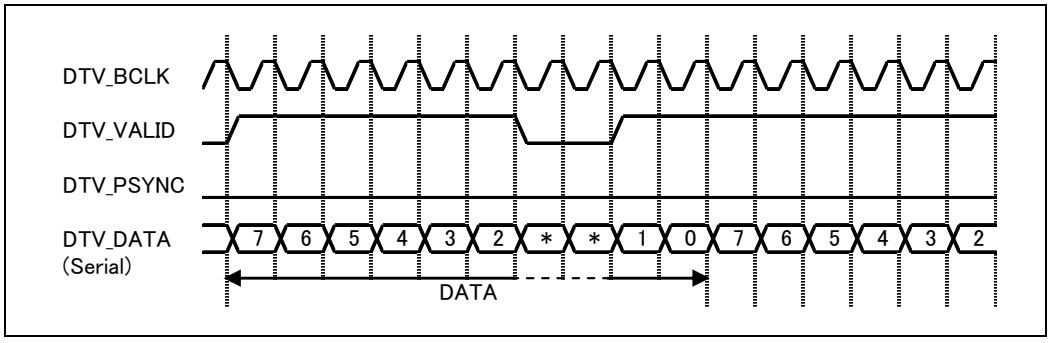


Figure 4-7. When DTV_VALID intermits while DTV_PSYNC is HIGH (Burst Serial)

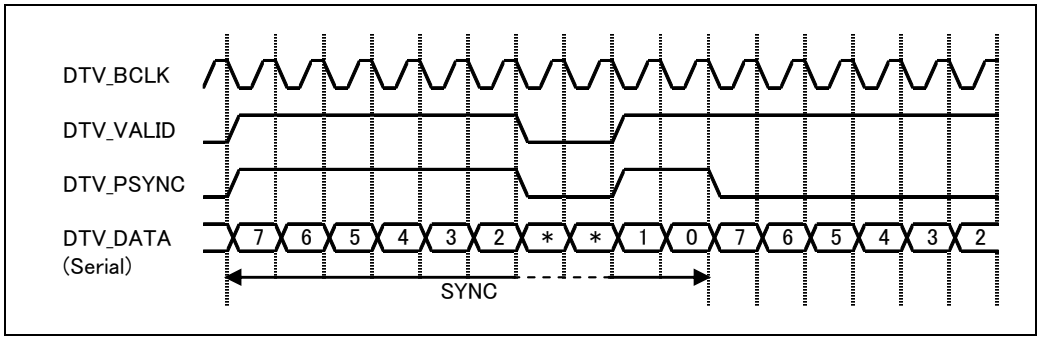
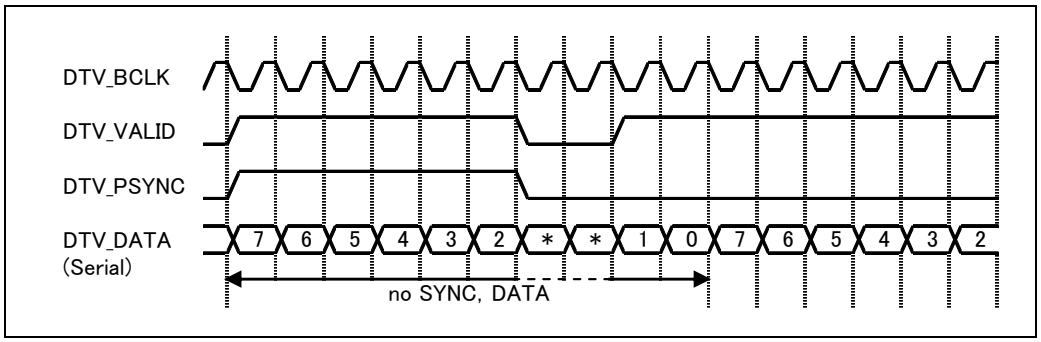


Figure 4-8. When DTV_PSYNC fall during a DTV_VALID intermission period (Burst Serial)



Even DTV_VALID=1 doesn't receive data in the period when DTV_BCLK doesn't enter (figure 4-9, 4-10).

Figure 4-9. When DTV_BCLK intermits (Burst Serial)

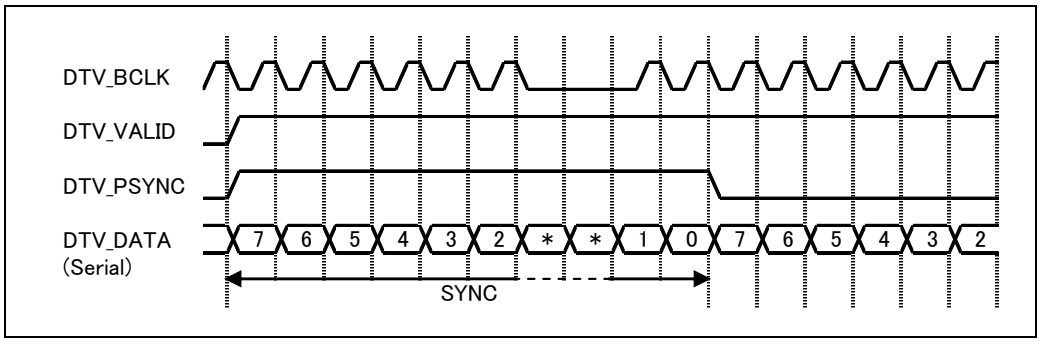
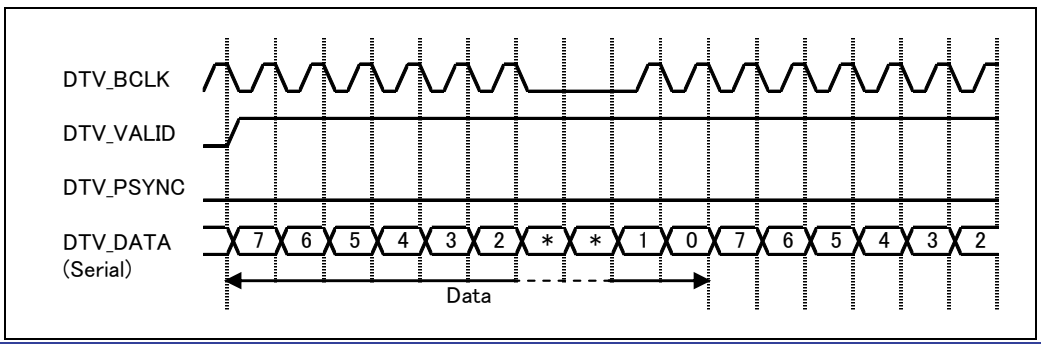


Figure 4-10. When DTV_PSYNC fall during a DTV_BCLK intermission period (Burst Serial)



When the bit line was DTV_PSYNC=1 in the state which isn't enough for 8bits, it's made Data after that 8 bits in even time. When DTV_PSYNC continues it 8 cycles, just after making the rising of DTV_PSYNC a cardinal point, it's made SYNC with 8bits (figure 4-11). When 8 cycles don't have enough DTV_PSYNC=1, it's made effective data just before from the bit line 8bits later (figure 4-12).

Figure 4-11. When I don't have enough bits just before the DTV_PSYNC arrival in 8bits (Burst Serial)

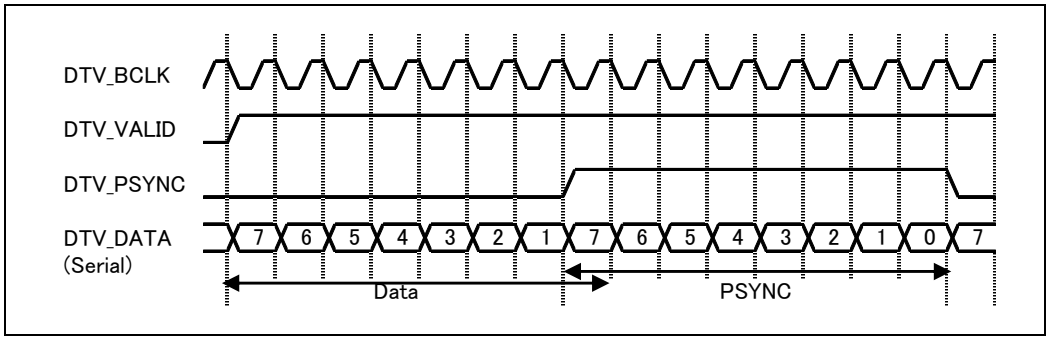
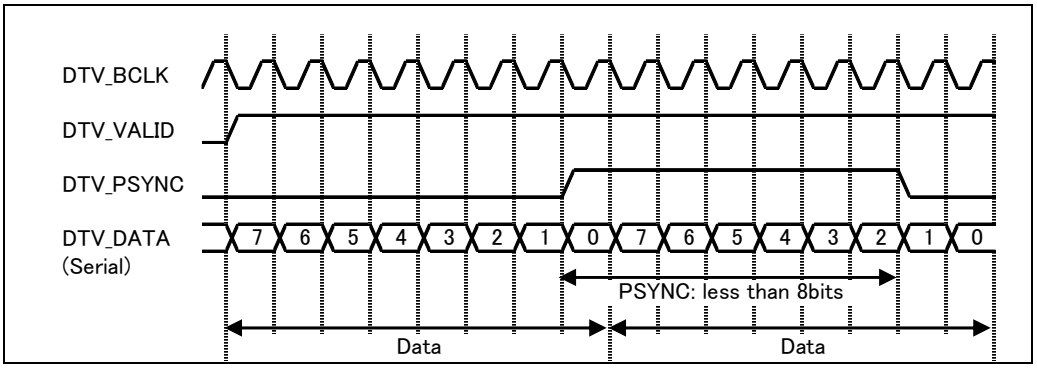


Figure 4-12. When the bit line just before the DTV_PSYNC arrival is 8bits below, and DTV_PSYNC is 8bits below (Burst Serial)



The bit line received just after the start and the reset will be the invalid bit, and it's made the effective bit from first DTV_PSYNC (figure 4-13). When resetting when receiving the effective bit, the data which isn't enough for 8bits received at the end is made invalid data (figure 4-14).

Figure 4-13. Until DTV_PSYNC comes to the data just after the reset, invalid data (Burst Serial)

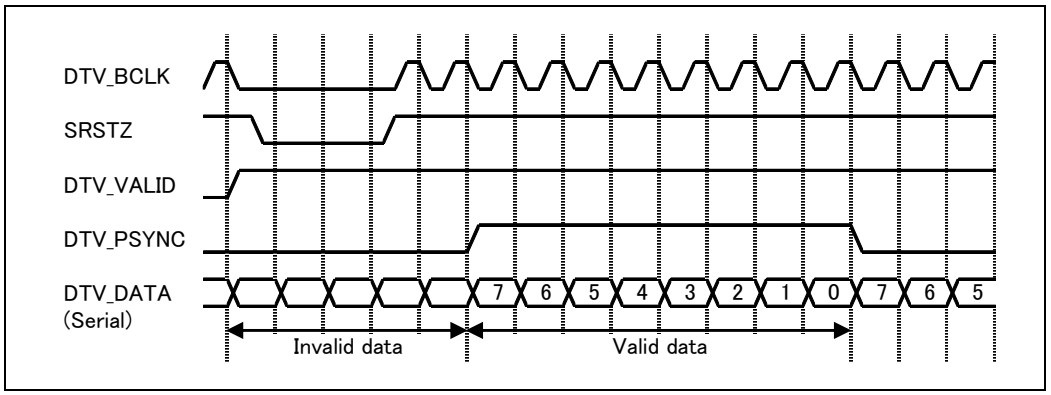
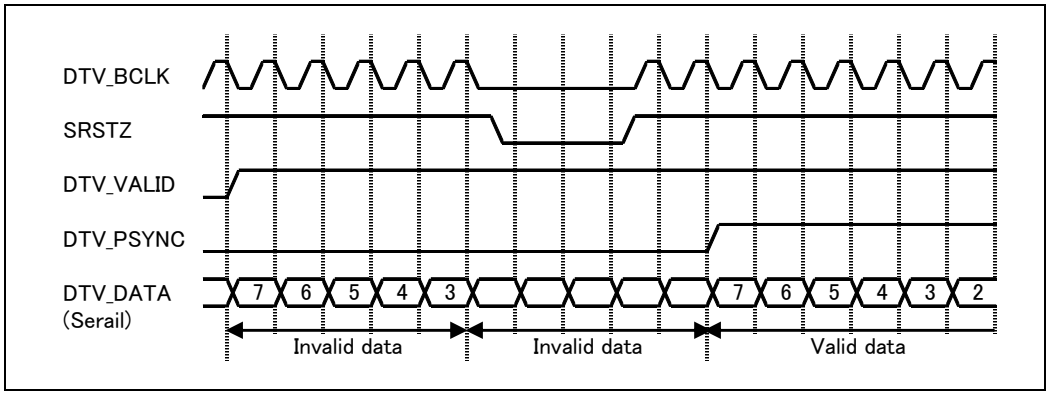


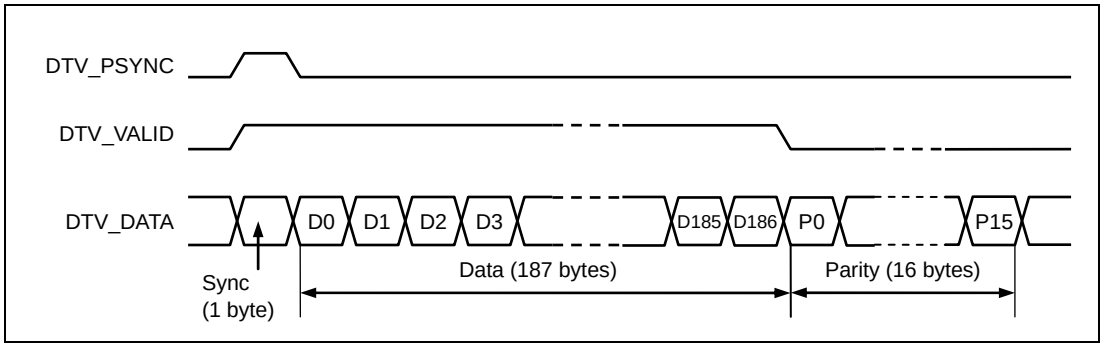
Figure 4-14. It was filled in 8bits just before the reset, the data I don't have is invalid data (Burst Serial)



4.2 Data Format

4.2.1 Stream data storage format

Figure 4-15. Stream Data Storage Format



Data input as shown in Figure 4-15 is stored in the memory in the following format, in accordance with the value set to the DTVENDIAN bit of the transfer control register (DT_DMACNT).

Bit alignment	31 to 24	23 to 16	15 to 8	7 to 0
50 words	P15	P14	P13	P12
49 words	P11	P10	P9	P8
48 words	P7	P6	P5	P4
47 words	P3	P2	P1	P0
46 words	D186	D185	D184	D183
	:	:	:	:
3 words	D14	D13	D12	D11
2 words	D10	D9	D8	D7
1 word	D6	D5	D4	D3
0 words	D2	D1	D0	Sync

Little endian

31 to 24	23 to 16	15 to 8	7 to 0
P14	P15	P12	P13
P10	P11	P8	P9
P6	P7	P4	P5
P2	P3	P0	P1
D185	D186	D183	D184
:	:	:	:
D13	D14	D11	D12
D9	D10	D7	D8
D5	D6	D3	D4
D1	D2	Sync	D0

Big endian

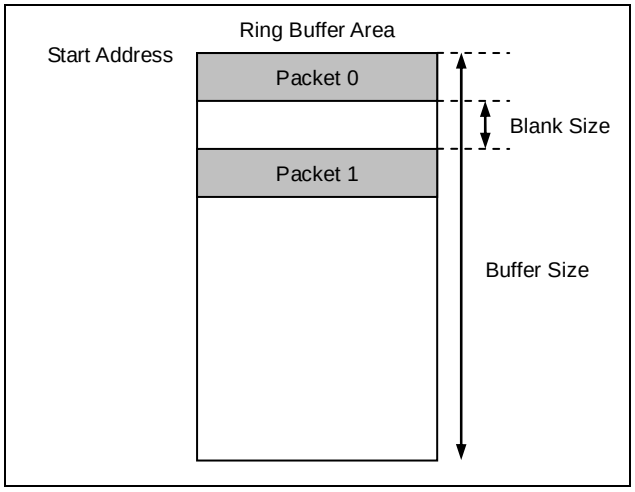
4.3 DTV DMA Transfer Processing

4.3.1 Stream data storage format

Stream data is transferred to the specified buffer area in the memory, in units of packets. The buffer is used as a ring buffer in which the pointer returns to the beginning of the buffer after the specified number of packets are stored.
The following three registers are used to set up the buffer.

- Start address register (32 bits): Specifies the ring buffer start address.
- Buffer size register (20 bits): Specifies the ring buffer area by a packet count.
- Blank size register (8 bits): Specifies the blanking interval between packets.

Figure 4-16. Ring Buffer Mapping



The valid size of a packet can be set to 188 or 204 bytes by using the DTVMODE bit of the transfer control register (DT_DMACNT).
The size of a packet to be mapped to a buffer is the valid size selected by the DTVMODE bit plus the blank size.
The total ring buffer size is the above packet size multiplied by the buffer size register setting.
The DTV flow received from OFDM is the byte unit, and buffering is done by FIFO inside DTV, and every time it gathers 4 bytes, DMA is forwarded to a memory (figure 4-17).
Data is stocked by new address aligning which made SyncByte the head as shown in figure 4-18 at the time of the SyncByte reception time at the time of normal operation and the following exception occurrence.
a) When next SyncByte has come after restoration from a FIFO overflow by a packet overrun.
b) When next SyncByte has come (An excess is repealed.) after the transfer amount of the data exceeded a packet of effective size.
c) When the transfer amount of the data is a packet of effective size sheep rise, and next SyncByte has come (The shortage will be unsettled data.)
d) When it's different from the expectation value (47H or B8H is established by the DTVMODE bit of the DMA control register.) in the value of received SyncByte.

Figure 4-17. Stock method of a packet (at DTVMODE=0)

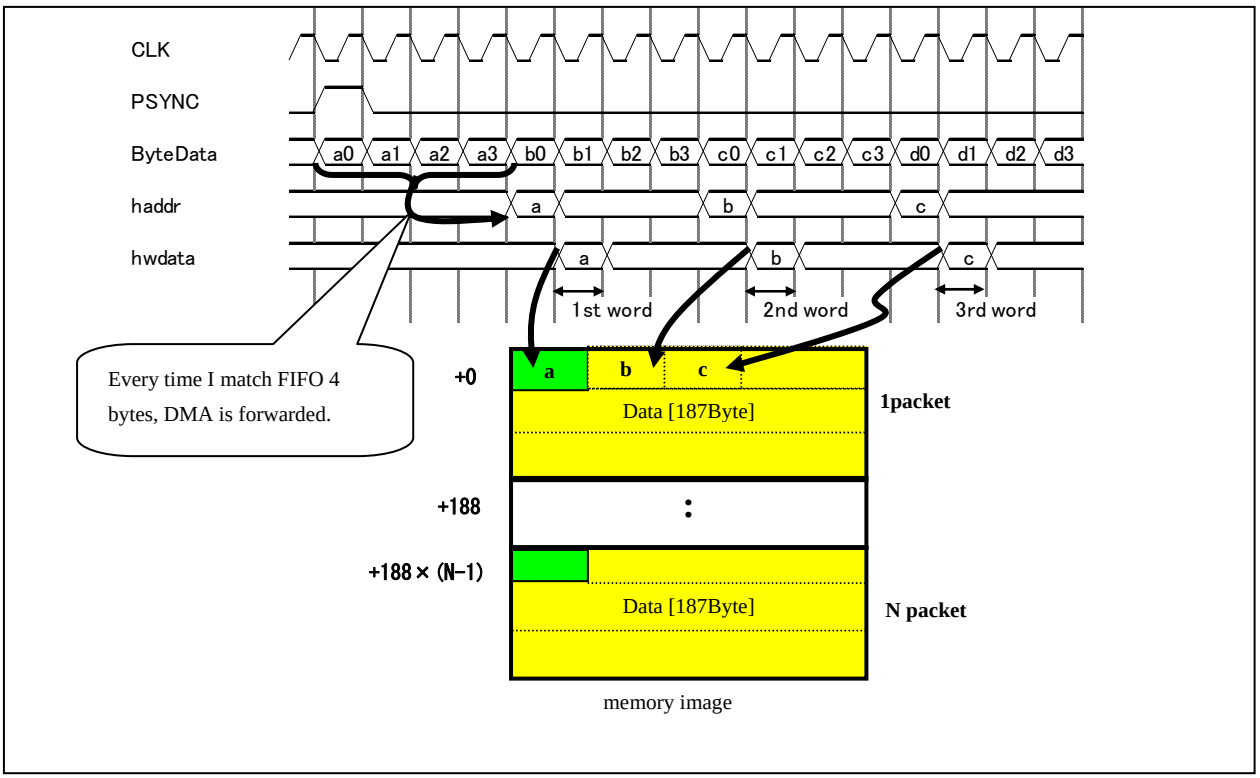
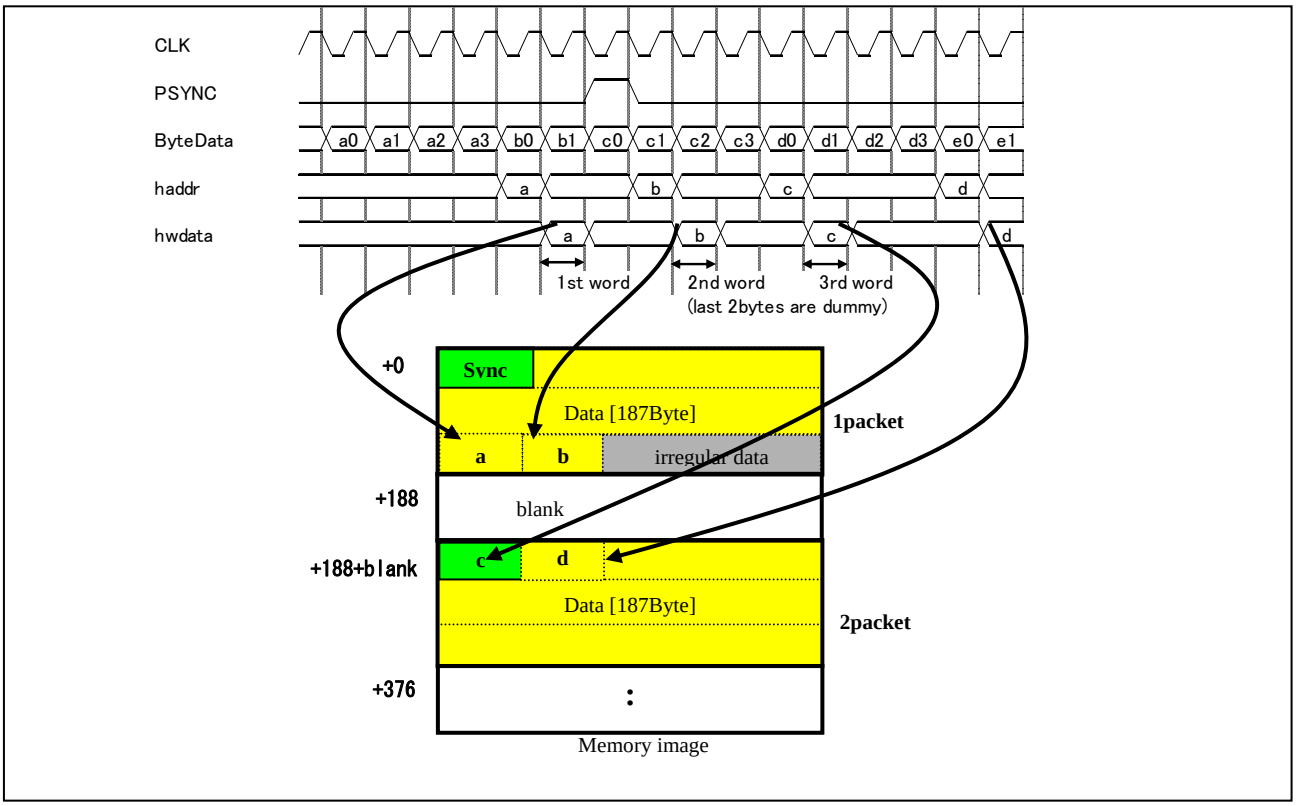


Figure 4-18. Packet stock method when next SyncByte has come, (at DTVMODE=0)



4.4 Interrupt Control

DTV issues 7 kinds of interrupt at the time of Stream reception. Control of each interrupt is assigned to each bit of the interrupt setting register.
Please refer to table 4-1 for details.

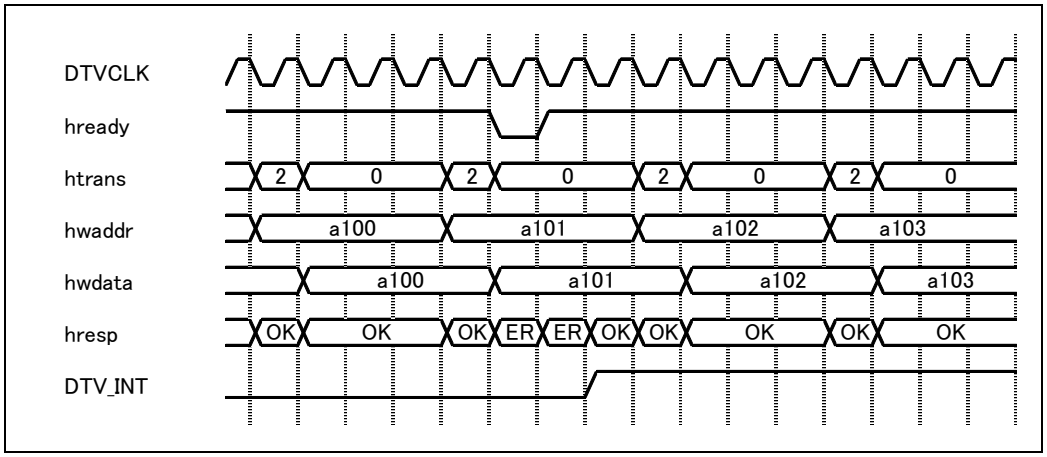
Table 4-1. Interrupt Sources

Interrupt Type	When to Issue	Bit Assignment
Packet length excess interrupt	Issued when 1 packet exceeded 188byte or 204byte.	Bit 6 (DTVLP)
Packet length short interrupt	Issued when DTV_PSYNC=1 and reception data are less than 187 bytes or less than 203 bytes.	Bit 5 (DTVSP)
Illegal SyncByte interrupt	Issued when the price of DTV_PSYNC=1 and SyncByte is 47H or anything but B8H.	Bit 4 (DTVSYNC)
DMA stop interrupt	Issued when the DMA transfer stops.	Bit 3 (DTVSTOP)
Packet overrun	Issued when the internal buffer overruns.	Bit 2 (DTVOR)
DMA completion interrupt	Issued when the specified number of packets have been transferred.	Bit 1 (DTVDMA)
Transfer error interrupt	Issued when the ERROR response is received during internal bus transfer.	Bit 0 (DMAERR)

4.4.1 Transfer error interrupt

When an ERROR reply is received during Internal bus transfer, interrupt is generated.

Figure 4-19. Transfer error interrupt Timing



4.4.2 DMA completion interrupt

Every time DMA of the number of packets set as register DT_INTCONT is completed, interrupt is generated.

4.4.3 Packet overrun interrupt

DTV I/F uses the inner memory (32 bits × 4 words) as a buffer. A bustle of a word does DMA transfer of completed data. When the interior buffer overflows, overrun interrupt is generated. When a packet overrun occurred, the adjustment-lessness occurs to the packet data input from DTV and the range stocked in a ring buffer, but after return, a normal packet bustle is resumed from next Psync from a packet overrun.

4.4.4 DMA Stop Interrupt

When doing DMA transfer of DMA immediately when not forwarding, when DMA transfer stop reservation was formed out of register DT_DMASTOP, when the transfer has been completed, interrupt is generated.

Figure 4-20. At the timing of the interruption when DMA transfer is being done, and transfer has been reserved to cry

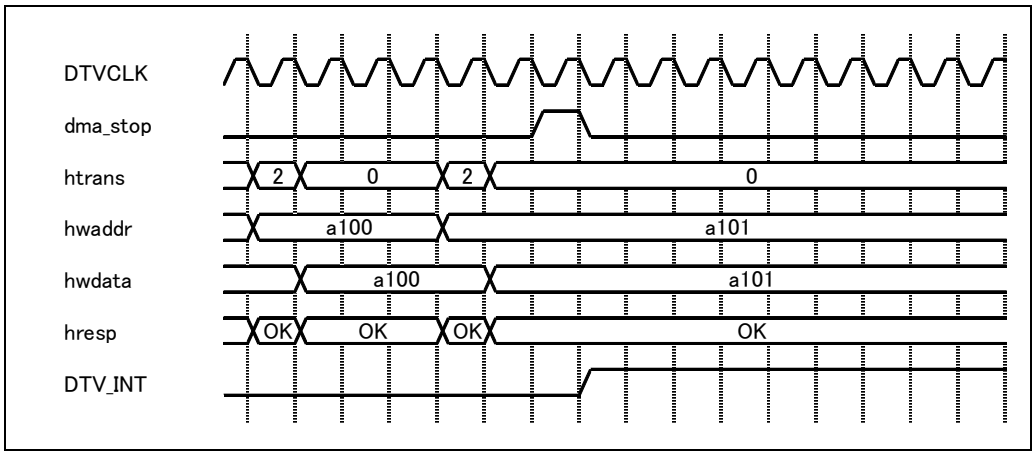
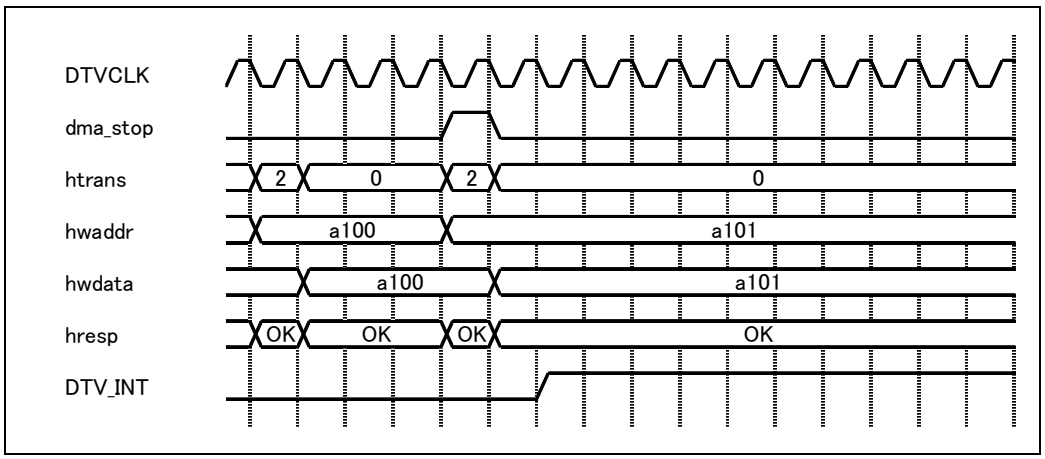


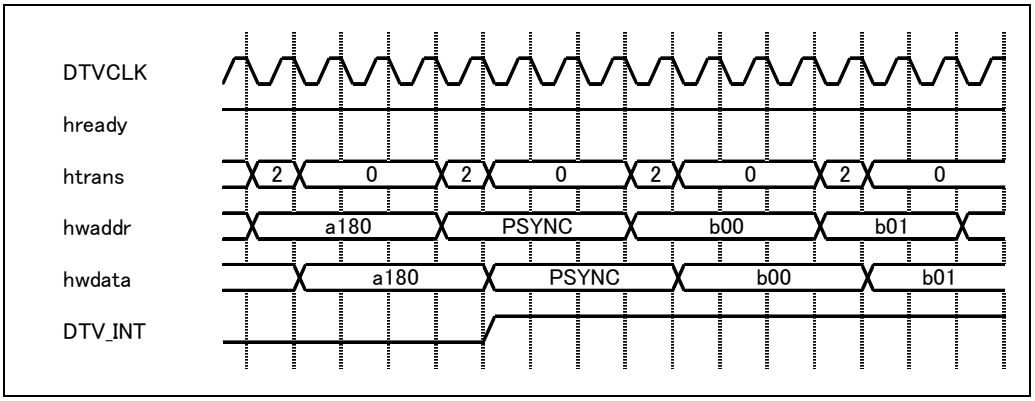
Figure 4-21. At the timing of the interruption when transfer has been reserved during DMA transfer



4.4.5 Packet length short interrupt

When next SyncByte has arrived in less than 203 bytes of state at less than 187 bytes and packet chief effective size 204byte at packet chief effective size 188byte, the forwarded data length generates interrupt. Effective size is established by the DTVMODE bit of the transfer control register.

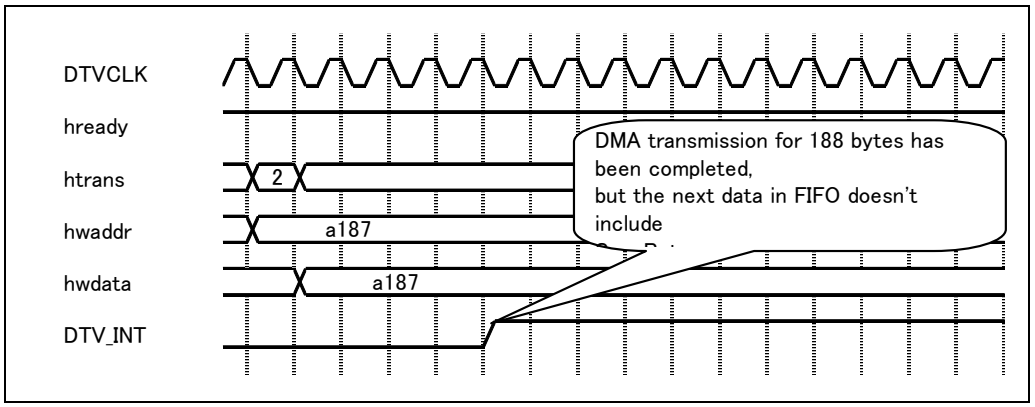
Figure 4-22. Interrupt timing of the word transfer which includes PSYNC byte by less than 187 bytes (at DTVMODE=0)



4.4.6 Packet length excess interrupt

When a packet chief closes beyond effective size (188byte or 204byte), interrupt is generated. Effective size is designated by the DTVMODE bit of the transfer control register.

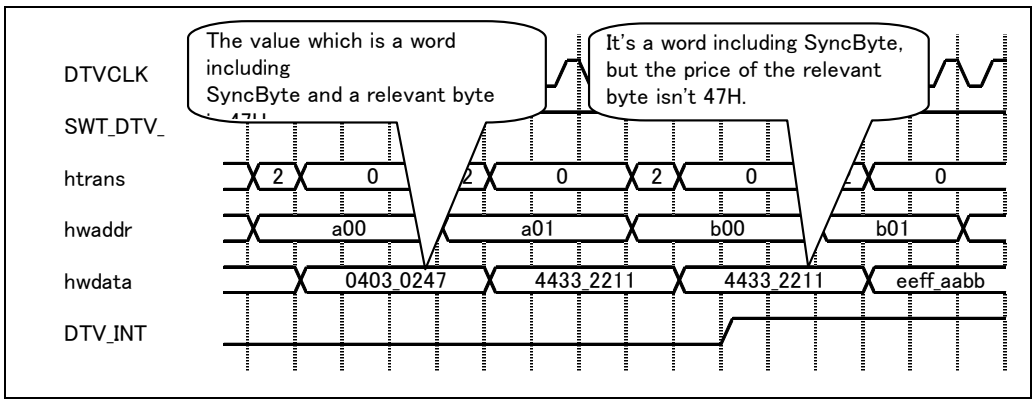
Figure 4-23. Interrupt timing when also not having complete set of word data including SyncByte beyond 188byte, (at DTVMODE=0)



4.4.7 Illegal SyncByte interrupt

SyncByte shows 47H or B8H. The time 47H the price is decided about by DTVMODE of a transfer control register,
and which is DTVMODE=0, the B8H is made the expectation value at DTVMODE=1. In case of all except for the expectation value, SyncByte of DMA transfer word data including SyncByte brings about unjust SyncByte interrupt.

Figure 4-24. Interrupt timing when PSYNC byte is the unjust value, (at DTVMODE=0)



4.5 Clock Control

In EM/EV, supply of the internal bus clock is controlled by each module to save power.
The internal bus clock is supplied upon requests from modules and upon register access.
In the DTV interface, a clock supply request is set when a DMA transfer is requested through register access, and the clock supply request is cleared when transfer of the current DMA is completed with no other transfers requested.

4.5.1 DTV_CLKREQ set timing

When a DTV transmission request register is set and data for DMA transmission exists.

4.5.2 DTV_CLKREQ clear timing

When the DTV transfer request cancellation register is set and DMA transfer of the word unit is completed.

REVISION HISTORY	EMMA Mobile EV2 User's Manual: Digital Terrestrial TV Interface

Rev.	Date	Description	
		Page	Summary
1.00	Jan 29, 2010	—	1st revision release
2.00	Jun 7, 2010	—	Incremental update from comments to the 1.0.
3.00	Sep 30, 2010	—	Incremental update from comments to the 2.0. (A change part from the old revision is "★" marked in the page left end.)
4.00	Apr 15, 2011	—	Incremental update from comments to the 3.0. (A change part from the old revision is "★" marked in the page left end.)
5.00	May 31, 2011	—	Incremental update from comments to the 4.0.
6.00	Sep 30, 2011	—	Incremental update from comments to the 5.0.
7.00	Dec 21, 2011	—	Incremental update from comments to the 6.0.

EMMA Mobile EV2 User's Manual:
Digital Terrestrial TV Interface

Publication Date: Rev.1.00 Jan 29, 2010
Rev.7.00 Dec 21, 2011

Published by: Renesas Electronics Corporation

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 1.0

Digital Terrestrial TV Interface

EMMA Mobile EV2

Renesas Electronics Corporation

R19UH0048EJ0700