Mobile Multimedia Processor Technical Information

Technical Notice Functional Restriction of EMMA Mobile EV(Ver.3)	Doc No.	R19TU0001EJ0300	1/12
	Date	18 Oct. 2011	
	Issued	Renesas Mobile Corporation	

Classification	×	Restriction		Version up		Modificaiton		Other
References	Multimedia Processor for Mobile Applications EMMA Mobile EV2 User's Manuals (see below)							

Document Name	Document No.	Document Name	Document No.
1chip	R19UH0036EJxxxx	LP-DDR/DDR2 Controller	R19UH0039EJxxxx
System Management Unit	R19UH0037EJxxxx	SD Memory Card Interface	R19UH0061EJxxxx
Rotator	R19UH0057EJxxxx	CF Card Interface	R19UH0062EJxxxx
Image Composer	R19UH0038EJxxxx	Unified Serial Interface	R19UH0047EJxxxx

※ Last 4 digit indicates version number.

1. Object Product.

EMMA Mobile EV
Product code: μPD7764xB

This document describes functional restrcion of the product show above.

2. Issue History

A histry of EMMA Mobile EV functional restriction documents issue.

Document number	Date	Notes
R19TU0001EJ0100	31 May 2011	
R19TU0001EJ0200	12 Jul. 2011	Error correction of item No.9.
R19TU0001EJ0300	18 Oct. 2011	Addition of item No.16.

3. Summary of Functional Restiction

List of restrictions

No.	Summary
1	SDC DMA fault
2	Irregular data output at the top of Tx transfer data in USI(PCM).
3	Picture is broken by RGB565 processing in ROT
4	Restriction of automatic clock control on A3D
5	Restriction of automatic clock control in AHB HCLK, AHB CLK, PBL0 CLK, and PBL1_CLK.
6	IMC REFRESH register may not be written in LCD synchronous mode.
7	INTT local timer can not be used.
8	CPU clock synchronous mode can not be used.
9	DMA transfer may be stopped when RDC is read.
10	SDC DMA Write burst transfer can not be used.
11	CFI DMA transfer can not be used.
12	Automatic control function in IMC/IMCW macro can not be used.
13	Invalid data output in USI PCM mode
14	LCD Underrun may be occurred.
15	Rch data may not be outputted in USI PCM mode.
16	Automatic self refresh function can not be used when memory chip are connected to both CS0 and CS1 memory interface.

(It will jump to detail description page when the related summary in the list is clicked.)

4. Detail of Functional Restriction

No.1. SDC DMA fault

■Contents

・Phenomena

(1) Read / write is done on wrong address in SD read / write transfer.

Specificaiton:

SD read transfer address value is set in SDC_RXMEM_ADDR0L/H register. SD write transfer address value is set in TXMEM_ADDR0 register.

Acutal function:

SD write transfer address value may be set in not SDC_TXMEM_ADDR0L/H register, but SDC_RXMEM_ADDR0L/H register. SD read transfer address value may be set in not SDC_RXMEM_ADDR0L/H register, but SDC_TXMEM_ADDR0L/H register.

(2) DMA transfer is stopped when SDC address, from 0xe210_0000 to 0xe210_0200, is accessed in SD write transfer.

・Condition:

Phenomenon (1) occurs in SD read / write using DMA function of AHB master IF.

Phenomenon (2) occurs in write DMA using DMA function of AHB master IF. Read DMA is no problem.

■Workaround

Workaround for phenomenon (1):

Please set the same address value of SDC_TXMEM_ADDR0L/H and SDC_RXMEM_ADDR0L/H before starting transfer.

Workaround for phenomenon (2):

Please detecet DMA transfer end by interrupt or poling of SDC_INT_ORG register.

Please be careful in debug time, DMA transfer may be stopped if ICE SDC module register monitor is ON, in case of ICE program read accessing SDC register ddress from 0xe210_0000 to 0xe210_0200.

（Reference: SD Memory Card Interface User's Manual　R19UH0061EJxxxx）

No.2. Irregular data output at the top of Tx transfer data in USI (PCM).

■Contents

・Pheonmena

Irregular output data, high level, may be outputted at the starting time of Tx transfer in USI (PCM).

・Condition:

In case of executing transfer (PCM_TXRX_EN.TX_EN=”1”） in the following condition.

(1) mode0 + Left adjusting time:

－PCM_FUNC_SEL.MODE_SEL=”000”

－PCM_FUNC_SEL.LR_AJUST=”0”

(2) mode1 + Left adjusting time:

－PCM_FUNC_SEL.MODE_SEL=”001”

－PCM_FUNC_SEL.LR_AJUST=”0”

(3)mode2

－PCM_FUNC_SEL.MODE_SEL=”010”

(4)mode3

－PCM_FUNC_SEL.MODE_SEL=”011”

(5)mode5

－PCM_FUNC_SEL.MODE_SEL=”101”

(6)mode6

－PCM_FUNC_SEL.MODE_SEL=”110”

■Workaround

Please write all ‘0’ (silence) data to PCM_TXQ before and after setting transfer enable (TX_EN=’1’).

1. All ‘0’ is written in PCM_TXQ.
   This all ‘0’ data are discarded as a preparation before enabling transfer. The ‘0’ data does not transfer.

2. Setting transfer enable. (PCM_TXRX_EN.TX_EN= ”1”)

3. All ‘0’ data for 1 frame are written in PCM_TXQ.
   First 1 frame of transfer data are transferred always all ‘0’ data.

4. Starting transfer data.（Starting Transfer DMA / Transfer data are written in PCM_TXQ.）

（Reference: Unified Serial Interface User’s Manual R19UH0047EJxxxx ）

No.3. Picture is broken by RGB565 processing in ROT

■Contents

・Phenomena:

Picture is broken, that holizontal or vertical irregular line is inserted, by RGB565 processing in ROT.

・Condition:

－At Raster Order Mode.

－RGB565（SRCFMT_CH0[2:0] = 0x2） processing is conducted.

■Workaround.

Please do not use Raster mode, or set other than 0x2 to SRCFMT_CH0[2:0] in Raster mode.

（Reference: Rotator User's Manual　R19UH0057EJxxxx ）

No.4. Restriction of automatic clock control on A3D

■Contents

・Phenomena:

There is a possibility to hand up CPU when A3D function is used while actomatioc control of A3D_MEM_CLK and A3D_CORE_CLK is ON.

・Condition:

－Automatic clock control of A3D_MEM_CLK and A3D_CORE_CLK is ON.

■Workarround

Please set following at starting A3D.
AHBCLKCTRL1[16]=0: A3D_MEM_CLK automatic control is OFF.
CLKCTRL[2]=0: A3D_CORE_CLK automatic control is OFF.

（Reference: System Management Unit User's Manual　R19UH0037EJxxxx ）

No.5. Restriction of automatic clock control in AHB_HCLK, AHB_CLK, PBL0_CLK, and PBL1_CLK.

■Contents

・Phenomena:

SIO, M2P, and P2M modules do not work normally when automatic clock control of AHB_HCLK, AHB_CLK, PBL0_CLK, and PBL1_CLK is ON.

・Condition:

－Automatic control of AHB_HCLK is ON.
－Automatic control of AHB_CLK is ON.
－Automatic control of PBL0_CLK is ON and DMA transfer of M2P/P2M.
－Automatic control of PBL1_CLK is ON and DMA transfer of M2P/P2M.

■Workaround

- When usinf SIO and P2M.
  Please do following before starting.
  AHBCLKCTRL0 [31:0] = 0x03373271 (AHBHLP, AHBLP is 0x0 (Automatic control is OFF))

- When using M2P.
  At the starting time, in addition to above setting of using SIO and P2M, please set following after M2P reset release.
  AHBCLKCTRL0 [31:0] = 0x03373271 (AHBHLP, AHBLP ⇒ 0x0 (Automatic control is OFF.))
  BUS1_M2P_CONF [31:0] = 0x00000008

（Reference: System Management Unit User's Manual　R19UH0037EJxxxx
1chip User's Manual　R19UH0036EJxxxx）

No.6. IMC_REFRESH register may not be written in LCD synchronous mode.

■Contents

・Phenomena：

After register setting is completed in LCD sync mode, when 0x1 is set to update reservation register (IMC_REFRESH), register update may not be issued.

・Condition：

－Operation is LCD sync mode.

－When 0x1 is set to IMC_REFRESH register, register update is used.

■Workaround

After write “1” to IMC_REFRESH in LCD sync mode, confirm(read) the value of IMC_REFRESH, and if IMC_REFRESH is still “0”, 0x1 must be set in the Update Reserve Register once again.

（Please refer to Image Composer User’s Manual　R19UH0038EJxxxx ）

No.7. INTT local timer can not be used.

■Contents

・Phenomena：

When you write the Timer Counter Register of INTT local timer twice within 100usec, the tImer stops.

・Condition：

－OneShot operation

■Workaround

Do not use the local timer of INTT.

No.8. CPU clock synchronous mode can not be used.

■Contents

・Phenomena:

CPU synchronous mode can not be used.

■Workaround

Use CPU asynchronous mode at PowerON mode after power-on.

（Please refer to System Management Unit User's Manual R19UH0037EJxxxx）

No.9. DMA transfer may be stopped when RDC is read.

■Contents

・Phenomena:

When SDC is not initialized, DMA transfer may be stopped.

・Condition:

－DMA transfer (Read)

■Workaround

1. Set 0x7 into 0xe2100210 register.
2. Set 0x0 into 0xe2100210register to clear the internal SDC module status.

（Please refer to SD Memory Card Interface User's Manual　R19UH0061EJxxxx ）

No.10. SDC DMA Write burst transfer can not be used.

■Contents

・Phenomena:

SDC DMA Write burst transfer may not be stopped.

・Condition:

－DMA burst transfer (Write)

■Workaround

Use DMA single Writetransfer

－SDC_BUSIF_CTRL[2:1]=0x0

（Please refer to SD Memory Card Interface User's Manual　R19UH0061EJxxxx）

No.11. CFI DMA transfer can not be used.

■Contents

・Phenomena:

When CFI DMA transfer is used, data may be incorrect.

・Condition:

－DMA transfer (both Single and Burst)

－DMA FIFO (DMA exclusive FIFO)is full. (in case of high load, DMA FIFO full is occurred.)

－only PIO mode

■Workaround

Do not use DMA transfer, Use CPU transfer instead.

（Please refer to CF Card Interface User's Manual　R19UH0062EJxxxx）

No.12. Automatic control function in IMC/IMCW macro can not be used.

■Contents

・Phenomena:

Automatic control function in IMC/IMCW macro can not be used.

■Workaround

Used by following settings.
IMC_CONTROL[19:8]=0
IMCW_CONTROL[19:8]=0

（Please refer to ：Image Composer User's Manual　R19UH0038EJxxxx ）

No.13. Invalid data output in USI PCM mode

■Contents

・Phenomena:

In case of PCM transfer stop in USI, invalid data (0x1) is output.

・Condition:

－similar to item No2

■Workaround

1. Write over 128 byte all "0" data into PCM_TXQ register.
2. Stop data writing into PCM_TXQ.
3. Write "1" into PCM_TXRX_DIS.TX_ENCLR register.

（Above procedure "3" is also possible by following procedure.）

※When the time interval between procedure 2 and 3 is long, it may be same as following procedure.

3. 1. Wait for FIFO Under Run detection.
3. 2. Write "1" into PCM_TXRX_DIS.TX_ENCLR register.

（Please refer to ：Unified Serial Interface User's Manual　R19UH0047EJxxxx ）

No.14. LCD Underrun may be occurred.

■Contents

・Phenomena:

When the read data from DRM is slower than LCD output, LCD Underrun is occurred.Once LCD Underrun is occurred, it is necessary to reset the LCDC module to output the correct data to LCD.In this moment LCDC stop the data output and screen becomes black.

・Condition:

In the case of series write by CPU.

■Workaround

To avoid the LCD Underrun, the following register setting must be done.
－MEMC_DEGFUN[10] = 1'b1

Additionally CPU series write can be constrained by write-allocation of L2 cache setting and Bandwidth of CPU write to 1/2~1/3.
For detail of L2 Cache setting, please refer to Cortex-A9 User's Manual.
For detail of CPU Write Band width setting, please refer to BUS1_CPU_CONF register.

（Please refer to ：LP-DDR/DDR2 Controller User's Manual　R19UH0039EJxxxx
1chip User's Manual　R19UH0036EJxxxx）

No.15. Rch data may not be outputted in USI PCM mode.

■Contents

・Phenomena:

I n case of following condition, data is not output to the R channel in USI PCM mode.

・Condition:

Please set below to PCM_CYCLE register.
TX_PD=1
CYC_VAL＝SOB
（In case of Tx/Rx simutenious start, CYC_VAL＝SIB）.

■Workaround

Set TX_PD=0
Or set CYC_VAL＞SOB（CYC_VAL＞SIB）
In case of CYC_VAL＝SOB, Do not use TX_PD=1

（Please refer to ：Unified Serial Interface User's Manual　R19UH0047EJxxxx ）

No.16. Automatic self refresh function can not be used when memory chip are connected to both CS0 and CS1 memory interface.

■Contents

・Phenomena：

When memory chips are connected to both CS0 and CS1 memory interface, auto self refresh may cause the memory controler module hang-up.

・Condition：

1. Memory chips are connected to both CS0 and CS1 memory interface.
2. COUNT_COMMON bit of MEMC_DDR_CONFIG2 register (0xe00a2018) is “1”.
3. CSx_SERF_COUNT bit of MEMC_DDR_CONFIG2 register (0xe00a2018) is “1”
4. EV2 access to both CS0 and CS1 memory chip.

■Workaround

Set “0x1313fdfd” to MEMC_DDR_CONFIGR2 refister (0xe00a2018)
Additionally PMU code modification is needed according to your system.Please access to Renesas for detail.

DRAM power consumption must be increased due to auto self refresh off.Strongly recommend to use only CS0 for DDR connection.

（Please refer to ：LP-DDR/DDR2 Controller User’s Manual　R19UH0039EJxxxx）