User's Manual

Camera Interface

User's Manual

Multimedia Processor for Mobile Applications
EMMA Mobile ™ EV2

Renesas Electronics
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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the EMMA Mobile EV2. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Data Sheet	Hardware overview and electrical characteristics	EMMA Mobile EV2 Datasheet	R19DS0010EJxxxx
User's manual (1chip)	Hardware whole specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description	EMMA Mobile EV2 User's manual 1chip	R19UH0036EJxxxx
User's manual (module)	Hardware each macro specifications and operation description.	EMMA Mobile EV2 User's manual each module	See below

Document Name	Document No.	Document Name	Document No.
1chip	R19UH0036EJxxxx	DMA Controller	R19UH0043EJxxxx
System Management Unit	R19UH0037EJxxxx	LP-DDR/DDR2 Controller	R19UH0039EJxxxx
Timer	R19UH0054EJxxxx	SD Memory Card Interface	R19UH0061EJxxxx
System Timer	R19UH0055EJxxxx	SDIO Interface	R19UH0042EJxxxx
HD Video Decoder	R19UH0056EJxxxx	CF Card Interface	R19UH0062EJxxxx
Rotator	R19UH0057EJxxxx	Unified Serial Interface	R19UH0047EJxxxx
Resizer	R19UH0058EJxxxx	UART interface	R19UH0040EJxxxx
Image Composer	R19UH0038EJxxxx	USB 2.0 Host Controller	R19UH0045EJxxxx
LCD Interface	R19UH0044EJxxxx	USB 2.0 Function Controller	R19UH0034EJxxxx
ITU-R BT.656 Interface	R19UH0059EJxxxx	IIC Interface	R19UH0052EJxxxx
Digital Terrestrial TV Interface	R19UH0048EJxxxx	General Purpose I/O Interface	R19UH0041EJxxxx
Camera Interface (This manual)	R19UH0060EJxxxx	Pulse Width Modulation Interface	R19UH0063EJxxxx

4 digits of end shows the version.

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names

Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.

Examples the PM03 bit in the PM0 register

P3_5 pin, VCC pin

(2) Notation of Numbers

The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.

Examples Binary: 11b or 11

Hexadecimal: EFA0h

Decimal: 1234

3. Register Notation

The symbols and terms used in register diagrams are described below.

x.x.x XXX register

This register (XXXXXXX: xxxx_xxxxh) …..

7	6	5	4	3	2	1	0
Reserved		CHG_P1_LAT	LATCH_P1_SEL	Reserved		CHG_P0_LAT	CHG_P0_LAT_SEL

Name	R/W	Bit No.	After Reset	Description
LATCH_P2_SEL	R/W	8	0	0: Use the P2_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P2_LAT bit to latch data.
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P1_LAT	R/W	5	1	0: Output data as is. 1: Output latched data.
LATCH_P1_SEL	R/W	4	0	0: Use the P1_LAT bit of the P1_POWERSW register in the SMU to latch data. 1: Use the CHG_P1_LAT bit to latch data.
Reserved	R	3:2	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P0_LAT	R/W	1	1	0: Output data as is. 1: Output latched data.
CHG_P0_LAT_SEL	R/W	0	0	0: Use the P0_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P0_LAT bit to latch data.

*1 *3 *2

*1

R/W: Read and Write.

R: Read only.

W: Write only.

-: Nothing is assigned.

*2

Reserved bit.

Reserved bit. Set to specified value.

*3

・ Nothing is assigned.

Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.

・ Do not set to a value.

Operation is not guaranteed when a value is set.

・ Function varies according to the operating mode.

The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Register
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

Abbreviation	Full Form
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
AXI	Advanced Extensible Interface
CAM	Camera interface module
CIF	Common Intermediate Format
DTV	Digital TV
EAV	End of Active Video
FIFO	First In, First Out
fps	Frame Per Second
GPIO	General Purpose I/O
HADDR	Home-Address
ITU-R	International Telecommunication Union Radiocommunications sector
QoS	Quality of Service
SAV	Start of Active Video

Table of Contents

1. Overview

CAM captures YUV422 image data from an external camera module, reduces the image to any size (down to 1/16), and transfers it to an external memory.

1.1 Features

- Camera interface signal
  - Data bus (CAM_YUV[7:0])
  - Vertical synchronization (CAM_VS)
  - Horizontal synchronization (CAM_HS)
  - Pixel clock (CAM_CLKI)
- Synchronization signal encoding
  - Vertical/horizontal synchronization signal sampling
  - Enable signal sampling
  - ITU-R BT.656 encoding
- ITU-R BT.656 input
  - The following three modes are available.
  - Store the first field to buffer A, and the second field to buffer B.
  - Store only the first field to buffer A.
  - Store only the second field to buffer A.
- Data format
  - Input: YUV422
  - Output: Selected from YUV422 or YUV420 format
    (YUV Semi-Planar, YUV Interleave and YUV Planar modes are selectable in YUV422 mode.
    YUV Semi-Planar and YUV Planar modes are selectable in YUV420 mode.)
- Maximum image size
  - 4,088 pixels (horizontal) × 4,092 pixels (vertical)
- Data sampling

  Data can be sampled at the following timing for the pixel clock:
  - Rising edge
  - Falling edge
  - Both edges
- Level adjustment

  The gain and offset of the captured external camera images can be adjusted. Values can be specified separately for Y, U and V.
- Reduction
  - Nearest-neighbor sampling
  - Reduction range of 1 to 1/16 (can be set to any size)

- ○ Frame-skipped transfer
  - No skipping: Every frame is transferred.
  - 1/2 skipping: half frames is transferred.
  - 1/3 skipping: One third frames is transferred.
  - 1/4 skipping: quarter frames is transferred.
- ○ Horizontal and vertical flipping

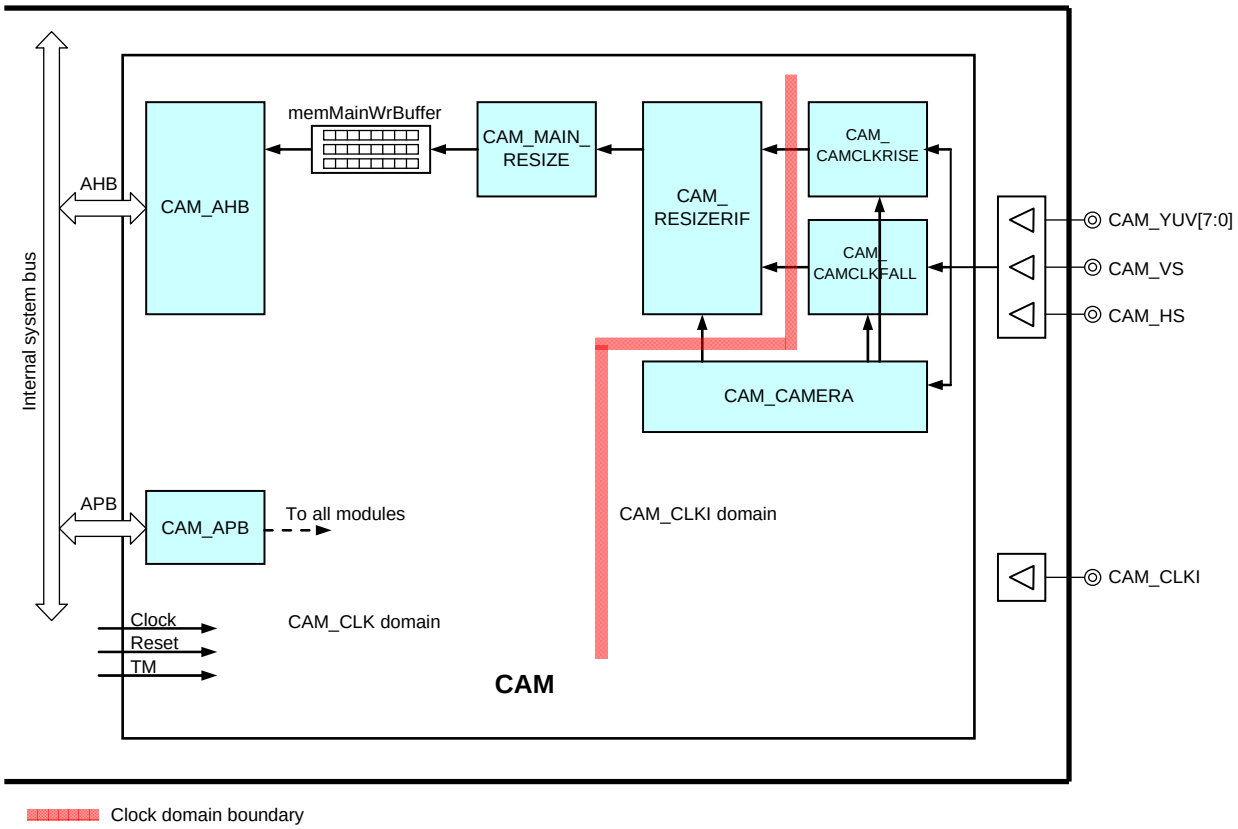
  Data can be individually flipped horizontally and/or vertically and transferred to memory.
- ○ Double buffer transfer

  The transfer destination frame is switched automatically for each transfer frame.
- ○ Buffer memory

  Two 32-bit × 256-word buffer memories
- ○ Simple QoS
  - Controls the priority of the AXI (AHB) bus modules based on the vacant space in the data buffer.
  - The threshold of the vacant space in the data buffer can be specified by using a register.
  - CAM outputs a priority signal to the control side.
- ○ Outputting of amount of valid data in FIFO (data buffer)
  - The amount of valid data in the data buffer is output.
- ○ Safe reset
  - A reset is asserted only when the AHB bus is in the idle state.

1.2 Function Block Diagram

Figure 1-1. Function Block Diagram



2. Pin Functions

Pin Name	I/O	Function	Alternate Pin
CAM_YUV0	Input	Camera YUV data	GPIO_135
CAM_YUV1	Input	Camera YUV data	GPIO_136
CAM_YUV2	Input	Camera YUV data	GPIO_137
CAM_YUV3	Input	Camera YUV data	GPIO_138
CAM_YUV4	Input	Camera YUV data	GPIO_139
CAM_YUV5	Input	Camera YUV data	GPIO_140
CAM_YUV6	Input	Camera YUV data	GPIO_141
CAM_YUV7	Input	Camera YUV data	GPIO_142
CAM_VS	Input	Camera vertical synchronization signal	GPIO_133
CAM_HS	Input	Camera horizontal synchronization signal	GPIO_134
CAM_CLKI	Input	Camera clock	GPIO_132
CAM_CLKO	Output	Camera clock	GPIO_131

3. Registers

3.1 Register List

Do not access reserved registers. An undefined value is returned for a read access.
Do not write any value other than 0 to reserved bits in each register.

Base address: E10B_0000H (1/2)

Address	Register Name	Register Symbol	R/W	Reset
0000H	INT status register	CA_STATUS	R	0000_0000H
0004H	INT raw status register	CA_RAWSTATUS	R	0000_0000H
0008H	INT enable set register	CA_ENSET	R/W	0000_0000H
000CH	INT enable clear register	CA_ENCLR	W	0000_0000H
0010H	INT source clear register	CA_FFCLR	W	0000_0000H
0014H	Error address register	CA_ERRORADR	R/W	0000_0000H
0018H to 001CH	Reserved	–	–	–
0020H	Camera control register	CA_CSR	R/W	0000_0000H
0024H to 002CH	Reserved	–	–	–
0030H	Transfer start X coordinate register	CA_X1R	R/W	0000_0000H
0034H	Transfer end X coordinate register	CA_X2R	R/W	0000_0000H
0038H	Transfer start Y coordinate register	CA_Y1R	R/W	0000_0000H
003CH	Transfer end Y coordinate register	CA_Y2R	R/W	0000_0000H
0040H	Luminance signal offset register	CA_BNZR	R/W	0000_0000H
0044H	Luminance signal gain register	CA_BNGR	R/W	0000_0080H
0048H	U color difference signal offset register	CA_CBZR	R/W	0000_0000H
004CH	U color difference signal gain register	CA_CBGR	R/W	0000_0080H
0050H	V color difference signal offset register	CA_CRZR	R/W	0000_0000H
0054H	V color difference signal gain register	CA_CRGR	R/W	0000_0080H
0058H to 007CH	Reserved	–	–	–
0080H	Transfer control register	CA_DMACNT	R/W	0000_0000H
0084H	Transfer frame register	CA_FRAME	R/W	0000_0005H
0088H	Transfer request register	CA_DMAREQ	R/W	0000_0000H
008CH	Transfer request cancellation register	CA_DMASTOP	W	0000_0000H
0090H to 00FCH	Reserved	–	–	–
0100H	Address addition value register (main frame)	CA_LINESIZE_MAIN	R/W	0000_0000H
0104H	Horizontal reduction ratio register (main frame)	CA_XRATIO_MAIN	R/W	0000_0000H
0108H	Vertical reduction ratio register (main frame)	CA_YRATIO_MAIN	R/W	0000_0000H
010CH	Horizontal transfer size register (main frame)	CA_DMAX_MAIN	R/W	0000_0000H
0110H	Vertical transfer size register (main frame)	CA_DMAY_MAIN	R/W	0000_0000H

(2/2)

Address	Register Name	Register Symbol	R/W	Reset
0114H	Y plane transfer address register (A frame)	CA_YPLANE_A	R/W	0000_0000H
0118H	UV plane transfer address register (A frame)	CA_UVPLANE_A	R/W	0000_0000H
011CH	Y plane transfer address register (B frame)	CA_YPLANE_B	R/W	0000_0000H
0120H	UV plane transfer address register (B frame)	CA_UVPLANE_B	R/W	0000_0000H
0124H to 0228H	Reserved	–	–	–
022CH	Module control register	CA_MODULECONT	R/W	0000_0000H
0230H	Update register	CA_UPDATE	R/W	0000_0000H
0234H	Horizontal/vertical flip control register	CA_MIRROR	R/W	0000_0000H
0238H	Byte lane control register (dedicated to YUV 422 Interleave)	CA_OD_BYTELANE	R/W	0000_00E4H
023CH	Reserved	–	–	–
0240H	Transfer end X coordinate register (dedicated to enable signal sampling mode)	CA_X3R	R/W	0000_0000H
0244H	V plane transfer address register (A frame)	CA_VPLANE_A	R/W	0000_0000H
0248H	V plane transfer address register (B frame)	CA_VPLANE_B	R/W	0000_0000H
024CH to 0250H	Reserved	–	–	–
0254H	Byte lane control register 2 (for video-system macros)	CA_OD_BYTELANE2	R/W	0000_E4E4H
0258H	Simple QoS setting register	CA_QOS	R/W	0000_0000H
025CH to FFFFH	Reserved	–	–	–

3.2 Register Details

3.2.1 Interrupt registers

CAM uses four interrupt sources. Control of interrupts is assigned to each bit of the control register. For details, see **Table 3-1**.

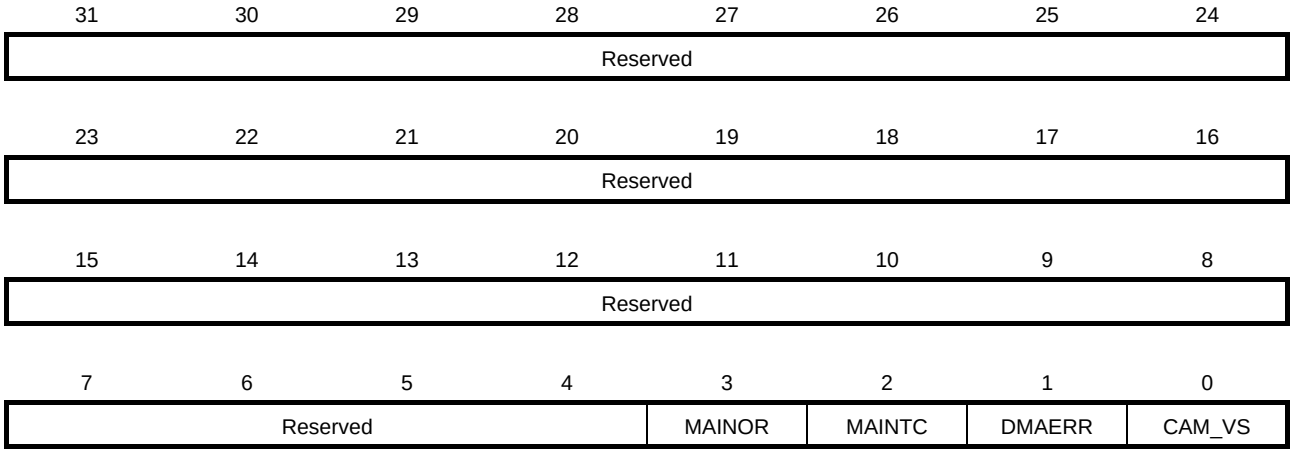
Table 3-1. Interrupt Sources

Interrupt Name	Source	Bit Assignment
Main frame overrun interrupt	This interrupt is issued when the internal buffer overruns during main frame transfer.	3
Main frame transfer completion interrupt	This interrupt is issued upon completion of transfer of one-frame data to the main frame.	2
Transfer error interrupt	This interrupt is issued if an ERROR, RETRY, or SPLIT response is received during an AHB transfer. When a transfer error occurs, the transaction during transfer is lost but the subsequent transfer is continued.	1
Vertical synchronization interrupt	This interrupt is issued at an edge of CAM_VS frame starting (VS_POL setting). If a CAM_VS signal is the positive logic, an interrupt is issued at a rising edge of the CAM_VS. If a CAM_VS signal is the negative logic, an interrupt is issued at a falling edge of the CAM_VS.	0

Remark If an interrupt source is set and cleared at the same time, setting takes precedence.

(1) INT status register

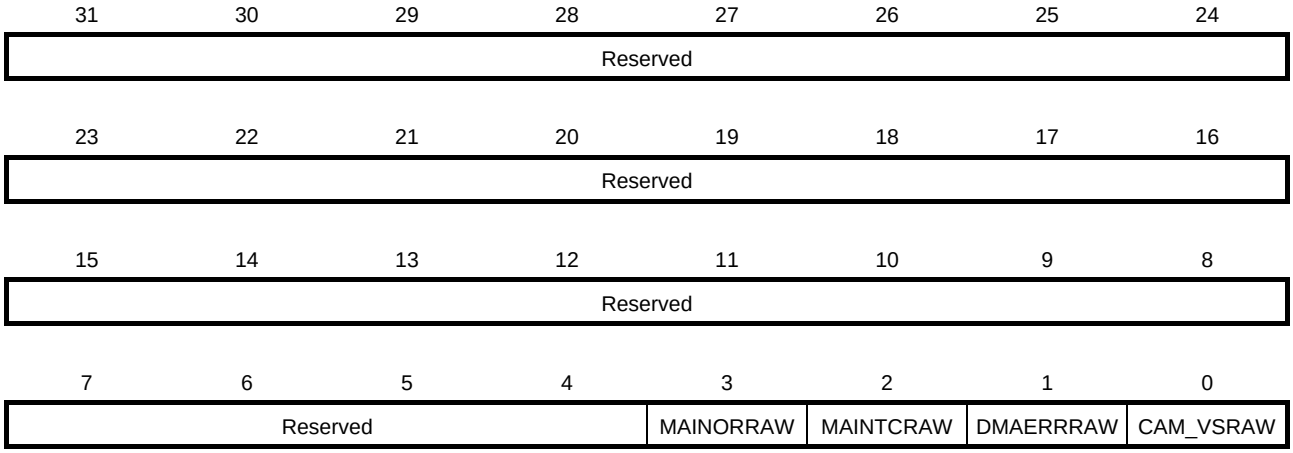
This register (CA_STATUS: E10B_0000H) indicates the status of the interrupt sources unmasked in the CA_ENSET register.



Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:4	000_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
MAINOR	R	3	0	Indicates the status of the main frame overrun interrupt source. 0: No interrupt source 1: Interrupt source has occurred
MAINTC	R	2	0	Indicates the status of the main frame transfer completion interrupt source. 0: No interrupt source 1: Interrupt source has occurred
DMAERR	R	1	0	Indicates the status of the transfer error interrupt source. 0: No interrupt source 1: Interrupt source has occurred
CAM_VS	R	0	0	Indicates the status of the vertical synchronization interrupt source. 0: No interrupt source 1: Interrupt source has occurred

(2) INT raw status register

This register (CA_RAWSTATUS: E10B_0004H) indicates the status of the interrupt sources, regardless of the CA_ENSET register settings.



Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:4	000_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
MAINORRAW	R	3	0	Indicates the raw status of the main frame overrun interrupt source. 0: No interrupt source 1: Interrupt source has occurred
MAINTCRAW	R	2	0	Indicates the raw status of the main frame transfer completion interrupt source. 0: No interrupt source 1: Interrupt source has occurred
DMAERRRAW	R	1	0	Indicates the raw status of the transfer error interrupt source. 0: No interrupt source 1: Interrupt source has occurred
CAM_VSRAW	R	0	0	Indicates the raw status of the vertical synchronization interrupt source. 0: No interrupt source 1: Interrupt source has occurred

(3) INT enable set register

This register (CA_ENSET: E10B_0008H) cancels masking of interrupts.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				MAINOR_EN	MAINTC_EN	DMAERR_EN	CAM_VS_EN

(1/2)

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:4	000_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
MAINOR_EN	R	3	0	Indicates whether issuance of main frame overrun interrupt requests is enabled. 0: Not enabled (Masked) 1: Enabled (Unmasked)
	W	3	0	Enables issuance of main frame overrun interrupt requests. 0: Ignored 1: Cancels interrupt masking.
MAINTC_EN	R	2	0	Indicates whether issuance of main frame transfer completion interrupt requests is enabled. 0: Not enabled (Masked) 1: Enabled (Unmasked)
	W	2	0	Enables issuance of main frame transfer completion interrupt requests. 0: Ignored 1: Cancels interrupt masking.
DMAERR_EN	R	1	0	Indicates whether issuance of DMA transfer error interrupt requests is enabled. 0: Not enabled (Masked) 1: Enabled (Unmasked)
	W	1	0	Enables issuance of DMA transfer error interrupt requests. 0: Ignored 1: Cancels interrupt masking.

(2/2)

Name	R/W	Bit No.	After Reset	Function
CAM_VS_EN	R	0	0	Indicates whether issuance of vertical synchronization interrupt requests is enabled. 0: Not enabled (Masked) 1: Enabled (Unmasked)
	W	0	0	Enables issuance of vertical synchronization interrupt requests. 0: Ignored 1: Cancels interrupt masking.

Caution When setting the CAM_VS_EN bit, wait for at least 16 CAM_CLKI cycles after the reset state of the CAM_CLKI domain is released.

(4) INT enable clear register

This register (CA_ENCLR: E10B_000CH) masks issuance of interrupt requests.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				MAINORMASK	MAINTCMASK	DMAERRMASK	CAM_VSMASK

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:4	000_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
MAINORMASK	W	3	0	Disables issuance of main frame overrun interrupt requests. 0: Ignored 1: Masks the interrupt.
MAINTCMASK	W	2	0	Disables issuance of main frame transfer completion interrupt requests. 0: Ignored 1: Masks the interrupt.
DMAERRMASK	W	1	0	Disables issuance of transfer error interrupt requests. 0: Ignored 1: Masks the interrupt.
CAM_VSMASK	W	0	0	Disables issuance of vertical synchronization interrupt requests. 0: Ignored 1: Masks the interrupt.

(5) INT source clear register

This register (CA_FFCLR: E10B_0010H) clears interrupt sources. The bit is cleared after the corresponding source is cleared.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

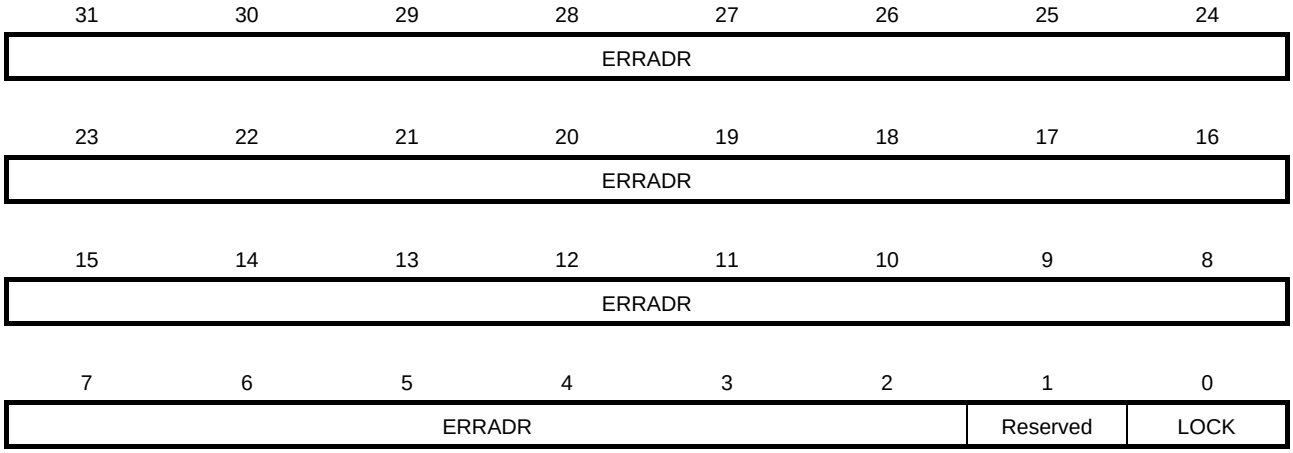
15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				MAINORCLR	MAINTCCLR	DMAERRCLR	CAM_VSCLR

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:4	000_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
MAINORCLR	W	3	0	Clears the main frame overrun interrupt source. 0: Ignored 1: Clears the interrupt source.
MAINTCCLR	W	2	0	Clears the main frame transfer completion interrupt source. 0: Ignored 1: Clears the interrupt source.
DMAERRCLR	W	1	0	Clears the transfer error interrupt source. 0: Ignored 1: Clears the interrupt source.
CAM_VSCLR	W	0	0	Clears the vertical synchronization interrupt source. 0: Ignored 1: Clears the interrupt source.

(6) Error address register

This register (CA_ERRORADR: E10B_0014H) retains the current HADDR status when an AHB bus response ERROR, RETRY, or SPLIT is received during DMA transfer.



Name	R/W	Bit No.	After Reset	Function
ERRADR	R	31:2	0000_0000H	Stores HADDR upon occurrence of a response other than OKAY.
Reserved	R	1	0	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
LOCK	R/W	0	0	Error status 0: Waiting to store the address where an error response occurred. 1: An error response occurred and the address was stored.

Caution If an error response occurs when the LOCK bit is 0, the current HADDR status is stored in the ERRADR bit and the LOCK bit is set to 1. To acquire the error status again, set the LOCK bit to 0. Writing 1 to the LOCK bit does not affect the setting.

3.2.2 Control registers

(1) Camera control register

This 16-bit register (CA_CSR: E10B_0020H) controls the CAM module. To specify the CAM_VS/CAM_HS signal sampling mode, set the SYNCTYPE and SYNCMODE bits to 0H.
Change the values only when DMA transfer is not being performed (transfer request register = 0H).

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
656MODE		PIXEL_YUV	SYNCTYPE	PIXELMODE	DATA_OD	DATA_ID	LD_TMG

7	6	5	4	3	2	1	0
VS_DET	HS_DET	LIMITSEL	SYNCMODE	CLK_EDGE	DATA_DET	VS_POL	HS_POL

(1/3)

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:16	0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
656MODE	R/W	15:14	0H	Specifies the field to be stored in the ITU-R BT.656 mode. (These bits are valid only when the ITU-R BT.656 mode is set by using the SYNCMODE bit.) 00: Stores both the first and second fields to a buffer, starting with the first field. 01: Stores both the first and second fields to a buffer, starting with the second field. 10: Stores only the first field to a buffer. 11: Stores only the second field to a buffer.
PIXEL_YUV	R/W	13	0	Specifies the format of the data to be transferred to memory. 0: Depends on the PIXELMODE bit setting. 1: YUV420/YUV422 Planar mode (Ignores the PIXELMODE bit setting.)
SYNCTYPE	R/W	12	0	Specifies the data sampling mode. (This bit is valid only when the CAM_VS/CAM_HS signal sampling mode is set by using the SYNCMODE bit.) 0: CAM_VS/CAM_HS signal sampling mode 1: Enable signal sampling mode

(2/3)

Name	R/W	Bit No.	After Reset	Function
PIXELMODE	R/W	11	0	Specifies the format of the data to be transferred to memory. (This bit is valid only when the CAM_VS/CAM_HS signal sampling mode is set by using the SYNCMODE bit.) 0: YUV 420/422 Semi-Planar mode 1: YUV422 Interleave mode
DATA_OD	R/W	10	0	Specifies the endian of the data to be transferred to memory. (This bit is valid only when the YUV 420/422 Semi-Planar mode is set by using the PIXELMODE bit.) Bit 32 Bit 0 0: Y plane | Y2 | Y3 | Y0 | Y1 | UV plane | U1 | V1 | U0 | V0 | 1: Y plane | Y3 | Y2 | Y1 | Y0 | UV plane | V1 | U1 | V0 | U0 |
DATA_ID	R/W	9	0	Specifies the sequence of data input via the CAM YUV signal. 0: U → Y → V → Y 1: Y → U → Y → V
LD_TMG	R/W	8	0	Selects the register value enable timing (see Figure 3-1). 0: At the beginning of CAM_VS (rising edge of CAM_VS if CAM_VS is positive) 1: At the end of CAM_VS (falling edge of CAM_VS if CAM_VS is positive)
VS_DET	R/W	7	0	Selects the CAM_VS detection clock edge. 0: Rising edge of CAM_CLKI 1: Falling edge of CAM_CLKI
HS_DET	R/W	6	0	Selects the CAM_HS detection clock edge. 0: Rising edge of CAM_CLKI 1: Falling edge of CAM_CLKI
LIMITSEL	R/W	5	0	Selects the limit value of the YUV output data. 0: Conforms to ITU-R BT.656 (Y: 16 to 235, U and V: 16 to 240) 1: All 8 bits are valid (Y, U, and V: 0 to 255)
SYNCMODE	R/W	4	0	Selects the synchronization mode. 0: CAM_VS/CAM_HS signal sampling mode 1: ITU-R BT.656 mode
CLK_EDGE	R/W	3	0	Selects a clock edge. 0: Single-edge transfer 1: Both-edge transfer For single-edge transfer, the valid edge of CAM_CLKI is selected by using the DATA_DET, HS_DET, and VS_DET bits. For both-edge transfer, CAM_VS and CAM_HS are detected at the rising edge.
DATA_DET	R/W	2	0	Selects the CAM YUV detection clock edge. 0: Rising edge of CAM_CLKI 1: Falling edge of CAM_CLKI

(3/3)

Name	R/W	Bit No.	After Reset	Function
VS_POL	R/W	1	0	Selects the polarity of CAM_VS. 0: Positive logic 1: Negative logic The result varies depending on the specified data sampling mode (SYNCTYPE bit). See Figure 3-2 for details.
HS_POL	R/W	0	0	Selects the polarity of CAM_HS. 0: Positive logic 1: Negative logic The result varies depending on the specified data sampling mode (SYNCTYPE bit). See Figure 3-2 for details.

Caution
- **For the SYNCTYPE and SYNCMODE bits, and the modes, see Table 3-2 Relationship Between SYNCTYPE and SYNCMODE Bits and Sampling Modes.**
- **Be sure to set up this register while the CAM_CLKI domain is in the reset state. The operation will not be guaranteed if the values of this register are changed while DMA transfer is being requested or while CAM is operating.**
- **In ITU-R BT.656 mode (SYNCMODE = 1, SYNCTYPE = 0), match the polarity of VS_DET and HS_DET with that of DATA_DET.**

Table 3-2. Relationship Between SYNCTYPE and SYNCMODE Bits and Sampling Modes

Sampling Mode	SYNCTYPE Bit	SYNCMODE Bit
CAM_VS, CAM_HS signal sampling mode	0	0
ITU-R BT.656 mode	0	1
Enable signal sampling mode	1	0

Table 3-3. Relationship Between Sampling Modes and Valid Bits

Sampling Mode	VS_POL	HS_POL	LD_TMG Bit
CAM_VS, CAM_HS signal sampling mode	Valid	Valid	Valid
ITU-R BT.656 mode	Valid	Valid	Valid
Enable signal sampling mode	Valid	Valid	Not valid

Bits other than VS_POL, HS_POL and LD_TMG are valid in all sampling modes.

Figure 3-1. Relationship Between LD_TMG Bit Value and Register Value Enable Timing

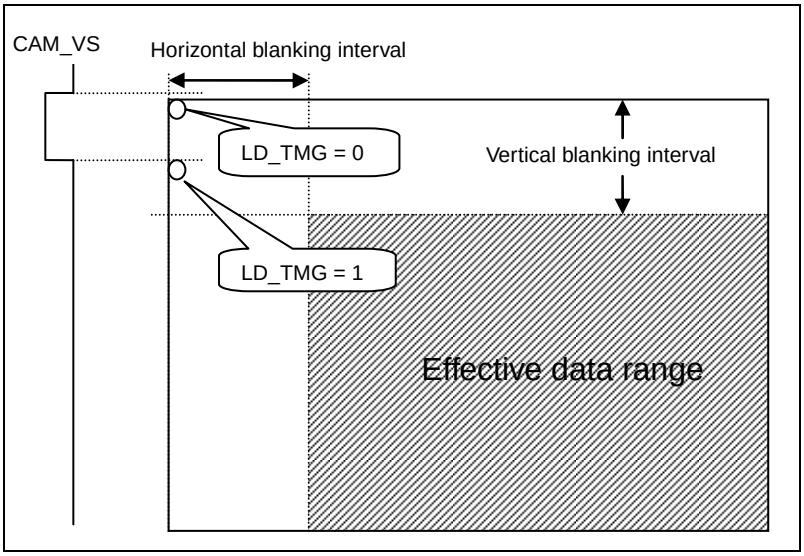
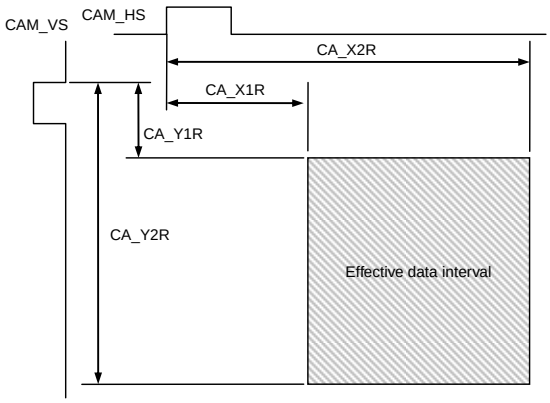


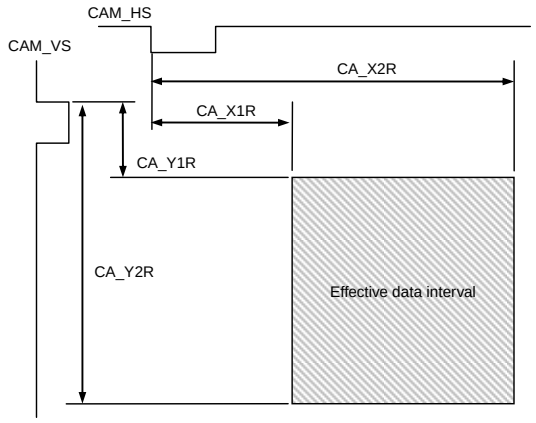
Figure 3-2. Sampling Modes and Settings of VS_POL and HS_POL

CAM_VS/CAM_HS signal sampling mode (SYNCTYPE = 0)

When VS_POL = 0 and HS_POL = 0:
CA_Y1R, CA_Y2R, CA_X1R and CA_X2R are specified based on the rising edges of CAM_VS and CAM_HS.

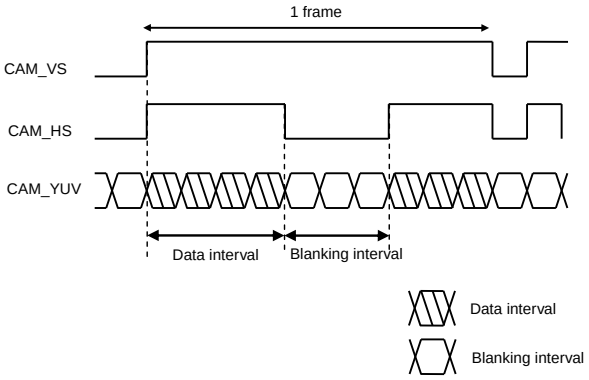


When VS_POL = 1 and HS_POL = 1:
CA_Y1R, CA_Y2R, CA_X1R and CA_X2R are specified based on the falling edges of CAM_VS and CAM_HS.

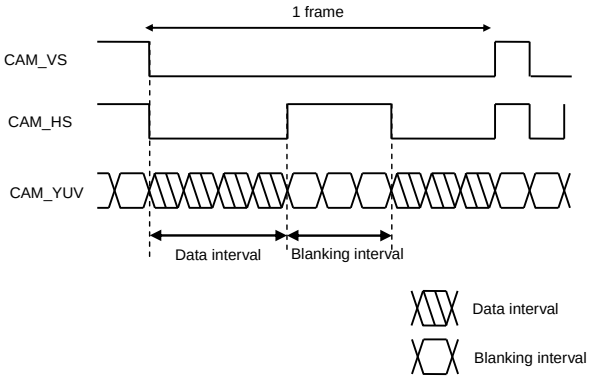


Enable signal sampling mode (SYNCTYPE = 1)

When VS_POL = 0 and HS_POL = 0:
The interval while CAM_VS = 1 and CAM_HS = 1 is regarded as a data interval.
CA_Y1R, CA_Y2R, CA_X1R and CA_X2R are specified based on the rising edges of CAM_VS and CAM_HS.



When VS_POL = 1 and HS_POL = 1:
The interval while CAM_VS = 0 and CAM_HS = 0 is regarded as a data interval.
CA_Y1R, CA_Y2R, CA_X1R and CA_X2R are specified based on the falling edge of CAM_VS and CAM_HS



(2) Byte lane control register

This register (CA_OD_BYTELANE: E10B_0238H) controls which component is to be output to the byte lane when data is stored in memory. This register can be set only in the YUV422 Interleave mode.
Change the value of this register when DMA transfer is not being performed (transfer request register = 0H).

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
YUV_OD_BYTELANE							

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:8	00_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
YUV_OD_BYTELANE	R/W	7:0	E4H	Specifies the byte lane of the data to be transferred to memory (see **Figure 3-3**). (This bit is valid only when the YUV422 Interleave mode is set by using the camera control register (CA_CSR).) Selects the component to be output to the byte lane when data is stored in memory. Interleave 00: Y0 01: Y1 10: U0 11: V0

Bit Corresponding to YUV_OD_BYTELANE	Byte Lane Corresponding to Output Data Component Selection
7:6	31:24
5:4	23:16
3:2	15:8
1:0	7:0

(3) Byte lane control register 2

This register (CA_OD_BYTELANE2: E10B_0254H) controls which component is to be output to the byte lane when data is stored in memory. The settings of this register apply to all output modes.
Change the value of this register when DMA transfer is not being performed (transfer request register = 0H).

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Y_BYTELANE							

7	6	5	4	3	2	1	0
UV_BYTELANE							

(1/2)

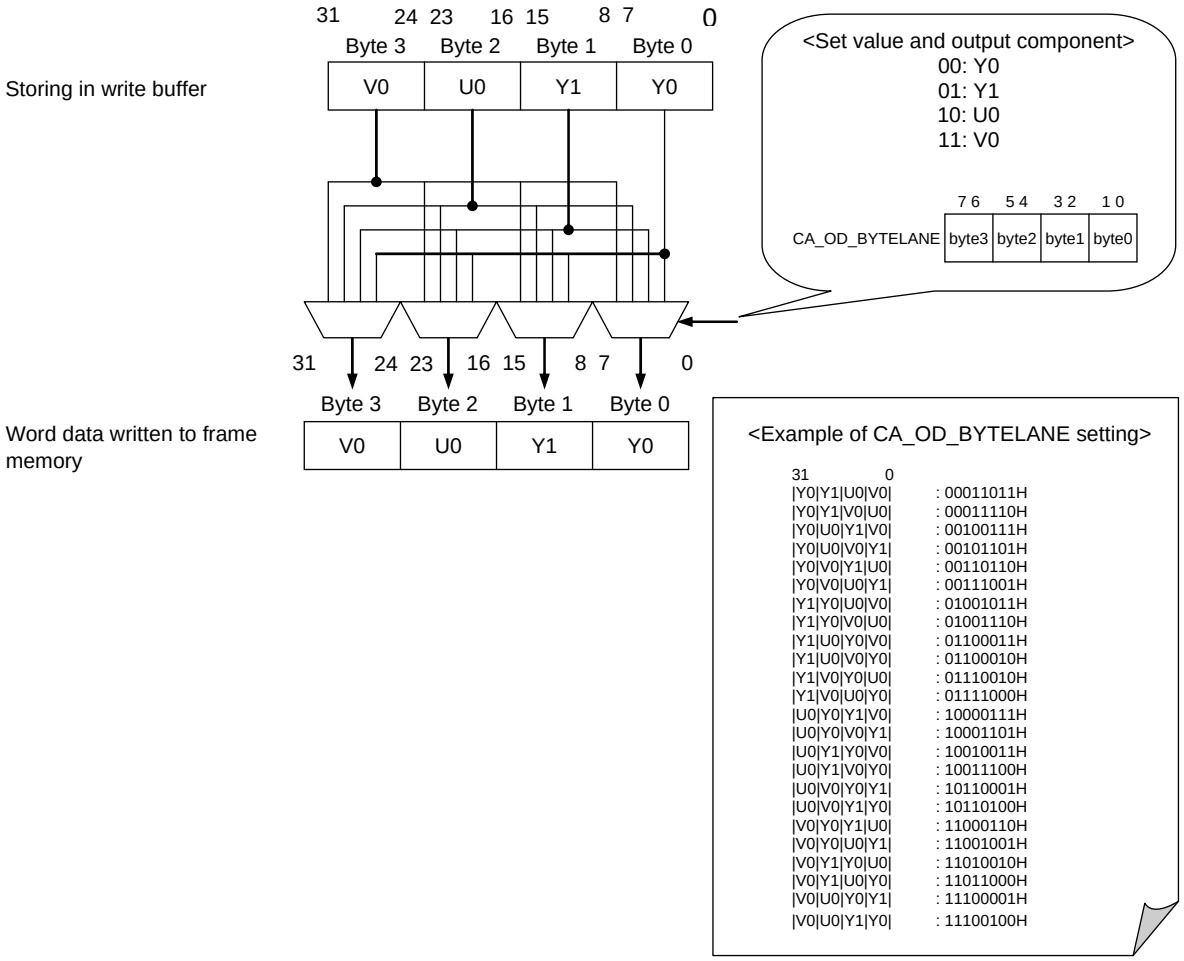
Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:16	0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
Y_BYTELANE	R/W	15:8	E4H	Specifies the byte lane of the data to be transferred to the memory. Selects the component to be output to the byte lane when data is stored in memory. 1) YUV 422 Interleave 00: Y0 01: Y1 10: U0 11: V0 Bit Corresponding to Y_BYTELANE / Byte Lane Corresponding to Output Data Component Selection 7:6 — 31:24 5:4 — 23:16 3:2 — 15:8 1:0 — 7:0 2) YUV 420/422 Semi-Planar and YUV 420/422 Planar 00: Y0 01: Y1 10: Y2 11: Y3 Bit Corresponding to Y_BYTELANE / Byte Lane Corresponding to Output Data Component Selection 7:6 — 31:24 5:4 — 23:16 3:2 — 15:8 1:0 — 7:0

(2/2)

<table>
<tr><th>Name</th><th>R/W</th><th>Bit No.</th><th>After Reset</th><th>Function</th></tr>
<tr><td>UV_BYTELANE</td><td>R/W</td><td>7:0</td><td>E4H</td><td>Specifies the byte lane of the data to be transferred to the memory.
(This bit is valid only when the YUV420/YUV422 Semi-Planar or YUV420/YUV422 Planar mode is set by using the YUVFMT bit.)
Selects the component to be output to the byte lane when data is stored in memory.
1) YUV 420/422 Semi-Planar
00: U0 01: V0 10: U1 11: V1
<table>
<tr><th>Bit Corresponding to UV_ BYTELANE</th><th>Byte Lane Corresponding to Output Data Component Selection</th></tr>
<tr><td>7:6</td><td>31:24</td></tr>
<tr><td>5:4</td><td>23:16</td></tr>
<tr><td>3:2</td><td>15:8</td></tr>
<tr><td>1:0</td><td>7:0</td></tr>
</table>
2) YUV 420/422 Planar
00: U0/V0 01: U1/V1 10: U2/V2 11: U3/V3
<table>
<tr><th>Bit Corresponding to UV_ BYTELANE</th><th>Byte Lane Corresponding to Output Data Component Selection</th></tr>
<tr><td>7:6</td><td>31:24</td></tr>
<tr><td>5:4</td><td>23:16</td></tr>
<tr><td>3:2</td><td>15:8</td></tr>
<tr><td>1:0</td><td>7:0</td></tr>
</table>
</td></tr>
</table>

Figure 3-3. Relationship Between CA_OD_BYTELANE/CA_OD_BYTELANE2 Value and Output Data

■ Setting example when YUV Interleave is the output data format



■ Setting example when YUV Planar is the output data format

Word data written to frame memory

Y3	Y2	Y1	Y0	Y plane
U3	U2	U1	U0	U plane
V3	V2	V1	V0	V plane

Set value: E4H (default)

Y2	Y3	Y0	Y1	Y plane
U2	U3	U0	U1	U plane
V2	V3	V0	V1	V plane

Set value: B1H

Caution Output format and valid byte lane setting:
The valid setting for a byte lane varies depending on the output format. See the following table.

Table 3-4. Output Formats and Valid Byte Lanes

Output Format	DATA_OD Bit (Endian Setting)	CA_OD_BYTELANE Register	CA_OD_BYTELANE2 Register
YUV 422 Interleave	Not valid	Valid	Valid
YUV 420/422 Semi-Planar	Valid	Not valid	Valid
YUV 420/422 Planar	Not valid	Not valid	Valid

Caution Do not specify the byte lane using multiple registers. Use the default value for registers other than the register being used to specify the byte lane. For example, use the CA_OD_BYTELANE2 register with the default value (E4H) when specifying the byte lane by using the DATA_OD bit of the CA_CSR register.

3.2.3 Effective image range setting registers

These registers are used to specify the effective range of the data to be captured from a camera. The design is such that data specified in the effective range starts with U (blue difference signal) or Y (luminance signal). The YUV422 data format handles one pixel as 2 bytes, so one pixel is captured during one CAM_CLKI cycle when executing both-edge transfer, and one pixel is captured during two CAM_CLKI cycles when executing single-edge transfer. Specify the effective image range according to the mode, based on the minimum setting units (YUV422 interleave mode: 2-pixel units, YUV422 interleave mode: 2-pixel units, and Planar mode: 8-pixel units).

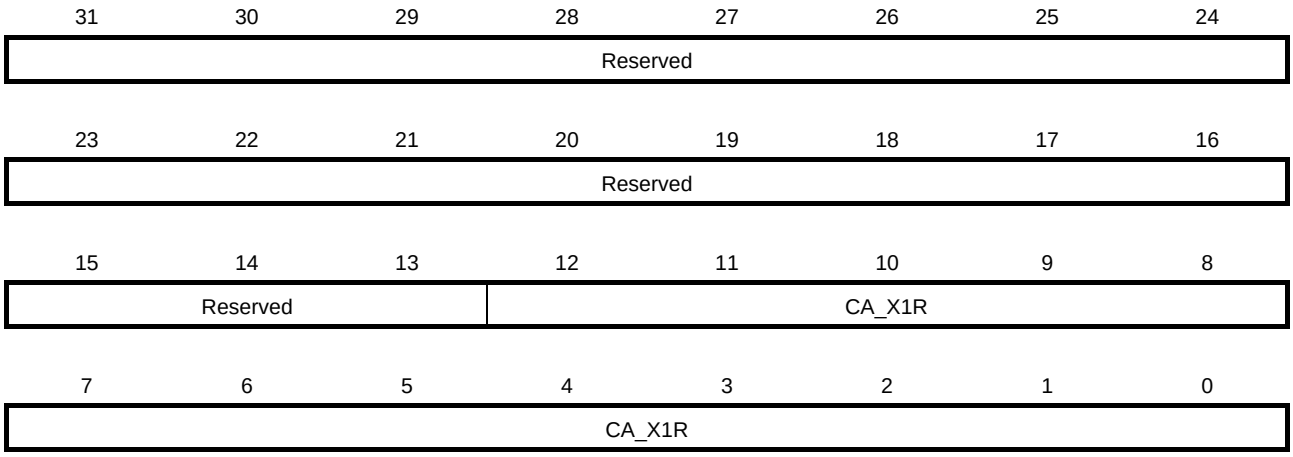
During normal transfer, data in the effective range captured from a camera is transferred to memory. However, note that during resize transfer, the transfer range is specified by the transfer size register and the transfer size is specified by using a different method. For details, see **4.8 Data Transfer Range Specification**.

The effective image range values specified by each register (CA_X1R, CA_X2R, CA_X3R, CA_Y1R, and CA_Y2R) are enabled by the update register. For details, see **3.2.10 Update register**.

(1) Transfer start X coordinate register

This register (CA_X1R: E10B_0030H) specifies the start timing of horizontal transfer according to the number of CAM_CLKI clocks, assuming that the start position is a rising edge of CAM_HS (if the CAM_HS signal has positive logic). Specify the number of clocks until the start timing by using this register.

For details, see **4.8 Data Transfer Range Specification** and **4.9 Restrictions on Transfer Data Range Values**.



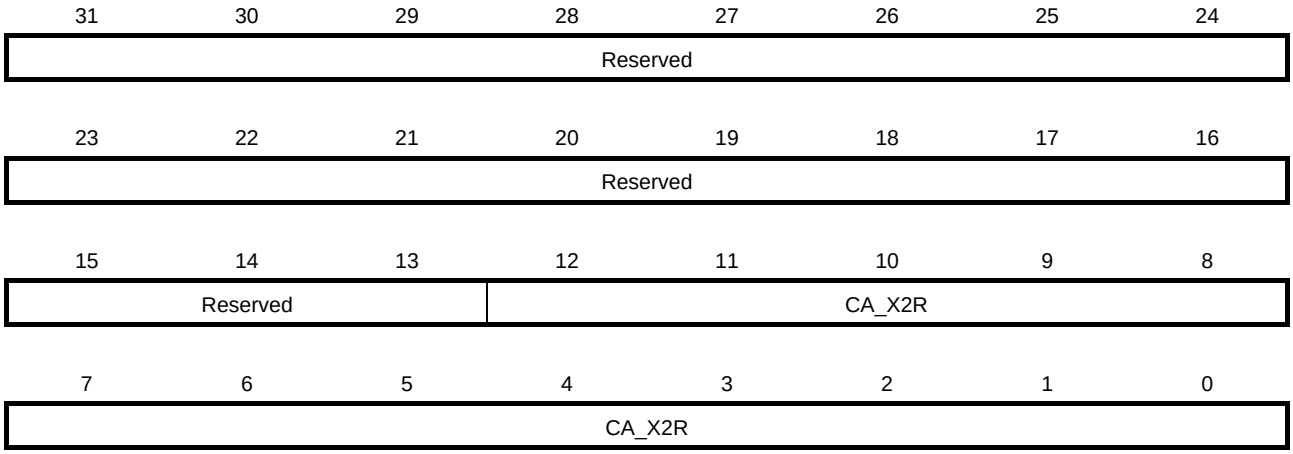
Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:13	0_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
CA_X1R	R/W	12:0	0000H	Transfer start X coordinate register CA_X1R (Camera X1 register) Specifies the number of clocks from CAM_HS to the effective image start position. Specify the number of clocks until cropping starts in the enable signal sampling mode (see 3.2.2 (1) Camera control register (CA_CSR)).

Caution The minimum setting value varies according to the mode.

- **Vertical/horizontal synchronization signal sampling: 0**
- **Enable signal sampling: 0**

(2) Transfer end X coordinate register

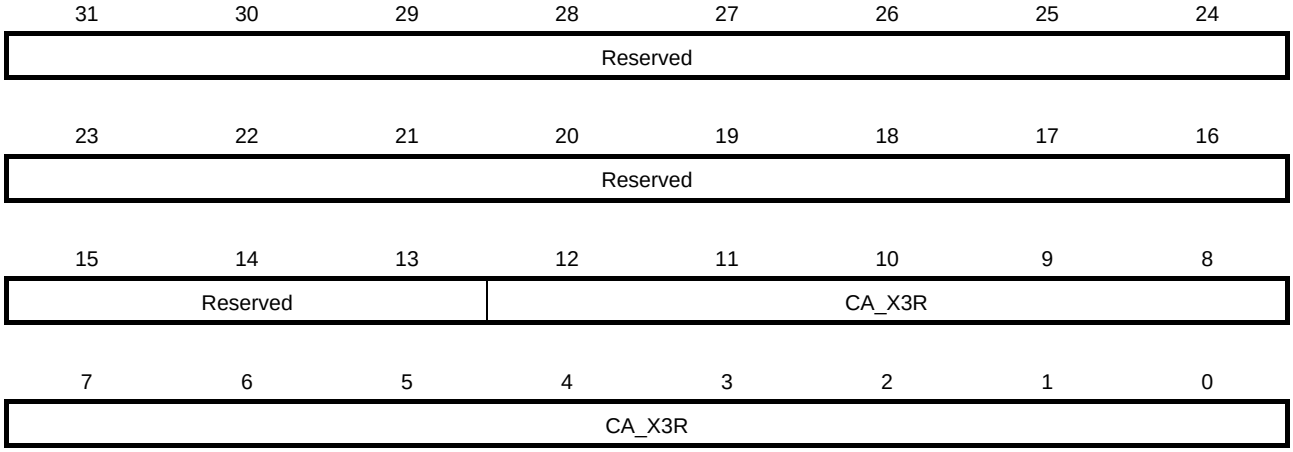
This register (CA_X2R: E10B_0034H) specifies the right edge of the image transfer area. Specify the end position of the area to be made effective, assuming that the end point is a rising edge of CAM_HS (if the CAM_HS signal has positive logic). Specify the number of clocks until the end timing by using this register. An image in the range specified by the CA_X1R and CA_X2R registers is transferred to memory. For details, see **4.8 Data Transfer Range Specification** and **4.9 Restrictions on Transfer Data Range Values**.



Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:13	0_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
CA_X2R	R/W	12:0	0000H	Transfer end X coordinate register CA_X2R (Camera X2 register) Specifies the number of clocks from CAM_HS to the effective image end position. Specify the number of clocks until cropping ends in the enable signal sampling mode (see 3.2.2 (1) Camera control register (CA_CSR)).

(3) Transfer end X coordinate register (dedicated to enable signal sampling mode)

This register (CA_X3R: E10B_0240H) is valid only in the enable signal sampling mode (SYNCTYPE bit of camera control register = 1). Specify the number of clocks until the effective image end position.
For details, see **4.8 Data Transfer Range Specification** and **4.9 Restrictions on Transfer Data Range Values**.
This register is ignored in the CAM_VS/CAM_HS signal sampling mode (SYNCTYPE bit of CA_CSR register = 0).

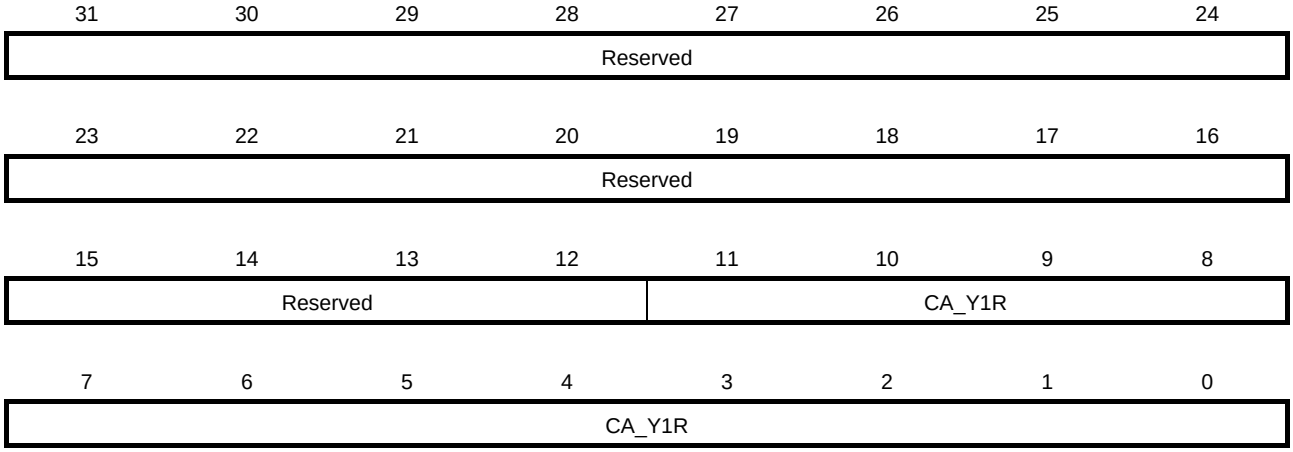


Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:13	0_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
CA_X3R	R/W	12:0	0000H	Transfer end X coordinate register CA_X3R (Camera X3 register) Specifies the number of clocks until the effective image X end position in the enable signal sampling mode.

(4) Transfer start Y coordinate register

This register (CA_Y1R: E10B_0038H) specifies the upper edge of the image transfer area. Specify the image transfer start line according to the number of CAM_HS counts, assuming that the start position is a rising edge of CAM_VS (if the CAM_VS signal is the positive logic).

For details, see **4.8 Data Transfer Range Specification** and **4.9 Restrictions on Transfer Data Range Values**.

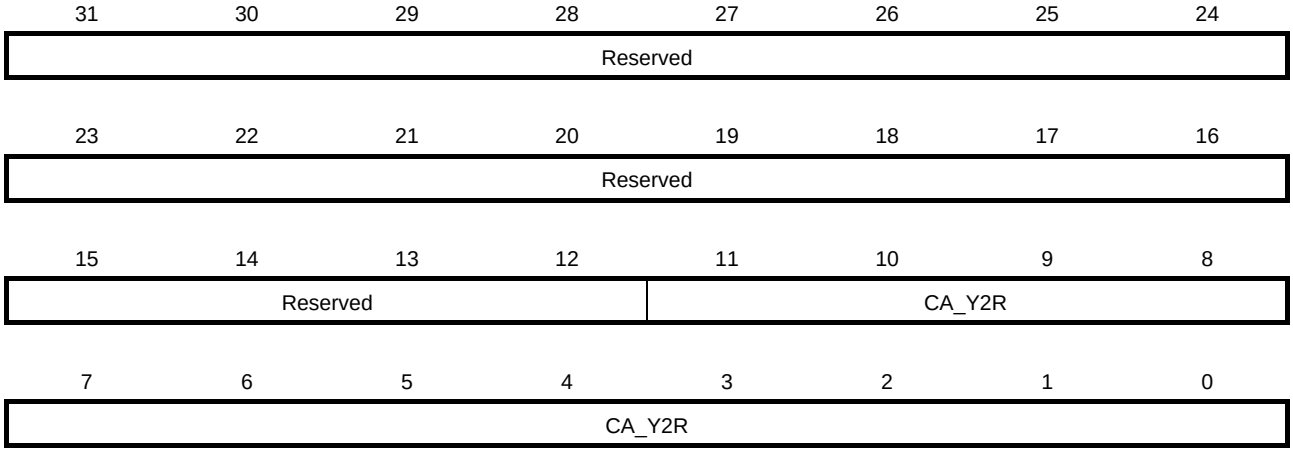


Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:12	0_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
CA_Y1R	R/W	11:0	000H	Transfer start Y coordinate register CA_Y1R (Camera Y1 register) Specifies the effective image start line. Specify the number of lines until cropping starts in the enable signal sampling mode (3.2.2 (1) Camera control register (CA_CSR)). If the output format is YUV420, specify the value in 2-line units. For other formats, the value can be specified in line units.

(5) Transfer end Y coordinate register

This register (CA_Y2R: E10B_003CH) specifies the bottom edge of the image transfer area. Specify the image transfer end line according to the number of CAM_HS counts, assuming that the end position is a rising edge of CAM_VS (if the CAM_VS signal has positive logic).

For details, see **4.8 Data Transfer Range Specification** and **4.9 Restrictions on Transfer Data Range Values**.

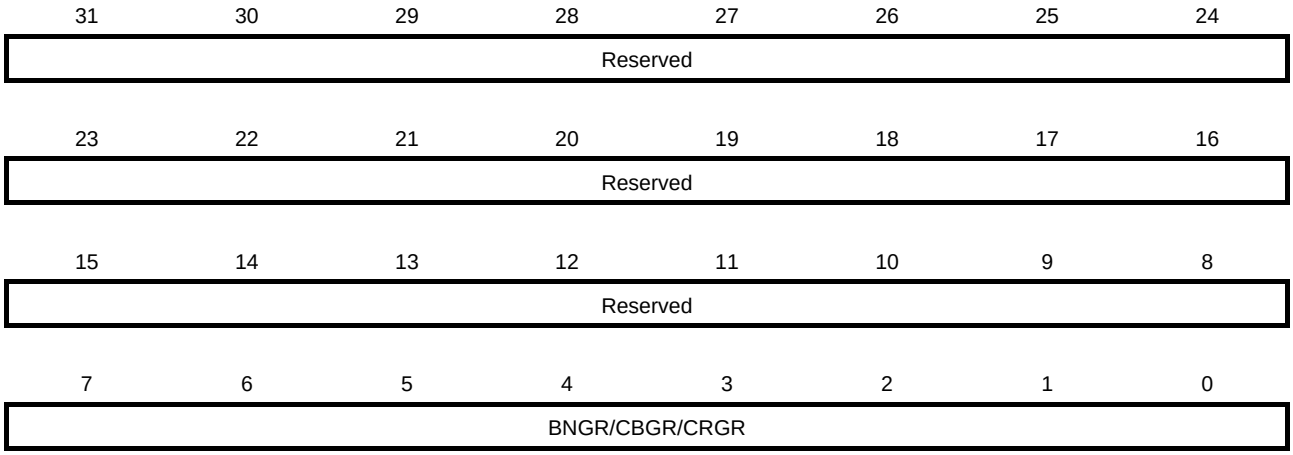


Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:12	0_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
CA_Y2R	R/W	11:0	000H	Transfer end Y coordinate register CA_Y2R (Camera Y2 register) Specifies the effective image end line. Specify the number of lines until cropping ends in the enable signal sampling mode (3.2.2 (1) Camera control register (CA_CSR)). If the output format is YUV420, specify the value in 2-line units. For other formats, the value can be specified in line units.

3.2.4 Level adjustment registers

(1) Gain registers (Luminance signal, U color difference signal, V color difference signal)

These registers (CA_BNGR: E10B_0044H, CA_CBGR: E10B_004CH, CA_CRGR: E10B_0054H) are used to adjust the gain for input data. The values can be specified for Y, U, and V, respectively.
These registers store an unsigned 8-bit fixed-point value. The MSB (INT0 bit) is used as the integer part and the 7 bits from the LSB (DEC[6:0]) are used as the decimal part. A gain of 0 to about 1.99 can be specified, in 1/128 units. If not adjusting the gain, set these registers to 80H (INT0 = 1, DEC[6:0] = 0).
If the gain registers are set to 0, the Y, U, and V component data items are replaced with the values specified by the respective offset registers and transferred to memory.
The values specified by these registers are enabled by the update register. For details, see **3.2.10 Update register**.



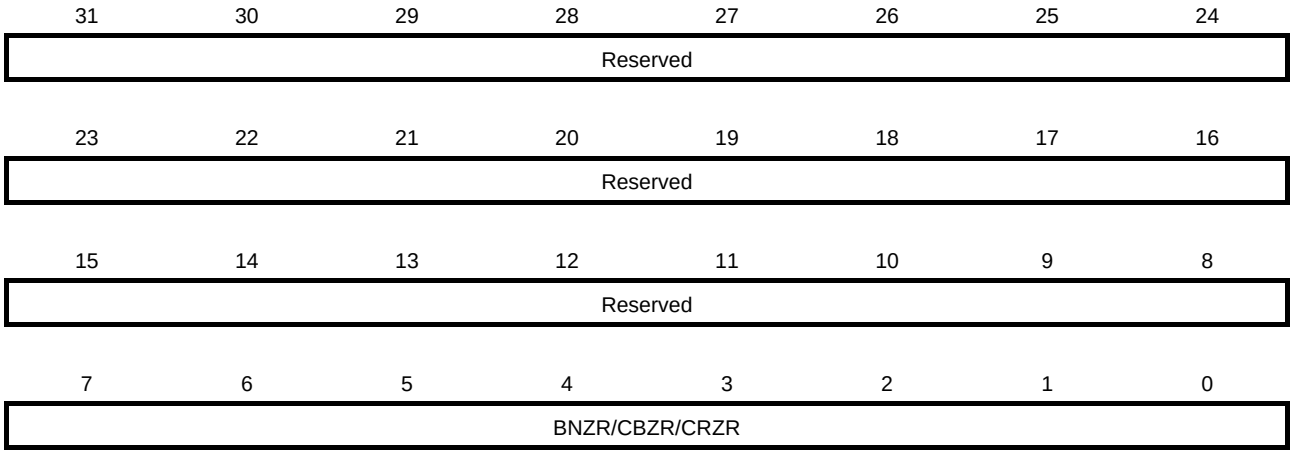
Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:8	00_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
BNGR	R/W	7:0	80H	Luminance gain register Ygain = Yin × BNGR
CBGR	R/W	7:0	80H	U color difference gain register Ugain = Uin × CBGR
CRGR	R/W	7:0	80H	V color difference gain register Vgain = Vin × CRGR

(2) Offset registers (Luminance signal, U color difference signal, V color difference signal)

These registers (CA_BNZR: E10B_0040H, CA_CBZR: E10B_0048H, CA_CRZR: E10B_0050H) are used to add and reduce the offset for data after gain adjustment. The values can be specified for Y, U, and V, respectively. These registers store a signed 8-bit integer value. The MSB (sign bit) indicates the sign and the 7 bits from the LSB (OD[6:0]) indicate the integer part. Values from –128 to +127 can be specified. If not adjusting the gain, set these registers to 0H.

These registers specify the Y/U/V data value when the gain registers are set to 0. If the register corresponding to the component data is set to 0, the data is replaced with the value specified by the offset register and transferred to memory. By using this mode, the color of an image can be converted to monochrome or sepia and transferred.

The values specified by these registers are enabled by the update register. For details, see **3.2.10 Update register**.

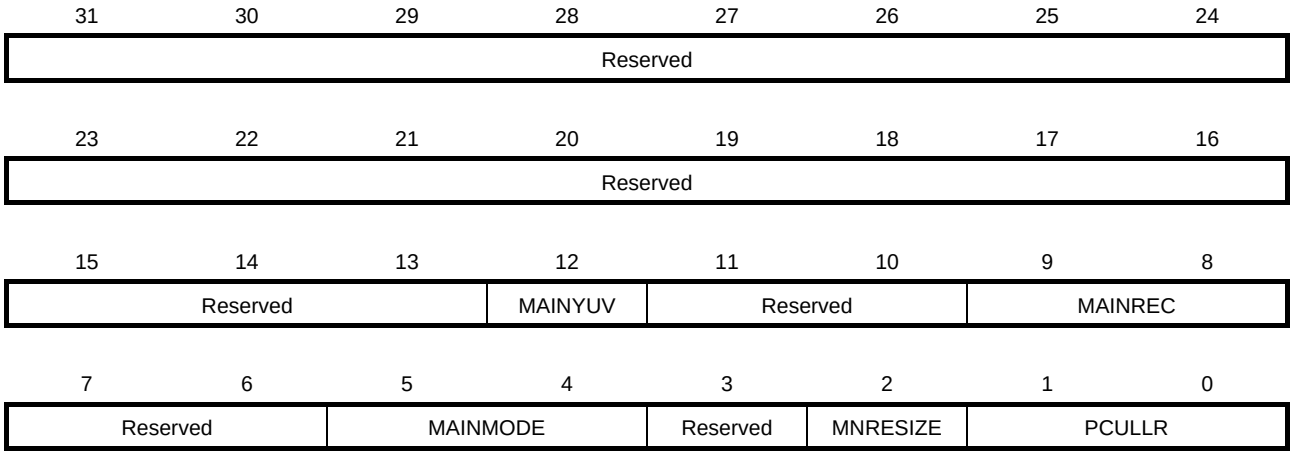


Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:8	00_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
BNZR	R/W	7:0	00H	Luminance offset register Yoffset = Ygain + BNZR Specify a signed 8-bit integer from –128 to +127 (2's complement) for BNZR.
CBZR	R/W	7:0	00H	U color difference offset register Uoffset = Ugain + CBZR Specify a signed 8-bit integer from –128 to +127 (2's complement) for CBZR.
CRZR	R/W	7:0	00H	V color difference offset register Voffset = Vgain + CRZR Specify a signed 8-bit integer from –128 to +127 (2's complement) for CRZR.

3.2.5 Transfer control registers

(1) Transfer control register

This register (CA_DMACNT: E10B_0080H) controls data transfer.
Change the values only when DMA transfer is not being performed (transfer request register = 0H).



(1/2)

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:13	0_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
MAINYUV	R/W	12	0	Specifies the format of main frame output to memory. 0: YUV422 1: YUV420
Reserved	R	11:10	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
MAINREC	R/W	9:8	0H	Indicates the history of the last frame transferred as a main frame. The history can be checked by reading these bitsNote 1. Writing 1, 1 clears the history. Writing other values is invalid.
Reserved	R	7:6	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.

MAINREC1	MAINREC0	Read	Write
0	0	A frame	–
0	1	A frame	–
1	0	B frame	–
1	1	B frame	Clears the history

(2/2)

<table>
<tr><th>Name</th><th>R/W</th><th>Bit No.</th><th>After Reset</th><th>Function</th></tr>
<tr><td>MAINMODE</td><td>R/W</td><td>5:4</td><td>0H</td><td>Specifies the main frame transfer mode.
<table>
<tr><th>MAIN MODE1</th><th>MAIN MODE0</th><th>Transfer Mode</th></tr>
<tr><td>0</td><td>0</td><td>Single transfer
Only one frame is transferred to the frame specified by the transfer frame register.</td></tr>
<tr><td>0</td><td>1</td><td>Repeat transfer (frame buffer fixed)
A frame is repeatedly transferred to the destination specified by the transfer frame register.</td></tr>
<tr><td>1</td><td>0</td><td>Repeat transfer (double buffer)Note 2
A and B frames are transferred alternately, starting with an A frame.</td></tr>
<tr><td>1</td><td>1</td><td>Repeat transfer (double buffer)Note 2
A and B frames are transferred alternately, starting with an A frame.</td></tr>
</table></td></tr>
<tr><td>Reserved</td><td>R</td><td>3</td><td>0</td><td>Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.</td></tr>
<tr><td>MNRESIZE</td><td>R/W</td><td>2</td><td>0</td><td>Specifies whether to resize main frames.
0: Does not resize main frames.
1: Resizes main frames.</td></tr>
<tr><td>PCULLR</td><td>R/W</td><td>1:0</td><td>0H</td><td>Specifies the skipping ratio of transfer frames. If no skipping mode is specified, every data frame is transferred. If a skipping ratio is specified, one data frame is transferred at intervals of the specified ratio.
<table>
<tr><th>PCULLR1</th><th>PCULLR0</th><th>Mode</th><th>Transfer Rate in 30 fps Operation</th></tr>
<tr><td>0</td><td>0</td><td>No skipping</td><td>30 fps</td></tr>
<tr><td>0</td><td>1</td><td>1/2 skipping</td><td>15 fps</td></tr>
<tr><td>1</td><td>0</td><td>1/3 skipping</td><td>10 fps</td></tr>
<tr><td>1</td><td>1</td><td>1/4 skipping</td><td>7.5 fps</td></tr>
</table></td></tr>
</table>

Caution The operation will not be guaranteed if the values of this register are changed while DMA transfer is being requested or while CAM is operating.

Notes 1. The history value becomes valid after transfer is completed.

2. To perform repeat transfer (double buffer), reset CAM immediately before transfer.

(2) Transfer frame register

This register (CA_FRAME: E10B_0084H) specifies the transfer frame destination. This setting is valid when single transfer or repeat transfer (frame buffer fixed) is specified in the transfer control register.
Change the values while DMA transfer is not being performed (transfer request register = 0H).

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved						MAINFRM	

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:2	0000_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
MAINFRM	R/W	1:0	1H	Specifies the transfer destination of a main frame. This setting is valid when single transfer or repeat transfer (frame buffer fixed) is specified by the transfer control register.

MAINFRM1	MAINFRM0	Frame
0	0	A frame
0	1	A frame
1	0	B frame
1	1	B frame

(3) Transfer request register

This register (CA_DMAREQ: E10B_0088H) specifies the starting of DMA transfer.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							MAINREQ

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:1	0000_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
MAINREQ	R	0	0	This bit is set to 1 when DMAREQ is acknowledged. This bit is cleared when DMA transfer terminates. In single transfer mode, this bit is cleared automatically after the end of 1-frame transfer.
	W		–	Requests DMA transfer when set to 1. The operation varies depending on the value of the MAINMODE bit of the transfer control register (CA_DMACNT). Single transfer mode: 1-frame transfer is performed. Repeat transfer mode: DMA transfer is repeated until the MAINSTOP bit of the CA_DMASTOP register is set to 1. Writing 0 to the MAINREQ bit does not affect the setting.

(4) Transfer request cancellation register

This register (CA_DMASTOP: E10B_008CH) stops transfer during repeat transfer. This register is enabled at transfer frame termination after request cancellation is specified. The transfer request status can be checked by polling the transfer request register.

This is a write-only register. Writing 1 terminates DMA transfer. Writing 0 to this register does not affect the setting.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

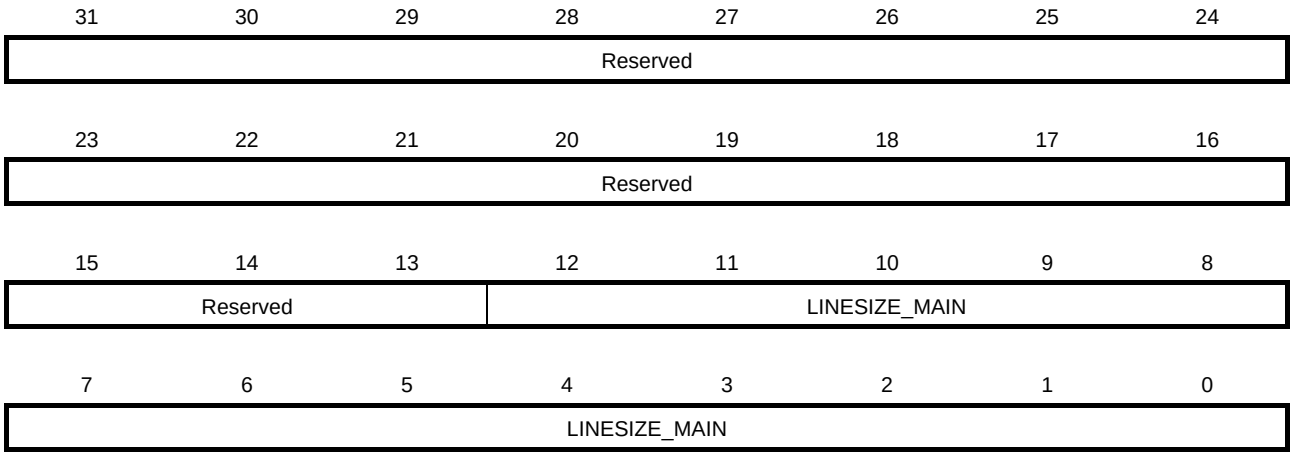
15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							MAINSTOP

Name	R/W	Bit No.	After Reset	Function
Reserved	W	31:1	0000_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
MAINSTOP	W	0	0	Stops main frame repeat transfer. 1: Stops transfer.

3.2.6 Address addition value registers

This register (CA_LINESIZE_MAIN: E10B_0100H) specifies the address size of one line of a transfer image. By using another method to specify the address size of one line of an image already saved in the transfer destination memory, a camera image in the required rectangular position can be sent to overwrite an image on the memory. The values specified by this register are enabled by the update register. For details, see **3.2.10 Update register**.



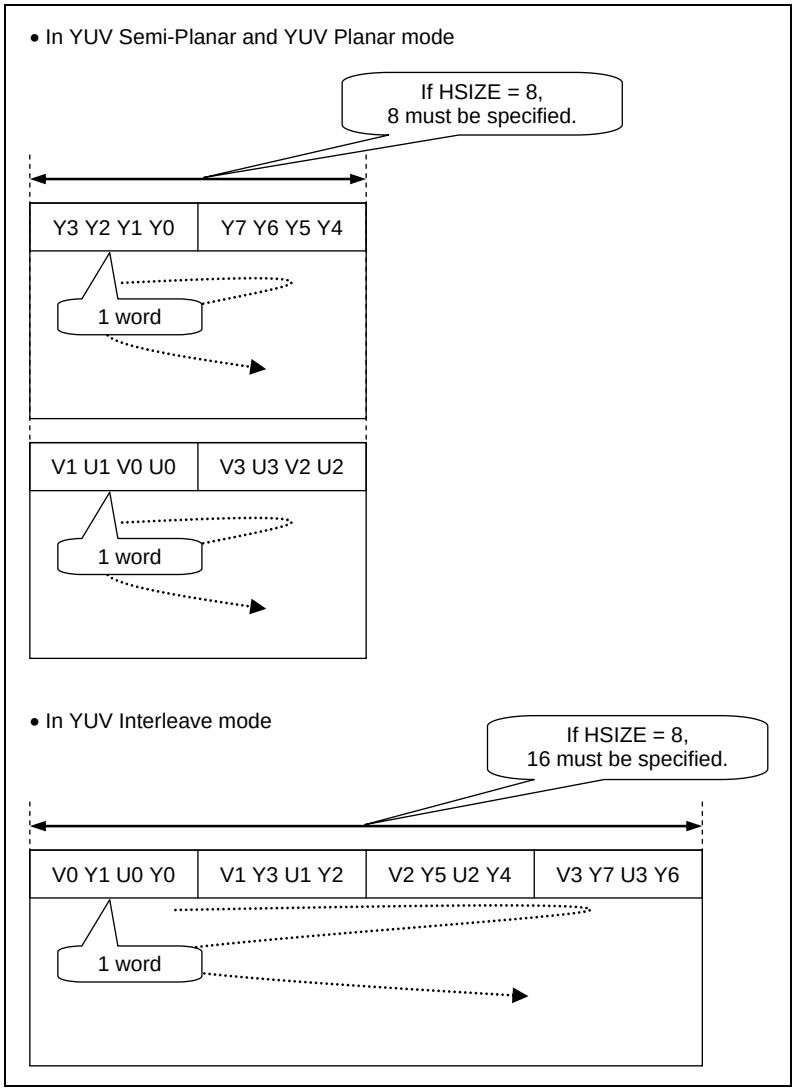
Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:13	0_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
LINESIZE_MAIN	R/W	12:0	0000H	Specifies the address addition value for one line. (The lower 2 bits are fixed to 0.)

Caution The specifiable value varies between the YUV420/YUV422 Semi-Planar mode and YUV422 Interleave mode (see 3.2.2 (1) Camera control register (CA_CSR)).

Table 3-5. Minimum Specifiable Unit

Output Format	Pixel Mode	Minimum Specifiable Unit
YUV422	YUV Interleave	4 bytes (1 word) (2 pixels)
	YUV Semi-Planar	4 bytes (1 word) (4 pixels)
	YUV Planar	8 bytes (2 words) (8 pixels)
YUV420	YUV Semi-Planar	4 bytes (1 word) (4 pixels)
	YUV Planar	8 bytes (2 words) (8 pixels)

Figure 3-4. Memory Storage and Specified Values



3.2.7 Resize registers

(1) Horizontal reduction ratio register

This register (CA_XRATIO_MAIN: E10B_0104H) specifies a reduction ratio in the horizontal direction. This register is valid when the RESIZE bit of the CA_DMACNT register is set to 1.
The values specified by this register are enabled by the update register. For details, see **3.2.10 Update register**.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved						XRATIO_MAIN	

7	6	5	4	3	2	1	0
XRATIO_MAIN							

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:10	00_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
XRATIO_MAIN	R/W	9:0	000H	Specifies a reduction ratio in the horizontal direction. The specifiable range is 0 to 959. Reduction transfer becomes valid when the MNRESIZE bit of the CA_DMACNT register is set to 1. In this case, reduction is not performed if XRATIO is set to 0. The reduction ratio is obtained according to XRATIO, by the following equation. $\text{Reduction ratio} = \frac{64}{64 + \text{XRATIO}}$

(2) Vertical reduction ratio register

This register (CA_YRATIO_MAIN: E10B_0108H) specifies a reduction ratio in the vertical direction. This register is valid when the RESIZE bit of the CA_DMACNT is set to 1.

The values specified by this register are enabled by the update register. For details, see **3.2.10 Update register**.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved						YRATIO_MAIN	

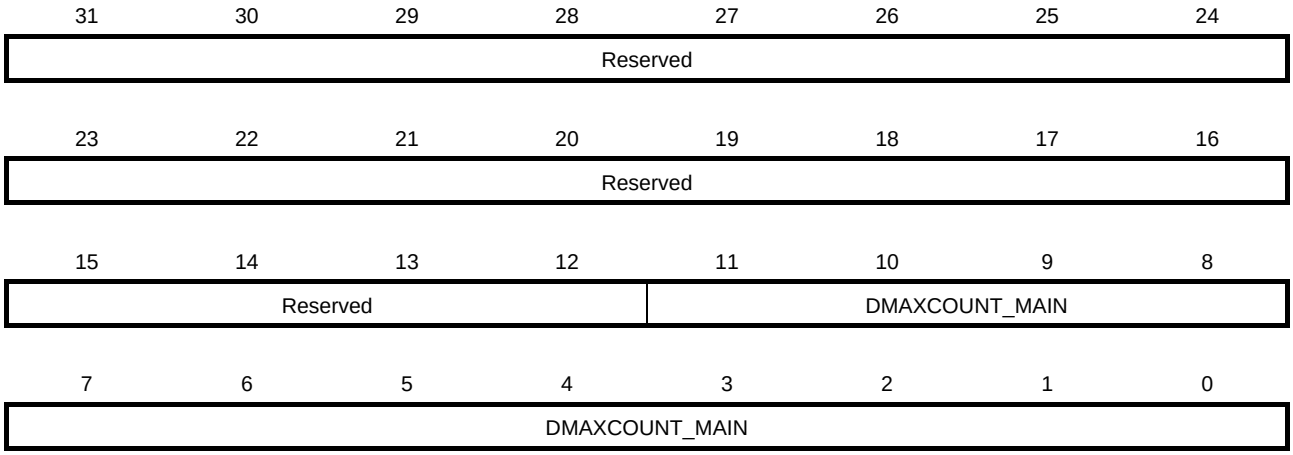
7	6	5	4	3	2	1	0
YRATIO_MAIN							

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:10	00_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
YRATIO_MAIN	R/W	9:0	000H	Specifies a reduction ratio in the vertical direction. The specifiable range is 0 to 959. Reduction transfer becomes valid when the MNRESIZE bit of the CA_DMACNT register is set to 1. In this case, reduction is not performed if YRATIO is set to 0. The reduction ratio is obtained according to YRATIO, by the following equation. $\text{Reduction ratio} = \frac{64}{64 + \text{YRATIO}}$

3.2.8 Frame control registers

(1) Horizontal transfer size register

This register (CA_DMAX_MAIN: E10B_010CH) specifies the number of horizontal pixels to be transferred. Specify the transfer pixels for each mode based on the minimum pixel units (YUV422 Interleave mode: 2-pixel units, Semi-Planar mode: 4-pixel units, and Planar mode: 8-pixel units).
The values specified by this register are enabled by the update register. For details, see **3.2.10 Update register**.



Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:12	0_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
DMAXCOUNT_MAIN	R/W	11:0	000H	Specifies the number of horizontal pixels to be transferred (4,088 max.). Specify in 2-, 4- or 8-pixel units depending on the mode. (The lowest bit is fixed to 0.)

Caution The minimum specifiable value varies between the YUV420/YUV422 Semi-Planar mode and YUV422 Interleave mode (see 3.2.2 (1) Camera control register (CA_CSR)).

(2) Vertical transfer size register

This register (CA_DMAY_MAIN: E10B_0110H) specifies the number of lines to be transferred vertically. The number of lines to be transferred can be specified in line units.

The values specified by this register are enabled by the update register. For details, see **3.2.10 Update register**.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

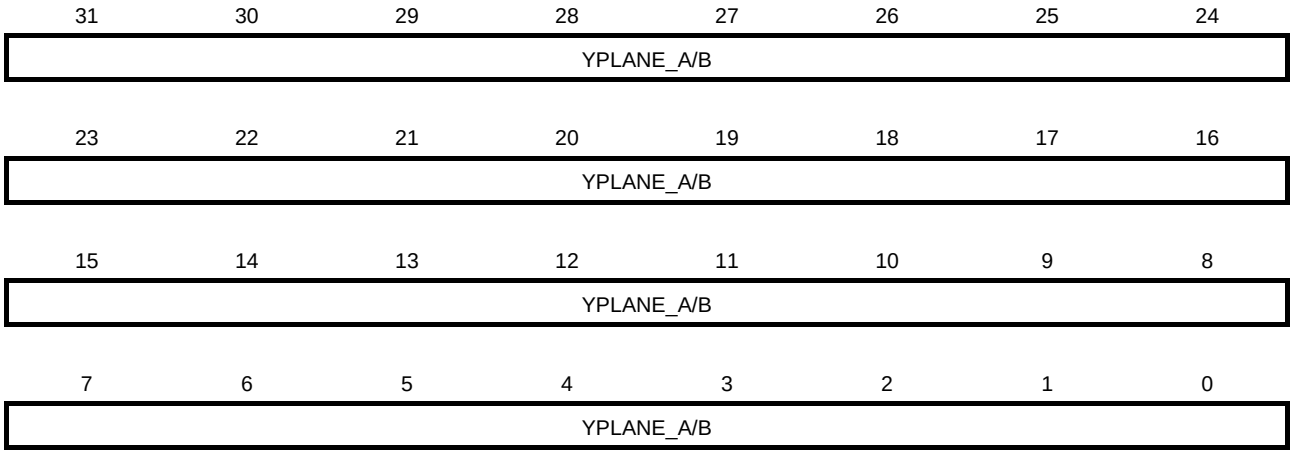
15	14	13	12	11	10	9	8
Reserved				DMAYCOUNT_MAIN			

7	6	5	4	3	2	1	0
DMAYCOUNT_MAIN							

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:12	0_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
DMAYCOUNT_MAIN	R/W	11:0	000H	Specifies the number of lines to be transferred vertically (4,092 max.). The value can be specified in line units.

(3) Y plane transfer address registers (A/B frame)

These registers (CA_YPLANE_A: E10B_0114H, CA_YPLANE_B: E10B_011CH) specify the transfer destination addresses of Y plane data.
To support double buffer control, two frame setting registers for main frames A and B are provided.
For details about double buffer control, see **4.11.2 Transfer mode**.
Change the values while DMA transfer is not being performed (transfer request register = 0H).



Name	R/W	Bit No.	After Reset	Function
YPLANE_A/B	R/W	31:0	0000_0000H	Specifies a Y plane address. The lower 2 bits are fixed to 0.

Caution In the YUV422 Interleave mode (see 3.2.2 (1) Camera control register (CA_CSR)), all the YUV data is output to the addresses specified by these registers.

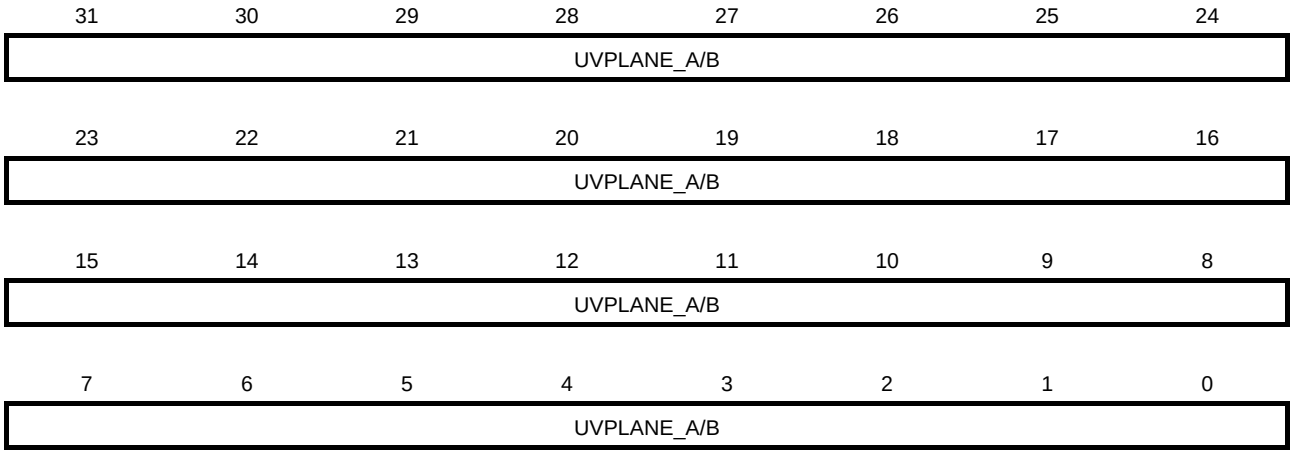
(4) UV plane transfer address registers (A/B frame)

These registers (CA_UVPLANE_A: E10B_0118H, CA_UVPLANE_B: E10B_0120H) specify the transfer destination addresses of UV plane data.

To support double buffer control, two frame setting registers for main frames A and B are provided.

For details about double buffer control, see **4.11.2 Transfer mode**.

Change the values while DMA transfer is not being performed (transfer request register = 0H).



Name	R/W	Bit No.	After Reset	Function
UVPLANE_A/B	R/W	31:0	0000_0000H	Specifies a UV plane address. The lower 2 bits are fixed to 0.

Caution The addresses specified by these registers are ignored in the YUV422 Interleave mode (see 3.2.2 (1) Camera control register (CA_CSR)).

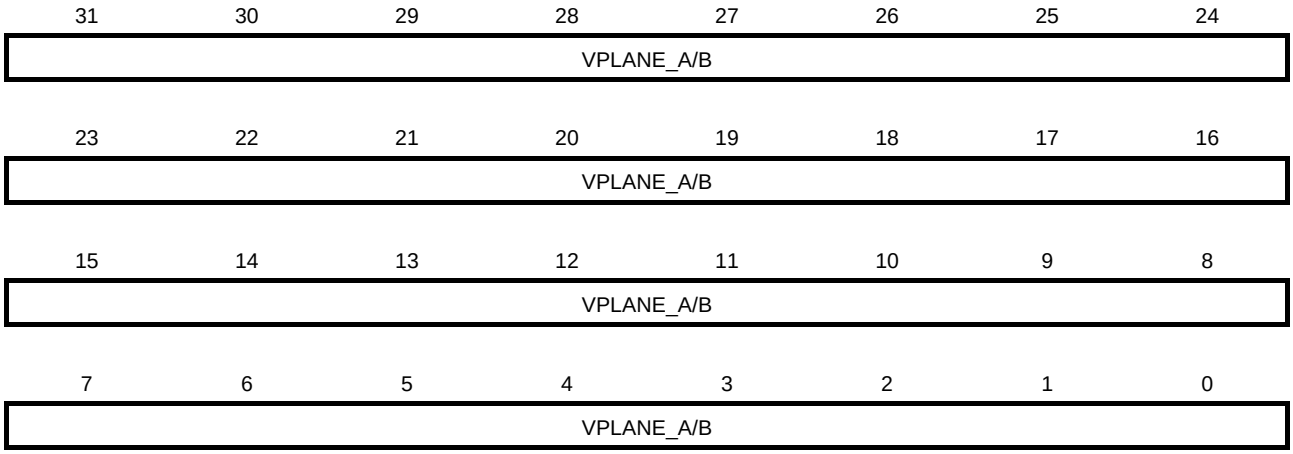
(5) V plane transfer address register (A/B frame)

These registers (CA_VPLANE_A: E10B_0244H, CA_VPLANE_B: E10B_0248H) specify the transfer destination addresses of V plane data.

To support double buffer control, two frame setting registers for main frames A and B are provided.

For details about double buffer control, see **4.11.2 Transfer mode**.

Change the values while DMA transfer is not being performed (transfer request register = 0H).



Name	R/W	Bit No.	After Reset	Function
VPLANE_A/B	R/W	31:0	0000_0000H	Specifies a V plane address. The lower 2 bits are fixed to 0.

Caution The addresses specified by these registers are ignored in the YUV422 Interleave and YUV420/422 Semi-planar modes (see 3.2.2 (1) Camera control register (CA_CSR)).

3.2.9 Module control register

This register (CA_MODULECONT: E10B_022CH) initializes a module synchronizing with CAM_CLKI.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

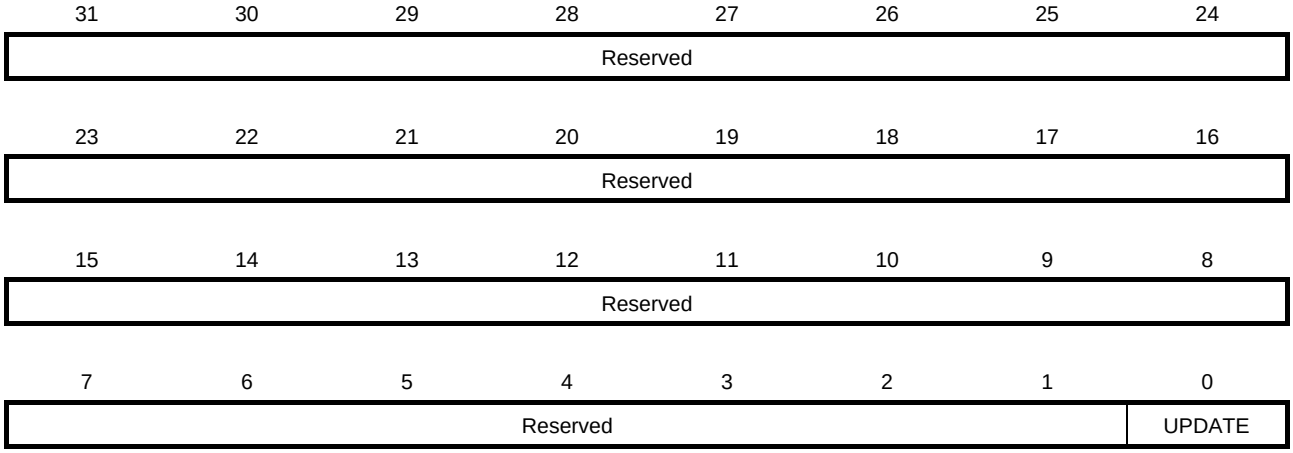
7	6	5	4	3	2	1	0
Reserved							HW_RSTZ

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:1	0000_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
HW_RSTZ	R/W	0	0	Performs hardware reset of modules operating with CAM_CLKI. 0: Reset 1: Cancels reset.

Caution The operation will not be guaranteed if the values of this register are changed while DMA transfer is being requested or while CAM is operating.

3.2.10 Update register

This register (CA_UPDATE: E10B_0230H) enables the capture position, capture size, resize ratio, DMA transfer size, YUV offset/gain, and flipping specified by the corresponding register. Writing 1 to the UPDATE bit sets the update reservation status in which each specified value is ready to be updated. When a register is updated (defined by the LD_TMG bit of camera control register), each specified value is enabled and the update register is cleared. Writing 0 to this register does not affect the setting.

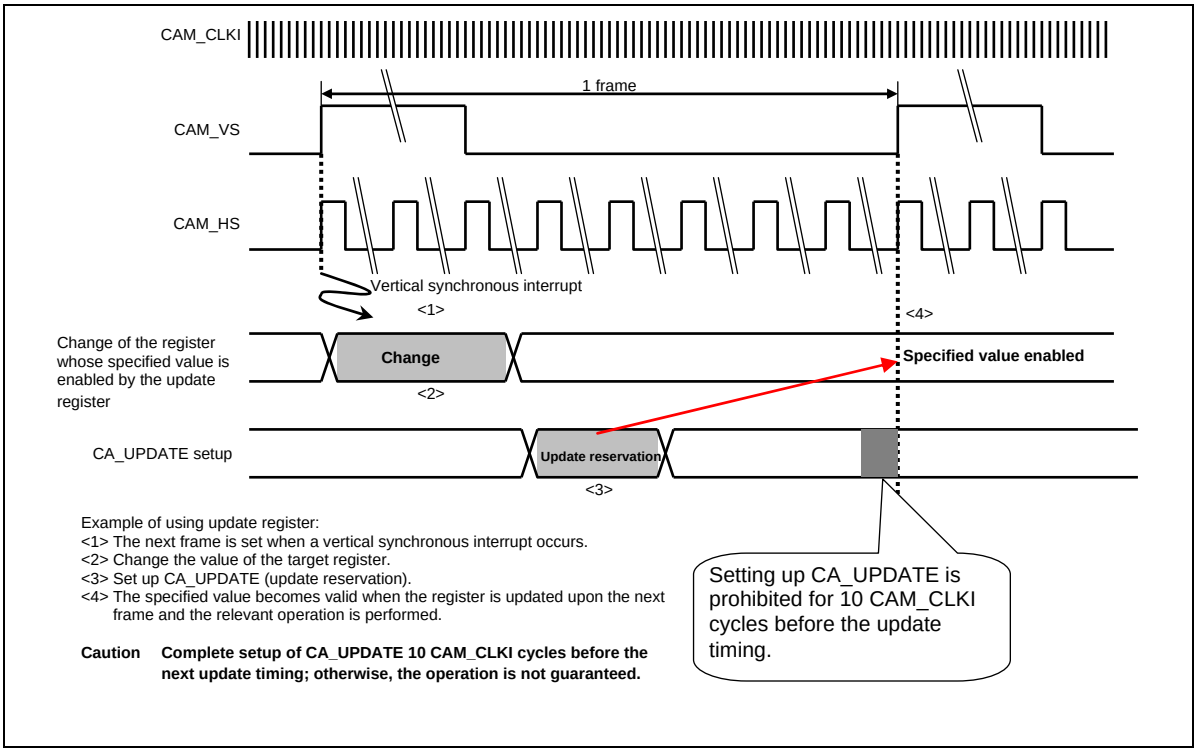


Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:1	0000_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
UPDATE	R	0	0	Specifies the update reservation status. 0: The set values are not updated. 1: The set values are updated at the register update timing.
	W			Enables the value specified by a specific register. 1: Reservation for updating

Caution **The values specified by the following registers are enabled by the update register. Do not change the values of registers other than the update register while DMA transfer is being requested or while CAM is operating.**

- CA_X (Y)1(2)R
- CA_X3R
- CA_CBG(Z)R
- CA_LINESIZE_MAIN
- CA_DMAX(Y)_MAIN
- CA_BNG(Z) R
- CA_CRG(Z) R
- CA_X (Y)RATIO_MAIN
- CA_MIRROR

Figure 3-5. Update Register Setup Timing



3.2.11 Horizontal/vertical flip control register

This register (CA_MIRROR: E10B_0234H) specifies flipping of an image during DMA transfer. Horizontal flip and vertical flip can be specified separately.

The values specified by this register are enabled by the update register. For details, see **3.2.10 Update register**.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

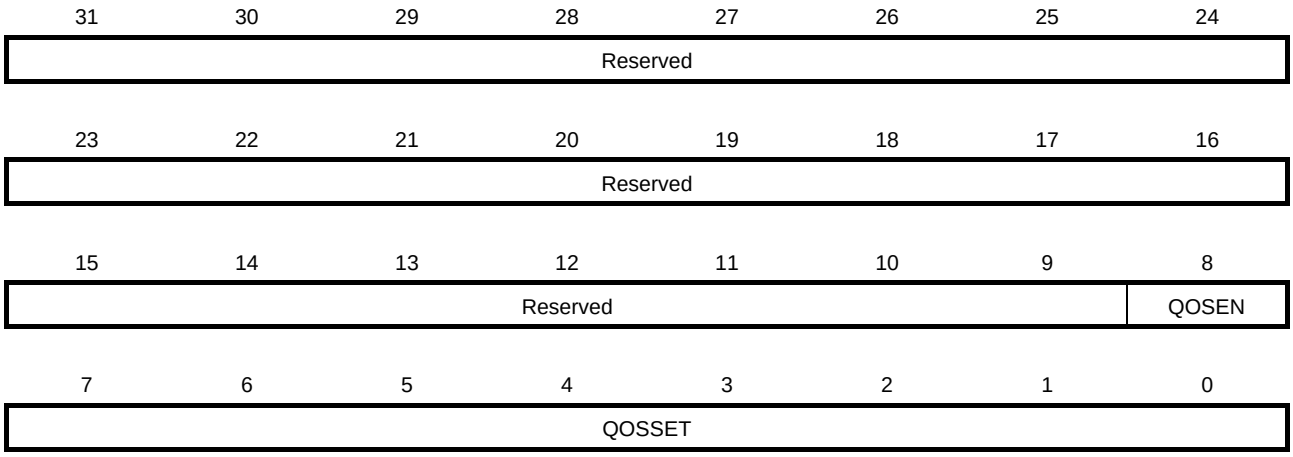
15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				MAIN_MIRROR		Reserved	

Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:4	000_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
MAIN_MIRROR	R/W	3:2	00b	Specifies flipping of the main frame. MAIN_MIRROR: 00b – No flip; 01b – Horizontal flip; 10b – Vertical flip; 11b – Horizontal and vertical flip (180° rotation)
Reserved	R	1:0	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.

3.2.12 Simple QoS setting register

This register (CA_QOS: E10B_0258H) specifies simple QoS.
Simple QoS is used to prevent overrun and underrun from occurring in image-system modules.
When a QoS request is issued from an image-system module, the bus switch temporarily gives a higher priority to access from that module, which reduces the access latency.



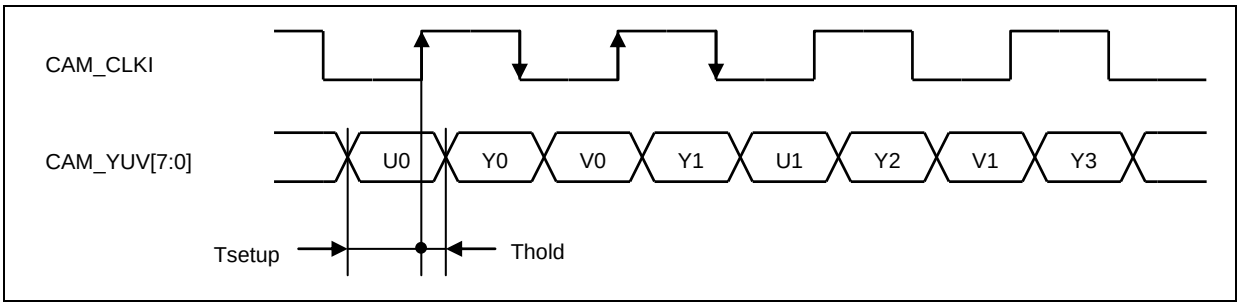
Name	R/W	Bit No.	After Reset	Function
Reserved	R	31:9	00_0000H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
QOSEN	R/W	8	0	Specifies whether to enable simple QoS. 0: Disable 1: Enable
QOSSET	R/W	7:0	00H	A QoS request is issued if the size of the vacant space in a buffer falls below the value specified in this field.

4. Description of Functions

4.1 Input Data Capture Timing

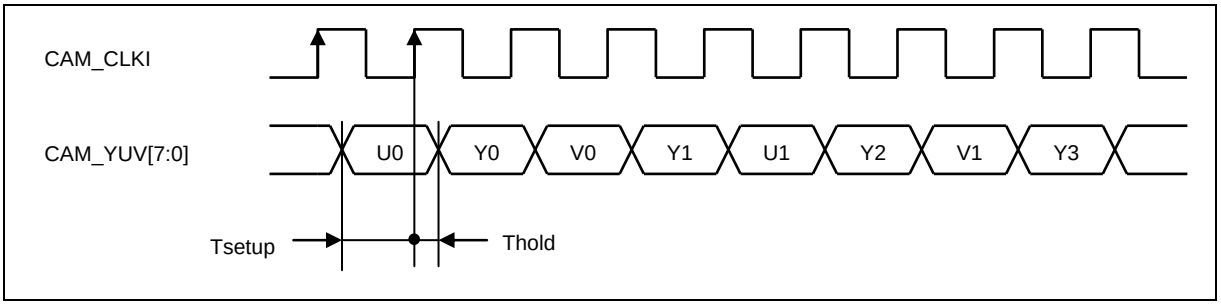
(1) Capture at rising and falling edges

Figure 4-1. Example of Capturing at Rising and Falling Edges



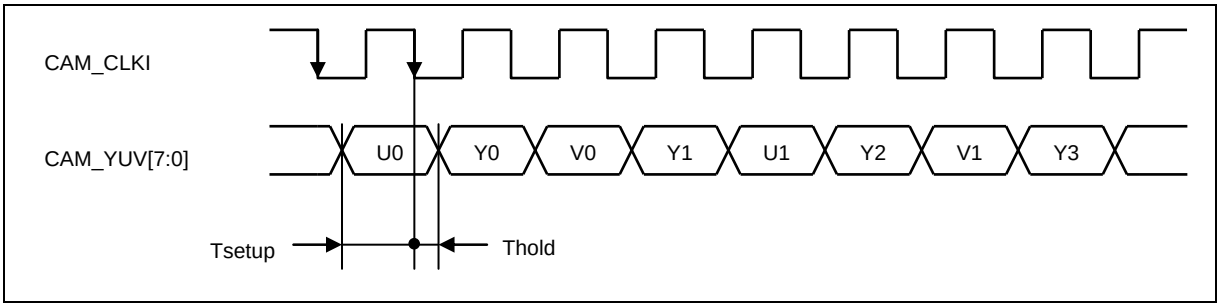
(2) Capture at rising edge

Figure 4-2. Example of Capturing at Rising Edge



(3) Capture at falling edge

Figure 4-3. Example of Capturing at Falling Edge

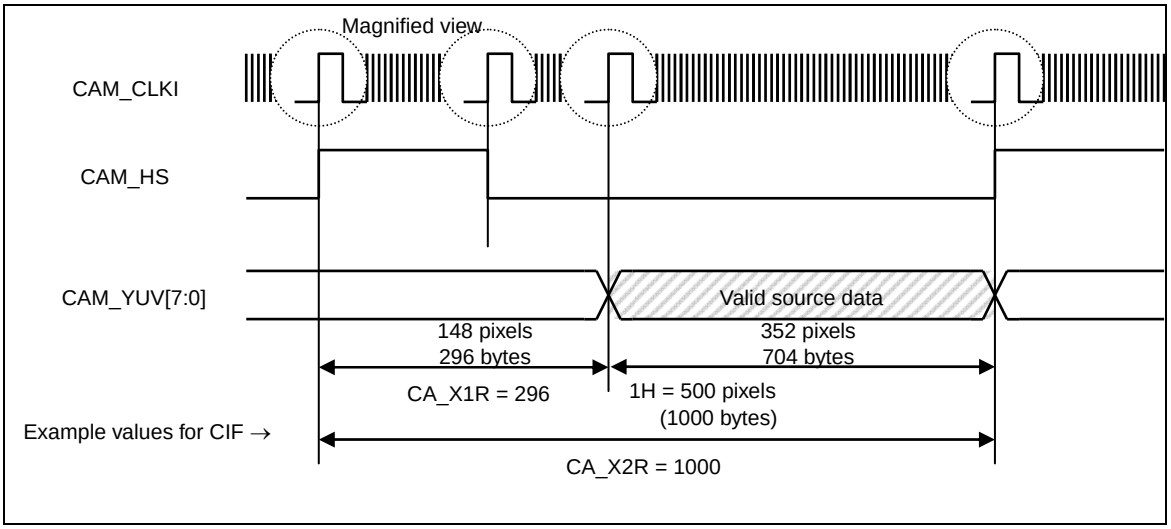


4.2 Horizontal/Vertical Synchronization Signal Sampling

(1) Horizontal synchronization signal sampling timing

The following figure shows an example of the horizontal synchronization signal sampling timing values for CIF (352H × 288V).

Figure 4-4. Horizontal Synchronization Signal Sampling Timing (If CAM_HS Has Positive Logic)

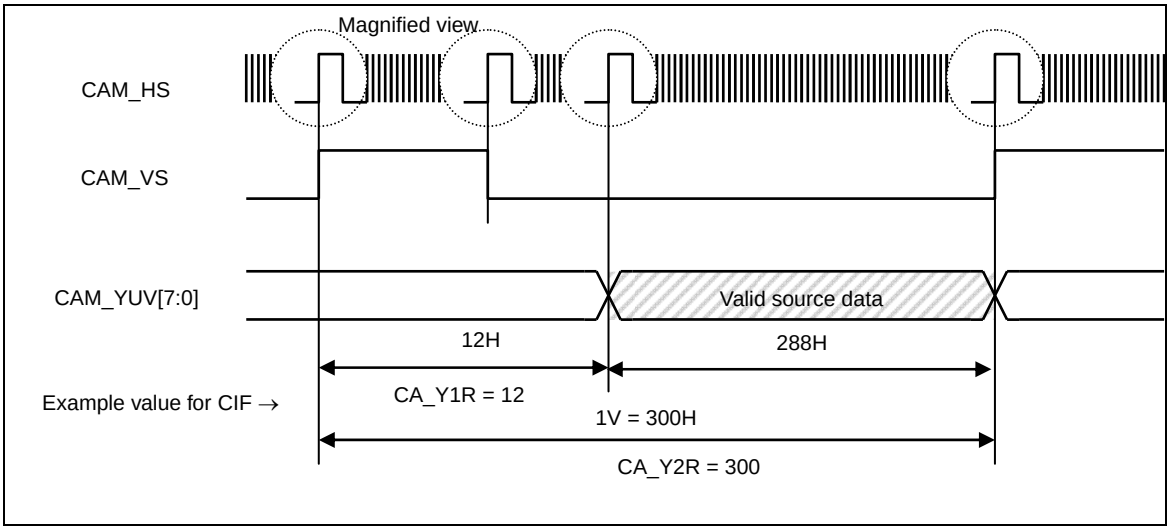


Caution Intervals for CAM_HS must be within the number of CAM_CLKI clocks × 8192. Synchronization at longer intervals is not supported.

(2) Vertical synchronization signal sampling timing

The following figure shows an example of the vertical synchronization signal sampling timing values for CIF (352H × 288V).

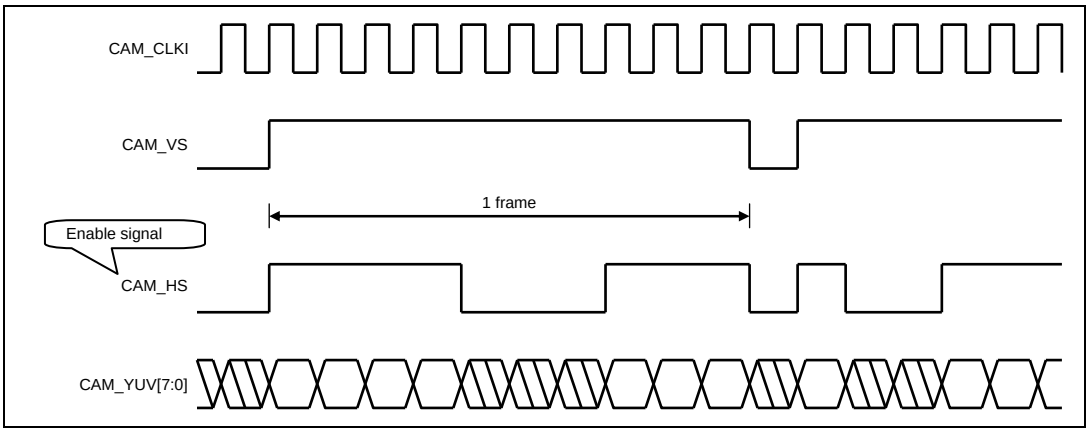
Figure 4-5. Vertical Synchronization Signal Sampling Timing (If CAM_VS Has Positive Logic)



4.3 Enable Signal Sampling

Connect the enable signal to the CAM_HS pin for enable sampling. The period during which the CAM_VS signal is asserted is recognized as one frame and data when the enable signal is valid is captured.

Figure 4-6. Enable Signal Sampling Timing

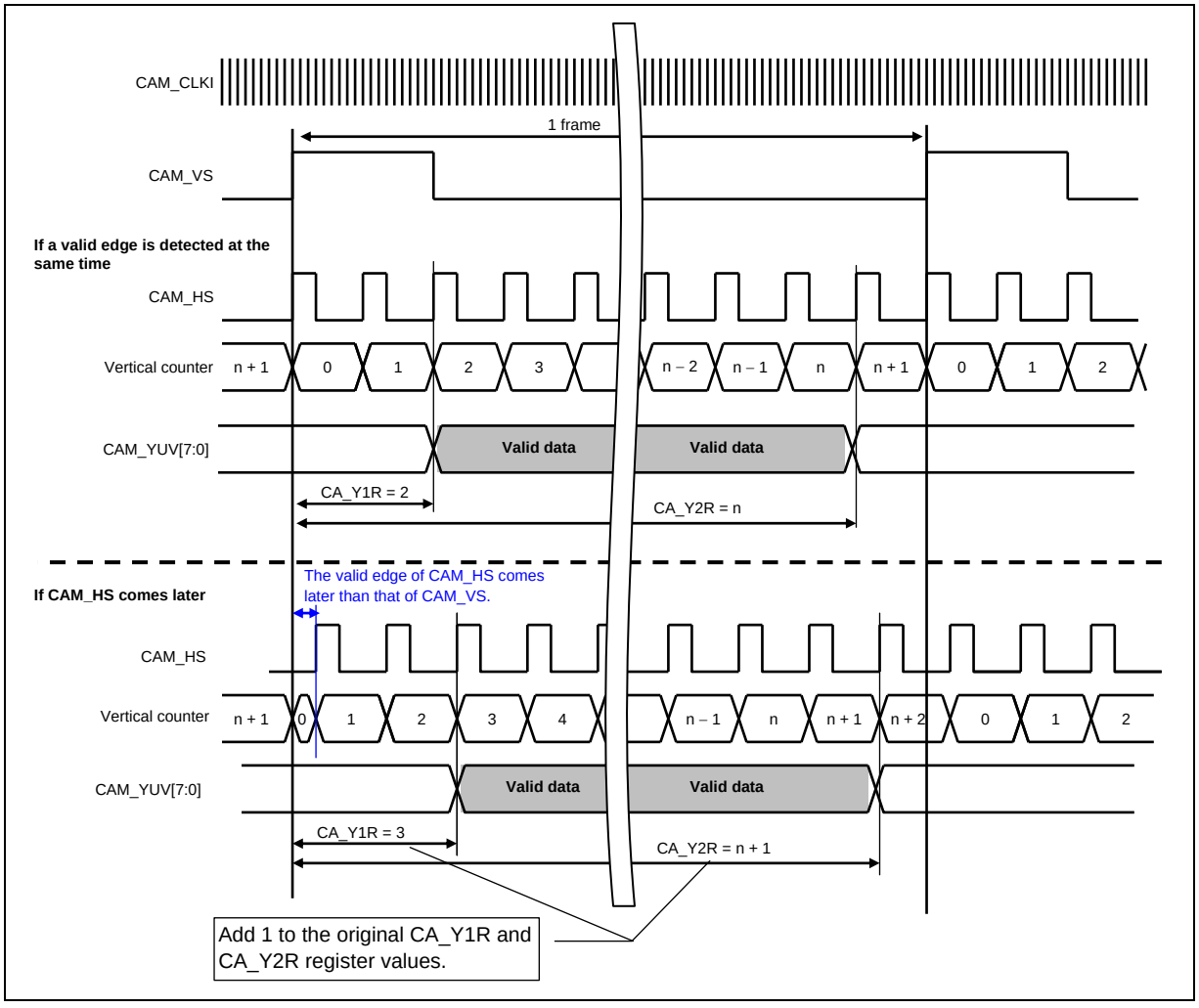


4.4 CAM_VS/CAM_HS Timing and CA_Y1R/CA_Y2R Values

The CAM module is designed assuming that the valid edge timing of CAM_VS and CAM_HS matches. If the valid edge of CAM_HS comes later than that of CAM_VS, the values of the CA_Y1R and CA_Y2R registers must be incremented by 1.

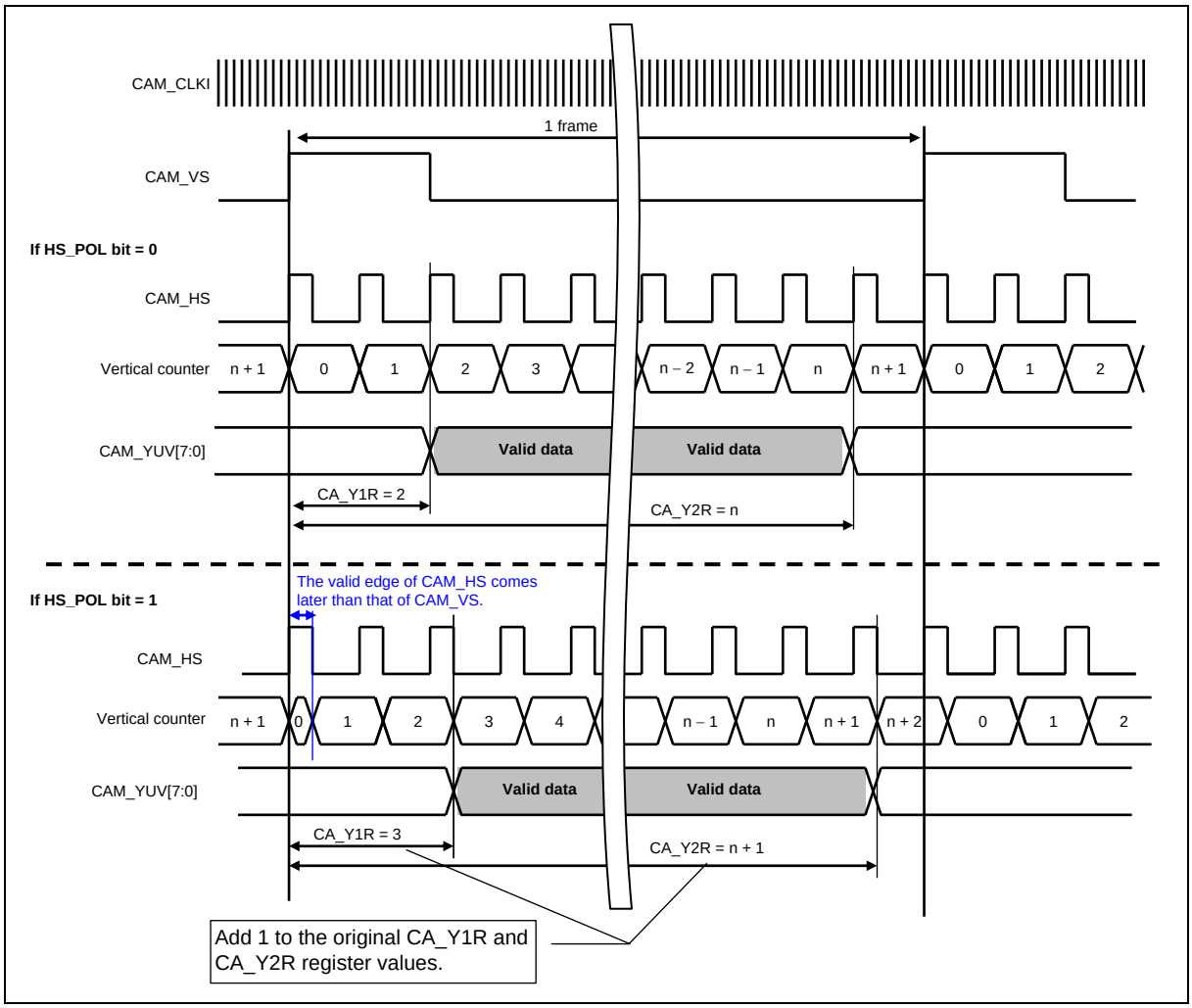
Figure 4-7 shows the relationship between the CAM_VS/CAM_HS input timing and the values specified by the CA_Y1R and CA_Y2R registers.

Figure 4-7. CAM_VS/CAM_HS Timing and CA_Y1R/CA_Y2R Values



If the HS_POL bit is set to 1 at the CAM_VS and CAM_HS input timing shown in Figure 4-8, add 1 to the CA_Y1R and CA_Y2R register values of when the HS_POL bit is set to 0.

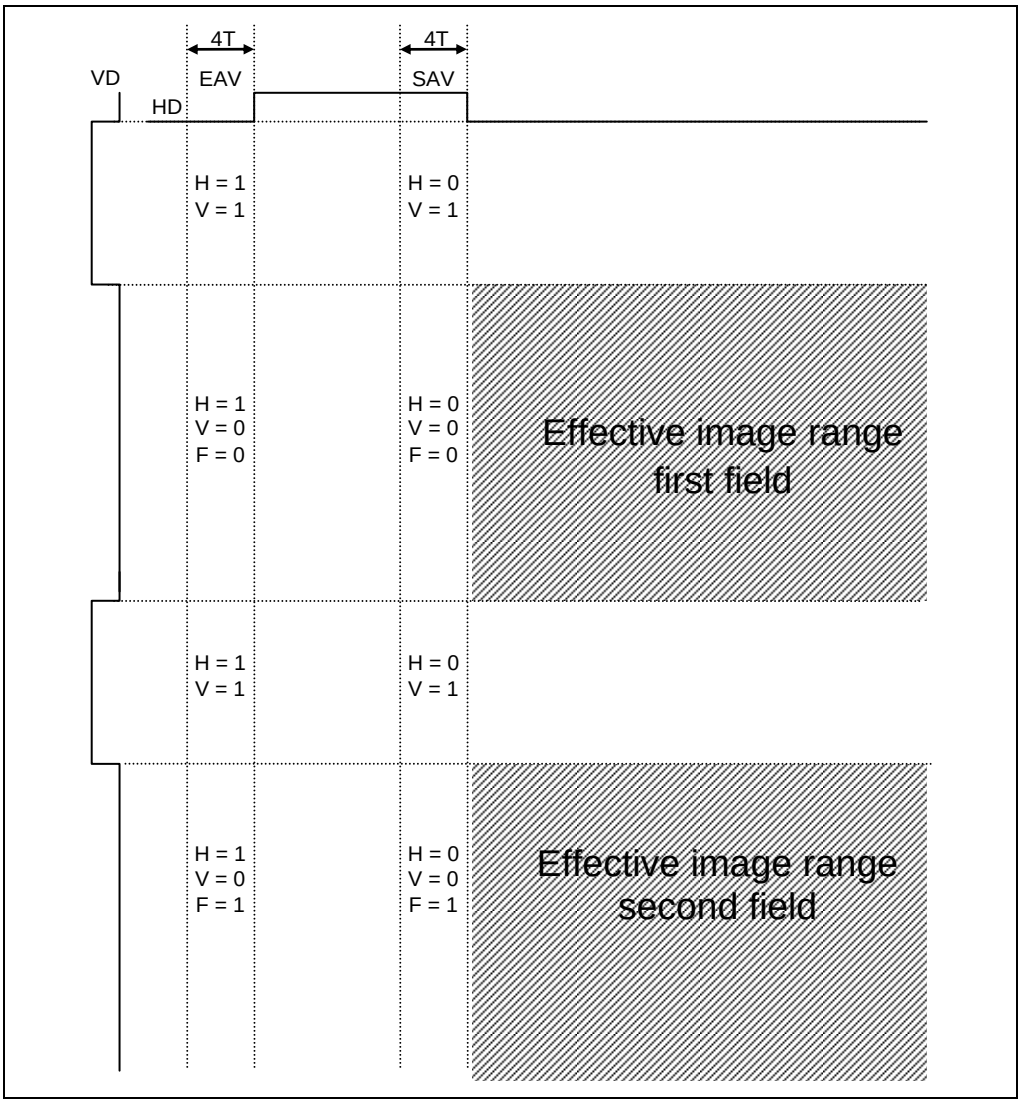
Figure 4-8. CAM_VS/CAM_HS Timing and CA_Y1R/CA_Y2R Values (If CAM_HS Has Negative Logic)



4.5 ITU-R BT.656 Encording

With ITU-R BT.656, a data field consists of the EAV and SAV fields indicating the synchronization timing. The ITU-R BT.656 encoding mode sets horizontal synchronization and vertical synchronization internally at the timing of the fourth word of the SAV and EAV fields. Figure 4-9 shows a conceptual diagram of the EAV and SAV fields and the synchronization signals.

Figure 4-9. ITU-R BT.656 Encoding Timing



The fields to be stored can be specified by using the 656MODE bit of the camera control register (CA_CSR). The 656MODE bit is valid only when the ITU-R BT.656 mode is selected by using the SYNCMODE bit.
Store operations listed in Table 4-1 can be specified by combinations of the transfer mode specification (MAINMODE) of the transfer control register (CA_DMACNT) and the transfer frame register (CA_FRAME).

Table 4-1. Field Store Operation Selected by Specifying 656MODE Bit

CA_CSR 656MODE Bit	CA_DMACNT MAINMODE Bit	CA_FRAME MAINFRM Bit	Field Store Operation
00	10 (Repeat transfer, double buffer)	Don't care	Starts storing from the first field. Stores the first field to the A frame and the second field to the B frame.
00	01 (Repeat transfer, fixed buffer)	00	Starts storing from the first field. Stores both the first and second fields to the A frame repeatedly.
01	10 (Repeat transfer, double buffer)	Don't care	Starts storing from the second field. Stores the second field to the A frame and the first field to the B frame.
01	01 (Repeat transfer, fixed buffer)	00	Starts storing from the second field. Stores both the first and second fields to the A frame repeatedly.
10	01 (Repeat transfer, fixed buffer)	00	Stores only the first field to the A frame (main frame setting)
10	00 (Single transfer)	Don't care	Prohibited[Note].
11	01 (Repeat transfer, fixed buffer)	10	Stores only the second field to the B frame (main frame setting).
11	00 (Single transfer)	Don't care	Prohibited[Note].

Note In the ITU-R BT.656 mode, specifying single transfer by using the MAINMODE bit is prohibited. To input an image of one frame, specify the repeat transfer mode and stop processing after a transfer completion interrupt has been issued. Figure 4-12 shows storage when one frame is input.

Figure 4-10. Field Data and Storage Frame According to Specification by 656MODE Bit

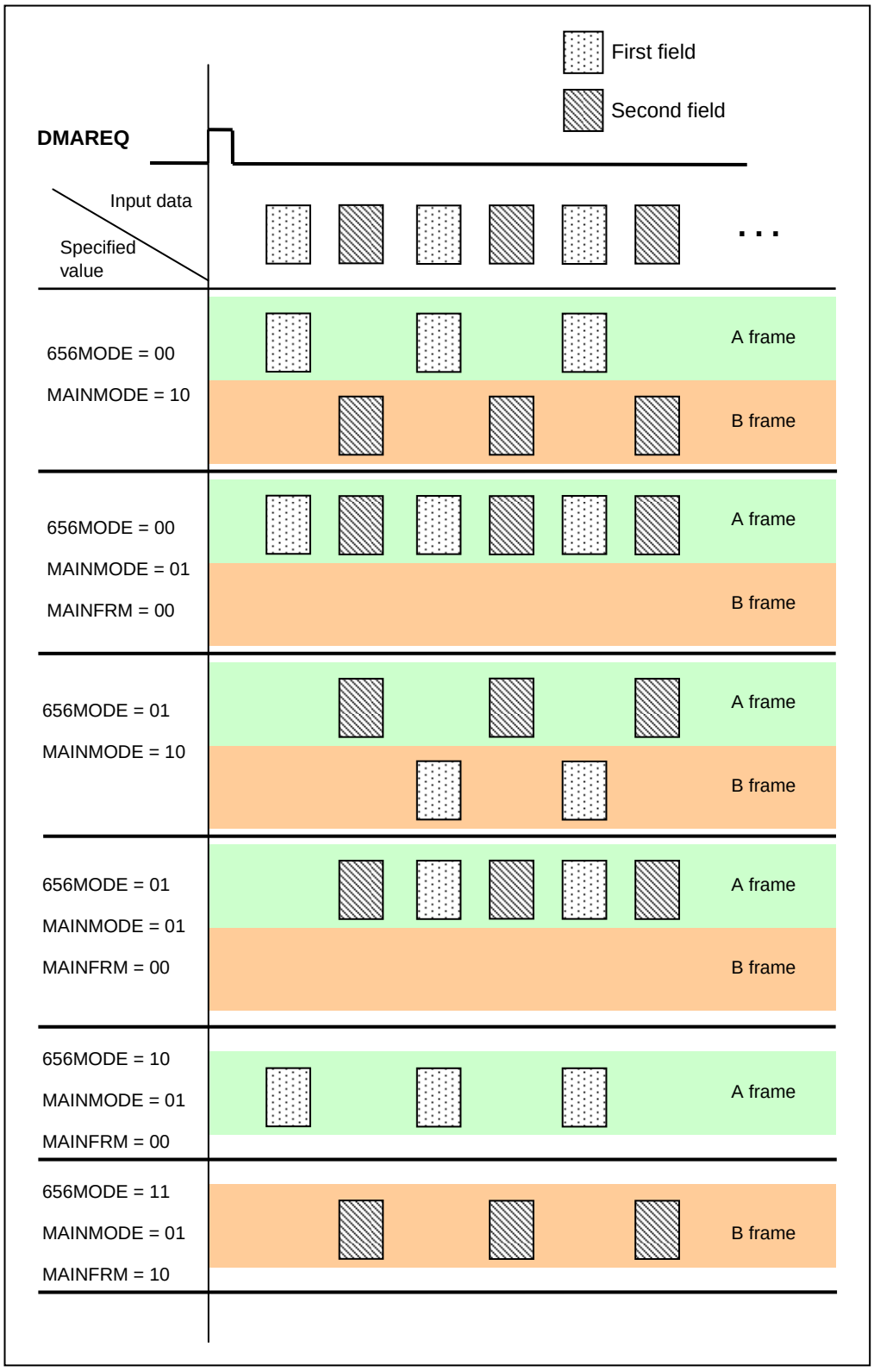


Figure 4-11 shows the timing of a vertical synchronization interrupt and a transfer completion interrupt for each 656MODE bit setting in the ITU-R BT.656 mode.
A vertical synchronization interrupt is output at the beginning of the data (position at which this signal is detected), in frame units. Two-stage registers are then updated when a vertical synchronization interrupt is issued. When data transfer ends, a transfer completion interrupt is issued in field units.

Figure 4-11. Timing of Vertical Synchronization Interrupt and Transfer Completion Interrupt According to Specification by 656MODE Bit

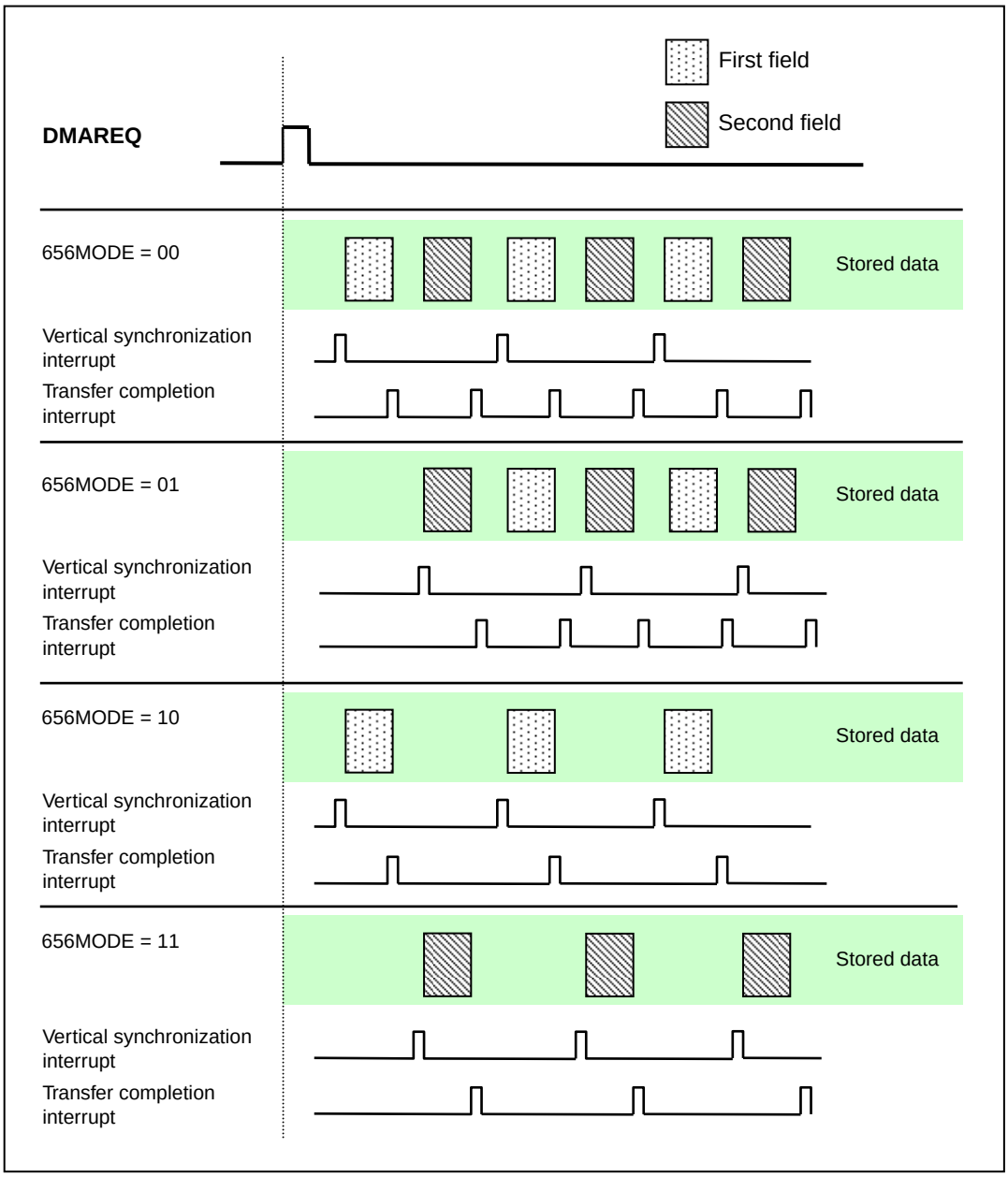
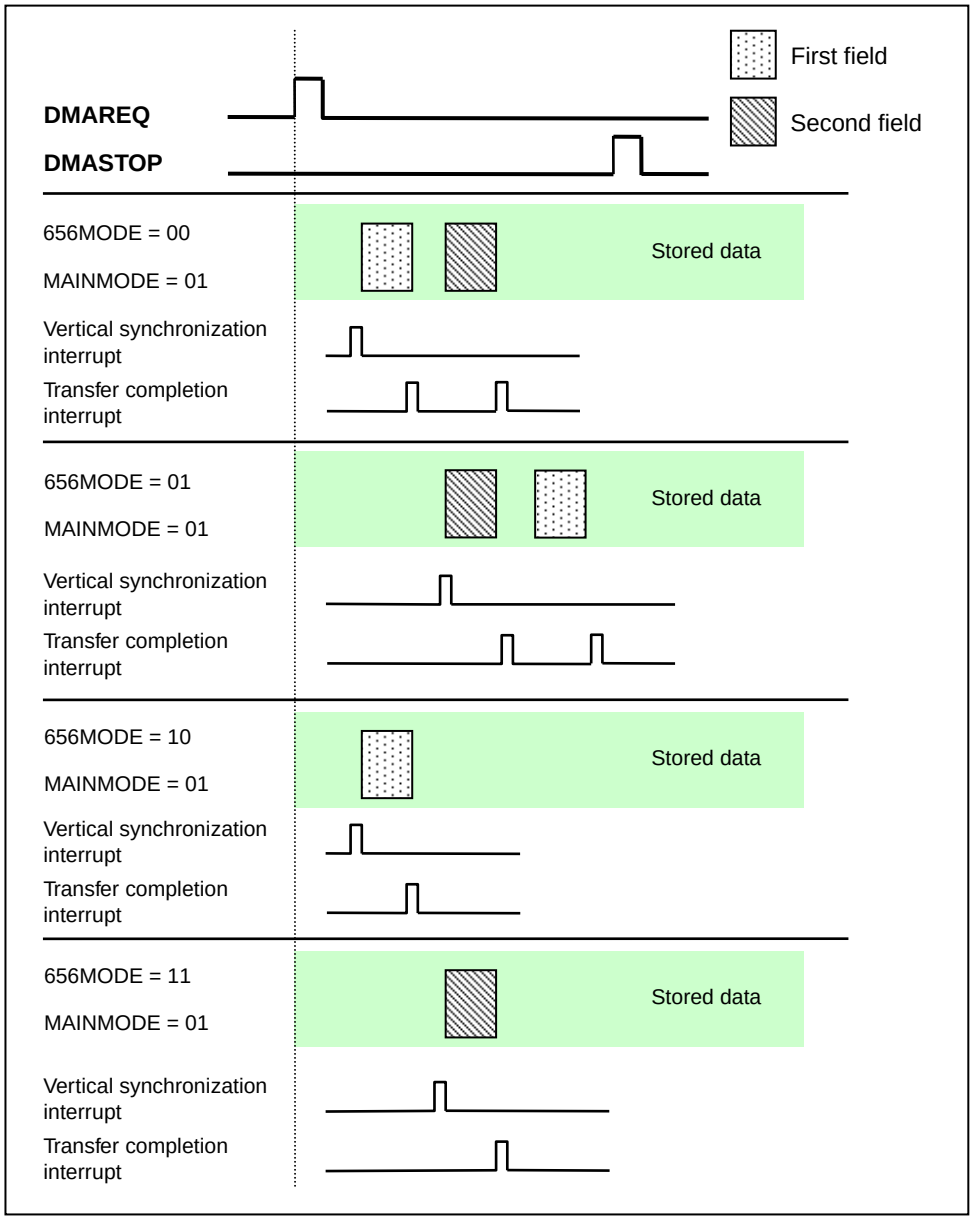


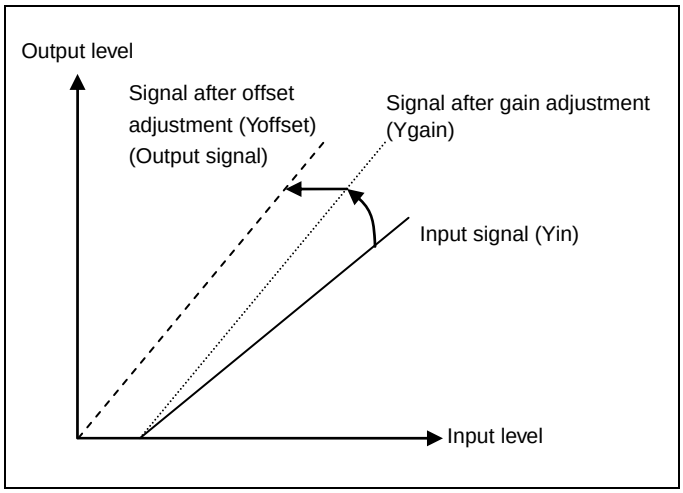
Figure 4-12. Data Storage During 1-Frame Transfer



4.6 Level Adjustment

The gain and offset can be adjusted for the input data level. The gain of data input via the CAM interface is first adjusted, and then the offset value of the data after gain adjustment is performed. Figure 4-13 shows the concept of this processing.

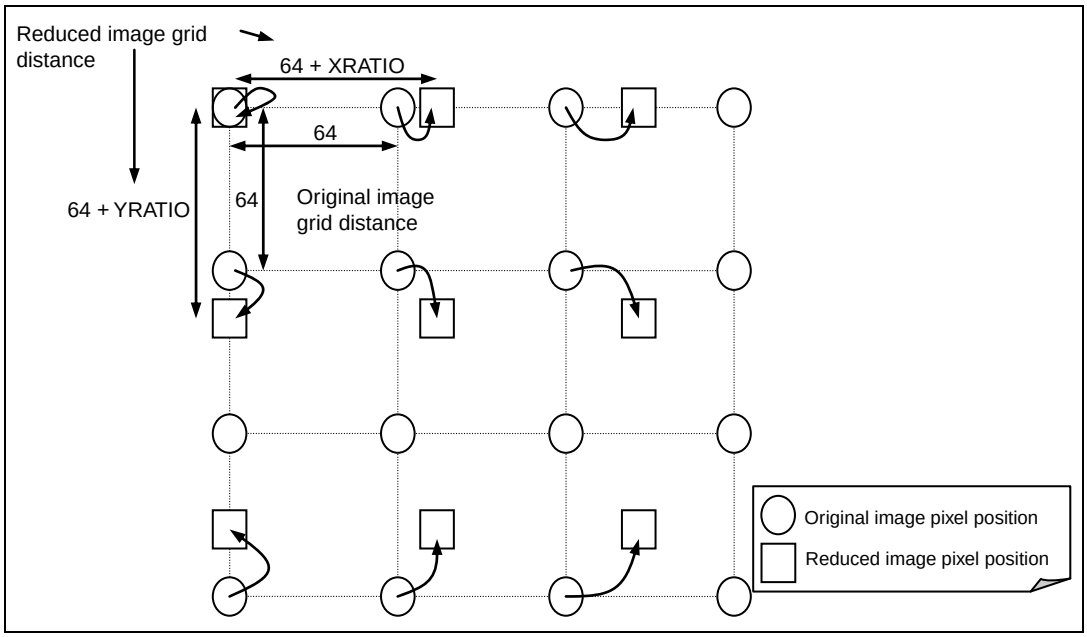
Figure 4-13. Level Adjustment



4.7 Reduction Method

The reduction method used is nearest-neighbor sampling, which copies the nearest neighbor pixels of an original image to the pixel positions of a reduced image. As shown in Figure 4-14, a reduced image is generated by finding the relationship between the pixels of the original image and the reduced image, using the method described below. The pixel-to-pixel distance of an original image is defined to be 64, and a value obtained by adding 64 to the value of the XRATIO/YRATIO register is defined to be the pixel-to-pixel distance of the reduced image, so that the coordinate positions obtained by multiplying this distance by integers function as the pixels of a reduced image. The reduced image is generated by copying the nearest neighbor pixels of an original image to the coordinate positions of the reduced image. Accordingly, the weight center of the pixels of the reduced image shifts by up to 1/2, but the vividness is preserved because the original image is not processed.

Figure 4-14. Reduced Image Sampling



Calculate the value to be set to XRATIO as follows.

$$XRATIO = \frac{64 \times \text{Input size}}{\text{Output size}} - 64 \text{ (The fractional digits are discarded.)}$$

Example When capturing an image of 320 × 240 pixels and resizing it to 160 × 120 pixels

$$XRATIO = \frac{64 \times 320}{160} - 64 = 128 - 64 = 64$$

$$YRATIO = \frac{64 \times 240}{120} - 64 = 128 - 64 = 64$$

4.8 Data Transfer range Specification

The register setting for the number of transfer pixels varies between normal transfer and resize transfer.
Figure 4-15 shows the relationship between the range of effective data transferred via CAM and the range of data transferred to memory. The following explanation uses the CAM_VS/CAM_HS signal sampling mode as an example, but the setting is the same for the enable signal sampling mode.

4.8.1 Horizontal transfer range

Normal transfer: The number of transfer pixels varies as follows, depending on the value of the clock edge select bit (CLK_EDGE) of the camera control register (CA_CSR).
Rising or falling edge sampling: {(CA_X2R – CA_X1R) / 2} pixels
Rising and falling edge sampling: (CA_X2R – CA_X1R) pixels

Resize transfer: The number of pixels specified by the CA_DMAXCOUNT_MAIN register is used.
Specify a value satisfying the following conditional expressions.
Rising or falling edge sampling:

$$DMAXCOUNT\_MAIN \leq \{(CA\_X2R - CA\_X1R) / 2\} \times \{64 / (64 + XRATIO\_MAIN)\}$$

Rising and falling edge sampling:

$$DMAXCOUNT\_MAIN \leq (CA\_X2R - CA\_X1R) \times \{64 / (64 + XRATIO\_MAIN)\}$$

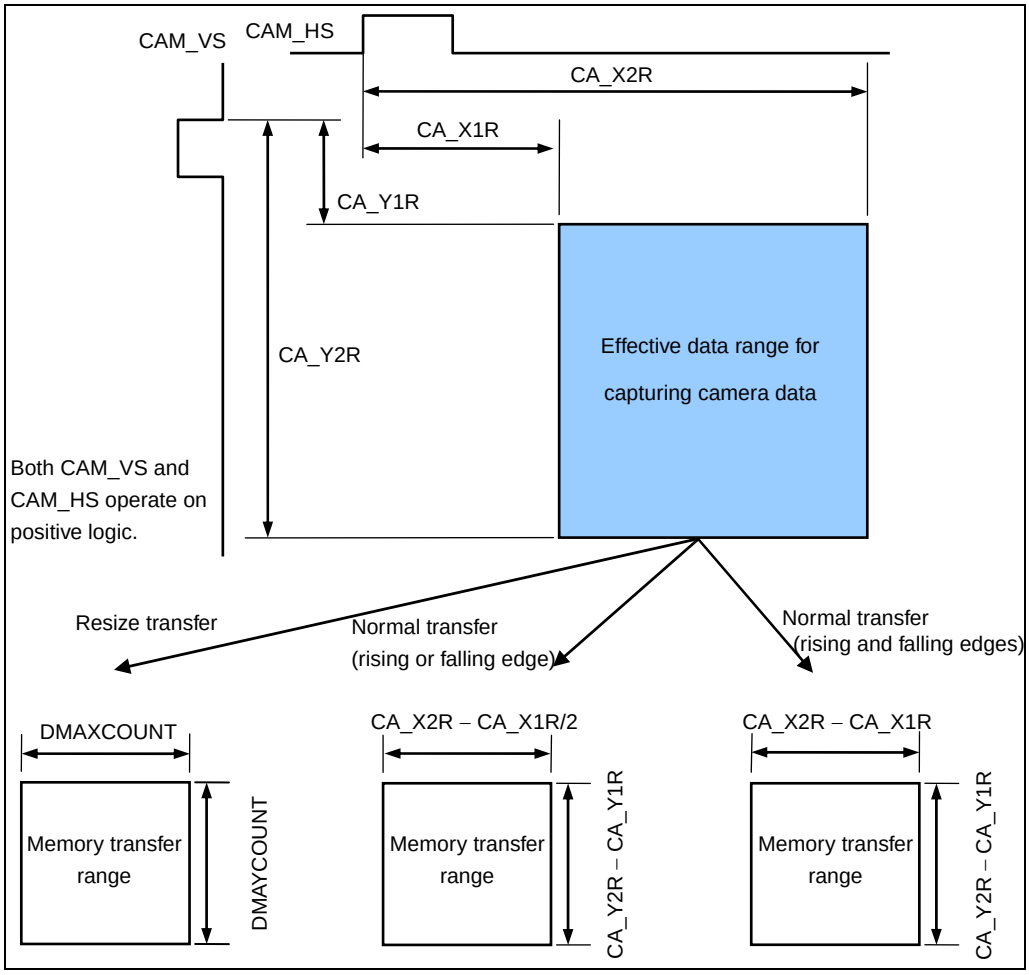
4.8.2 Vertical transfer range

Normal transfer: (CA_Y2R – CA_Y1R)

Resize transfer: The number of pixels specified by the DMAYCOUNT_MAIN register is used.
Specify a value satisfying the following conditional equations.

$$DMAYCOUNT\_MAIN \leq (CA\_Y2R - CA\_Y1R) \times \{64 / (64 + YRATIO\_MAIN)\}$$

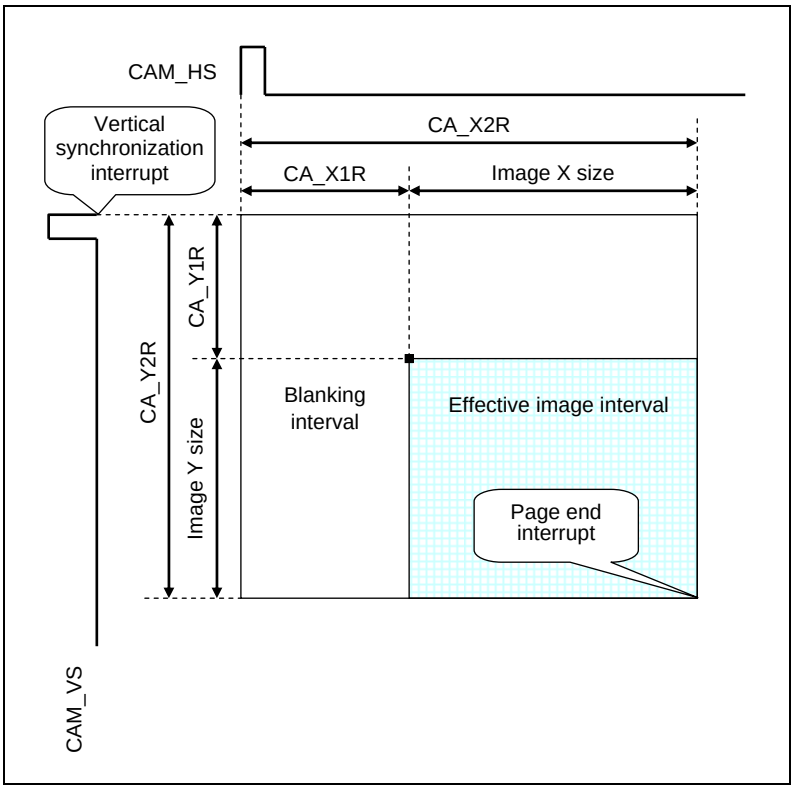
Figure 4-15. Data Transfer Range



4.9 Restriction on Data Transfer Range Values

4.9.1 Vertical/horizontal synchronization signal sampling

Figure 4-16. CAM_VS/CAM_HS Signal Sampling



Set up the registers as follows.

Register Name	Condition
CA_Y2R	CA_Y2R = Image Y size + CA_Y1R
CA_Y1R	0 ≤ CA_Y1R
CA_X2R	CA_X2R = (Image X size × 2) + CA_X1R (rising or falling edge)
	CA_X2R = Image X size + CA_X1R (rising and falling edges)
CA_X1R	0 ≤ CA_X1R

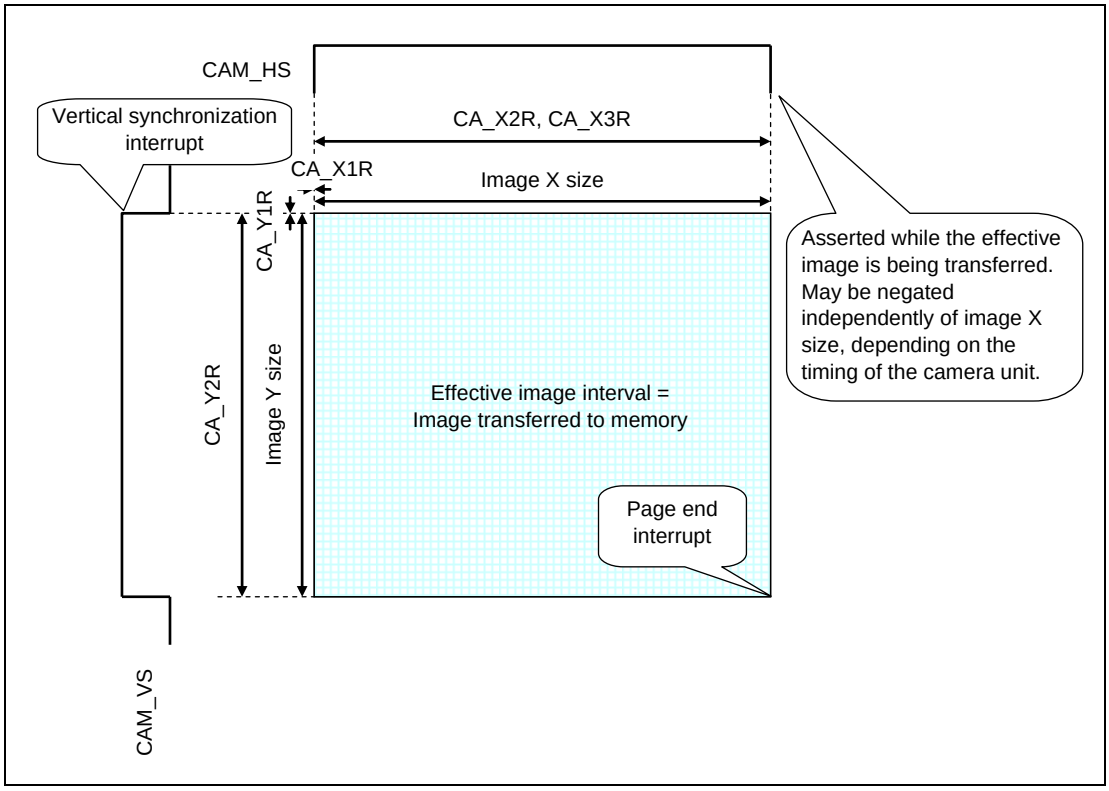
Caution The value set to CA_X3R is ignored.

4.9.2 Enable signal sampling

(1) Normal

All the effective image data input via the CAM interface is captured and written to the frame memory.

Figure 4-17. Enable Signal Sampling (Normal)



Set up the registers as follows.

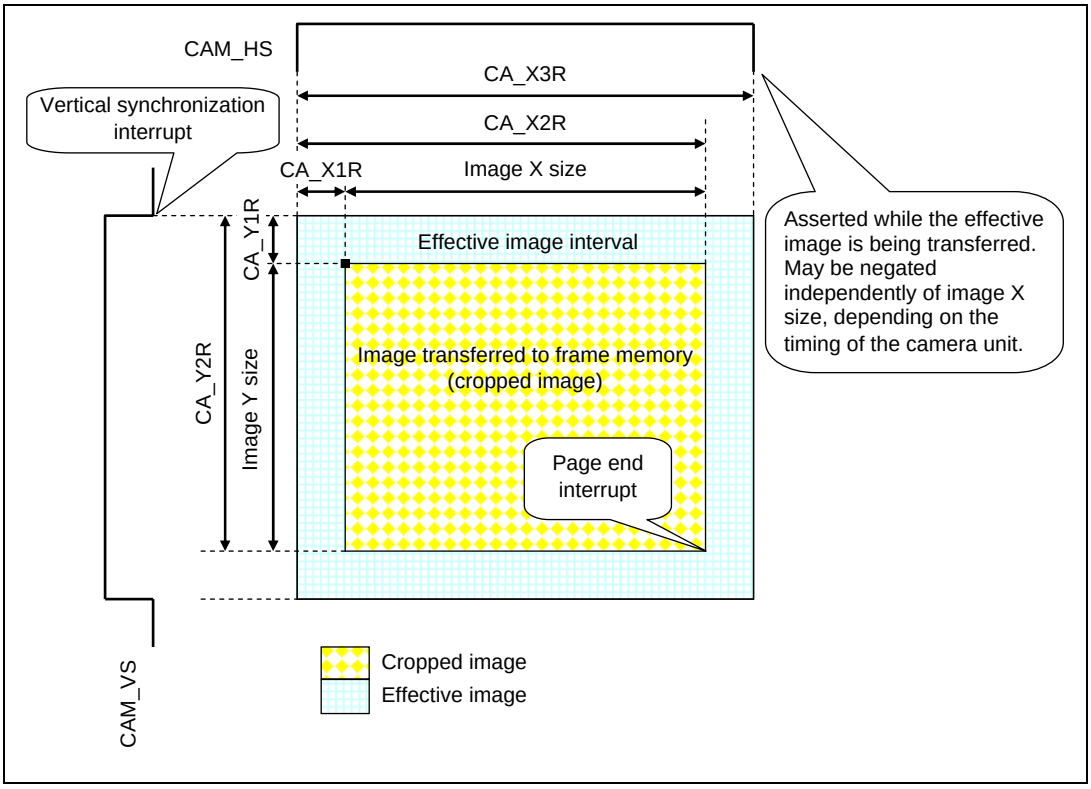
Register Name	Condition
CA_Y2R	CA_Y2R = Image Y size
CA_Y1R	CA_Y1R = 0
CA_X3R	CA_X3R = Image X size × 2 (rising or falling edge)
	CA_X3R = Image X size (rising and falling edges)
CA_X2R	CA_X2R = Image X size × 2 (rising or falling edge)
	CA_X2R = Image X size (rising and falling edges)
CA_X1R	CA_X1R = 0

Caution Be sure to set CA_X3R.

(2) Cropping

Any rectangle can be cropped from the effective image data input via the CAM interface and can be written to the frame memory.

Figure 4-18. Enable Signal Sampling (Cropping)



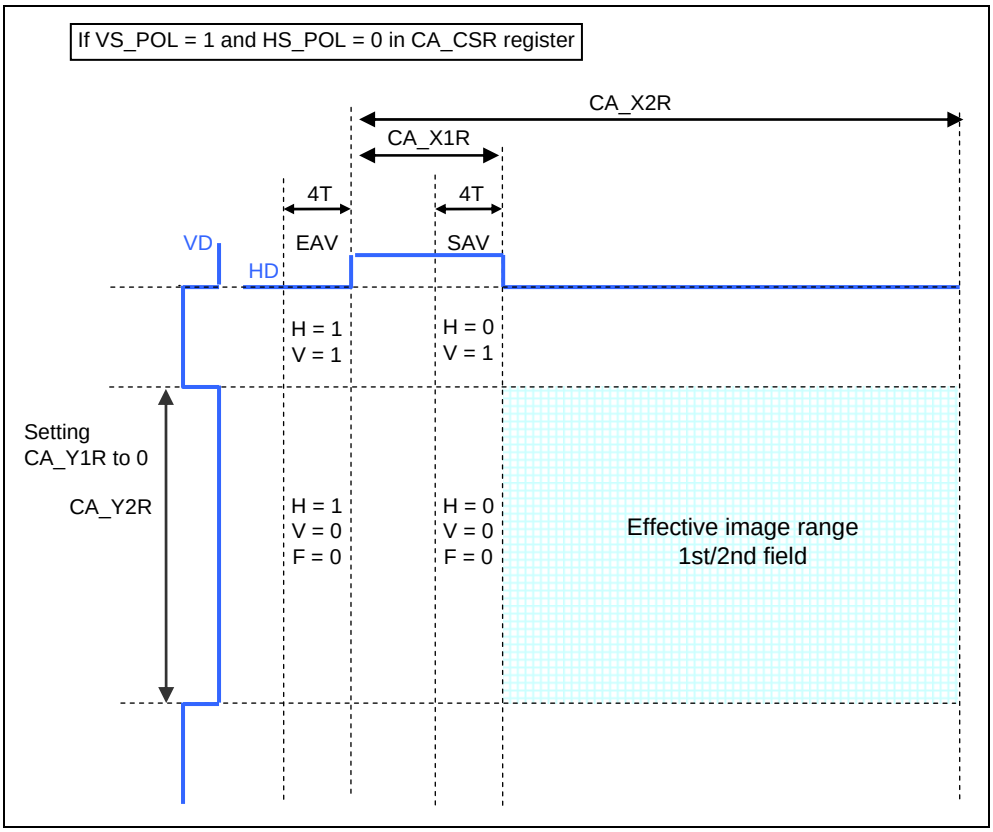
Set up the registers as follows.

Register Name	Condition
CA_Y2R	CA_Y2R = Cropped image Y size + CA_Y1R
CA_Y1R	CA_Y1R = Cropping starting line
CA_X3R	CA_X3R = Effective image X size × 2 (rising or falling edge)
	CA_X3R = Effective image X size (rising and falling edges)
CA_X2R	CA_X2R = Cropped image X size × 2 (rising or falling edge)
	CA_X2R = Cropped image X size (rising and falling edges)
CA_X1R	CA_X1R = Cropping starting pixel × 2 (rising or falling edge) CA_X1R = Cropping starting pixel (rising and falling edges)

Caution Be sure to set CA_X3R.

(3) ITU-R BT.656 signal sampling

Figure 4-19. Signal Sampling in ITU-R BT.656 Mode



To capture NTSC/PAL REC656 inputs, set VS_POL to 1 and HS_POL to 0 in the CA_CSR register, and specify the values shown in the following table for the effective image range setting registers.

Register	Register Values	
	NTSC	PAL
CA_Y2R	243	288
CA_Y1R	0	0
CA_X2R	1712	1724
CA_X1R	272	284

If values other than above need to be specified, follow the criterion shown on the following page.

It is recommended to set VS_POL to 1 and HS_POL to 0 in the CA_CSR register. Set CA_Y1R to 0, and then specify the effective image range by using the CA_X1R, CA_X2R, and CA_Y2R registers (see **Figure 4-19**).

Register	Condition
CA_Y2R	CA_Y2R = Image Y size + CA_Y1R CA_Y2R < Total number of lines in one frame/2[Note]
CA_Y1R	0 ≤ CA_Y1R (vertical blanking interval)
CA_X2R	CA_X2R = (Image X size × 2) + CA_X1R (rising or falling edge)
CA_X1R	0 ≤ CA_X1R (horizontal blanking interval)

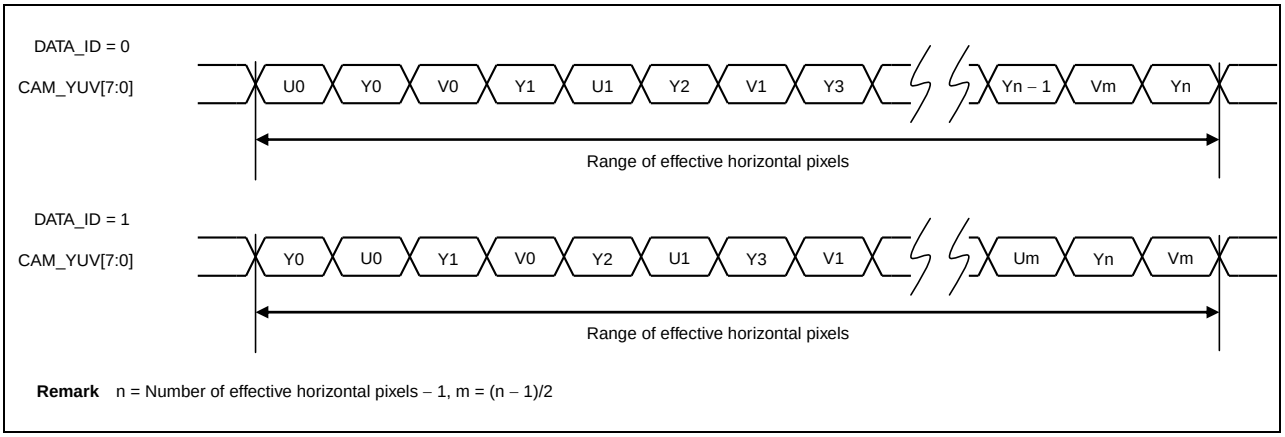
Note The same values must be specified for the CA_Y1R, CA_Y2R, CA_X1R, and CA_X2R registers.
Cases where the image size in the 1st and 2nd fields differs are not supported.
The value set to CA_X3R is ignored.
If HS_POL is set to 1, add 1 to the values specified for the CA_Y1R and CA_Y2R registers while HS_POL is set to 0 and specify the obtained values for the CA_Y1R and CA_Y2R registers.

4.10 Data Format

4.10.1 Camera

Image data can be input from a camera in the two different orders, specified by setting the DATA_ID bit of the CA_CSR register.
Figure 4-20 shows the image data sequence when the DATA_ID bit is set to 0. Image data is output from a camera in the order of Y0, V, and Y1, starting with U0. If the DATA_ID bit is set to 1, image data is output from a camera in the order of U, Y1, and V, starting with Y0.

Figure 4-20. Camera Data Format



Remark n = Number of effective horizontal pixels – 1, m = (n – 1)/2

4.10.2 Memory mapping

(1) YUV420/422 Semi-Planar mode

Image data input from a camera is transferred to separate areas Y and UV in memory (these areas are respectively referred to as the Y plane and UV plane in the specification). Data is transferred to memory in 32-bit units. The endianness can be specified for the higher and lower 16 bits by setting the Y_UV_OD_ENDIAN bit of the CA_CSR register. The higher and lower bytes can be swapped. Figure 4-21 shows the memory format in big endian mode and Figure 4-22 shows the memory format in little endian mode.

Figure 4-21. Memory Format (Big Endian)

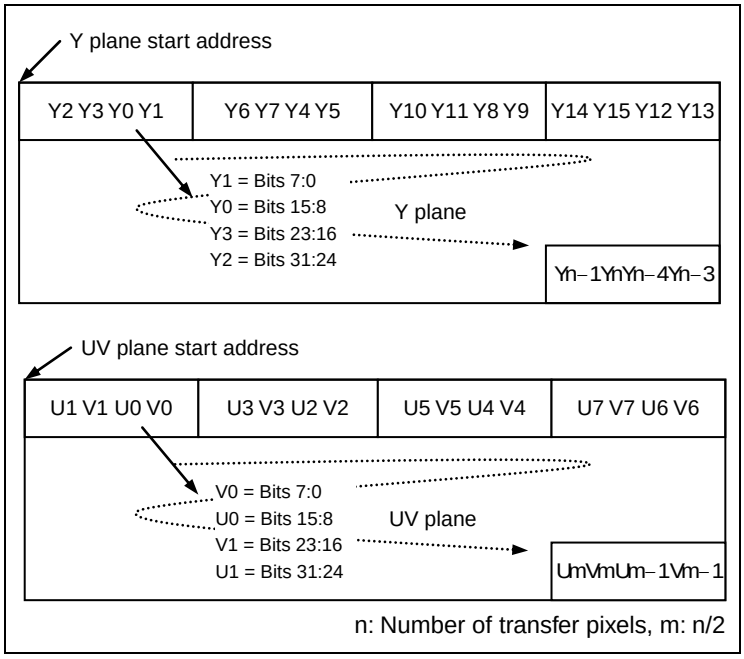
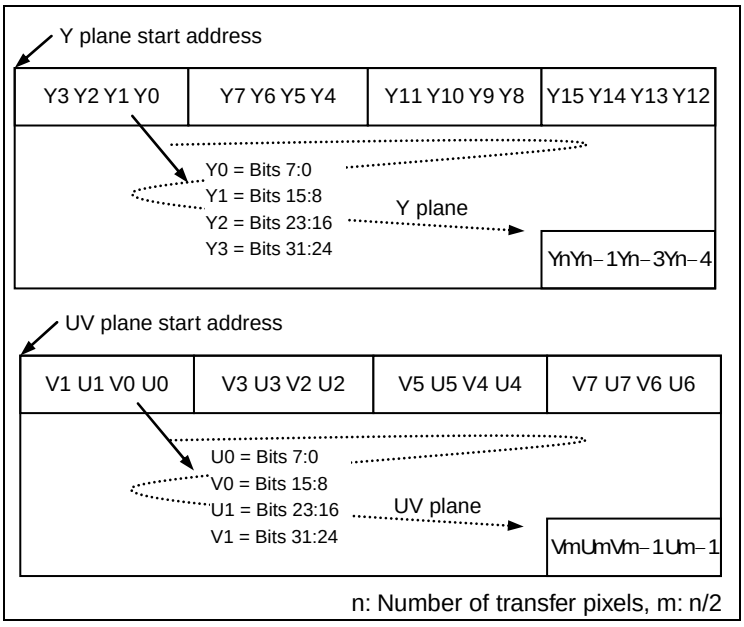


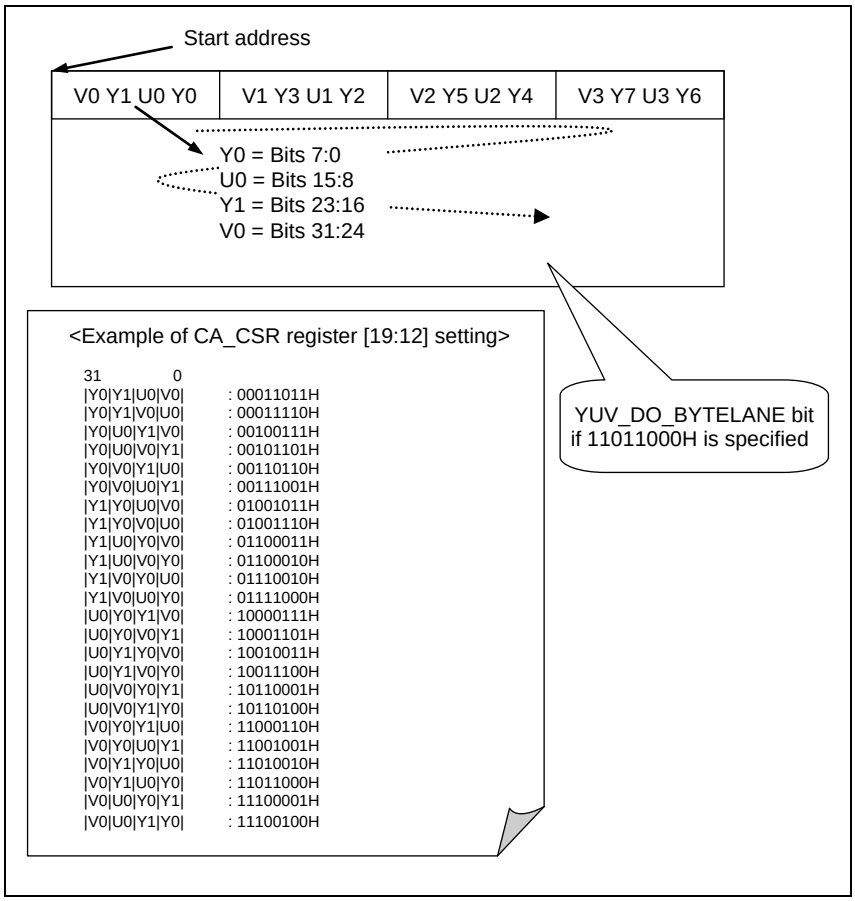
Figure 4-22. Memory Format (Little Endian)



(2) YUV422 Interleave mode

In this mode, image data input from a camera is transferred to memory with Y0Y1U0V0 components (2 pixels) as a set. Data is transferred to memory in 32-bit units, and the output byte lane of each component can be specified by using the CA_OD_BYTELANE register. Figure 4-23 shows a setting example.
Specify the transfer address by using the CA_YPLANE_A/B registers (Y plane). Values specified by the CA_UVPLANE_A/B register (UV plane) are ignored.

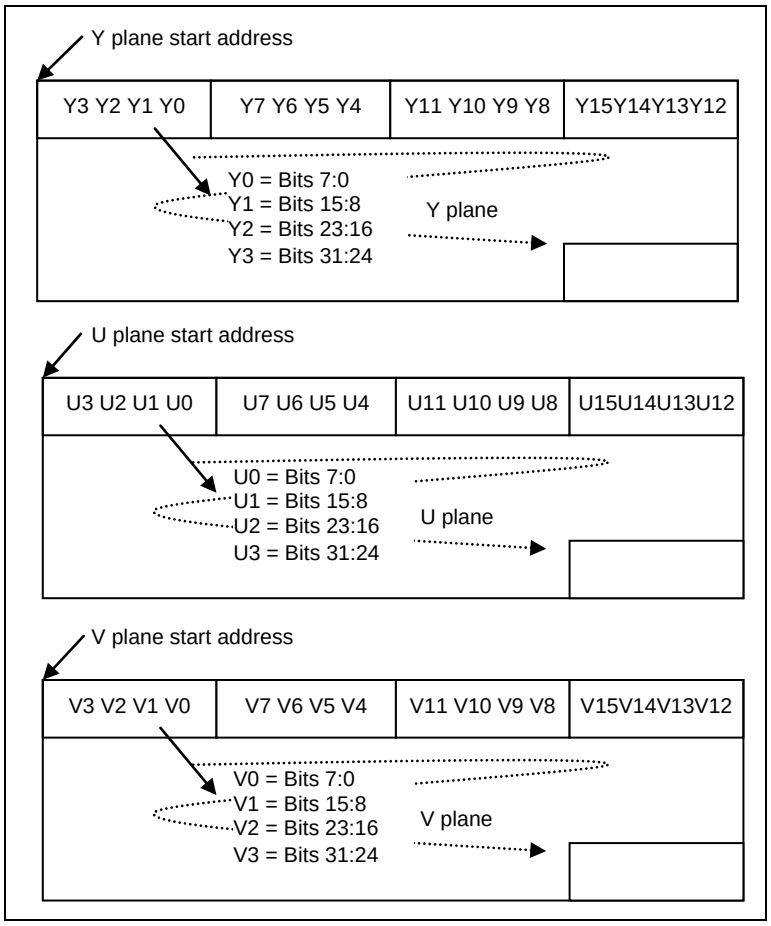
Figure 4-23. Example of YUV_OD_BYTELANE Setting



(3) YUV420/422 Planar mode

Image data input from a camera is transferred to separate areas Y, U, and V in memory (these areas are respectively referred to as the Y plane, U plane and V plane in the specification). Data is transferred to memory in 32-bit units, and the output byte lane of each component can be specified by using the CA_OD_BYTELANE2 register. Figure 4-24 shows the memory format.

Figure 4-24. YUV 420/422 Planar Memory Format

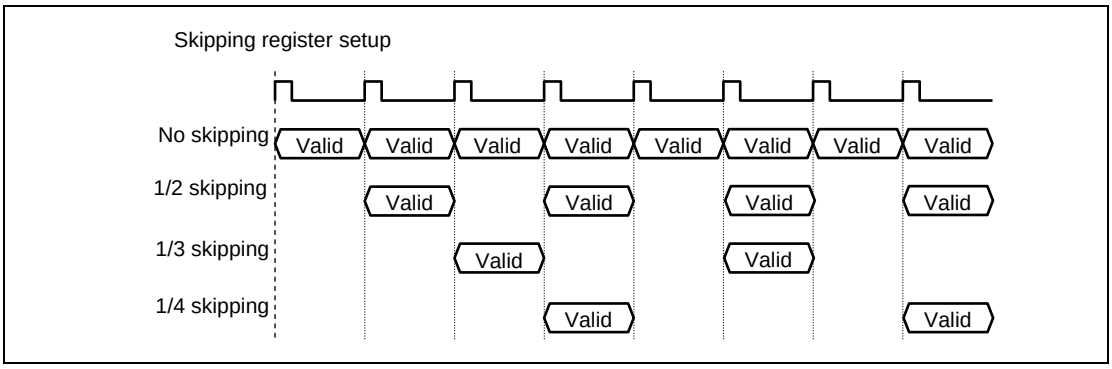


4.11 Transfer Processing

4.11.1 Frame skipping

The frame skipping bit of the transfer control register is used to set skipping of image data frames input from a camera. Figure 4-25 shows the relationship between skipping and effective transfer frames. Frame skipping is executed from the frame specified by the corresponding register.

Figure 4-25. Frame Skipping

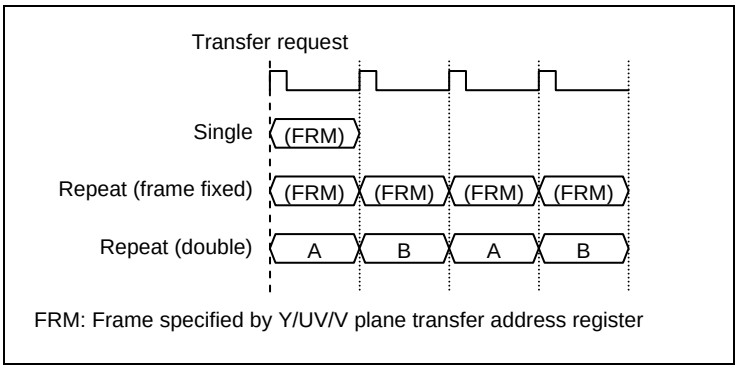


4.11.2 Transfer mode

The transfer mode bit of the transfer control register is used to specify the method of switching a transfer destination frame. Figure 4-26 shows the relationship between the transfer modes and the transfer destination frame. This figure shows the operations performed when no skipping is specified. If a skipping mode is specified, the transfer destination frame is switched for frames after skipping.

- Single transfer: Only one frame is transferred to a specified frame.
- Repeat transfer (frame fixed): Transfer to a specified frame is repeated.
- Repeat transfer (double): Transfer to the A and B frames is repeated alternately.

Figure 4-26. Transfer Mode

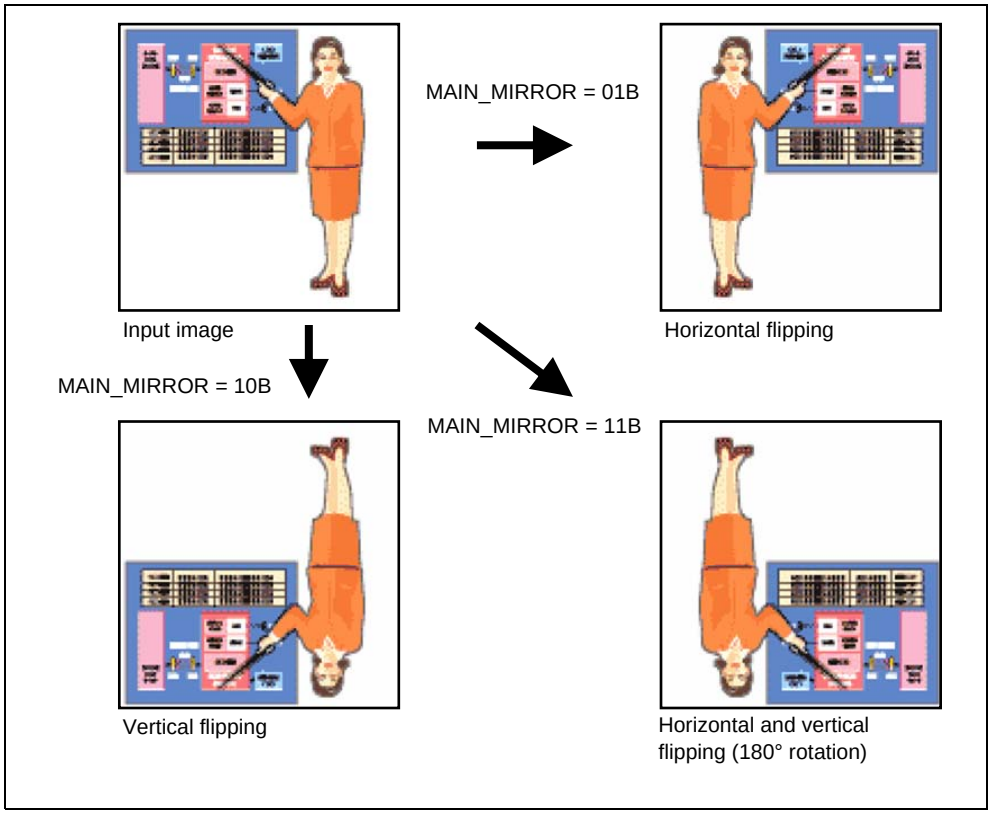


Caution When performing a repeat transfer (double), reset CAM immediately before transfer.

4.11.3 Horizontal/vertical flip control

The images can be flipped during DMA transfer by using the horizontal/vertical flip control register.
When flip control is performed, the frame memory area does not differ from the area used when flip control is not performed.

Figure 4-27. Flip Control



4.12 Frame Interval

The operation will not be performed correctly if the frame interval is too short. Make sure that the frame interval is sufficiently long.

If the register setting enable timing (CA_CSR) is the rising edge and if CAM_VS of the next frame will rise before transfer of one frame to the frame memory is completed, the register setting of the next frame at that point is enabled and the operation cannot be correctly performed.

Similarly, if the register setting enable timing (CA_CSR) is the falling edge, make sure that CAM_VS of the next frame does not fall before transfer of one frame to the frame memory is completed.

Figure 4-28. Frame Interval (Register Setting Enable Timing: Rising Edge)

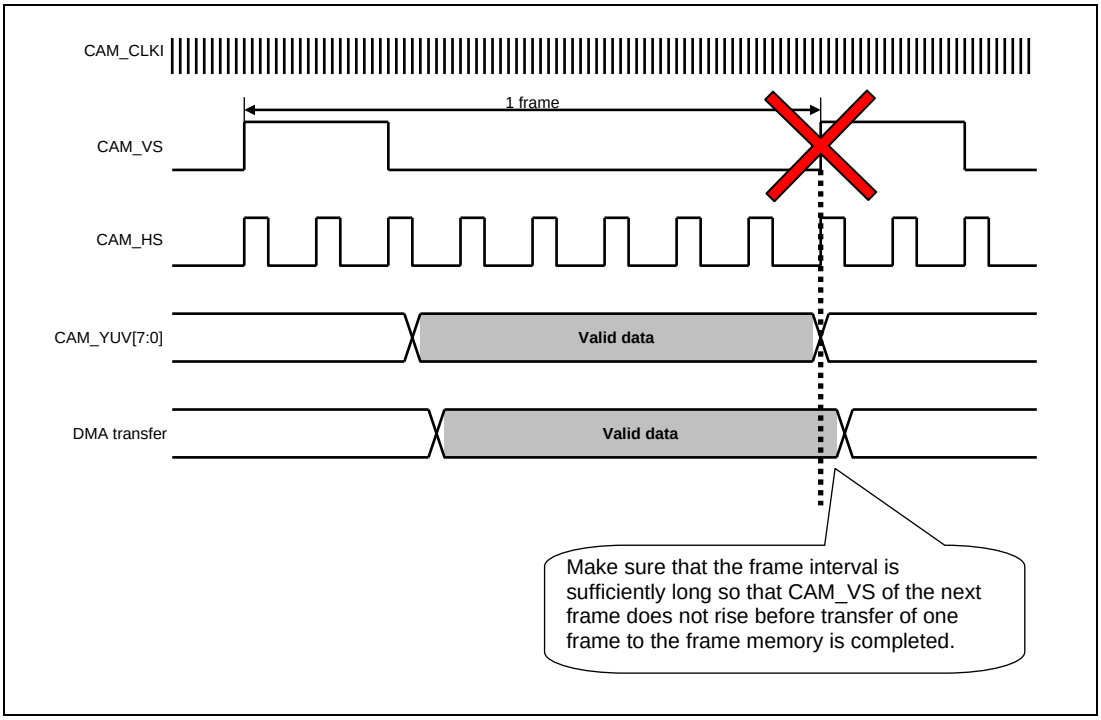
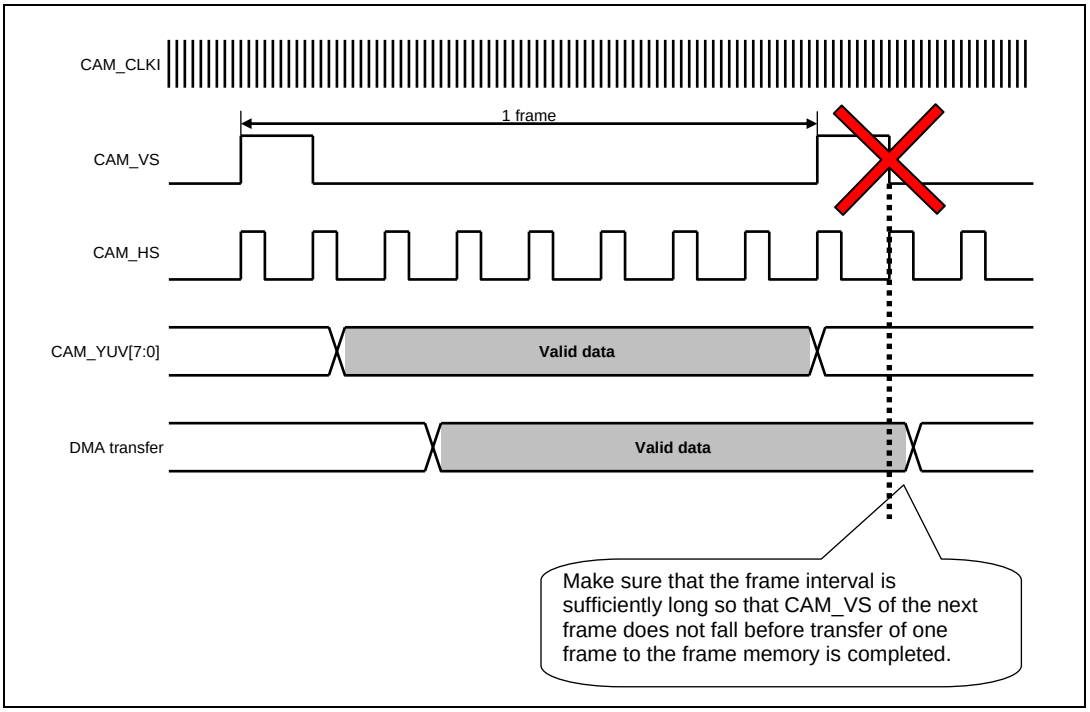


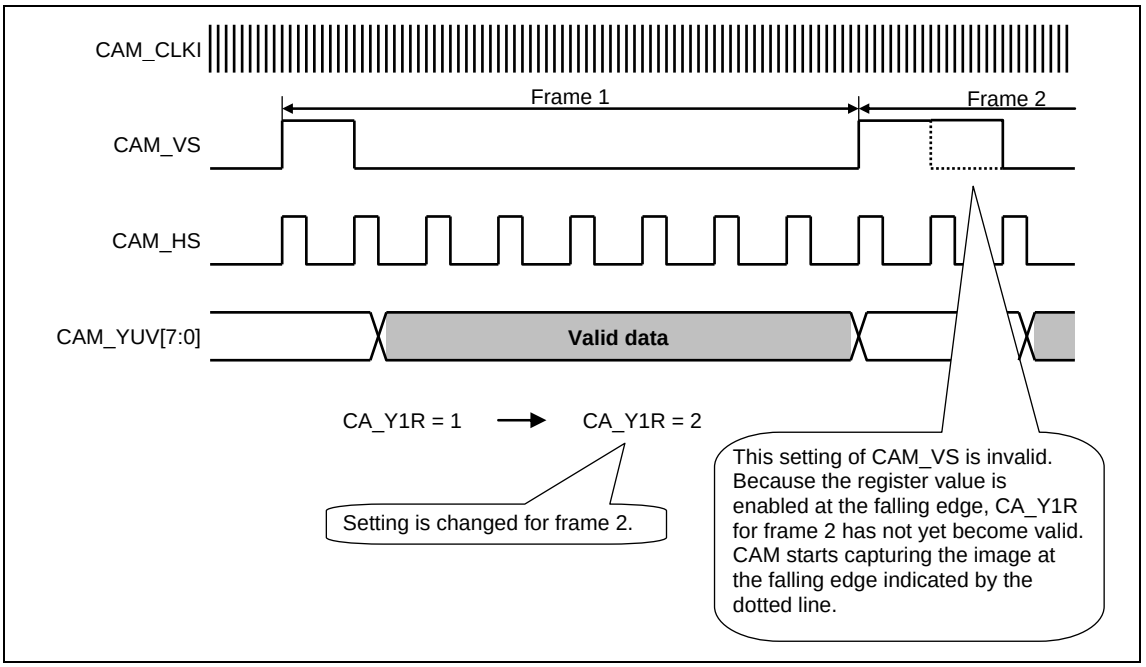
Figure 4-29. Frame Interval (Register Setting Enable Timing: Falling Edge)



4.13 Register Setting Enable Timing

If the register setting enable timing is the falling edge, note the values set to CA_X1R and CA_Y1R for the preceding frame. Depending on these values, the specified values may not become valid for the intended frame.

Figure 4-30. Register Setting Enable Timing: Falling Edge



5. Usage

5.1 Notice

Initialization (reset) of Camera interface is executed by register setting of SMU,
but this is reflected just asynchronously with an external synchronizing signal (VS/HS).

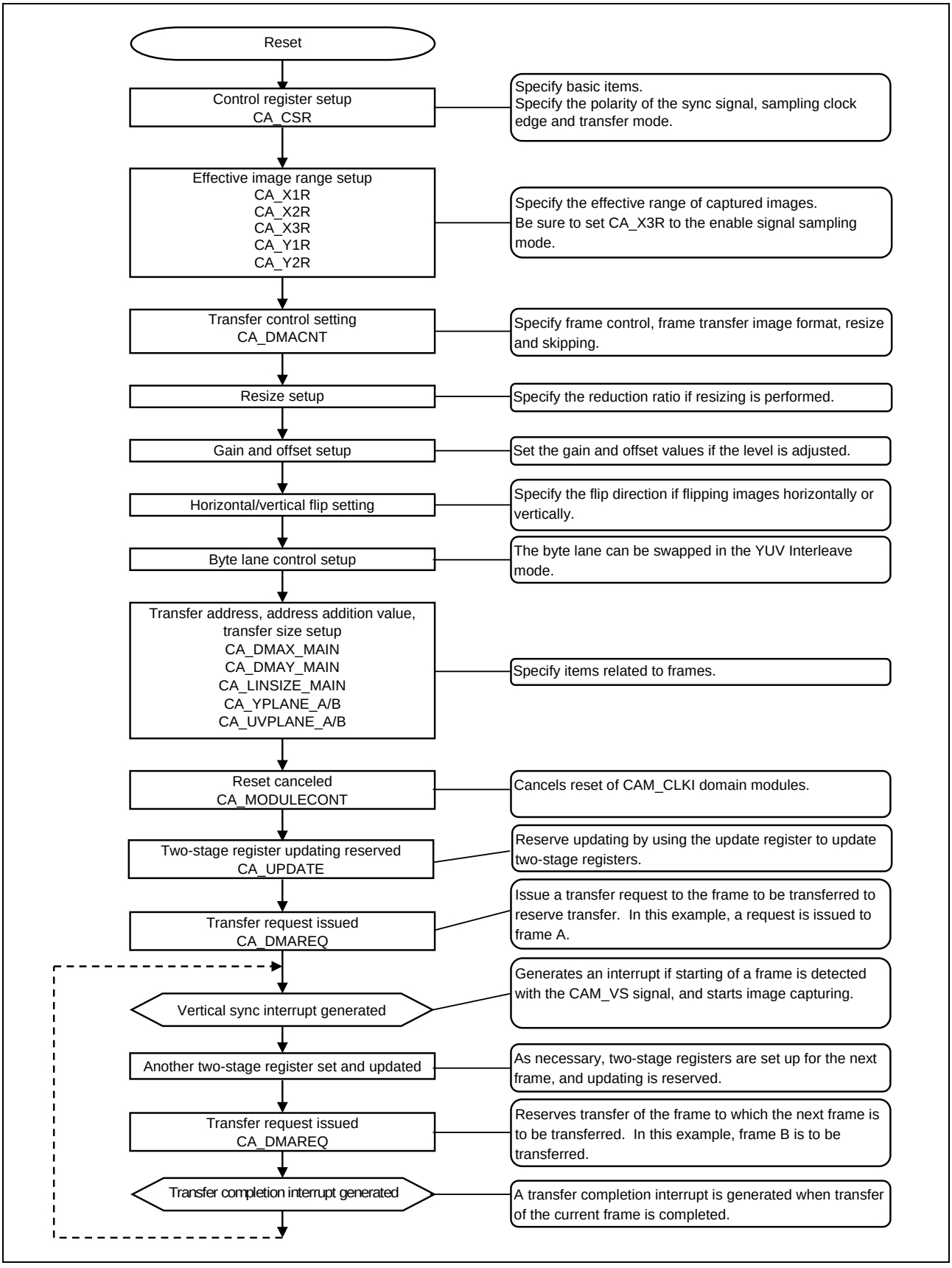
5.2 Example of Setting Procedure

An example of operations from reset to image capturing is shown below.
Be sure to satisfy the following timing conditions when releasing the reset state of the CAM_CLKI domain module; otherwise, the transfer request cannot be issued and thus transfer processing is not performed.

<1> After completion of CA_CSR register setup.
<2> Before reservation of updating the two-stage register and before issuance of a transfer request.

To release masking of the vertical synchronization interrupt (CAM_VS_EN bit of CA_ENSET register), wait for at least 16 CAM_CLKI cycles after the reset state of the CAM_CLKI domain is released.

Figure 5-1. Example of Setting Procedure

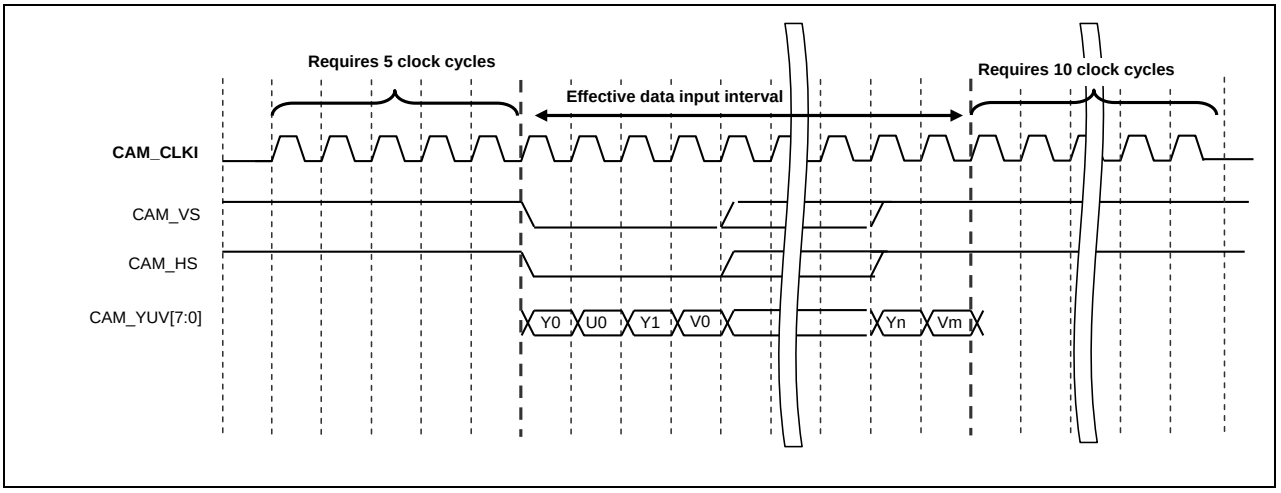


5.3 Restiction

There is a restriction regarding the timing of CAM_CLKI (the external clock), CAM_VS, CAM_HS, and CAMYUV[7:0] (input data).

CAM_CLKI must be supplied 5 clock cycles before effective data input and 10 clock cycles after effective data input. The former cycles are used to prepare for data capturing, and the latter cycles are used to pass the input data by using the AHB clock.

Figure 5-2. Relationship Between CAM_CLKI and Data



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		Page	Summary
1.00	Jan 29, 2010	—	1st revision release
2.00	Jun 7,2010	—	Incremental update from comments to the 1.0.
3.00	May 31, 2011	—	Document format changed.
4.00	Sep 30,2011	—	Incremental update from comments to the 3.0.
5.00	Dec 21, 2011	39	Chapter 3.2.7 (2) corrected. (bit[9:0] Function)
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