User's Manual

System Timer

User's Manual

Multimedia Processor for Mobile Applications
EMMA Mobile ™ EV2

Renesas Electronics
www.renesas.com

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the EMMA Mobile EV2. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Data Sheet	Hardware overview and electrical characteristics	EMMA Mobile EV2 Datasheet	R19DS0010EJxxxx
User's manual (1chip)	Hardware whole specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description	EMMA Mobile EV2 User's manual 1chip	R19UH0036EJxxxx
User's manual (module)	Hardware each macro specifications and operation description.	EMMA Mobile EV2 User's manual each module	See below

Document Name	Document No.	Document Name	Document No.
1chip	R19UH0036EJxxxx	DMA Controller	R19UH0043EJxxxx
System Management Unit	R19UH0037EJxxxx	LP-DDR/DDR2 Controller	R19UH0039EJxxxx
Timer	R19UH0054EJxxxx	SD Memory Card Interface	R19UH0061EJxxxx
System Timer (This manual)	R19UH0055EJxxxx	SDIO Interface	R19UH0042EJxxxx
HD Video Decoder	R19UH0056EJxxxx	CF Card Interface	R19UH0062EJxxxx
Rotator	R19UH0057EJxxxx	Unified Serial Interface	R19UH0047EJxxxx
Resizer	R19UH0058EJxxxx	UART interface	R19UH0040EJxxxx
Image Composer	R19UH0038EJxxxx	USB 2.0 Host Controller	R19UH0045EJxxxx
LCD Interface	R19UH0044EJxxxx	USB 2.0 Function Controller	R19UH0034EJxxxx
ITU-R BT.656 Interface	R19UH0059EJxxxx	IIC Interface	R19UH0052EJxxxx
Digital Terrestrial TV Interface	R19UH0048EJxxxx	General Purpose I/O Interface	R19UH0041EJxxxx
Camera Interface	R19UH0060EJxxxx	Pulse Width Modulation Interface	R19UH0063EJxxxx

4 digits of end shows the version.

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names

Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.

Examples the PM03 bit in the PM0 register

P3_5 pin, VCC pin

(2) Notation of Numbers

The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.

Examples Binary: 11b or 11

Hexadecimal: EFA0h

Decimal: 1234

3. Register Notation

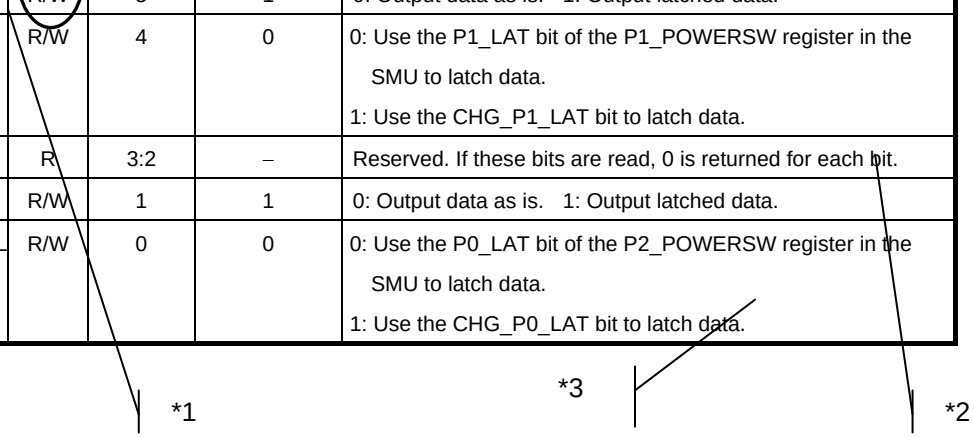
The symbols and terms used in register diagrams are described below.

x.x.x XXX register

This register (XXXXXXX: xxxx_xxxxh) …..

7	6	5	4	3	2	1	0
Reserved		CHG_P1_LAT	LATCH_P1_SEL	Reserved		CHG_P0_LAT	CHG_P0_LAT_SEL

Name	R/W	Bit No.	After Reset	Description
LATCH_P2_SEL	R/W	8	0	0: Use the P2_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P2_LAT bit to latch data.
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P1_LAT	R/W	5	1	0: Output data as is. 1: Output latched data.
LATCH_P1_SEL	R/W	4	0	0: Use the P1_LAT bit of the P1_POWERSW register in the SMU to latch data. 1: Use the CHG_P1_LAT bit to latch data.
Reserved	R	3:2	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P0_LAT	R/W	1	1	0: Output data as is. 1: Output latched data.
CHG_P0_LAT_SEL	R/W	0	0	0: Use the P0_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P0_LAT bit to latch data.



*1

R/W: Read and Write.

R: Read only.

W: Write only.

-: Nothing is assigned.

*2

Reserved bit.

Reserved bit. Set to specified value.

*3

・ Nothing is assigned.

Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.

・ Do not set to a value.

Operation is not guaranteed when a value is set.

・ Function varies according to the operating mode.

The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Register
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

Table of Contents

1. Overview

STI is a unique system timer designed to provide system time over a long period.
STI is a 48-bit counter that runs on a 32.768 kHz or 32 kHz timer clock.

Caution 32.768 kHz or 32 kHz can be selected by using an SMU register.

1.1 Features

The main features of STI are as follows.

(1) Operating frequency 32 kHz

STI includes a counter that runs on a 32 kHz timer clock.

(2) 48-bit counter

When the timer runs on a 32 kHz timer clock, a count value will be displayed for approximately 272 years.

(3) Hardware-based bus clock synchronization

Software-based synchronization is not required when reading data.

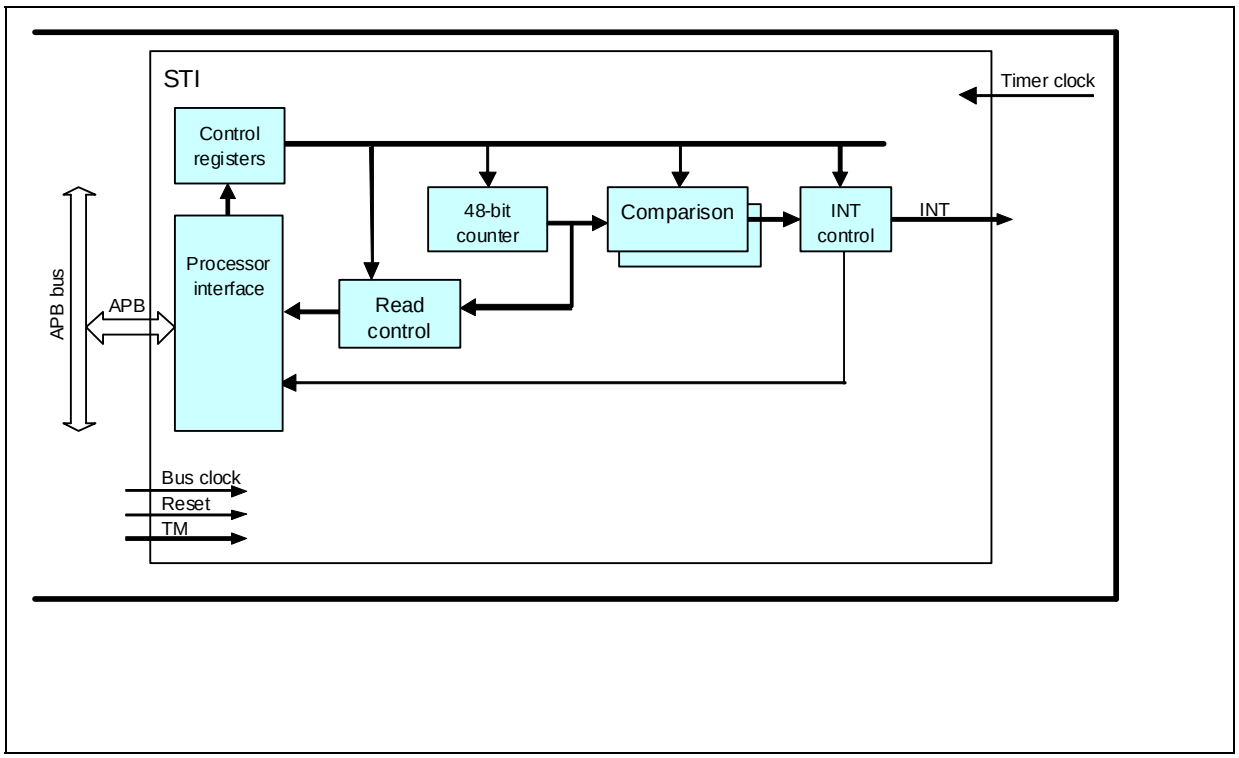
(4) Two count value match detection interrupt registers (higher 16 bits and lower 32 bits)

Two count value match detection interrupt registers are available. These registers are used to generate an interrupt when the system counter value matches the specified value.

Interrupt sources can be masked and cleared individually.

1.2 Block Diagram

Figure 1-1 Block Diagram



2. Registers

These registers are accessed via the APB bus, and can only be accessed in 32-bit units.
Do not access reserved registers. When a reserved register is read, the value 0000_0000H is returned.
Do not write any value other than 0 to reserved bits in each register.

2.1 Register List

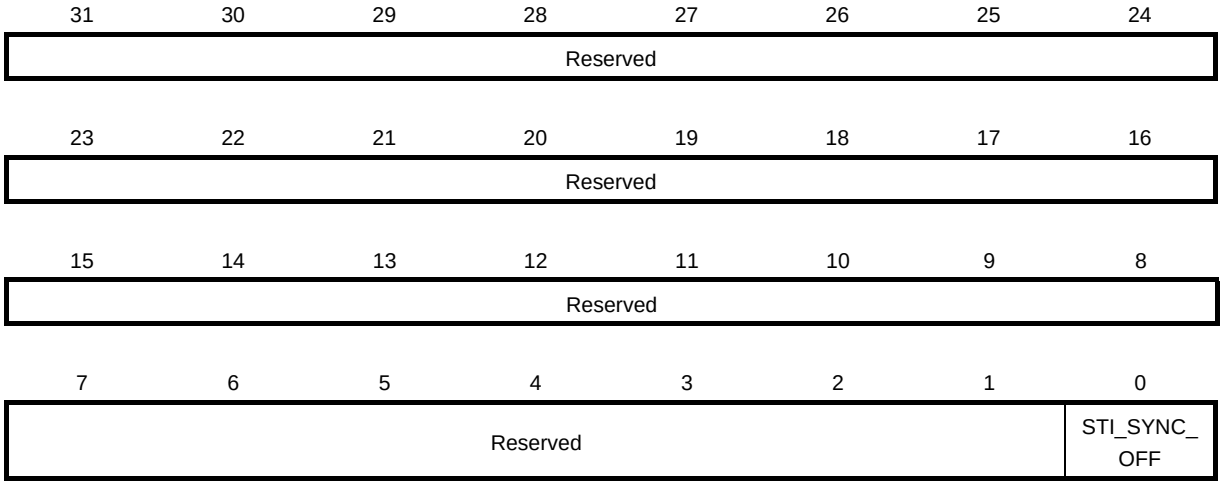
Base address: E018_0000H

Address	Register Name	Symbol	R/W	After Reset
0000H	Control register	STI_CONTROL	R/W, W	0000_0000H
0004H to 000CH	Reserved	–	–	–
0010H	Timer compare register A (higher 16 bits)	STI_COMPA_H	R/W	0000_FFFFH
0014H	Timer compare register A (lower 32 bits)	STI_COMPA_L	R/W	FFFF_FFFFH
0018H	Timer compare register B (higher 16 bits)	STI_COMPB_H	R/W	0000_FFFFH
001CH	Timer compare register B (lower 32 bits)	STI_COMPB_L	R/W	FFFF_FFFFH
0020H	Synchronous timer count value register (higher 16 bits)	STI_COUNT_H	R	0000_0000H
0024H	Synchronous timer count value register (lower 32 bits)	STI_COUNT_L	R	0000_0000H
0028H	Asynchronous timer count value register (higher 16 bits)	STI_COUNT_RAW_H	R	0000_0000H
002CH	Asynchronous timer count value register (lower 32 bits)	STI_COUNT_RAW_L	R	0000_0000H
0030H	Counter value set register (higher 16 bits)	STI_SET_H	R/W, W	0000_0000H
0034H	Counter value set register (lower 32 bits)	STI_SET_L	R/W	0000_0000H
0038H to 003CH	Reserved	–	–	–
0040H	Interrupt status register	STI_INTSTATUS	R	0000_0000H
0044H	Interrupt raw status register	STI_INTRAWSTATUS	R	0000_0000H
0048H	Interrupt enable set register	STI_INTENSET	R/W	0000_0000H
004CH	Interrupt enable clear register	STI_INTENCLR	W	0000_0000H
0050H	Interrupt source clear register	STI_INTFFCLR	W	0000_0000H
0054H to FFFCH	Reserved	–	–	–

2.2 Register Details

2.2.1 Control register (STI_CONTROL: 0000H)

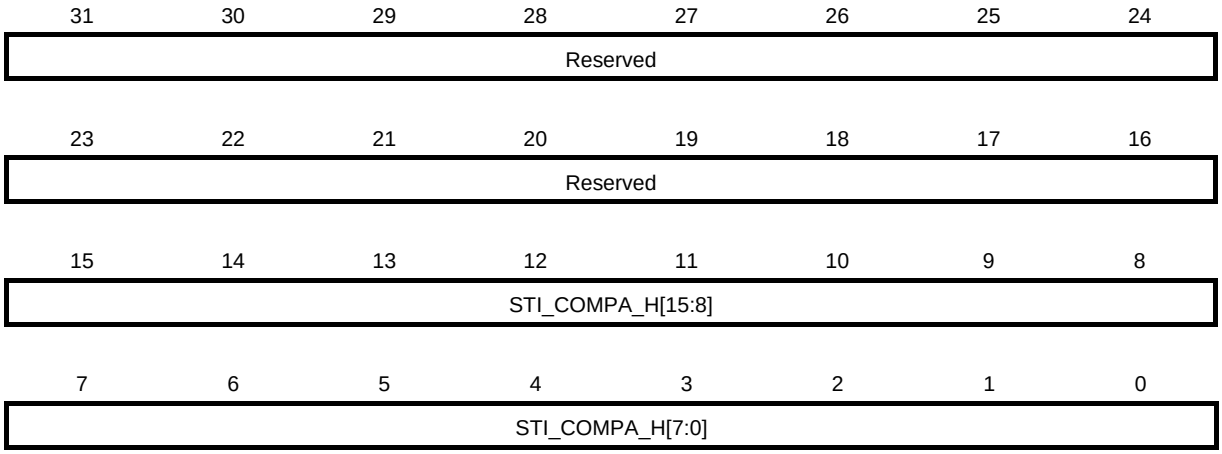
This register controls the STI module.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	0000_0000H	Reserved. If these bits are read, 0 is returned for each bit.
STI_SYNC_OFF	W	0	0	This bit releases the synchronization-stopped state of the synchronous timer count value register (STI_COUNT_H/L). 0: Ignored. 1: Release the synchronization-stopped state. If this bit is read, 0 is returned.

2.2.2 Timer compare register A (higher 16 bits) (STI_COMPA_H: 0010H)

This register specifies the reference timer count value used to generate an interrupt when the system timer count value matches the reference value.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:16	0000H	Reserved. If these bits are read, 0 is returned for each bit.
STI_COMPA_H[15:0]	R/W	15:0	FFFFH	These bits specify the value to be compared with the system timer count value. If these bits are read, the specified value is returned.

(1) Procedure for setting up timer compare register A/B

When setting up a timer compare register, be sure to follow the procedure below so as not to generate unnecessary interrupts. If an interrupt has occurred, clear the interrupt first.

(a) Mask issuance of interrupt requests by using the interrupt enable clear register.

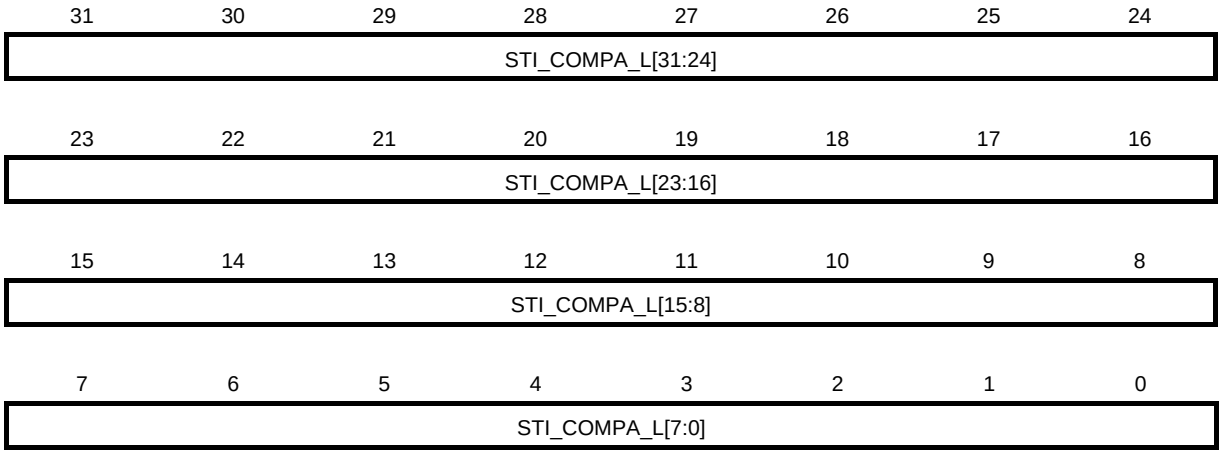
(b) Set the timer compare register.

(c) Clear the interrupt source by using the interrupt source clear register.

(d) Enable issuance of interrupt requests by using the interrupt enable set register.

2.2.3 Timer compare register A (lower 32 bits) (STI_COMPA_L: 0014H)

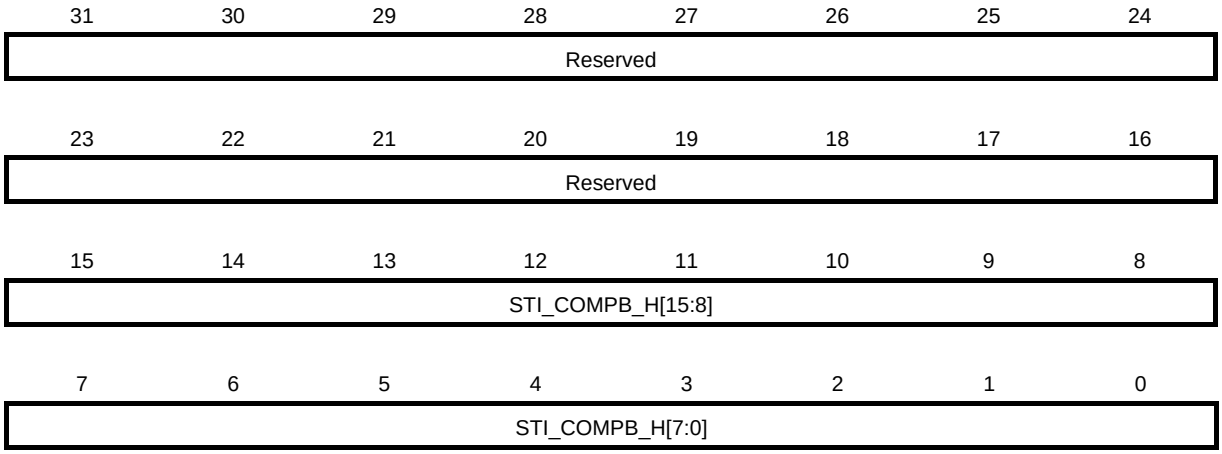
This register specifies the reference timer count value used to generate an interrupt when the system timer count value matches the reference value.



Name	R/W	Bit No.	After Reset	Description
STI_COMPA_L	R/W	31:0	FFFF_FFFFH	These bits specify the value to be compared with the system timer count value. If these bits are read, the specified value is returned.

2.2.4 Timer compare register B (higher 16 bits) (STI_COMPB_H: 0018H)

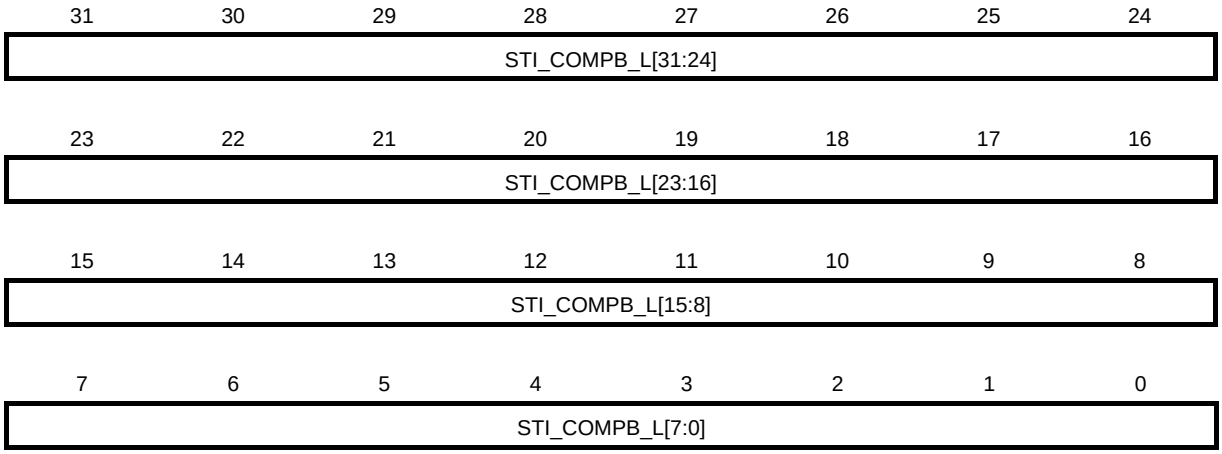
This register specifies the reference timer count value used to generate an interrupt when the system timer count value matches the reference value.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:16	0000H	Reserved. If these bits are read, 0 is returned for each bit.
STI_COMPB_H	R/W	15:0	FFFFH	These bits specify the value to be compared with the system timer count value. If these bits are read, the specified value is returned.

2.2.5 Timer compare register B (lower 32 bits) (STI_COMPB_L: 001CH)

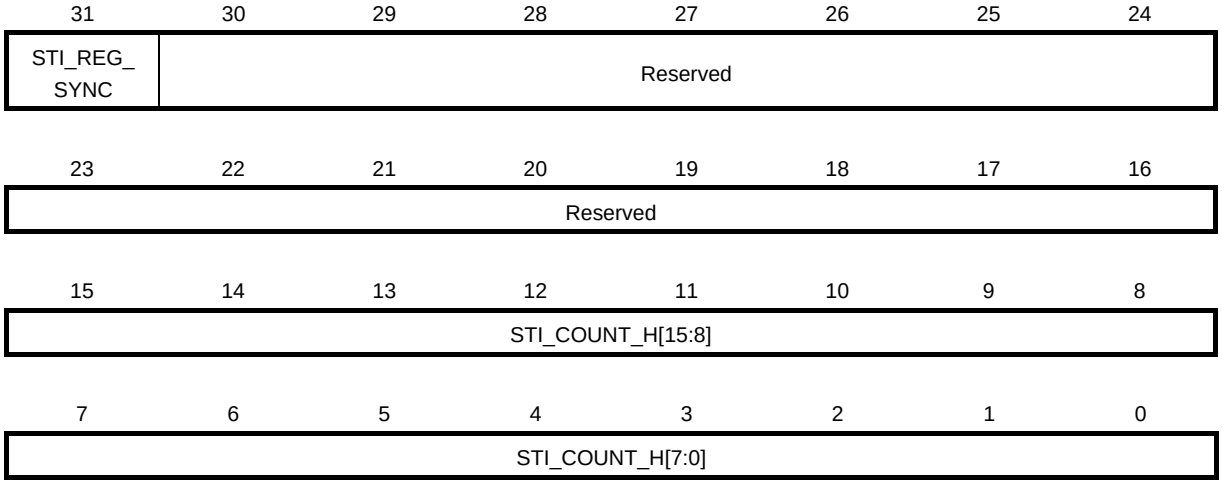
This register specifies the reference timer count value used to generate an interrupt when the system timer count value matches the reference value.



Name	R/W	Bit No.	After Reset	Description
STI_COMPB_L	R/W	31:0	FFFF_FFFFH	These bits specify the value to be compared with the system timer count value. If these bits are read, the specified value is returned.

2.2.6 Synchronous timer count value register (higher 16 bits) (STI_COUNT_H: 0020H)

This register is used to read the system timer count value synchronously.



Name	R/W	Bit No.	After Reset	Description
STI_REG_SYNC	R	31	0	0: Indicates that the values read from the STI_COUNT_H/L registers are not synchronized with the STI count values. 1: Indicates that the values read from the STI_COUNT_H/L registers are synchronized with the STI count values. Writing this bit is ignored.
Reserved	R	30:16	0000H	Reserved. If these bits are read, 0 is returned for each bit. Writing these bits is ignored.
STI_COUNT_H	R	15:0	0000H	The STI count value synchronized with the bus clock is read from these bits. Writing these bits is ignored.

(1) Match of time at which data is read

To read the 48-bit counter value via the 32-bit bus, the bus access must be separated into two clock cycles and the counter must be read in two steps: from the STI_COUNT_H register and then from the STI_COUNT_L register.

The following mechanism has been implemented to guarantee that the count time between the read data matches:

If the STI_COUNT_H bits of the STI_COUNT_H register are read, updating the STI_COUNT_H and STI_COUNT_L register values is suspended until the STI_COUNT_L bits of the STI_COUNT_L register have been read. Consequently, by reading the higher and lower bits in that order, count values of the same time are guaranteed to be read as long as the STI_COUNT_H register is read and then the STI_COUNT_L register is read.

If the STI_COUNT_H bits are read successively, the same data as the first read data is read out. The time is guaranteed to match the STI_COUNT_H bit data for the first data subsequently read from the STI_COUNT_L bits.

If the STI_COUNT_L bits are read successively, the count value is updated continually. If data is read from the STI_COUNT_L bits and then the STI_COUNT_H bits, the time is not guaranteed to match between the data read from both sides.

(2) Read operation after bus clock supply is stopped and then resumed

If the bus clock stops, the read data is not updated, because the mechanism that synchronizes the counter operating on the timer clock with the bus clock also stops.

When clock supply resumes, the counter synchronizes with the clock within one timer clock cycle.

(3) Reading the synchronous timer count value

Reading the synchronous timer count value via the PMU is prohibited when the bus clock speed is low (32 kHz). The correct value cannot be read, even if attempted.

If the low-speed bus clock is used, read the count value from the PMU by using the asynchronous timer count value register.

2.2.7 Synchronous timer count value register (lower 32 bits) (STI_COUNT_L: 0024H)

This register is used to read the system timer count value synchronously.

31	30	29	28	27	26	25	24
STI_COUNT_L[31:24]							

23	22	21	20	19	18	17	16
STI_COUNT_L[23:16]							

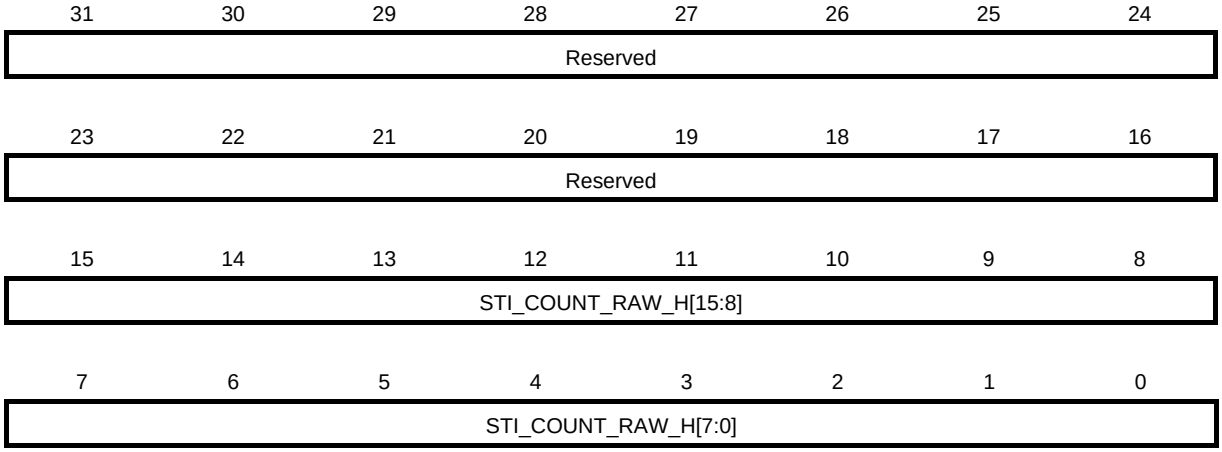
15	14	13	12	11	10	9	8
STI_COUNT_L[15:8]							

7	6	5	4	3	2	1	0
STI_COUNT_L[7:0]							

Name	R/W	Bit No.	After Reset	Description
STI_COUNT_L	R	31:0	0000_0000H	These bits return the system timer count value. Writing these bits is ignored.

2.2.8 Asynchronous timer count value register (higher 16 bits) (STI_COUNT_RAW_H: 0028H)

This register is used to read the system timer count value asynchronously.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:16	0000H	Reserved. If these bits are read, 0 is returned for each bit. Writing these bits is ignored.
STI_COUNT_RAW _H	R	15:0	0000H	These bits return the system timer count value. Writing these bits is ignored.

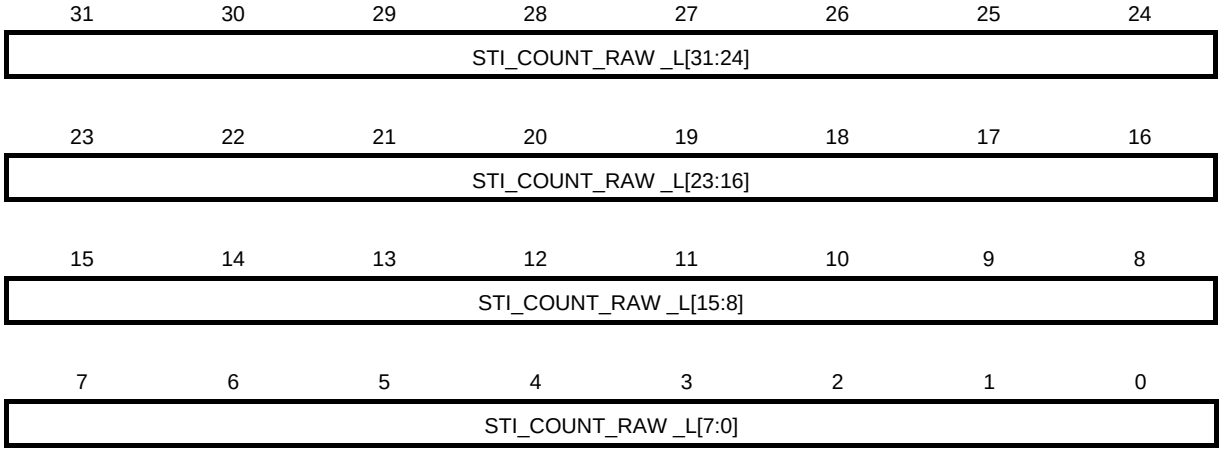
The counter value can usually be read without synchronization by software, by reading a synchronous timer count value register.
When the bus clock supply stops and then resumes, the system must be programmed to wait for up to one timer clock cycle until the counter synchronizes with the bus clock.
If this wait time might cause problems, read the asynchronous timer count register value using the following procedure to eliminate the need to wait for synchronization:

Count value read order

(1) H1 ← STI_COUNT_RAW_H
(2) L1 ← STI_COUNT_RAW_L
(3) H2 ← STI_COUNT_RAW_H
(4) L2 ← STI_COUNT_RAW_L
(5) If both H1 and H2, L1 and L2 match, H1 and L1 are used as the count value and read processing ends.
If they do not match, repeat the procedure from (1).

2.2.9 Asynchronous timer count value register (lower 32 bits) (STI_COUNT_RAW_L: 002CH)

This register is used to read the system timer count value asynchronously.



Name	R/W	Bit No.	After Reset	Description
STI_COUNT_RAW _L	R	31:0	0000_0000H	These bits return the system timer count value. Writing to these bits is ignored.

2.2.10 Counter value set register (higher 16 bits) (STI_SET_H: 0030H)

This register specifies the initial values for the system timer.

31	30	29	28	27	26	25	24
STI_SET_IMME	STI_SET_SYNC	Reserved					

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
STI_SET_H[15:8]							

7	6	5	4	3	2	1	0
STI_SET_H[7:0]							

Name	R/W	Bit No.	After Reset	Description
STI_SET_IMME	W	31	–	0: Ignored. 1: Specify the STI_SET_H[15:0] bit values to the counter without waiting for the STI_SET_L register to be set. If this bit is read, 0 is returned.
STI_SET_SYNC	R/W	30	0	0: Do not set the value of this register to the counter when the STI_SET_L register is written. 1: Specify the value of this register to the counter when the STI_SET_L register is written.
Reserved	–	29:16	0000H	Reserved. If these bits are read, 0 is returned for each bit.
STI_SET_H	R/W	15:0	0000H	These bits specify the initial values to be set to the system timer. If these bits are read, the specified value is returned.

Because the 48-bit timer counter is initialized in two steps—writing to a higher register and a lower register as a pair—the following mechanism is implemented so as to prevent mismatch in the timing at which the higher and lower registers are written.

(1) Immediate setting mode

If the STI_SET_IMME bit of this register is set to 1, the values set to the STI_SET_H bits are set to the system timer, regardless of the STI_SET_SYNC bit setting.

(2) Synchronous setting mode

If the lower bits of the counter value set register (STI_SET_L) are written while the STI_SET_SYNC bit of this register is set to 1, the values set to the higher bits (STI_SET_H) are also set to the system timer at the same time, in synchronization with the 32 kHz timer clock.

To synchronize the counter value with the 32 kHz timer clock, the setting of values to the counter is delayed for one timer clock cycle, and reading values from the timer is also delayed for one timer clock cycle. Consequently, the set value is applied to the read data after two timer clock cycles.

2.2.11 Counter value set register (lower 32 bits) (STI_SET_L: 0034H)

This register specifies the initial values for the system timer.

31	30	29	28	27	26	25	24
STI_SET _L[31:24]							

23	22	21	20	19	18	17	16
STI_SET_L[23:16]							

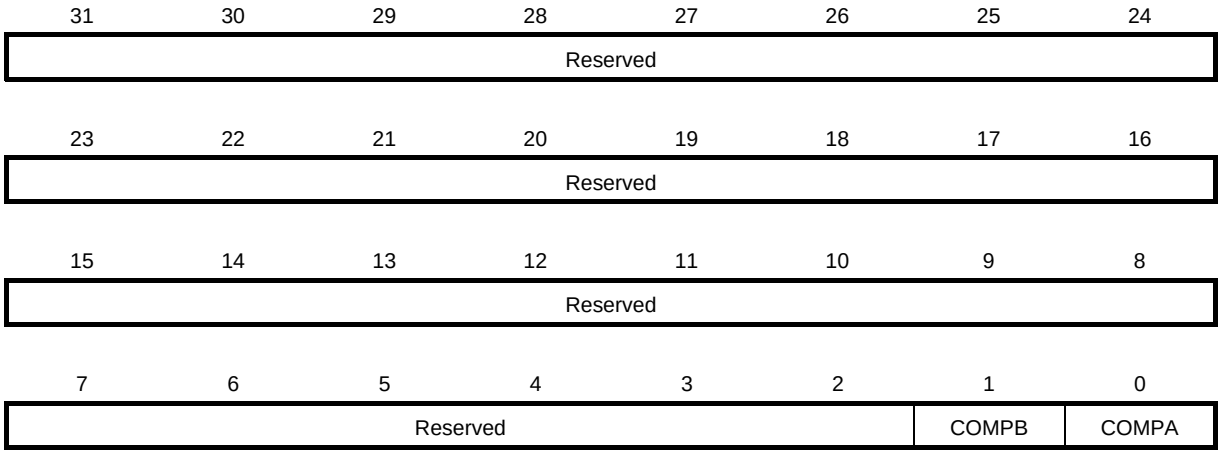
15	14	13	12	11	10	9	8
STI_SET _L[15:8]							

7	6	5	4	3	2	1	0
STI_SET _L[7:0]							

Name	R/W	Bit No.	After Reset	Description
STI_SET _L	R/W	31:0	0000_0000H	These bits specify the initial values to be set to the system timer. If these bits are read, the specified value is returned.

2.2.12 Interrupt status register (STI_INTSTATUS: 0040H)

This is a read-only register that indicates the status of interrupt sources.
The status of the interrupt sources enabled by using the interrupt enable set register (STI_INTENSET: 48H) can be read from this register.

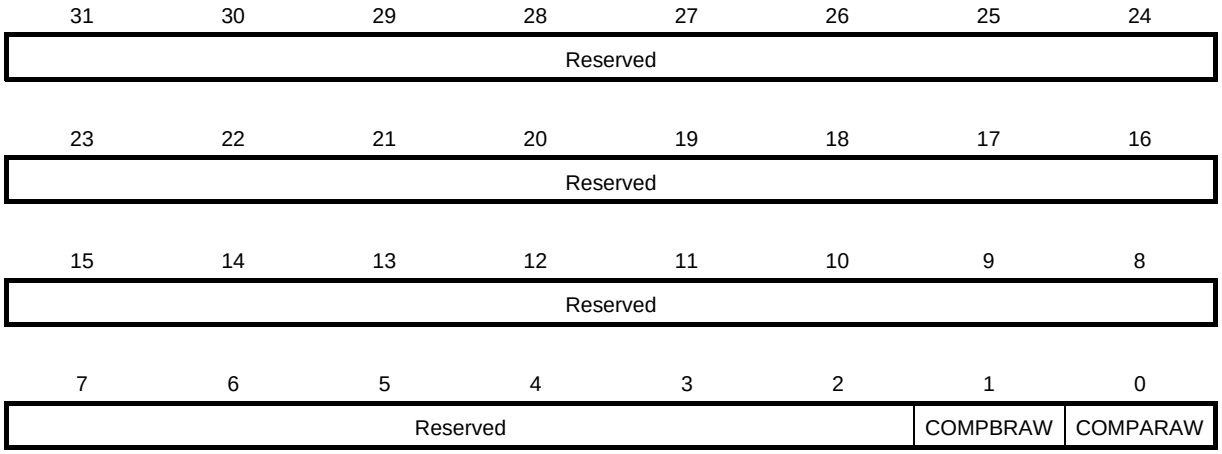


Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	0000_0000H	Reserved. If these bits are read, 0 is returned for each bit.
COMPB	R	1	0	This bit indicates the status of the count match interrupt of timer compare register B. 0: No interrupt 1: Interrupt occurred.
COMPA	R	0	0	This bit indicates the status of the count match interrupt of timer compare register A. 0: No interrupt 1: Interrupt occurred.

2.2.13 Interrupt raw status register (STI_INTRAWSTATUS: 0044H)

This is a read-only register that indicates the status of interrupt sources.

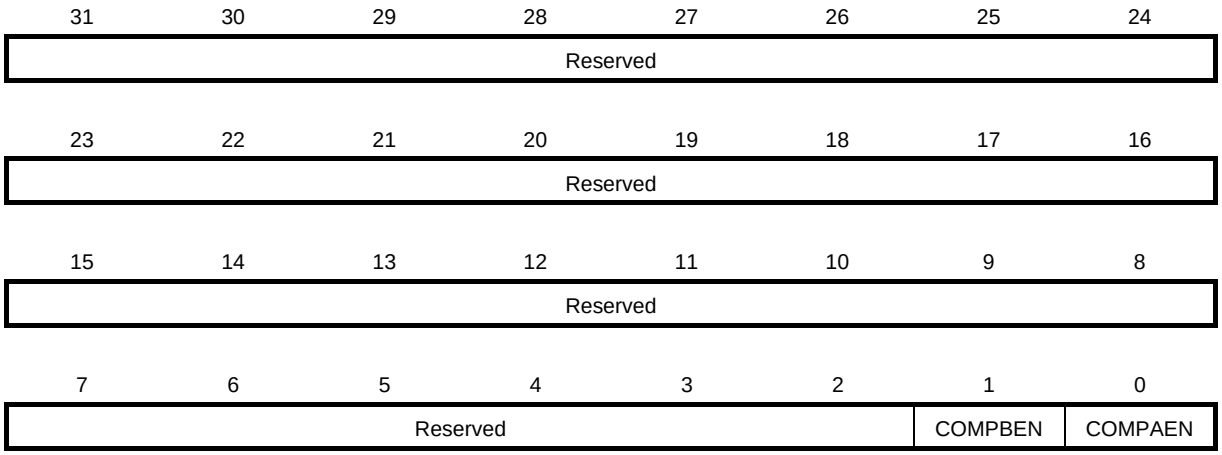
The bits corresponding to the interrupt sources are set regardless of the settings of the interrupt enable set register (STI_INTENSET: 48H) and the interrupt enable clear register (STI_INTENCLR: 4CH).



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	0000_0000H	Reserved. If these bits are read, 0 is returned for each bit.
COMPBRAW	R	1	0	Indicates the status of the count match interrupt of timer compare register B. 0: No interrupt 1: Interrupt occurred.
COMPARAW	R	0	0	Indicates the status of the count match interrupt of timer compare register A. 0: No source 1: Interrupt occurred.

2.2.14 Interrupt enable set register (STI_INTENSET: 0048H)

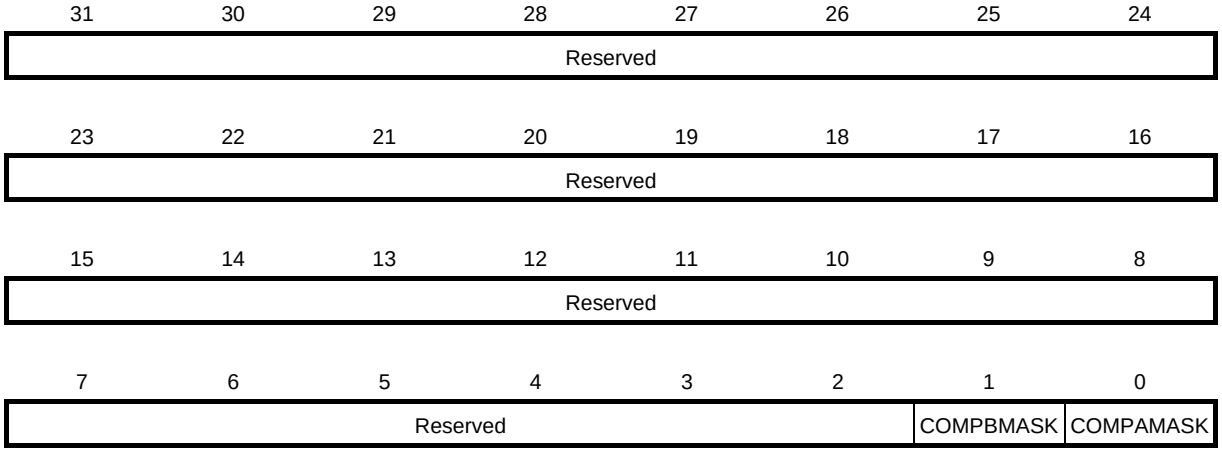
This register specifies whether to enable issuance of interrupt requests.
Only the data of the bits to which 1 is written is updated.
If the bit corresponding to an interrupt source is set to 1 in this register, the interrupt source is enabled, the relevant interrupt request is issued, and the corresponding bit of the interrupt status register (STI_INTSTATUS: 40H) is set to 1. If no bits are set in this register, no interrupt requests are issued even if the interrupt source is enabled, but the corresponding bit of the interrupt raw status register is set to 1.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	0000_0000H	Reserved. If these bits are read, 0 is returned for each bit.
COMPBEN	R	1	0	This bit indicates whether issuance of the count match interrupt request of timer compare register B is enabled. 0: Not enabled 1: Enabled
	W	1	–	This bit enables issuance of the count match interrupt request of the timer compare register. 0: Ignored 1: Unmask the interrupt.
COMPAEN	R	0	0	This bit indicates whether issuance of the count match interrupt request of timer compare register A is enabled. 0: Not enabled 1: Enabled
	W	0	–	This bit enables issuance of the count match interrupt request of timer compare register A. 0: Ignored 1: Unmask the interrupt.

2.2.15 Interrupt enable clear register (STI_INTENCLR: 004CH)

This is a write-only register that masks issuance of interrupt requests.
Only the data of the bits to which 1 is written is updated.
If the bit corresponding to an interrupt source in this register is set to 1, no interrupt requests are issued even if the interrupt source occurs. The status of the corresponding bit in the interrupt status register also remains unchanged.
If no bits are set in this register, an interrupt request is issued and the corresponding bit of the interrupt status register is set to 1 when the interrupt source is enabled.



Name	R/W	Bit No.	After Reset	Description
Reserved	–	31:2	0000_0000H	Reserved. If these bits are read, 0 is returned for each bit.
COMPBMASK	W	1	0	This bit disables issuance of the count match interrupt request of timer compare register B. 0: Ignored. 1: Mask the interrupt.
COMPAMASK	W	0	0	This bit disables issuance of the count match interrupt request of timer compare register A. 0: Ignored. 1: Mask the interrupt.

2.2.16 Interrupt source clear register (STI_INTFFCLR: 0050H)

This is a write-only register that clears the interrupt sources.

Only the data of the bits to which 1 is written is updated.

Setting the bit corresponding to an interrupt source to 1 clears the interrupt source.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved						COMPBCLR	COMPACLR

Name	R/W	Bit No.	After Reset	Description
Reserved	–	31:2	0000_0000H	Reserved. If these bits are read, 0 is returned for each bit.
COMPBCLR	W	1	0	This bit clears the count match interrupt request source of timer compare register B. 0: Ignored. 1: Clear the interrupt source.
COMPACLR	W	0	0	This bit clears the count match interrupt request source of timer compare register A. 0: Ignored. 1: Clear the interrupt source.

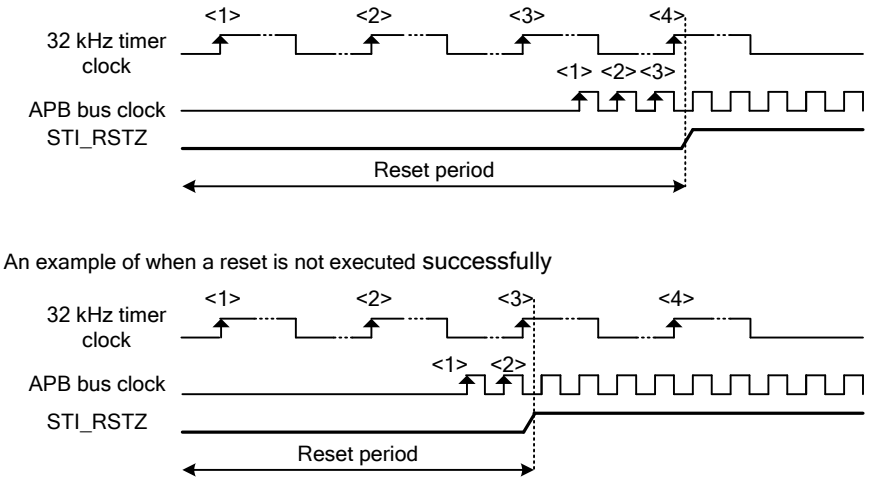
3. Description of Functions

3.1 Reset Control

- All the system timer module registers use a synchronous reset.
- To reset all registers while the power is on, the APB bus clock and 32 kHz timer clock must be supplied from the SMU during the power-on reset period.
- To execute a reset by setting a reset register in the SMU, clock supply must be enabled by setting a clock control register in the SMU.
- When an SMU reset register is set, the count value is reset to 0H and counting stops.
- The count value does not change even if the reset state is entered while supply of the 32 kHz timer clock is stopped.
- If the timer value is specified within the first 32 kHz timer clock cycle after reset ends, the specified value is not applied to the timer (but it is applied to the register).

Assert the reset signal for at least three bus clock cycles, or for at least four 32 kHz timer clock cycles.

Figure 3-1. Reset Signal Timing



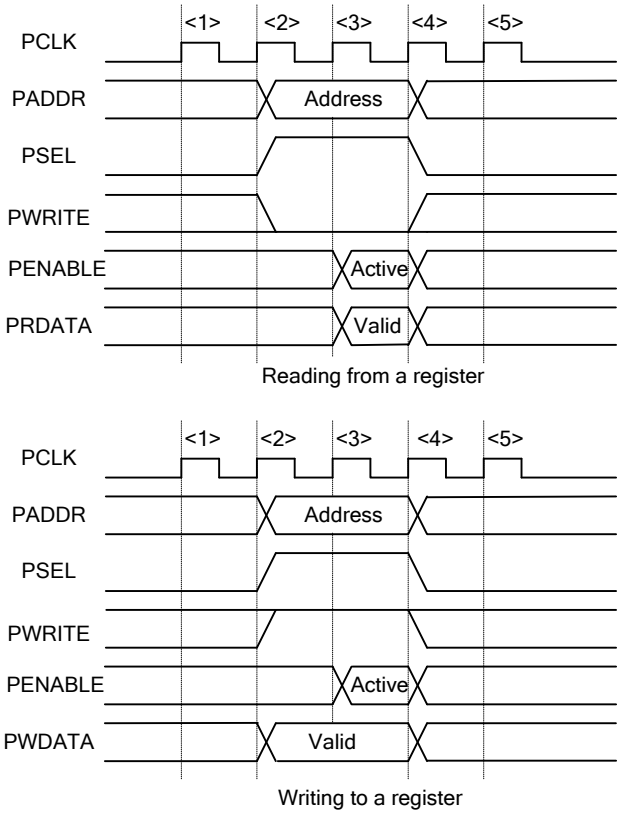
3.2 Clocks

- The STI module runs on the APB bus clock supplied to the APB controller and the timer clock supplied to the timer block.
  Supply of these clocks can be enabled and stopped by setting a clock control register in the SMU.
- If supply of the timer clock is stopped by setting a clock control register in the SMU, counting stops.
  The count value at this time is the value just before the timer clock was stopped.
- Supply of the APB bus clock can be automatically enabled and stopped by performing control using the APB bridge and SMU.
- In the STI module, the timer clock must be supplied for at least four cycles near the rising and falling edges to allow the data of each clock to synchronize.
  The relationship between the clocks must be established in the SMU.

3.2.1 Clock supply when accessing registers

When the bus clock is controlled automatically, be sure to input the clock for at least the number of cycles shown in the figure below.

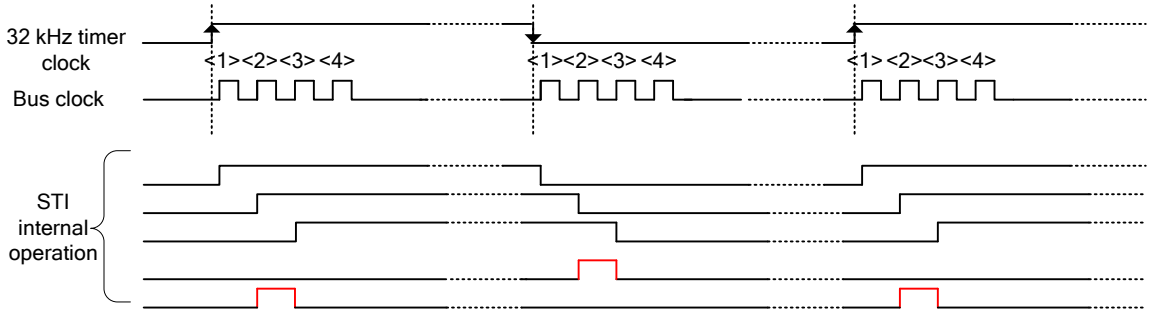
Figure 3-2. Clock Supply Timing When Bus Clock Is Controlled Automatically



3.2.2 Relationship between timer clock and bus clock

Ensure that the timer clock and bus clock are supplied for at least the number of cycles shown in the figure below to allow the data of each clock to synchronize.

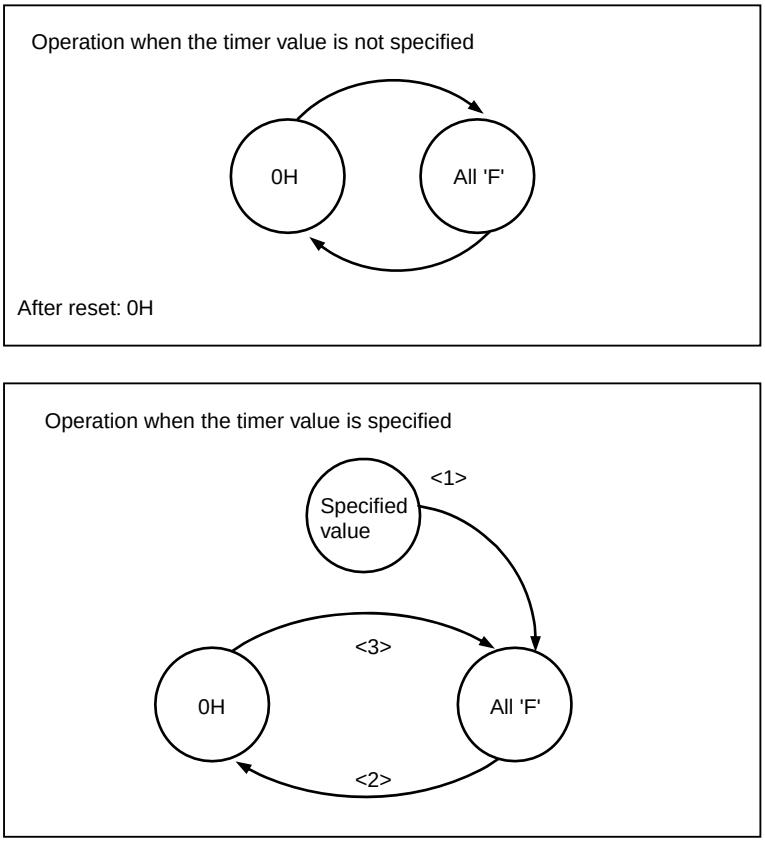
Figure 3-3. Relationship Between Timer Clock and Bus Clock



3.3 Timer Operation

If reset ends while the 32 kHz timer clock is being supplied from the SMU, the STI module starts counting from 0H.
STI module counting cannot be controlled other than by enabling and stopping clock supply, and executing a reset via the SMU.
If clock supply from the SMU stops, the counter stops at the value immediately before the clock stopped.
When clock supply from the SMU resumes, the counter starts counting from that value.
After reset ends, the timer counts from 0H to FFFF_FFFF_FFFFH in free-running mode, and returns to 0H when the value reaches FFFF_FFFF_FFFFH.
If a timer value is specified, the timer counts from the specified value to FFFF_FFFF_FFFFH. When the value reaches FFFF_FFFF_FFFFH, the count does not return to the specified value but to 0H.

Figure 3-4. Timer Operation Transition



3.3.1 Specifying timer values

Two modes are available for specifying the timer value: immediate setting mode and synchronous setting mode. To specify the timer value, specify the initial counter value for the system timer.

Table 3-1. Specifying Timer Values

STI_SET_H: 30H		Operation	Remark
Bit 31	Bit 30		
STI_SET_IMME	STI_SET_SYNC		
1	– (Ignored)	The values specified to the STI_SET_H register are set to the timer immediately. A total of the current value + 1 is set to the STI_SET_L register (that is, nothing is performed).	Immediate setting of higher bits
0	0	If values are written to the STI_SET_L register, the specified values are set to the timer, but the values of the STI_SET_H register are not set to the timer.	Immediate setting of lower bits
0	1	If values are written to the STI_SET_L register, the values set to the STI_SET_L register and the values set to the STI_SET_H register are set to the timer at the same time.	Synchronous setting of higher and lower bits

3.3.2 Timing of setting timer value

Data updating is triggered by the falling edge of the timer clock.
The timer value is applied to the timer one timer clock cycle after setting the value to allow for synchronization with the 32 kHz timer clock.

Figure 3-5. Timing of Setting Timer Value <1>

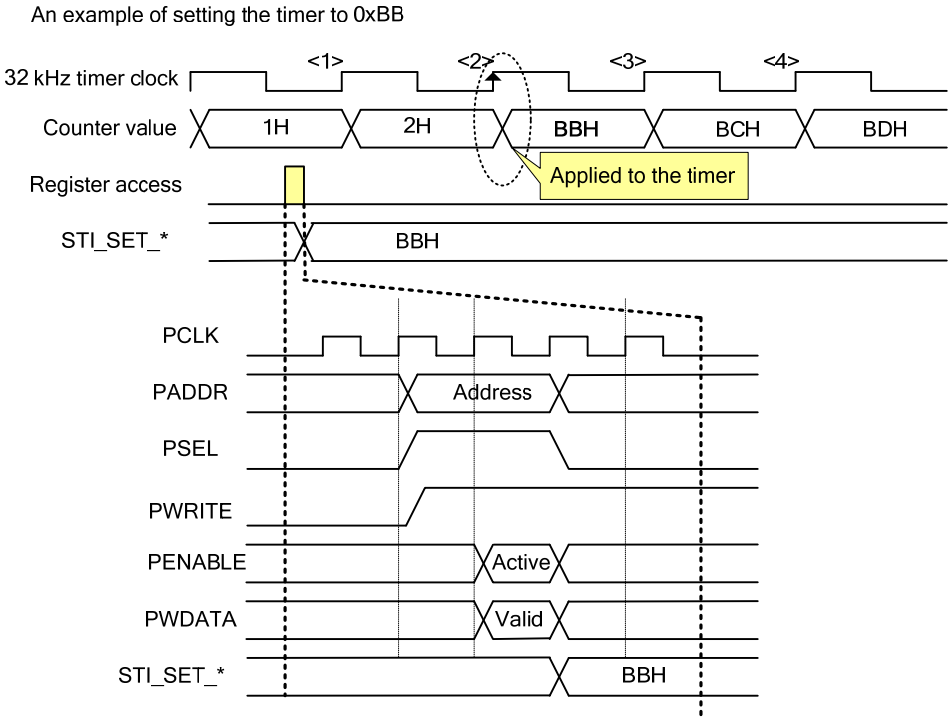


Figure 3-6. Timing of Setting Timer Value <2>

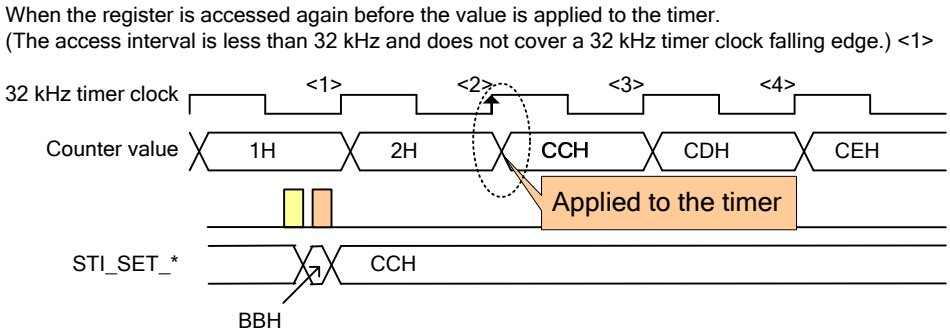
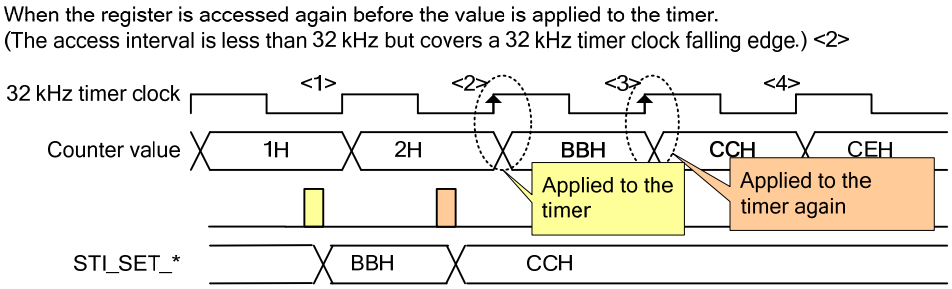


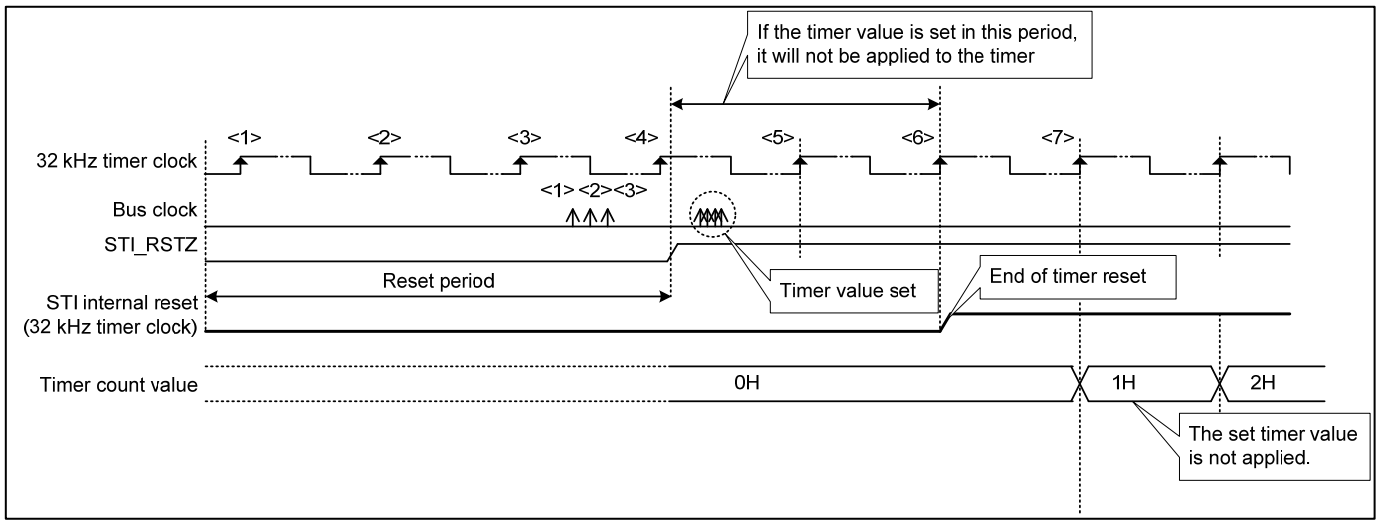
Figure 3-7. Timing of Setting Timer Value <3>



Cautions on setting the timer value

If the timer value is set immediately after a reset ends, there is an interval of two 32 kHz timer clock cycles in which the set value is not applied to the timer. See the figure below for details.

Figure 3-8. Timing at Which Set Value Is Not Applied to Timer

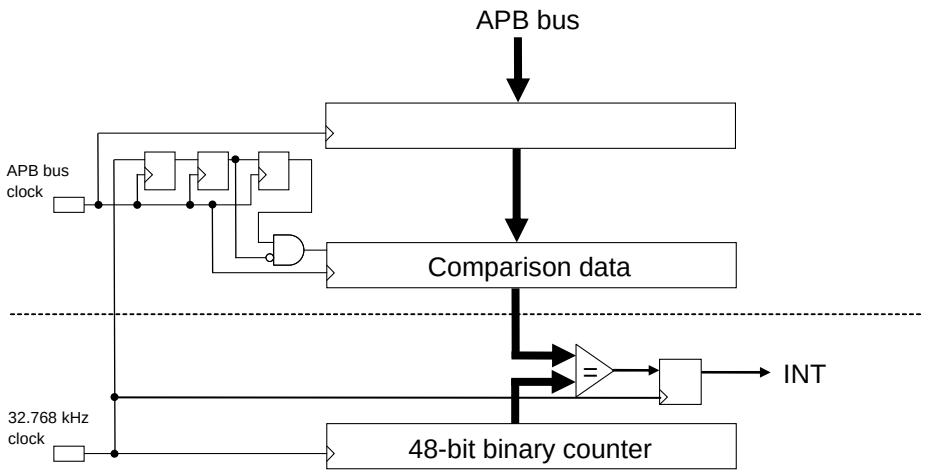


3.4 Timer Comparison

An interrupt occurs if the STI count value matches the value set to the timer compare register.
The interrupt source statuses are retained in the interrupt raw status register.
The interrupt raw status register is cleared by writing 1 to the interrupt clear register.
Because the timer compare register has two systems (A and B), two values can be specified at the same time.
Two systems of interrupts (A and B) have individual status registers, so masking and clearing of interrupts can also be specified individually.

Timer comparison is performed and a match is detected in synchronization with the timer clock so that the timer compare interrupt can be issued even while the APB bus clock is stopped. This essentially means that the timer compare registers must be updated in synchronization with the timer clock. However, because the timer compare register is updated at the falling edge of the timer clock, the timer compare registers can also be controlled by the APB bus clock (without synchronizing with the timer clock).

Figure 3-9. Count Match Detection

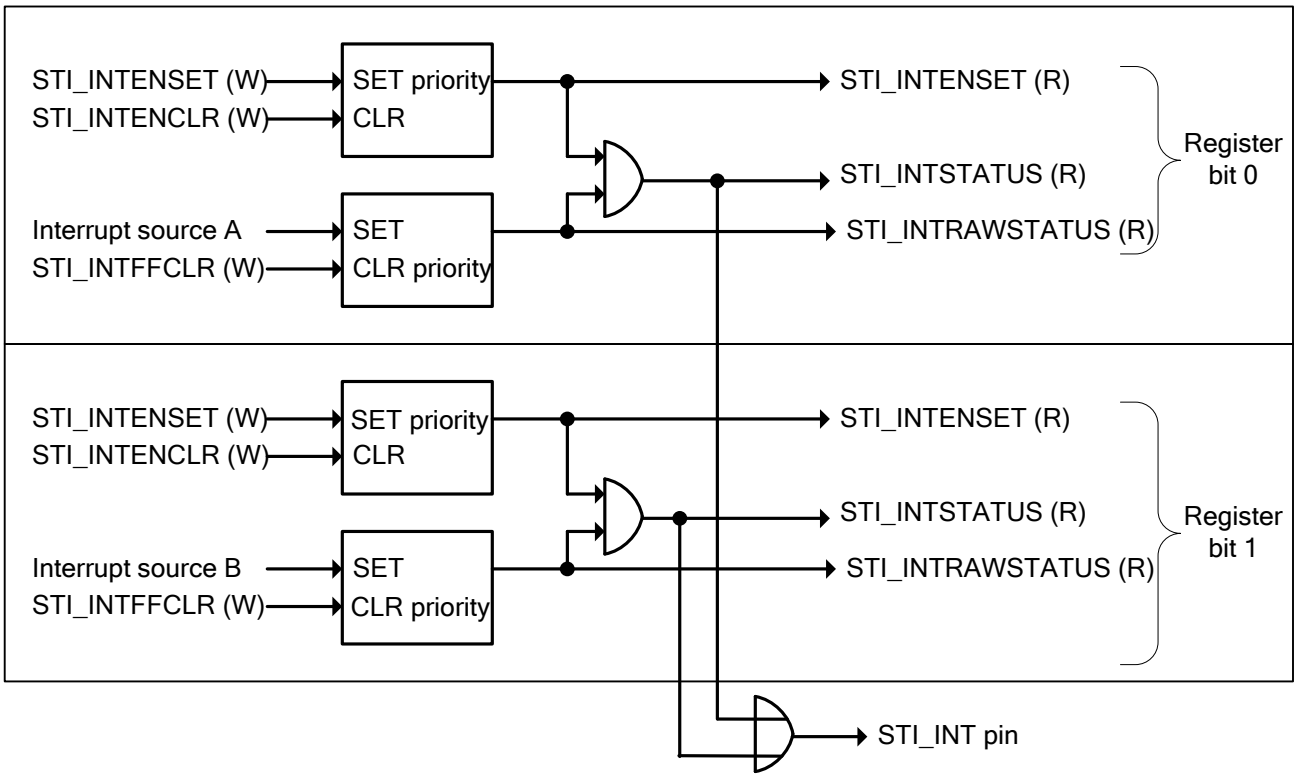


The interrupt source register must run on the timer clock to enable it to issue interrupts and hold the sources even when the bus clock is stopped.

3.5 Interrupt Signal Output

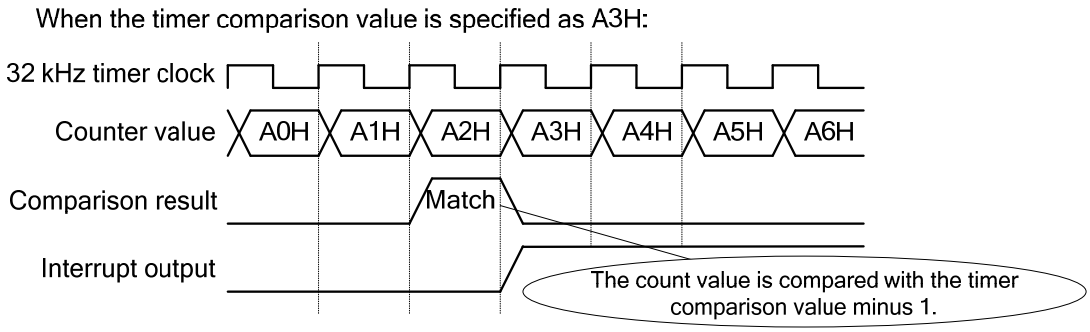
The interrupt output pin (STI_INT) outputs a signal that is the result of ORing interrupt source A and interrupt source B.

Figure 3-10. Interrupt Output



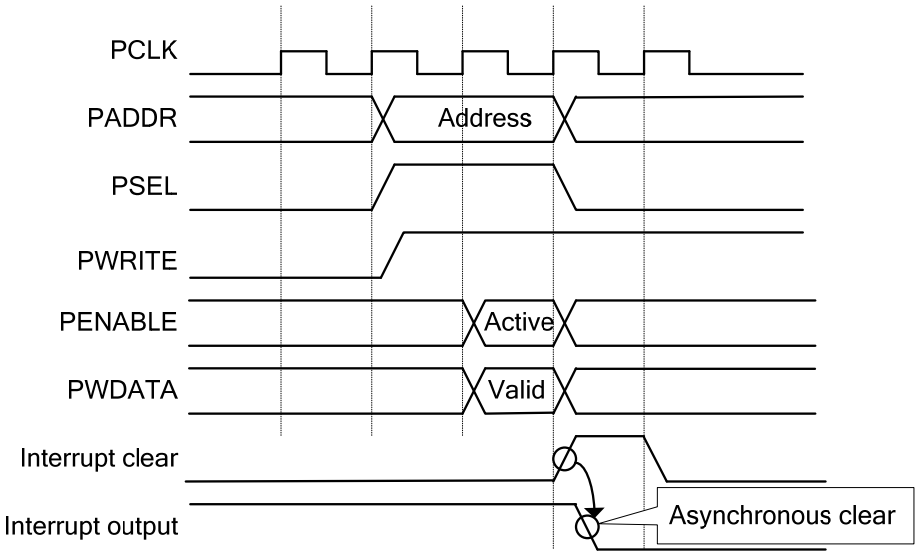
The timing at which interrupts are output is shown below.

Figure 3-11. Interrupt Output Timing



The timing at which interrupts are cleared is shown below.

Figure 3-12. Interrupt Clearance Timing



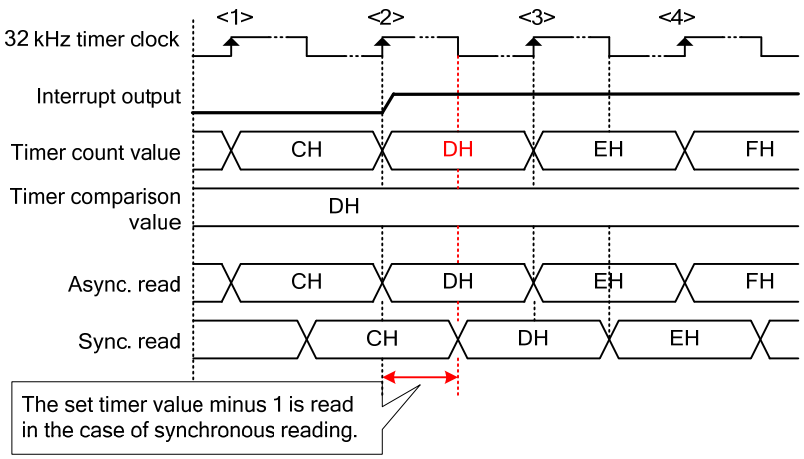
Cautions on reading the timer count value immediately after an interrupt signal is output

If the timer count value is read (synchronously) immediately after an interrupt signal is output, a value that is one less than the value set to the timer compare register will be read because the falling edge of the timer clock is synchronized with the APB bus clock.

If the timer count value is read at least half a system clock cycle after the interrupt signal is output, the same value as the value set to the timer compare register will be read.

If the timer count value is read asynchronously, the same value as the value set to the timer compare register will be read. See the figure below for details.

Figure 3-13. Timer Count Value That Is Read



Caution Interrupt signals are not output in synchronization with the bus clock.

3.6 Reading the Timer Count Value

To simplify reading the count value via the APB bus, the STI module provides the two mechanisms below for reading the timer count value. Values can also be read synchronously or asynchronously.

<1> Count value synchronization mechanism

<2> Higher/lower register data match guarantee mechanism

3.6.1 Count value synchronization mechanism (value read synchronously)

With this mechanism, the APB bus clock and timer clock are synchronized, allowing the count value to be read via the APB bus in a single operation.

The system timer value is stored in the bus clock synchronization register at the reverse phase (the falling edge of the timer clock) to the phase at which the system timer is updated (which is the rising edge of the timer clock), enabling the value to be read via the APB bus in synchronization with the clock. The timing at which the timer value is stored in the register is generated by synchronizing the falling edge of the timer clock with the APB bus clock.

In power save mode (Sleep mode), if the APB bus clock is stopped, the above synchronization mechanism will also stop. This means that the count value before the power save mode was entered will be read immediately after the system returns to normal operation. In order to read the correct count value, it is therefore necessary to wait for up to one timer clock cycle after the system returns to normal operation from power save mode.

The higher 16 bits of the synchronous timer count value register (STI_COUNT_H: 20H) has a status bit (STI_REG_SYNC) that indicates whether the correct count value was set after the system returned from power save mode.

The system references the STI_PCLK_EN signal that indicates whether the APB bus clock is being supplied from the SMU. If the APB bus clock is stopped, the STI_REG_SYNC bit is cleared, and if the APB bus clock is being supplied, the STI_REG_SYNC bit is set when the count value is synchronized.

Diagrams showing the timing of these operations when auto clock control is on and off are shown below.

Figure 3-14. When Auto Clock Control Is On

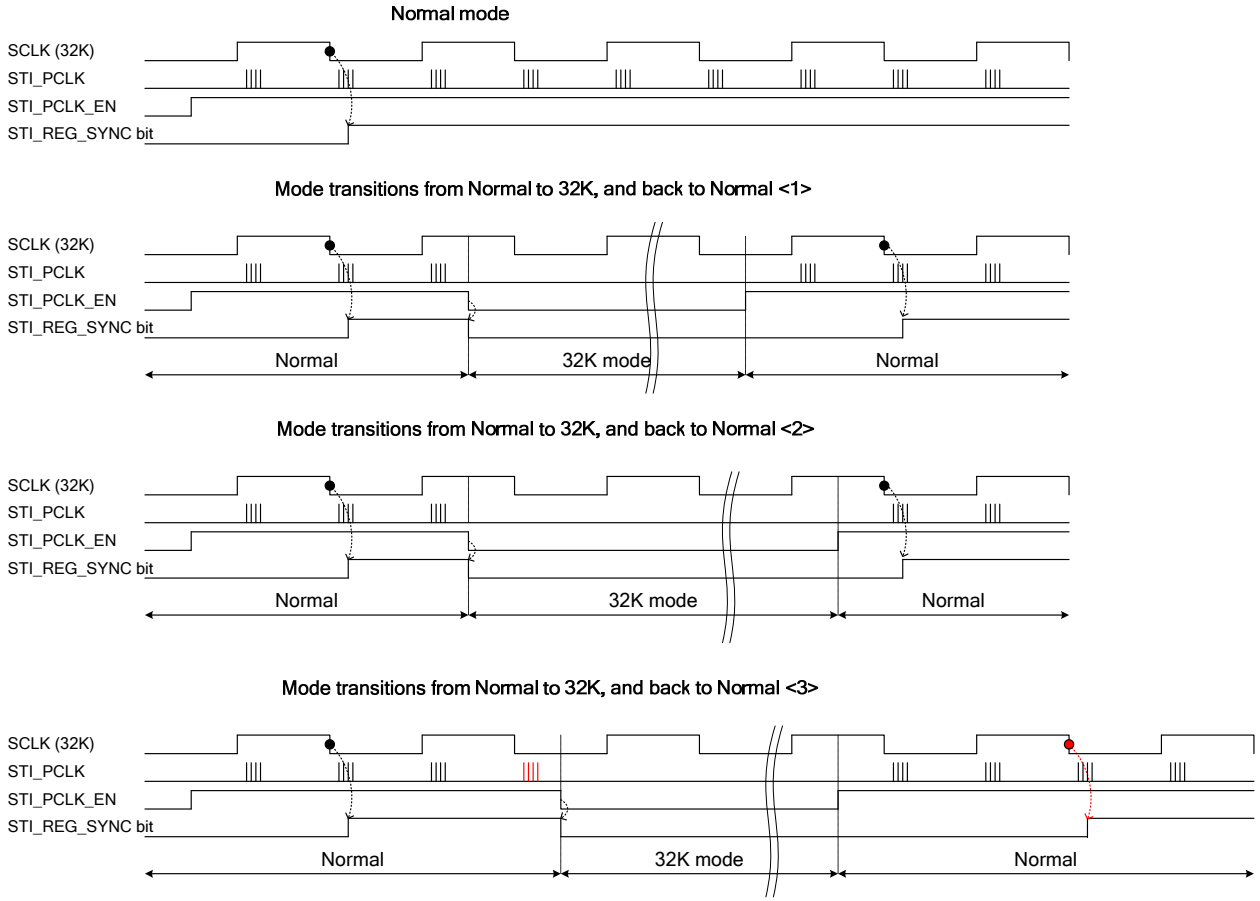
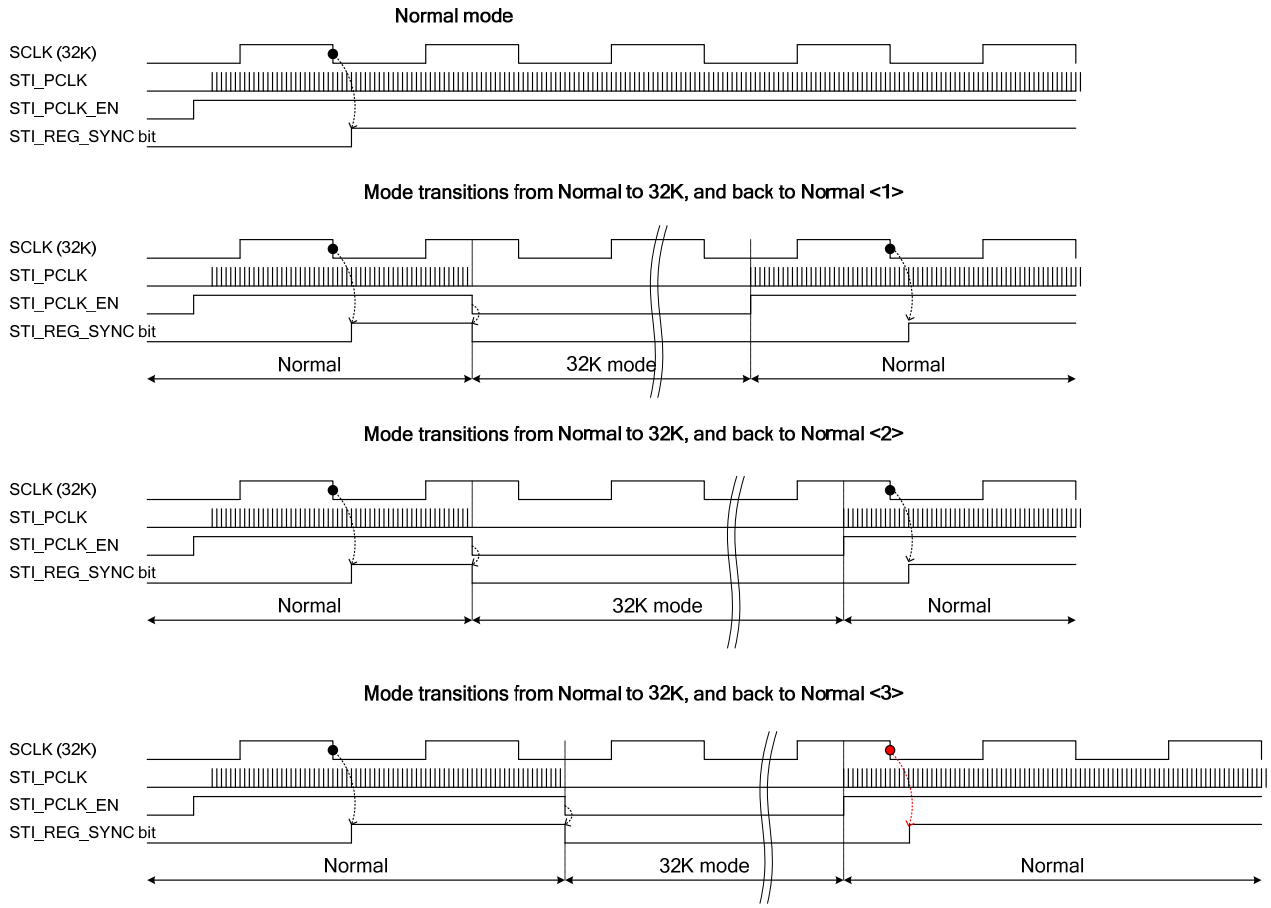


Figure 3-15. When Auto Clock Control Is Off



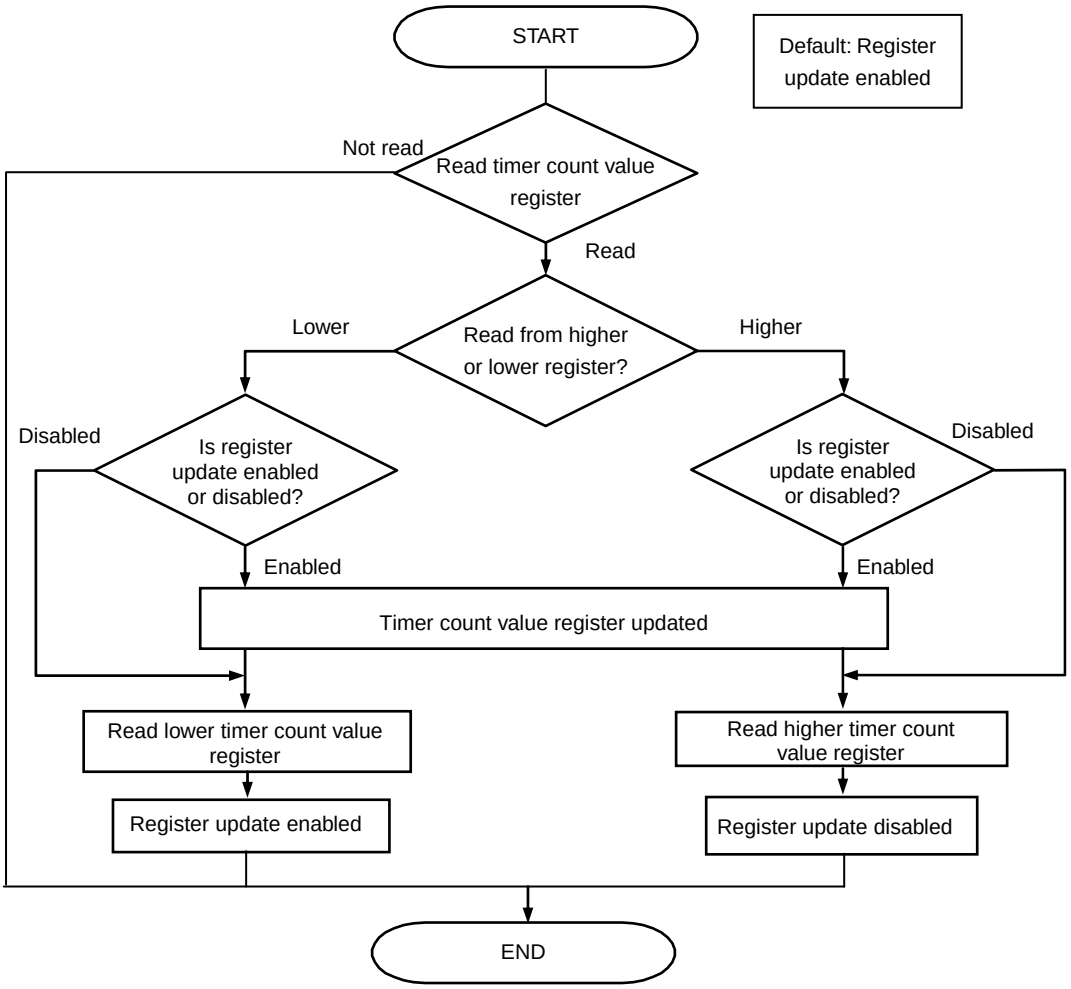
The correct count value can be obtained by making the software wait for the STI_REG_SYNC bit to be set after the system returns from power save (sleep) mode.

The STI_REG_SYNC bit is controlled based on the APB bus clock, but if the APB bus clock is stopped before the STI_PCLK_EN signal from the SMU enters the clock-stopped status, the STI_REG_SYNC bit will not be cleared correctly. The STI_REG_SYNC bit has therefore been designed to be reset asynchronously; that is, the timing does not have to be adjusted to match the SMU.

3.6.2 Higher/lower register data match guarantee mechanism

To read the 48-bit counter value via the 32-bit bus, bus access must be separated into two clock cycles. Because a time lag occurs between the two accesses, the timer continues to increment between the first and second access. As a result, values read from a higher register and a lower register might be inconsistent.
To avoid this problem, a higher/lower register data match guarantee mechanism has been implemented.
This mechanism stops synchronization of the count value between when the count value is set to the STI_COUNT_H register and when the count value is set to the STI_COUNT_L register. As a result, the count value set to the STI_COUNT_L register at the time the STI_COUNT_H register is read can be read, regardless of the timing at which the STI_COUNT_L register is read.
Synchronization can be stopped by reading the STI_COUNT_L register or by setting the STI_SYNC_OFF bit of the control register (STI_CONTROL: 00H).
If the STI_COUNT_H register is read successively, the STI_COUNT_L register is not updated from the second and subsequent reads.
If only the STI_COUNT_L register is read, the latest synchronized count value is read because synchronization is not stopped.

Figure 3-16. Timer Count Synchronous Read Operation



3.6.3 Asynchronous reading

The value of the asynchronous timer count value register is read asynchronously to the APB bus clock.

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		Page	Summary
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2.00	Jun 7, 2010	—	Incremental update from comments to the 1.0.
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