User's Manual

# SD Card Interface

User's Manual

## Multimedia Processor for Mobile Applications
## EMMA Mobile ™ EV2



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## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

# How to Use This Manual

## 1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the EMMA Mobile EV2. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

| Document Type | Description | Document Title | Document No. |
|---|---|---|---|
| Data Sheet | Hardware overview and electrical characteristics | EMMA Mobile EV2 Datasheet | R19DS0010EJxxxx |
| User's manual (1chip) | Hardware whole specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description | EMMA Mobile EV2 User's manual 1chip | R19UH0036EJxxxx |
| User's manual (module) | Hardware each macro specifications and operation description. | EMMA Mobile EV2 User's manual each module | See below |

| Document Name | Document No. | Document Name | Document No. |
|---|---|---|---|
| 1chip | R19UH0036EJxxxx | DMA Controller | R19UH0043EJxxxx |
| System Management Unit | R19UH0037EJxxxx | LP-DDR/DDR2 Controller | R19UH0039EJxxxx |
| Timer | R19UH0054EJxxxx | SD Memory Card Interface (This manual) | R19UH0061EJxxxx |
| System Timer | R19UH0055EJxxxx | SDIO Interface | R19UH0042EJxxxx |
| HD Video Decoder | R19UH0056EJxxxx | CF Card Interface | R19UH0062EJxxxx |
| Rotator | R19UH0057EJxxxx | Unified Serial Interface | R19UH0047EJxxxx |
| Resizer | R19UH0058EJxxxx | UART interface | R19UH0040EJxxxx |
| Image Composer | R19UH0038EJxxxx | USB 2.0 Host Controller | R19UH0045EJxxxx |
| LCD Interface | R19UH0044EJxxxx | USB 2.0 Function Controller | R19UH0034EJxxxx |
| ITU-R BT.656 Interface | R19UH0059EJxxxx | IIC Interface | R19UH0052EJxxxx |
| Digital Terrestrial TV Interface | R19UH0048EJxxxx | General Purpose I/O Interface | R19UH0041EJxxxx |
| Camera Interface | R19UH0060EJxxxx | Pulse Width Modulation Interface | R19UH0063EJxxxx |

4 digits of end shows the version.

## 2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names

Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.

Examples the PM03 bit in the PM0 register

P3_5 pin, VCC pin

(2) Notation of Numbers

The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.

Examples Binary: 11b or 11

Hexadecimal: EFA0h

Decimal: 1234

## 3. Register Notation

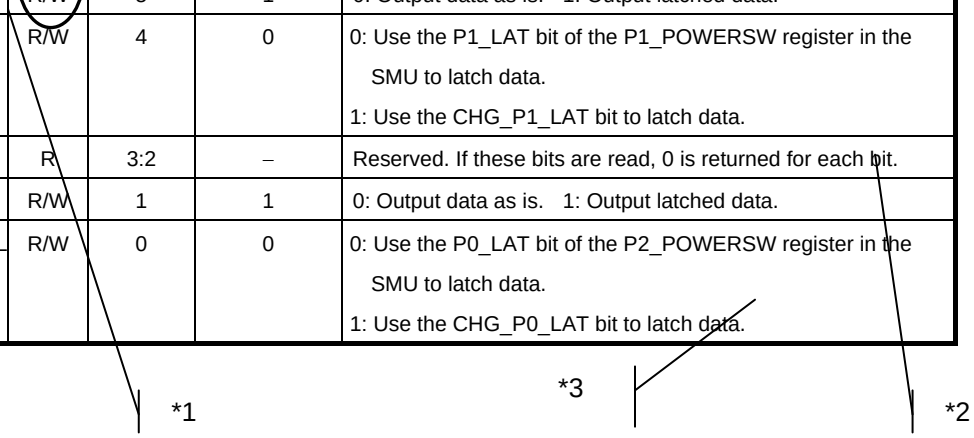
The symbols and terms used in register diagrams are described below.

**x.x.x XXX register**

This register (XXXXXXX: xxxx_xxxxh) …..

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | CHG_P1_LAT | LATCH_P1_SEL | Reserved | | CHG_P0_LAT | CHG_P0_LAT_SEL |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| LATCH_P2_SEL | R/W | 8 | 0 | 0: Use the P2_LAT bit of the P2_POWERSW register in the SMU to latch data.<br>1: Use the CHG_P2_LAT bit to latch data. |
| Reserved | R | 7:6 | – | Reserved. If these bits are read, 0 is returned for each bit. |
| CHG_P1_LAT | R/W | 5 | 1 | 0: Output data as is. 1: Output latched data. |
| LATCH_P1_SEL | R/W | 4 | 0 | 0: Use the P1_LAT bit of the P1_POWERSW register in the SMU to latch data.<br>1: Use the CHG_P1_LAT bit to latch data. |
| Reserved | R | 3:2 | – | Reserved. If these bits are read, 0 is returned for each bit. |
| CHG_P0_LAT | R/W | 1 | 1 | 0: Output data as is. 1: Output latched data. |
| CHG_P0_LAT_SEL | R/W | 0 | 0 | 0: Use the P0_LAT bit of the P2_POWERSW register in the SMU to latch data.<br>1: Use the CHG_P0_LAT bit to latch data. |




*1

R/W: Read and Write.

R: Read only.

W: Write only.

-: Nothing is assigned.

*2

Reserved bit.

Reserved bit. Set to specified value.

*3

・ Nothing is assigned.

Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.

・ Do not set to a value.

Operation is not guaranteed when a value is set.

・ Function varies according to the operating mode.

The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

## 4. List of Abbreviations and Acronyms

| Abbreviation | Full Form |
|---|---|
| ACIA | Asynchronous Communication Interface Adapter |
| bps | bits per second |
| CRC | Cyclic Redundancy Check |
| DMA | Direct Memory Access |
| DMAC | Direct Memory Access Controller |
| GSM | Global System for Mobile Communications |
| Hi-Z | High Impedance |
| IEBus | Inter Equipment Bus |
| I/O | Input/Output |
| IrDA | Infrared Data Association |
| LSB | Least Significant Bit |
| MSB | Most Significant Bit |
| NC | Non-Connect |
| PLL | Phase Locked Loop |
| PWM | Pulse Width Modulation |
| SFR | Special Function Register |
| SIM | Subscriber Identity Module |
| UART | Universal Asynchronous Receiver/Transmitter |
| VCO | Voltage Controlled Oscillator |

| Abbreviation | Full Form |
|---|---|
| AHB | Advanced High-performance Bus |
| CHG | Alternate Pin Function Switching Module |
| CPRM | Content Protection for Recordable Media |
| eMMC | Embedded Multi Media Card |
| GPIO | General Purpose I/O |
| IRQ | Interrupt Request |
| MMC | Multi Media Card |
| MP3 | MPEG Audio Layer-3 |

# Table of Contents

# 1. Overview

This module (SDC) is an SD card interface that complies with SD card interface Physical Layer Version 2.00 and SD card interface Security Version 2.00. In addition to performing I/O with a card, this module can perform hardware-based CPRM authentication, and encrypt or decrypt data. The module can also be used as an SDIO card or MMC/eMMC (4.0 or equivalent) host controller.
(CPRM is the option function.)

## 1.1 Features

The main features of the SDC module are as follows:

- Serial interface for SD cards and SDIO cards
- Supports a line width of 1 bit or 4 bits for transferring data to and from SD cards or SDIO cards.
- Supports data transfers in frame units.
- Supports CRC7 error checks on the command line and CRC16 checks (hardware) on each data bit line.
- Provides one SD card and SDIO card port.
- The data transfer buffer for SD cards is configured of two blocks of 16 bits × 256 words.
- Supports data transfers from 1 to 512 bytes.
- Two 256 word × 16 bit encryption circuit data transfer buffers, one for input and one for output
- Supports normal SD cards (transfer frequency: 25 MHz) and high-speed SD cards (transfer frequency: 50 MHz)
- The SD card transfer clock signal can be derived from the source clock signal in the SDC module (by selecting to divide the source clock frequency by 2, 4, 8, 16, …, or 512).
- A source clock is internal system clock of a SDC （SDC_CLK : A normal mode operate by 133MHz.）. The maximum clock frequency which can be used as SD transfer clock by a normal mode of EMEV is 33.25MHz.
  When SDCCLK is 133MHz (the CPU:532MHz system) : up to 33.25MHz.
  When SDCCLK is 100MHz (the CPU:400MHz system) : up to 50.00MHz.
  At most 50 MHz is covered as a SDC module.
- Supports hardware-based mutual authentication and provides a hardware implementation of an encryption algorithm using a C2 core.
- Provides a master key for performing device key encryption and decryption.
- Turns off the clock in the standby mode (when no SD card is inserted).
- Provides hardware-based CPRM.
- Supports SD Binding and SDSD (secure digital separate delivery).
- Performs hardware-based analysis of sound format headers such as MP3.
- Supports SDIP version 2.8.

# 2. Pin Functions

| Pin Name | I/O | Function | Alternate Pin Function |
|---|---|---|---|
| SD_CKO | Output | SD card clock output | – |
| SD_CKI | Input | SD card clock input | GPIO_048 |
| SD_CMD | I/O | SD card command | – |
| SD_DATA3 | I/O | SD card data bit 3 | – |
| SD_DATA2 | I/O | SD card data bit 2 | – |
| SD_DATA1 | I/O | SD card data bit 1 | – |
| SD_DATA0 | I/O | SD card data bit 0 | – |

# 3. Registers

## 3.1 Register List

The SDC registers can only be accessed by way of the AHB slave devices, and only in 32-bit units.
If register access in 16-bit or 8-bit units is attempted, it is handled as 32-bit access.

Base address: E210_0000H

(1/2)

| Address | Register Name | Register Symbol | R/W | Reset |
|---|---|---|---|---|
| 0000H | SD card command register | SDC_CMD | R/W | 0000_0000H |
| 0004H | SD card port select register | SDC_PORT | R/W | 0000_0100H |
| 0008H | SD card command parameter register 0 | SDC_ARG0 | R/W | 0000_0000H |
| 000CH | SD card command parameter register 1 | SDC_ARG1 | R/W | 0000_0000H |
| 0010H | SD card stop register | SDC_STOP | R/W | 0000_0000H |
| 0014H | SD card transfer sector count register | SDC_SECCNT | R/W | 0000_0000H |
| 0018H | SD card response register 0 | SDC_RSP0 | R | 0000_0000H |
| 001CH | SD card response register 1 | SDC_RSP1 | R | 0000_0000H |
| 0020H | SD card response register 2 | SDC_RSP2 | R | 0000_0000H |
| 0024H | SD card response register 3 | SDC_RSP3 | R | 0000_0000H |
| 0028H | SD card response register 4 | SDC_RSP4 | R | 0000_0000H |
| 002CH | SD card response register 5 | SDC_RSP5 | R | 0000_0000H |
| 0030H | SD card response register 6 | SDC_RSP6 | R | 0000_0000H |
| 0034H | SD card response register 7 | SDC_RSP7 | R | 0000_0000H |
| 0038H | SD card information register 1 | SDC_INFO1 | R/W, R | Undefined (0000_068DH) |
| 003CH | SD card information register 2 | SDC_INFO2 | R/W, R | Undefined (0000_2080H) |
| 0040H | SD card information mask register 1 | SDC_INFO1_MASK | R/W | 0000_031DH |
| 0044H | SD card information mask register 2 | SDC_INFO2_MASK | R/W | 0000_8B7FH |
| 0048H | SD card transfer clock control register | SDC_CLK_CTRL | R/W | 0000_0020H |
| 004CH | SD card transfer data size register | SDC_SIZE | R/W | 0000_0200H |
| 0050H | SD card option setting register | SDC_OPTION | R/W | 0000_00EEH |
| 0054H | Reserved | – | – | – |
| 0058H | SD card error interrupt status register 1 | SDC_ERR_STS1 | R | 0000_2000H |
| 005CH | SD card error interrupt status register 2 | SDC_ERR_STS2 | R | 0000_0000H |
| 0060H | SD card data buffer 0 register | SDC_BUF0 | R/W | Undefined |
| 0064H | Reserved | – | – | – |
| 0068H | SDIO mode setting register | SDC_SDIO_MODE | R/W | 0000_0000H |
| 006CH | SDIO information register | SDC_SDIO_INFO1 | R/W | 0000_0000H |
| 0070H | SDIO information mask register | SDC_SDIO_INFO1_MASK | R/W | 0000_C007H |
| 0074H to 01BCH | Reserved | – | – | – |

(2/2)

| Address | Register Name | Register Symbol | R/W | Reset |
|---|---|---|---|---|
| 01C0H | SDC software reset control register | SDC_SOFT_RST | R/W | 0000_0000H |
| 01C4H to 01E0H | Reserved | – | – | – |
| 0200H | SDC user register | SDC_USER | R/W, R | 0000_0004H |
| 0204H | SDC user register 2 | SDC_USER2 | R/W | 0000_0000H |
| 0208H to 020CH | Reserved | – | – | – |
| 0210H | Module reset control register | SDC_RST_CTRL | R/W | 0000_0000H |
| 0214H | AHB bus interface control register | SDC_BUSIF_CTRL | R/W, R | 0000_0000H |
| 0218H | Reserved | – | – | – |
| 021CH | DMA mask setting register | SDC_DMAMSK_CTRL | R/W | 0000_000FH |
| 0220H | SD write transfer data storage address | SDC_TXMEM_ADDR0L | R/W | 0000_0000H |
| 0224H | Reserved | – | – | – |
| 0228H | SD read transfer data storage address | SDC_RXMEM_ADDR0L | R/W | 0000_0000H |
| 022CH | Reserved | – | – | – |
| 0230H | SD sector length setting register | SDC_SECTOR_LENGTH0 | R/W | 0000_0000H |
| 0234H to 023CH | Reserved | – | – | – |
| 0240H | SD block length setting register | SDC_BLOCK_LENGTH0 | R/W | 0000_0000H |
| 0244H to 025CH | Reserved | – | – | – |
| 0260H | DMA startup register | SDC_TRANS_START | R/W | 0000_0000H |
| 0264H to 026CH | Reserved | – | – | – |
| 0270H | Interrupt mask register | SDC_INT_MSK | R/W | 0000_000FH |
| 0274H | Interrupt factor RAW register | SDC_INT_RAW | R/W | 0000_000FH |
| 0278H | Interrupt factor register | SDC_INT_ORG | R/W | 0000_000FH |
| 027CH | Interrupt factor clear register | SDC_INT_CLR | R/W | 0000_000FH |
| 0274H to 028CH | Reserved | – | – | – |
| 0290H | SD write transfer data storage address | SDC_TXMEM_ADDR0H | R/W | 0000_0000H |
| 0294H | Reserved | – | – | – |
| 0298H | SD read transfer data storage address | SDC_RXMEM_ADDR0H | R/W | 0000_0000H |
| 0300H | DMA mode SD buffer register | SDC_DMASD | R/W | 0000_0000H |

## 3.2 Register Details

### 3.2.1 SD card command register

This register (SDC_CMD: 0000H) controls the SD card commands and responses.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| MD7 | MD6 | MD5 | MD4 | MD3 | MD2 | MD1 | MD0 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| C1 | C0 | CF45 | CF44 | CF43 | CF42 | CF41 | CF40 |

(1/2)

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| MD[7:6] | R/W | 15:14 | 00b | Specify the CMD12 mode.<br>00: Automatic CMD12 transfer<br>01: Non-automatic CMD12 transfer (SDIO command) (transfer between host and SD card)<br>10: Reserved<br>11: Reserved<br>**Remark** Automatic CMD12 transfer means that CMD12 is automatically transferred according to the sector count, after which data transfer stops. |
| MD5 | R/W | 13 | 0 | Select the transfer type.<br>0: Single-block transfer<br>1: Multiple-block transfer |
| MD4 | R/W | 12 | 0 | Specify the write or read mode.<br>0: Write<br>1: Read |
| MD3 | R/W | 11 | 0 | Specify the data mode.<br>0: No data<br>1: Data is present |
| MD[2:0] | R/W | 10:8 | 000b | Specify an expansion command and the response type.<br>Command mode / Response type<br>000: Normal mode / SD cards and multimedia cards decoding command<br>001: Expansion command / Reserved<br>010: Expansion command / Reserved<br>011: Expansion command / No response<br>100: Expansion command / R1, R6, R5<br>101: Expansion command / R1b, R5b<br>110: Expansion command / R2<br>111: Expansion command / R3, R4 |

(2/2)

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| C[1:0] | R/W | 7:6 | 00b | Specify the command mode.<br>00: SD card or multimedia card command<br>01: ACMD following CMD55 of an SD card<br>10: Mutual recognition command<br>11: Reserved |
| CF[45:40] | R/W | 5:0 | 00H | Specify the command index specified for bits 45 to 40 in the SD card command format.<br>0: CF40<br>1: CF41<br>2: CF42<br>3: CF43<br>4: CF44<br>5: CF45 |

**Remark** For details about setup commands and responses, see *SD Specifications Part 1 Physical Layer Simplified Specification Ver. 2.0*.

### 3.2.2 SD card port select register

This register (SDC_PORT: 0004H) specifies the port used when multiple SD card ports are mounted.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | NP2 | NP1 | NP0 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | P1 | P0 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| Reserved | R | 15:11 | – | Reserved. If these bits are read, 0 is returned for each bit. |
| NP[2:0] | R | 10:8 | 001b | Specify the number of supported SD cards.<br>000: Setting prohibited<br>001: 1 port (default)<br>010: Setting prohibited<br>011: Setting prohibited<br>100: Setting prohibited |
| Reserved | R | 7:2 | – | Reserved. If these bits are read, 0 is returned for each bit. |
| P[1:0] | R/W | 1:0 | 00b | Select the port number of the selected SD card.<br>00: Port 0<br>01: Setting prohibited[Note]<br>10: Setting prohibited[Note]<br>11: Setting prohibited[Note] |

**Note** Operation is not guaranteed if a value other than 0 is specified for bits P1 and P0.

### 3.2.3 SD card command parameter register 0

This register (SDC_ARG0: 0008H) stores the SD card command parameters.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| CF23 | CF22 | CF21 | CF20 | CF19 | CF18 | CF17 | CF16 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CF15 | CF14 | CF13 | CF12 | CF11 | CF10 | CF9 | CF8 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| CF[23:8] | R/W | 15:0 | 0000H | Specify the parameters for the command to be transferred to the SD card. The settings of these bits correspond to bits 23 to 8 of the command format. |

**Remark** For details about setup commands and responses, see *SD Specifications Part 1 Physical Layer Simplified Specification Ver. 2.0*.

### 3.2.4 SD card command parameter register 1

This register (SDC_ARG1: 000CH) stores the SD card command parameters.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| CF39 | CF38 | CF37 | CF36 | CF35 | CF34 | CF33 | CF32 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CF31 | CF30 | CF29 | CF28 | CF27 | CF26 | CF25 | CF24 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| CF[39:24] | R/W | 15:0 | 0000H | Specify the parameters for the command to be transferred to the SD card. The settings of these bits correspond to bits 39 to 24 of the command format. |

**Remark** For details about setup commands and responses, see *SD Specifications Part 1 Physical Layer Simplified Specification Ver. 2.0*.

### 3.2.5 SD card stop register

This register (SDC_STOP: 0010H) specifies stopping SD transfers.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | SEC |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | STP |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| Reserved | R | 15:9 | 00H | Reserved. If these bits are read, 0 is returned for each bit. |
| SEC | R/W | 8 | 0 | Specify whether to enable or disable the SDC_SECCNT register.<br>0: Disable<br>1: Enable |
| Reserved | R | 7:1 | 00H | Reserved. If these bits are read, 0 is returned for each bit. |
| STP | R/W | 0 | 0 | Transfer stop bit<br>0: Do not stop transfer.<br>Clear this bit to 0 before CMD17, CMD18, CMD24, CMD27, CMD30, CMD42, CMD56, CMD43 to CMD48, ACMD18, or ACMD25 is set.<br>1: Stop transfer. |

### 3.2.6 SD card transfer sector count register

This register (SDC_SECCNT: 0014H) counts the number of transfer sectors.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| CNT15 | CNT14 | CNT13 | CNT12 | CNT11 | CNT10 | CNT9 | CNT8 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CNT7 | CNT6 | CNT5 | CNT4 | CNT3 | CNT2 | CNT1 | CNT0 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| CNT[15:0] | R/W | 15:0 | 0000H | 16-bit counter that counts the number of transfer sectors |

**Remark** If the SDC_SECCNT register is 0001H, the number of transfer sectors is 1.
If the SDC_SECCNT register is FFFFH, the number of transfer sectors is 65,535.
If the SDC_SECCNT register is 0000H, the number of transfer sectors is 65,536.

### 3.2.7 SD card response register 0

This register (SDC_RSP0: 0018H) stores the responses returned from the SD card.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| R23 | R22 | R21 | R20 | R19 | R18 | R17 | R16 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| R15 | R14 | R13 | R12 | R11 | R10 | R9 | R8 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| R[23:8] | R | 15:0 | 0000H | Store the responses returned from the SD card. The settings of these bits correspond to bits 23 to 8 of the response format. |

**Remark** For details about the response formats, see *SD Specifications Part 1 Physical Layer Simplified Specification Ver. 2.0*.

### 3.2.8 SD card response register 1

This register (SDC_RSP1: 001CH) stores the responses returned from the SD card.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| R39 | R38 | R37 | R36 | R35 | R34 | R33 | R32 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| R31 | R30 | R29 | R28 | R27 | R26 | R25 | R24 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| R[39:24] | R | 15:0 | 0000H | Store the responses returned from the SD card. The settings of these bits correspond to bits 39 to 24 of the response format. |

**Remark** For details about the response formats, see *SD Specifications Part 1 Physical Layer Simplified Specification Ver. 2.0*.

### 3.2.9 SD card response register 2

This register (SDC_RSP2: 0020H) stores the responses returned from the SD card.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| R55 | R54 | R53 | R52 | R51 | R50 | R49 | R48 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| R47 | R46 | R45 | R44 | R43 | R42 | R41 | R40 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| R[55:40] | R | 15:0 | 0000H | Store the responses returned from the SD card. The settings of these bits correspond to bits 55 to 40 of the response format. |

**Remark** For details about the response formats, see *SD Specifications Part 1 Physical Layer Simplified Specification Ver. 2.0*.

### 3.2.10 SD card response register 3

This register (SDC_RSP3: 0024H) stores the responses returned from the SD card.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| R71 | R70 | R69 | R68 | R67 | R66 | R65 | R64 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| R63 | R62 | R61 | R60 | R59 | R58 | R57 | R56 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| R[71:56] | R | 15:0 | 0000H | Store the responses returned from the SD card. The settings of these bits correspond to bits 71 to 56 of the response format. |

**Remark** For details about the response formats, see *SD Specifications Part 1 Physical Layer Simplified Specification Ver. 2.0*.

### 3.2.11 SD card response register 4

This register (SDC_RSP4: 0028H) stores the responses returned from the SD card.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| R87 | R86 | R85 | R84 | R83 | R82 | R81 | R80 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| R79 | R78 | R77 | R76 | R75 | R74 | R73 | R72 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| R[87:72] | R | 15:0 | 0000H | Store the responses returned from the SD card. The settings of these bits correspond to bits 87 to 72 of the response format. |

**Remark** For details about the response formats, see *SD Specifications Part 1 Physical Layer Simplified Specification Ver. 2.0*.

### 3.2.12 SD card response register 5

This register (SDC_RSP5: 002CH) stores the responses returned from the SD card.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| R103 | R102 | R101 | R100 | R99 | R98 | R97 | R96 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| R95 | R94 | R93 | R92 | R91 | R90 | R89 | R88 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| R[103:88] | R | 15:0 | 0000H | Store the responses returned from the SD card. The settings of these bits correspond to bits 103 to 88 of the response format. |

**Remark** For details about the response formats, see *SD Specifications Part 1 Physical Layer Simplified Specification Ver. 2.0*.

### 3.2.13 SD card response register 6

This register (SDC_RSP6: 0030H) stores the responses returned from the SD card.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| R119 | R118 | R117 | R116 | R115 | R114 | R113 | R112 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| R111 | R110 | R109 | R108 | R107 | R106 | R105 | R104 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| R[119:104] | R | 15:0 | 0000H | Store the responses returned from the SD card. The settings of these bits correspond to bits 119 to 104 of the response format. |

**Remark** For details about the response formats, see *SD Specifications Part 1 Physical Layer Simplified Specification Ver. 2.0*.

### 3.2.14 SD card response register 7

This register (SDC_RSP7: 0034H) stores the responses returned from the SD card.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| R127 | R126 | R125 | R124 | R123 | R122 | R121 | R120 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| Reserved | R | 15:8 | 0 | Reserved. If these bits are read, 0 is returned for each bit. |
| R[127:120] | R | 7:0 | 0000H | Store the responses returned from the SD card. The settings of these bits correspond to bits 127 to 120 of the response format. |

**Remark** For details about the response formats, see *SD Specifications Part 1 Physical Layer Simplified Specification Ver. 2.0*.

### 3.2.15 SD card information register 1

This register (SDC_INFO1: 0038H) indicates the status of the SDC interrupt sources.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | INFO2 | Reserved | INFO0 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| Reserved | R | 15:3 | 000H | Reserved. If these bits are read, 0 is returned for each bit. |
| INFO2 | R/W | 2 | 0 | Indicates whether the read/write access has finished.<br>0: Not finished<br>1: Finished |
| Reserved | R | 1 | 0 | Reserved. If this bit is read, 0 is returned. |
| INFO0 | R/W | 0 | 0 | Indicates whether the response has finished.<br>0: Not finished<br>1: Finished |

### 3.2.16 SD card information register 2

This register (SDC_INFO2: 003CH) indicates the error and buffer status interrupt sources of the SDC module.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| ILA | CBSY | SCLKDIVEN | Reserved | | | BWE | BRE |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DAT0 | ERR6 | ERR5 | ERR4 | ERR3 | ERR2 | ERR1 | ERR0 |

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| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| ILA | R/W | 15 | 0 | Illegal access error[Note 1]<br>0: Normal access<br>1: Illegal access error |
| CBSY | R | 14 | 0 | Command register busy<br>0: Transfer is complete.<br>1: Transfer is in progress. |
| SCLKDIVEN | R | 13 | 0 | Indicates whether the SD bus is busy transmitting commands and data.<br>0: Busy<br>1: Not busy |
| Reserved | R | 12:10 | 0H | Reserved. If these bits are read, 0 is returned for each bit. |
| BWE | R/W | 9 | 0 | Specify whether to enable writing to the SD card.<br>0: Disable<br>1: Enable (The SDC data buffer is empty.) |
| BRE | R/W | 8 | 0 | Specify whether to enable reading from the SD card.<br>0: Disable<br>1: Enable (The SDC data buffer is full.) |
| DAT0 | R | 7 | Undefined | Indicates the status of SD data line 0.<br>0: SD_DATA0 = 0<br>1: SD_DATA0 = 1 |
| ERR6 | R/W | 6 | 0 | Response timeout<br>0: No response timeout error occurred.<br>1: A response timeout error occurred (because no command response or SD_STOP response was issued for 64 SD clock cycles or more). |
| ERR5 | R/W | 5 | 0 | Invalid data buffer read error bit<br>0: No invalid data buffer read error occurred.<br>1: An invalid data buffer read error occurred (because an attempt was made to read data from the data buffer even though the data buffer was empty). |

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| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| ERR4 | R/W | 4 | 0 | Invalid data buffer write error bit<br>0: No invalid data buffer write error occurred.<br>1: An invalid data buffer write error occurred[Note 2]. |
| ERR3 | R/W | 3 | 0 | Timeout (other than a response) error<br>0: No timeout error occurred.<br>1: A timeout error occurred[Note 3]. |
| ERR2 | R/W | 2 | 0 | End error status bit<br>0: No end error occurred.<br>1: An end error occurred[Note 4]. |
| ERR1 | R/W | 1 | 0 | CRC error status bit<br>0: No CRC error occurred.<br>1: A CRC error occurred[Note 5]. |
| ERR0 | R/W | 0 | 0 | Command error status bit<br>0: No command error occurred.<br>1: A command error occurred[Note 6]. |

**Remark** For details about the response formats, see *SD Specifications Part 1 Physical Layer Simplified Specification Ver. 2.0*.

**Note** **1.** This error occurs in any of the following cases:
- If the command register is rewritten during a transfer.
- If *no response* (MD[2:0] = 011) and *data is present* (MD3 = 1) is specified for the SDC_CMD register.
- If CMD12 for which data is present is specified for the SDC_CMD register.

**2.** This error occurs in any of the following cases:
- If data is written to data buffer SDC_BUF0 when the data read or data write command status is not asserted.
- If data is written before SDC_BUF0 becomes empty during a single block write.
- If data is written to bank 1 of the data buffer before the bank becomes empty during a multiple block write.

**3.** This error occurs in any of the following five cases:
- If SDDAT0 is 0 (busy) for a longer period of time than the number of cycles specified by bits 7 to 4 of the SDC_OPTION register after an R1b response is received.
- If SDDAT0 is 0 (busy) for a longer period of time than the number of cycles specified by bits 7 to 4 of the SDC_OPTION register after the CRC status is written.
- If the CRC status is not written for a longer period of time than the number of cycles specified by bits 7 to 4 of the SDC_OPTION register after a write access.
- If SDDAT0 is 0 (busy) for a longer period of time than the number of cycles specified by bits 7 to 4 of the SDC_OPTION register after a read command is issued.
- If SDDAT0 is 0 (busy) for a longer period of time than the number of cycles specified by bits 7 to 4 of the SDC_OPTION register after an SD_STOP response is issued.

**4.** *End error* refers to an END bit error in a command response (response length), in the data read (data length), when the CRC status is written (CRC status length), or in an SD_STOP response.

**5.** *CRC error* refers to a CRC status write error, a CRC16 error in the data read, a CRC7 error in a stop response, or a CRC7 error in a response.

**6.** *Command error* refers to a command index error in a command response or in an SD_STOP response.

### 3.2.17 SD card information mask register 1

This register (SDC_INFO1_MASK: 0040H) disables the SDC interrupt sources shown in the SDC_INFO1 register.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | IMASK2 | Reserved | IMASK0 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| Reserved | R | 15:3 | 000H | Reserved. If these bits are read, 0 is returned for each bit. |
| IMASK2 | R/W | 2 | 1 | Specify whether to disable the interrupt issued when the end of a read/write access is detected.<br>0: Enable<br>1: Disable |
| Reserved | R | 1 | 0 | Reserved. If this bit is read, 0 is returned. |
| IMASK0 | R/W | 0 | 1 | Specify whether to disable the interrupt issued when the end of a response is detected.<br>0: Enable<br>1: Disable |

### 3.2.18 SD card information mask register 2

This register (SDC_INFO2_MASK: 0044H) disables the SDC interrupt sources shown in the SDC_INFO2 register.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| IMASK | Reserved | | | | | BMSK1 | BMSK0 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | EMASK6 | EMASK5 | EMASK4 | EMASK3 | EMASK2 | EMASK1 | EMASK0 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| IMASK | R/W | 15 | 1 | Specify whether to disable the illegal access interrupt.<br>0: Enable<br>1: Disable |
| Reserved | R | 14:10 | 00H | Reserved. If these bits are read, 0 is returned for each bit. |
| BMASK1 | R/W | 9 | 1 | Specify whether to disable the write enable interrupt.<br>0: Enable<br>1: Disable |
| BMASK0 | R/W | 8 | 1 | Specify whether to disable the read enable interrupt.<br>0: Enable<br>1: Disable |
| Reserved | R | 7 | 0 | Reserved. If this bit is read, 0 is returned. |
| EMASK6 | R/W | 6 | 1 | Specify whether to disable the response timeout interrupt.<br>0: Enable<br>1: Disable |
| EMASK5 | R/W | 5 | 1 | Specify whether to disable the illegal data buffer read access interrupt.<br>0: Enable<br>1: Disable |
| EMASK4 | R/W | 4 | 1 | Specify whether to disable the illegal data buffer write access interrupt.<br>0: Enable<br>1: Disable |
| EMASK3 | R/W | 3 | 1 | Specify whether to disable the timeout (other than response) interrupt.<br>0: Enable<br>1: Disable |
| EMASK2 | R/W | 2 | 1 | Specify whether to disable the end error interrupt.<br>0: Enable<br>1: Disable |
| EMASK1 | R/W | 1 | 1 | Specify whether to disable the CRC error interrupt.<br>0: Enable<br>1: Disable |
| EMASK0 | R/W | 0 | 1 | Specify whether to disable the command error interrupt.<br>0: Enable<br>1: Disable |

### 3.2.19 SD card transfer clock control register

This register (SDC_CLK_CTRL: 0048H) specifies the ratio for dividing the SD card transfer clock frequency.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | SDCLKSEL | SDCLKOFFEN | SCLKEN |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DIV7 | DIV6 | DIV5 | DIV4 | DIV3 | DIV2 | DIV1 | DIV0 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| Reserved | R | 15:11 | 00H | Reserved. If these bits are read, 0 is returned for each bit. |
| SDCLKSEL | R/W | 10 | 0 | Select the type of SD card according to the transfer clock speed.<br>0: Normal SD card<br>1: High-speed SD card |
| SDCLKOFFEN | R/W | 9 | 0 | Specify whether to enable turning on and off the SD card transfer clock signal (SDCLK).<br>0: Disable<br>1: Enable (The clock signal can be turned off when no transfers are being executed). |
| SCLKEN | R/W | 8 | 0 | Specify whether to enable the SDCLK signal.<br>0: Disable (low output)<br>1: Enable |
| DIV[7:0] | R/W | 7:0 | 20H | Specify the ratio for dividing the frequency of the SDCLK signal created from SDC_CLK.<br>0: Division by 2<br>1: Division by 4<br>2: Division by 8<br>4: Division by 16<br>8: Division by 32<br>16: Division by 64<br>32: Division by 128<br>64: Division by 256<br>128: Division by 512<br>**Caution The SDCLK signal stops if a value other the above is specified.** |

### 3.2.20 SD card transfer data size register

This register (SDC_SIZE: 004CH) specifies the transfer data size.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | LEN9 | LEN8 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LEN7 | LEN6 | LEN5 | LEN4 | LEN3 | LEN2 | LEN1 | LEN0 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| Reserved | R | 15:10 | 000H | Reserved. If these bits are read, 0 is returned for each bit. |
| LEN[9:0] | R/W | 9:0 | 200H | Specify the size of the SD data to be transferred.<br>1 to 512 bytes can be specified in byte units. Do not set this field to 0. Do not specify 513 or more bytes. |

### 3.2.21 SD card option setting register

This register (SDC_OPTION: 0050H) specifies various options.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| WIDTH | Reserved | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TOP27 | TOP26 | TOP25 | TOP24 | CTOP24 | CTOP23 | CTOP22 | CTOP21 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| WIDTH | R/W | 15 | 0 | Specify the SD data transfer bit width.<br>0: 4 bits<br>1: 1 bit |
| Reserved | R | 14:8 | 00H | Reserved. If these bits are read, 0 is returned for each bit. |
| TOP[27:24] | R/W | 7:4 | EH | Response timeout counter |
| CTOP[24:21] | R/W | 3:0 | EH | Card detection stabilization time counter |

TOP[27:24] Response timeout counter

| TOP27 | TOP26 | TOP25 | TOP24 | Description |
|---|---|---|---|---|
| 1 | 1 | 1 | 1 | Timeout testing mode |
| 1 | 1 | 1 | 0 | SD transfer clock × $2^{27}$ |
| 1 | 1 | 0 | 1 | SD transfer clock × $2^{26}$ |
| 1 | 1 | 0 | 0 | SD transfer clock × $2^{25}$ |
| 1 | 0 | 1 | 1 | SD transfer clock × $2^{24}$ |
| 1 | 0 | 1 | 0 | SD transfer clock × $2^{23}$ |
| 1 | 0 | 0 | 1 | SD transfer clock × $2^{22}$ |
| 1 | 0 | 0 | 0 | SD transfer clock × $2^{21}$ |
| 0 | 1 | 1 | 1 | SD transfer clock × $2^{20}$ |
| 0 | 1 | 1 | 0 | SD transfer clock × $2^{19}$ |
| 0 | 1 | 0 | 1 | SD transfer clock × $2^{18}$ |
| 0 | 1 | 0 | 0 | SD transfer clock × $2^{17}$ |
| 0 | 0 | 1 | 1 | SD transfer clock × $2^{16}$ |
| 0 | 0 | 1 | 0 | SD transfer clock × $2^{15}$ |
| 0 | 0 | 0 | 1 | SD transfer clock × $2^{14}$ |
| 0 | 0 | 0 | 0 | SD transfer clock × $2^{13}$ |

CTOP[24:21] Card detection stabilization time counter

| CTOP24 | CTOP23 | CTOP22 | CTOP21 | Description |
|---|---|---|---|---|
| 1 | 1 | 1 | 1 | Timeout testing mode |
| 1 | 1 | 1 | 0 | SD transfer clock × $2^{27}$ |
| 1 | 1 | 0 | 1 | SD transfer clock × $2^{26}$ |
| 1 | 1 | 0 | 0 | SD transfer clock × $2^{25}$ |
| 1 | 0 | 1 | 1 | SD transfer clock × $2^{24}$ |
| 1 | 0 | 1 | 0 | SD transfer clock × $2^{23}$ |
| 1 | 0 | 0 | 1 | SD transfer clock × $2^{22}$ |
| 1 | 0 | 0 | 0 | SD transfer clock × $2^{21}$ |
| 0 | 1 | 1 | 1 | SD transfer clock × $2^{20}$ |
| 0 | 1 | 1 | 0 | SD transfer clock × $2^{19}$ |
| 0 | 1 | 0 | 1 | SD transfer clock × $2^{18}$ |
| 0 | 1 | 0 | 0 | SD transfer clock × $2^{17}$ |
| 0 | 0 | 1 | 1 | SD transfer clock × $2^{16}$ |
| 0 | 0 | 1 | 0 | SD transfer clock × $2^{15}$ |
| 0 | 0 | 0 | 1 | SD transfer clock × $2^{14}$ |
| 0 | 0 | 0 | 0 | SD transfer clock × $2^{13}$ |

### 3.2.22 SD card error interrupt status register 1

This register (SDC_ERR_STS1: 0058H) indicates the status of the interrupts that are generated by an SDC error.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Reserved | E14 | E13 | E12 | E11 | E10 | E9 | E8 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | E5 | E4 | E3 | E2 | E1 | E0 |

(1/2)

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| Reserved | R | 15 | 0 | Reserved. If this bit is read, 0 is returned. |
| E[14:12] | R | 14:12 | 010b | Stores the CRC status in data sent from the SD card. |
| E11 | R | 11 | 0 | Indicates whether a CRC write error occurred.<br>0: Did not occur<br>1: Occurred |
| E10 | R | 10 | 0 | Indicates whether a CRC error occurred in read data.<br>0: Did not occur<br>1: Occurred |
| E9 | R | 9 | 0 | Indicates whether a CRC error occurred in an SD_STOP response.<br>0: Did not occur<br>1: Occurred |
| E8 | R | 8 | 0 | Indicates whether a CRC error occurred in a command response.<br>0: Did not occur<br>1: Occurred |
| Reserved | R | 7:6 | 0H | Reserved. If these bits are read, 0 is returned for each bit. |
| E5 | R | 5 | 0 | Indicates whether an end bit error occurred during CRC status writing.<br>0: Did not occur<br>1: Occurred |
| E4 | R | 4 | 0 | Indicates whether an end bit error occurred in read data.<br>0: Did not occur<br>1: Occurred |
| E3 | R | 3 | 0 | Indicates whether an end bit error occurred in an SD_STOP response.<br>0: Did not occur<br>1: Occurred |
| E2 | R | 2 | 0 | Indicates whether an end bit error occurred in a command response.<br>0: Did not occur<br>1: Occurred |

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| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| E1 | R | 1 | 0 | Indicates whether a command index error occurred in an SD_STOP response.<br>0: Did not occur<br>1: Occurred |
| E0 | R | 0 | 0 | Indicates whether a command index error occurred in a command response.<br>0: Did not occur<br>1: Occurred |

### 3.2.23 SD card error interrupt status register 2

This register (SDC_ERR_STS2: 005CH) indicates the status of the interrupts that are generated by an SDC error.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | E6 | E5 | E4 | E3 | E2 | E1 | E0 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| Reserved | R | 15:7 | 00H | Reserved. If these bits are read, 0 is returned for each bit. |
| E6 | R | 6 | 0 | 0: No error has occurred.<br>1: An error has occurred (because the busy status continued for a period of time longer than the number of cycles specified for SDC_OPTION[7:4], after the CRC status was written). |
| E5 | R | 5 | 0 | 0: No error has occurred.<br>1: An error has occurred (because the CRC write status was not returned for a period of time longer than the number of cycles specified for SDC_OPTION[7:4] after a write access). |
| E4 | R | 4 | 0 | 0: No error has occurred.<br>1: An error has occurred (because the read data was not returned for a period of time longer than the number of cycles specified for SDC_OPTION[7:4] after the read command was issued). |
| E3 | R | 3 | 0 | 0: No error has occurred.<br>1: An error has occurred (because the status continued for a period of time longer than the number of cycles specified for SDC_OPTION[7:4] after a SD_STOP response was returned). |
| E2 | R | 2 | 0 | 0: No error has occurred.<br>1: An error has occurred (because the busy status continued for a period of time longer than the number of cycles specified for SDC_OPTION[7:4], after an R1b response was returned). |
| E1 | R | 1 | 0 | 0: No error has occurred.<br>1: An error has occurred (because no SD_STOP response was returned for 640 SD transfer clock cycles or more). |
| E0 | R | 0 | 0 | 0: No error has occurred.<br>1: An error has occurred (because no command response was returned for 640 SD transfer clock cycles or more). |

### 3.2.24 SD card data buffer 0 register

This buffer register (SDC_BUF0: 0060H) stores the data read from and written to the SD card in the SDC module.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| BUF15 | BUF14 | BUF13 | BUF12 | BUF11 | BUF10 | BUF9 | BUF8 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| BUF7 | BUF6 | BUF5 | BUF4 | BUF3 | BUF2 | BUF1 | BUF0 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| BUF[15:0] | R/W | 15:0 | Undefined | Register for inputting and outputting data to and from the 512-byte × 2-bank data buffer |

### 3.2.25 SDIO mode setting register

This register (SDC_SDIO_MODE: 0068H) controls selection of the SDIO mode.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | C52PUB | IOABT |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | RWREQ | Reserved | IOMOD |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| Reserved | R | 15:10 | 00H | Reserved. If these bits are read, 0 is returned for each bit. |
| C52PUB | R/W | 9 | 0 | SD IO abortion (Data being transferred is guaranteed.)<br>0: Default<br>1: CMD52 is sent and the SD host holds IP transmission pending. The value before setting this bit is used as the CMD52 parameter. This bit is cleared after a CMD52 response is issued. |
| IOABT | R/W | 8 | 0 | SD IO abortion (Data being transferred is lost.)<br>This bit must be specified only during multiple IO transactions.<br>0: Default<br>1: CMD52 is sent and the SD host stops IP transmission. The value before setting this bit is used as the CMD52 parameter. |
| Reserved | R | 7:3 | 0H | Reserved. If these bits are read, 0 is returned for each bit. |
| RWREQ | R/W | 2 | 0 | Read wait request signal used during a multiple block read |
| Reserved | R/W | 1 | 0 | Reserved. If this bit is read, 0 is returned. |
| IOMOD | R/W | 0 | 0 | Specify whether to enable acknowledgment of interrupts from the SDIO card<br>0: Disable<br>1: Enable |

### 3.2.26 SDIO information register

This register (SDC_SDIO_INFO1: 006CH) indicates the status of interrupt sources when the SDC module is used in SDIO mode.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| EXWT | EXPUB52 | Reserved | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | RWRDY | C52RDY | IOIRQ |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| EXWT | R/W | 15 | 0 | Software read/write request<br>0: No request was issued.<br>1: A request was issued. |
| EXPUB52 | R/W | 14 | 0 | Software read/write source<br>0: Data was written<br>1: C52PUB was set to 1 other than when a read or write transfer was performed |
| Reserved | R | 13:3 | 000H | Reserved. If these bits are read, 0 is returned for each bit. |
| RWRDY | R/W | 2 | 0 | Indicates the read wait mode ready status.<br>0: Not ready<br>1: Ready |
| C52RDY | R/W | 1 | 0 | Indicates the CMD52 ready status.<br>0: Not ready to be issued.<br>1: Ready to be issued. |
| IOIRQ | R/W | 0 | 0 | Indicates the SDIO interrupt status.<br>0: No interrupt was issued from the SDIO card.<br>1: An interrupt was issued from the SDIO card. |

### 3.2.27 SDIO information mask register

This register (SDC_SDIO_INFO1_MASK: 0070H) disables the interrupt sources assigned to the corresponding bits in SDIO mode.

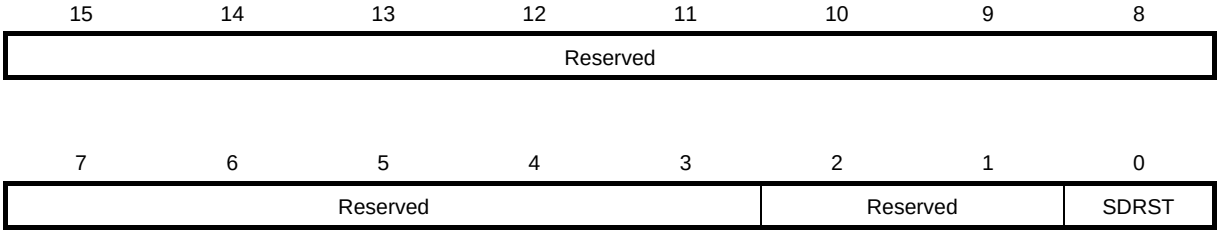
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| EXWT_MASK | EXPUB52_ MASK | Reserved | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | RWRDY_MASK | C52RDY_MASK | IOIRQ_MASK |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| EXWT_MASK | R/W | 15 | 1 | Specify whether to disable the software read/write request.<br>0: Enable<br>1: Disable |
| EXPUB52_MASK | R/W | 14 | 1 | Specify whether to disable the software read/write request.<br>0: Enable<br>1: Disable |
| Reserved | R | 13:3 | 000H | Reserved. If these bits are read, 0 is returned for each bit. |
| RWRDY_MASK | R/W | 2 | 1 | Specify whether to disable the read wait mode ready source.<br>0: Enable<br>1: Disable |
| C52RDY_MASK | R/W | 1 | 1 | Specify whether to disable the CMD52 ready source.<br>0: Enable<br>1: Disable |
| IOIRQ_MASK | R/W | 0 | 1 | Specify whether to disable the SDIO interrupt status source.<br>0: Enable<br>1: Disable |

### 3.2.28 SDC software reset control register

This register (SDC_SOFT_RST: 01C0H) is used to execute a software reset for the SDC blocks.




| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| Reserved | R | 15:3 | 0000H | Reserved. If these bits are read, 0 is returned for each bit. |
| Reserved | R | 2:1 | 01b | Reserved. If these bits are read, 1 is returned for each bit. |
| SDRST | R/W | 0 | 1 | Control resetting the SD card interface block.<br>0: Reset the SDC module.<br>1: Cancel the reset state. |

**Caution Be sure to set bits 2 and 1 to 1.**

### 3.2.29 SDC user register

This register (SDC_USER: 0200H) controls the SDC wrapper block.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| SYNC | DMASDI | DMASDO | Reserved | | | | SDCLKSTP |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CLKSTP | Reserved | | DMARQSEL2 | DMARQSEL1 | DMARQSEL0 | Reserved | CD |

(1/2)

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| SYNC | R/W | 15 | 0 | Specify AB1 synchronous or asynchronous mode.<br>0: AB1 synchronous mode<br>1: AB1 asynchronous mode |
| DMASDI | R | 14 | 0 | Indicates whether there are DMA requests for reading the SD read buffer.<br>0: No request was issued.<br>1: A request was issued. |
| DMASDO | R | 13 | 0 | Indicates whether there are DMA requests for reading the SD write buffer.<br>0: No request was issued.<br>1: A request was issued. |
| Reserved | R | 12:9 | 0H | Reserved. If these bits are read, 0 is returned for each bit. |
| SDCLKSTP | R/W | 8 | 0 | Select the SDCLK loop path.<br>0: External loop (SD_CKO → SD_CKI) Note<br>1: Setting prohibited |
| CLKSTP | R/W | 7 | 0 | Specify whether to oscillate or stop the SDC main module clock signal IMCLK.<br>0: Oscillate IMCLK.<br>1: Stop IMCLK. |
| Reserved | R | 6:5 | 0H | Reserved. If these bits are read, 0 is returned for each bit. |
| DMARQSEL[2:0] | R/W | 4:2 | 1H | Select the DMA request signal trigger.<br>100: SDC_RXDMARQ: Not assigned<br>SDC_TXDMARQ: Writing SD data<br>011: SDC_RXDMARQ: Reading SD data<br>SDC_TXDMARQ: Not assigned<br>010: SDC_RXDMARQ: Not assigned<br>SDC_TXDMARQ: Not assigned<br>001: SDC_RXDMARQ: Reading SD data<br>SDC_TXDMARQ Writing SD data<br>000: SDC_RXDMARQ: Reading SD data<br>SDC_TXDMARQ: Writing SD data |
| Reserved | R | 1 | 0 | Reserved. If this bit is read, 0 is returned. |

(2/2)

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| CD | R/W | 0 | 0 | Resets the SDC bus wrapper and DMA interrupt control blocks by using software.<br>0: Cancel the reset state.<br>1: Reset the blocks.<br>**Caution SDC_SOFT_RST has inverted logic.** |

**Note** Using of external loop

Output of SD_CKO is wired from EMEV to a SD card and it's connected to a SD card.
A loop back to EMEV, and input that to SD_CKI.
When SD_CKO and SD_CKI are connected simply, an AC specification can't sometimes be satisfied..

### 3.2.30 SDC user register 2

This register (SDC_USER2: 0204H) specifies the internal SD clock group delay and the synchronization mode.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | IntParam2 | IntParam1 | IntParam0 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | SYNCMODE |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| Reserved | R | 15:11 | 00H | Reserved. If these bits are read, 0 is returned for each bit. |
| IntParam[2:0] | R/W | 10:8 | 0H | Internal adjustment bit<br>Do not specify a value other than 000b. |
| Reserved | R | 7:1 | 00H | Reserved. If these bits are read, 0 is returned for each bit. |
| SYNCMODE | R/W | 0 | 0 | Specify the synchronization mode.<br>0: Asynchronous mode<br>1: Synchronous mode |

The signal that results from logically combining (ORing) bit 15 of the SDC use register (SDC_USER) and bit 0 of SDC use register 2 (SDC_USER2) is the synchronization signal to be used to control the circuits.

| | Bit 15 of SDC_USER | Bit 0 of SDC_USER2 | Mode Control Signal Level | Mode |
|---|---|---|---|---|
| Pattern 1 | 0 | 0 | 0 | Asynchronous mode |
| Pattern 2 | 0 | 1 | 1 | Synchronous mode |
| Pattern 3 | 1 | 0 | 1 | Synchronous mode |
| Pattern 4 | 1 | 1 | 1 | Synchronous mode |

### 3.2.31 Module reset control register

This register (SDC_RST_CTRL_CTRL: 0210H)

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | Reserved | Reserved | Reserved | F0RST | MHRST | AMRST |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| Reserved | R | 15:6 | 000H | Reserved. If these bits are read, 0 is returned for each bit. |
| Reserved | R | 5 | 0 | Reserved. If this bit is read, 0 is returned.<br>Writing in of "1" is prohibited. |
| Reserved | R | 4 | 0 | Reserved. If this bit is read, 0 is returned.<br>Writing in of "1" is prohibited. |
| Reserved | R | 3 | 0 | Reserved. If this bit is read, 0 is returned.<br>Writing in of "1" is prohibited. |
| F0RST | R/W | 2 | 0 | FIFO0 (SD R/W) control module reset<br>0 : Reset release<br>1 : Reset |
| MHRST | R/W | 1 | 0 | HOST control module reset<br>0 : Reset release<br>1 : Reset |
| AMRST | R/W | 0 | 0 | AHB master control module reset<br>0 : Reset release<br>1 : Reset |

### 3.2.32 AHB bus interface control register

This register (SDC_BUSIF_CTRL: 0214H)

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | ACCTYPE | ERR_MASTER | | BURSTMODE | | AMCEN |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| Reserved | R | 15:6 | 000H | Reserved. If these bits are read, 0 is returned for each bit. |
| ACCTYPE | R/W | 5 | 0 | Select the core access address type (This function not used)<br>0: Register setting<br>1: Value fixed (0x7F) |
| ERR_MASTER | R | 4:3 | 00b | AHB error occurrence master ID<br>00b: SD R/W transfer<br>01b: C2 input transfer<br>10b: C2 output transfer |
| BURSTMODE | R/W | 2:1 | 00b | Select the AHB master/burst transfer mode<br>00b: Single<br>01b: INCR4<br>10b: INCR8<br>11b: INCR16 |
| AMCEN | R/W | 0 | 0 | Specify the AHB master transfer.<br>0: Invalid<br>1: Valid |

### 3.2.33 DMA mask setting register

This register (SDC_DMAMSK_CTRL: 021CH)

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | DMAMSK_CCW | DMAMSK_CCR | DMAMSK_SDW | DMAMSK_SDR |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| Reserved | R | 15:4 | 000H | Reserved. If these bits are read, 0 is returned for each bit. |
| DMAMSK_CCW | R/W | 3 | 1 | Specify the mask control of C2 write transfer DMA.<br>0: Valid<br>1: Mask |
| DMAMSK_CCR | R/W | 2 | 1 | Specify the mask control of C2 read transfer DMA.<br>0: Valid<br>1: Mask |
| DMAMSK_SDW | R/W | 1 | 1 | Specify the mask control of SD write transfer DMA.<br>0: Valid<br>1: Mask |
| DMAMSK_SDR | R/W | 0 | 1 | Specify the mask control of SD read transfer DMA.<br>0: Valid<br>1: Mask |

### 3.2.34 SD write transfer data storage address

This register (SDC_TXMEM_ADDR0L: 0220H)

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| TXMEM_ADDR0[15:8] | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TXMEM_ADDR0[7:0] | | | | | | | |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| TXMEM_ADDR0 | R/W | 15:0 | 0000H | The start address (lower 16bit) when reading data from a memory, is established at the time of writing in on a SD card. |

### 3.2.35 SD read transfer data storage address

This register (SDC_RXMEM_ADDR0L: 0228H)

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RXMEM_ADDR0[15:8] | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RXMEM_ADDR0[7:0] | | | | | | | |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| RXMEM_ADDR0 | R/W | 15:0 | 0000H | The start address (lower 16bit) when writing data from a memory, is established at the time of reading in on a SD card. |

### 3.2.36 SD sector length setting register

This register (SDC_SECTOR_LENGTH0: 0230H)

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | LENGTH0[9:8] | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LENGTH0[7:0] | | | | | | | |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| Reserved | R | 15:10 | 00H | Reserved. If these bits are read, 0 is returned for each bit. |
| LENGTH0 | R/W | 9:0 | 000H | The sector length which is at the time of DMA transmission is set. |

### 3.2.37 SD block length setting register

This register (SDC_BLOCK_LENGTH0: 0240H)

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | LENGTH0[9:8] | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LENGTH0[7:0] | | | | | | | |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| Reserved | R | 15:10 | 00H | Reserved. If these bits are read, 0 is returned for each bit. |
| LENGTH0 | R/W | 9:0 | 000H | The block length which is at the time of DMA transmission is set. |

### 3.2.38 DMA startup register

This register (SDC_TRANS_START: 0260H)

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | START2 | START1 | START0 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| Reserved | R | 15:3 | 0000H | Reserved. If these bits are read, 0 is returned for each bit. |
| START2 | R/W | 2 | 0 | Specify the C2 write DMA startup.<br>0: Stop<br>1: Start |
| START1 | R/W | 1 | 0 | Specify the C2 Read DMA startup.<br>0: Stop<br>1: Start |
| START0 | R/W | 0 | 0 | Specify the SD R/W DMA startup.<br>0: Stop<br>1: Start |

### 3.2.39 Interrupt mask register

This register (SDC_INT_MSK: 0270H)

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | INTMSK3 | INTMSK2 | INTMSK1 | INTMSK0 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| Reserved | R | 15:4 | 000H | Reserved. If these bits are read, 0 is returned for each bit. |
| INTMSK3 | R/W | 3 | 1 | Specify the error occurrence interrupt mask.<br>0: No mask<br>1: Mask |
| INTMSK2 | R/W | 2 | 1 | Specify the C2 writing in completion interrupt mask.<br>0: No mask<br>1: Mask |
| INTMSK1 | R/W | 1 | 1 | Specify the C2 reading in completion interrupt mask.<br>0: No mask<br>1: Mask |
| INTMSK0 | R/W | 0 | 1 | Specify the SD R/W in completion interrupt mask.<br>0: No mask<br>1: Mask |

### 3.2.40 Interrupt factor RAW register

This register (SDC_INT_RAW: 0274H)

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | INTRAW3 | INTRAW2 | INTRAW1 | INTRAW0 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| Reserved | R | 15:4 | 000H | Reserved. If these bits are read, 0 is returned for each bit. |
| INTRAW3 | R/W | 3 | 1 | Specify the error occurrence interrupt RAW factor.<br>0: No mask<br>1: Mask |
| INTRAW2 | R/W | 2 | 1 | Specify the C2 writing in completion interrupt RAW factor.<br>0: No mask<br>1: Mask |
| INTRAW1 | R/W | 1 | 1 | Specify the C2 reading in completion interrupt RAW factor.<br>0: No mask<br>1: Mask |
| INTRAW0 | R/W | 0 | 1 | Specify the SD R/W in completion interrupt RAW factor.<br>0: No mask<br>1: Mask |

### 3.2.41 Interrupt factor register

This register (SDC_INT_ORG: 0278H)

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | INTORG3 | INTORG2 | INTORG1 | INTORG0 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| Reserved | R | 15:4 | 000H | Reserved. If these bits are read, 0 is returned for each bit. |
| INTORG3 | R/W | 3 | 1 | Specify the error occurrence interrupt factor.<br>0: No mask<br>1: Mask |
| INTORG2 | R/W | 2 | 1 | Specify the C2 writing in completion interrupt factor.<br>0: No mask<br>1: Mask |
| INTORG1 | R/W | 1 | 1 | Specify the C2 reading in completion interrupt factor.<br>0: No mask<br>1: Mask |
| INTORG0 | R/W | 0 | 1 | Specify the SD R/W in completion interrupt factor.<br>0: No mask<br>1: Mask |

### 3.2.42 Interrupt factor clear register

This register (SDC_INT_CLR: 027CH)

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | INTCLR3 | INTCLR2 | INTCLR1 | INTCLR0 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| Reserved | R | 15:4 | 000H | Reserved. If these bits are read, 0 is returned for each bit. |
| INTCLR3 | R/W | 3 | 1 | Specify the error occurrence interrupt factor clear.<br>0: No mask<br>1: Mask |
| INTCLR2 | R/W | 2 | 1 | Specify the C2 writing in completion interrupt factor clear.<br>0: No mask<br>1: Mask |
| INTCLR1 | R/W | 1 | 1 | Specify the C2 reading in completion interrupt factor clear.<br>0: No mask<br>1: Mask |
| INTCLR0 | R/W | 0 | 1 | Specify the SD R/W in completion interrupt factor clear.<br>0: No mask<br>1: Mask |

### 3.2.43 SD write transfer data storage address

This register (SDC_TXMEM_ADDR0H: 0290H)

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| TXMEM_ADDR0[31:24] | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TXMEM_ADDR0[23:16] | | | | | | | |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| TXMEM_ADDR0 | R/W | 15:0 | 0000H | The start address (upper 16bit) when reading data from a memory, is established at the time of writing in on a SD card. |

### 3.2.44 SD read transfer data storage address

This register (SDC_RXMEM_ADDR0H: 0298H)

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RXMEM_ADDR0[31:24] | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RXMEM_ADDR0[23:16] | | | | | | | |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| RXMEM_ADDR0 | R/W | 15:0 | 0000H | The start address (upper 16bit) when writing data from a memory, is established at the time of reading in on a SD card. |

### 3.2.45 DMA mode SD buffer register

This buffer register (SDC_DMASD: 0300H) is used to read or write the SD registers when the SDC module runs in DMA mode.

**Remark** If the DMA controller accesses the SDC SD read/write buffer: SDC_DMASD
If the CPU accesses the SDC SD read/write buffer: SDC_BUF0

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| SDC_ DMASD15 | SDC_ DMASD14 | SDC_ DMASD13 | SDC_ DMASD12 | SDC_ DMASD11 | SDC_ DMASD10 | SDC_ DMASD9 | SDC_ DMASD8 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SDC_ DMASD7 | SDC_ DMASD6 | SDC_ DMASD5 | SDC_ DMASD4 | SDC_ DMASD3 | SDC_ DMASD2 | SDC_ DMASD1 | SDC_ DMASD0 |

| Name | R/W | Bit No. | After Reset | Description |
|---|---|---|---|---|
| SDC_DMASD[15:0] | R/W | 15:0 | 0000H | SD buffer used during a DMA transfer |

# 4. Description of Functions

## 4.1 SD Card Data Format

Figures 4-1 and 4-2 show the timing for transferring data in 1-bit transfer mode and in 4-bit transfer mode, respectively. In 1-bit transfer mode, SDC_DATA0 is used as the data line.

**Figure 4-1. SD Card Data Format (in 1-bit Transfer Mode)**

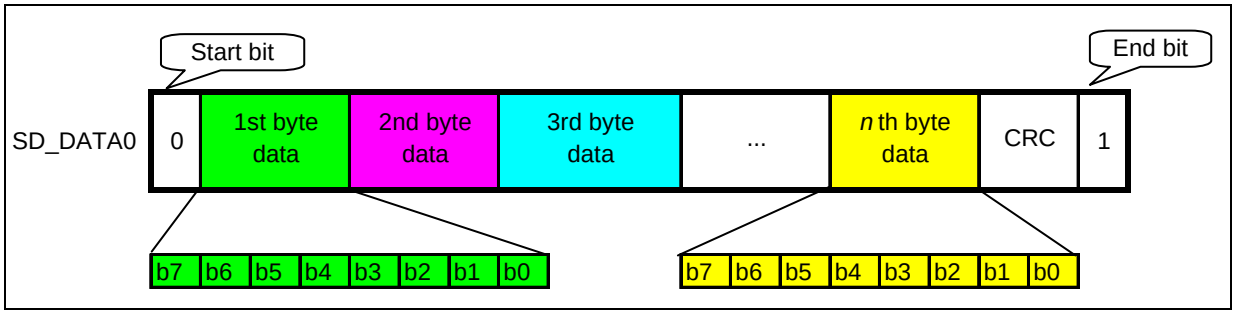
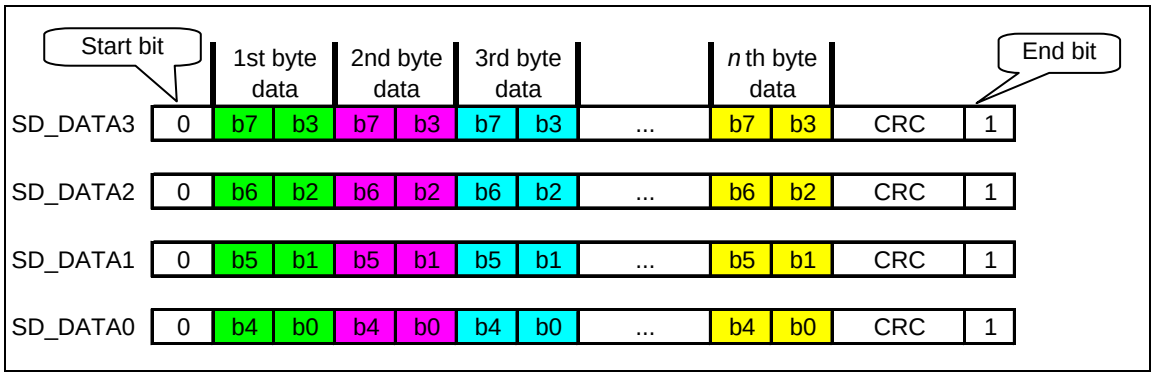



**Figure 4-2. SD Card Data Format (in 4-bit Transfer Mode)**



## 4.2 SDIO Interrupts

The SDC module supports SDIO interrupts that conform to SDIO Card Specification Ver. 1.0.
According to this specification, interrupts from an SDIO card are generated using bit 1 of the SD data line, but an SDIO card can only be detected in either of the following periods:

<1> In an asynchronous interrupt period: The SD data line is used as an interrupt line when data transfer that uses bit 1 of the SD data line is not taking place.
<2> In a synchronous interrupt period: Interrupts are output only at a certain timing when multiple blocks are transferred if the SD data line is in 4-bit mode.

The following figures show the interrupt periods when the SDC module is used with the SD data line in 1-bit mode and in 4-bit mode (for single block transfers and multiple block transfers).

The SDC module is allocated to the L1 domain. Because the power is not necessarily supplied to the L1 domain when the SDC module starts, SD_DATA1 is connected to CHG, which is allocated to the L0 domain (where the power is always on), interrupts are disabled in CHG, and a register that stores interrupt sources is implemented in CHG. Startup interrupts from the SDIO device are handled by CHG using an SDC startup interrupt feature. To enable this operation, after the SDC module starts, disable the SDC startup interrupt by using a CHG register, and then enable the SDC asynchronous interrupts to perform normal operations.

Figure 4-3 shows the overview of the SDC startup sequence when an SDIO card is detected.

**Figure 4-3. SDC Startup Sequence Triggered by SDIO Card Detection**

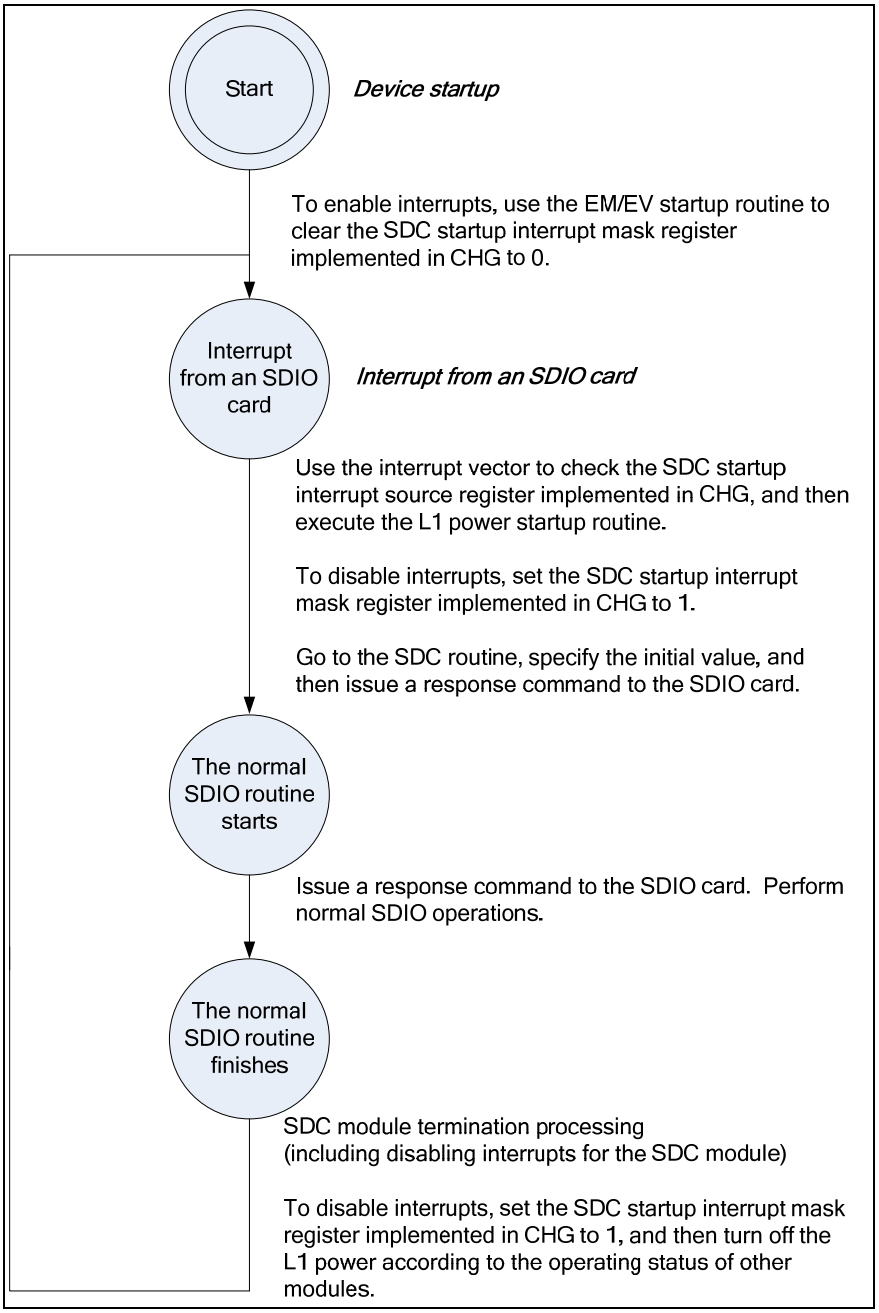
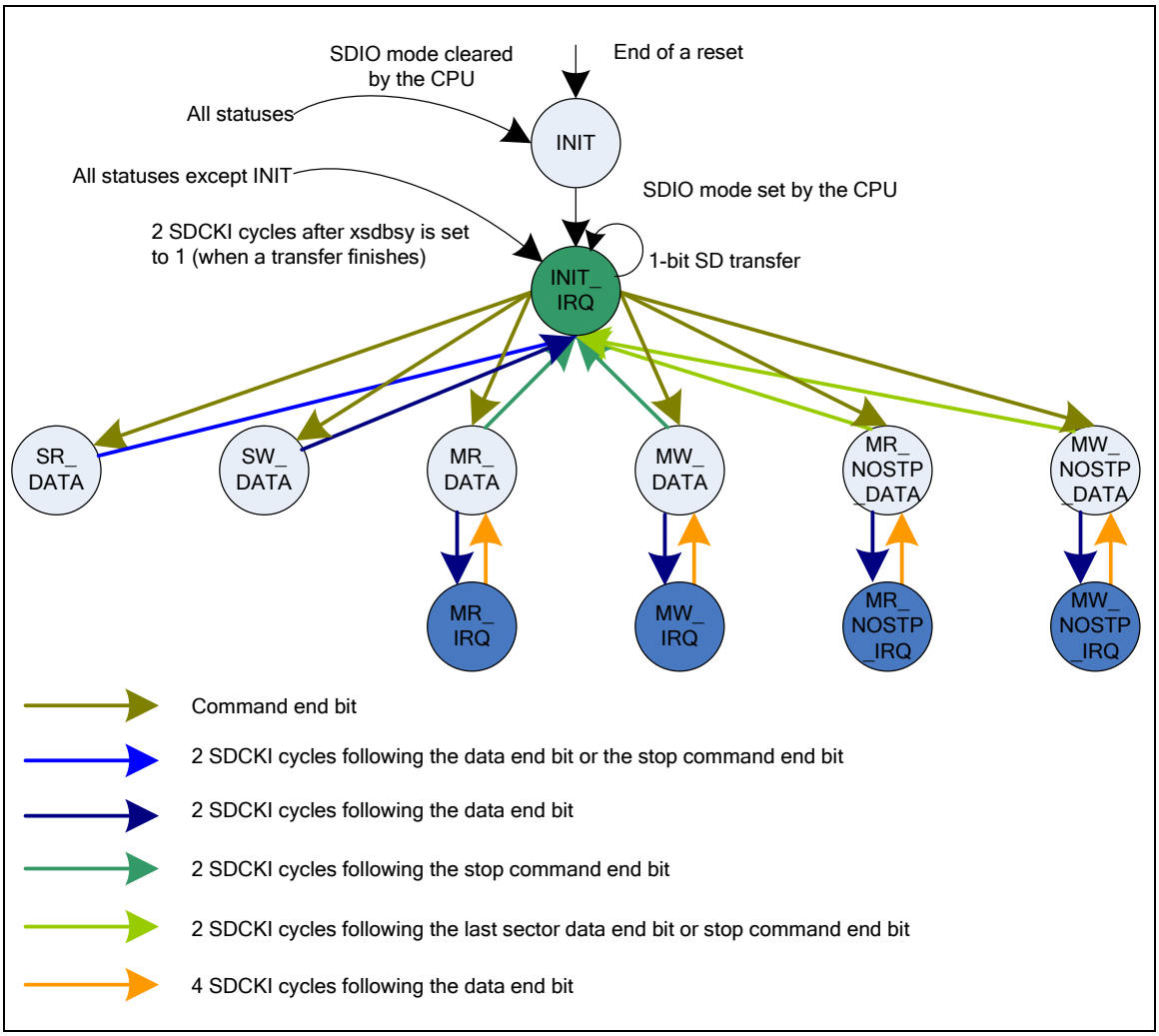


Figure 4-4 shows the status transitions.

In this figure, INIT_IRQ shows the asynchronous interrupt period, MR_IRQ, MW_IRQ, MR_NOSTP_IRQ, and MW_NOSTP_IRQ show the synchronous interrupt period, and other items show the interrupt-disabled period.

**Figure 4-4. SDC SDIO Interrupt Status Transitions**




**Remark**

| | |
|---|---|
| SR_DATA: | Single-block data read transaction |
| SW_DATA: | Single-block data write transaction |
| MR_DATA: | Multi-block data read transaction (not affected by a stop command) |
| MW_DATA: | Multi-block data write transaction (not affected by a stop command) |
| MR_NOSTP_DATA: | Multi-block data read transaction |
| MW_NOSTP_DATA: | Multi-block data write transaction |
| MR_IRQ: | Multi-block read interrupt timing (not affected by a stop command) |
| MW_IRQ: | Multi-block write interrupt timing (not affected by a stop command) |
| MR_NOSTP_IRQ: | Multi-block read interrupt timing |
| MW_NOSTP_IRQ: | Multi-block write interrupt timing |

| REVISION HISTORY | EMMA Mobile EV2 User's Manual: SD Card Interface |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
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| 2.00 | Jun 7, 2010 | — | Incremental update from comments to the 1.0. |
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# SD Card Interface

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