

# System Management Unit

User's Manual

Multimedia Processor for Mobile Applications  
EMMA Mobile™ EV2

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## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

### 1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

### 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.  
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.  
In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

### 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

### 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable.

When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

### 5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

# How to Use This Manual

## 1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the EMMA Mobile EV2. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Data Sheet	Hardware overview and electrical characteristics	EMMA Mobile EV2 Datasheet	R19DS0010EJxxxx
User's manual (1chip)	Hardware whole specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description	EMMA Mobile EV2 User's manual 1chip	R19UH0036EJxxxx
User's manual (module)	Hardware each macro specifications and operation description.	EMMA Mobile EV2 User's manual each module	See below

Document Name	Document No.	Document Name	Document No.
1chip	R19UH0036EJxxxx	DMA Controller	R19UH0043EJxxxx
System Management Unit (This manual)	R19UH0037EJxxxx	LP-DDR/DDR2 Controller	R19UH0039EJxxxx
Timer	R19UH0054EJxxxx	SD Memory Card Interface	R19UH0061EJxxxx
System Timer	R19UH0055EJxxxx	SDIO Interface	R19UH0042EJxxxx
HD Video Decoder	R19UH0056EJxxxx	CF Card Interface	R19UH0062EJxxxx
Rotator	R19UH0057EJxxxx	Unified Serial Interface	R19UH0047EJxxxx
Resizer	R19UH0058EJxxxx	UART interface	R19UH0040EJxxxx
Image Composer	R19UH0038EJxxxx	USB 2.0 Host Controller	R19UH0045EJxxxx
LCD Interface	R19UH0044EJxxxx	USB 2.0 Function Controller	R19UH0034EJxxxx
ITU-R BT.656 Interface	R19UH0059EJxxxx	IIC Interface	R19UH0052EJxxxx
Digital Terrestrial TV Interface	R19UH0048EJxxxx	General Purpose I/O Interface	R19UH0041EJxxxx
Camera Interface	R19UH0060EJxxxx	Pulse Width Modulation Interface	R19UH0063EJxxxx

4 digits of end shows the version.

## 2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

### (1) Register Names, Bit Names, and Pin Names

Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.

Examples      the PM03 bit in the PM0 register  
                  P3\_5 pin, VCC pin

### (2) Notation of Numbers

The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.

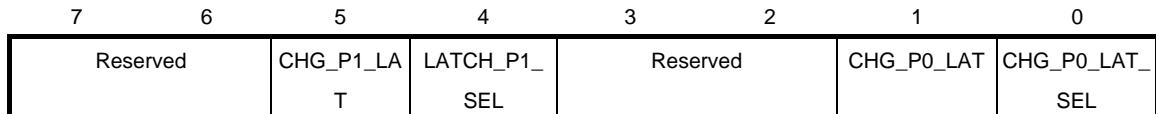
Examples      Binary: 11b or 11  
                  Hexadecimal: EFA0h  
                  Decimal: 1234

### 3. Register Notation

The symbols and terms used in register diagrams are described below.

#### X.X.X XXX register

This register (XXXXXXXX: xxxx\_xxxxh) .....



Name	R/W	Bit No.	After Reset	Description
LATCH_P2_SEL	R/W	8	0	0: Use the P2_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P2_LAT bit to latch data.
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P1_LAT	R/W	5	1	0: Output data as is. 1: Output latched data.
LATCH_P1_SEL	R/W	4	0	0: Use the P1_LAT bit of the P1_POWERSW register in the SMU to latch data. 1: Use the CHG_P1_LAT bit to latch data.
Reserved	R	3:2	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P0_LAT	R/W	1	1	0: Output data as is. 1: Output latched data.
CHG_P0_LAT_SEL	R/W	0	0	0: Use the P0_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P0_LAT bit to latch data.

\*1

\*3

\*2

\*1

R/W: Read and Write.

R: Read only.

W: Write only.

–: Nothing is assigned.

\*2

Reserved bit.

Reserved bit. Set to specified value.

\*3

- Nothing is assigned.

Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.

- Do not set to a value.

Operation is not guaranteed when a value is set.

- Function varies according to the operating mode.

The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

#### 4. List of Abbreviations and Acronyms

<b>Abbreviation</b>	<b>Full Form</b>
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Register
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

<b>Abbreviation</b>	<b>Full Form</b>
AFS	Anti Fuse
AHB	Advanced High-performance Bus
CAM	Camera interface module
IMC	Image Composer
M2M	Memory to Memory
MEMC	Memory Controller
NTS	National Television System
P2M	Peripheral to Memory
ROT	Rotator
SIO	Serial Input / Output
SIZ	Resizer
STI	System Timer
USI	Unified Serial Interface

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## 1. Overview

Note : The following word changes the expression for the convenience.

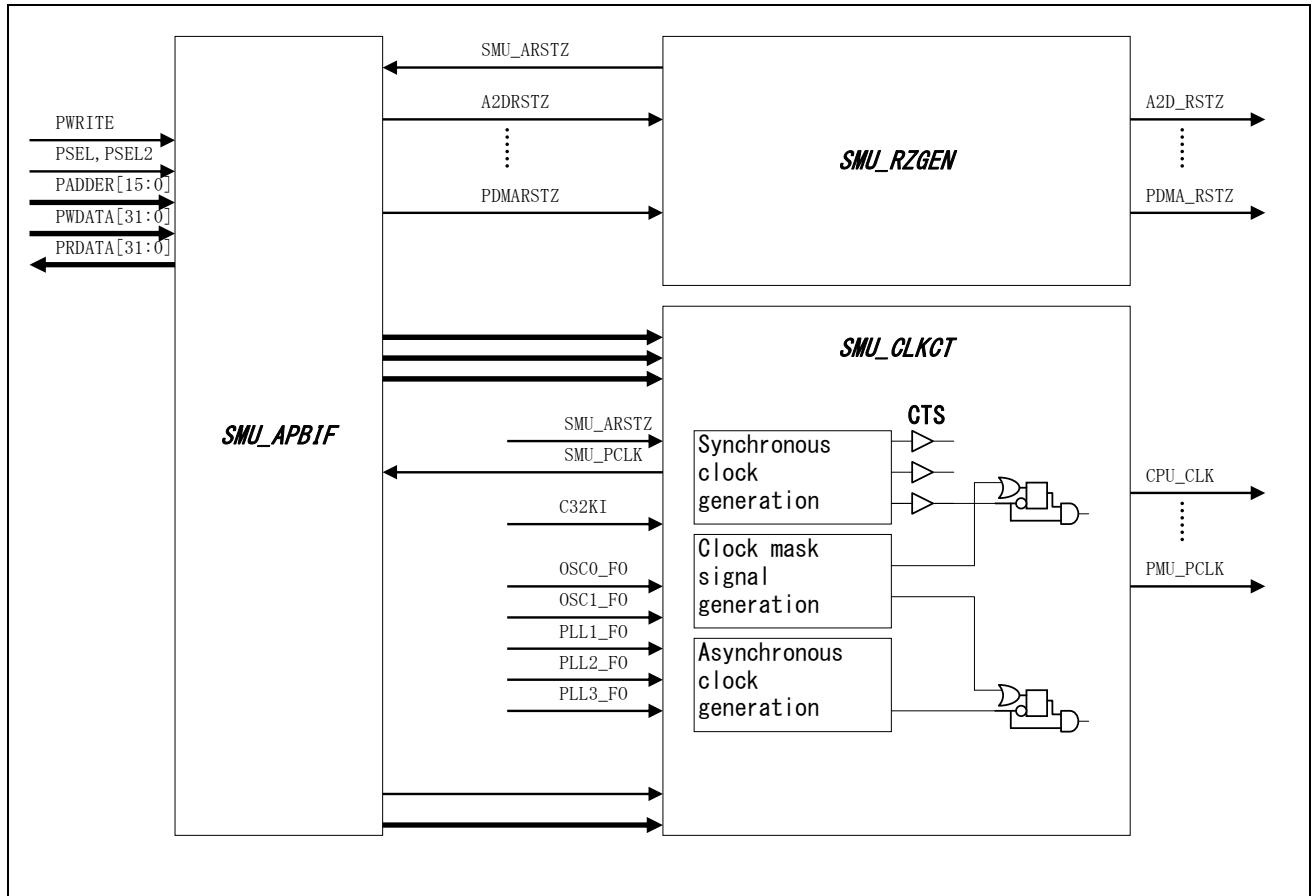
- UART0 -> USIA\_U0 or USIAU0
- UART1 -> USIB\_U1 or USIBU1
- UART2 -> USIB\_U2 or USIBU2
- UART3 -> USIB\_U3 or USIBU3
  
- SIO0 of USIA -> USIA\_S0 or USIAS0
- SIO1 of USIA -> USIA\_S1 or USIAS1
- SIO2 of USIB -> USIB\_S2 or USIBS2
- SIO3 of USIB -> USIB\_S3 or USIBS3
- SIO4 of USIB -> USIB\_S4 or USIBS4
- SIO5 of USIB -> USIB\_S5 or USIBS5

### 1.1 Features

- During operation, a 32.768 kHz system clock is input, and this can be multiplied by up to 7,000 (for a frequency of 229.376 MHz, which is expressed as 230 MHz below) when selecting a clock.
- Clock generation and gated clock control are performed.
- For clocks that require synchronization, a clock is generated by dividing the input 32.768 kHz system clock with the clock generated using OSC0, OSC1, PLL1, PLL2, PLL3, or PLL4 as the reference.
- Registers can be set up to individually control whether to supply clocks to each macro.
- A clock generated by dividing the PLL output is used in the low frequency mode.
- A clock is supplied while receiving a clock request signal from a master module (such as an LCD, IMC, or CAM).
- A clock frequency determined by dividing the clock source frequency is automatically switched to if there is no longer a clock request from a master module.

## 1.2 Function Block Diagram

Figure 1-1. Function Block Diagram



## 2. Pin Functions

Pin Name	I/O Type	Description	Alternate Pin Function
PONDET	Input	Power-on reset	–
SRESETB	Input	System reset	–
C32K	Input	32.768 kHz clock	–

## 3. Registers

### 3.1 Register List

Do not write the reserved registers. An undefined value is returned for a read access.

Do not write any value other than 0 to reserved bits in each register.

These registers are accessed can only be accessed in 32-bit units.

Base address: E011\_0000H

Address	Register Name	Symbol	R/W	After Reset
S0 domain registers				
0000H	CPU reset control register 0	CPU_RSTCTRL0	R/W	0000_001FH
0004H	CPU reset control register 1	CPU_RSTCTRL1	R/W	0000_0003H
0008H	Reserved	-	-	-
000CH	GIO reset control register	GIO_RSTCTRL	R/W	0000_0000H
0010H	INTA reset control register	INTA_RSTCTRL	R/W	0000_0001H
0014H	CHG reset control register	CHG_RSTCTRL	R/W	0000_0001H
0018H	CHG1 reset control register	CHG1_RSTCTRL	R/W	0000_0000H
001CH	BUS0 reset control register	BUS0_RSTCTRL	R/W	0000_0001H
0020H	BUS1 reset control register	BUS1_RSTCTRL	R/W	0000_0001H
0024H	PBL0 reset control register	PBL0_RSTCTRL	R/W	0000_0001H
0028H	PBL1 reset control register	PBL1_RSTCTRL	R/W	0000_0001H
002CH	AHB reset control register	AHB_RSTCTRL	R/W	0000_0001H
0030H	P2M reset control register	P2M_RSTCTRL	R/W	0000_0000H
0034H	M2P reset control register	M2P_RSTCTRL	R/W	0000_0000H
0038H	M2M reset control register	M2M_RSTCTRL	R/W	0000_0000H
003CH	PMU reset control register	PMU_RSTCTRL	R/W	0000_0000H
0040H	SRC reset control register	SRC_RSTCTRL	R/W	0000_0001H
0044H	ROM reset control register	ROM_RSTCTRL	R/W	0000_0001H
0048H	AB0 reset control register	AB0_RSTCTRL	R/W	0000_0001H
004CH	MEMC reset control register	MEMC_RSTCTRL	R/W	0000_0000H
0050H	LCD reset control register	LCD_RSTCTRL	R/W	0000_0000H
0054H	IMC reset control register	IMC_RSTCTRL	R/W	0000_0000H
0058H	IMCW reset control register	IMCW_RSTCTRL	R/W	0000_0000H
005CH	SIZ reset control register	SIZ_RSTCTRL	R/W	0000_0000H
0060H	ROT reset control register	ROT_RSTCTRL	R/W	0000_0000H
0064H	Reserved	-	-	-
0068H	AVE reset control register	AVE_RSTCTRL	R/W	0000_0000H
006CH	A3D reset control register	A3D_RSTCTRL	R/W	0000_0000H
0070H	DTV reset control register	DTV_RSTCTRL	R/W	0000_0000H
0074H	NTS reset control register	NTS_RSTCTRL	R/W	0000_0000H
0078H	CAM reset control register	CAM_RSTCTRL	R/W	0000_0000H
007CH to	Reserved	-	-	-

Address	Register Name	Symbol	R/W	After Reset
0084H				
0088H	PWM reset control register	PWM_RSTCTRL	R/W	0000_0000H
008CH	USIAS0 reset control register	USIAS0_RSTCTRL	R/W	0000_0000H
0090H	USIAS1 reset control register	USIAS1_RSTCTRL	R/W	0000_0000H
0094H	USIAU0 reset control register	USIAU0_RSTCTRL	R/W	0000_0000H
0098H	Reserved	-	-	-
009CH	USIBS2 reset control register	USIBS2_RSTCTRL	R/W	0000_0000H
00A0H	USIBS3 reset control register	USIBS3_RSTCTRL	R/W	0000_0000H
00A4H	USIBS4 reset control register	USIBS4_RSTCTRL	R/W	0000_0000H
00A8H	USIBS5 reset control register	USIBS5_RSTCTRL	R/W	0000_0000H
00ACh	USIBU1 reset control register	USIBU1_RSTCTRL	R/W	0000_0000H
00B0H	USIBU2 reset control register	USIBU2_RSTCTRL	R/W	0000_0000H
00B4H	USIBU3 reset control register	USIBU3_RSTCTRL	R/W	0000_0000H
00B8H	Reserved	-	-	-
00BCH	SDIO0 reset control register	SDIO0_RSTCTRL	R/W	0000_0000H
00C0H	SDIO1 reset control register	SDIO1_RSTCTRL	R/W	0000_0000H
00C4H	SDIO2 reset control register	SDIO2_RSTCTRL	R/W	0000_0000H
00C8H	SDC reset control register	SDC_RSTCTRL	R/W	0000_0000H
00CCH	Reserved	-	-	-
00D0H	CFI reset control register	CFI_RSTCTRL	R/W	0000_0000H
00D4H to 00D8H	Reserved	-	-	-
00DCH	IIC0 reset control register	IIC0_RSTCTRL	R/W	0000_0000H
00E0H	IIC1 reset control register	IIC1_RSTCTRL	R/W	0000_0000H
00E4H	USB0 reset control register	USB0_RSTCTRL	R/W	0000_0000H
00E8H	USB1 reset control register	USB1_RSTCTRL	R/W	0000_0000H
00ECH	TI0 reset control register	TI0_RSTCTRL	R/W	0000_0000H
00F0H	TI1 reset control register	TI1_RSTCTRL	R/W	0000_0000H
00F4H	TI2 reset control register	TI2_RSTCTRL	R/W	0000_0000H
00F8H	TI3 reset control register	TI3_RSTCTRL	R/W	0000_0000H
00FCH	TW0 reset control register	TW0_RSTCTRL	R/W	0000_0000H
0100H	TW1 reset control register	TW1_RSTCTRL	R/W	0000_0000H
0104H	TW2 reset control register	TW2_RSTCTRL	R/W	0000_0000H
0108H	TW3 reset control register	TW3_RSTCTRL	R/W	0000_0000H
010CH	TG0 reset control register	TG0_RSTCTRL	R/W	0000_0000H
0110H	TG1 reset control register	TG1_RSTCTRL	R/W	0000_0000H
0114H	TG2 reset control register	TG2_RSTCTRL	R/W	0000_0000H
0118H	TG3 reset control register	TG3_RSTCTRL	R/W	0000_0000H
011CH	TG4 reset control register	TG4_RSTCTRL	R/W	0000_0000H
0120H	TG5 reset control register	TG5_RSTCTRL	R/W	0000_0000H
0124H	STI reset control register	STI_RSTCTRL	R/W	0000_0000H
0128H	Reserved	-	-	-
012CH	AFS reset control register	AFS_RSTCTRL	R/W	0000_0000H

Address	Register Name	Symbol	R/W	After Reset
0130H to 013CH	Reserved	-	-	-
0140H	TW4 reset control register	TW4_RSTCTRL	R/W	0000_0000H
0144H	Reserved	-	-	-
0148H	PDMA reset control register	PDMA_RSTCTRL	R/W	0000_0000H
014CH to 0150H	Reserved	-	-	-
0154H	CPU0 safe reset control register	CPU_SAFE_RESET0	R/W	0000_001FH
0158H	CPU1 safe reset control register	CPU_SAFE_RESET1	R/W	0000_0003H
015CH	Reserved	-	-	-
0160H	USB0 safe reset control register	USB0_SAFE_RESET	R/W	0000_0001H
0164H	USB1 safe reset control register	USB1_SAFE_RESET	R/W	0000_0001H
0168H	DTV safe reset control register	DTV_SAFE_RESET	R/W	0000_0001H
016CH	CFI safe reset control register	CFI_SAFE_RESET	R/W	0000_0001H
0170H	SDC safe reset control register	SDC_SAFE_RESET	R/W	0000_0001H
0174H	SDIO0 safe reset control register	SDIO0_SAFE_RESET	R/W	0000_0001H
0178H	SDIO1 safe reset control register	SDIO1_SAFE_RESET	R/W	0000_0001H
017CH	SDIO2 safe reset control register	SDIO2_SAFE_RESET	R/W	0000_0001H
0180H	USIA safe reset control register	USIA_SAFE_RESET	R/W	0000_0001H
0184H	USIB safe reset control register	USIB_SAFE_RESET	R/W	0000_0001H
0188H	Reserved	-	-	-
018CH	CAM safe reset control register	CAM_SAFE_RESET	R/W	0000_0001H
0190H to 0198H	Reserved	-	-	-
019CH	AHB safe reset control register	AHB_SAFE_RESET	R/W	0000_0001H
01A0H	A3D safe reset control register	A3D_SAFE_RESET	R/W	0000_0001H
01A4H	AVE safe reset control register	AVE_SAFE_RESET	R/W	0000_0001H
01A8H	SIZ safe reset control register	SIZ_SAFE_RESET	R/W	0000_0001H
01ACH	ROT safe reset control register	ROT_SAFE_RESET	R/W	0000_0001H
01B0H	IMC safe reset control register	IMC_SAFE_RESET	R/W	0000_0001H
01B4H	IMCW safe reset control register	IMCW_SAFE_RESET	R/W	0000_0001H
01B8H	M2M safe reset control register	M2M_SAFE_RESET	R/W	0000_0001H
01BCH	M2P safe reset control register	M2P_SAFE_RESET	R/W	0000_0001H
01C0H	P2M safe reset control register	P2M_SAFE_RESET	R/W	0000_0001H
01C4H	Reserved	-	-	-
01C8H	Reset clock control specification register	RSTZ_CLKREQ	R/W	1F1F_1F1FH
01CCH	Reserved	-	-	-
01D0H	Watchdog timer forced reset control register	WDT_INT_RESET	R/W	0000_0000H
01D4H to 01D8H	Reserved	-	-	-
01DCH	Software interrupt source setting register	SFTWARE_INTGEN	R	0000_0000H
01E0H	Interrupt status register	INT_STATUS	R	0000_0000H
01E4H	Interrupt raw status register	INT_RAW_STATUS	R	0000_0000H
01E8H	Interrupt enable set register	INT_ENSET	R/W	0000_0000H

Address	Register Name	Symbol	R/W	After Reset
01ECH	Interrupt enable clear register	INT_ENCLR	R	0000_0000H
01F0H	Interrupt clear register	INT_CLEAR	R	0000_0000H
01F4H to 01FCH	Reserved	-	-	-
0200H	System PLL1 setting register 0	PLL1CTRL0	R/W	0001_04DDH
0204H	System PLL1 setting register 1	PLL1CTRL1	R/W	0000_00FFH
0208H	System PLL2 setting register 0	PLL2CTRL0	R/W	0000_0079H
020CH	System PLL2 setting register 1	PLL2CTRL1	R/W	0000_00FFH
0210H	System PLL3 setting register 0	PLL3CTRL0	R/W	0000_0037H
0214H	System PLL3 setting register 1	PLL3CTRL1	R/W	0000_0000H
0218H	PLL4 serial clock setting register 0	PLL4CTRL0	R/W	0000_0079H
021CH	PLL4 serial clock setting register 1	PLL4CTRL1	R/W	0000_00FFH
0220H	System OSC0 setting register	OSC0CTRL1	R/W	0000_00FFH
0224H	System OSC1 setting register	OSC1CTRL1	R/W	0000_00FFH
0228H	PLL lockup time setting register 0	PLLLOCKTIME0	R/W	0022_0022H
022CH	PLL lockup time setting register 1	PLLLOCKTIME1	R/W	0022_0032H
0230H	OSC lockup time setting register	OSCLKTIME	R/W	0022_0022H
0234H	PLL status register	PLL_STATUS	R	0000_0000H
0238H	ROSC setting register	ROSCCTRL1	R/W	0000_0000H
023CH to 0244H	Reserved	-	-	-
0248H	OSC setting register	OSC_CX	R/W	0000_0000H
024CH to 02ECH	Reserved	-	-	-
02F0H	Automatic PLL standby mode register	AUTO_PLL_STANDBY	R/W	0000_0002H
02F4H	Automatic mode transition enable register	AUTO_MODE_EN	R/W	0000_0000H
02F8H to 02FCH	Reserved	-	-	-
0300H	Clock mode select register	CLK_MODE_SEL	R/W	0000_0F00H
0304H	SMU-MEMC handshaking switch register	MEMC_HAND_SHAKE_FAKE	R/W	0000_0000H
0308H to 0318H	Reserved	-	-	-
031CH	PLL select register	CKMODE_PLLSEL	R/W	D00C_0000H
0320H	Normal mode A clock frequency division setting register	NORMALA_DIV	R/W	0531_5100H
0324H	Normal mode B clock frequency division setting register	NORMALB_DIV	R/W	0531_5100H
0328H	Normal mode C clock frequency division setting register	NORMALC_DIV	R/W	0531_5100H
032CH	Normal mode D clock frequency division setting register	NORMALD_DIV	R/W	0531_5100H
0330H	Power-on mode clock frequency division setting register	POWERON_DIV	R/W	0777_7707H
0334H	Economy mode clock frequency division setting register	ECONOMY_DIV	R/W	0531_5100H
0338H	Sleep mode clock frequency division setting register	SLEEP_DIV	R/W	0555_5500H
033CH to 034CH	Reserved	-	-	-
0350H	MEMC_CLK270 switch register	MEMCCLK270_SEL	R/W	0000_0000H

Address	Register Name	Symbol	R/W	After Reset
0354H	Reserved	-	-	-
0358H	CPU_CLK synchronous/asynchronous switch register	CPUCLK_SYNCSET	R/W	0000_0101H
035CH	CPU_CLK source clock select register	CPUCLK_ASYNC_MOD_E	R/W	0000_0100H
0360H	FLASHCLK delay adjustment register	FLA_CLK_DLY	R/W	0000_1000H
0364H	FLASHCLK stop status setting register	FLASHCLK_CTRL	R/W	0000_0000H
0368H	DSP_CLK source clock select register	DSPCLK_ASYNC_MOD_E	R/W	0001_0000H
036CH to 037CH	Reserved	-	-	-
0380H	AHB macro clock control register 0	AHBCLKCTRL0	R/W	0000_0000H
0384H	AHB macro clock control register 1	AHBCLKCTRL1	R/W	0000_0000H
0388H	AHB macro clock control register 2	AHBCLKCTRL2	R/W	0000_0000H
038CH	AHB macro clock control register 3	AHBCLKCTRL3	R/W	0000_0000H
0390H	APB macro clock control register 0	APBCLKCTRL0	R/W	1173_0331H
0394H	APB macro clock control register 1	APBCLKCTRL1	R/W	0133_3137H
0398H	APB macro clock control register 2	APBCLKCTRL2	R/W	1331_6FFFH
039CH	Asynchronous macro clock control register	CLKCTRL	R/W	0000_0000H
03A0H	AVE macro clock control register	AVECLKCTRL	R/W	0000_0000H
03A4H to 03C4H	Reserved	-	-	-
03C8H	Access start timing setting register0	ACNT0	R/W	0000_0000H
03CCH	Access start timing setting register1	ACNT1	R/W	0000_0000H
03D0H	Transaction states register	TRANEXIST	R	0000_0000H
03D4 to 03FCH	Reserved	-	-	-
0400H	CPU clock gate control register	CPUGCLKCTRL	R/W	0000_0007H
0404H	Reserved	-	-	-
0408H	GIO clock gate control register	GIOGCLKCTRL	R/W	0000_0003H
040CH	INTA clock gate control register	INTAGCLKCTRL	R/W	0000_0007H
0410H	CHG clock gate control register	CHGGCLKCTRL	R/W	0000_0003H
0414H	BUS0 clock gate control register	BUS0GCLKCTRL	R/W	0000_0003H
0418H	BUS1 clock gate control register	BUS1GCLKCTRL	R/W	0000_0003H
041CH	PBL0 clock gate control register	PBL0GCLKCTRL	R/W	0000_0001H
0420H	PBL1 clock gate control register	PBL1GCLKCTRL	R/W	0000_0001H
0424H	AHB clock gate control register	AHBGCLKCTRL	R/W	0000_0003H
0428H	P2M clock gate control register	P2MGCLKCTRL	R/W	0000_0007H
042CH	M2P clock gate control register	M2PGCLKCTRL	R/W	0000_0007H
0430H	M2M clock gate control register	M2MGCLKCTRL	R/W	0000_0003H
0434H	PMU clock gate control register	PMUGCLKCTRL	R/W	0000_0003H
0438H	SRC clock gate control register	SRCGCLKCTRL	R/W	0000_0001H
043CH	ROM clock gate control register	ROMGCLKCTRL	R/W	0000_0001H
0440H	AB clock gate control register	ABGCLKCTRL	R/W	0000_0001H
0444H	FLA clock gate control register	FLAGCLKCTRL	R/W	0000_0000H

Address	Register Name	Symbol	R/W	After Reset
0448H	MEMC clock gate control register	MEMGCLKCTRL	R/W	0000_000FH
044CH	LCD clock gate control register	LCDGCLKCTRL	R/W	0000_000BH
0450H	IMC clock gate control register	IMCGCLKCTRL	R/W	0000_0003H
0454H	IMCW clock gate control register	IMCWGCLKCTRL	R/W	0000_0003H
0458H	SIZ clock gate control register	SIZGCLKCTRL	R/W	0000_0003H
045CH	ROT clock gate control register	ROTGCLKCTRL	R/W	0000_0003H
0460H	Reserved	—	—	—
0464H	AVE clock gate control register	AVEGCLKCTRL	R/W	0000_0005H
0468H	A3D clock gate control register	A3DGCLKCTRL	R/W	0000_0003H
046CH	DTV clock gate control register	DTVGCLKCTRL	R/W	0000_0007H
0470H	NTS clock gate control register	NTSGCLKCTRL	R/W	0000_0003H
0474H	CAM clock gate control register	CAMGCLKCTRL	R/W	0000_0003H
0478H to 0480H	Reserved	—	—	—
0484H	PWM clock gate control register	PWMGCLKCTRL	R/W	0000_0001H
0488H	Reserved	—	—	—
048CH	IIC0 clock gate control register	IIC0GCLKCTRL	R/W	0000_0001H
0490H	IIC1 clock gate control register	IIC1GCLKCTRL	R/W	0000_0001H
0494H	USB clock gate control register	USBGCLKCTRL	R/W	0000_0003H
0498H	USIAS0 clock gate control register	USIAS0GCLKCTRL	R/W	0000_0007H
049CH	USIAS1 clock gate control register	USIAS1GCLKCTRL	R/W	0000_0005H
04A0H	USIAU0 clock gate control register	USIAU0GCLKCTRL	R/W	0000_0003H
04A4H	Reserved	—	—	—
04A8H	USIBS2 clock gate control register	USIBS2GCLKCTRL	R/W	0000_0005H
04ACH	USIBS3 clock gate control register	USIBS3GCLKCTRL	R/W	0000_0005H
04B0H	USIBS4 clock gate control register	USIBS4GCLKCTRL	R/W	0000_0005H
04B4H	USIBS5 clock gate control register	USIBS5GCLKCTRL	R/W	0000_0005H
04B8H	USIBU1 clock gate control register	USIBU1GCLKCTRL	R/W	0000_0001H
04BCH	USIBU2 clock gate control register	USIBU2GCLKCTRL	R/W	0000_0001H
04C0H	USIBU3 clock gate control register	USIBU3GCLKCTRL	R/W	0000_0001H
04C4H	Reserved	—	—	—
04C8H	SDIO0 clock gate control register	SDIO0GCLKCTRL	R/W	0000_0005H
04CCH	SDIO1 clock gate control register	SDIO1GCLKCTRL	R/W	0000_0005H
04D0H	SDIO2 clock gate control register	SDIO2GCLKCTRL	R/W	0000_0005H
04D4H	SDC clock gate control register	SDCGCLKCTRL	R/W	0000_0005H
04D8H	Reserved	—	—	—
04DCH	CFI clock gate control register	CFIGCLKCTRL	R/W	0000_0006H
04E0H to 04E8H	Reserved	—	—	—
04ECH	TI0 clock gate control register	TI0GCLKCTRL	R/W	0000_0001H
04F0H	TI1 clock gate control register	TI1GCLKCTRL	R/W	0000_0001H
04F4H	TI2 clock gate control register	TI2GCLKCTRL	R/W	0000_0001H
04F8H	TI3 clock gate control register	TI3GCLKCTRL	R/W	0000_0001H

Address	Register Name	Symbol	R/W	After Reset
04FCH	TG0 clock gate control register	TG0GCLKCTRL	R/W	0000_0001H
0500H	TG1 clock gate control register	TG1GCLKCTRL	R/W	0000_0001H
0504H	TG2 clock gate control register	TG2GCLKCTRL	R/W	0000_0001H
0508H	TG3 clock gate control register	TG3GCLKCTRL	R/W	0000_0001H
050CH	TG4 clock gate control register	TG4GCLKCTRL	R/W	0000_0001H
0510H	TG5 clock gate control register	TG5GCLKCTRL	R/W	0000_0001H
0514H	TW0 clock gate control register	TW0GCLKCTRL	R/W	0000_0001H
0518H	TW1 clock gate control register	TW1GCLKCTRL	R/W	0000_0001H
051CH	TW2 clock gate control register	TW2GCLKCTRL	R/W	0000_0001H
0520H	TW3 clock gate control register	TW3GCLKCTRL	R/W	0000_0001H
0524H	TIM clock gate control register	TIMGCLKCTRL	R/W	0000_0001H
0528H	STI clock gate control register	STIGCLKCTRL	R/W	0000_0003H
052CH	Reserved	—	—	—
0530H	AFS clock gate control register	AFSGCLKCTRL	R/W	0000_0003H
0534H to 0538H	Reserved	—	—	—
053CH	REF clock gate control register	REFGCLKCTRL	R/W	0000_0000H
0540H	TW4 clock gate control register	TW4GCLKCTRL	R/W	0000_0001H
0544H to 0550H	Reserved	—	—	—
0554H	PDMA clock gate control register	PDMAGCLKCTRL	R/W	0000_0001H
0558H to 5FCH	Reserved	—	—	—
0600H	TW0_TIN/TI0_TIN setting register	TWI0TIN_SEL	R/W	0001_0001H
0604H	TW1_TIN/TI1_TIN setting register	TWI1TIN_SEL	R/W	0001_0001H
0608H	TW2_TIN/TI2_TIN setting register	TWI2TIN_SEL	R/W	0001_0001H
060CH	TW3_TIN/TI3_TIN setting register	TWI3TIN_SEL	R/W	0001_0001H
0610H	TG0-TG5_TIN setting register	TGNTIN_SEL	R/W	0011_1111H
0614H	Timer clock frequency division setting register	TIMCLKDIV	R/W	0000_00FFH
0618H	USIA_SCLK clock frequency division setting register	USIASCLKDIV	R/W	000F_000FH
061CH	USIA_U0_SCLK frequency division setting register	USIAU0SCLKDIV	R/W	0000_0005H
0620H	Reserved	—	—	—
0624H	IIC_SCLK frequency division setting register	IICSCLKDIV	R/W	002F_002FH
0628H	USB_SCLK frequency division setting register	USBCLKDIV	R/W	0007_0000H
062CH	MEMC_RCLK frequency division setting register	MEMCRCLKDIV	R/W	0000_000FH
0630H	LCD_LCLK frequency division setting register	LCDLCLKDIV	R/W	0000_0009H
0634H to 0644H	Reserved	—	—	—
0648H	SDIO0_SCLK frequency division setting register	SDIO0SCLKDIV	R/W	0000_0005H
064CH	SDIO1_SCLK frequency division setting register	SDIO1SCLKDIV	R/W	0000_0005H
0650H	SDIO2_SCLK frequency division setting register	SDIO2SCLKDIV	R/W	0000_0005H
0654H	USIB0_SCLK frequency division setting register	USIB0SCLKDIV	R/W	000F_000FH
0658H	USIB1_SCLK frequency division setting register	USIB1SCLKDIV	R/W	000F_000FH
065CH	USIB2_SCLK frequency division setting register	USIB2SCLKDIV	R/W	0005_0005H

Address	Register Name	Symbol	R/W	After Reset
0660H	USIB3_SCLK frequency division setting register	USIB3SCLKDIV	R/W	0000_0005H
0664H to 0668H	Reserved	-	-	-
066CH	PWM_PWCLK frequency division setting register	PWMPWCLKDIV	R/W	0013_0013H
0670H	CAM_SCLK frequency division setting register	CAMSCLKDIV	R/W	0000_0019H
0674H to 0678H	Reserved	-	-	-
067CH	A3D_CCLK frequency division setting register	A3DCORECLKDIV	R/W	0000_0000H
0680H	AVE_CCLK frequency division setting register	AVECCLKDIV	R/W	0000_0000H
0684H	QR_CLK frequency division setting register	QRCLKDIV	R/W	0000_0001H
0688H	STI_SCLK source select register	STI_CLKSEL	R/W	0000_0000H
068CH	REF_CLKO frequency division setting register	REFCLKDIV	R/W	0000_0005H
0690H to 0694H	Reserved	-	-	-
0698H	TW4_TIN setting register	TW4TIN_SEL	R/W	0000_0001H
069CH	INTA_TCLK setting register	INTA_CLKSEL	R/W	0000_0000H
06A0H to 06DCH	Reserved	-	-	-
06E0H	32.768 kHz clock status register	CLK32_STATUS	R	0000_0000H
06E4H to 06ECH	Reserved	-	-	-
06F0H	Clock stop instruction signal status register	CLKSTOPSIG_ST	R	0000_0000H
06F4H to 06FCH	Reserved	-	-	-
0700H	Automatic frequency switch control REQMASK0 register	CKRQMODE_MASK0	R/W	0000_0000H
0704H	Automatic frequency switch control REQMASK1 register	CKRQMODE_MASK1	R/W	7FFE_FFFFH
0708H	Automatic frequency switch control register	CKRQ_MODE	R/W	F000_0000H
070CH	Reserved	-	-	-
0710H	Automatic frequency control FIFO space mode setting register	DFS_FIFOMODE	R/W	0000_0000H
0714H	Automatic frequency switch control register	DFS_FIFO_REQMASK	R/W	0000_0007H
0718H	Automatic frequency control LCD_FIFO threshold register	LCD_FIFOTHRESHOLD	R/W	0000_0000H
071CH	Automatic frequency control CAM_FIFO threshold register	CAM_FIFOTHRESHOLD	R/W	0000_0000H
0720H to 072CH	Reserved	-	-	-
0730H	Automatic frequency control domain clock division switch mode register	AUTO_DMDIVCNG_MODE	R/W	0000_0000H
0734H	Automatic frequency control domain clock division switch parameter register	AUTO_DMDIVCNG_PARAMETER	R/W	0531_5100H
0738H to 07BCH	Reserved	-	-	-
07C0H	General-purpose register 0	GENERAL_REG0	R/W	0000_0000H
07C4H	General-purpose register 1	GENERAL_REG1	R/W	0000_0000H
07C8H to 07ECH	Reserved	-	-	-
07F0H	Low power register	LOWPWR	R/W	0000_0000H

Address	Register Name	Symbol	R/W	After Reset
07F4H	PLL power stabilization time setting register	PLLVDDWAIT	R/W	0000_0000H
07F8H to 07FCH	Reserved	-	-	-
0800H	P0 power switch, R-FF/R-RAM control register	P0_POWERSW	R/W	3300_0000H
0804H	Reserved	-	-	-
0808H	PU power switch, R-FF/R-RAM control register	PU_POWERSW	R/W	3300_0000H
080CH	PM power switch, R-FF/R-RAM control register	PM_POWERSW	R/W	3300_0000H
0810H	PL power switch, R-FF/R-RAM control register	PL_POWERSW	R/W	3300_0000H
0814H	Reserved	-	-	-
0818H	P1 power switch, R-FF/R-RAM control register	P1_POWERSW	R/W	3300_0000H
081CH	P2 power switch, R-FF/R-RAM control register	P2_POWERSW	R/W	3300_0000H
0820H	PG power switch, R-FF/R-RAM control register	PG_POWERSW	R/W	3300_0000H
0824H	PV power switch, R-FF/R-RAM control register	PV_POWERSW	R/W	3300_0000H
0828H	PR power switch control register	PR_POWERSW	R/W	0001_0000H
082CH	Power domain status monitor register	POWER_STATUS	R	0000_0000H
0830H	Power switch control sequencer status monitor register	SEQ_BUSY	R	0000_0000H
0834H	Automatic P0 power control register	P0_SWON	R/W	0000_0001H
0838H	Reserved	-	-	-
083CH	Automatic PU power control register	PU_SWON	R/W	0000_0001H
0840H	Automatic PM power control register	PM_SWON	R/W	0000_0001H
0844H	Automatic PL power control register	PL_SWON	R/W	0000_0001H
0848H	Reserved	-	-	-
084CH	Automatic P1 power control register	P1_SWON	R/W	0000_0001H
0850H	Automatic P2 power control register	P2_SWON	R/W	0000_0001H
0854H	Automatic PG power control register	PG_SWON	R/W	0000_0001H
0858H	Automatic PV power control register	PV_SWON	R/W	0000_0001H
085CH	Automatic PR power control register	PR_SWON	R/W	0000_0001H
0860H	P0 power RFF/RRAM control signal input interval setting register 0	P0_RFF_PARA0	R/W	0404_0404H
0864H	P0 power RFF/RRAM control signal input interval setting register 1	P0_RFF_PARA1	R/W	0004_0404H
0868H	P0 power turn-on interval setting register	P0_PWSW_PARA	R/W	0000_0085H
086CH to 0874H	Reserved	-	-	-
0878H	PU power RFF/RRAM control signal input interval setting register 0	PU_RFF_PARA0	R/W	0404_0404H
087CH	PU power RFF/RRAM control signal input interval setting register 1	PU_RFF_PARA1	R/W	0004_0404H
0880H	PU power turn-on interval setting register	PU_PWSW_PARA	R/W	0000_0085H
0884H	PM power RFF/RRAM control signal input interval setting register 0	PM_RFF_PARA0	R/W	0404_0404H
0888H	PM power RFF/RRAM control signal input interval setting register 1	PM_RFF_PARA1	R/W	0004_0404H
088CH	PM power turn-on interval setting register	PM_PWSW_PARA	R/W	0000_0085H
0890H	PL power RFF/RRAM control signal input interval setting	PL_RFF_PARA0	R/W	0404_0404H

Address	Register Name	Symbol	R/W	After Reset
	register 0			
0894H	PL power RFF/RRAM control signal input interval setting register 1	PL_RFF_PARA1	R/W	0004_0404H
0898H	PL power turn-on interval setting register	PL_PWSW_PARA	R/W	0000_0085H
089CH to 08A4H	Reserved	-	-	-
08A8H	P1 power RFF/RRAM control signal input interval setting register 0	P1_RFF_PARA0	R/W	0404_0404H
08ACH	P1 power RFF/RRAM control signal input interval setting register 1	P1_RFF_PARA1	R/W	0004_0B04H
08B0H	P1 power turn-on interval setting register	P1_PWSW_PARA	R/W	0000_0085H
08B4H	P2 power RFF/RRAM control signal input interval setting register 0	P2_RFF_PARA0	R/W	0404_0404H
08B8H	P2 power RFF/RRAM control signal input interval setting register 1	P2_RFF_PARA1	R/W	0004_0B04H
08BCH	P2 power turn-on interval setting register	P2_PWSW_PARA	R/W	0000_0085H
08C0H	PG power RFF/RRAM control signal input interval setting register 0	PG_RFF_PARA0	R/W	0404_0404H
08C4H	PG power RFF/RRAM control signal input interval setting register 1	PG_RFF_PARA1	R/W	0004_0404H
08C8H	PG power turn-on interval setting register	PG_PWSW_PARA	R/W	0000_0085H
08CCH	PV power RFF/RRAM control signal input interval setting register 0	PV_RFF_PARA0	R/W	0404_0404H
08D0H	PV power RFF/RRAM control signal input interval setting register 1	PV_RFF_PARA1	R/W	0004_0404H
08D4H	PV power turn-on interval setting register	PV_PWSW_PARA	R/W	0000_0085H
08D8H	PR power RFF/RRAM control signal input interval setting register 0	PR_RFF_PARA0	R/W	0000_0004H
08DCH	PR power RFF/RRAM control signal input interval setting register 1	PR_RFF_PARA1	R/W	0000_0004H
08E0H	PR power turn-on interval setting register	PR_PWSW_PARA	R/W	0000_0085H
08E4H to 0988H	Reserved	-	-	-
098CH	CPU RAM power switch register	CPU_PWSW_L2RAM	R/W	0000_0000H
0990H	CPU logic power switch register	CPU_PWSW_LOGIC	R/W	0000_0000H
0994H	CPU RAM power switch register	CPU_PWSW_L1RAM	R/W	0000_0000H
0998H	CPU RAM PD control register	CPU_SRAM_PD	R/W	0000_0000H
099CH	CPU power switch control register	CPU_PWSW_CTRL	R/W	0000_0007H
09A0H	CPU power status register	CPU_POWER_STATUS	R	0000_0000H
09A4H	CPU power switch sequencer status register	CPU_SEQ_BUSY	R	0000_0000H
09A8H to 09B0H	Reserved	-	-	-
09B4H	QR WFE setting register	QR_WFE	R/W	0000_0000H
09B8H	QR WFI setting register	QR_WFI	R/W	0000_0000H
09BCH	CPU NEON enable register	CPU_NEON_ENABLE	R/W	0000_0003H
09C0H	Reserved	-	-	-

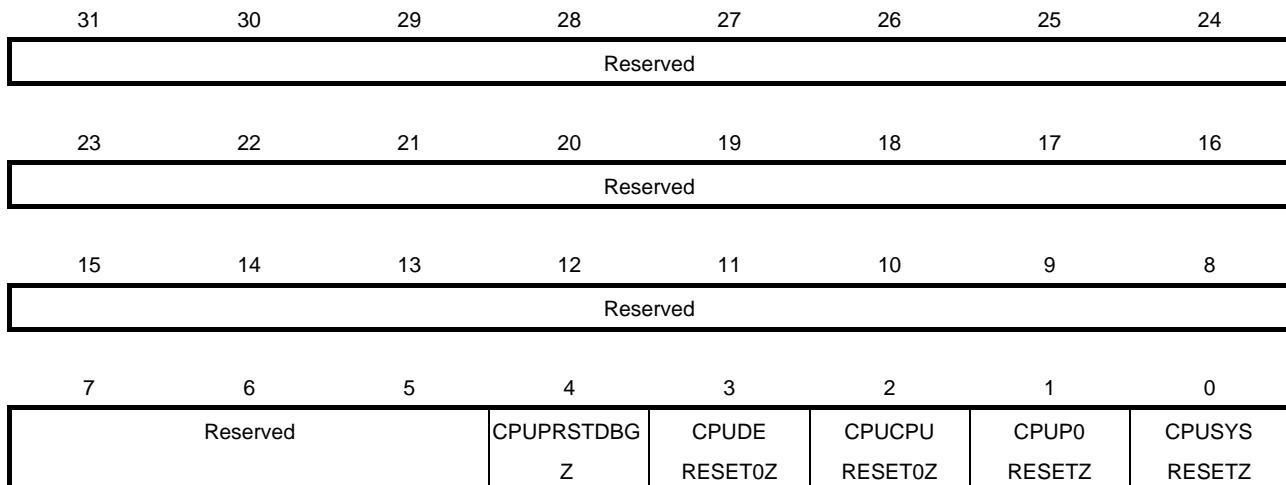
Address	Register Name	Symbol	R/W	After Reset
09C4H	QR_DSIIDEOFF setting register	QR_DSIIDEOFF	R/W	0000_0000H
09C8H to 09CCH	Reserved	-	-	-
09D0H	CPU DS0 power automatic control register	DS0_SWON	R/W	0000_0001H
09D4H	CPU DS1 power automatic control register	DS1_SWON	R/W	0000_0001H
09D8H	CPU HM power automatic control register	HM_SWON	R/W	0000_0001H
09DCH	CPU PE0 power automatic control register	PE0_SWON	R/W	0000_0001H
09E0H	CPU PE1 power automatic control register	PE1_SWON	R/W	0000_0001H
09E4H	CPU NE0 power automatic control register	NE0_SWON	R/W	0000_0001H
09E8H	CPU NE1 power automatic control register	NE1_SWON	R/W	0000_0001H
09ECH	PC power RFF control parameter register 0	PC_RFF_PARA0	R/W	0000_0404H
09F0H	PC power switch control parameter register	PC_PWSW_PARA	R/W	0000_0085H
09F4H	QR_WAIT count setting register	QR_WAITCNT	R/W	0000_0000H
09F8H to 0A2CH	Reserved	-	-	-
0A30H	PMU interrupt source control register	PMU_INTCTRL	R/W	0000_0000H
0A34H to 0A48H	Reserved	-	-	-
0A4CH	CPU ASSOCIATIVITY setting register 0	CPU_ASSOCIATIVITY	R/W	0000_0000H
0A50H	CPUWAYSIZE setting register	CPU_WAYSIZE	R/W	0000_0002H
0A54H	CPU CFGADDRSET setting register	CPU_CFGADDRSET	R/W	0000_0000H
0A58H	CPU CFGADDRFILT setting register	CPU_CFGADDRFILT	R/W	0000_0000H
0A5CH	Reserved	-	-	-
0A60H	CPU SCU address filter enable register	CPU_FILTEREN	R/W	0000_0000H
0A64H	CPU SCU access address setting register	CPU_FILTERADDR	R/W	0000_0000H
0A68H to 0A6CH	Reserved	-	-	-
0A70H	CPU COH setting register	CPU_COH	R/W	0000_0000H
0A74 to 0ADCH	Reserved	-	-	-
0AE0H	ICEREG_DATA[31:0] read register	ICEREG_DATA0	R	0000_0000H
0AE4H	ICEREG_DATA[63:32] read register	ICEREG_DATA1	R	0000_0000H
0AE8H	ICEREG_DATA[95:64] read register	ICEREG_DATA2	R	0000_0000H
0AECH	ICEREG_DATA[127:96] read register	ICEREG_DATA3	R	0000_0000H
0AF0H	ICEREG_DATA[159:128] read register	ICEREG_DATA4	R	0000_0000H
0AF4H	ICEREG_DATA[191:160] read register	ICEREG_DATA5	R	0000_0000H
0AF8H	ICEREG_DATA[223:192] read register	ICEREG_DATA6	R	0000_0000H
0AFCH	ICEREG_DATA[255:224] read register	ICEREG_DATA7	R	00FA_0000H
0B00H	CP15S disable status register	R_CP15SDISABLE	R	0111_0100H
0B04H to 1008H	Reserved	-	-	-
100CH	SMU control register	SMU_CONTROL	R/W	0000_0000H
1010H	Automatic frequency switch control REQMASK2 register	CKRQMODE_MASK2	R/W	0000_0000H
1014H	Reserved	-	-	-

Address	Register Name	Symbol	R/W	After Reset
1018H	MEMC hand shake enable register	MEMCHSENA_AFRQ	R/W	0000_0000H
101CH to 1FFCH	Reserved	-	-	-
2000H	Chip revision register	CHIP_REVISION	R/W	0000_0030H
2004H to FFFFH	Reserved	-	-	-
S2 domain registers				
0000H	CPU15S disable setting register	CP15SDISABLE	R/W	0111_0100H
0004H	CPU SCU secure register protect setting register	CPU_CFGSDISABLE	R/W	0000_0000H
0008H	INT_TIMSEL control register	INT_TIMSEL	R/W	0000_0000H
000CH to FFFCH	Reserved	-	-	-

## 3.2 Register Details

### 3.2.1 CPU reset control register 0

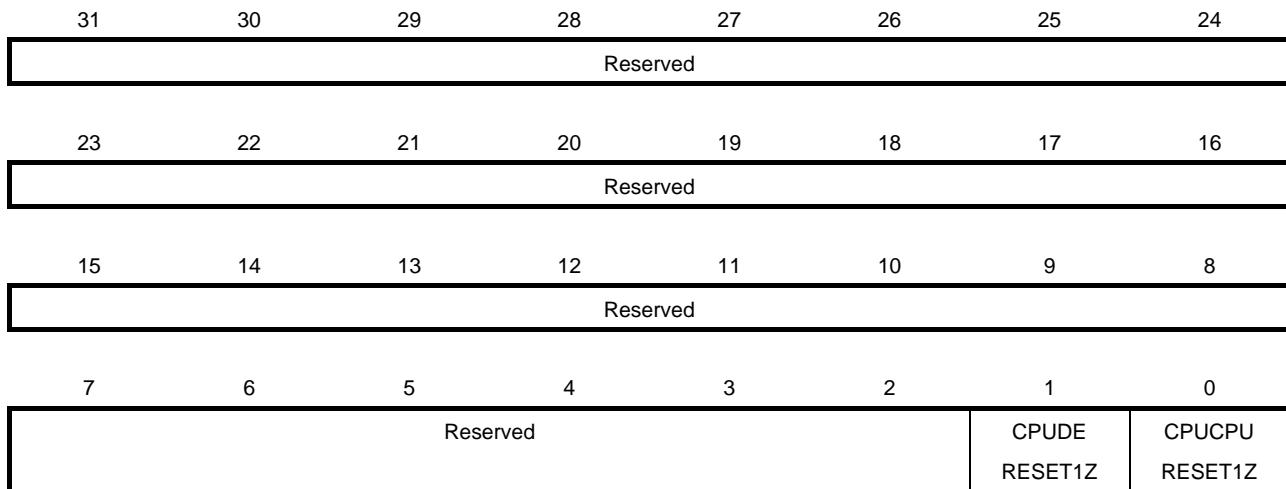
This register (CPU\_RSTCTRL0: E011\_0000H) controls the reset of the CPU macro.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:5	–	Reserved. If these bits are read, 0 is returned for each bit.
CPUPRSTDBGZ	R/W	4	1	Control CPU_PRSTDBGZ. 0: Reset macro 1: Cancel reset
CPUDERESET0Z	R/W	3	1	Control CPU_DERSTZ[0]. 0: Reset macro 1: Cancel reset
CPUCPURESET0Z	R/W	2	1	Control CPU_CPURESTZ[0]. 0: Reset macro 1: Cancel reset
CPUPORESETZ	R/W	1	1	Control CPU_P0RSTZ. 0: Reset macro 1: Cancel reset
CPUSYSRESETZ	R/W	0	1	Control CPU_SYSRSTZ. 0: Reset macro 1: Cancel reset

### 3.2.2 CPU reset control register 1

This register (CPU\_RSTCTRL1: E011\_0004H) controls the reset of the CPU macro.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
CPUDEREST1Z	R/W	1	1	Control CPU_DERSTZ[1]. 0: Reset macro 1: Cancel reset
CPUCPURESET1Z	R/W	0	1	Control CPU_CPURESTZ[1]. 0: Reset macro 1: Cancel reset

### 3.2.3 GIO reset control register

This register (GIO\_RSTCTRL: E011\_000CH) controls the reset of the GIO macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							GIORSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
GIORSTZ	R/W	0	0	Control GIO_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.4 INTA reset control register

This register (INTA\_RSTCTRL: E011\_0010H) controls the reset of the INTA macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							INTARSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
INTARSTZ	R/W	0	1	Control INTA_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.5 CHG reset control register

This register (CHG\_RSTCTRL: E011\_0014H) controls the reset of the CHG macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							CHGRSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
CHGRSTZ	R/W	0	1	Control CHG_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.6 CHG1 reset control register

This register (CHG1\_RSTCTRL: E011\_0018H) controls the reset of the CHG1 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							CHG1RSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
CHG1RSTZ	R/W	0	0	Control CHG1_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.7 BUS0 reset control register

This register (BUS0\_RSTCTRL: E011\_001CH) controls the reset of the BUS0 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							BUS0RSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
BUS0RSTZ	R/W	0	1	Control BUS0_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.8 BUS1 reset control register

This register (BUS1\_RSTCTRL: E011\_0020H) controls the reset of the BUS1 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							BUS1RSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
BUS1RSTZ	R/W	0	1	Control BUS1_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.9 PBL0 reset control register

This register (PBL0\_RSTCTRL: E011\_0024H) controls the reset of the PBL0 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							PBL0RSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
PBL0RSTZ	R/W	0	1	Control PBL0_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.10 PBL1 reset control register

This register (PBL1\_RSTCTRL: E011\_0028H) controls the reset of the PBL1 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							PBL1RSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
PBL1RSTZ	R/W	0	1	Control PBL1_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.11 AHB reset control register

This register (AHB\_RSTCTRL: E011\_002CH) controls the reset of the AHB macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							AHBRSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
AHBRSTZ	R/W	0	1	Control AHB_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.12 P2M reset control register

This register (P2M\_RSTCTRL: E011\_0030H) controls the reset of the P2M macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							P2MRSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
P2MRSTZ	R/W	0	0	Control P2M_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.13 M2P reset control register

This register (M2P\_RSTCTRL: E011\_0034H) controls the reset of the M2P macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							M2PRSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
M2PRSTZ	R/W	0	0	Control M2P_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.14 M2M reset control register

This register (M2M\_RSTCTRL: E011\_0038H) controls the reset of the M2M macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							M2MRSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
M2MRSTZ	R/W	0	0	Control M2M_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.15 PMU reset control register

This register (PMU\_RSTCTRL: E011\_003CH) controls the reset of the PMU macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							PMURSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
PMURSTZ	R/W	0	0	Control PMU_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.16 SRC reset control register

This register (SRC\_RSTCTRL: E011\_0040H) controls the reset of the SRC macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							SRCRSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
SRCRSTZ	R/W	0	1	Control SRC_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.17 ROM reset control register

This register (ROM\_RSTCTRL: E011\_0044H) controls the reset of the ROM macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							ROMRSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
ROMRSTZ	R/W	0	1	Control ROM_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.18 AB0 reset control register

This register (AB0\_RSTCTRL: E011\_0048H) controls the reset of the AB0 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							AB0RSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
AB0RSTZ	R/W	0	1	Control AB0_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.19 MEMC reset control register

This register (MEMC\_RSTCTRL: E011\_004CH) controls the reset of the MEMC macro.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								
7	6	5	4	3	2	1	0	
Reserved								MEMCRSTZ
Name	R/W	Bit No.	After Reset	Description				
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.				
MEMCRSTZ	R/W	0	0	Control MEMC_RSTZ. 0: Reset macro 1: Cancel reset				

### 3.2.20 LCD reset control register

This register (LCD\_RSTCTRL: E011\_0050H) controls the reset of the LCD macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						LCDARSTZ	LCDRSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
LCDARSTZ	R/W	1	0	Control LCD_ARSTZ. 0: Reset macro 1: Cancel reset
LCDRSTZ	R/W	0	0	Control LCD_RSTZ. 0: Reset macro 1: Cancel reset

### 3.2.21 IMC reset control register

This register (IMC\_RSTCTRL: E011\_0054H) controls the reset of the IMC macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							IMCRSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
IMCRSTZ	R/W	0	0	Control IMC_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.22 IMCW reset control register

This register (IMCW\_RSTCTRL: E011\_0058H) controls the reset of the IMCW macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							IMCWRSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
IMCWRSTZ	R/W	0	0	Control IMCW_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.23 SIZ reset control register

This register (SIZ\_RSTCTRL: E011\_005CH) controls the reset of the SIZ macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							SIZRSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
SIZRSTZ	R/W	0	0	Control SIZ_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.24 ROT reset control register

This register (ROT\_RSTCTRL: E011\_0060H) controls the reset of the ROT macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							ROTRSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
ROTRSTZ	R/W	0	0	Control ROT_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.25 AVE reset control register

This register (AVE\_RSTCTRL: E011\_0068H) controls the reset of the AVE macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				AVECRSTZ	AVEARSTZ	AVEPRSTZ	

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:3	–	Reserved. If these bits are read, 0 is returned for each bit.
AVECRSTZ	R/W	2	0	Control AVE_CRSTZ. 0: Reset macro, 1: Cancel reset
AVEARSTZ	R/W	1	0	Control AVE_ARSTZ. 0: Reset macro, 1: Cancel reset
AVEPRSTZ	R/W	0	0	Control AVE_PRSTZ. 0: Reset macro, 1: Cancel reset

### 3.2.26 A3D reset control register

This register (A3D\_RSTCTRL: E011\_006CH) controls the reset of the A3D macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							A3DRSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
A3DRSTZ	R/W	0	0	Control A3D_RSTZ. 0: Reset macro, 1: Cancel reset			

### 3.2.27 DTV reset control register

This register (DTV\_RSTCTRL: E011\_0070H) controls the reset of the DTV macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							DTVRSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
DTVRSTZ	R/W	0	0	Control DTV_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.28 NTS reset control register

This register (NTS\_RSTCTRL: E011\_0074H) controls the reset of the NTS macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							NTSRSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
NTSRSTZ	R/W	0	0	Control NTS_RSTZ. 0: Reset macro 1: Cancel reset

### 3.2.29 CAM reset control register

This register (CAM\_RSTCTRL: E011\_0078H) controls the reset of the CAM macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							CAMRSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
CAMRSTZ	R/W	0	0	Control CAM_RSTZ. 0: Reset macro 1: Cancel reset

### 3.2.30 PWM reset control register

This register (PWM\_RSTCTRL: E011\_0088H) controls the reset of the PWM macro.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								
7	6	5	4	3	2	1	0	PWMRSTZ
Reserved								

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
PWMRSTZ	R/W	0	0	Control PWM_RSTZ. 0: Reset macro 1: Cancel reset

### 3.2.31 USIAS0 reset control register

This register (USIAS0\_RSTCTRL: E011\_008CH) controls the reset of the USIAS0 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						USIAS0ARSTZ	USIAS0SRSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
USIAS0ARSTZ	R/W	1	0	Control USIA_S0_ARSTZ. 0: Reset macro 1: Cancel reset
USIAS0SRSTZ	R/W	0	0	Control USIA_S0_SRSTZ. 0: Reset macro 1: Cancel reset

### 3.2.32 USIAS1 reset control register

This register (USIAS1\_RSTCTRL: E011\_0090H) controls the reset of the USIAS1 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						USIAS1ARSTZ	USIAS1SRSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
USIAS1ARSTZ	R/W	1	0	Control USIA_S1_ARSTZ. 0: Reset macro 1: Cancel reset
USIAS1SRSTZ	R/W	0	0	Control USIA_S1_SRSTZ. 0: Reset macro 1: Cancel reset

### 3.2.33 USIAU0 reset control register

This register (USIAU0\_RSTCTRL: E011\_0094H) controls the reset of the USIAU0 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						USIAU0ARSTZ	Reserved

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
USIAU0ARSTZ	R/W	1	0	Control USIA_U0_ARSTZ. 0: Reset macro 1: Cancel reset
Reserved	R	0	–	Reserved. If this bit is read, 0 is returned.

### 3.2.34 USIBS2 reset control register

This register (USIBS2\_RSTCTRL: E011\_009CH) controls the reset of the USIBS2 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						USIBS2ARSTZ	USIBS2SRSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
USIBS2ARSTZ	R/W	1	0	Control USIB_S2_ARSTZ. 0: Reset macro 1: Cancel reset
USIBS2SRSTZ	R/W	0	0	Control USIB_S2_SRSTZ. 0: Reset macro 1: Cancel reset

### 3.2.35 USIBS3 reset control register

This register (USIBS3\_RSTCTRL: E011\_00A0H) controls the reset of the USIBS3 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						USIBS3ARSTZ	USIBS3SRSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
USIBS3ARSTZ	R/W	1	0	Control USIB_S3_ARSTZ. 0: Reset macro, 1: Cancel reset
USIBS3SRSTZ	R/W	0	0	Control USIB_S3_SRSTZ. 0: Reset macro, 1: Cancel reset

### 3.2.36 USIBS4 reset control register

This register (USIBS4\_RSTCTRL: E011\_00A4H) controls the reset of the USIBS4 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						USIBS4ARSTZ	USIBS4SRSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
USIBS4ARSTZ	R/W	1	0	Control USIB_S4_ARSTZ. 0: Reset macro 1: Cancel reset
USIBS4SRSTZ	R/W	0	0	Control USIB_S4_SRSTZ. 0: Reset macro 1: Cancel reset

### 3.2.37 USIBS5 reset control register

This register (USIBS5\_RSTCTRL: E011\_00A8H) controls the reset of the USIBS5 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						USIBS5ARSTZ	USIBS5SRSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
USIBS5ARSTZ	R/W	1	0	Control USIB_S5_ARSTZ. 0: Reset macro, 1: Cancel reset
USIBS5SRSTZ	R/W	0	0	Control USIB_S5_SRSTZ. 0: Reset macro, 1: Cancel reset

### 3.2.38 USIBU1 reset control register

This register (USIBU1\_RSTCTRL: E011\_00ACH) controls the reset of the USIBU1 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						USIBU1ARSTZ	Reserved

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
USIBU1ARSTZ	R/W	1	0	Control USIB_U1_ARSTZ. 0: Reset macro 1: Cancel reset
Reserved	R	0	–	Reserved. If this bit is read, 0 is returned.

### 3.2.39 USIBU2 reset control register

This register (USIBU2\_RSTCTRL: E011\_00B0H) controls the reset of the USIBU2 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						USIBU2ARSTZ	Reserved

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
USIBU2ARSTZ	R/W	1	0	Control USIB_U2_ARSTZ. 0: Reset macro 1: Cancel reset
Reserved	R	0	–	Reserved. If this bit is read, 0 is returned.

### 3.2.40 USIBU3 reset control register

This register (USIBU3\_RSTCTRL: E011\_00B4H) controls the reset of the USIBU3 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						USIBU3ARSTZ	Reserved
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.			
USIBU3ARSTZ	R/W	1	0	Control USIB_U3_ARSTZ. 0: Reset macro 1: Cancel reset			
Reserved	R	0	–	Reserved. If this bit is read, 0 is returned.			

### 3.2.41 SDIO0 reset control register

This register (SDIO0\_RSTCTRL: E011\_00BCH) controls the reset of the SDIO0 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						SDIO0RSTZ	
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
SDIO0RSTZ	R/W	0	0	Control SDIO0_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.42 SDIO1 reset control register

This register (SDIO1\_RSTCTRL: E011\_00C0H) controls the reset of the SDIO1 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							SDIO1RSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
SDIO1RSTZ	R/W	0	0	Control SDIO1_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.43 SDIO2 reset control register

This register (SDIO2\_RSTCTRL: E011\_00C4H) controls the reset of the SDIO2 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							SDIO2RSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
SDIO2RSTZ	R/W	0	0	Control SDIO2_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.44 SDC reset control register

This register (SDC\_RSTCTRL: E011\_00C8H) controls the reset of the SDC macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							SDCRSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
SDCRSTZ	R/W	0	0	Control SDC_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.45 CFI reset control register

This register (SDC\_RSTCTRL: E011\_00D0H) controls the reset of the CFI macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							CFIRSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
CFIRSTZ	R/W	0	0	Control CFI_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.46 IIC0 reset control register

This register (IIC0\_RSTCTRL: E011\_00DCH) controls the reset of the IIC0 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							IIC0RSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
IIC0RSTZ	R/W	0	0	Control IIC0_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.47 IIC1 reset control register

This register (IIC1\_RSTCTRL: E011\_00E0H) controls the reset of the IIC1 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							IIC1RSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
IIC1RSTZ	R/W	0	0	Control IIC1_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.48 USB0 reset control register

This register (USB0\_RSTCTRL: E011\_00E4H) controls the reset of the USB0 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							USB0RSTZ
Name							
Reserved	R	Bit No.	After Reset	Description			
USB0RSTZ	R/W	0	0	Control USB0_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.49 USB1 reset control register

This register (USB1\_RSTCTRL: E011\_00E8H) controls the reset of the USB1 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							USB1RSTZ
Name							
Reserved	R	Bit No.	After Reset	Description			
USB1RSTZ	R/W	0	0	Control USB1_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.50 TI0 reset control register

This register (TI0\_RSTCTRL: E011\_00ECH) controls the reset of the TI0 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							TI0RSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
TI0RSTZ	R/W	0	0	Control TI0_RSTZ. 0: Reset macro 1: Cancel reset

### 3.2.51 TI1 reset control register

This register (TI1\_RSTCTRL: E011\_00F0H) controls the reset of the TI1 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							TI1RSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
TI1RSTZ	R/W	0	0	Control TI1_RSTZ. 0: Reset macro 1: Cancel reset

### 3.2.52 TI2 reset control register

This register (TI2\_RSTCTRL: E011\_00F4H) controls the reset of the TI2 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							TI2RSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
TI2RSTZ	R/W	0	0	Control TI2_RSTZ. 0: Reset macro 1: Cancel reset

### 3.2.53 TI3 reset control register

This register (TI3\_RSTCTRL: E011\_00F8H) controls the reset of the TI3 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							TI3RSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
TI3RSTZ	R/W	0	0	Control TI3_RSTZ. 0: Reset macro 1: Cancel reset

### 3.2.54 TW0 reset control register

This register (TW0\_RSTCTRL: E011\_00FCH) controls the reset of the TW0 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							TW0RSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
TW0RSTZ	R/W	0	0	Control TW0_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.55 TW1 reset control register

This register (TW1\_RSTCTRL: E011\_0100H) controls the reset of the TW1 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							TW1RSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
TW1RSTZ	R/W	0	0	Control TW1_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.56 TW2 reset control register

This register (TW2\_RSTCTRL: E011\_0104H) controls the reset of the TW2 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							TW2RSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
TW2RSTZ	R/W	0	0	Control TW2_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.57 TW3 reset control register

This register (TW3\_RSTCTRL: E011\_0108H) controls the reset of the TW3 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							TW3RSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
TW3RSTZ	R/W	0	0	Control TW3_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.58 TG0 reset control register

This register (TG0\_RSTCTRL: E011\_010CH) controls the reset of the TG0 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							TG0RSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
TG0RSTZ	R/W	0	0	Control TG0_RSTZ. 0: Reset macro 1: Cancel reset

### 3.2.59 TG1 reset control register

This register (TG1\_RSTCTRL: E011\_0110H) controls the reset of the TG1U macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							TG1RSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
TG1RSTZ	R/W	0	0	Control TG1_RSTZ. 0: Reset macro 1: Cancel reset

### 3.2.60 TG2 reset control register

This register (TG2\_RSTCTRL: E011\_0114H) controls the reset of the TG2 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							TG2RSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
TG2RSTZ	R/W	0	0	Control TG2_RSTZ. 0: Reset macro 1: Cancel reset

### 3.2.61 TG3 reset control register

This register (TG3\_RSTCTRL: E011\_0118H) controls the reset of the TG3 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							TG3RSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
TG3RSTZ	R/W	0	0	Control TG3_RSTZ. 0: Reset macro 1: Cancel reset

### 3.2.62 TG4 reset control register

This register (TG4\_RSTCTRL: E011\_011CH) controls the reset of the TG4 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							TG4RSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
TG4RSTZ	R/W	0	0	Control TG4_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.63 TG5 reset control register

This register (TG5\_RSTCTRL: E011\_0120H) controls the reset of the TG5 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							TG5RSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
TG5RSTZ	R/W	0	0	Control TG5_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.64 STI reset control register

This register (STI\_RSTCTRL: E011\_0124H) controls the reset of the STI macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							STIRSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
STIRSTZ	R/W	0	0	Control STI_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.65 AFS reset control register

This register (AFS\_RSTCTRL: E011\_012CH) controls the reset of the AFS macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							AFSRSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
AFSRSTZ	R/W	0	0	Control AFS_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.66 TW4 reset control register

This register (TW4\_RSTCTRL: E011\_0140H) controls the reset of the TW4 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							TW4RSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
TW4RSTZ	R/W	0	0	Control TW4_RSTZ. 0: Reset macro 1: Cancel reset			

### 3.2.67 PDMA reset control register

This register (PDMA\_RSTCTRL: E011\_0148H) controls the reset of the PDMA macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							PDMARSTZ
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
PDMARSTZ	R/W	0	0	Control PDMA_RSTZ. 0: Reset macro 1: Cancel reset			

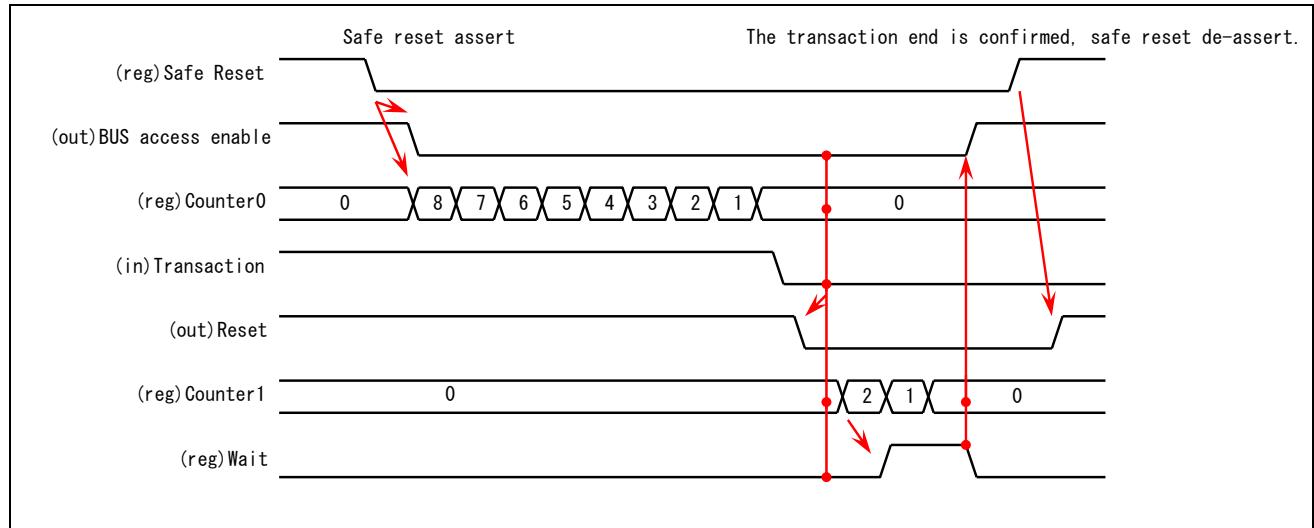
### 3.2.68 CPU0 safe reset control register

This register (CPU\_SAFE\_RESET0: E011\_0154H) controls the safe reset of the CPU macro.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								
7	6	5	4	3	2	1	0	
Reserved			CPUPRSTSFD BGZ	CPUDE0 SFRSTZ	CPUCPU0 SFRSTZ	CPUPO SFRSTZ	CPUSYS SFRSTZ	

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:5	–	Reserved. If these bits are read, 0 is returned for each bit.
CPUPRSTSDBGZ	R/W	4	1	Control CPU_PRSTDBGZ. 0: Reset macro 1: Cancel reset
CPUDE0SFRSTZ	R/W	3	1	Control CPU_DERSTZ[0]. 0: Reset macro 1: Cancel reset
CPUCPU0SFRSTZ	R/W	2	1	Control CPU_CPURSTZ[0]. 0: Reset macro 1: Cancel reset
CPUPOSFRSTZ	R/W	1	1	Control CPU_P0RSTZ. 0: Reset macro 1: Cancel reset
CPUSYSSFRSTZ	R/W	0	1	Control CPU_SYSRSTZ. 0: Reset macro 1: Cancel reset

When transaction doesn't occur to CPU macro, it's possible to assert xxx\_RSTZ by asserting xxxSFRSTZ. De- Assert a safe reset after an end of transaction. The state of the transaction can be confirmed in [Addr:0x03D0] TRANEXIST (transaction status register).



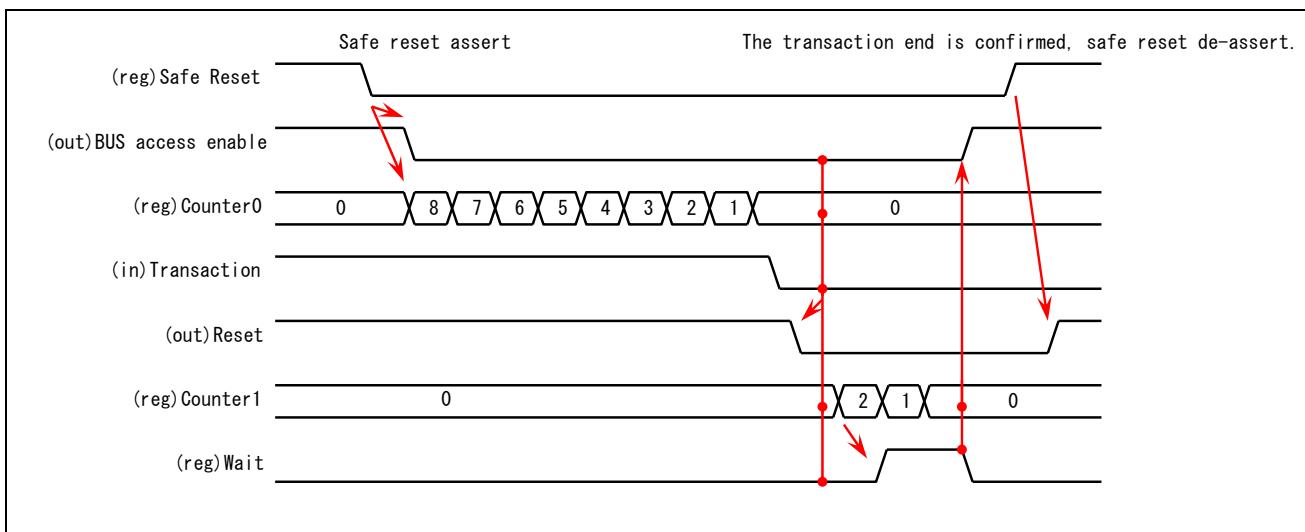
### 3.2.69 CPU1 safe reset control register

This register (CPU\_SAFE\_RESET1: E011\_0158H) controls the safe reset of the CPU macro.

31	30	29	28	27	26	25	24	Reserved
23	22	21	20	19	18	17	16	Reserved
15	14	13	12	11	10	9	8	Reserved
7	6	5	4	3	2	1	0	Reserved
						CPUDE1	CPUCPU1	SFRSTZ
						SFRSTZ		

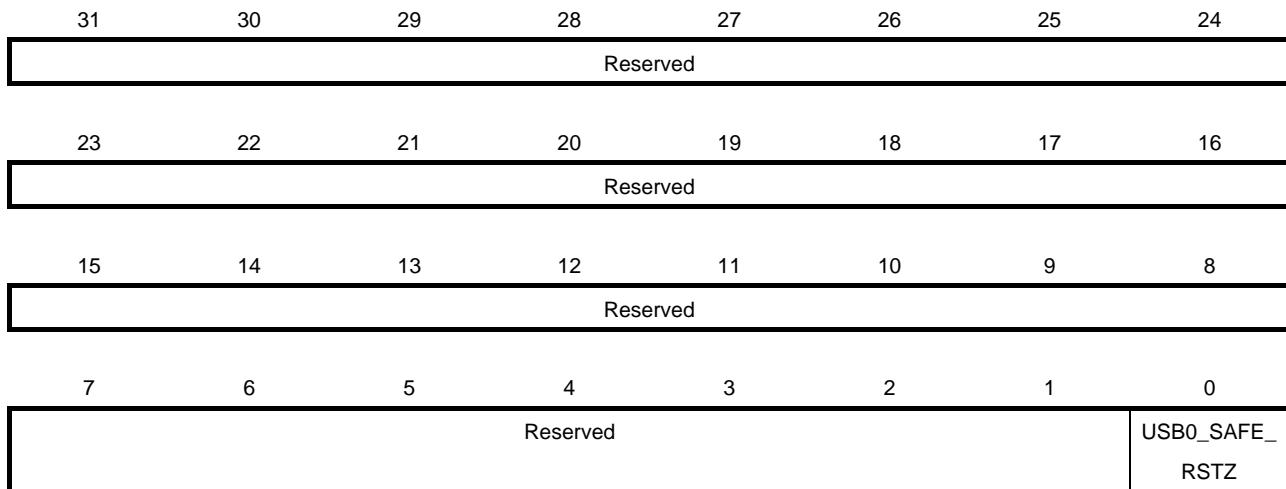
Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
CPUDE1SFRSTZ	R/W	1	1	Control CPU_DERSTZ[1]. 0: Reset macro 1: Cancel reset
CPUCPU1SFRSTZ	R/W	0	1	Control CPU_CPURESTZ[1]. 0: Reset macro 1: Cancel reset

When transaction doesn't occur to CPU macro, it's possible to assert xxx\_RSTZ by asserting xxxSFRSTZ. De-Assert a safe reset after an end of transaction. The state of the transaction can be confirmed in [Addr:0x03D0] TRANEXIST (transaction status register).



### 3.2.70 USB0 safe reset control register

This register (USB0\_SAFE\_RESET: E011\_0160H) controls the safe reset of the USB0 macro.

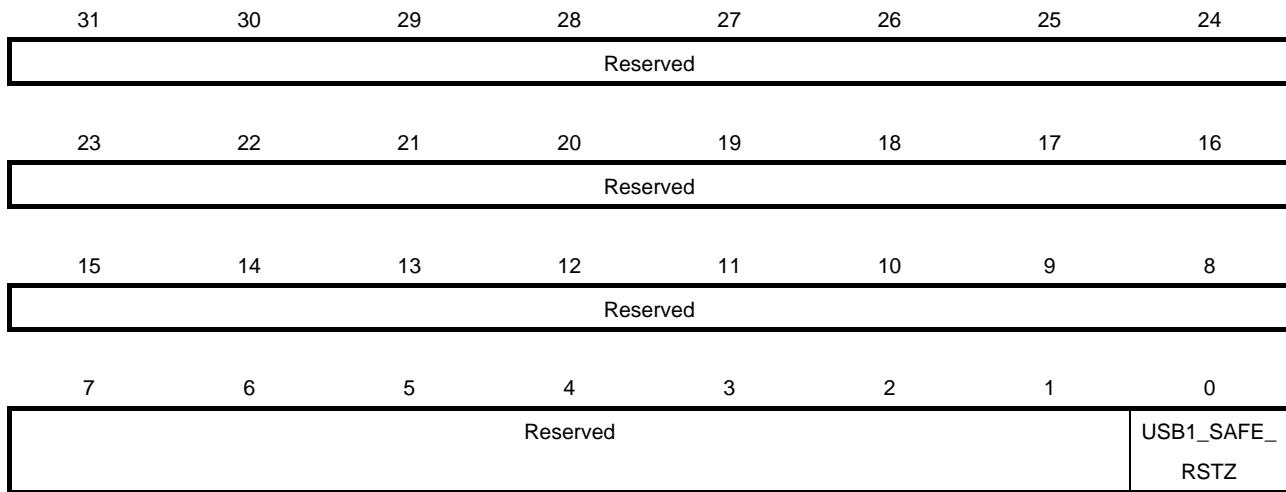


Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
USB0_SAFE_RSTZ	R/W	0	1	Control USB0_SAFE_RSTZ. 0: Reset macro 1: Cancel reset

When transaction doesn't occur, assert.

### 3.2.71 USB1 safe reset control register

This register (USB1\_SAFE\_RESET: E011\_0164H) controls the safe reset of the USB1 macro.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
USB1_SAFE_RSTZ	R/W	0	1	Control USB1_SAFE_RSTZ. 0: Reset macro 1: Cancel reset

When transaction doesn't occur, assert.

### 3.2.72 DTV safe reset control register

This register (DTV\_SAFE\_RESET: E011\_0168H) controls the safe reset of the DTV macro.

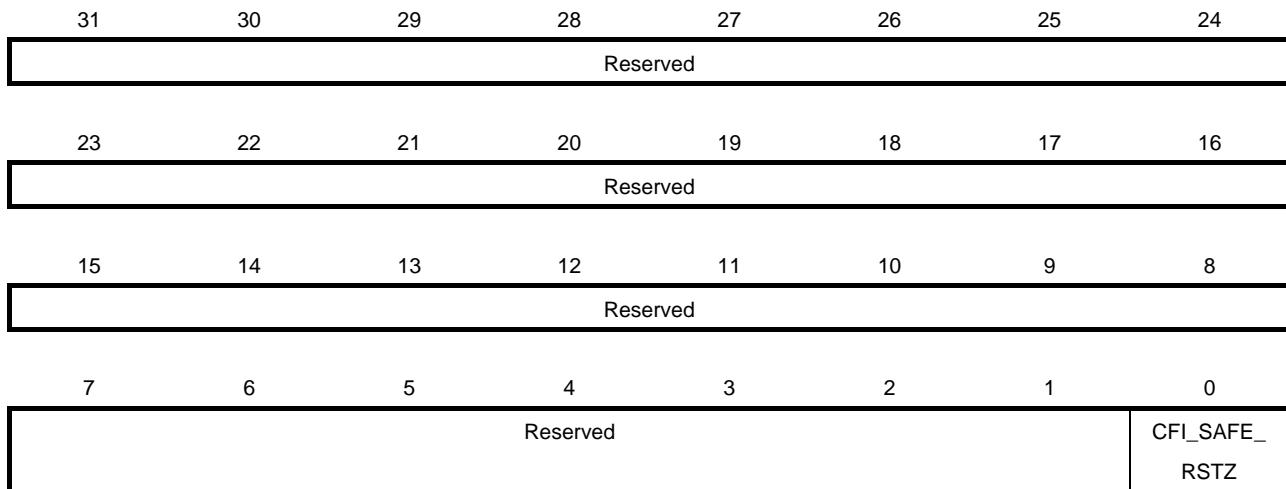
31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							DTV_SAFE_RSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
DTV_SAFE_RSTZ	R/W	0	1	Control DTV_SAFE_RSTZ. 0: Reset macro 1: Cancel reset

When transaction doesn't occur, assert.

### 3.2.73 CFI safe reset control register

This register (CFI\_SAFE\_RESET: E011\_016CH) controls the safe reset of the CFI macro.

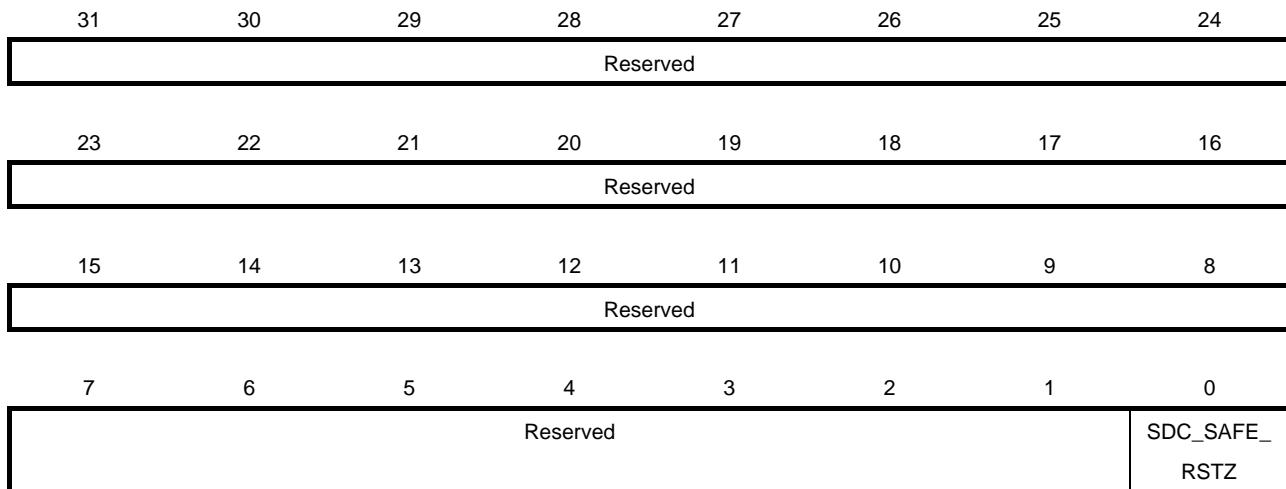


Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
CFI_SAFE_RSTZ	R/W	0	1	Control CFI_SAFE_RSTZ. 0: Reset macro 1: Cancel reset

When transaction doesn't occur, assert.

### 3.2.74 SDC safe reset control register

This register (SDC\_SAFE\_RESET: E011\_0170H) controls the safe reset of the SDC macro.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
SDC_SAFE_RSTZ	R/W	0	1	Control SDC_SAFE_RSTZ. 0: Reset macro 1: Cancel reset

When transaction doesn't occur, assert.

### 3.2.75 SDIO0 safe reset control register

This register (SDIO0\_SAFE\_RESET: E011\_0174H) controls the safe reset of the SDIO0 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							SDIO0_SAFE_RSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
SDIO0_SAFE_RSTZ	R/W	0	1	Control SDIO0_SAFE_RSTZ. 0: Reset macro 1: Cancel reset

When transaction doesn't occur, assert.

### 3.2.76 SDIO1 safe reset control register

This register (SDIO1\_SAFE\_RESET: E011\_0178H) controls the safe reset of the SDIO1 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							SDIO1_SAFE_RSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
SDIO1_SAFE_RSTZ	R/W	0	1	Control SDIO1_SAFE_RSTZ. 0: Reset macro 1: Cancel reset

When transaction doesn't occur, assert.

### 3.2.77 SDIO2 safe reset control register

This register (SDIO1\_SAFE\_RESET: E011\_017CH) controls the safe reset of the SDIO2 macro.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							SDIO2_SAFE_RSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
SDIO2_SAFE_RSTZ	R/W	0	1	Control SDIO2_SAFE_RSTZ. 0: Reset macro 1: Cancel reset

When transaction doesn't occur, assert.

### 3.2.78 USIA safe reset control register

This register (USIA\_SAFE\_RESET: E011\_0180H) controls the safe reset of the USIA macro.

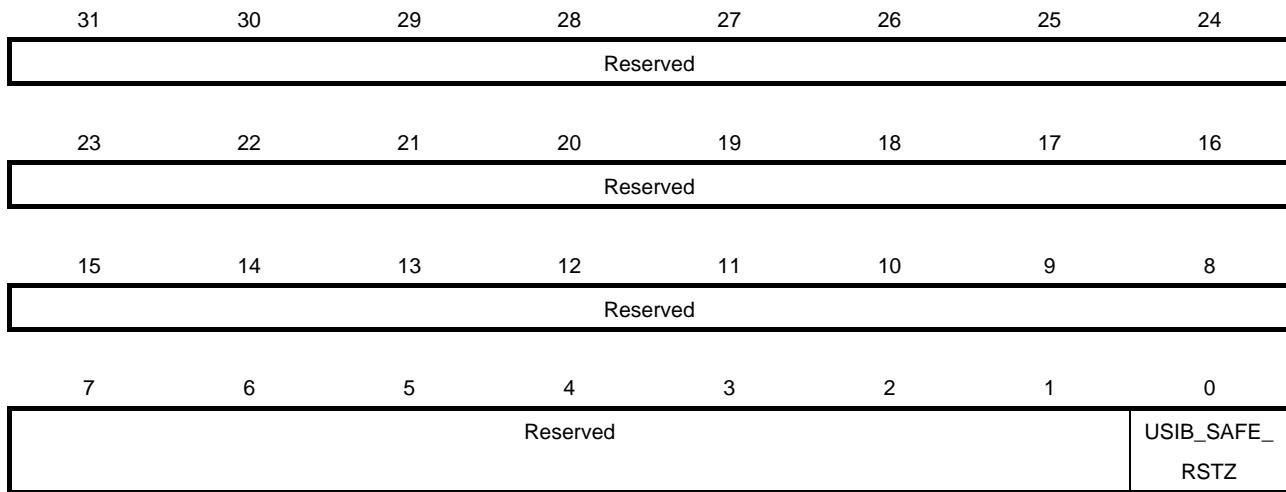
31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							USIA_SAFE_RSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
USIA_SAFE_RSTZ	R/W	0	1	Control USIA_SAFE_RSTZ. 0: Reset macro 1: Cancel reset

When transaction doesn't occur, assert.

### 3.2.79 USIB safe reset control register

This register (USIB\_SAFE\_RESET: E011\_0184H) controls the safe reset of the USIB macro.

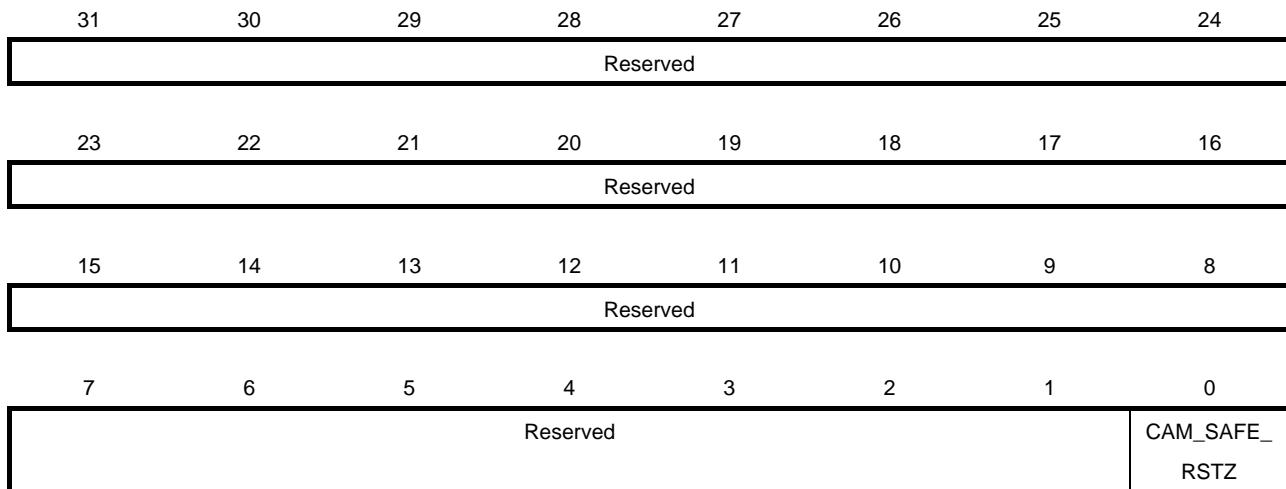


Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
USIB_SAFE_RSTZ	R/W	0	1	Control USIB_SAFE_RSTZ. 0: Reset macro 1: Cancel reset

When transaction doesn't occur, assert.

### 3.2.80 CAM safe reset control register

This register (CAM\_SAFE\_RESET: E011\_018CH) controls the safe reset of the CAM macro.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
CAM_SAFE_RSTZ	R/W	0	1	Control CAM_SAFE_RSTZ. 0: Reset macro 1: Cancel reset

When transaction doesn't occur, assert.

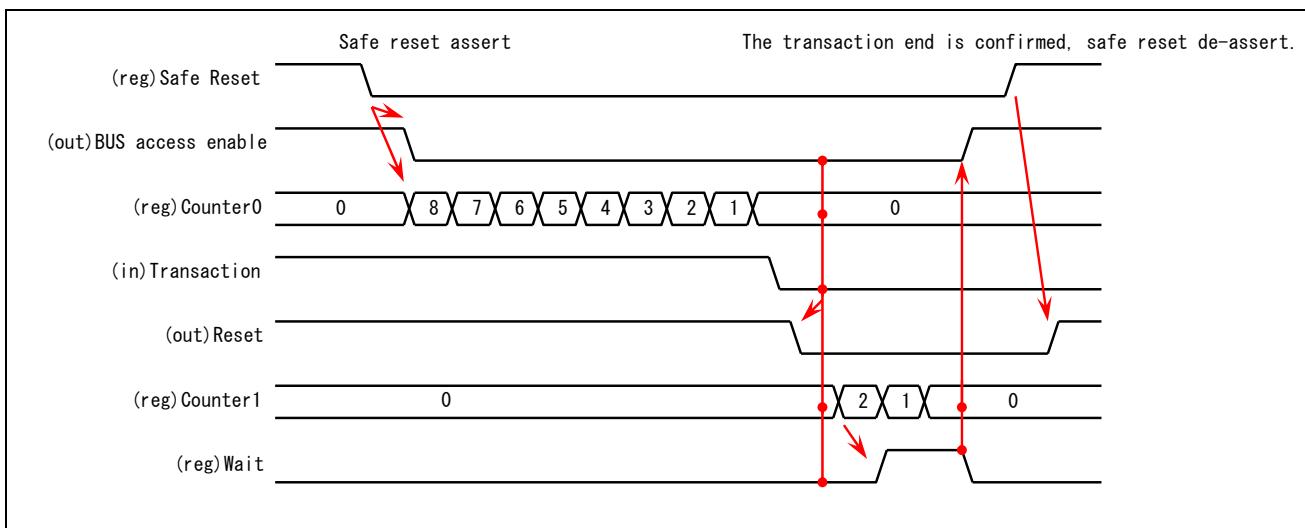
### 3.2.81 AHB safe reset control register

This register (AHB\_SAFE\_RESET: E011\_019CH) controls the safe reset of the AHB macro.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								
7	6	5	4	3	2	1	0	
Reserved								AHBSFRSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
AHBSFRSTZ	R/W	0	1	Control AHB_RSTZ. 0: Reset macro 1: Cancel reset

When transaction doesn't occur to AHB macro, it's possible to assert AHB\_RSTZ by asserting AHBSFRSTZ. De-Assert a safe reset after an end of transaction. The state of the transaction can be confirmed in [Addr:0x03D0] TRANEXIST (transaction status register).



### 3.2.82 A3D safe reset control register

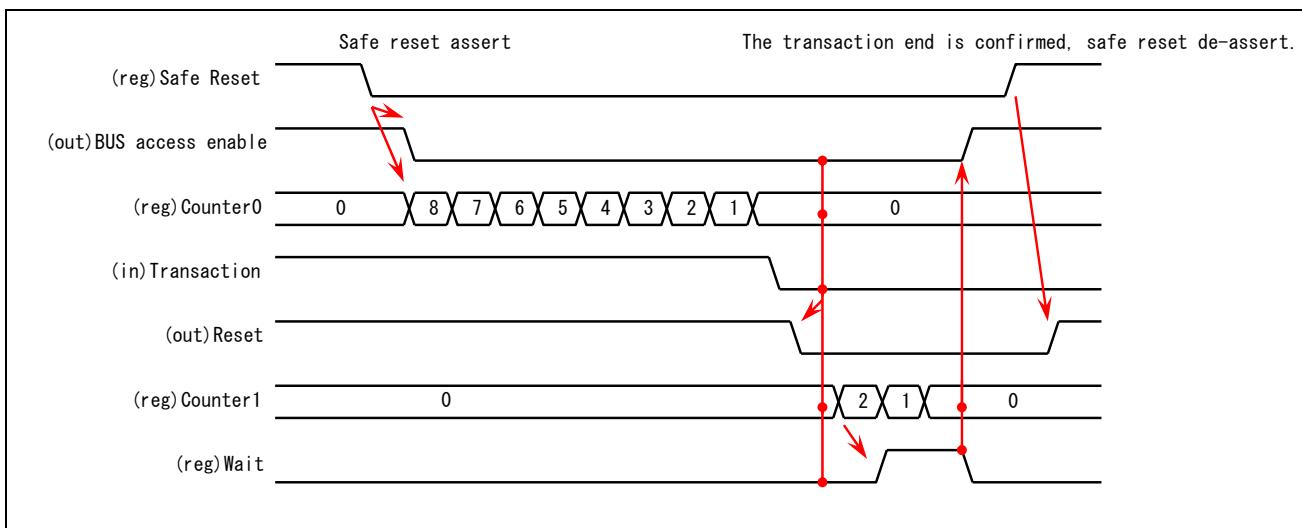
This register (A3D\_SAFE\_RESET: E011\_01A0H) controls the safe reset of the A3D macro.

31	30	29	28	27	26	25	24	Reserved
23	22	21	20	19	18	17	16	Reserved
15	14	13	12	11	10	9	8	Reserved
7	6	5	4	3	2	1	0	Reserved
								A3DSFRSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	-	Reserved. If these bits are read, 0 is returned for each bit.
A3DSFRSTZ	R/W	0	1	Control A3D_RSTZ. 0: Reset macro 1: Cancel reset

When transaction doesn't occur to A3D macro, it's possible to assert A3D\_RSTZ by asserting A3DSFRSTZ. De-Assert a safe reset after an end of transaction. The state of the transaction can be confirmed in [Addr:0x03D0] TRANEXIST (transaction status register).



### 3.2.83 AVE safe reset control register

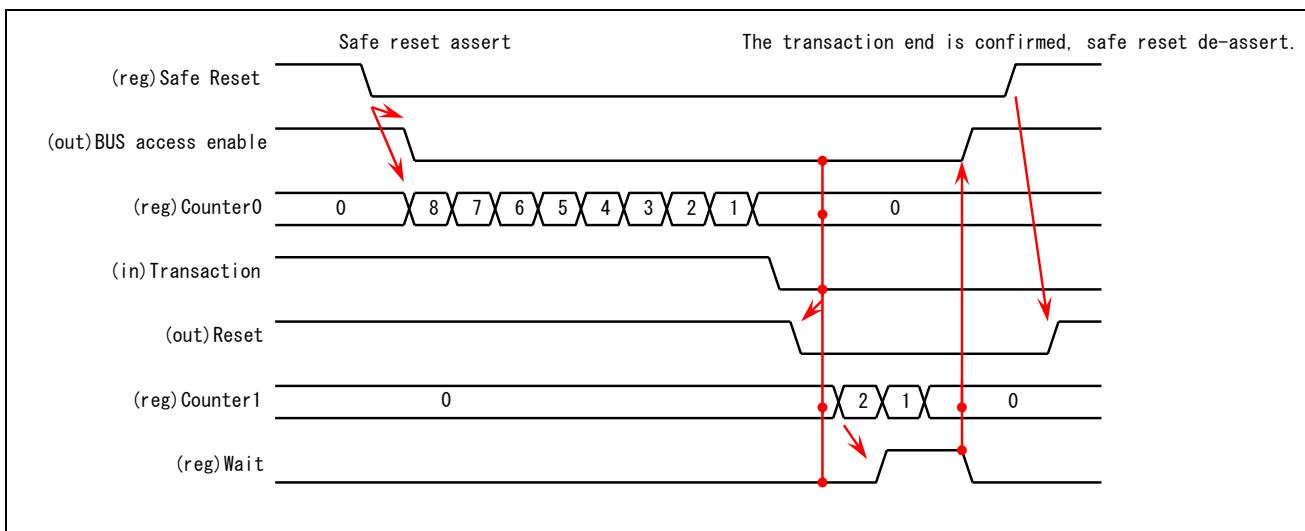
This register (AVE\_SAFE\_RESET: E011\_01A4H) controls the safe reset of the AVE macro.

31	30	29	28	27	26	25	24	Reserved
23	22	21	20	19	18	17	16	Reserved
15	14	13	12	11	10	9	8	Reserved
7	6	5	4	3	2	1	0	Reserved
								AVESFRSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	-	Reserved. If these bits are read, 0 is returned for each bit.
AVESFRSTZ	R/W	0	1	Control AVE_RSTZ. 0: Reset macro 1: Cancel reset

When transaction doesn't occur to AVE macro, it's possible to assert AVE\_RSTZ by asserting AVESFRSTZ. De-Assert a safe reset after an end of transaction. The state of the transaction can be confirmed in [Addr:0x03D0] TRANEXIST (transaction status register).



### 3.2.84 SIZ safe reset control register

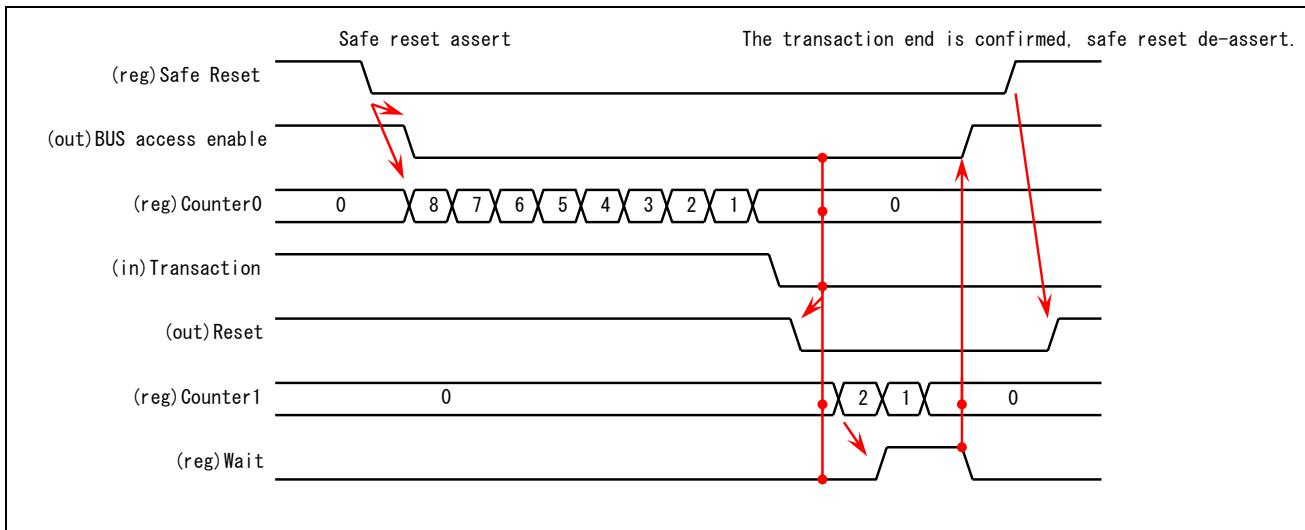
This register (SIZ\_SAFE\_RESET: E011\_01A8H) controls the safe reset of the SIZ macro.

31	30	29	28	27	26	25	24	Reserved
23	22	21	20	19	18	17	16	Reserved
15	14	13	12	11	10	9	8	Reserved
7	6	5	4	3	2	1	0	Reserved
								SIZSFRSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
SIZSFRSTZ	R/W	0	1	Control SIZ_RSTZ. 0: Reset macro 1: Cancel reset

When transaction doesn't occur to SIZ macro, it's possible to assert SIZ\_RSTZ by asserting SIZSFRSTZ. De-Assert a safe reset after an end of transaction. The state of the transaction can be confirmed in [Addr:0x03D0] TRANEXIST (transaction status register).



### 3.2.85 ROT safe reset control register

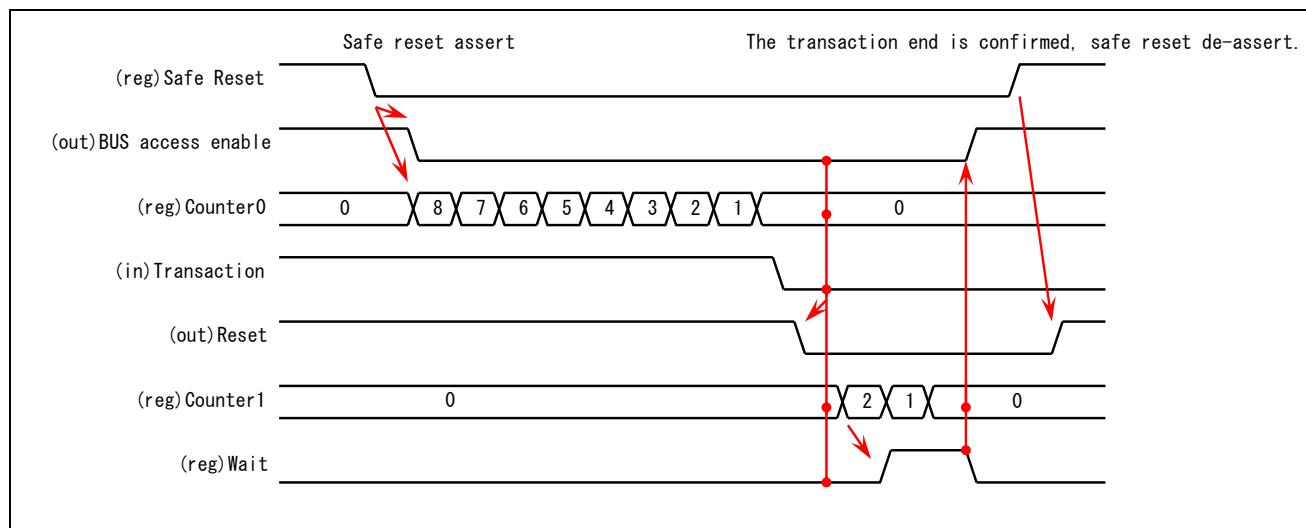
This register (ROT\_SAFE\_RESET: E011\_01ACH) controls the safe reset of the ROT macro.

31	30	29	28	27	26	25	24	Reserved
23	22	21	20	19	18	17	16	Reserved
15	14	13	12	11	10	9	8	Reserved
7	6	5	4	3	2	1	0	Reserved
								ROTSFRSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	-	Reserved. If these bits are read, 0 is returned for each bit.
ROTSFRSTZ	R/W	0	1	Control ROT_RSTZ. 0: Reset macro 1: Cancel reset

When transaction doesn't occur to ROT macro, it's possible to assert ROT\_RSTZ by asserting ROTSFRSTZ. De-Assert a safe reset after an end of transaction. The state of the transaction can be confirmed in [Addr:0x03D0] TRANEXIST (transaction status register).



### 3.2.86 IMC safe reset control register

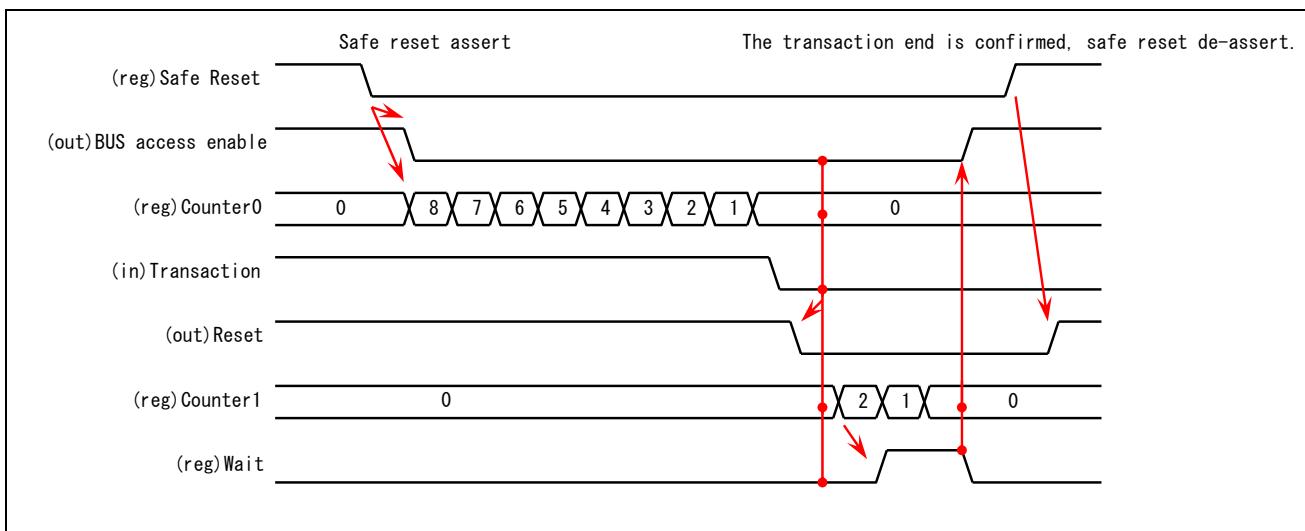
This register (IMC\_SAFE\_RESET: E011\_01B0H) controls the safe reset of the IMC macro.

31	30	29	28	27	26	25	24	Reserved
23	22	21	20	19	18	17	16	Reserved
15	14	13	12	11	10	9	8	Reserved
7	6	5	4	3	2	1	0	Reserved
								IMCSFRSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	-	Reserved. If these bits are read, 0 is returned for each bit.
IMCSFRSTZ	R/W	0	1	Control IMC_RSTZ. 0: Reset macro 1: Cancel reset

When transaction doesn't occur to IMC macro, it's possible to assert IMC\_RSTZ by asserting IMCSFRSTZ. De-Assert a safe reset after an end of transaction. The state of the transaction can be confirmed in [Addr:0x03D0] TRANEXIST (transaction status register).



### 3.2.87 IMCW safe reset control register

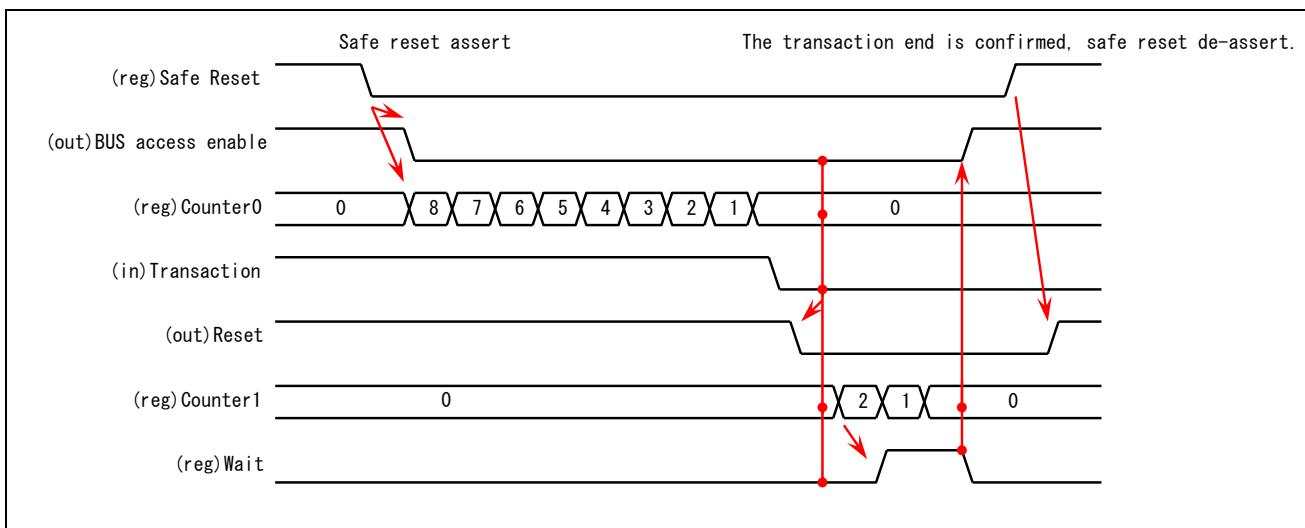
This register (IMCW\_SAFE\_RESET: E011\_01B4H) controls the safe reset of the IMCW macro.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								
7	6	5	4	3	2	1	0	
Reserved								IMCWSFRSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
IMCWSFRSTZ	R/W	0	1	Control IMCW_RSTZ. 0: Reset macro 1: Cancel reset

When transaction doesn't occur to IMCW macro, it's possible to assert IMCW\_RSTZ by asserting IMCWSFRSTZ. De-Assert a safe reset after an end of transaction. The state of the transaction can be confirmed in [Addr:0x03D0] TRANEXIST (transaction status register).



### 3.2.88 M2M safe reset control register

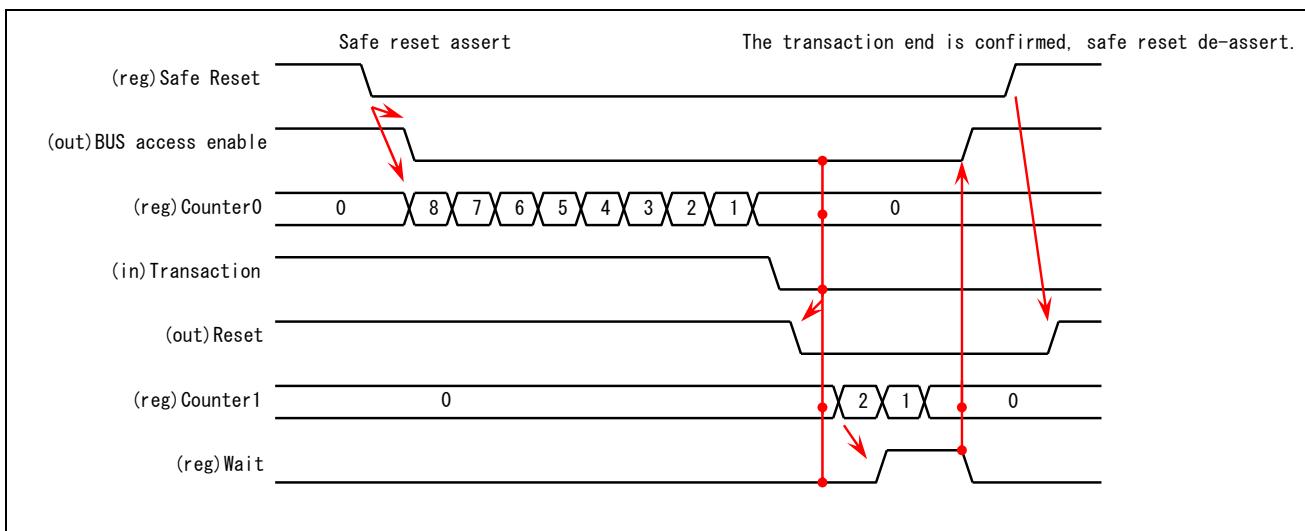
This register (M2M\_SAFE\_RESET: E011\_01B8H) controls the safe reset of the M2M macro.

31	30	29	28	27	26	25	24	Reserved
23	22	21	20	19	18	17	16	Reserved
15	14	13	12	11	10	9	8	Reserved
7	6	5	4	3	2	1	0	Reserved
								M2MSFRSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	-	Reserved. If these bits are read, 0 is returned for each bit.
M2MSFRSTZ	R/W	0	1	Control M2M_RSTZ. 0: Reset macro 1: Cancel reset

When transaction doesn't occur to M2M macro, it's possible to assert M2M\_RSTZ by asserting M2MSFRSTZ. De-Assert a safe reset after an end of transaction. The state of the transaction can be confirmed in [Addr:0x03D0] TRANEXIST (transaction status register).



### 3.2.89 M2P safe reset control register

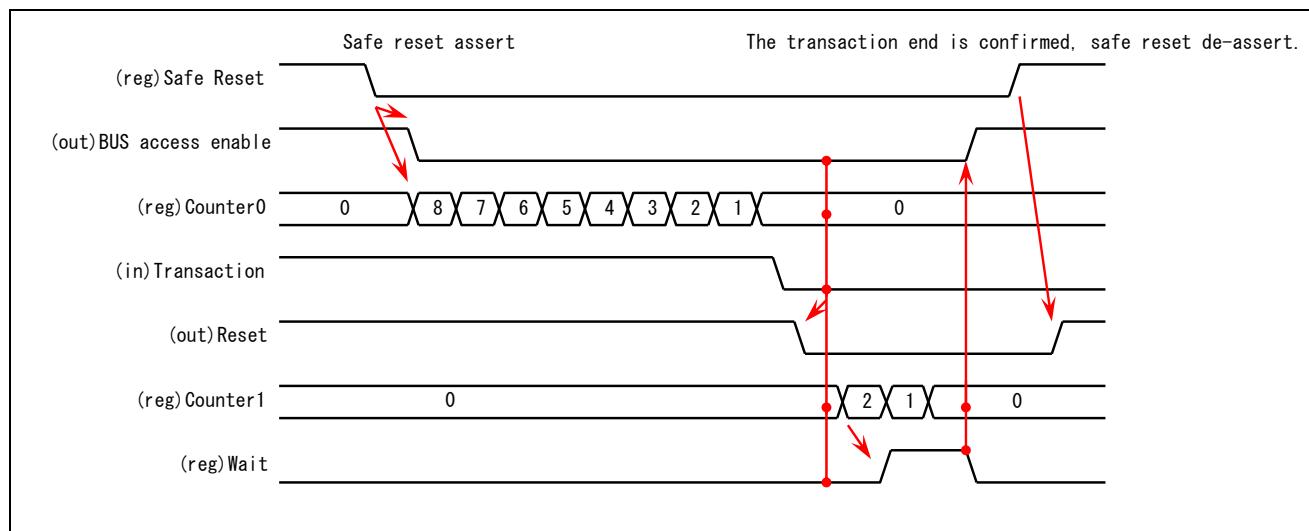
This register (M2P\_SAFE\_RESET: E011\_01BCH) controls the safe reset of the M2P macro.

31	30	29	28	27	26	25	24	Reserved
23	22	21	20	19	18	17	16	Reserved
15	14	13	12	11	10	9	8	Reserved
7	6	5	4	3	2	1	0	Reserved
								M2PSFRSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	-	Reserved. If these bits are read, 0 is returned for each bit.
M2PSFRSTZ	R/W	0	1	Control M2P_RSTZ. 0: Reset macro 1: Cancel reset

When transaction doesn't occur to M2P macro, it's possible to assert M2P\_RSTZ by asserting M2PSFRSTZ. De-Assert a safe reset after an end of transaction. The state of the transaction can be confirmed in [Addr:0x03D0] TRANEXIST (transaction status register).



### 3.2.90 P2M safe reset control register

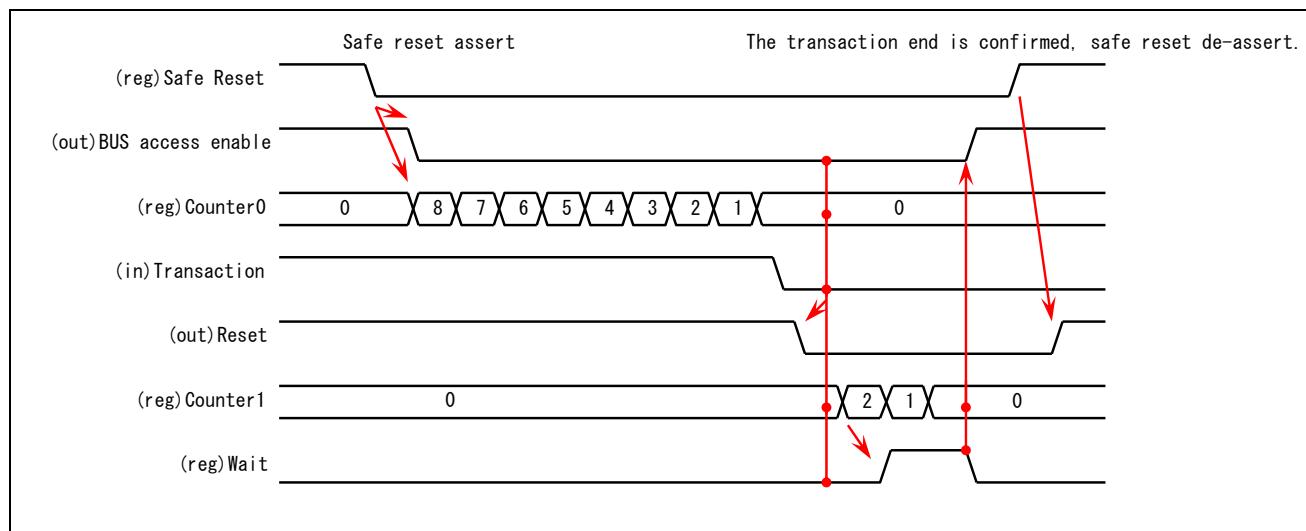
This register (P2M\_SAFE\_RESET: E011\_01C0H) controls the safe reset of the P2M macro.

31	30	29	28	27	26	25	24	Reserved
23	22	21	20	19	18	17	16	Reserved
15	14	13	12	11	10	9	8	Reserved
7	6	5	4	3	2	1	0	Reserved
								P2MSFRSTZ

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	-	Reserved. If these bits are read, 0 is returned for each bit.
P2MSFRSTZ	R/W	0	1	Control P2M_RSTZ. 0: Reset macro 1: Cancel reset

When transaction doesn't occur to P2M macro, it's possible to assert P2M\_RSTZ by asserting P2MSFRSTZ. De-Assert a safe reset after an end of transaction. The state of the transaction can be confirmed in [Addr:0x03D0] TRANEXIST (transaction status register).



### 3.2.91 Reset clock control specification register

This register (RSTZ\_CLKREQ: E011\_01C8H) specifies whether to enable or disable the clock and the number of clock cycles to input when a reset register value is changed.

31	30	29	28	27	26	25	24
Reserved		RSTZGRP3_CLKREQ_ENA		RSTZGRP3_CLKREQ_WDH			
23	22	21	20	19	18	17	16
Reserved		RSTZGRP2_CLKREQ_ENA		RSTZGRP2_CLKREQ_WDH			
15	14	13	12	11	10	9	8
Reserved		RSTZGRP1_CLKREQ_ENA		RSTZGRP1_CLKREQ_WDH			
7	6	5	4	3	2	1	0
Reserved		RSTZGRP0_CLKREQ_ENA		RSTZGRP0_CLKREQ_WDH			

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:29	–	Reserved. If these bits are read, 0 is returned for each bit.
RSTZGRP3_CLKREQ_ENA	R/W	28	1	Specify whether to enable the clock forcibly when the setting of a reset register for a macro included in group 3 is changed. 0: Disable 1: Enable (It's set as an enable certainly at Synchronous Reset. (Clock automatic control On))
RSTZGRP3_CLKREQ_WDH	R/W	27:24	FH	Specify the number of clock cycles to supply, if bit 28 is 1, when the reset register is changed. The clock will be supplied for (specified value + 1) cycles. (Clock count of PCLK)
Reserved	R	23:21	–	Reserved. If these bits are read, 0 is returned for each bit.
RSTZGRP2_CLKREQ_ENA	R/W	20	1	Specify whether to enable the clock forcibly when the setting of a reset register for a macro included in group 2 is changed. 0: Disable 1: Enable (It's set as an enable certainly at Synchronous Reset. (Clock automatic control On))
RSTZGRP2_CLKREQ_WDH	R/W	19:16	FH	Specify the number of clock cycles to supply, if bit 20 is 1, when the reset register is changed. The clock will be supplied for (specified value + 1) cycles. (Clock count of PCLK)

(2/2)

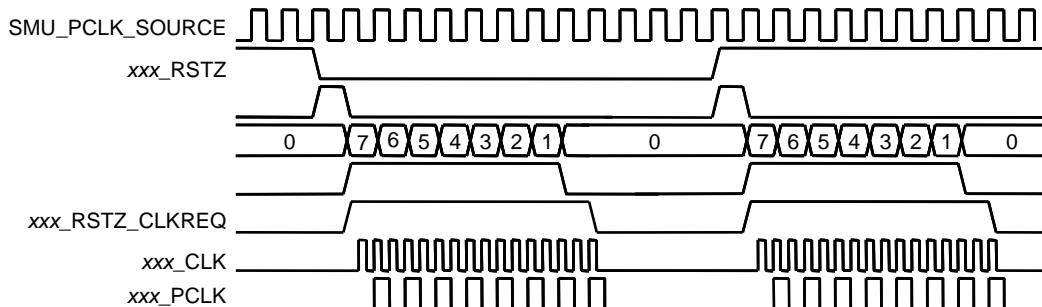
Name	R/W	Bit No.	After Reset	Description
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
RSTZGRP1_CLKREQ_ENA	R/W	12	1	Specify whether to enable the clock forcibly when the setting of a reset register for a macro included in group 1 is changed. 0: Disable 1: Enable (It's set as an enable certainly at Synchronous Reset. (Clock automatic control On))
RSTZGRP1_CLKREQ_WDH	R/W	11:8	FH	Specify the number of clock cycles to supply, if bit 12 is 1, when the reset register is changed. The clock will be supplied for (specified value + 1) cycles. (Clock count of PCLK)
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.
RSTZGRP0_CLKREQ_ENA	R/W	4	1	Specify whether to enable the clock forcibly when the setting of a reset register for a macro included in group 0 is changed. 0: Disable 1: Enable (It's set as an enable certainly at Synchronous Reset. (Clock automatic control On))
RSTZGRP0_CLKREQ_WDH	R/W	3:0	FH	Specify the number of clock cycles to supply, if bit 4 is 1, when the reset register is changed. The clock will be supplied for (specified value + 1) cycles. (Clock count of PCLK)

The reset signals are classified into the groups shown in the table below. When the value specified for a reset control register for a macro changes, the clock is supplied to the macro for the number of cycles specified in this register.

Group No.	Group 0	Group 1	Group 2	Group 3
31	–	–	–	LCD_ARSTZ
30	–	–	–	A3D_RSTZ
29	–	PDMA_RSTZ	–	AVE_CRSTZ
28	–	TW4_RSTZ	–	AVE_ARSTZ
27	CPU_PRSTDBGZ	–	IIC1_RSTZ	AVE_PRSTZ
26	P2M_RSTZ	–	IIC0_RSTZ	–
25	ROM_RSTZ	–	USIB_SAFE_SRSTZ	ROT_RSTZ
24	M2M_RSTZ	–	–	SIZ_RSTZ
23	M2P_RSTZ	–	–	CAM_RSTZ
22	PBL1_RSTZ	–	USIB_U3_SRSTZ	CAM_SAFE_RSTZ
21	PBL0_RSTZ	–	USIB_U3_ARSTZ	–
20	AHB_RSTZ	AFS_RSTZ	USIB_U2_SRSTZ	–
19	CHG1_RSTZ	USB1_RSTZ	USIB_U2_ARSTZ	LCD_RSTZ
18	CHG_RSTZ	USB1_SAFE_RSTZ	USIB_U1_SRSTZ	IMCW_RSTZ
17	–	USB0_RSTZ	USIB_U1_ARSTZ	IMC_RSTZ

16	MEMC_RSTZ	USB0_SAFE_RSTZ	USIB_S5_SRSTZ	PWM_RSTZ
15	SRC_RSTZ	-	USIB_S5_ARSTZ	NTS_RSTZ
14	AB0_RSTZ	STI_RSTZ	USIB_S4_SRSTZ	DTV_RSTZ
13	PMU_RSTZ	TG5_RSTZ	USIB_S4_ARSTZ	DTV_SAFE_RSTZ
12	INTA_RSTZ	TG4_RSTZ	USIB_S3_SRSTZ	-
11	GIO_RSTZ	TG3_RSTZ	USIB_S3_ARSTZ	-
10	BUS1_RSTZ	TG2_RSTZ	USIB_S2_SRSTZ	CFI_RSTZ
9	BUS0_RSTZ	TG1_RSTZ	USIB_S2_ARSTZ	CFI_SAFE_RSTZ
8	-	TG0_RSTZ	USIA_SAFE_SRSTZ	-
7	-	TW3_RSTZ	-	SDC_RSTZ
6	-	TW2_RSTZ	-	SDC_SAFE_RSTZ
5	CPUDE_RESET0Z	TW1_RSTZ	USIA_U0_SRSTZ	SDIO2_RSTZ
4	CPUDE_RESET1Z	TW0_RSTZ	USIA_U0_ARSTZ	SDIO2_SAFE_RSTZ
3	CPUCPU_RESET0Z	TI3_RSTZ	USIA_S1_SRSTZ	SDIO1_RSTZ
2	CPUCPU_RESET1Z	TI2_RSTZ	USIA_S1_ARSTZ	SDIO1_SAFE_RSTZ
1	CPUPO_RESETZ	TI1_RSTZ	USIA_S0_SRSTZ	SDIO0_RSTZ
0	CPUSYS_RESETZ	TI0_RSTZ	USIA_S0_ARSTZ	SDIO0_SAFE_RSTZ

Synchronous clock systems can be reset without turning off the automatic clock control, by generating a clock request signal when asserting or deasserting the reset signal so as to output the requested clock forcibly, as shown below.



### 3.2.92 Watchdog timer forced reset control register

This register (WDT\_INT\_RESET: E011\_01D0H) controls the watchdog timer reset signal.

31	30	29	28	27	26	25	24
Reserved		CPU_RST_MODE		Reserved		CPUALL_WDTRST	
23	22	21	20	19	18	17	16
Reserved		TW4_RSTREQ		Reserved		TW1_RSTREQ	TW0_RSTREQ
15	14	13	12	11	10	9	8
Reserved							CPU_WDTRST_MODE[1:0]
7	6	5	4	3	2	1	0
Reserved							CPU_WDTRST[1:0]

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:29	–	Reserved. If these bits are read, 0 is returned for each bit.
CPU_RST_MODE	R/W	28	0	Specify how to assert the reset signal for CPU0 and CPU1 by using the watchdog timer. 0: Use a forced reset. 1: Use a safe reset.
Reserved	R	27:25	–	Reserved. If these bits are read, 0 is returned for each bit.
CPUALL_WDTRST	R/W	24	0	0: Asserts each CPU0 and CPU1 reset when TW0 and TW1 run out. 1: Asserts both CPU0 and CPU1 reset whether TW0 or TW1 run out.
Reserved	R	23:21	–	Reserved. If these bits are read, 0 is returned for each bit.
TW4_RSTREQ	R/W	20	0	Control the ERR_RST_REQB pin (external reset request signal) when TW4 runs out. 0: Do not assert ERR_RST_REQB. 1: Assert ERR_RST_REQB.
Reserved	R	19:18	–	Reserved. If these bits are read, 0 is returned for each bit.
TW1_RSTREQ	R/W	17	0	Control the ERR_RST_REQB pin (external reset request signal) when TW1 runs out. 0: Do not assert ERR_RST_REQB. 1: Assert ERR_RST_REQB.
TW0_RSTREQ	R/W	16	0	Control the ERR_RST_REQB pin (external reset request signal) when TW0 runs out. 0: Do not assert ERR_RST_REQB. 1: Assert ERR_RST_REQB.
Reserved	R	15:10	–	Reserved. If these bits are read, 0 is returned for each bit.

(2/2)

Name	R/W	Bit No.	After Reset	Description
CPU_WDTRST_MODE	R/W	9:8	0H	<p>Control the CPU reset asserted as specified by the CPU_WDTRST bit.</p> <p>Bit 9: Specify how the CPU0 reset is controlled. Bit 8: Specify how the CPU1 reset is controlled. 0: Cancel reset after a specific period has elapsed. 1: Keep the reset asserted.</p> <p>(Clear the CPUDERESETxZ and CPUCPURESETxZ bits of the CPU_RSTCTRLx register to 0.)</p>
Reserved	R	7:2	–	Reserved. If these bits are read, 0 is returned for each bit.
CPU_WDTRST	R/W	1:0	0H	<p>Control the CPU reset when TW runs out</p> <p>Bit 1: Specify how the CPU1 reset is controlled when TW1 runs out. Bit 0: Specify how the CPU0 reset is controlled when TW0 runs out. 0: Do not assert a CPU reset. 1: Assert a CPU reset.</p>

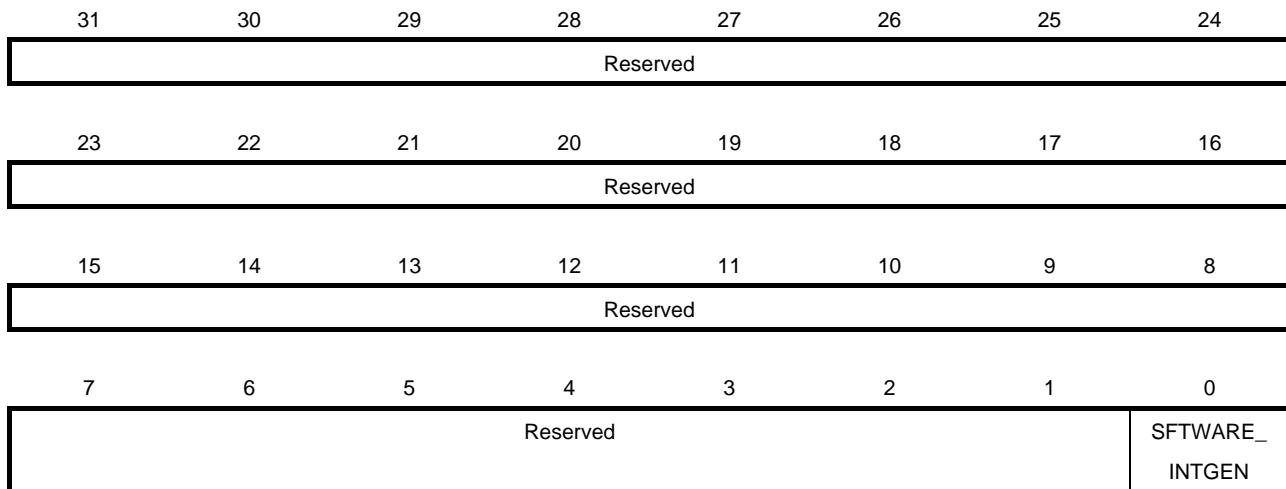
The conditions for asserting ERR\_RST\_REQB (external reset request signal, active low) are as follows:

- PMU\_ERR\_RST\_REQZ = 0 (WDT reset request from PMU)
- TIM\_TW0\_INT = 1 when TW0\_RSTREQ = 1 (TW0 runs out)
- TIM\_TW4\_INT = 1 when TW4\_RSTREQ = 1 (TW4 runs out)

The asserted ERR\_RST\_REQB (external reset request signal) can be cancelled by a system reset (SRESETB).

### 3.2.93 Software interrupt source setting register

This register (SFTWARE\_INTGEN: E011\_01DCH) enables software interrupts.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
SFTWARE_INTGEN	W	0	0	Software interrupts occur. If 1 is written, SMU interrupts occur. It isn't necessary to be interrupt factor clearance at this register. ("0" writing in is unnecessary.)

### 3.2.94 Interrupt status register

This read-only register (INT\_STATUS: E011\_01E0H) indicates the status of the interrupt source enabled with the interrupt enable set register can be read.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								INT_STATUS8
7	6	5	4	3	2	1	0	
Reserved								INT_STATUS0

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:9	–	Reserved. If these bits are read, 0 is returned for each bit.
INT_STATUS8	R	8	0	Indicates the software interrupt status when the corresponding bit in the interrupt enable set register is set.
Reserved	R	7:1	–	Reserved. If these bits are read, 0 is returned for each bit.
INT_STATUS0	R	0	0	Indicates the clock mode change interrupt status when the corresponding bit in the interrupt enable set register is set.

### 3.2.95 Interrupt raw status register

This read-only register (INT\_RAW\_STATUS: E011\_01E4H) indicates the relevant interrupt status. An interrupt source is set to this register regardless of the settings of the interrupt enable set register and the interrupt enable clear register.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							INT_RAW_STATUS8
7	6	5	4	3	2	1	0
Reserved							INT_RAW_STATUS0

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:9	–	Reserved. If these bits are read, 0 is returned for each bit.
INT_RAW_STATUS8	R	8	0	Indicates software interrupt raw status.
Reserved	R	7:1	–	Reserved. If these bits are read, 0 is returned for each bit.
INT_RAW_STATUS0	R	0	0	Indicates clock mode change interrupt raw status.

### 3.2.96 Interrupt enable set register

This register (INT\_ENSET: E011\_01E8H) enables the relevant interrupt.

Writing 0 to this register does not affect the setting. The interrupt request issuance enable status can be checked by reading this register.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								INT_ENSET8
7	6	5	4	3	2	1	0	
Reserved								INT_ENSET0

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:9	–	Reserved. If these bits are read, 0 is returned for each bit.
INT_ENSET8	R/W	8	0	Specify whether to enable the software interrupt. 0: Retain the interrupt enable state. 1: Enable the interrupt.
Reserved	R	7:1	–	Reserved. If these bits are read, 0 is returned for each bit.
INT_ENSET0	R/W	0	0	Specify whether to enable the clock mode change interrupt. 0: Retain the interrupt enable state. 1: Enable the interrupt.

### 3.2.97 Interrupt enable clear register

This register (INT\_ENCLR: E011\_01ECH) clears the interrupt enabled state.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							INT_ENCLR8
7	6	5	4	3	2	1	0
Reserved							INT_ENCLR0

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:9	–	Reserved. If these bits are read, 0 is returned for each bit.
INT_ENCLR8	W	8	0	Specify whether to clear the software interrupt enabled state. 0: Retain the interrupt enable state. 1: Clear the interrupt enable state.
Reserved	R	7:1	–	Reserved. If these bits are read, 0 is returned for each bit.
INT_ENCLR0	W	0	0	Specify whether to clear the clock mode change interrupt enabled state. 0: Retain the interrupt enable state. 1: Clear the interrupt enable state.

### 3.2.98 Interrupt clear register

This register (INT\_CLEAR: E11\_01F0H) clears the interrupt source.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							INT_CLEAR8
7	6	5	4	3	2	1	0
Reserved							INT_CLEAR0

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:9	–	Reserved. If these bits are read, 0 is returned for each bit.
INT_CLEAR8	W	8	0	Specify whether to clear the software interrupt source. 0: Retains the interrupt source. 1: Clears the interrupt source.
Reserved	R	7:1	–	Reserved. If these bits are read, 0 is returned for each bit.
INT_CLEAR0	W	0	0	Specify whether to clear the clock mode change interrupt source. 0: Retains the interrupt source. 1: Clears the interrupt source.

### 3.2.99 System PLL1 setting register 0

This register (PLL1CTRL0: E011\_0200H) specifies the PLL1 multiplication ratio.

31	30	29	28	27	26	25	24
Reserved		OSC_SEL		Reserved			
23	22	21	20	19	18	17	16
Reserved			PLL1_P_VAL				
15	14	13	12	11	10	9	8
Reserved		PLL1_M_VAL					
7	6	5	4	3	2	1	0
PLL1_N_VAL							

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:30	–	Reserved. If these bits are read, 0 is returned for each bit.
OSC_SEL	R/W	29:28	0H	Select the oscillator used for the PLL1 reference clock. (Change this setting while PLL1 is on standby.) 0: OSC0 1: OSC1 2: EXT_CLKI 3: Reserved (Setting prohibited)
Reserved	R	27:20	–	Reserved. If these bits are read, 0 is returned for each bit.
PLL1_P_VAL	R/W	19:16	1H	These bits correspond to the P[3:0] pins of PLL1. 0H: Setting prohibited 1H: pr = 2 (400 MHz ≤ fout ≤ 533 MHz) 2H: pr = 4 (200 MHz ≤ fout ≤ 400 MHz) 3H: pr = 4 (200 MHz ≤ fout ≤ 400 MHz) 4H: pr = 6 (133.34 MHz ≤ fout ≤ 266.66 MHz) 5H: pr = 6 (133.34 MHz ≤ fout ≤ 266.66 MHz) 6H: pr = 8 (100 MHz ≤ fout ≤ 200 MHz) 7H: pr = 8 (100 MHz ≤ fout ≤ 200 MHz) 8H: pr = 10 (80 MHz ≤ fout ≤ 160 MHz) 9H: pr = 10 (80 MHz ≤ fout ≤ 160 MHz) AH: pr = 12 (66.67 MHz ≤ fout ≤ 133.33 MHz) BH: pr = 12 (66.67 MHz ≤ fout ≤ 133.33 MHz) CH: pr = 14 (57.15 MHz ≤ fout ≤ 114.28 MHz) DH: pr = 14 (57.15 MHz ≤ fout ≤ 114.28 MHz) EH: pr = 16 (50 MHz ≤ fout ≤ 100 MHz) FH: pr = 16 (50 MHz ≤ fout ≤ 100 MHz)
Reserved	R	15	–	Reserved. If this bit is read, 0 is returned.

(2/2)

Name	R/W	Bit No.	After Reset	Description
PLL1_M_VAL	R/W	14:8	04H	These bits correspond to the M[6:0] pins of PLL1. mr = M[6:0] + 1
PLL1_N_VAL	R/W	7:0	DDH	These bits correspond to the N[7:0] pins of PLL1. nr = N[7:0] + 1 00H to 0FH: Setting prohibited

Arithmetic expression of an output frequency of PLL1 (fout) and the inner vco frequency (fvco).

$$\text{fout} = (\text{fstd} * \text{nr}) / (\text{mr} * \text{pr})$$

$$\text{fvco} = (\text{fout} * \text{pr}) = (\text{fstd} * \text{nr}) / (\text{mr})$$

$$50\text{MHz} \leq \text{fout} \leq 533\text{MHz}$$

### 3.2.100 System PLL1 setting register 1

This register (PLL1CTRL1: E011\_0204H) specifies the STBY pins of PLL1.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
PLL1_STANDBY							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:8	–	Reserved. If these bits are read, 0 is returned for each bit.
PLL1_STANDBY	R/W	7:0	FFH	These bits correspond to the STBY pins of PLL1. 00H to FEH: Not on standby (oscillation enabled) FFH: On standby (oscillation disabled)

Wait for 200 us after PLL1 is taken off standby (PLL1\_STANDBY = 0); the PLL1 output can then be used as a clock.  
PLL1 goes on standby when all of bits PLL1\_STANDBY0 to PLL1\_STANDBY7 are set to 1.

But, when setting a reference clock of PLL1 (PLL1CTRL0 [29:28]) as OSC0/OSC1, release a stand-by of  
OSC0/OSC1 first, and after PLL\_STATUS [16] or [20] was 1, set it as PLL1\_STANDBY=0x00.

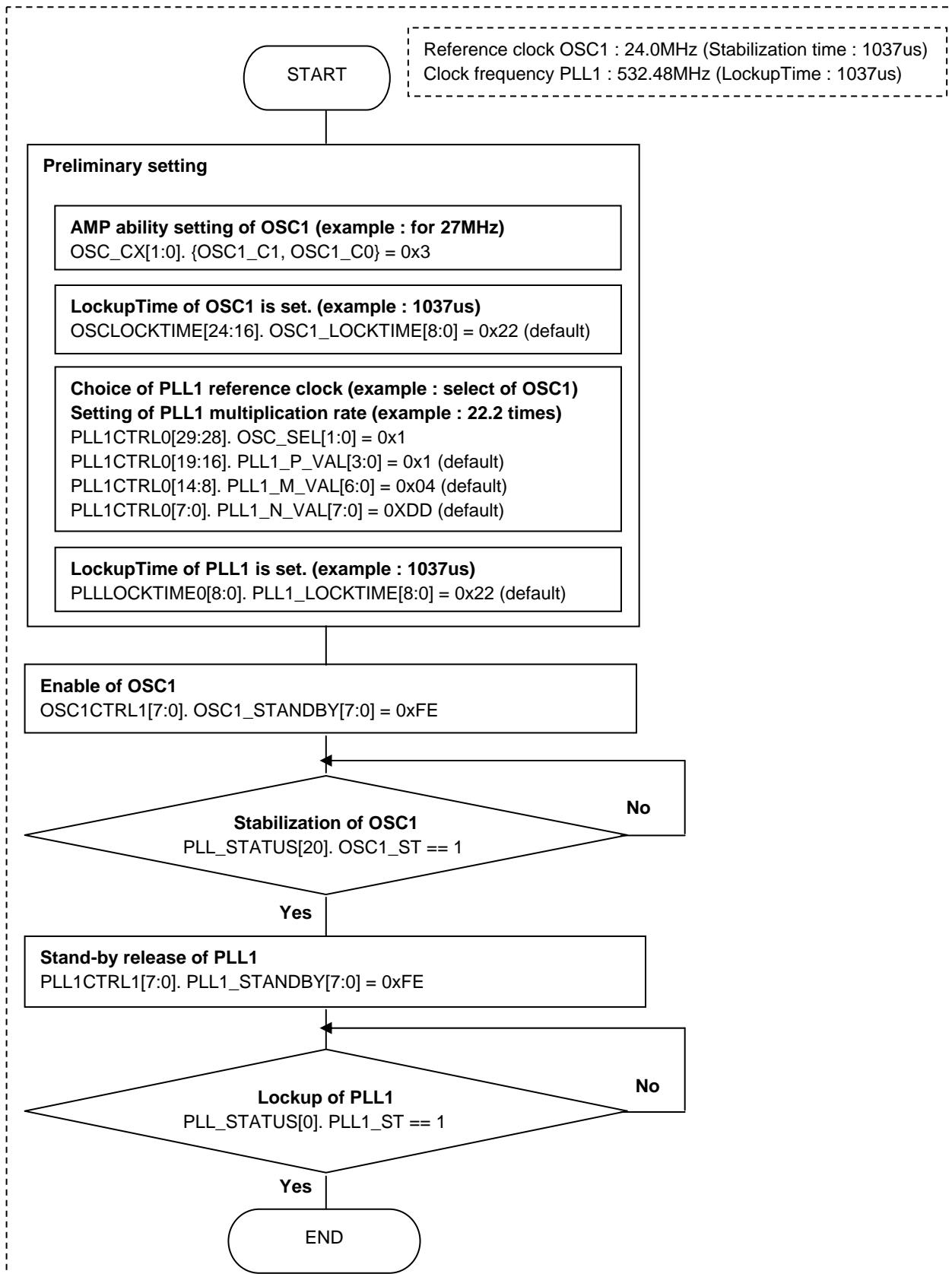
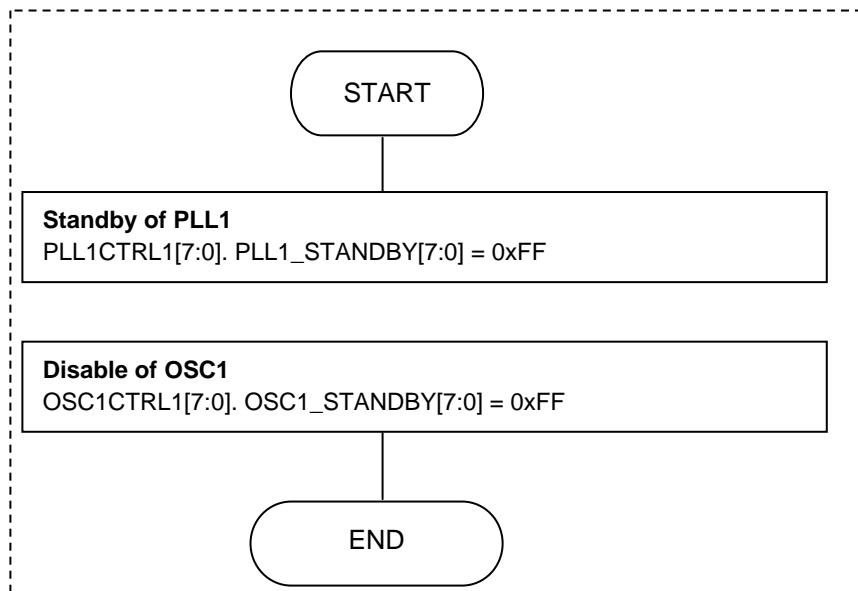
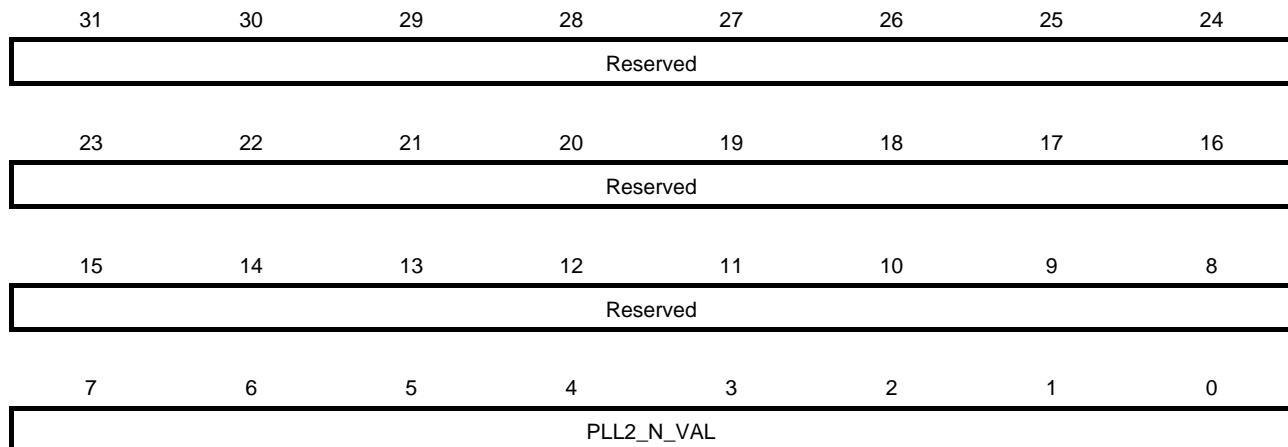
**Figure 3-1. PLL1 is oscillated**

Figure 3-2. Oscillation of PLL1 is suspended



### 3.2.101 System PLL2 setting register 0

This register (PLL2CTRL0: E011\_0208H) specifies the PLL2 multiplication ratio.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:8	–	Reserved. If these bits are read, 0 is returned for each bit.
PLL2_N_VAL	R/W	7:0	79H	<p>These bits correspond to the N[7:0] pins of PLL2 (reference clock: 32.768 kHz).</p> <p>00H to 4DH: Setting prohibited</p> <p>4EH: 78 (<math>\times 9875</math>)</p> <p>...</p> <p>5FH: 95 (<math>\times 12000</math>)</p> <p>60H: 96 (<math>\times 12125</math>)</p> <p>...</p> <p>78H: 120 (<math>\times 15125</math>)</p> <p>79H: 121 (<math>\times 15250</math>): Default (= 499.712 MHz)</p> <p>...</p> <p>81H: 129 (<math>\times 16250</math>)</p> <p>82H to FFH: Setting prohibited</p>

**Remarks** 1. PLL2 output frequency (FO) = 32768 (FR : input reference clock)  $\times$  125  $\times$  (PLL2\_N\_VAL + 1).

Specify the output frequency range so as to be from 320 MHz to 533 MHz.

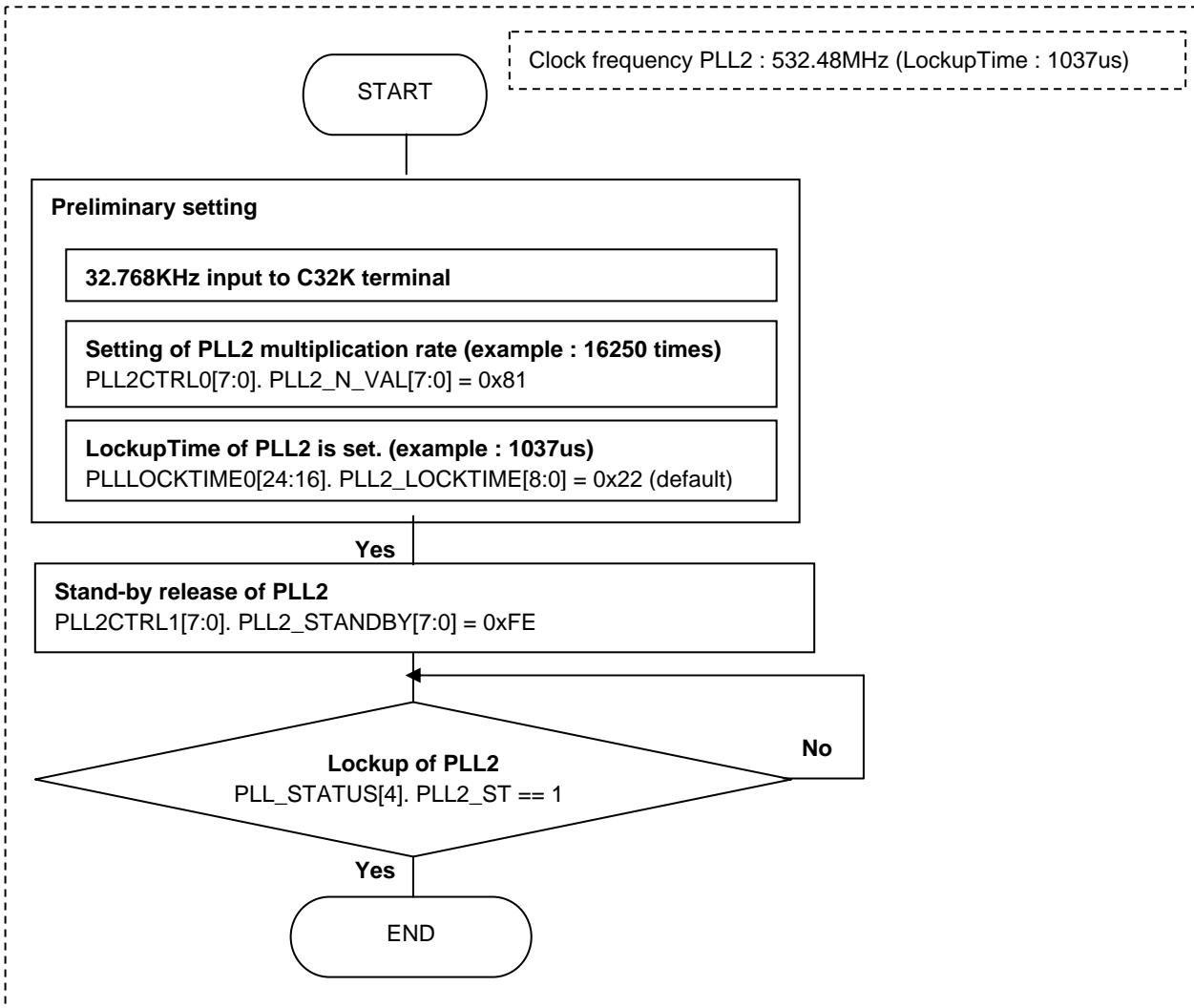
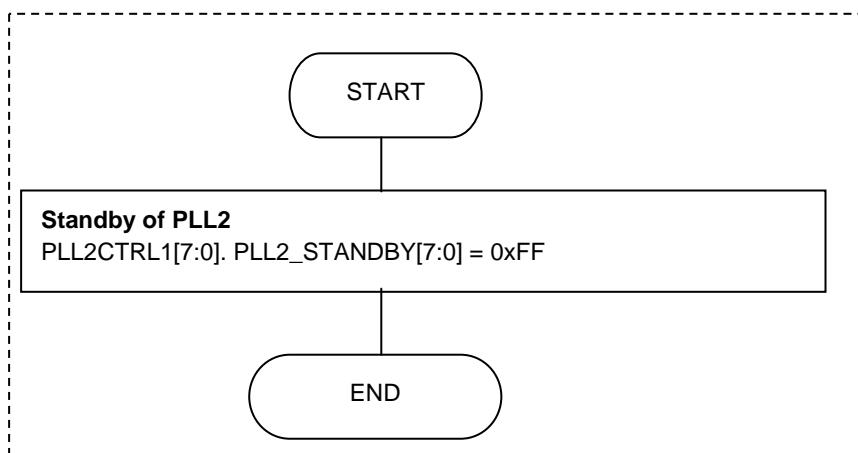
2. Change the PLL2 multiplication ratio when PLL2 is not used as the clock.

### 3.2.102 System PLL2 setting register 1

This register (PLL2CTRL1: E011\_020CH) specifies the STBY pins of PLL2.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
PLL2_STANDBY							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:8	–	Reserved. If these bits are read, 0 is returned for each bit.			
PLL2_STANDBY	R/W	7:0	FFH	These bits correspond to the STBY pins of PLL2. 00H to FEH: Not on standby (oscillation enabled) FFH: On standby (oscillation disabled)			

Wait for 2 ms after PLL2 is taken off standby (PLL2\_STANDBY = 0); the PLL2 output can then be used as a clock.  
 PLL2 goes on standby when all of bits PLL2\_STANDBY0 to PLL2\_STANDBY7 are set to 1.

**Figure 3-3. PLL2 is oscillated****Figure 3-4. Oscillation of PLL2 is suspended**

### 3.2.103 System PLL3 setting register 0

This register (PLL3CTRL0: E011\_0210H) specifies the PLL3 multiplication ratio.

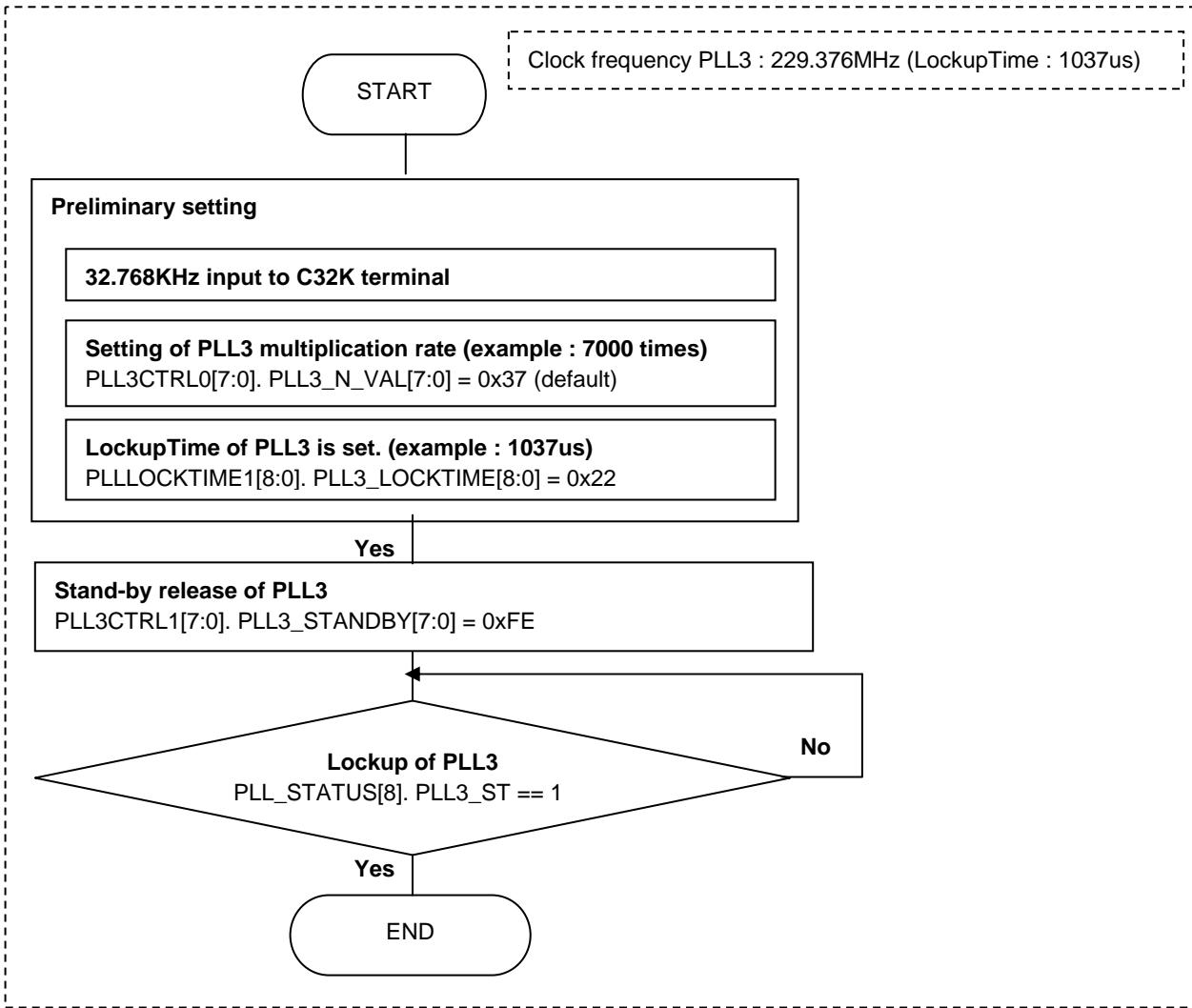
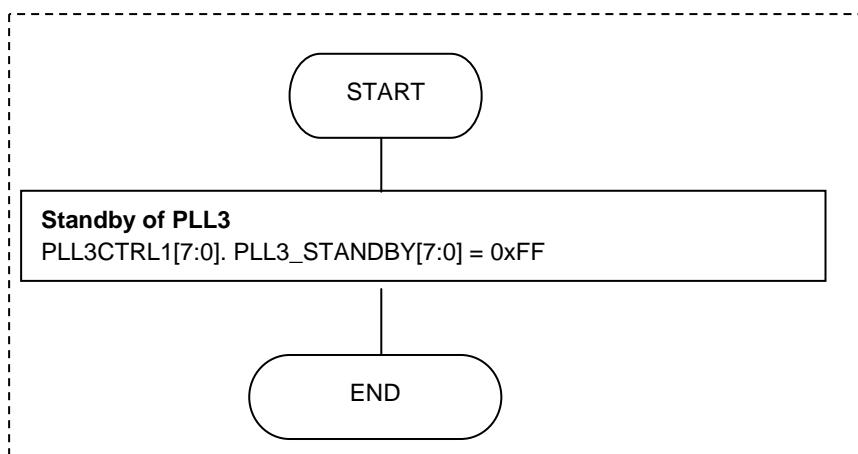
31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								
7	6	5	4	3	2	1	0	
Reserved	PLL3_N_VAL							
Name	R/W	Bit No.	After Reset	Description				
Reserved	R	31:7	–	Reserved. If these bits are read, 0 is returned for each bit.				
PLL3_N_VAL	R/W	6:0	37H	These bits correspond to the N[6:0] pins of PLL3. 37H: 55 (x7000): Default (= 229.376 MHz) Don't change the setting from defaults value.				

### 3.2.104 System PLL3 setting register 1

This register (PLL3CTRL1: E011\_0214H) specifies the STBY pins of PLL3.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
PLL3_STANDBY							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:8	–	Reserved. If these bits are read, 0 is returned for each bit.			
PLL3_STANDBY	R/W	7:0	00H	These bits correspond to the STBY pins of PLL3. 00H to FEH: Not on standby (oscillation enabled) FFH: On standby (oscillation disabled)			

Wait for 800  $\mu$ s after PLL3 is taken off standby (PLL3\_STANDBY = 0); the PLL3 output can then be used as a clock. If an interrupt to the CPU (IRQ or FIQ) occurs in deep sleep mode, PLL3 is automatically taken off standby. When all bits of PLL3\_STANDBY0-7 are set by 1, PLL3 will be a standby.

**Figure 3-5. PLL3 is oscillated****Figure 3-6. Oscillation of PLL3 is suspended**

### 3.2.105 PLL4 serial clock setting register 0

This register (PLL4CTRL0: E011\_0218H) specifies the PLL4 multiplication ratio.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
PLL4_N_VAL							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:8	–	Reserved. If these bits are read, 0 is returned for each bit.
PLL4_N_VAL	R/W	7:0	79H	<p>These bits correspond to the N[7:0] pins of PLL4 (reference clock: 32.768 kHz).</p> <p>00H to 4DH: Setting prohibited</p> <p>4EH: 78 (<math>\times 9875</math>)</p> <p>...</p> <p>5FH: 95 (<math>\times 12000</math>)</p> <p>60H: 96 (<math>\times 12125</math>)</p> <p>...</p> <p>78H: 120 (<math>\times 15125</math>)</p> <p>79H: 121 (<math>\times 15250</math>): Default (= 499.712 MHz)</p> <p>...</p> <p>81H: 129 (<math>\times 16250</math>)</p> <p>82H to FFH: Setting prohibited</p>

**Remarks 1.** PLL4 output frequency (FO) = 32768 (FR : input reference clock)  $\times$  125  $\times$  (PLL4\_N\_VAL + 1).

Specify the output frequency range so as to be from 320 MHz to 533 MHz.

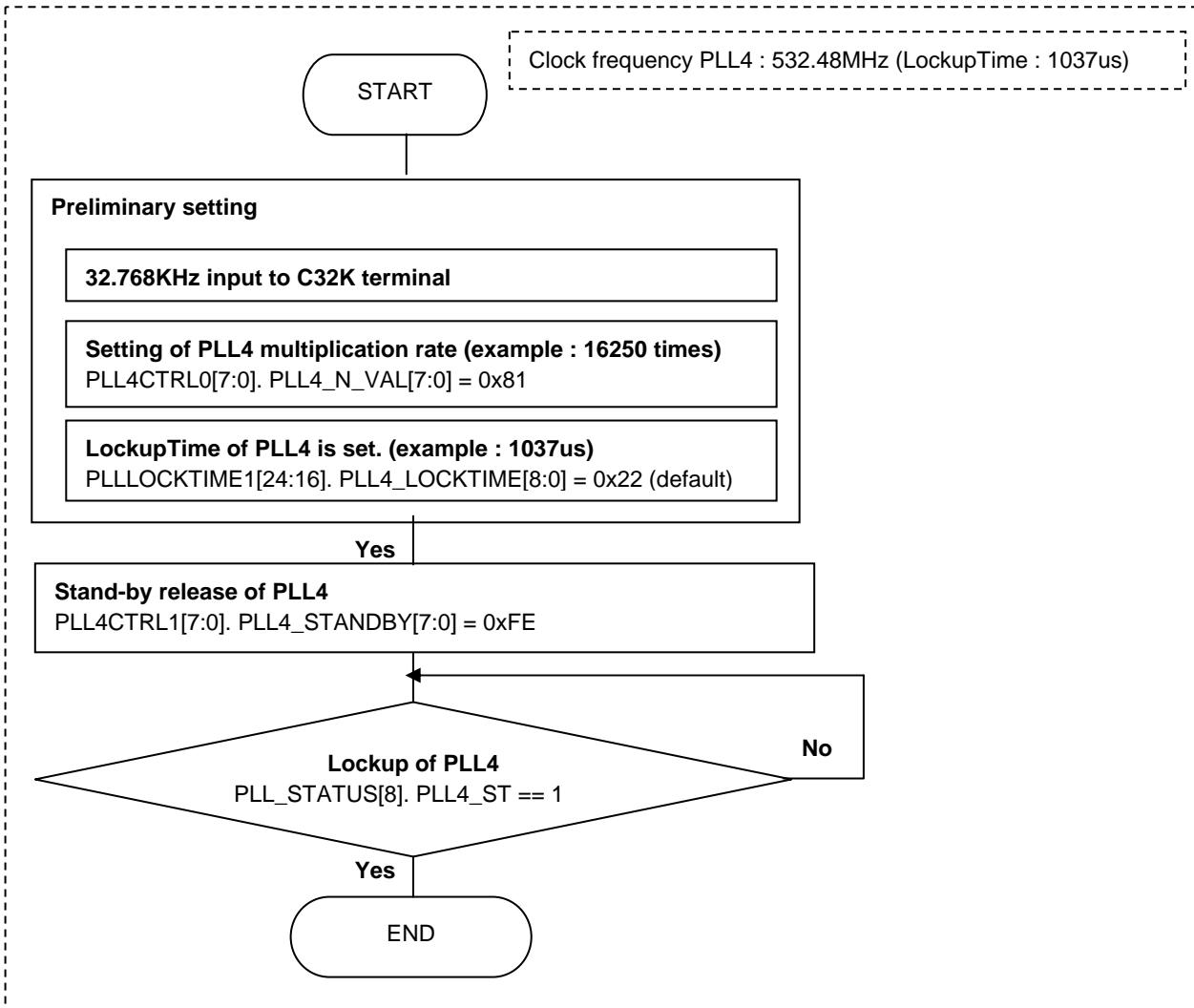
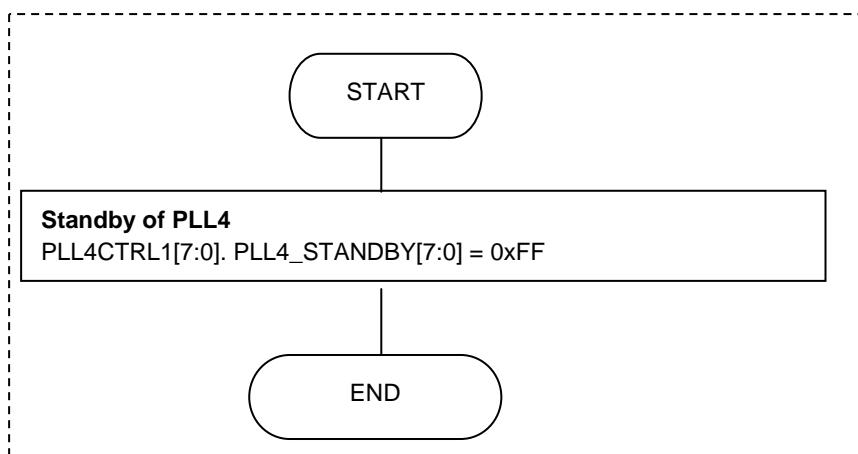
**2.** Change the PLL4 multiplication ratio when PLL4 is not used as the clock.

### 3.2.106 PLL4 serial clock setting register 1

This register (PLL4CTRL1: E011\_021CH) specifies the STBY pins of PLL4.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
PLL4_STANDBY							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:8	–	Reserved. If these bits are read, 0 is returned for each bit.			
PLL4_STANDBY	R/W	7:0	FFH	These bits correspond to the STBY pins of PLL4. 00H to FEH: Not on standby (oscillation enabled) FFH: On standby (oscillation disabled)			

Wait for 2ms after PLL4 is taken off standby (PLL4\_STANDBY = 0); the PLL4 output can then be used as a clock.  
PLL4 goes on standby when all of bits PLL4\_STANDBY0 to PLL4\_STANDBY7 are set to 1.

**Figure 3-7. PLL4 is oscillated****Figure 3-8. Oscillation of PLL4 is suspended**

### 3.2.107 System OSC0 setting register

This register (OSC0CTRL1: E011\_0220H) specifies the STBY pins of OSC0.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
OSC0_STANDBY							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:8	–	Reserved. If these bits are read, 0 is returned for each bit.			
OSC0_STANDBY	R/W	7:0	FFH	These bits correspond to the STBYZ pins of OSC0. 00H to FEH: Not on standby (oscillation enabled) FFH: On standby (oscillation disabled)			

Wait for 2 ms after OSC0 is taken off standby (OSC0\_STANDBY = 0); the OSC0 output can then be used as a clock.  
(OSC\_CX[3:2] = 3H, 1H)

Wait for 3.5 ms after OSC0 is taken off standby (OSC0\_STANDBY = 0); the OSC0 output can then be used as a clock. (OSC\_CX[3:2] = 2H, 0H)

OSC0 goes on standby when all of bits OSC0\_STANDBY0 to OSC0\_STANDBY7 are set to 1.

### 3.2.108 System OSC1 setting register

This register (OSC1CTRL1: E011\_0224H) specifies the STBY pins of OSC1.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
OSC1_STANDBY							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:8	–	Reserved. If these bits are read, 0 is returned for each bit.			
OSC1_STANDBY	R/W	7:0	FFH	These bits correspond to the STBY pins of OSC1. 00H to FEH: Not on standby (oscillation enabled) FFH: On standby (oscillation disabled)			

Wait for 2 ms after OSC1 is taken off standby (OSC1\_STANDBY = 0); the OSC1 output can then be used as a clock.  
(OSC\_CX[1:0] = 3H, 1H)

Wait for 3.5 ms after OSC1 is taken off standby (OSC1\_STANDBY = 0); the OSC1 output can then be used as a clock. (OSC\_CX[1:0] = 2H, 0H)

OSC1 goes on standby when all of bits OSC1\_STANDBY0 to OSC1\_STANDBY7 are set to 1.

### 3.2.109 PLL lockup time setting register 0

This register (PLLLOCKTIME0: E011\_0228H) specifies PLL lockup times.

31	30	29	28	27	26	25	24	Reserved	PLL2_LOCK TIME
23	22	21	20	19	18	17	16	PLL2_LOCKTIME	
15	14	13	12	11	10	9	8	Reserved	PLL1_LOCK TIME
7	6	5	4	3	2	1	0	PLL1_LOCKTIME	
Name	R/W	Bit No.	After Reset	Description					
Reserved	R	31:25	–	Reserved. If these bits are read, 0 is returned for each bit.					
PLL2_LOCKTIME	R/W	24:16	022H	Specify the PLL2 lockup time. Lockup waiting time = $1/32768 \mu s \times$ Specified value Change this setting while the PLL2_STANDBY[7:0] bits are FFH.					
Reserved	R	15:9	–	Reserved. If these bits are read, 0 is returned for each bit.					
PLL1_LOCKTIME	R/W	8:0	022H	Specify the PLL1 lockup time. Lockup waiting time = $1/32768 \mu s \times$ Specified value Change this setting while the PLL1_STANDBY[7:0] bits are FFH.					

Counting starts when at least one of bits 0 to 7 in the PLL1CTRL1 or PLL2CTRL1 registers are set to 0.

### 3.2.110 PLL lockup time setting register 1

This register (PLLLOCKTIME1: E011\_022CH) specifies PLL lockup times.

31	30	29	28	27	26	25	24	Reserved	PLL4_LOCK TIME
23	22	21	20	19	18	17	16	PLL4_LOCKTIME	
15	14	13	12	11	10	9	8	Reserved	PLL3_LOCK TIME
7	6	5	4	3	2	1	0	PLL3_LOCKTIME	
Name	R/W	Bit No.	After Reset	Description					
Reserved	R	31:25	–	Reserved. If these bits are read, 0 is returned for each bit.					
PLL4_LOCKTIME	R/W	24:16	022H	Specify the PLL4 lockup time. Lockup waiting time = $1/32768 \mu s \times$ Specified value Change this setting while the PLL4_STANDBY[7:0] bits are FFH.					
Reserved	R	15:9	–	Reserved. If these bits are read, 0 is returned for each bit.					
PLL3_LOCKTIME	R/W	8:0	032H	Specify the PLL3 lockup time. Lockup waiting time = $1/32768 \mu s \times$ Specified value Change this setting while the PLL3_STANDBY[7:0] bits are FFH.					

Counting starts when at least one of bits 0 to 7 in the PLL3CTRL1 or PLL4CTRL1 registers are set to 0.

### 3.2.111 OSC lockup time setting register

This register (OSCLOCKTIME: E011\_0230H) specifies OSC stabilization times.

31	30	29	28	27	26	25	24	Reserved	OSC1_LOCKTIME
23	22	21	20	19	18	17	16	OSC1_LOCKTIME	
15	14	13	12	11	10	9	8	Reserved	OSC0_LOCKTIME
7	6	5	4	3	2	1	0	OSC0_LOCKTIME	
Name	R/W	Bit No.	After Reset	Description					
Reserved	R	31:25	–	Reserved. If these bits are read, 0 is returned for each bit.					
OSC1_LOCKTIME	R/W	24:16	022H	Specify the OSC1 stabilization time. Stabilization waiting time = $30.5 \mu\text{s} \times$ Specified value Change this setting while the OSC1_STANDBY[7:0] bits are FFH.					
Reserved	R	15:9	–	Reserved. If these bits are read, 0 is returned for each bit.					
OSC0_LOCKTIME	R/W	8:0	022H	Specify the OSC0 stabilization time. Stabilization waiting time = $30.5 \mu\text{s} \times$ Specified value Change this setting while the OSC0_STANDBY[7:0] bits are FFH.					

Counting starts when at least one of bits 0 to 7 in the OSC0CTRL1 or OSC1CTRL1 registers are set to 0.

OSC0\_LOCKTIME [8:0] establishes it as it'll be the following waiting time.

The waiting time when OSC\_CS [3:2] = 3H, 1H is more than 2ms.

The waiting time when OSC\_CS [3:2] = 2H, 0H is more than 3.5ms.

OSC1\_LOCKTIME [8:0] establishes it as it'll be the following waiting time.

The waiting time when OSC\_CS [1:0] = 3H, 1H is more than 2ms.

The waiting time when OSC\_CS [1:0] = 2H, 0H is more than 3.5ms.

### 3.2.112 PLL status register

This register (PLL\_STATUS: E011\_0234H) indicates PLL statuses.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved		OSC1_ST	Reserved			OSC0_ST	
15	14	13	12	11	10	9	8
Reserved		PLL4_ST	Reserved			PLL3_ST	
7	6	5	4	3	2	1	0
Reserved		PLL2_ST	Reserved		PLL1_PLOCK	PLL1_ST	
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:21	–	Reserved. If these bits are read, 0 is returned for each bit.			
OSC1_ST	R	20	0	Indicates the OSC1 status. 0: On standby (before the frequency is locked) 1: Running (the frequency is locked)			
Reserved	R	19:17	–	Reserved. If these bits are read, 0 is returned for each bit.			
OSC0_ST	R	16	0	Indicates the OSC0 status. 0: On standby (before the frequency is locked) 1: Running (the frequency is locked)			
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.			
PLL4_ST	R	12	1	Indicates the PLL4 status. 0: On standby (before the frequency is locked) 1: Running (the frequency is locked)			
Reserved	R	11:9	–	Reserved. If these bits are read, 0 is returned for each bit.			
PLL3_ST	R	8	1	Indicates the PLL3 status. 0: On standby (before the frequency is locked) 1: Running (the frequency is locked)			
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.			
PLL2_ST	R	4	0	Indicates the PLL2 status. 0: On standby (before the frequency is locked) 1: Running (the frequency is locked)			
Reserved	R	3:2	–	Reserved. If these bits are read, 0 is returned for each bit.			
PLL1_PLOCK	R	1	0	Status of PLL1_PLOCK			
PLL1_ST	R	0	0	Indicates the PLL1 status. 0: On standby (before the frequency is locked) 1: Running (the frequency is locked)			

**Remark** Each bit is set to 1 after the PLL or OSC lockup stabilization waiting period has elapsed.

### 3.2.113 ROSC setting register

This register (ROSCCTRL1: E011\_0238H) specifies the STBY pins of ROSC.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							ROSC_ STANDBY

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
ROSC_STANDBY	R/W	0	0	These bits correspond to the STBY pins of ROSC. 0 : Not on standby (oscillation enabled) 1 : On standby (oscillation disabled)

A clock for AFS (ROSC: ring oscillator) is controlled.

Set this register as a standby after power supply on sequence completion.

### 3.2.114 OSC setting register

This register (OSC\_CX: E011\_0248H) specifies the OSC amplification capability.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				OSC0_C0	OSC0_C1	OSC1_C0	OSC1_C1

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:4	–	Reserved. If these bits are read, 0 is returned for each bit.
OSC0_C0	R/W	3	0	Specify the OSC0 amplification capability. C1 C0 1 1: 27 MHz 1 0: 20 MHz 0 1: 10 MHz 0 0: 4 MHz
OSC0_C1	R/W	2	0	
OSC1_C0	R/W	1	0	Specify the OSC1 amplification capability. C1 C0 1 1: 27 MHz 1 0: 20 MHz 0 1: 10 MHz 0 0: 4 MHz
OSC1_C1	R/W	0	0	

It's different in stabilization time of an OSC clock depending on setting of C0, C1 (the OSC oscillating frequency).

C0 = 1, C1 = 1 : OSC clock stabilization time is 2ms.

C0 = 0, C1 = 1 : OSC clock stabilization time is 2ms.

C0 = 1, C1 = 0 : OSC clock stabilization time is 3.5ms.

C0 = 1, C1 = 0 : OSC clock stabilization time is 3.5ms.

### 3.2.115 Automatic PLL standby mode register

This register (AUTO\_PLL\_STANDBY: E011\_02F0H) controls automatic transition to PLL standby mode.

31	30	29	28	27	26	25	24	Reserved
23	22	21	20	19	18	17	16	Reserved
15	14	13	12	11	10	9	8	Reserved
7	6	5	4	3	2	1	0	Reserved
AUTO_STAND BY_CLR								AUTO_STAND BY_CLR
								AUTO_STANDBY

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
AUTO_STANDBY_CLR	R/W	1	1	Specify whether to automatically exit the standby mode. 0: Do not automatically exit the standby mode. 1: Automatically exit the standby mode.
AUTO_STANDBY	R/W	0	0	Specify whether to enter standby mode automatically. 0: Do not automatically enter the standby mode. 1: Automatically enter the standby mode.

#### ○ Automatic standby exit mode

PLL1: If the setting of bits 3 to 0 (MODE\_SEL) of the CLK\_MODE\_SEL register is changed to switch from a mode other than normal A, B, C, and D to normal A, B, C, or D while the PLL1\_STANDBY[7:0] bits of the PLL1CTRL1 register are FFH (PLL1 is on standby) and bits 3 to 0 of the CKMODE\_PLLSEL register are 0H, the PLL1\_STANDBY[7:0] bits are automatically set to 00H.

PLL2: If the setting of bits 3 to 0 (MODE\_SEL) of the CLK\_MODE\_SEL register is changed to switch from a mode other than normal A, B, C, and D to normal A, B, C, or D while the PLL2\_STANDBY[7:0] bits of the PLL2CTRL1 register are FFH (PLL2 is on standby) and bits 3 to 0 of the CKMODE\_PLLSEL register are 4H, the PLL2\_STANDBY[7:0] bits are automatically set to 00H.

PLL3: If one of the four following conditions is met while the PLL3\_STANDBY[7:0] bits of the PLL3CTRL1 register are FFH (PLL3 is on standby), the PLL3\_STANDBY[7:0] bits are automatically set to 00H.

- (1) If the setting of bits 3 to 0 (MODE\_SEL) of the CLK\_MODE\_SEL register is changed to select the power-on mode
- (2) If the setting of bits 3 to 0 (MODE\_SEL) of the CLK\_MODE\_SEL register is changed to switch from a mode other than normal A, B, C, and D to normal A, B, C, or D
- (3) If the setting of bits 3 to 0 (MODE\_SEL) of the CLK\_MODE\_SEL register is changed to select the economy mode

- (4) If an interrupt to the CPU (IRQ or FIQ) occurs while the deep sleep mode is specified for bits 11 to 8 (MODE\_STATUS) of the CLK\_MODE\_SEL register

OSC0: If one of the four following conditions is met while the OSC0\_STANDBY[7:0] bits of the OSC0CTRL1 register are FFH (OSC0 is on standby), the OSC0\_STANDBY[7:0] bits are automatically set to 00H.

- (1) If the setting of bits 3 to 0 (MODE\_SEL) of the CLK\_MODE\_SEL register is changed to switch from a mode other than normal A, B, C, and D to normal A, B, C, or D while bits 3 to 0 of the CKMODE\_PLLSEL register are 0H and bits 29 and 28 (OSC\_SEL) of the PLL1CTRL0 register are 0H
- (2) If the setting of bits 3 to 0 (MODE\_SEL) of the CLK\_MODE\_SEL register is changed to select the economy mode while bits 31 to 28 of the CKMODE\_PLLSEL register are DH
- (3) If the setting of bits 3 to 0 (MODE\_SEL) of the CLK\_MODE\_SEL register is changed to select the sleep mode while bits 31 to 28 of the CKMODE\_PLLSEL register are DH
- (4) If an interrupt to the CPU (IRQ or FIQ) occurs while the deep sleep mode is specified for bits 11 to 8 (MODE\_STATUS) of the CLK\_MODE\_SEL register while bits 31 to 28 of the CKMODE\_PLLSEL register are DH

OSC1: If one of the four following conditions is met while the OSC1\_STANDBY[7:0] bits of the OSC1CTRL1 register are FFH (OSC1 is on standby), the OSC1\_STANDBY[7:0] bits are automatically set to 00H.

- (1) If the setting of bits 3 to 0 (MODE\_SEL) of the CLK\_MODE\_SEL register is changed to switch from a mode other than normal A, B, C, and D to normal A, B, C, or D while bits 3 to 0 of the CKMODE\_PLLSEL register are 0H and bits 29 and 28 (OSC\_SEL) of the PLL1CTRL0 register are 1H
- (2) If the setting of bits 3 to 0 (MODE\_SEL) of the CLK\_MODE\_SEL register is changed to select the economy mode while bits 31 to 28 of the CKMODE\_PLLSEL register are EH
- (3) If the setting of bits 3 to 0 (MODE\_SEL) of the CLK\_MODE\_SEL register is changed to select the sleep mode while bits 31 to 28 of the CKMODE\_PLLSEL register are EH
- (4) If an interrupt to the CPU (IRQ or FIQ) occurs while the deep sleep mode is specified for bits 11 to 8 (MODE\_STATUS) of the CLK\_MODE\_SEL register while bits 31 to 28 of the CKMODE\_PLLSEL register are EH

#### ○ Automatic standby mode

PLL1: If bits 11 to 8 (MODE\_STATUS) of the CLK\_MODE\_SEL register show that the mode has changed from normal A, B, C, or D to a mode other than normal A, B, C, and D while the PLL1\_STANDBY[7:0] bits of the PLL1CTRL1 register are 00H (PLL1 is no longer on standby), the PLL1\_STANDBY[7:0] bits are automatically set to FFH.

PLL2: If bits 11 to 8 (MODE\_STATUS) of the CLK\_MODE\_SEL register show that the mode has changed from normal A, B, C, or D to a mode other than normal A, B, C, and D while the PLL2\_STANDBY[7:0] bits of the PLL2CTRL1 register are 00H (PLL2 is no longer on standby), the PLL2\_STANDBY[7:0] bits are automatically set to FFH.

PLL3: If the mode changes under either of the two following conditions while the PLL3\_STANDBY[7:0] bits of the PLL3CTRL1 register are 00H (PLL3 is no longer on standby), the PLL3\_STANDBY[7:0] bits are automatically set to FFH.

- (1) If bits 11 to 8 (MODE\_STATUS) of the CLK\_MODE\_SEL register show that the mode has changed to

sleep mode

- (2) If bits 11 to 8 (MODE\_STATUS) of the CLK\_MODE\_SEL register show that the mode has changed to deep sleep mode

OSC0: If the mode changes under either of the two following conditions while the OSC0\_STANDBY[7:0] bits of the OSC0CTRL1 are 00H (OSC0 is no longer on standby) and bits 31 to 28 of the CKMODE\_PLLSEL register are DH, the OSC0\_STANDBY[7:0] bits are automatically set to FFH.

- (1) If bits 11 to 8 (MODE\_STATUS) of the CLK\_MODE\_SEL register show that the mode has changed to power-on mode
- (2) If bits 11 to 8 (MODE\_STATUS) of the CLK\_MODE\_SEL register show that the mode has changed to deep sleep mode

OSC1: If the mode changes under either of the two following conditions while the OSC1\_STANDBY[7:0] bits of the OSC1CTRL1 are 00H (OSC1 is no longer on standby) and bits 31 to 28 of the CKMODE\_PLLSEL register are EH, the OSC1\_STANDBY[7:0] bits are automatically set to FFH.

- (1) If bits 11 to 8 (MODE\_STATUS) of the CLK\_MODE\_SEL register show that the mode has changed to power-on mode
- (2) If bits 11 to 8 (MODE\_STATUS) of the CLK\_MODE\_SEL register show that the mode has changed to deep sleep mode

The AUTO\_STANDBY\_CLR and AUTO\_STANDBY bits can be set to 0 or 1 simultaneously.

### 3.2.116 Automatic mode transition enable register

This register (AUTO\_MODE\_EN: E011\_02F4H) controls automatic mode transition between Low Power modes.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								
7	6	5	4	3	2	1	0	
Reserved	POWERDOWN_INT_MASK_EN	POWERDOWN_INT_MASK_EN		Reserved		AUTO_DSL2ECN_EN		

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:6	–	Reserved. If these bits are read, 0 is returned for each bit.
POWERDOWN_INT_MASK_EN	R/W	5	0	Specify whether to enable setting bit 4 (POWERDOWN_INT_MASK) to 1 when an interrupt to the CPU (IRQ or FIQ) occurs in deep sleep mode. 0: Disable 1: Enable
POWERDOWN_INT_MASK	R/W	4	0	When this bit is set to 1, write accesses to registers CLK_MODE_SEL, PLL1CTRL1, PLL2CTRL1, PLL3CTRL1 and LOWPWR via APB are ignored (APB write is unavailable). This bit is automatically set to 1 when bit 5 (POWERDOWN_INT_MASK_EN) is set to 1 (enable) and when an interrupt to the CPU (IRQ or FIQ) occurs in deep sleep mode. 0: Enables write access via APB. 1: Masks write access via APB.
Reserved	R	3:1	–	Reserved. If these bits are read, 0 is returned for each bit.
AUTO_DSL2ECN_EN	R/W	0	0	Specify whether to enable automatic mode transition from deep sleep to economy, which is triggered by an interrupt to the CPU. 0: Disable 1: Enable

### 3.2.117 Clock mode select register

This register (CLK\_MODE\_SEL: E011\_0300H) selects the clock mode of the PLL frequency.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved				MODE_STATUS			
7	6	5	4	3	2	1	0
Reserved				MODE_SEL			

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:17	–	Reserved. If these bits are read, 0 is returned for each bit.
AUTO_FRQ_CHANGE_BUSY	R	16	0	Indicates the status of the automatic PLL frequency switch function. 0: Normal (operating at default frequency) 1: Busy (operating at low frequency)
Reserved	R	15:12	–	Reserved. If these bits are read, 0 is returned for each bit.
MODE_STATUS	R	11:8	FH	Indicates the status of the clock mode of the PLL frequency. 0H: Power-on 1H: Normal A 2H: Normal B 3H: Normal C 4H: Normal D 5H: Economy 7H: Sleep 8H: Deep sleep FH: Unknown
Reserved	R	7:4	–	Reserved. If these bits are read, 0 is returned for each bit.

(2/2)

Name	R/W	Bit No.	After Reset	Description
MODE_SEL	R/W	3:0	0H	<p>Specify the initial mode after boot.</p> <p>0H: Power-on (default)  1H: Normal A  2H: Normal B  3H: Normal C  4H: Normal D  5H: Economy  6H: Setting prohibited  7H: Sleep  8H: Deep sleep  9H to FH: Setting prohibited</p>

After a reset ends, the application block is automatically booted in power-on mode.

Before selecting normal A, B, C, or D by using the MODE\_SEL bit, enable the PLL to use in the selected mode.

If an interrupt to the CPU (IRQ or FIQ) occurs in deep sleep mode, economy mode is automatically entered after the time specified for the PLL3\_LOCKTIME bit has elapsed (when AUTO\_DSL2ECN\_EN is enabled).

Disable the automatic frequency switching before changing the MODE\_SEL setting.

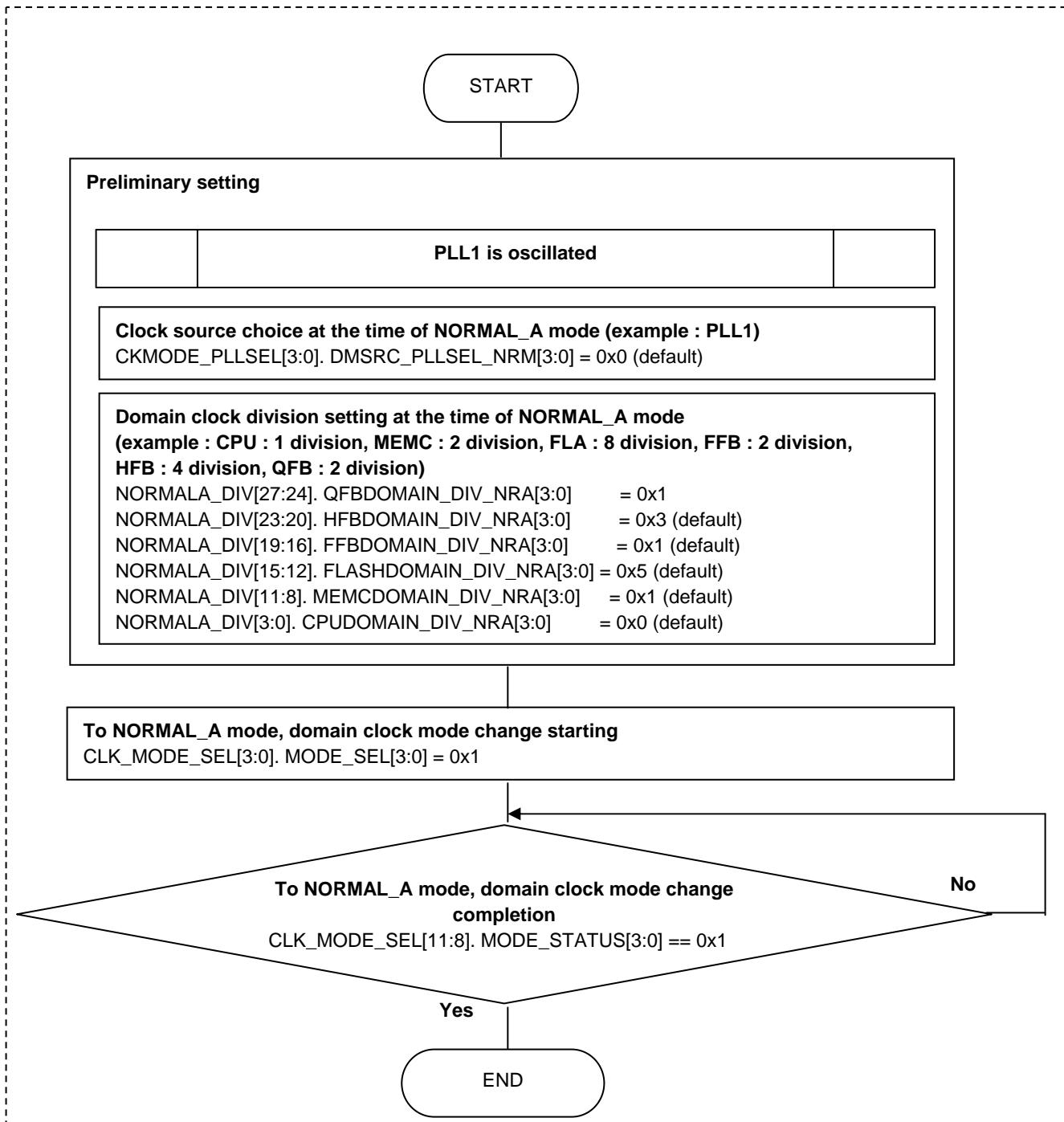
SMU\_CONTROL[4] is set as each clock mode by division setting of that case's MEMC domain clock.

Refer to a table of a division setting register of each clock mode for the set value of SMU\_CONTROL[4].

Refer to following flow chart for a setting method of SMU\_CONTROL[4].

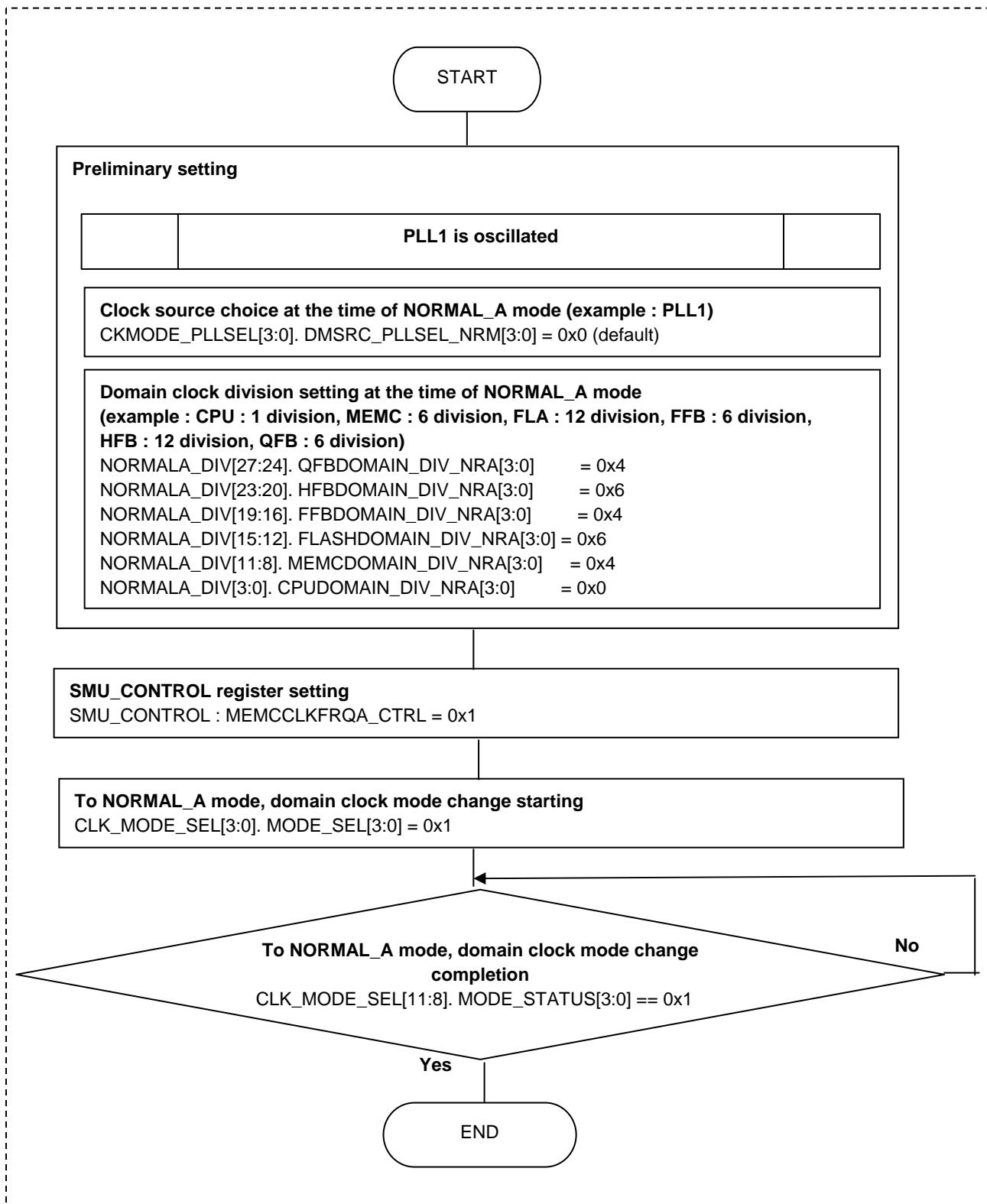
**Figure 3-9. Domain clock mode not change (SMU\_CONTROL[4] = 0 -> 0)**

(to NORMAL\_A (clock source : PLL1))



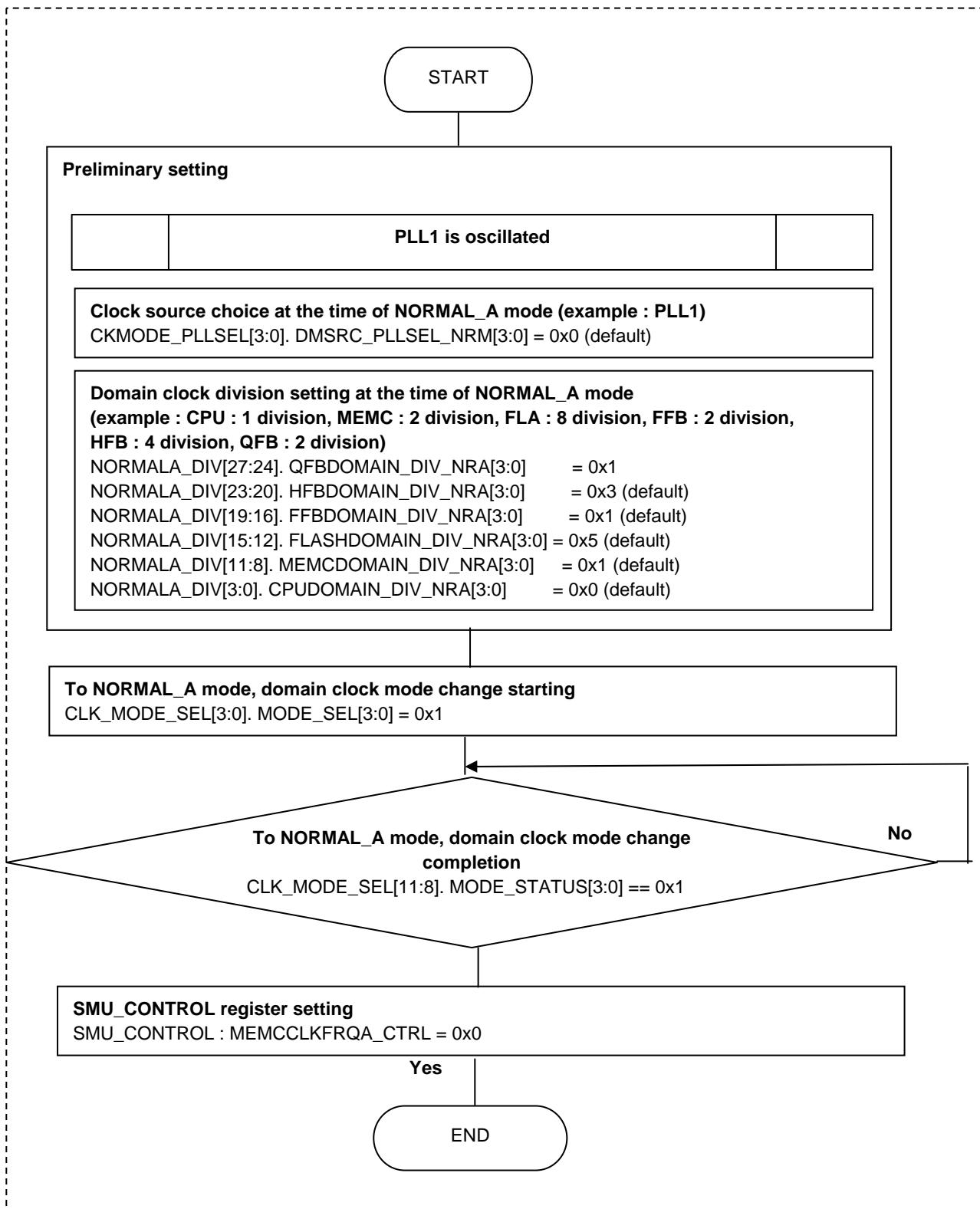
**Figure 3-10.** Domain clock mode change (SMU\_CONTROL[4] = 0 -> 1)

(to NORMAL\_A (clock source : PLL1))



**Figure 3-11. Domain clock mode change (SMU\_CONTROL[4] = 1 -> 0)**

(to NORMAL\_A (clock source : PLL1))



### 3.2.118 SMU-MEMC handshake function switch register

This register (MEMC\_HAND\_SHAKE\_FAKE: E011\_0304H) is used to fake the handshake between the SMU and MEMC when the clock mode is switched. If fake handshaking is enabled, the clock mode is switched even if ACK is not returned from the MEMC.

Handshaking is not possible when the P1 power is off or when the reset signal for the MEMC is active. In this case, set the SMU\_MEMC\_HS\_FAKE bit to 1.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							SMU_MEMC_HS_FAKE
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
SMU_MEMC_HS_FAKE	R/W	0	0	Specify whether to fake the handshake between the SMU and MEMC when the clock mode is switched. 0: Disable faking. 1: Enable faking.			

### 3.2.119 PLL select register

This register (CKMODE\_PLLSEL: E011\_031CH) selects the PLL and OSC in each mode.

31	30	29	28	27	26	25	24
DMSRC_PLLSEL_SLP					Reserved		
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				DMSRC_PLLSEL_NRM			
Name	R/W	Bit No.	After Reset	Description			
DMSRC_PLLSEL_SLP	R/W	31:28	DH	Specify the oscillator used in sleep mode. DH: OSC0 EH: OSC1 Other: Setting prohibited			
Reserved	R	27:20	–	Reserved. If these bits are read, 0 is returned for each bit.			
Reserved	R/W	19:16	CH	Reserved. 0xC is written in certainly.			
Reserved	R	15:4	–	Reserved. If these bits are read, 0 is returned for each bit.			
DMSRC_PLLSEL_NRM	R/W	3:0	0H	Specify the PLL used in NORMAL_A, NORMAL_B, NORMAL_C, and NORMAL_D modes. 0H: PLL1 4H: PLL2 Other: Setting prohibited			

The source of the domain clock in the Normal mode, sleep mode, and power-on mode can be selected.

### 3.2.120 Normal mode A clock frequency division setting register

This register (NORMALA\_DIV: E011\_0320H) specifies the division factor for the clocks in normal mode A.

31	30	29	28	27	26	25	24
Reserved				QFB_DOMAIN_DIV_NRA			
23	22	21	20	19	18	17	16
HFBDOMAIN_DIV_NRA				FFBDOMAIN_DIV_NRA			
15	14	13	12	11	10	9	8
FLASHDOMAIN_DIV_NRA				MEMCDOMAIN_DIV_NRA			
7	6	5	4	3	2	1	0
Reserved				CPUDOMAIN_DIV_NRA			

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:28	–	Reserved. If these bits are read, 0 is returned for each bit.
QFBDOMAIN_DIV_NRA	R/W	27:24	5H	Specify the division factor for the QFB domain clock.
HFBDOMAIN_DIV_NRA	R/W	23:20	3H	Specify the division factor for the HFB domain clock.
FFBDOMAIN_DIV_NRA	R/W	19:16	1H	Specify the division factor for the FFB domain clock.
FLASHDOMAIN_DIV_NRA	R/W	15:12	5H	Specify the division factor for the FLASH domain clock.
MEMCDOMAIN_DIV_NRA	R/W	11:8	1H	Specify the division factor for the MEMC domain clock.
Reserved	R/W	7:4	0H	Reserved. The recommendation set value is 0H.
CPUDOMAIN_DIV_NRA	R/W	3:0	0H	Specify the division factor for the CPU domain clock.

- Remark**
- xxxxDOMAIN\_DIV\_NRA = 0H: Undivided
  - xxxxDOMAIN\_DIV\_NRA = 1H: Divided by 2
  - xxxxDOMAIN\_DIV\_NRA = 2H: Divided by 3
  - xxxxDOMAIN\_DIV\_NRA = 3H: Divided by 4
  - xxxxDOMAIN\_DIV\_NRA = 4H: Divided by 6
  - xxxxDOMAIN\_DIV\_NRA = 5H: Divided by 8
  - xxxxDOMAIN\_DIV\_NRA = 6H: Divided by 12
  - xxxxDOMAIN\_DIV\_NRA = 7H: Divided by 16
  - xxxxDOMAIN\_DIV\_NRA = 8H: Divided by 1.5
  - xxxxDOMAIN\_DIV\_NRA = 9H: Divided by 2.5
  - xxxxDOMAIN\_DIV\_NRA = AH: Divided by 5
  - xxxxDOMAIN\_DIV\_NRA = BH: Divided by 10
  - xxxxDOMAIN\_DIV\_NRA = CH to FH: Setting prohibited

It's established so that a frequency of a divided domain clock may meet the following condition.

CPU  $\geq$  MEMC  $\geq$  FFB,QFB  $\geq$  HFB,FLA

It's established as each item domain clock frequency will be a integral multiple.

When changing a clock mode by division setting of a MEMC domain clock, it's necessary to set SMU\_CONTROL [4]. (The following table referring)

The upper limit value of each domain clock is as follows.

533MHz  $\geq$  CPU

266MHz  $\geq$  MEMC, FFB, QFB

133MHz  $\geq$  HFB, FLA

**Table 3-1 NORMAL DIV**

<b>Clock Mode</b>	<b>MEMC domain clock</b>			<b>DDR access</b>	<b>SMU_CONTROL[4]</b>	<b>Note</b>
	<b>Division setting</b>	<b>Division value</b>	<b>Frequency (MHz)</b>			
NORMAL A/B/C/D	0x0	1	533.00	Disable	0	The access to a DDR is impossible because generation of DQS is impossible.
	0x1	2	266.50	Enable	0	High speed access to a DDR.
	0x2	3	177.67	Enable	0	
	0x3	4	133.25	Enable	0	
	0x4	6	88.83	Enable	1	
	0x5	8	66.63	Enable	0	
	0x6	12	44.42	Enable	0	
	0x7	16	33.31	Enable	0	
	0x8	1.5	355.33	Disable	0	The access to a DDR is impossible because generation of DQS is impossible.
	0x9	2.5	213.20	Enable	0	
	0xA	5	106.60	Enable	0	
	0xB	10	53.30	Enable	0	

### 3.2.121 Normal mode B clock frequency division setting register

This register (NORMALB\_DIV: E011\_0324H) specifies the division factor for the clocks in normal mode B.

31	30	29	28	27	26	25	24
Reserved				QFBDOMAIN_DIV_NRB			
23	22	21	20	19	18	17	16
HFBDOMAIN_DIV_NRB				FFBDOMAIN_DIV_NRB			
15	14	13	12	11	10	9	8
FLASHDOMAIN_DIV_NRB				MEMCDOMAIN_DIV_NRB			
7	6	5	4	3	2	1	0
Reserved				CPUDOMAIN_DIV_NRB			

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:28	–	Reserved. If these bits are read, 0 is returned for each bit.
QFBDOMAIN_DIV_NRB	R/W	27:24	5H	Specify the division factor for the QFB domain clock.
HFBDOMAIN_DIV_NRB	R/W	23:20	3H	Specify the division factor for the HFB domain clock.
FFBDOMAIN_DIV_NRB	R/W	19:16	1H	Specify the division factor for the FFB domain clock.
FLASHDOMAIN_DIV_NRB	R/W	15:12	5H	Specify the division factor for the FLASH domain clock.
MEMCDOMAIN_DIV_NRB	R/W	11:8	1H	Specify the division factor for the MEMC domain clock.
Reserved	R/W	7:4	0H	Reserved. The recommendation set value is 0H.
CPUDOMAIN_DIV_NRB	R/W	3:0	0H	Specify the division factor for the CPU domain clock.

- Remark**
- xxxxDOMAIN\_DIV\_NRB = 0H: Undivided
  - xxxxDOMAIN\_DIV\_NRB = 1H: Divided by 2
  - xxxxDOMAIN\_DIV\_NRB = 2H: Divided by 3
  - xxxxDOMAIN\_DIV\_NRB = 3H: Divided by 4
  - xxxxDOMAIN\_DIV\_NRB = 4H: Divided by 6
  - xxxxDOMAIN\_DIV\_NRB = 5H: Divided by 8
  - xxxxDOMAIN\_DIV\_NRB = 6H: Divided by 12
  - xxxxDOMAIN\_DIV\_NRB = 7H: Divided by 16
  - xxxxDOMAIN\_DIV\_NRB = 8H: Divided by 1.5
  - xxxxDOMAIN\_DIV\_NRB = 9H: Divided by 2.5
  - xxxxDOMAIN\_DIV\_NRB = AH: Divided by 5
  - xxxxDOMAIN\_DIV\_NRB = BH: Divided by 10
  - xxxxDOMAIN\_DIV\_NRB = CH to FH: Setting prohibited

It's established so that a frequency of a divided domain clock may meet the following condition.

CPU  $\geq$  MEMC  $\geq$  FFB,QFB  $\geq$  HFB,FLA

It's established as each item domain clock frequency will be a integral multiple.

When changing a clock mode by division setting of a MEMC domain clock, it's necessary to set SMU\_CONTROL [4]. (See Table 3-1)

The upper limit value of each domain clock is as follows.

533MHz  $\geq$  CPU

266MHz  $\geq$  MEMC, FFB, QFB

133MHz  $\geq$  HFB, FLA

### 3.2.122 Normal mode C clock frequency division setting register

This register (NORMALC\_DIV: E011\_0328H) specifies the division factor for the clocks in normal mode C.

31	30	29	28	27	26	25	24
Reserved				QFBDOMAIN_DIV_NRC			
23	22	21	20	19	18	17	16
HFBDOMAIN_DIV_NRC				FFBDOMAIN_DIV_NRC			
15	14	13	12	11	10	9	8
FLASHDOMAIN_DIV_NRC				MEMCDOMAIN_DIV_NRC			
7	6	5	4	3	2	1	0
Reserved				CPUDOMAIN_DIV_NRC			

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:28	–	Reserved. If these bits are read, 0 is returned for each bit.
QFBDOMAIN_DIV_NRC	R/W	27:24	5H	Specify the division factor for the QFB domain clock.
HFBDOMAIN_DIV_NRC	R/W	23:20	3H	Specify the division factor for the HFB domain clock.
FFBDOMAIN_DIV_NRC	R/W	19:16	1H	Specify the division factor for the FFB domain clock.
FLASHDOMAIN_DIV_NRC	R/W	15:12	5H	Specify the division factor for the FLASH domain clock.
MEMCDOMAIN_DIV_NRC	R/W	11:8	1H	Specify the division factor for the MEMC domain clock.
Reserved	R/W	7:4	0H	Reserved. The recommendation set value is 0H.
CPUDOMAIN_DIV_NRC	R/W	3:0	0H	Specify the division factor for the CPU domain clock.

**Remark**    xxxxDOMAIN\_DIV\_NRC = 0H: Undivided  
 xxxxDOMAIN\_DIV\_NRC = 1H: Divided by 2  
 xxxxDOMAIN\_DIV\_NRC = 2H: Divided by 3  
 xxxxDOMAIN\_DIV\_NRC = 3H: Divided by 4  
 xxxxDOMAIN\_DIV\_NRC = 4H: Divided by 6  
 xxxxDOMAIN\_DIV\_NRC = 5H: Divided by 8  
 xxxxDOMAIN\_DIV\_NRC = 6H: Divided by 12  
 xxxxDOMAIN\_DIV\_NRC = 7H: Divided by 16  
 xxxxDOMAIN\_DIV\_NRC = 8H: Divided by 1.5  
 xxxxDOMAIN\_DIV\_NRC = 9H: Divided by 2.5  
 xxxxDOMAIN\_DIV\_NRC = AH: Divided by 5  
 xxxxDOMAIN\_DIV\_NRC = BH: Divided by 10  
 xxxxDOMAIN\_DIV\_NRC = CH to FH: Setting prohibited

It's established so that a frequency of a divided domain clock may meet the following condition.

CPU  $\geq$  MEMC  $\geq$  FFB, QFB  $\geq$  HFB, FLA

It's established as each item domain clock frequency will be a integral multiple.

When changing a clock mode by division setting of a MEMC domain clock, it's necessary to set SMU\_CONTROL [4]. (See Table 3-1)

The upper limit value of each domain clock is as follows.

533MHz  $\geq$  CPU

266MHz  $\geq$  MEMC, FFB, QFB

133MHz  $\geq$  HFB, FLA

### 3.2.123 Normal mode D clock frequency division setting register

This register (NORMALD\_DIV: E011\_032CH) specifies the division factor for the clocks in normal mode D.

31	30	29	28	27	26	25	24
Reserved				QFBDOMAIN_DIV_NRD			
23	22	21	20	19	18	17	16
HFBDOMAIN_DIV_NRD				FFBDOMAIN_DIV_NRD			
15	14	13	12	11	10	9	8
FLASHDOMAIN_DIV_NRD				MEMCDOMAIN_DIV_NRD			
7	6	5	4	3	2	1	0
Reserved				CPUDOMAIN_DIV_NRD			

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:28	–	Reserved. If these bits are read, 0 is returned for each bit.
QFBDOMAIN_DIV_NRD	R/W	27:24	5H	Specify the division factor for the QFB domain clock.
HFBDOMAIN_DIV_NRD	R/W	23:20	3H	Specify the division factor for the HFB domain clock.
FFBDOMAIN_DIV_NRD	R/W	19:16	1H	Specify the division factor for the FFB domain clock.
FLASHDOMAIN_DIV_NRD	R/W	15:12	5H	Specify the division factor for the FLASH domain clock.
MEMCDOMAIN_DIV_NRD	R/W	11:8	1H	Specify the division factor for the MEMC domain clock.
Reserved	R/W	7:4	0H	Reserved. The recommendation set value is 0H.
CPUDOMAIN_DIV_NRD	R/W	3:0	0H	Specify the division factor for the CPU domain clock.

**Remark** xxxxDOMAIN\_DIV\_NRD = 0H: Undivided  
 xxxxDOMAIN\_DIV\_NRD = 1H: Divided by 2  
 xxxxDOMAIN\_DIV\_NRD = 2H: Divided by 3  
 xxxxDOMAIN\_DIV\_NRD = 3H: Divided by 4  
 xxxxDOMAIN\_DIV\_NRD = 4H: Divided by 6  
 xxxxDOMAIN\_DIV\_NRD = 5H: Divided by 8  
 xxxxDOMAIN\_DIV\_NRD = 6H: Divided by 12  
 xxxxDOMAIN\_DIV\_NRD = 7H: Divided by 16  
 xxxxDOMAIN\_DIV\_NRD = 8H: Divided by 1.5  
 xxxxDOMAIN\_DIV\_NRD = 9H: Divided by 2.5  
 xxxxDOMAIN\_DIV\_NRD = AH: Divided by 5  
 xxxxDOMAIN\_DIV\_NRD = BH: Divided by 10  
 xxxxDOMAIN\_DIV\_NRD = CH to FH: Setting prohibited

It's established so that a frequency of a divided domain clock may meet the following condition.

CPU  $\geq$  MEMC  $\geq$  FFB,QFB  $\geq$  HFB,FLA

It's established as each item domain clock frequency will be a integral multiple.

When changing a clock mode by division setting of a MEMC domain clock, it's necessary to set

SMU\_CONTROL [4]. (See Table 3-1)

The upper limit value of each domain clock is as follows.

533MHz  $\geq$  CPU

266MHz  $\geq$  MEMC, FFB, QFB

133MHz  $\geq$  HFB, FLA

### 3.2.124 Power-on mode clock frequency division setting register

This register (POWERON\_DIV: E011\_0330H) specifies the division factor for the clocks in power-on mode.

31	30	29	28	27	26	25	24
Reserved				QFBDOMAIN_DIV_PON			
23	22	21	20	19	18	17	16
HFBDOMAIN_DIV_PON				FFBDOMAIN_DIV_PON			
15	14	13	12	11	10	9	8
FLASHDOMAIN_DIV_PON				MEMCDOMAIN_DIV_PON			
7	6	5	4	3	2	1	0
Reserved				CPUDOMAIN_DIV_PON			

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:28	–	Reserved. If these bits are read, 0 is returned for each bit.
QFBDOMAIN_DIV_PON	R/W	27:24	7H	Specify the division factor for the QFB domain clock.
HFBDOMAIN_DIV_PON	R/W	23:20	7H	Specify the division factor for the HFB domain clock.
FFBDOMAIN_DIV_PON	R/W	19:16	7H	Specify the division factor for the FFB domain clock.
FLASHDOMAIN_DIV_PON	R/W	15:12	7H	Specify the division factor for the FLASH domain clock.
MEMCDOMAIN_DIV_PON	R/W	11:8	7H	Specify the division factor for the MEMC domain clock.
Reserved	R/W	7:4	0H	Reserved. The recommendation set value is 7H.
CPUDOMAIN_DIV_PON	R/W	3:0	7H	Specify the division factor for the CPU domain clock.

**Remark**    xxxxDOMAIN\_DIV\_PON = 0H: Undivided  
                   xxxxDOMAIN\_DIV\_PON = 1H: Divided by 2  
                   xxxxDOMAIN\_DIV\_PON = 2H: Divided by 3  
                   xxxxDOMAIN\_DIV\_PON = 3H: Divided by 4  
                   xxxxDOMAIN\_DIV\_PON = 4H: Divided by 6  
                   xxxxDOMAIN\_DIV\_PON = 5H: Divided by 8  
                   xxxxDOMAIN\_DIV\_PON = 6H: Divided by 12  
                   xxxxDOMAIN\_DIV\_PON = 7H: Divided by 16  
                   xxxxDOMAIN\_DIV\_PON = 8H: Divided by 1.5  
                   xxxxDOMAIN\_DIV\_PON = 9H: Divided by 2.5  
                   xxxxDOMAIN\_DIV\_PON = AH: Divided by 5  
                   xxxxDOMAIN\_DIV\_PON = BH: Divided by 10  
                   xxxxDOMAIN\_DIV\_PON = CH to FH: Setting prohibited

It's established so that a frequency of a divided domain clock may meet the following condition.

CPU  $\geq$  MEMC  $\geq$  FFB, QFB  $\geq$  HFB, FLA

It's established as each item domain clock frequency will be a integral multiple.

When changing a clock mode by division setting of a MEMC domain clock, it's necessary to set SMU\_CONTROL [4]. (The following table referring)

**Table 3-2 POWER ON DIV**

Clock Mode	MEMC domain clock			DDR access	SMU_CONT ROL[4]	Note
	Division setting	Division value	Frequency (MHz)			
POWERON	0x0	1	230.00	Disable	0	The access to a DDR is impossible because generation of DQS is impossible.
	0x1	2	115.00	Enable	0	
	0x2	3	76.67	Enable	1	
	0x3	4	57.50	Enable	0	
	0x4	6	38.33	Enable	0	
	0x5	8	28.75	Enable	0	
	0x6	12	19.17	Enable	0	
	0x7	16	14.38	Enable	0	Default setting after power on.
	0x8	1.5	153.33	Disable	0	The access to a DDR is impossible because generation of DQS is impossible.
	0x9	2.5	92.00	Enable	1	
	0xA	5	46.00	Enable	0	
	0xB	10	23.00	Enable	0	

### 3.2.125 Economy mode clock frequency division setting register

This register (ECONOMY\_DIV: E011\_0334H) specifies the division factor for the clocks in economy mode.

31	30	29	28	27	26	25	24
Reserved				QFBDOMAIN_DIV_ECN			
23	22	21	20	19	18	17	16
HFBDOMAIN_DIV_ECN				FFBDOMAIN_DIV_ECN			
15	14	13	12	11	10	9	8
FLASHDOMAIN_DIV_ECN				MEMCDOMAIN_DIV_ECN			
7	6	5	4	3	2	1	0
Reserved				CPUDOMAIN_DIV_ECN			

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:28	–	Reserved. If these bits are read, 0 is returned for each bit.
QFBDOMAIN_DIV_ECN	R/W	27:24	5H	Specify the division factor for the QFB domain clock.
HFBDOMAIN_DIV_ECN	R/W	23:20	3H	Specify the division factor for the HFB domain clock.
FFBDOMAIN_DIV_ECN	R/W	19:16	1H	Specify the division factor for the FFB domain clock.
FLASHDOMAIN_DIV_ECN	R/W	15:12	5H	Specify the division factor for the FLASH domain clock.
MEMCDOMAIN_DIV_ECN	R/W	11:8	1H	Specify the division factor for the MEMC domain clock.
Reserved	R/W	7:4	0H	Reserved. The recommendation set value is 0H.
CPUDOMAIN_DIV_ECN	R/W	3:0	0H	Specify the division factor for the CPU domain clock.

**Remark**    xxxxDOMAIN\_DIV\_ECN = 0H: Undivided  
                   xxxxDOMAIN\_DIV\_ECN = 1H: Divided by 2  
                   xxxxDOMAIN\_DIV\_ECN = 2H: Divided by 3  
                   xxxxDOMAIN\_DIV\_ECN = 3H: Divided by 4  
                   xxxxDOMAIN\_DIV\_ECN = 4H: Divided by 6  
                   xxxxDOMAIN\_DIV\_ECN = 5H: Divided by 8  
                   xxxxDOMAIN\_DIV\_ECN = 6H: Divided by 12  
                   xxxxDOMAIN\_DIV\_ECN = 7H: Divided by 16  
                   xxxxDOMAIN\_DIV\_ECN = 8H: Divided by 1.5  
                   xxxxDOMAIN\_DIV\_ECN = 9H: Divided by 2.5  
                   xxxxDOMAIN\_DIV\_ECN = AH: Divided by 5  
                   xxxxDOMAIN\_DIV\_ECN = BH: Divided by 10  
                   xxxxDOMAIN\_DIV\_ECN = CH to FH: Setting prohibited

It's established so that a frequency of a divided domain clock may meet the following condition.

CPU  $\geq$  MEMC  $\geq$  FFB,QFB  $\geq$  HFB,FLA

It's established as each item domain clock frequency will be a integral multiple.

When changing a clock mode by division setting of a MEMC domain clock, it's necessary to set SMU\_CONTROL [4]. (The following table referring)

**Table 3-3 ECONOMY DIV**

Clock Mode	MEMC domain clock			DDR access	SMU_CONT ROL[4]	Note
	Division setting	Division value	Frequency (MHz)			
ECONOMY	0x0	1	230.00	Disable	0	The access to a DDR is impossible because generation of DQS is impossible.
	0x1	2	115.00	Enable	0	High speed access to a DDR.
	0x2	3	76.67	Enable	1	
	0x3	4	57.50	Enable	0	
	0x4	6	38.33	Enable	0	
	0x5	8	28.75	Enable	0	
	0x6	12	19.17	Enable	0	
	0x7	16	14.38	Enable	0	
	0x8	1.5	153.33	Disable	0	The access to a DDR is impossible because generation of DQS is impossible.
	0x9	2.5	92.00	Enable	1	
	0xA	5	46.00	Enable	0	
	0xB	10	23.00	Enable	0	

### 3.2.126 Sleep mode clock frequency division setting register

This register (SLEEP\_DIV: E011\_0338H) specifies the division factor for the clocks in sleep mode.

31	30	29	28	27	26	25	24
Reserved				QFBDOMAIN_DIV_SLP			
23	22	21	20	19	18	17	16
HFBDOMAIN_DIV_SLP				FFBDOMAIN_DIV_SLP			
15	14	13	12	11	10	9	8
FLASHDOMAIN_DIV_SLP				MEMCDOMAIN_DIV_SLP			
7	6	5	4	3	2	1	0
Reserved				CPUDOMAIN_DIV_SLP			

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:28	–	Reserved. If these bits are read, 0 is returned for each bit.
QFBDOMAIN_DIV_SLP	R/W	27:24	5H	Specify the division factor for the QFB domain clock.
HFBDOMAIN_DIV_SLP	R/W	23:20	5H	Specify the division factor for the HFB domain clock.
FFBDOMAIN_DIV_SLP	R/W	19:16	5H	Specify the division factor for the FFB domain clock.
FLASHDOMAIN_DIV_SLP	R/W	15:12	5H	Specify the division factor for the FLASH domain clock.
MEMCDOMAIN_DIV_SLP	R/W	11:8	5H	Specify the division factor for the MEMC domain clock.
Reserved	R/W	7:4	0H	Reserved. The recommendation set value is 7H.
CPUDOMAIN_DIV_SLP	R/W	3:0	0H	Specify the division factor for the CPU domain clock.

**Remark** xxxxDOMAIN\_DIV\_SLP = 0H: Divided by 1  
 xxxxDOMAIN\_DIV\_SLP = 1H: Divided by 2  
 xxxxDOMAIN\_DIV\_SLP = 2H: Divided by 3  
 xxxxDOMAIN\_DIV\_SLP = 3H: Divided by 4  
 xxxxDOMAIN\_DIV\_SLP = 4H: Divided by 6  
 xxxxDOMAIN\_DIV\_SLP = 5H: Divided by 8  
 xxxxDOMAIN\_DIV\_SLP = 6H: Divided by 12  
 xxxxDOMAIN\_DIV\_SLP = 7H: Divided by 16  
 xxxxDOMAIN\_DIV\_SLP = 8H: Divided by 1.5  
 xxxxDOMAIN\_DIV\_SLP = 9H: Divided by 2.5  
 xxxxDOMAIN\_DIV\_SLP = AH: Divided by 5  
 xxxxDOMAIN\_DIV\_SLP = BH: Divided by 10  
 xxxxDOMAIN\_DIV\_SLP = CH to FH: Setting prohibited

It's established so that a frequency of a divided domain clock may meet the following condition.

CPU  $\geq$  MEMC  $\geq$  FFB, QFB  $\geq$  HFB, FLA

It's established as each item domain clock frequency will be a integral multiple.

When changing a clock mode by division setting of a MEMC domain clock, it's necessary to set SMU\_CONTROL [4]. (The following table referring)

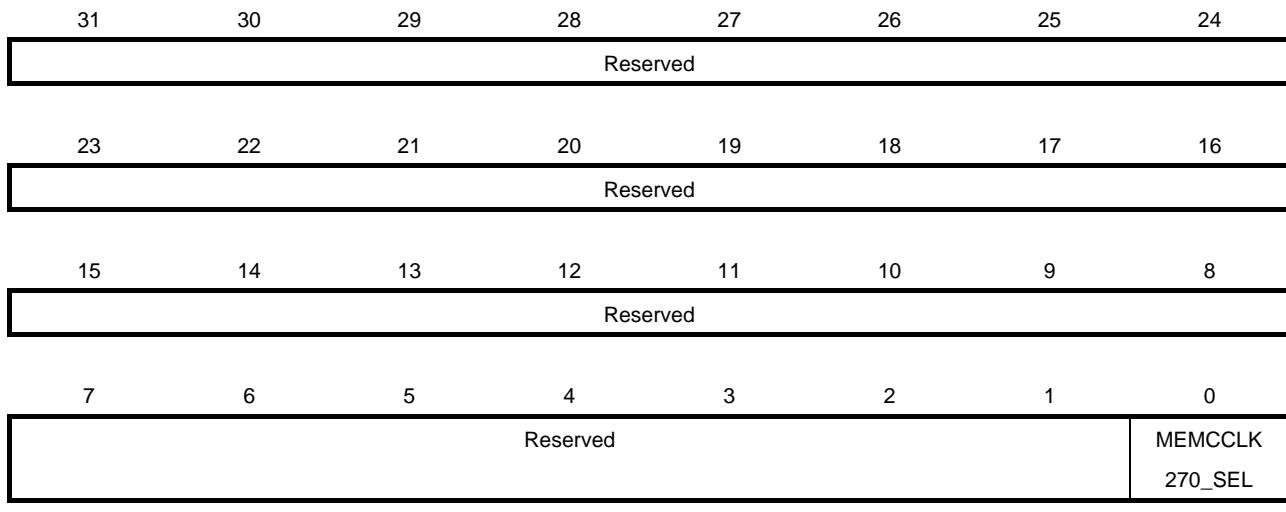
**Table 3-4 SLEEP DIV**

Clock Mode	MEMC domain clock			DDR access	SMU_CONT ROL[4]	Note
	Division setting	Division value	Frequency (MHz)			
SLEEP	0x0	1	30.00	Disable	0	Access prohibited to a DDR for the specification by which PM power supply territory off.
	0x1	2	15.00	Disable	0	
	0x2	3	10.00	Disable	0	
	0x3	4	7.50	Disable	0	
	0x4	6	5.00	Disable	0	
	0x5 <sup>Note</sup>	8	3.75	Disable	0	
	0x6	12	2.50	Disable	0	
	0x7	16	1.88	Disable	0	
	0x8	1.5	20.00	Disable	0	
	0x9	2.5	12.00	Disable	0	
	0xA	5	6.00	Disable	0	
	0xB	10	3.00	Disable	0	

Note : Default

### 3.2.127 MEMC\_CLK270 switch register

This register (MEMCCLK270\_SEL: E011\_0350H) selects an MEMC\_CLK delay amount.



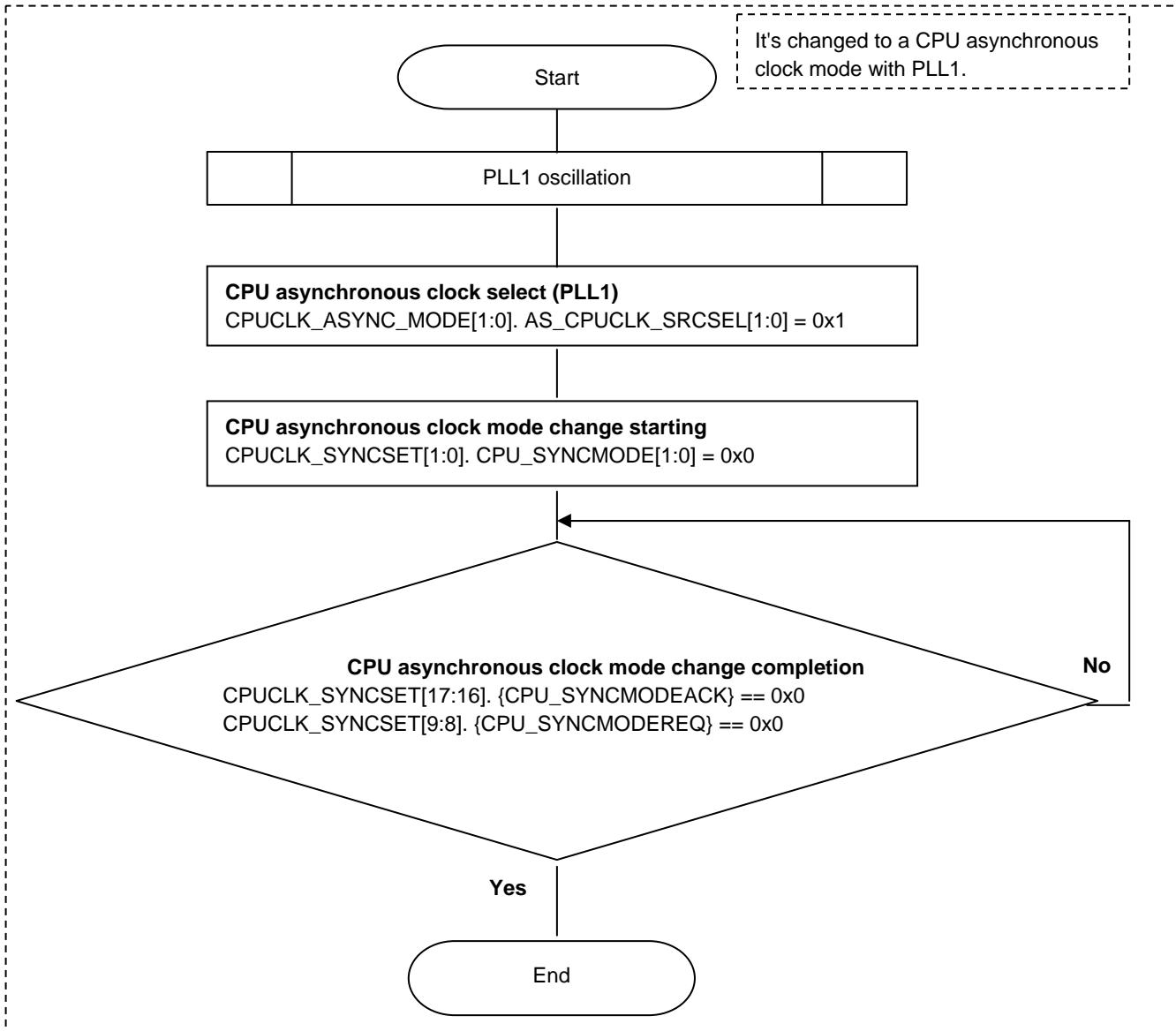
Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
MEMCCLK270_SEL	R/W	0	0	Select an MEMC_CLK270 delay amount. 0: Delay by 270° 1: MEMC_CLK (no phase delay)

**Remark** Setting of MEMCCLK270\_SEL to 1 is used for automatic calibration in the MEMC.

### 3.2.128 CPU\_CLK synchronous/asynchronous switch register

This register (CPUCLK\_SYNCSET: E011\_0358H) selects the CPUCLK mode.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								CPU_SYNCM ODEACK
15	14	13	12	11	10	9	8	
Reserved								CPU_SYNCM ODEREQ
7	6	5	4	3	2	1	0	
Reserved								CPU_SYNCMODE
Name	R/W	Bit No.	After Reset	Description				
Reserved	R	31:17	–	Reserved. If these bits are read, 0 is returned for each bit.				
CPU_SYNCMODEACK	R	16	1	Indicates the status of SYNCMODEACK. 0: Asynchronous mode 1: Synchronous clock mode				
Reserved	R	15:9	–	Reserved. If these bits are read, 0 is returned for each bit.				
CPU_SYNCMODEREQ	R	8	1	Indicates the status of SYNCMODEREQ. 0: Asynchronous mode 1: Synchronous clock mode				
Reserved	R	7:2	–	Reserved. If these bits are read, 0 is returned for each bit.				
CPU_SYNCMODE	R/W	1:0	3H	Specify the mode in which the CPU accesses the bus. Bit 0: Specify the setting for CPU_SYNCMODERREQ. 0H: Asynchronous mode 1H: Setting prohibited 2H: Setting prohibited 3H: Synchronous clock mode				

**Figure 3-12. CPU asynchronous clock mode change**

**3.2.129 CPU\_CLK source clock select register**

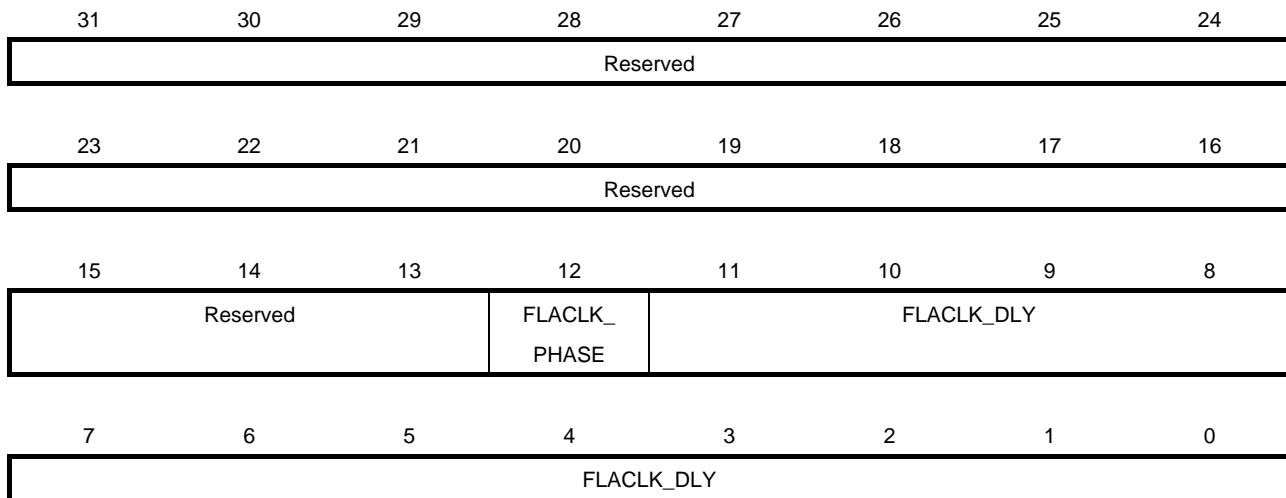
This register (CPUCLK\_ASYNC\_MODE: E011\_035CH) selects the source of CPU\_CLK.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved					AS_CPUCLK_SRCST		
7	6	5	4	3	2	1	0
Reserved						AS_CPUCLK_SRCSEL	

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
AS_CPUCLK_SRCST	R	10:8	1H	Indicates the clock used as the CPU domain clock. Bit 8: HM output Bit 9: PLL1 Bit 10: PLL4 One of these bits must be set to 1.
Reserved	R	7:2	–	Reserved. If these bits are read, 0 is returned for each bit.
AS_CPUCLK_SRCSEL	R/W	1:0	0H	Specify the source of CPU_CLK. In the clock synchronization mode, CPU_DOMAINCLK is forcibly used. Change the settings of these bits before switching the CPU_SYNMODE setting. 0H: CPU_DOMAINCLK 1H: PLL1 2H: PLL4 3H: Setting prohibited

### 3.2.130 FLASHCLK delay adjustment register

This register (FLA\_CLK\_DLY: E011\_0360H) selects a FLASHCLK delay amount.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:13	–	Reserved. If these bits are read, 0 is returned for each bit.
FLACLK_PHASE	R/W	12	1	Select the phase of the output FLASHCLK. 0: Inverted 1: Normal
FLACLK_DLY	R/W	11:0	000H	Select the amount of FLASHCLK delay. It's possible to set it as 13 stages and the delay value will be the rule of thumb of the type condition.  Bit 11 10 9 8 7 6 5 4 3 2 1 0 No. of Delay Selectors 0 1 0 0ps 0 1 1 500ps 0 1 1 1 1ns 0 1 1 1 1 1 1.5ns 0 1 1 1 1 1 1 2ns 0 1 1 1 1 1 1 1 1 2.5ns 0 1 1 1 1 1 1 1 1 1 3ns 0 1 1 1 1 1 1 1 1 1 1 3.5ns 0 1 1 1 1 1 1 1 1 1 1 1 4ns 0 1 1 1 1 1 1 1 1 1 1 1 1 4.5ns 0 1 1 1 1 1 1 1 1 1 1 1 1 1 5ns 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 5.5ns 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 6ns

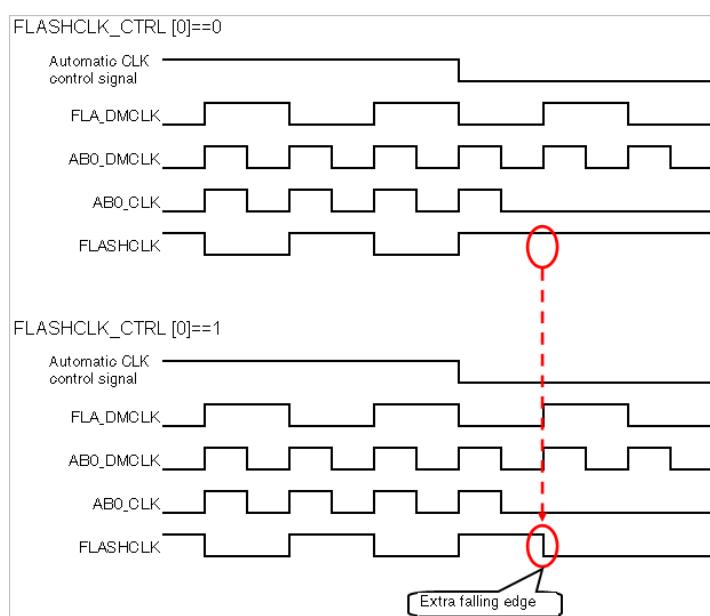
### 3.2.131 FLASHCLK stop status setting register

This register (FLASHCLK\_CTRL: E011\_0364H) specifies how to switch the gating cell for FLASHCLK.

31	30	29	28	27	26	25	24	Reserved
23	22	21	20	19	18	17	16	Reserved
15	14	13	12	11	10	9	8	FLASHCLK_CTRL_15_1
7	6	5	4	3	2	1	0	FLASHCLK_CTRL_15_1
								FLASHCLK_CTRL_0

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:16	–	Reserved. If these bits are read, 0 is returned for each bit.
FLASHCLK_CTRL_15_1	R/W	15:1	000H	General-purpose bits
FLASHCLK_CTRL_0	R/W	0	0	Specify how to switch the gating cell for FLASHCLK. 0: FLASHCLK is stopped at high (not controlled). 1: FLASHCLK is not allowed to stop at high.

If FLASHCLK is stopped while the FLA\_CLK\_DLY[12] is set to 0 (FLASHCLK is inverted), FLASHCLK is stopped at high if FLASHCLK\_CTRL[0] is set to 0 and is stopped at low if FLASHCLK\_CTRL[0] is set to 1. (An extra falling edge occurs.)



### 3.2.132 DSP\_CLK source clock select register

This register (DSPCLK\_ASYNC\_MODE: E011\_0368H) selects the source of DSP\_CLK (Audio engine).

※It's equipped with a DSP for Audio. But, the user can't use directly.

31	30	29	28	27	26	25	24			
Reserved										
23	22	21	20	19	18	17	16			
Reserved					DSPCLK_PLL4 0EN	DSPCLK_PLL1 0EN	DSPCLK_DMC K0EN			
15	14	13	12	11	10	9	8			
Reserved										
7	6	5	4	3	2	1	0			
Reserved					AS_DSPCLK_SRCSEL					
Name	R/W	Bit No.	After Reset	Description						
Reserved	R	31:19	0000H	Reserved. If these bits are read, 0 is returned for each bit.						
DSPCLK_PLL40EN	R	18	0	When DSP is using the PLL4, read value is "1".						
DSPCLK_PLL10EN	R	17	0	When DSP is using the PLL1, read value is "1".						
DSPCLK_DMCK0EN	R	16	1	When DSP is using the DOMAINCLK, read value is "1".						
Reserved	R	15:2	0000H	Reserved. If these bits are read, 0 is returned for each bit.						
AS_DSPCLK_SRCSEL	R/W	1:0	0H	Specify the source of DSP_CLK. 0H: DSP_DOMAINCLK 1H: PLL1 2H: PLL4 3H: Setting prohibited.						

### 3.2.133 AHB macro clock control register 0

This register (AHBCLKCTRL0: E011\_0380H) specifies whether to enable automatically control supply of the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved						MEMCLP	AB0LP
23	22	21	20	19	18	17	16
Reserved	ROMLP	SRCLP	Reserved	M2MLP	M2PLP	P2MLP	
15	14	13	12	11	10	9	8
AHBHL	AHBL	PBL1LP	PBL0LP	Reserved	BUS1LP	Reserved	
7	6	5	4	3	2	1	0
Reserved						CPULP	

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:26	–	Reserved. If these bits are read, 0 is returned for each bit.
MEMCLP	R/W	25	0	Specify whether to enable automatically control MEMC_CLK supply.
AB0LP	R/W	24	0	Specify whether to enable automatically control AB0_CLK supply.
Reserved	R	23:22	–	Reserved. If these bits are read, 0 is returned for each bit.
ROMLP	R/W	21	0	Specify whether to enable automatically control ROM_CLK supply.
SRCLP	R/W	20	0	Specify whether to enable automatically control SRC_CLK supply.
Reserved	R	19	–	Reserved. If this bit is read, 0 is returned.
M2MLP	R/W	18	0	Specify whether to enable automatically control M2M_CLK supply.
M2PLP	R/W	17	0	Specify whether to enable automatically control M2P_CLK supply.
P2MLP	R/W	16	0	Specify whether to enable automatically control P2M_CLK supply.
AHBHL	R/W	15	0	Specify whether to enable automatically control AHB_HCLK supply.
AHBL	R/W	14	0	Specify whether to enable automatically control AHB_CLK supply.
PBL1LP	R/W	13	0	Specify whether to enable automatically control PBL1_CLK supply.
PBL0LP	R/W	12	0	Specify whether to enable automatically control PBL0_CLK supply.
Reserved	R	11:10	–	Reserved. If these bits are read, 0 is returned for each bit.
BUS1LP	R/W	9	0	Specify whether to enable automatically control BUS1_CLK supply.
Reserved	R	8:7	–	Reserved. If these bits are read, 0 is returned for each bit.
Reserved	R/W	6:4	0H	Reserved. The recommendation set value is 7H.
Reserved	R	3:1	–	Reserved. If these bits are read, 0 is returned for each bit.
CPULP	R/W	0	0	Specify whether to enable automatically control CPU_CLK supply.

**Remark** 0: Disable, 1: Enable

### 3.2.134 AHB macro clock control register 1

This register (AHBCLKCTRL1: E011\_0384H) specifies whether to enable automatically control supply of the clock supplied to each block.

31	30	29	28	27	26	25	24	
Reserved								CAMLP
23	22	21	20	19	18	17	16	
Reserved	NTSLP	DTVLP		Reserved	A3DSYSLP	A3DVGLP		
15	14	13	12	11	10	9	8	
Reserved								ROTLP SIZLP
7	6	5	4	3	2	1	0	
Reserved	IMCWLP	IMCLP		Reserved	LCDCLP	LCDLP		
Name	R/W	Bit No.	After Reset	Description				
Reserved	R	31:29	–	Reserved. If these bits are read, 0 is returned for each bit.				
Reserved	R/W	28	0	Reserved. The recommendation set value is 1B.				
Reserved	R	27:26	–	Reserved. If these bits are read, 0 is returned for each bit.				
Reserved	R/W	25	0	Reserved. The recommendation set value is 1B.				
CAMLP	R/W	24	0	Specify whether to enable automatically control CAM_CLK supply.				
Reserved	R	23:22	–	Reserved. If these bits are read, 0 is returned for each bit.				
NTSLP	R/W	21	0	Specify whether to enable automatically control NTS_CLK supply.				
DTVLP	R/W	20	0	Specify whether to enable automatically control DTV_CLK supply.				
A2DSYSLP	R/W	19:18	0H	Reserved. If these bits are read, 0 is returned for each bit.				
A3DSYSLP	R/W	17	0	Specify whether to enable automatically control A3D_SYS_CLK supply.				
A3DMEMLP	R/W	16	0	Specify whether to enable automatically control A3D_MEM_CLK supply.				
Reserved	R	15:10	–	Reserved. If these bits are read, 0 is returned for each bit.				
ROTLP	R/W	9	0	Specify whether to enable automatically control ROT_CLK supply.				
SIZLP	R/W	8	0	Specify whether to enable automatically control SIZ_CLK supply.				
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.				
IMCWLP	R/W	5	0	Specify whether to enable automatically control IMCW_CLK supply.				
IMCLP	R/W	4	0	Specify whether to enable automatically control IMC_CLK supply.				
Reserved	R	3:2	–	Reserved. If these bits are read, 0 is returned for each bit.				
LCDCLP	R/W	1	0	Specify whether to enable automatically control LCD_CCLK supply.				
LCDLP	R/W	0	0	Specify whether to enable automatically control LCD_CLK supply.				

**Remark** 0: Disable, 1: Enable

### 3.2.135 AHB macro clock control register 2

This register (AHBCLKCTRL2: E011\_0388H) specifies whether to enable automatically control supply of the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved						CFIHP	CFILP
23	22	21	20	19	18	17	16
Reserved	SDCHLP	SDCLP	Reserved	SDIO2HLP	SDIO2LP		
15	14	13	12	11	10	9	8
Reserved	SDIO1HLP	SDIO1LP	Reserved	SDIO0HLP	SDIO0LP		
7	6	5	4	3	2	1	0
Reserved	USB1LP	USB0LP	Reserved				
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:26	–	Reserved. If these bits are read, 0 is returned for each bit.			
CFIHP	R/W	25	0	Specify whether to enable automatically control CFI_HCLK supply.			
CFILP	R/W	24	0	Specify whether to enable automatically control CFI_CLK supply.			
Reserved	R	23:22	–	Reserved. If these bits are read, 0 is returned for each bit.			
SDCHLP	R/W	21	0	Specify whether to enable automatically control SDC_HCLK supply.			
SDCLP	R/W	20	0	Specify whether to enable automatically control SDC_CLK supply.			
Reserved	R	19:18	–	Reserved. If these bits are read, 0 is returned for each bit.			
SDIO2HLP	R/W	17	0	Specify whether to enable automatically control SDIO2_HCLK supply.			
SDIO2LP	R/W	16	0	Specify whether to enable automatically control SDIO2_CLK supply.			
Reserved	R	15:14	–	Reserved. If these bits are read, 0 is returned for each bit.			
SDIO1HLP	R/W	13	0	Specify whether to enable automatically control SDIO1_HCLK supply.			
SDIO1LP	R/W	12	0	Specify whether to enable automatically control SDIO1_CLK supply.			
Reserved	R	11:10	–	Reserved. If these bits are read, 0 is returned for each bit.			
SDIO0HLP	R/W	9	0	Specify whether to enable automatically control SDIO0_HCLK supply.			
SDIO0LP	R/W	8	0	Specify whether to enable automatically control SDIO0_CLK supply.			
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.			
USB1LP	R/W	5	0	Specify whether to enable automatically control USB1_CLK supply.			
USB0LP	R/W	4	0	Specify whether to enable automatically control USB0_CLK supply.			
Reserved	R	3:0	–	Reserved. If these bits are read, 0 is returned for each bit.			

**Remark** 0: Disable, 1: Enable

### 3.2.136 AHB macro clock control register 3

This register (AHBCLKCTRL3: E011\_038CH) specifies whether to enable automatically control supply of the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved		INTALP		Reserved			
23	22	21	20	19	18	17	16
Reserved		PDMALP		Reserved			
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
USIBS5HLP	USIBS4HLP	USIBS3HLP	USIBS2HLP	Reserved		USIAS1HLP	USIAS0HLP
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:29	–	Reserved. If these bits are read, 0 is returned for each bit.			
INTALP	R/W	28	0	Specify whether to enable automatically control INTA_CLK supply.			
Reserved	R	27:25	–	Reserved. If these bits are read, 0 is returned for each bit.			
Reserved	R/W	24	0	Reserved. The recommendation set value is 1B.			
Reserved	R	23:21	–	Reserved. If these bits are read, 0 is returned for each bit.			
PDMALP	R/W	20	0	Specify whether to enable automatically control PDMA_CLK supply.			
Reserved	R	19:9	–	Reserved. If these bits are read, 0 is returned for each bit.			
Reserved	R/W	8	0	Reserved. The recommendation set value is 1B.			
USIBS5HLP	R/W	7	0	Specify whether to enable automatically control USIB_S5_HCLK supply.			
USIBS4HLP	R/W	6	0	Specify whether to enable automatically control USIB_S4_HCLK supply.			
USIBS3HLP	R/W	5	0	Specify whether to enable automatically control USIB_S3_HCLK supply.			
USIBS2HLP	R/W	4	0	Specify whether to enable automatically control USIB_S2_HCLK supply.			
Reserved	R	3	–	Reserved. If these bits are read, 0 is returned for each bit.			
Reserved	R/W	2	0	Reserved. The recommendation set value is 1B.			
USIAS1HLP	R/W	1	0	Specify whether to enable automatically control USIA_S1_HCLK supply.			
USIAS0HLP	R/W	0	0	Specify whether to enable automatically control USIA_S0_HCLK supply.			

**Remark** 0: Disable, 1: Enable

### 3.2.137 APB macro clock control register 0

This register (APBCLKCTRL0: E011\_0390H) specifies whether to enable automatically control supply of the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved			MEMCPCLKLP	Reserved			PMUPCLKLP
23	22	21	20	19	18	17	16
Reserved	M2MPCLKLP	M2PPCLKLP	P2MPCLKLP	Reserved		BUS1PCLKLP	BUS0PCLKLP
15	14	13	12	11	10	9	8
Reserved			SMUPCLKLP	Reserved		CHG1PCLKLP	CHGCLKLP
7	6	5	4	3	2	1	0
Reserved		GIOPCLKLP	INTAPCLKLP	Reserved			
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:29	–	Reserved. If these bits are read, 0 is returned for each bit.			
MEMCPCLKLP	R/W	28	1	Specify whether to enable automatically control APB clock for the MEMC.			
Reserved	R	27:25	–	Reserved. If these bits are read, 0 is returned for each bit.			
PMUPCLKLP	R/W	24	1	Specify whether to enable automatically control APB clock for the PMU.			
Reserved	R	23	–	Reserved. If this bit is read, 0 is returned.			
M2MPCLKLP	R/W	22	1	Specify whether to enable automatically control APB clock for M2M.			
M2PPCLKLP	R/W	21	1	Specify whether to enable automatically control APB clock for M2P.			
P2MPCLKLP	R/W	20	1	Specify whether to enable automatically control APB clock for P2M.			
Reserved	R	19:18	–	Reserved. If these bits are read, 0 is returned for each bit.			
BUS1PCLKLP	R/W	17	1	Specify whether to enable automatically control APB clock for BUS1.			
BUS0PCLKLP	R/W	16	1	Specify whether to enable automatically control APB clock for BUS0.			
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.			
SMUPCLKLP	R/W	12	0	Specify whether to enable automatically control APB clock for the SMU.			
Reserved	R	11:10	–	Reserved. If these bits are read, 0 is returned for each bit.			
CHG1PCLKLP	R/W	9	1	Specify whether to enable automatically control APB clock for CHG1.			
CHGCLKLP	R/W	8	1	Specify whether to enable automatically control APB clock for CHG.			
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.			
GIOPCLKLP	R/W	5	1	Specify whether to enable automatically control APB clock for GIO.			
INTAPCLKLP	R/W	4	1	Specify whether to enable automatically control APB clock for INTA.			
Reserved	R	3:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
Reserved	R/W	0	1	Reserved.			

**Remark** 0: Disable, 1: Enable

### 3.2.138 APB macro clock control register 1

This register (APBCLKCTRL1: E011\_0394H) specifies whether to enable automatically control supply of the clock supplied to each block.

31	30	29	28	27	26	25	24	
Reserved								PWMPCCLKLP
23	22	21	20	19	18	17	16	
Reserved								CAMPCLKLP
15	14	13	12	11	10	9	8	
Reserved		NTSPCLKLP	DTVPCCLKLP	Reserved			AVEPCLKLP	
7	6	5	4	3	2	1	0	
Reserved		ROTPCLKLP	SIZPCLKLP	Reserved	IMCWPCCLKLP	IMCPCLKLP	LCDPCLKLP	
Name	R/W	Bit No.	After Reset	Description				
Reserved	R	31:25	–	Reserved. If these bits are read, 0 is returned for each bit.				
PWMPCCLKLP	R/W	24	1	Specify whether to enable automatically control APB clock for PWM.				
Reserved	R	23:22	–	Reserved. If these bits are read, 0 is returned for each bit.				
Reserved	R/W	21	1	Reserved.				
Reserved	R	20:17	–	Reserved. If these bits are read, 0 is returned for each bit.				
CAMPCLKLP	R/W	16	1	Specify whether to enable automatically control APB clock for CAM.				
Reserved	R	15:14	–	Reserved. If these bits are read, 0 is returned for each bit.				
NTSPCLKLP	R/W	13	1	Specify whether to enable automatically control APB clock for NTS.				
DTVPCCLKLP	R/W	12	1	Specify whether to enable automatically control APB clock for DTV.				
Reserved	R	11:9	–	Reserved. If these bits are read, 0 is returned for each bit.				
AVEPCLKLP	R/W	8	1	Specify whether to enable automatically control APB clock for the AVE.				
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.				
ROTPCLKLP	R/W	5	1	Specify whether to enable automatically control APB clock for ROT.				
SIZPCLKLP	R/W	4	1	Specify whether to enable automatically control APB clock for SIZ.				
Reserved	R	3	–	Reserved. If this bit is read, 0 is returned.				
IMCWPCCLKLP	R/W	2	1	Specify whether to enable automatically control APB clock for IMCW.				
IMCPCLKLP	R/W	1	1	Specify whether to enable automatically control APB clock for the IMC.				
LCDPCLKLP	R/W	0	1	Specify whether to enable automatically control APB clock for the LCD.				

**Remark** 0: Disable, 1: Enable

### 3.2.139 APB macro clock control register 2

This register (APBCLKCTRL2: E011\_0398H) specifies whether to enable automatically control supply of the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							AFSPCLKLP
23	22	21	20	19	18	17	16
Reserved	STIPCLKLP	TIMPCLKLP	Reserved				
15	14	13	12	11	10	9	8
Reserved	ICEPCLKLP	Reserved			USIBU3PCLK LP	USIBU2PCLK LP	USIBU1PCLK LP
7	6	5	4	3	2	1	0
USIBS5PCLK LP	USIBS4PCLKLP	USIBS3PCLKLP	USIBS2PCLKLP	Reserved	USIAU0PCLK LP	USIAS1PCLKLP	USIAS0PCLK LP

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Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:29	–	Reserved. If these bits are read, 0 is returned for each bit.
Reserved	R/W	28	1	Reserved.
Reserved	R	27:26	–	Reserved. If these bits are read, 0 is returned for each bit.
Reserved	R/W	25	1	Reserved.
AFSPCLKLP	R/W	24	1	Specify whether to enable automatically control APB clock for AFS.
Reserved	R	23:22	–	Reserved. If these bits are read, 0 is returned for each bit.
STIPCLKLP	R/W	21	1	Specify whether to enable automatically control APB clock for STI.
TIMPCLKLP	R/W	20	1	Specify whether to enable automatically control APB clock for TIM.
Reserved	R	19:15	–	Reserved. If these bits are read, 0 is returned for each bit.
ICEPCLKLP	R/W	14	1	Specify whether to enable automatically control APB clock for ICE.
Reserved	R/W	13	–	Reserved
USIBU4PCLKLP	R/W	12	1	Specify whether to enable automatically control APB clock for USIB_U4
Reserved	R/W	11	1	Reserved
USIBU3PCLKLP	R/W	10	1	Specify whether to enable automatically control APB clock for USIB_U3.
USIBU2PCLKLP	R/W	9	1	Specify whether to enable automatically control APB clock for USIB_U2.
USIBU1PCLKLP	R/W	8	1	Specify whether to enable automatically control APB clock for USIB_U1.
USIBS5PCLKLP	R/W	7	1	Specify whether to enable automatically control APB clock for USIB_S5.
USIBS4PCLKLP	R/W	6	1	Specify whether to enable automatically control APB clock for USIB_S4.

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Name	R/W	Bit No.	After Reset	Description
USIBS3PCLKLP	R/W	5	1	Specify whether to enable automatically control APB clock for USIB_S3.
USIBS2PCLKLP	R/W	4	1	Specify whether to enable automatically control APB clock for USIB_S2.
Reserved	R/W	3	1	Reserved.
USIAU0PCLKLP	R/W	2	1	Specify whether to enable automatically control APB clock for USIA_U0.
USIAS1PCLKLP	R/W	1	1	Specify whether to enable automatically control APB clock for USIA_S1.
USIAS0PCLKLP	R/W	0	1	Specify whether to enable automatically control APB clock for USIA_S0.

**Remark** 0: Disable, 1: Enable

### 3.2.140 Asynchronous macro clock control register

This register (CLKCTRL: E011\_039CH) specifies whether to enable automatically control supply of the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved		USBPCICLKLP	Reserved				
15	14	13	12	11	10	9	8
USIBS5SCLK LP	USIBS4SCLK LP	USIBS3SCLK LP	USIBS2SCLK LP	Reserved		USIAS1SCLK LP	USIAS0S CLKLP
7	6	5	4	3	2	1	0
Reserved		MEMCCLK 270LP	AB0FLASH CLKLP	Reserved	A3DCORELP	Reserved	QR LP

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:22	–	Reserved. If these bits are read, 0 is returned for each bit.
USBPCICLKLP	R/W	21	0	Specify whether to enable automatically changing USB_PCICLK.
Reserved	R	20:16	–	Reserved. If these bits are read, 0 is returned for each bit.
USIBS5SCLKLP	R/W	15	0	Specify whether to enable automatically changing USIB_S5_SCLK.
USIBS4SCLKLP	R/W	14	0	Specify whether to enable automatically changing USIB_S4_SCLK.
USIBS3SCLKLP	R/W	13	0	Specify whether to enable automatically changing USIB_S3_SCLK.
USIBS2SCLKLP	R/W	12	0	Specify whether to enable automatically changing USIB_S2_SCLK.
Reserved	R	11:10	–	Reserved. If these bits are read, 0 is returned for each bit.
USIAS1SCLKLP	R/W	9	0	Specify whether to enable automatically changing USIA_S1_SCLK.
USIAS0SCLKLP	R/W	8	0	Specify whether to enable automatically changing USIA_S0_SCLK.
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.
MEMCCLK270LP	R/W	5	0	Specify whether to enable automatically changing MEMC_CLK270.
AB0FLASHCLKLP	R/W	4	0	Specify whether to enable automatically changing AB_CLK.
Reserved	R	3	–	Reserved. If this bit is read, 0 is returned.
A3DCORELP	R/W	2	0	Specify whether to enable automatically changing A3D_CORE_CLK.
Reserved	R	1	–	Reserved. If this bit is read, 0 is returned.
QR LP	R/W	0	0	Specify whether to enable automatically changing QR_CLK.

**Remark** 0: Disable, 1: Enable

### 3.2.141 AVE macro clock control register

This register (AVECLKCTRL: E011\_03A0H) specifies whether to enable automatically control supply of the clock supplied to each block.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								
7	6	5	4	3	2	1	0	
Reserved			AVECLP	Reserved			AVEALP	

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:5	–	Reserved. If these bits are read, 0 is returned for each bit.
AVECLP	R/W	4	0	Specify whether to enable automatically control AVE_CCLK supply. Set this bit to 0 before using the AVE.
Reserved	R/W	3:1	–	Reserved. If these bits are read, 0 is returned for each bit.
AVEALP	R/W	0	0	Specify whether to enable automatically control AVE_ACLK supply. Set this bit to 0 before using the AVE.

**Remark** 0: Disable, 1: Enable

Make AVECLKCTRL [0] [4] automatic control Off at the time of AVE initialization.

Make it automatic control On just after the DEC\_PIC\_RUN issue.

Every processing 1 frame do automatic control in Off and do clock supply.

Do automatic control in On once again just after the next DEC\_PIC\_RUN issue.

### 3.2.142 Access start timing setting register 0

This register (ACNT0: E011\_03C8H) sets up the access start timing.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved   SRC_ACNT   Reserved   AB_ACNT							
15	14	13	12	11	10	9	8
Reserved   MEMC_ACNT   Reserved   ROM_ACNT							
7	6	5	4	3	2	1	0
Reserved   AHB_ACNT   Reserved   BUS1_ACNT							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:22	–	Reserved. If these bits are read, 0 is returned for each bit.			
SRC_ACNT	R/W	21:20	0	Setting at the timing of SRC-BUS access starting permission. The recommendation value : 2H			
Reserved	R	19:18	–	Reserved. If these bits are read, 0 is returned for each bit.			
AB_ACNT	R/W	17:16	0	Setting at the timing of CPU-BUS access starting permission. The recommendation value : 2H			
Reserved	R	15:14	0	Reserved. If these bits are read, 0 is returned for each bit.			
MEMC_ACNT	R/W	13:12	0	Setting at the timing of MEMC-BUS access starting permission. The recommendation value : 2H			
Reserved	R	11:10	0	Reserved. If these bits are read, 0 is returned for each bit.			
ROM_ACNT	R/W	9:8	0	Setting at the timing of ROM-BUS access starting permission. The recommendation value : 2H			
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.			
AHB_ACNT	R/W	5:4	0	Setting at the timing of AHB-BUS access starting permission. The recommendation value : 2H			
Reserved	R	3:2	–	Reserved. If these bits are read, 0 is returned for each bit.			
BUS1_ACNT	R/W	1:0	0	Setting at the timing of BUS1-BUS access starting permission. The recommendation value : 2H			

After clock automatic control release of target macro, the setting is changed.

**Note : There is a possibility that it's changed for the recommendation value.**

### 3.2.143 Access start timing setting register 1

This register (ACNT1: E011\_03CCH) sets up the access start timing.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved						A3D_ACNT	
15	14	13	12	11	10	9	8
Reserved		IMCW_ACNT		Reserved		IMC_ACNT	
7	6	5	4	3	2	1	0
Reserved		ROT_ACNT		Reserved		SIZ_ACNT	
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:18	–	Reserved. If these bits are read, 0 is returned for each bit.			
A3D_ACNT	R/W	17:16	0	Setting at the timing of A3D-BUS access starting permission. The recommendation value : 2H			
Reserved	R/	15:14	0	Reserved. If these bits are read, 0 is returned for each bit.			
IMCW_ACNT	R/W	13:12	0	Setting at the timing of IMCW-BUS access starting permission. The recommendation value : 2H			
Reserved	R	11:10	0	Reserved. If these bits are read, 0 is returned for each bit.			
IMC_ACNT	R/W	9:8	0	Setting at the timing of IMC-BUS access starting permission. The recommendation value : 2H			
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.			
ROT_ACNT	R/W	5:4	0	Setting at the timing of ROT-BUS access starting permission. The recommendation value : 2H			
Reserved	R	3:2	–	Reserved. If these bits are read, 0 is returned for each bit.			
SIZ_ACNT	R/W	1:0	0	Setting at the timing of SIZ-BUS access starting permission. The recommendation value : 2H			

After clock automatic control release of target macro, the setting is changed.

**Note : There is a possibility that it's changed for the recommendation value.**

### 3.2.144 Transaction status register

This register (TRANEXIST: E011\_03D0H) indicates the status of the transaction.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		A3D_TRANEXI ST		AVE_TRANEXI ST		IMCW_TRANEXI XIST	
7	6	5	4	3	2	1	0
SIZ_TRANEXI ST	P2M_TRANEX IST	M2P_TRANEX IST	M2M_TRANEX IST	AHB_TRANEX IST	Reserved	CPU1_TRANEX XIST	CPU0_TRANEX XIST

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:13	–	Reserved. If these bits are read, 0 is returned for each bit.
A3D_TRANEXIST	R	12	0	The transaction state of the A3D is indicated.
AVE_TRANEXIST	R	11	0	The transaction state of the AVE is indicated.
IMCW_TRANEXIST	R	10	0	The transaction state of the IMCW is indicated.
IMC_TRANEXIST	R	9	0	The transaction state of the IMC is indicated.
ROT_TRANEXIST	R	8	0	The transaction state of the ROT is indicated.
SIZ_TRANEXIST	R	7	0	The transaction state of the SIZ is indicated.
P2M_TRANEXIST	R	6	0	The transaction state of the P2M is indicated.
M2P_TRANEXIST	R	5	0	The transaction state of the M2P is indicated.
M2M_TRANEXIST	R	4	0	The transaction state of the M2M is indicated.
AHB_TRANEXIST	R	3	0	The transaction state of the AHB is indicated.
Reserved	R	2	–	Reserved
CPU1_TRANEXIST	R	1	0	The transaction state of the CPU1 is indicated.
CPU0_TRANEXIST	R	0	0	The transaction state of the CPU0 is indicated.

**Remark** 0: Without transaction, 1: Transaction occurrence

### 3.2.145 CPU clock gate control register

This register (CPUGCLKCTRL: E011\_0400H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					CPU_SYSCLK_GCC	QR_CLK_GCC	CPU_CLK_GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:3	–	Reserved. If these bits are read, 0 is returned for each bit.
CPU_SYSCLK_GCC	R/W	2	1	Specify the gate control mode for CPU_SYSCLK.
QR_CLK_GCC	R/W	1	1	Specify the gate control mode for QR_CLK.
CPU_CLK_GCC	R/W	0	1	Specify the gate control mode for CPU_CLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.146 GIO clock gate control register

This register (GIOGCLKCTRL: E011\_0408H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						GIO_INT_CLK _GCC	GIO_CLK_ GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
GIO_INT_CLK_GCC	R/W	1	1	Specify the gate control mode for GIO_INT_CLK.
GIO_CLK_GCC	R/W	0	1	Specify the gate control mode for GIO_CLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.147 INTA clock gate control register

This register (INTAGCLKCTRL: E011\_040CH) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					INTA_TCLK_ GCC	INTA_CLK_ GCC	INTA_PCLK_ GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:3	–	Reserved. If these bits are read, 0 is returned for each bit.
INTA_TCLK_GCC	R/W	2	1	Specify the gate control mode for INTA_TCLK.
INTA_CLK_GCC	R/W	1	1	Specify the gate control mode for INTA_CLK.
INTA_PCLK_GCC	R/W	0	1	Specify the gate control mode for INTA_PCLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.148 CHG clock gate control register

This register (CHGGCLKCTRL: E011\_0410H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						CHG1_PCLK_GCC	CHG_PCLK_GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG1_PCLK_GCC	R/W	1	1	Specify the gate control mode for CHG1_PCLK.
CHG_PCLK_GCC	R/W	0	1	Specify the gate control mode for CHG_PCLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.149 BUS0 clock gate control register

This register (BUS0GCLKCTRL: E011\_0414H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							BUS0_PCLK_GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
Reserved	R	1	1	Reserved.
BUS0_PCLK_GCC	R/W	0	1	Specify the gate control mode for BUS0_PCLK. 0: Stop clock supply 1: Supply clock

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.150 BUS1 clock gate control register

This register (BUS1GCLKCTRL: E011\_0418H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						BUS1_CLK_GCC	BUS1_PCLK_GCC

Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.			
BUS1_CLK_GCC	R/W	1	1	Specify the gate control mode for BUS1_CLK.			
BUS1_PCLK_GCC	R/W	0	1	Specify the gate control mode for BUS1_PCLK.			

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.151 PBL0 clock gate control register

This register (PBL0GCLKCTRL: E011\_041CH) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						PBL0_CLK_GCC	

Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
PBL0_CLK_GCC	R/W	0	1	Specify the gate control mode for PBL0_CLK.			

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.152 PBL1 clock gate control register

This register (PBL1GCLKCTRL: E011\_0420H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							
PBL1_CLK_GCC							

**Remark 0:** Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.153 AHB clock gate control register

This register (AHBGCLKCTRL: E011\_0424H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							
AHB_HCLK_GCC      AHB_CLK_GCC							

Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.			
AHB_HCLK_GCC	R/W	1	1	Specify the gate control mode for AHB_HCLK.			
AHB_CLK_GCC	R/W	0	1	Specify the gate control mode for AHB_CLK.			

**Remark 0:** Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.154 P2M clock gate control register

This register (P2MGCLKCTRL: E011\_0428H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					P2M_TCLK_ GCC	P2M_CLK_ GCC	P2M_PCLK_ GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:3	–	Reserved. If these bits are read, 0 is returned for each bit.
P2M_TCLK_GCC	R/W	2	1	Specify the gate control mode for P2M_TCLK.
P2M_CLK_GCC	R/W	1	1	Specify the gate control mode for P2M_CLK.
P2M_PCLK_GCC	R/W	0	1	Specify the gate control mode for P2M_PCLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.155 M2P clock gate control register

This register (M2PGCLKCTRL: E011\_042CH) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					M2P_TCLK_ GCC	M2P_CLK_ GCC	M2P_PCLK_ GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:3	–	Reserved. If these bits are read, 0 is returned for each bit.
M2P_TCLK_GCC	R/W	2	1	Specify the gate control mode for M2P_TCLK.
M2P_CLK_GCC	R/W	1	1	Specify the gate control mode for M2P_CLK.
M2P_PCLK_GCC	R/W	0	1	Specify the gate control mode for M2P_PCLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.156 M2M clock gate control register

This register (M2MGCLKCTRL: E011\_0430H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						M2M_CLK_ GCC	M2M_PCLK_ GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
M2M_CLK_GCC	R/W	1	1	Specify the gate control mode for M2M_CLK.
M2M_PCLK_GCC	R/W	0	1	Specify the gate control mode for M2M_PCLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.157 PMU clock gate control register

This register (PMUGCLKCTRL: E011\_0434H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						PMU_32K_ CLK_GCC	PMU_CLK_ GCC

Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.			
PMU_32K_CLK_GCC	R/W	1	1	Specify the gate control mode for PMU_32K_CLK.			
PMU_CLK_GCC	R/W	0	1	Specify the gate control mode for PMU_CLK.			

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.158 SRC clock gate control register

This register (SRCGCLKCTRL: E011\_0438H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						SRC_CLK_ GCC	

Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
SRC_CLK_GCC	R/W	0	1	Specify the gate control mode for SRC_CLK.			

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.159 ROM clock gate control register

This register (ROMGCLKCTRL: E011\_043CH) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							
ROM_CLK_GCC							

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.160 AB clock gate control register

This register (ABGCLKCTRL: E011\_0440H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							
AB0_CLK_GCC							

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.161 FLA clock gate control register

This register (FLAGCLKCTRL: E011\_0444H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							FLASHCLK_GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
FLASHCLK_GCC	R/W	0	0	Specify the gate control mode for AB_CLK.

**Remark 0:** Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.162 MEMC clock gate control register

This register (MEMCGCLKCTRL: E011\_0448H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				MEMC_CLK 270_GCC	MEMC_RCLK_ GCC	MEMC_CLK_ GCC	MEMC_PCLK_ GCC

Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:4	–	Reserved. If these bits are read, 0 is returned for each bit.			
MEMC_CLK270_GCC	R/W	3	1	Specify the gate control mode for MEMC_CLK270.			
MEMC_RCLK_GCC	R/W	2	1	Specify the gate control mode for MEMC_RCLK.			
MEMC_CLK_GCC	R/W	1	1	Specify the gate control mode for MEMC_CLK.			
MEMC_PCLK_GCC	R/W	0	1	Specify the gate control mode for MEMC_PCLK.			

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.163 LCD clock gate control register

This register (LCDGCLKCTRL: E011\_044CH) sets up the clock supplied to each block.

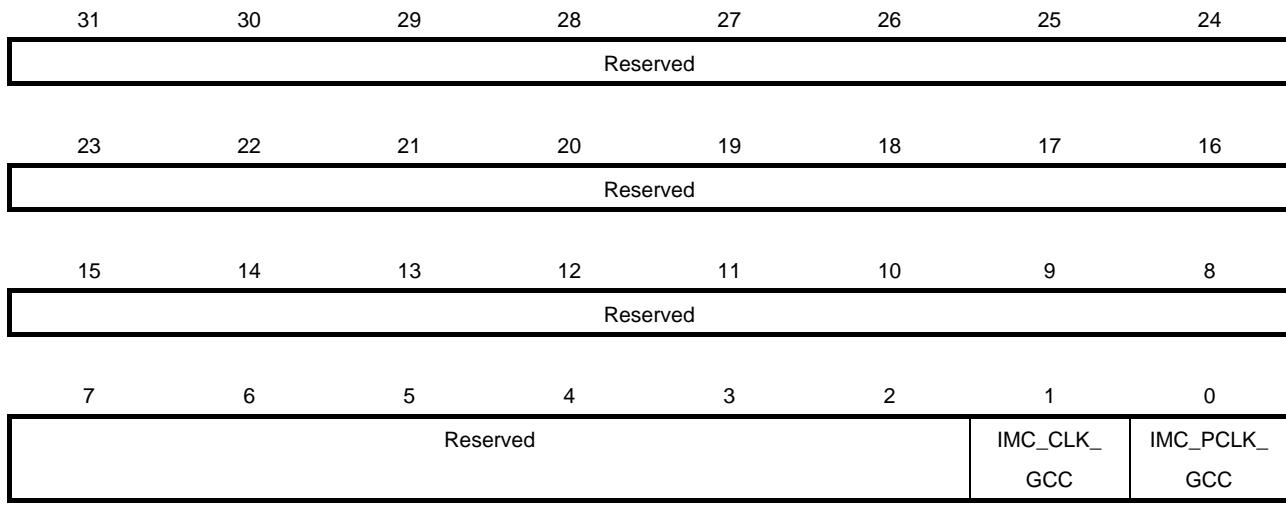
31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								
7	6	5	4	3	LCD_CCLK_ GCC	LCD_LCLK_ GCC	LCD_PCLK_ GCC	LCD_CLK_ GCC
Reserved				3				

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:4	0	Reserved. If these bits are read, 0 is returned for each bit.
LCD_CCLK_GCC	R/W	3	1	Specify the gate control mode for LCD_CCLK.
LCD_LCLK_GCC	R/W	2	0	Specify the gate control mode for LCD_LCLK.
LCD_PCLK_GCC	R/W	1	1	Specify the gate control mode for LCD_PCLK.
LCD_CLK_GCC	R/W	0	1	Specify the gate control mode for LCD_CLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.164 IMC clock gate control register

This register (IMCGCLKCTRL: E011\_0450H) sets up the clock supplied to each block.



Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.			
IMC_CLK_GCC	R/W	1	1	Specify the gate control mode for IMC_CLK.			
IMC_PCLK_GCC	R/W	0	1	Specify the gate control mode for IMC_PCLK.			

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.165 IMCW clock gate control register

This register (IMCWGCLKCTRL: E011\_0454H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						IMCW_CLK_ GCC	IMCW_PCLK_ GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
IMCW_CLK_GCC	R/W	1	1	Specify the gate control mode for IMCW_CLK.
IMCW_PCLK_GCC	R/W	0	1	Specify the gate control mode for IMCW_PCLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.166 SIZ clock gate control register

This register (SIZGCLKCTRL: E011\_0458H) sets up the clock supplied to each block.

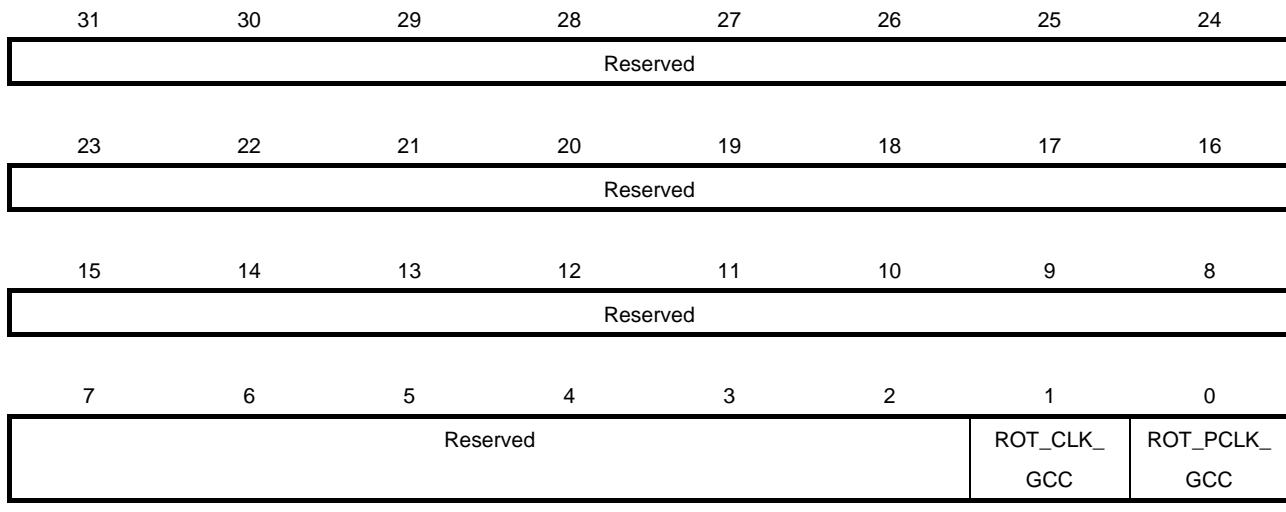
31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						SIZ_CLK_GCC	SIZ_PCLK_GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
SIZ_CLK_GCC	R/W	1	1	Specify the gate control mode for SIZ_CLK.
SIZ_PCLK_GCC	R/W	0	1	Specify the gate control mode for SIZ_PCLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.167 ROT clock gate control register

This register (ROTGCLKCTRL: E011\_045CH) sets up the clock supplied to each block.



Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.			
ROT_CLK_GCC	R/W	1	1	Specify the gate control mode for ROT_CLK.			
ROT_PCLK_GCC	R/W	0	1	Specify the gate control mode for ROT_PCLK.			

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.168 AVE clock gate control register

This register (AVEGCLKCTRL: E011\_0464H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					AVE_ACLK_ GCC	AVE_CCLK_ GCC	AVE_PCLK_ GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:3	–	Reserved. If these bits are read, 0 is returned for each bit.
AVE_ACLK_GCC	R/W	2	1	Specify the gate control mode for AVE_ACLK.
AVE_CCLK_GCC	R/W	1	0	Specify the gate control mode for AVE_CCLK.
AVE_PCLK_GCC	R/W	0	1	Specify the gate control mode for AVE_PCLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.169 A3D clock gate control register

This register (AVEGCLKCTRL: E011\_0464H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					A3D_CORE_CLK_GCC	A3D_MEM_CLK_GCC	A3D_SYS_CLK_GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:3	–	Reserved. If these bits are read, 0 is returned for each bit.
A3D_CORE_CLK_GCC	R/W	2	0	Specify the gate control mode for A3D_CORE_CLK.
A3D_MEM_CLK_GCC	R/W	1	1	Specify the gate control mode for A3D_MEM_CLK .
A3D_SYS_CLK_GCC	R/W	0	1	Specify the gate control mode for A3D_SYS_CLK .

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.170 DTV clock gate control register

This register (DTVGCLKCTRL: E011\_046CH) sets up the clock supplied to each block.

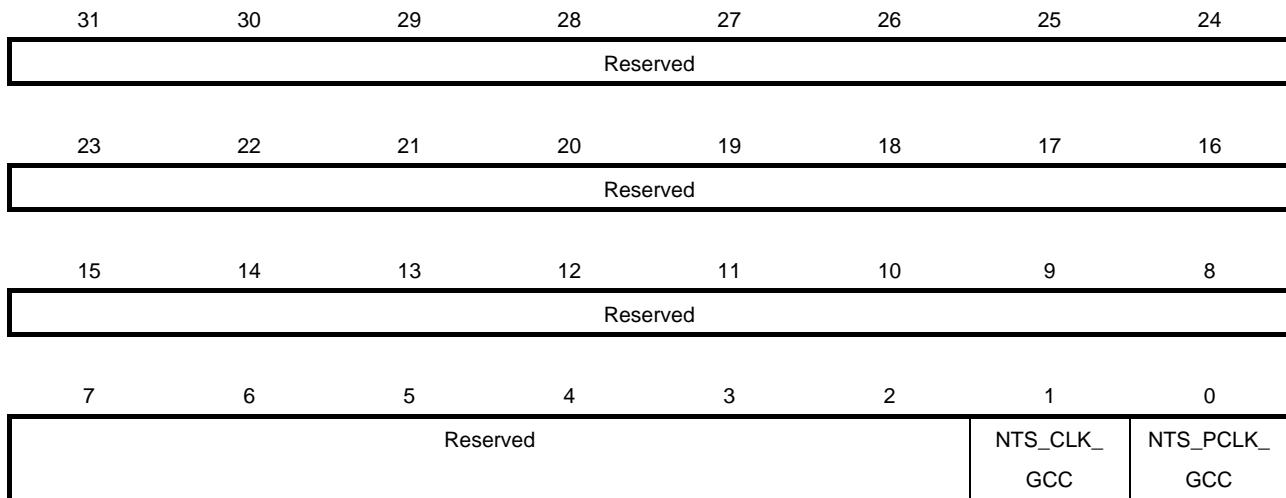
31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					DTV_SCLK_ GCC	DTV_CLK_ GCC	DTV_PCLK_ GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:3	–	Reserved. If these bits are read, 0 is returned for each bit.
DTV_SCLK_GCC	R/W	2	1	Specify the gate control mode for DTV_SCLK.
DTV_CLK_GCC	R/W	1	1	Specify the gate control mode for DTV_CLK.
DTV_PCLK_GCC	R/W	0	1	Specify the gate control mode for DTV_PCLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.171 NTS clock gate control register

This register (NTSGCLKCTRL: E011\_0470H) sets up the clock supplied to each block.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
NTS_CLK_GCC	R/W	1	1	Specify the gate control mode for NTS_CLK.
NTS_PCLK_GCC	R/W	0	1	Specify the gate control mode for NTS_PCLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.172 CAM clock gate control register

This register (CAMGCLKCTRL: E011\_0474H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					CAM_SCLK_ GCC	CAM_CLK_ GCC	CAM_PCLK_ GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:3	–	Reserved. If these bits are read, 0 is returned for each bit.
CAM_SCLK_GCC	R/W	2	0	Specify the gate control mode for CAM_SCLK.
CAM_CLK_GCC	R/W	1	1	Specify the gate control mode for CAM_CLK.
CAM_PCLK_GCC	R/W	0	1	Specify the gate control mode for CAM_PCLK.

**Remark 0:** Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.173 PWM clock gate control register

This register (PWMGCLKCTRL: E011\_0484H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					PWM_ PWCLK1_GCC	PWM_ PWCLK0_GCC	PWM_ PCLK_GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:3	–	Reserved. If these bits are read, 0 is returned for each bit.
PWM_PWCLK1_GCC	R/W	2	0	Specify the gate control mode for PWM_PWCLK1.
PWM_PWCLK0_GCC	R/W	1	0	Specify the gate control mode for PWM_PWCLK0.
PWM_PCLK_GCC	R/W	0	1	Specify the gate control mode for PWM_PCLK.

**Remark 0:** Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.174 IIC0 clock gate control register

This register (IIC0GCLKCTRL: E011\_048CH) sets up the clock supplied to each block.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
IIC0_SCLK_GCC	R/W	1	0	Specify the gate control mode for IIC0_SCLK.
IIC0_CLK_GCC	R/W	0	1	Specify the gate control mode for IIC0_CLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.175 IIC1 clock gate control register

This register (IIC1GCLKCTRL: E011\_0490H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						IIC1_SCLK_GCC	IIC1_CLK_GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
IIC1_SCLK_GCC	R/W	1	0	Specify the gate control mode for IIC1_SCLK.
IIC1_CLK_GCC	R/W	0	1	Specify the gate control mode for IIC1_CLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.176 USB clock gate control register

This register (USBGCLKCTRL: E011\_0494H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	USB_PCICLK_GCC	Reserved	USB1_CLK_GCC
Reserved				3	USB_PCICLK_GCC	Reserved	USB1_CLK_GCC
Reserved				2	USB_PCICLK_GCC	Reserved	USB0_CLK_GCC
Reserved				1	USB1_CLK_GCC	Reserved	USB0_CLK_GCC
Reserved				0	USB0_CLK_GCC	Reserved	USB0_CLK_GCC

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.177 USIAS0 clock gate control register

This register (USIAS0GCLKCTRL: E011\_0498H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					USIA_S0_ HCLK_GCC	USIA_S0_ SCLK_GCC	USIA_S0_ PCLK_GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:3	–	Reserved. If these bits are read, 0 is returned for each bit.
USIA_S0_HCLK_GCC	R/W	2	1	Specify the gate control mode for SIO0_HCLK.
USIA_S0_SCLK_GCC	R/W	1	1	Specify the gate control mode for SIO0_SCLK.
USIA_S0_PCLK_GCC	R/W	0	1	Specify the gate control mode for SIO0_PCLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.178 USIAS1 clock gate control register

This register (USIAS1GCLKCTRL: E011\_049CH) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					USIA_S1_ HCLK_GCC	USIA_S1_ SCLK_GCC	USIA_S1_ PCLK_GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:3	–	Reserved. If these bits are read, 0 is returned for each bit.
USIA_S1_HCLK_GCC	R/W	2	1	Specify the gate control mode for SIO1_HCLK.
USIA_S1_SCLK_GCC	R/W	1	0	Specify the gate control mode for SIO1_SCLK.
USIA_S1_PCLK_GCC	R/W	0	1	Specify the gate control mode for SIO1_PCLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.179 USIAU0 clock gate control register

This register (USIAU0GCLKCTRL: E011\_04A0H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						USIA_U0_ SCLK_GCC	USIA_U0_ PCLK_GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
USIA_U0_SCLK_GCC	R/W	1	1	Specify the gate control mode for UART0_SCLK.
USIA_U0_PCLK_GCC	R/W	0	1	Specify the gate control mode for UART0_PCLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.180 USIBS2 clock gate control register

This register (USIBS2GCLKCTRL: E011\_04A8H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					USIB_S2_ HCLK_GCC	USIB_S2_ SCLK_GCC	USIB_S2_ PCLK_GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:3	–	Reserved. If these bits are read, 0 is returned for each bit.
USIB_S2_HCLK_GCC	R/W	2	1	Specify the gate control mode for SIO2_HCLK.
USIB_S2_SCLK_GCC	R/W	1	0	Specify the gate control mode for SIO2_SCLK.
USIB_S2_PCLK_GCC	R/W	0	1	Specify the gate control mode for SIO2_PCLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.181 USIBS3 clock gate control register

This register (USIBS3GCLKCTRL: E011\_04ACH) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					USIB_S3_ HCLK_GCC	USIB_S3_ SCLK_GCC	USIB_S3_ PCLK_GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:3	–	Reserved. If these bits are read, 0 is returned for each bit.
USIB_S3_HCLK_GCC	R/W	2	1	Specify the gate control mode for SIO3_HCLK.
USIB_S3_SCLK_GCC	R/W	1	0	Specify the gate control mode for SIO3_SCLK.
USIB_S3_PCLK_GCC	R/W	0	1	Specify the gate control mode for SIO3_PCLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.182 USIBS4 clock gate control register

This register (USIBS4GCLKCTRL: E011\_04B0H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					USIB_S4_ HCLK_GCC	USIB_S4_ SCLK_GCC	USIB_S4_ PCLK_GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:3	–	Reserved. If these bits are read, 0 is returned for each bit.
USIB_S4_HCLK_GCC	R/W	2	1	Specify the gate control mode for SIO4_HCLK.
USIB_S4_SCLK_GCC	R/W	1	0	Specify the gate control mode for SIO4_SCLK.
USIB_S4_PCLK_GCC	R/W	0	1	Specify the gate control mode for SIO4_PCLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.183 USIBS5 clock gate control register

This register (USIBS5GCLKCTRL: E011\_04B4H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					USIB_S5_ HCLK_GCC	USIB_S5_ SCLK_GCC	USIB_S5_ PCLK_GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:3	–	Reserved. If these bits are read, 0 is returned for each bit.
USIB_S5_HCLK_GCC	R/W	2	1	Specify the gate control mode for SIO5_HCLK.
USIB_S5_SCLK_GCC	R/W	1	0	Specify the gate control mode for SIO5_SCLK.
USIB_S5_PCLK_GCC	R/W	0	1	Specify the gate control mode for SIO5_PCLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.184 USIBU1 clock gate control register

This register (USIBU1GCLKCTRL: E011\_04B8H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						USIB_U1_ SCLK_GCC	USIB_U1_ PCLK_GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
USIB_U1_SCLK_GCC	R/W	1	0	Specify the gate control mode for UART1_SCLK.
USIB_U1_PCLK_GCC	R/W	0	1	Specify the gate control mode for UART1_PCLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.185 USIBU2 clock gate control register

This register (USIBU2GCLKCTRL: E011\_04BCH) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						USIB_U2_ SCLK_GCC	USIB_U2_ PCLK_GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
USIB_U2_SCLK_GCC	R/W	1	0	Specify the gate control mode for UART2_SCLK.
USIB_U2_PCLK_GCC	R/W	0	1	Specify the gate control mode for UART2_PCLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.186 USIBU3 clock gate control register

This register (USIBU3GCLKCTRL: E011\_04C0H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						USIB_U3_ SCLK_GCC	USIB_U3_ PCLK_GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
USIB_U3_SCLK_GCC	R/W	1	0	Specify the gate control mode for UART3_SCLK.
USIB_U3_PCLK_GCC	R/W	0	1	Specify the gate control mode for UART3_PCLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.187 SDIO0 clock gate control register

This register (SDIO0GCLKCTRL: E011\_04C8H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					SDIO0_HCLK_ GCC	SDIO0_SCLK_ GCC	SDIO0_CLK_ GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:3	–	Reserved. If these bits are read, 0 is returned for each bit.
SDIO0_HCLK_GCC	R/W	2	1	Specify the gate control mode for SDIO0_HCLK.
SDIO0_SCLK_GCC	R/W	1	0	Specify the gate control mode for SDIO0_SCLK.
SDIO0_CLK_GCC	R/W	0	1	Specify the gate control mode for SDIO0_CLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.188 SDIO1 clock gate control register

This register (SDIO1GCLKCTRL: E011\_04CCH) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					SDIO1_HCLK_ GCC	SDIO1_SCLK_ GCC	SDIO1_CLK_ GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:3	–	Reserved. If these bits are read, 0 is returned for each bit.
SDIO1_HCLK_GCC	R/W	2	1	Specify the gate control mode for SDIO1_HCLK.
SDIO1_SCLK_GCC	R/W	1	0	Specify the gate control mode for SDIO1_SCLK.
SDIO1_CLK_GCC	R/W	0	1	Specify the gate control mode for SDIO1_CLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.189 SDIO2 clock gate control register

This register (SDIO2GCLKCTRL: E011\_04D0H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				SDIO2_HCLK_ GCC	SDIO2_SCLK_ GCC	SDIO2_CLK_G CC	

Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:3	–	Reserved. If these bits are read, 0 is returned for each bit.			
SDIO2_HCLK_GCC	R/W	2	1	Specify the gate control mode for SDIO2_HCLK.			
SDIO2_SCLK_GCC	R/W	1	0	Specify the gate control mode for SDIO2_SCLK.			
SDIO2_CLK_GCC	R/W	0	1	Specify the gate control mode for SDIO2_CLK.			

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.190 SDC clock gate control register

This register (SDCGCLKCTRL: E011\_04D4H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					SDC_HCLK_ GCC	Reserved	SDC_CLK_ GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:3	–	Reserved. If these bits are read, 0 is returned for each bit.
SDC_HCLK_GCC	R/W	2	1	Specify the gate control mode for SDC_HCLK.
Reserved	R/W	1	–	Reserved.
SDC_CLK_GCC	R/W	0	1	Specify the gate control mode for SDC_CLK.

**Remark 0:** Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.191 CFI clock gate control register

This register (CFIGCLKCTRL: E011\_04DCH) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					CFI_CLK_ GCC	CFI_HCLK_ GCC	Reserved

Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:3	–	Reserved. If these bits are read, 0 is returned for each bit.			
CFI_CLK_GCC	R/W	2	1	Specify the gate control mode for CFI_CLK.			
CFI_HCLK_GCC	R/W	1	1	Specify the gate control mode for CFI_HCLK.			
Reserved	R/W	0	–	Reserved. If this bit is read, 0 is returned.			

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.192 TI0 clock gate control register

This register (TI0GCLKCTRL: E011\_04ECH) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							TI0_CLK_GCC

Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
TI0_CLK_GCC	R/W	0	1	Specify the gate control mode for TI0_CLK.			

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.193 TI1 clock gate control register

This register (TI1GCLKCTRL: E011\_04F0H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								
7	6	5	4	3	2	1	0	
Reserved								TI1_CLK_GCC
Name	R/W	Bit No.	After Reset	Description				
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.				
TI1_CLK_GCC	R/W	0	1	Specify the gate control mode for TI1_CLK.				

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.194 TI2 clock gate control register

This register (TI2GCLKCTRL: E011\_04F4H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								
7	6	5	4	3	2	1	0	
Reserved								TI2_CLK_GCC
Name	R/W	Bit No.	After Reset	Description				
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.				
TI2_CLK_GCC	R/W	0	1	Specify the gate control mode for TI2_CLK.				

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.195 TI3 clock gate control register

This register (TI3GCLKCTRL: E011\_04F8H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							
TI3_CLK_GCC							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
TI3_CLK_GCC	R/W	0	1	Specify the gate control mode for TI3_CLK.			

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.196 TG0 clock gate control register

This register (TG0GCLKCTRL: E011\_04FCH) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							
TG0_CLK_GCC							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
TG0_CLK_GCC	R/W	0	1	Specify the gate control mode for TG0_CLK.			

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.197 TG1 clock gate control register

This register (TG1GCLKCTRL: E011\_0500H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							
TG1_CLK_GCC							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
TG1_CLK_GCC	R/W	0	1	Specify the gate control mode for TG1_CLK.			

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.198 TG2 clock gate control register

This register (TG2GCLKCTRL: E011\_0504H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							
TG2_CLK_GCC							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
TG2_CLK_GCC	R/W	0	1	Specify the gate control mode for TG2_CLK.			

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.199 TG3 clock gate control register

This register (TG3GCLKCTRL: E011\_0508H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							
TG3_CLK_GCC							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
TG3_CLK_GCC	R/W	0	1	Specify the gate control mode for TG3_CLK.			

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.200 TG4 clock gate control register

This register (TG4GCLKCTRL: E011\_050CH) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							
TG4_CLK_GCC							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
TG4_CLK_GCC	R/W	0	1	Specify the gate control mode for TG4_CLK.			

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.201 TG5 clock gate control register

This register (TG5GCLKCTRL: E011\_0510H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							
TG5_CLK_GCC							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
TG5_CLK_GCC	R/W	0	1	Specify the gate control mode for TG5_CLK.			

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.202 TW0 clock gate control register

This register (TW0GCLKCTRL: E011\_0514H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							
TW0_CLK_GCC							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
TW0_CLK_GCC	R/W	0	1	Specify the gate control mode for TW0_CLK.			

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.203 TW1 clock gate control register

This register (TW1GCLKCTRL: E011\_0518H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							
TW1_CLK_GCC							

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.204 TW2 clock gate control register

This register (TW2GCLKCTRL: E011\_051CH) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							
TW2_CLK_GCC							

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.205 TW3 clock gate control register

This register (TW3GCLKCTRL: E011\_0520H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							TW3_CLK_GCC

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.206 TIM clock gate control register

This register (TIMGCLKCTRL: E011\_0524H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							TIM_PCLK_GCC

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.207 STI clock gate control register

This register (STIGCLKCTRL: E011\_0528H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						STI_SCLK_ GCC	STI_PCLK_ GCC

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
STI_SCLK_GCC	R/W	1	1	Specify the gate control mode for STI_SCLK.
STI_PCLK_GCC	R/W	0	1	Specify the gate control mode for STI_PCLK.

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.208 AFS clock gate control register

This register (AFSGCLKCTRL: E011\_0530H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						AFS_32K_ CLK_GCC	AFS_PCLK_ GCC

Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.			
AFS_32K_CLK_GCC	R/W	1	1	Specify the gate control mode for AFS_32K_CLK.			
AFS_PCLK_GCC	R/W	0	1	Specify the gate control mode for AFS_PCLK.			

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.209 REF clock gate control register

This register (REFGCLKCTRL: E011\_053CH) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						REF_CLKO_ GCC	

Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
REF_CLK_GCC	R/W	0	0	Specify the gate control mode for REF_CLKO.			

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.210 TW4 clock gate control register

This register (TW4GCLKCTRL: E011\_0540H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							TW4_CLK_GCC

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.211 PDMA clock gate control register

This register (PDMAGCLKCTRL: E011\_0554H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							PDMA_CLK_GCC

**Remark** 0: Stop clock supply (with gate control), 1: Supply clock (without gate control)

### 3.2.212 TW0\_TIN/TI0\_TIN setting register

This register (TWI0TIN\_SEL: E011\_0600H) specifies the clock source for TW0 and TI0.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved						TW0TIN_SEL	
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						TI0TIN_SEL	

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:18	–	Reserved. If these bits are read, 0 is returned for each bit.
TW0TIN_SEL	R/W	17:16	1H	Specify the clock source for TW0. 0H: PLL3 division (division factor is specified by TIMCLK_DIV) 1H: 32.768 kHz 2H: 32 kHz (32.768 kHz clock thinned out) 3H: Setting prohibited
Reserved	R	15:2	–	Reserved. If these bits are read, 0 is returned for each bit.
TI0TIN_SEL	R/W	1:0	1H	Specify the clock source for TI0. 0H: PLL3 division (division factor is specified by TIMCLK_DIV) 1H: 32.768 kHz 2H: 32 kHz (32.768 kHz clock thinned out) 3H: Setting prohibited

### 3.2.213 TW1\_TIN/TI1\_TIN setting register

This register (TWI1TIN\_SEL: E011\_0604H) specifies the clock source for TW1 and TI1.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved						TW1TIN_SEL	
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						TI1TIN_SEL	

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:18	–	Reserved. If these bits are read, 0 is returned for each bit.
TW1TIN_SEL	R/W	17:16	1H	Specify the clock source for TW1. 0H: PLL3 division (division factor is specified by TIMCLK_DIV) 1H: 32.768 kHz 2H: 32 kHz (32.768 kHz clock thinned out) 3H: Setting prohibited
Reserved	R	15:2	–	Reserved. If these bits are read, 0 is returned for each bit.
TI1TIN_SEL	R/W	1:0	1H	Specify the clock source for TI1. 0H: PLL3 division (division factor is specified by TIMCLK_DIV) 1H: 32.768 kHz 2H: 32 kHz (32.768 kHz clock thinned out) 3H: Setting prohibited

### 3.2.214 TW2\_TIN/TI2\_TIN setting register

This register (TWI2TIN\_SEL: E011\_0608H) specifies the clock source for TW2 and TI2.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved						TW2TIN_SEL	
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						TI2TIN_SEL	

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:18	–	Reserved. If these bits are read, 0 is returned for each bit.
TW2TIN_SEL	R/W	17:16	1H	Specify the clock source for TW2. 0H: PLL3 division (division factor is specified by TIMCLK_DIV) 1H: 32.768 kHz 2H: 32 kHz (32.768 kHz clock thinned out) 3H: Setting prohibited
Reserved	R	15:2	–	Reserved. If these bits are read, 0 is returned for each bit.
TI2TIN_SEL	R/W	1:0	1H	Specify the clock source for TI2. 0H: PLL3 division (division factor is specified by TIMCLK_DIV) 1H: 32.768 kHz 2H: 32 kHz (32.768 kHz clock thinned out) 3H: Setting prohibited

### 3.2.215 TW3\_TIN/TI3\_TIN setting register

This register (TWI3TIN\_SEL: E011\_060CH) specifies the clock source for TW3 and TI3.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved						TW3TIN_SEL	
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						TI3TIN_SEL	

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:18	–	Reserved. If these bits are read, 0 is returned for each bit.
TW3TIN_SEL	R/W	17:16	1H	Specify the clock source for TW3. 0H: PLL3 division (division factor is specified by TIMCLK_DIV) 1H: 32.768 kHz 2H: 32 kHz (32.768 kHz clock thinned out) 3H: Setting prohibited
Reserved	R	15:2	–	Reserved. If these bits are read, 0 is returned for each bit.
TI3TIN_SEL	R/W	1:0	1H	Specify the clock source for TI3. 0H: PLL3 division (division factor is specified by TIMCLK_DIV) 1H: 32.768 kHz 2H: 32 kHz (32.768 kHz clock thinned out) 3H: Setting prohibited

### 3.2.216 TG0-TG5\_TIN setting register

This register (TGnTIN\_SEL: E011\_0610H) specifies the clock source for TG0 to TG5.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved		TG5TIN_SEL		Reserved		TG4TIN_SEL	
15	14	13	12	11	10	9	8
Reserved		TG3TIN_SEL		Reserved		TG2TIN_SEL	
7	6	5	4	3	2	1	0
Reserved		TG1TIN_SEL		Reserved		TG0TIN_SEL	

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:22	–	Reserved. If these bits are read, 0 is returned for each bit.
TG5TIN_SEL	R/W	21:20	1H	Specify the clock source for TG5. 0H: PLL3 division (division factor is specified by TIMCLK_DIV) 1H: 32.768 kHz 2H: 32 kHz (32.768 kHz clock thinned out) 3H: Setting prohibited
Reserved	R	19:18	–	Reserved. If these bits are read, 0 is returned for each bit.
TG4TIN_SEL	R/W	17:16	1H	Specify the clock source for TG4. 0H: PLL3 division (division factor is specified by TIMCLK_DIV) 1H: 32.768 kHz 2H: 32 kHz (32.768 kHz clock thinned out) 3H: Setting prohibited
Reserved	R	15:14	–	Reserved. If these bits are read, 0 is returned for each bit.
TG3TIN_SEL	R/W	13:12	1H	Specify the clock source for TG3. 0H: PLL3 division (division factor is specified by TIMCLK_DIV) 1H: 32.768 kHz 2H: 32 kHz (32.768 kHz clock thinned out) 3H: Setting prohibited
Reserved	R	11:10	–	Reserved. If these bits are read, 0 is returned for each bit.
TG2TIN_SEL	R/W	9:8	1H	Specify the clock source for TG2. 0H: PLL3 division (division factor is specified by TIMCLK_DIV) 1H: 32.768 kHz 2H: 32 kHz (32.768 kHz clock thinned out) 3H: Setting prohibited
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.

(2/2)

Name	R/W	Bit No.	After Reset	Description
TG1TIN_SEL	R/W	5:4	1H	Specify the clock source for TG1. 0H: PLL3 division (division factor is specified by TIMCLK_DIV) 1H: 32.768 kHz 2H: 32 kHz (32.768 kHz clock thinned out) 3H: Setting prohibited
Reserved	R	3:2	–	Reserved. If these bits are read, 0 is returned for each bit.
TG0TIN_SEL	R/W	1:0	1H	Specify the clock source for TG0. 0H: PLL3 division (division factor is specified by TIMCLK_DIV) 1H: 32.768 kHz 2H: 32 kHz (32.768 kHz clock thinned out) 3H: Setting prohibited

### 3.2.217 Timer clock frequency division setting register

This register (TIMCLKDIV: E011\_0614H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved						TIMCLK_PLLSEL	
7	6	5	4	3	2	1	0
TIMCLK_DIV							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:10	–	Reserved. If these bits are read, 0 is returned for each bit.			
TIMCLK_PLLSEL	R/W	9:8	0H	Specify the source of TIM_CLK. 0H: PLL3 1H: PLL4 2H: OSC0 3H: OSC1			
TIMCLK_DIV	R/W	7:0	FFH	Specify the division factor for TIM_CLK. Division factor = specified value + 1 It's set as 50MHz >= TIM_CLK.			

When changing the settings of this register, make sure that the TIM\_CLK output has stopped.

Use this register to select the source of TIM\_CLK and specify the frequency division factor.

If this register is set to 0000\_00FFH (PLL3 is selected as the clock source), the frequency is calculated as follows:

$$\text{TIM\_CLK} = 229.376 \text{ (MHz)} / 256 = 0.896 \text{ MHz}$$

### 3.2.218 USIA\_SCLK frequency division setting register

This register (USIASCLKDIV: E011\_0618H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved						USIAS1SCLK_PLLSEL	
23	22	21	20	19	18	17	16
USIAS1SCLK_DIV							
15	14	13	12	11	10	9	8
Reserved						USIAS0SCLK_PLLSEL	
7	6	5	4	3	2	1	0
USIAS0SCLK_DIV							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:26	–	Reserved. If these bits are read, 0 is returned for each bit.
USIAS1SCLK_PLLSEL	R/W	25:24	0H	Specify the source of USIA_S1_SCLK. 0H: PLL3 1H: PLL1 2H: OSC0 3H: EXT_CLKI
USIAS1SCLK_DIV	R/W	23:16	0FH	Specify the division factor for USIA_S1_SCLK. Division factor = specified value + 1 It's set as 60.2MHz >= USIA_S1_SCLK.
Reserved	R	15:10	–	Reserved. If these bits are read, 0 is returned for each bit.
USIAS0SCLK_PLLSEL	R/W	9:8	0H	Specify the source of USIA_S0_SCLK. 0H: PLL3 1H: PLL1 2H: OSC0 3H: EXT_CLKI
USIAS0SCLK_DIV	R/W	7:0	0FH	Specify the division factor for USIA_S0_SCLK. Division factor = specified value + 1 It's set as 60.2MHz >= USIA_S0_SCLK.

When changing the settings of this register, make sure that the USIA\_S0\_SCLK/USIA\_S1\_SCLK output has stopped.

Use this register to select the source of USIA\_S0\_SCLK/USIA\_S1\_SCLK and specify the frequency division factor.

If this register is set to 000F\_000FH (PLL3 is selected as the clock source), the frequency is calculated as follows:

$$\text{USIA\_S0\_SCLK/USIA\_S1\_SCLK} = 229.376 \text{ (MHz)} / 16 = 14.336 \text{ MHz}$$

### 3.2.219 USIA\_U0\_SCLK frequency division setting register

This register (USIAU0SCLKDIV: E011\_061CH) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved						USIAU0SCLK_PLLSEL	
7	6	5	4	3	2	1	0
USIAU0SCLK_DIV							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:10	–	Reserved. If these bits are read, 0 is returned for each bit.
USIAU0SCLK_PLLSEL	R/W	9:8	0H	Specify the source of USIA_U0_SCLK. 0H: PLL3 1H: PLL4 2H: PLL1 3H: OSC1
USIAU0SCLK_DIV	R/W	7:0	05H	Specify the division factor for USIA_U0_SCLK. Division factor = specified value + 1 It's set as 115MHz >= USIA_U0_SCLK

When changing the settings of this register, make sure that the USIA\_U0\_SCLK output has stopped.

Use this register to select the source of USIA\_U0\_SCLK and specify the frequency division factor.

If this register is set to 0000\_0005H (PLL3 is selected as the clock source), the frequency is calculated as follows:

$$\text{USIA\_U0\_SCLK} = 229.376 \text{ (MHz)} / 6 = 38.229 \text{ MHz}$$

### 3.2.220 IIC\_SCLK frequency division setting register

This register (IICSCLKDIV: E011\_0624H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved						IIC1SCLK_PLLSEL	
23	22	21	20	19	18	17	16
IIC1SCLK_DIV							
15	14	13	12	11	10	9	8
Reserved						IIC0SCLK_PLLSEL	
7	6	5	4	3	2	1	0
IIC0SCLK_DIV							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:26	–	Reserved. If these bits are read, 0 is returned for each bit.
IIC1SCLK_PLLSEL	R/W	25:24	0H	Specify the source of IIC1_SCLK. 0H: PLL3 1H: PLL4 2H: OSC0 3H: OSC1
IIC1SCLK_DIV	R/W	23:16	2FH	Specify the division factor for IIC1_SCLK. Division factor = specified value + 1 It's set as 9.2MHz >= IIC1_SCLK
Reserved	R	15:10	–	Reserved. If these bits are read, 0 is returned for each bit.
IIC0SCLK_PLLSEL	R/W	9:8	0H	Specify the source of IIC0_SCLK. 0H: PLL3 1H: PLL4 2H: OSC0 3H: OSC1
IIC0SCLK_DIV	R/W	7:0	2FH	Specify the division factor for IIC0_SCLK. Division factor = specified value + 1 It's set as 9.2MHz >= IIC0_SCLK

When changing the settings of this register, make sure that the IIC1\_SCLK/IIC0\_SCLK output has stopped.

Use this register to select the source of IIC1\_SCLK/IIC0\_SCLK and specify the frequency division factor.

If this register is set to 002F\_002FH (PLL3 is selected as the clock source), the frequency is calculated as follows:

$$\text{IIC1_SCLK/IIC0_SCLK} = 229.376 \text{ (MHz)} / 48 = 4.778 \text{ MHz}$$

### 3.2.221 USB\_SCLK frequency division setting register

This register (USBSCLKDIV: E011\_0628H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved						USBPCICLK_PLLSEL	
23	22	21	20	19	18	17	16
USBPCICLK_DIV							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:26	–	Reserved. If these bits are read, 0 is returned for each bit.
USBPCICLK_PLLSEL	R/W	25:24	0H	Specify the source of USB_PCICLK. 0H: PLL3 1H: PLL4 2H: OSC0 3H: OSC1
USBPCICLK_DIV	R/W	23:16	7H	Specify the division factor for USB_PCICLK. Division factor = specified value + 1 It's set as 33.3MHz >= USB_PCICLK
Reserved	R	15:0	–	Reserved. If these bits are read, 0 is returned for each bit.

When changing the settings of this register, make sure that the USB\_PCICLK output has stopped.

Use this register to select the source of USB\_PCICLK and specify the frequency division factor.

If this register is set to 0007\_0000H (PLL3 is selected as the clock source), the frequency is calculated as follows:

$$\text{USB\_PCICLK} = 229.376 \text{ (MHz)} / 8 = 28.672 \text{ MHz}$$

### 3.2.222 MEMC\_RCLK frequency division setting register

This register (MEMCRCLKDIV: E011\_062CH) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved						MEMCRCLK_PLLSEL	
7	6	5	4	3	2	1	0
MEMCRCLK_DIV							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:10	–	Reserved. If these bits are read, 0 is returned for each bit.
MEMCRCLK_PLLSEL	R/W	9:8	0H	Specify the source of MEMC_RCLK. 0H: PLL3 1H: PLL4 2H: OSC0 3H: OSC1
MEMCRCLK_DIV	R/W	7:0	0FH	Specify the division factor for MEMC_RCLK. Division factor = specified value + 1 It's set as 50MHz >= MEMC_RCLK

When changing the settings of this register, make sure that the MEMC\_RCLK output has stopped.

Use this register to select the source of MEMC\_RCLK and specify the frequency division factor.

If this register is set to 0000\_000FH (PLL3 is selected as the clock source), the frequency is calculated as follows:

$$\text{MEMC_RCLK} = 229.376 \text{ (MHz)} / 16 = 14.336 \text{ MHz}$$

### 3.2.223 LCD\_LCLK frequency division setting register

This register (LCDLCLKDIV: E011\_0630H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved						LCDLCLK_PLLSEL	
7	6	5	4	3	2	1	0
LCDLCLK_DIV							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:10	–	Reserved. If these bits are read, 0 is returned for each bit.			
LCDLCLK_PLLSEL	R/W	9:8	0H	Specify the source of LCD_LCLK. 0H: PLL3 1H: PLL4 2H: OSC0 3H: OSC1			
LCDLCLK_DIV	R/W	7:0	09H	Specify the division factor for LCD_LCLK. Division factor = specified value + 1 It's set as 100MHz >= LCD_LCLK			

When changing the settings of this register, make sure that the LCD\_LCLK output has stopped.

Use this register to select the source of LCD\_LCLK and specify the frequency division factor.

If this register is set to 0000\_0009H (PLL3 is selected as the clock source), the frequency is calculated as follows:

$$\text{LCD\_LCLK} = 229.376 \text{ (MHz)} / 10 = 22.937 \text{ MHz}$$

### 3.2.224 SDIO0\_SCLK frequency division setting register

This register (SDIO0SCLKDIV: E011\_0648H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved						SDIO0SCLK_PLLSEL	
7	6	5	4	3	2	1	0
SDIO0SCLK_DIV							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:10	–	Reserved. If these bits are read, 0 is returned for each bit.			
SDIO0SCLK_PLLSEL	R/W	9:8	0H	Specify the source of SDIO0_SCLK. 0H: PLL3 1H: PLL4 2H: OSC0 3H: OSC1			
SDIO0SCLK_DIV	R/W	7:0	05H	Specify the division factor for SDIO0_SCLK. Division factor = specified value + 1			

When changing the settings of this register, make sure that the SDIO0\_SCLK output has stopped.

Use this register to select the source of SDIO0\_SCLK and specify the frequency division factor.

If this register is set to 0000\_0005H (PLL3 is selected as the clock source), the frequency is calculated as follows:

$$\text{SDIO0_SCLK} = 229.376(\text{MHz}) / 6 = 38.229 \text{ MHz}$$

### 3.2.225 SDIO1\_SCLK frequency division setting register

This register (SDIO1SCLKDIV: E011\_064CH) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved							SDIO1SCLK_PLLSEL	
7	6	5	4	3	2	1	0	
SDIO1SCLK_DIV								
Name	R/W	Bit No.	After Reset	Description				
Reserved	R	31:10	–	Reserved. If these bits are read, 0 is returned for each bit.				
SDIO1SCLK_PLLSEL	R/W	9:8	0H	Specify the source of SDIO1_SCLK. 0H: PLL3 1H: PLL4 2H: OSC0 3H: OSC1				
SDIO1SCLK_DIV	R/W	7:0	05H	Specify the division factor for SDIO1_SCLK. Division factor = specified value + 1				

When changing the settings of this register, make sure that the SDIO1\_SCLK output has stopped.

Use this register to select the source of SDIO1\_SCLK and specify the frequency division factor.

If this register is set to 0000\_0005H (PLL3 is selected as the clock source), the frequency is calculated as follows:

$$\text{SDIO1_SCLK} = 229.376 \text{ (MHz)} / 6 = 38.229 \text{ MHz}$$

### 3.2.226 SDIO2\_SCLK frequency division setting register

This register (SDIO2SCLKDIV: E011\_0650H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved						SDIO2SCLK_PLLSEL	
7	6	5	4	3	2	1	0
SDIO2SCLK_DIV							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:10	–	Reserved. If these bits are read, 0 is returned for each bit.			
SDIO2SCLK_PLLSEL	R/W	9:8	0H	Specify the source of SDIO2_SCLK. 0H: PLL3 1H: PLL4 2H: OSC0 3H: OSC1			
SDIO2SCLK_DIV	R/W	7:0	05H	Specify the division factor for SDIO2_SCLK. Division factor = specified value + 1			

When changing the settings of this register, make sure that the SDIO2\_SCLK output has stopped.

Use this register to select the source of SDIO2\_SCLK and specify the frequency division factor.

If this register is set to 0000\_0005H (PLL3 is selected as the clock source), the frequency is calculated as follows:

$$\text{SDIO2_SCLK} = 229.376 \text{ (MHz)} / 6 = 38.229 \text{ MHz}$$

### 3.2.227 USIB0\_SCLK frequency division setting register

This register (USIB0SCLKDIV: E011\_0654H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved						USIBS3SCLK_PLLSEL	
23	22	21	20	19	18	17	16
USIBS3SCLK_DIV							
15	14	13	12	11	10	9	8
Reserved						USIBS2SCLK_PLLSEL	
7	6	5	4	3	2	1	0
USIBS2SCLK_DIV							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:26	–	Reserved. If these bits are read, 0 is returned for each bit.
USIBS3SCLK_PLLSEL	R/W	25:24	0H	Specify the source of USIB_S3_SCLK. 0H: PLL3 1H: PLL1 2H: OSC0 3H: EXT_CLKI
USIBS3SCLK_DIV	R/W	23:16	0FH	Specify the division factor for USIB_S3_SCLK. Division factor = specified value + 1 It's set as 60.2MHz >= USIB_S3_SCLK
Reserved	R	15:10	–	Reserved. If these bits are read, 0 is returned for each bit.
USIBS2SCLK_PLLSEL	R/W	9:8	0H	Specify the source of USIB_S2_SCLK. 0H: PLL3 1H: PLL1 2H: OSC0 3H: EXT_CLKI
USIBS2SCLK_DIV	R/W	7:0	0FH	Specify the division factor for USIB_S2_SCLK. Division factor = specified value + 1 It's set as 60.2MHz >= USIB_S2_SCLK

When changing the settings of this register, make sure that the USIB\_S3\_SCLK/USIB\_S2\_SCLK output has stopped.

Use this register to select the source of USIB\_S3\_SCLK/USIB\_S2\_SCLK and specify the frequency division factor.

If this register is set to 000F\_000FH (PLL3 is selected as the clock source), the frequency is calculated as follows:

$$\text{USIB\_S3\_SCLK/USIB\_S2\_SCLK} = 229.376 \text{ (MHz)} / 16 = 14.336 \text{ MHz}$$

### 3.2.228 USIB1\_SCLK frequency division setting register

This register (USIB1SCLKDIV: E011\_0658H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved						USIBS5SCLK_PLLSEL	
23	22	21	20	19	18	17	16
USIBS5SCLK_DIV							
15	14	13	12	11	10	9	8
Reserved						USIBS4SCLK_PLLSEL	
7	6	5	4	3	2	1	0
USIBS4SCLK_DIV							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:26	–	Reserved. If these bits are read, 0 is returned for each bit.
USIBS5SCLK_PLLSEL	R/W	25:24	0H	Specify the source of USIB_S5_SCLK. 0H: PLL3 1H: PLL1 2H: OSC0 3H: EXT_CLKI
USIBS5SCLK_DIV	R/W	23:16	0FH	Specify the division factor for USIB_S5_SCLK. Division factor = specified value + 1 It's set as 60.2MHz >= USIB_S5_SCLK
Reserved	R	15:10	–	Reserved. If these bits are read, 0 is returned for each bit.
USIBS4SCLK_PLLSEL	R/W	9:8	H	Specify the source of USIB_S4_SCLK. 0H: PLL3 1H: PLL1 2H: OSC0 3H: EXT_CLKI
USIBS4SCLK_DIV	R/W	7:0	0FH	Specify the division factor for USIB_S4_SCLK. Division factor = specified value + 1 It's set as 60.2MHz >= USIB_S4_SCLK

When changing the settings of this register, make sure that the USIB\_S5\_SCLK/USIB\_S4\_SCLK output has stopped.

Use this register to select the source of USIB\_S5\_SCLK/USIB\_S4\_SCLK and specify the frequency division factor.

If this register is set to 000F\_000FH (PLL3 is selected as the clock source), the frequency is calculated as follows:

$$\text{USIB\_S5\_SCLK/USIB\_S4\_SCLK} = 229.376 \text{ (MHz)} / 16 = 14.336 \text{ MHz}$$

### 3.2.229 USIB2\_SCLK frequency division setting register

This register (USIB2SCLKDIV: E011\_065CH) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved						USIBU2SCLK_PLLSEL	
23	22	21	20	19	18	17	16
USIBU2SCLK_DIV							
15	14	13	12	11	10	9	8
Reserved						USIBU1SCLK_PLLSEL	
7	6	5	4	3	2	1	0
USIBU1SCLK_DIV							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:26	–	Reserved. If these bits are read, 0 is returned for each bit.
USIBU2SCLK_PLLSEL	R/W	25:24	0H	Specify the source of USIB_U2_SCLK. 0H: PLL3 1H: PLL4 2H: OSC0 3H: OSC1
USIBU2SCLK_DIV	R/W	23:16	05H	Specify the division factor for USIB_U2_SCLK. Division factor = specified value + 1 It's set as 115MHz >= USIB_U2_SCLK
Reserved	R	15:10	–	Reserved. If these bits are read, 0 is returned for each bit.
USIBU1SCLK_PLLSEL	R/W	9:8	0H	Specify the source of USIB_U1_SCLK. 0H: PLL3 1H: PLL4 2H: OSC0 3H: OSC1
USIBU1SCLK_DIV	R/W	7:0	05H	Specify the division factor for USIB_U1_SCLK. Division factor = specified value + 1 It's set as 115MHz >= USIB_U1_SCLK

When changing the settings of this register, make sure that the output of USIB\_U2\_SCLK/USIB\_U1\_SCLK has stopped.

Use this register to select the source of USIB\_U2\_SCLK/USIB\_U1\_SCLK and specify the frequency division factor.

If this register is set to 0005\_0005H (PLL3 is selected as the clock source), the frequency is calculated as follows:

$$\text{USIB\_U2\_SCLK/USIB\_U1\_SCLK} = 229.376 \text{ (MHz)} / 6 = 38.229 \text{ MHz}$$

### 3.2.230 USIB3\_SCLK frequency division setting register

This register (USIB3SCLKDIV: E011\_0660H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved						USIBU4SCLK_PLLSEL	
23	22	21	20	19	18	17	16
USIBU4SCLK_DIV							
15	14	13	12	11	10	9	8
Reserved						USIBU3SCLK_PLLSEL	
7	6	5	4	3	2	1	0
USIBU3SCLK_DIV							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:10	–	Reserved. If these bits are read, 0 is returned for each bit.
USIBU3SCLK_PLLSEL	R/W	9:8	0H	Specify the source of USIB_U3_SCLK. 0H: PLL3 1H: PLL4 2H: OSC0 3H: OSC1
USIBU3SCLK_DIV	R/W	7:0	05H	Specify the division factor for USIB_U3_SCLK. Division factor = specified value + 1 It's set as 115MHz >= USIB_U3_SCLK

When changing the settings of this register, make sure that the output of USIB\_U3\_SCLK has stopped.

Use this register to select the source of USIB\_U3\_SCLK and specify the frequency division factor.

If this register is set to 0000\_0005H (PLL3 is selected as the clock source), the frequency is calculated as follows:

$$\text{USIB\_U3\_SCLK} = 229.376 \text{ (MHz)} / 6 = 38.229 \text{ MHz}$$

### 3.2.231 PWM\_PWCLK frequency division setting register

This register (PWMPWCLKDIV: E011\_066CH) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved						PWMPWCLK1_PLLSEL	
23	22	21	20	19	18	17	16
PWMPWCLK1_DIV							
15	14	13	12	11	10	9	8
Reserved						PWMPWCLK0_PLLSEL	
7	6	5	4	3	2	1	0
PWMPWCLK0_DIV							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:26	–	Reserved. If these bits are read, 0 is returned for each bit.
PWMPWCLK1_PLLSEL	R/W	25:24	0H	Specify the source of PWM_PWCLK1. 0H: PLL3 1H: PLL4 2H: OSC0 3H: OSC1
PWMPWCLK1_DIV	R/W	23:16	13H	Specify the division factor for PWM_PWCLK1. Division factor = specified value + 1 It's set as 12.5MHz >= PWM_PWCLK1
Reserved	R	15:10	–	Reserved. If these bits are read, 0 is returned for each bit.
PWMPWCLK0_PLLSEL	R/W	9:8	0H	Specify the source of PWM_PWCLK0. 0H: PLL3 1H: PLL4 2H: OSC0 3H: OSC1
PWMPWCLK0_DIV	R/W	7:0	13H	Specify the division factor for PWM_PWCLK0. Division factor = specified value + 1 It's set as 12.5MHz >= PWM_PWCLK0

When changing the settings of this register, make sure that the output of PWM\_PWCLK1/PWM\_PWCLK0 has stopped.

Use this register to select the source of PWM\_PWCLK1/PWM\_PWCLK0 and specify the frequency division factor.

If this register is set to 0013\_0013H (PLL3 is selected as the clock source), the frequency is calculated as follows:

$$\text{PWM_PWCLK1/PWM_PWCLK0} = 229.376 \text{ (MHz)} / 20 = 11.469 \text{ MHz}$$

### 3.2.232 CAM\_SCLK frequency division setting register

This register (CAMSCLKDIV: E011\_0670H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved						CAMSCLK_PLLSEL	
7	6	5	4	3	2	1	0
CAMSCLK_DIV							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:10	–	Reserved. If these bits are read, 0 is returned for each bit.
CAMSCLK_PLLSEL	R/W	9:8	0H	Specify the source of CAM_SCLK. 0H: PLL3 1H: PLL4 2H: OSC0 3H: OSC1
CAMSCLK_DIV	R/W	7:0	19H	Specify the division factor for CAM_SCLK. Division factor = specified value + 1 It's set as 50MHz >= CAM_SCLK

When changing the settings of this register, make sure that the output of CAM\_SCLK has stopped.

Use this register to select the source of CAM\_SCLK and specify the frequency division factor.

If this register is set to 0000\_0019H (PLL3 is selected as the clock source), the frequency is calculated as follows:

$$\text{CAM_SCLK} = 229.376 \text{ (MHz)} / 26 = 8.822 \text{ MHz}$$

### 3.2.233 A3D\_CORE\_CLK frequency division setting register

This register (A3DCORECLKDIV: E011\_067CH) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							A3DCORECLK_PLLSEL
7	6	5	4	3	2	1	0
A3DCORECLK_DIV							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:10	–	Reserved. If these bits are read, 0 is returned for each bit.			
A3DCORECLK_PLLSEL	R/W	9:8	0H	Specify the source of A3D_CORE_CLK. 0H: FFB_DMCLK 1H: PLL4 2H: PLL1 3H: PLL2			
A3DCORECLK_DIV	R/W	7:0	00H	Specify the division factor for A3D_CORE_CLK. Division factor = specified value + 1 It's set as 200MHz >= A3D_CORE_CLK			

When changing the settings of this register, make sure that the output of A3D\_CORE\_CLK has stopped.

Use this register to select the source of A3D\_CORE\_CLK and specify the frequency division factor.

If this register is set to 0000\_0000H (FFB\_DMCLK is 200.000MHz (500MHz/2.5 division) and FFB\_DMCLK is selected as the clock source), the frequency is calculated as follows:

$$\text{A3D\_CORE\_CLK} = 200.000 \text{ (MHz)} / 1 = 200.000 \text{ MHz}$$

### 3.2.234 AVE\_CCLK frequency division setting register

This register (AVECCLKDIV: E011\_0680H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved						AVECCLK_PLLSEL	
7	6	5	4	3	2	1	0
AVECCLK_DIV							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:10	–	Reserved. If these bits are read, 0 is returned for each bit.
AVECCLK_PLLSEL	R/W	9:8	0H	Specify the source of AVE_CCLK. 0H: PLL3 1H: PLL4 2H: PLL1 3H: PLL2
AVECCLK_DIV	R/W	7:0	00H	Specify the division factor for AVE_CCLK. Division factor = specified value + 1 It's set as 267.4MHz >= AVE_CCLK

When changing the settings of this register, make sure that the output of AVE\_CCLK has stopped.

Use this register to select the source of AVE\_CCLK and specify the frequency division factor.

If this register is set to 0000\_0201H (PLL1 is selected as the clock source), the frequency is calculated as follows:

$$\text{AVE\_CCLK} = 532.80 \text{ (MHz)} / 2 = 266.4 \text{ MHz}$$

### 3.2.235 QR\_CLK frequency division setting register

This register (QRCLKDIV: E011\_0684H) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
QRCLK_DIV							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:8	–	Reserved. If these bits are read, 0 is returned for each bit.			
QRCLK_DIV	R/W	7:0	01H	Specify the division factor for CPU_DMCLK. Division factor = specified value + 1			

When changing the settings of this register, make sure that the output of QR\_CLK has stopped.

Use this register to select the source of QR\_CLK and specify the frequency division factor.

If this register is set to 0000\_0001H (The clock source is CPU\_DOMAINCLOCK only), the frequency is calculated as follows:

$$\text{QR\_CLK} = 532.80 \text{ (MHz)} / 2 = 266.4 \text{ MHz}$$

### 3.2.236 STI\_SCLK source select register

This register (STI\_CLKSEL: E011\_0688H) specifies the source of STI\_SCLK.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								
7	6	5	4	3	2	1	0	
Reserved								STI_CLKSEL
Name	R/W	Bit No.	After Reset	Description				
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.				
STI_CLKSEL	R/W	0	0	Specify the source of STI_SCLK. 0: 32.768 kHz 1: 32 kHz (32.768 kHz clock thinned out)				

### 3.2.237 REF\_CLKO frequency division setting register

This register (REFCLKDIV: E011\_068CH) sets up the clock supplied to each block.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved						REFCLK_PLLSEL	
7	6	5	4	3	2	1	0
REFCLK_DIV							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:10	–	Reserved. If these bits are read, 0 is returned for each bit.			
REFCLK_PLLSEL	R/W	9:8	0H	Specify the source of REF_CLKO. 0H: PLL3 1H: EXT_CLKI 2H: OSC0 3H: OSC1			
REFCLK_DIV	R/W	7:0	05H	Specify the division factor for REF_CLKO. Division factor = specified value + 1 It's set as 50MHz >= REF_CLKO			

When changing the settings of this register, make sure that the output of REF\_CLKO has stopped.

Use this register to select the source of REF\_CLKO and specify the frequency division factor.

If this register is set to 0000\_0005H (PLL3 is selected as the clock source), the frequency is calculated as follows:

$$\text{REF\_CLKO} = 229.376 \text{ (MHz)} / 6 = 38.229 \text{ MHz}$$

### 3.2.238 TW4\_TIN setting register

This register (TI4TIN\_SEL: E011\_0698H) specifies the clock source for TW4.

31	30	29	28	27	26	25	24		
Reserved									
23	22	21	20	19	18	17	16		
Reserved									
15	14	13	12	11	10	9	8		
Reserved									
7	6	5	4	3	2	1	0		
Reserved						TW4TIN_SEL			
Name	R/W	Bit No.	After Reset	Description					
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.					
TW4TIN_SEL	R/W	1:0	1H	Specify the clock source for TW4. 0H: PLL3 division (division factor is specified by TIMCLK_DIV) 1H: 32.768 kHz 2H: 32 kHz (32.768 kHz clock thinned out) 3H: Setting prohibited					

### 3.2.239 INTA\_TCLK frequency division setting register

This register (INTA\_CLKSEL: C011\_069CH) specifies the source of INTA\_TCLK.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							
INTA_CLKSEL							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
INTA_CLKSEL	R/W	0	0	Specify the source of INTA_TCLK. 0: 32.768 kHz 1: 32 kHz (32.768 kHz clock thinned out)			

### 3.2.240 32.768 kHz clock status register

This register (CLK32\_STATUS: E011\_06E0H) indicates the status of external clock input pin CLK32.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							
CK32KI							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
CK32KI	R	0	0	Indicates the status of external clock (32.768 kHz) input pin C32K.			

### 3.2.241 Clock stop instruction signal status register

This register (CLKSTOPSIG\_ST: E011\_06F0H) indicates the status of the clock stop instruction signals.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved				PWSTATE[6:0]			
7	6	5	4	3	2	1	0
Reserved						ALLSTANDBY	
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:15	–	Reserved.			
PWSTATE[7:0]	R	14:8	00H	Indicates the status of the CPU power. 0: Off 1: On PWSTATE0: Indicates the status of the PD_HM power. PWSTATE1: Indicates the status of the PD_DS0 power. PWSTATE2: Indicates the status of the PD_PE0 power. PWSTATE3: Indicates the status of the PD_NE0 power. PWSTATE4: Indicates the status of the PD_DS1 power. PWSTATE5: Indicates the status of the PD_PE1 power. PWSTATE6: Indicates the status of the PD_NE1 power.			
Reserved	R	7:1	–	Reserved.			
ALLSTANDBY	R	0	0	Indicates the ALLSTANDBY of CPU input status.			

### 3.2.242 Automatic frequency switch control REQMASK0 register

This register (CKRQMODE\_MASK0: E011\_0700H) specifies whether to switch the clock for each block automatically.

This register establishes judgment of whether a domain clock is returned at high speed by each macro operating state. When the macro set as “0” operated, a domain clock is returned at high speed from low speed. When the macro set as “1” operated, a domain clock doesn't change while being low-speed.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
CAM_REQ MASK	NTS_REQ MASK	DTV_REQ MASK	A3D_REQ MASK	AVE_REQ MASK	Reserved	ROT_REQ MASK	SIZ_REQ MASK
7	6	5	4	3	2	1	0
IMCW_REQ MASK	IMC_REQ MASK	LCD_REQ MASK	M2M_REQ MASK	M2P_REQ MASK	P2M_REQ MASK	Reserved	CPU_REQ MASK

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:17	–	Reserved. If these bits are read, 0 is returned for each bit.
Reserved	R/W	16	0	Reserved. The recommendation set value is 1
CAM_REQMASK	R/W	15	0	It's established whether you make operation of CAM module the judgment target of frequency control.
NTS_REQMASK	R/W	14	0	It's established whether you make operation of NTS module the judgment target of frequency control.
DTV_REQMASK	R/W	13	0	It's established whether you make operation of DTV module the judgment target of frequency control.
A3D_REQMASK	R/W	12	0	It's established whether you make operation of A3D module the judgment target of frequency control.
AVE_REQMASK	R/W	11	0	It's established whether you make operation of AVE module the judgment target of frequency control.
Reserved	R/W	10	0	Reserved. The recommendation set value is 1
ROT_REQMASK	R/W	9	0	It's established whether you make operation of ROT module the judgment target of frequency control.
SIZ_REQMASK	R/W	8	0	It's established whether you make operation of SIZ module the judgment target of frequency control.
IMCW_REQMASK	R/W	7	0	It's established whether you make operation of IMCW module the judgment target of frequency control.
IMC_REQMASK	R/W	6	0	It's established whether you make operation of IMC module the judgment target of frequency control.

(2/2)

Name	R/W	Bit No.	After Reset	Description
LCD_REQMASK	R/W	5	0	It's established whether you make operation of LCD module the judgment target of frequency control.
M2M_REQMASK	R/W	4	0	It's established whether you make operation of M2M the judgment target of frequency control.
M2P_REQMASK	R/W	3	0	It's established whether you make operation of M2P the judgment target of frequency control.
P2M_REQMASK	R/W	2	0	It's established whether you make operation of P2M the judgment target of frequency control.
Reserved	R/W	1	0	Reserved. The recommendation set value is 1
CPU_REQMASK	R/W	0	0	It's established whether you make operation of CPU module the judgment target of frequency control.

**Remark** 0: Applicable, 1: Non-applicable (setting ignored)

### 3.2.243 Automatic frequency switch control REQMASK1 register

This register (CKRQMODE\_MASK1: E011\_0704H) specifies whether to switch the clock for each block automatically.

This register establishes judgment of whether a domain clock is returned at high speed by each macro operating state. When the macro set as “0” operated, a domain clock is returned at high speed from low speed. When the macro set as “1” operated, a domain clock doesn't change while being low-speed.

31	30	29	28	27	26	25	24
Reserved			USB1_REQ MASK	USB0_REQ MASK	IIC1_REQ MASK	IIC0_REQ MASK	
23	22	21	20	19	18	17	16
Reserved	PWM_REQ MASK	Reserved	AB_REQ MASK	ROM_REQ MASK	Reserved	CFI_REQ MASK	Reserved
15	14	13	12	11	10	9	8
SDC_REQ MASK	SDIO2_REQ MASK	SDIO1_REQ MASK	SDIO0_REQ MASK	Reserved	USIB_U3_ REQMASK	USIB_U2_ REQMASK	USIB_U1_ REQMASK
7	6	5	4	3	2	1	0
USIB_S5_ REQMASK	USIB_S4_ REQMASK	USIB_S3_ REQMASK	USIB_S2_ REQMASK	Reserved	USIA_U0_ REQMASK	USIA_S1_ REQMASK	USIA_S0_ REQMASK

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31	–	Reserved. If this bit is read, 0 is returned.
Reserved	R/W	30:28	111B	Reserved.
USB1_REQMASK	R/W	27	1	It's established whether you make operation of USB1 module the judgment target of frequency control.
USB0_REQMASK	R/W	26	1	It's established whether you make operation of USB0 module the judgment target of frequency control.
IIC1_REQMASK	R/W	25	1	It's established whether you make operation of IIC1 module the judgment target of frequency control.
IIC0_REQMASK	R/W	24	1	It's established whether you make operation of IIC0 module the judgment target of frequency control.
Reserved	R/W	23	–	Reserved.
PWM_REQMASK	R/W	22	1	It's established whether you make operation of PWM module the judgment target of frequency control.
Reserved	R/W	21	1	Reserved.
AB_REQMASK	R/W	20	1	It's established whether you make operation of AB_BUS the judgment target of frequency control.
ROM_REQMASK	R/W	19	1	It's established whether you make operation of ROM the judgment target of frequency control.
Reserved	R/W	18	1	Reserved.

(2/2)

Name	R/W	Bit No.	After Reset	Description
CFI_REQMASK	R/W	17	1	It's established whether you make operation of CFI module the judgment target of frequency control.
Reserved	R	16	–	Reserved. If this bit is read, 0 is returned.
SDC_REQMASK	R/W	15	1	It's established whether you make operation of SDC module the judgment target of frequency control.
SDIO2_REQMASK	R/W	14	1	It's established whether you make operation of SDIO2 module the judgment target of frequency control.
SDIO1_REQMASK	R/W	13	1	It's established whether you make operation of SDIO1 module the judgment target of frequency control.
SDIO0_REQMASK	R/W	12	1	It's established whether you make operation of SDIO0 module the judgment target of frequency control.
Reserved	R/W	11	1	Reserved.
USIB_U3_REQMASK	R/W	10	1	It's established whether you make operation of USIB_U3 module the judgment target of frequency control.
USIB_U2_REQMASK	R/W	9	1	It's established whether you make operation of USIB_U2 module the judgment target of frequency control.
USIB_U1_REQMASK	R/W	8	1	It's established whether you make operation of USIB_U1 module the judgment target of frequency control.
USIB_S5_REQMASK	R/W	7	1	It's established whether you make operation of USIB_S5 module the judgment target of frequency control.
USIB_S4_REQMASK	R/W	6	1	It's established whether you make operation of USIB_S4 module the judgment target of frequency control.
USIB_S3_REQMASK	R/W	5	1	It's established whether you make operation of USIB_S3 module the judgment target of frequency control.
USIB_S2_REQMASK	R/W	4	1	It's established whether you make operation of USIB_S2 module the judgment target of frequency control.
Reserved	R/W	3	1	Reserved.
USIA_U0_REQMASK	R/W	2	1	It's established whether you make operation of USIA_U0 module the judgment target of frequency control.
USIA_S1_REQMASK	R/W	1	1	It's established whether you make operation of USIA_S1 module the judgment target of frequency control.
USIA_S0_REQMASK	R/W	0	1	It's established whether you make operation of USIA_S0 module the judgment target of frequency control.

**Remark** 0: Applicable, 1: Non-applicable (setting ignored)

### 3.2.244 Automatic frequency switch control register

This register (CKRQ\_MODE: E011\_0708H) specifies the division factor for the PLL1 clock when the frequency is lowered.

31	30	29	28	27	26	25	24
CKRQMODE_DIV_RATE				Reserved			
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
CKRQMODE_TIM							
7	6	5	4	3	2	1	0
Reserved				CKRQMODE_T IMEN		CKRQ_MODE _EN	

(1/2)

Name	R/W	Bit No.	After Reset	Description
CKRQMODE_DIV_RATE	R/W	31:28	FH	Frequency dividing rate of PLL1 clock at the time of frequency DOWN is established. 0H: Setting prohibited 1H: 2 division 2H: 3 division 3H: 4 division 4H: 5 division 5H: 6 division 6H: Setting prohibited. 7H: 8 division 9H: 10 division AH: Setting prohibited. BH: 12 division CH: Setting prohibited. DH: 14 division EH: Setting prohibited. FH: 16 division
Reserved	R	27:16	–	Reserved. If these bits are read, 0 is returned for each bit.
CKRQMODE_TIM	R/W	15:8	00H	Specify the timer value for suppressing transition to low-frequency mode. 00H: 61 $\mu$ s 01H: 92 $\mu$ s ... FFH: 7843 $\mu$ s

(2/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	7:2	–	Reserved. If these bits are read, 0 is returned for each bit.
CKRQMODE_TIMEN	R/W	1	0	<p>Specify whether to enable the timer for suppressing transition to low-frequency mode.</p> <p>0: Disable 1: Enable</p> <p>Low-frequency mode is entered after the count value (number of 32.768 kHz clock cycles) set by the CKRQMODE_TIM bit has elapsed.</p> <p>Transition to low-frequency mode is cancelled if a request for increase the frequency is received during the transition wait period.</p>
CKRQ_MODE_EN	R/W	0	0	<p>Specify whether to enable automatic frequency switching.</p> <p>0: Disable 1: Enable</p>

**Remarks 1.** When no clock requests are sent from any macro in which automatic frequency change is enabled in the CKRQ\_MODE register while normal mode A, B, C, or D is specified in the CLK\_MODE\_SEL register, the AUTO\_DMDIVCNG\_EN bit of the AUTO\_DMDIVCNG\_MODE register is set to 1 (Automatic frequency control domain clock division switching enabled), and the CKRQ\_MODE\_EN bit of the CKRQ\_MODE register is set to 1 (automatic frequency switching enabled), the SMU switches the domain clock frequency according to the division factor specified by the AUTO\_DMDIVCNG\_PARAM [27:0] division rates.

When it's AUTO\_DMDIVCNG\_MODE[0] = 0x0, the source clock of a domain clock (PLL) is changed with frequency dividing rate of CKRQMODE\_DIV\_RATE [3:0].

2. The SMU restores the original domain clock frequency if at least one of the macros to which automatic frequency change is enabled sends a clock request while changing to low-frequency mode, or if a burst read request is sent from the AB0 macro.
3. If the division factor is changed while changing to low-frequency mode, the new factor takes effect when low-frequency mode is entered next time.
4. In economy, standby, sleep, or deep sleep mode (power save mode), disable automatic frequency change (CKRQ\_MODE\_EN = 0).
5. When it's a domain source clock division mode, "1" is set as 4th bit of SMU\_CONTROL (0xE011\_100C).

When it's a domain clock division change mode, 4th bit of SMU\_CONTROL (0xE011\_100C) is established with the following table.

Auto frequency control	Register setting		
Control mode	CKRQ_MODE[0]	AUTO_DMDIVCNG_MODE[0]	SMU_CONTROL[4]
Domain source clock division	1	0	1
Domain clock division switching	1	1	Change is unnecessary

Figure 3-13. Automatic frequency control on setting procedure

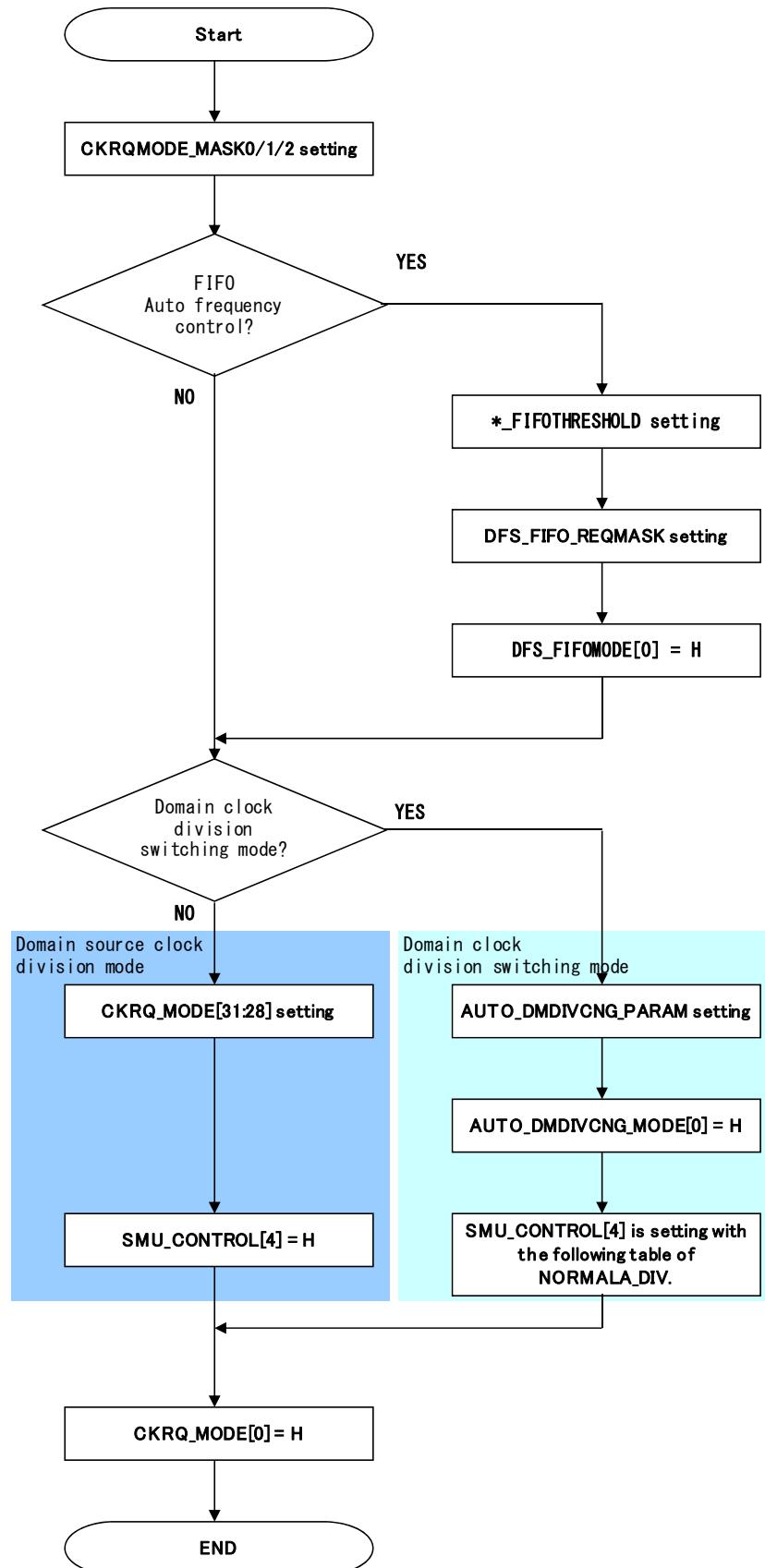
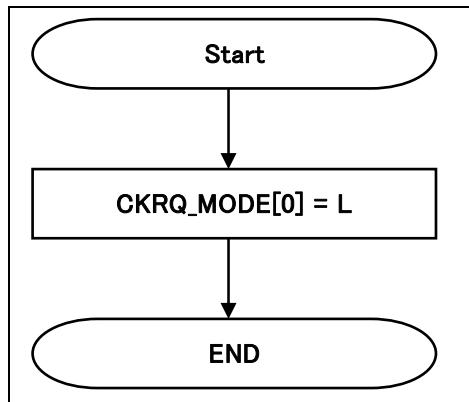


Figure 3-14. Automatic frequency control off setting procedure



### 3.2.245 Automatic frequency control FIFO space mode register

This register (DFS\_FIFOMODE: E011\_0710H) specifies whether to enable the DFS\_FIFO mode due to automatic frequency change.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								
7	6	5	4	3	2	1	0	
Reserved								DFS_FIFOMO DE_EN

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
DFS_FIFOMODE_EN	R/W	0	0	Specify whether to enable the DFS_FIFO mode. 0: Disable 1: Enable

If normal mode A, B, C, or D is specified by using the CLK\_MODE\_SEL register, the CKRQ\_MODE\_EN bit of the CKRQ\_MODE register is set to 1 (automatic frequency switching enabled), the AUTO\_DMDIVCNG\_EN bit of the AUTO\_DMDIVCNG\_MODE register is set to 1 (Automatic frequency control domain clock division switching enabled), and the DFS\_FIFOMODE\_EN bit of the DFS\_FIFOMODE register is set to 1 (transition to DFS\_FIFO mode enabled), the frequency is automatically changed according to the amount of space remaining in the FIFO of a macro for which judgment based on the FIFO amount is enabled in the DFS\_FIFO\_REQMASK register. To use this function, judgment for the relevant macro must be masked by using the CKRQMODE\_MASK register.

If LCDFIFO\_REQMASK is enabled, for example, the frequency is lowered when the amount of data in the FIFO of the LCD controller exceeds the value specified by the LCDFIFO\_UPPER\_TH bits of the LCD\_FIFOTHRESHOLD register, and the frequency is raised when the the amount of data falls below the value specified by these bits.

If CAMFIFO\_REQMASK is enabled, for example, the frequency is raised when the amount of data in the FIFO of the CAM controller exceeds the value specified by the CAMFIFO\_UPPER\_TH bits of the CAM\_FIFOTHRESHOLD register, and the frequency is lowered when the the amount of data falls below the value specified by these bits.

The CAM use is made the division setting which satisfies the following.

HFBDOMAIN frequency (After division of automatic frequency control) > CAM input frequency × 0.75  
When invalidating a FIFO mode, it's necessary to set it as DFS\_FIFOMODE (0xE011\_0710) = 0,

DFS\_FIFO\_REQMASK (0xE011\_0714) = 0x7.

### 3.2.246 Automatic frequency switch control register

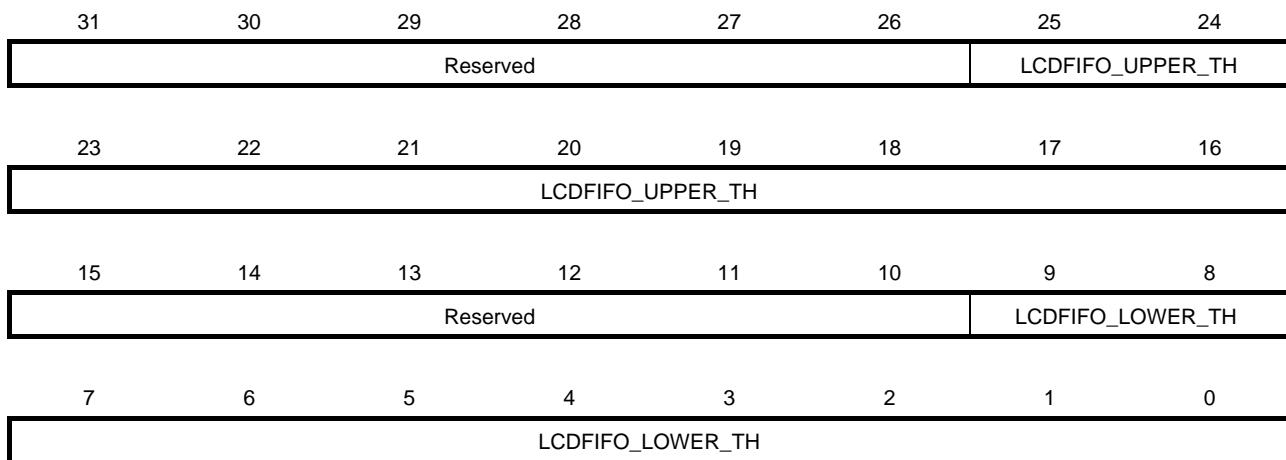
This register (DFS\_FIFO\_REQMASK: E011\_0714H) specifies whether to enable judgment for automatic frequency change based on the amount of space remaining in the FIFO in each module.

31	30	29	28	27	26	25	24	Reserved		
23	22	21	20	19	18	17	16	Reserved		
15	14	13	12	11	10	9	8	Reserved		
7	6	5	4	3	2	1	0	Reserved	CAMFIFO_REQMASK	LCDFIFO_REQMASK
Name	R/W	Bit No.	After Reset	Description						
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.						
CAMFIFO_REQMASK	R/W	1	1	Specify whether to enable judgment for automatic frequency change based on the amount of space remaining in the FIFO in the CAM module.						
LCDFIFO_REQMASK	R/W	0	1	Specify whether to enable judgment for automatic frequency change based on the amount of space remaining in the FIFO in the LCD controller.						

**Remark** 0: Enable, 1: Do not enable

### 3.2.247 Automatic frequency LCD\_FIFO threshold register

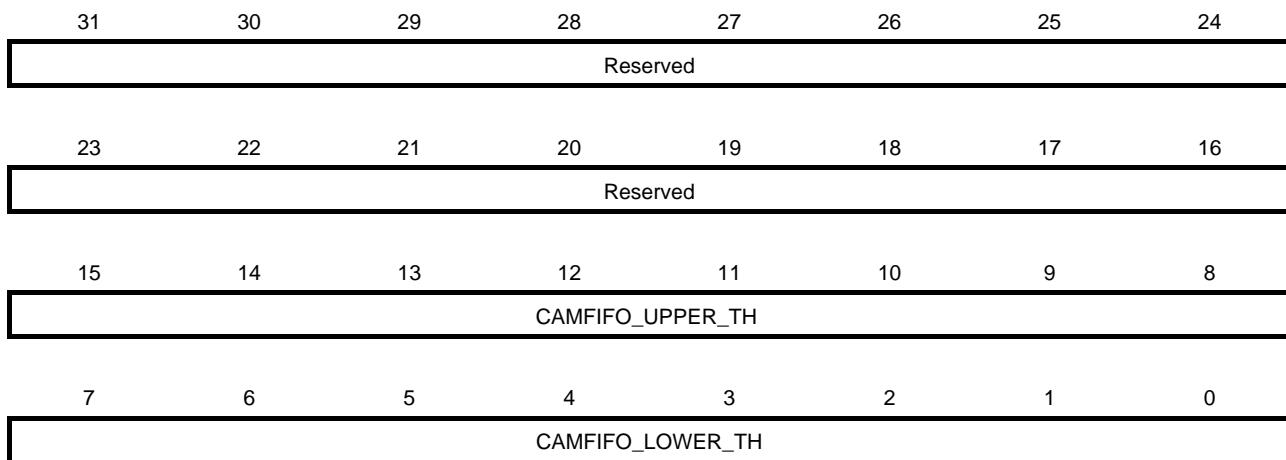
This register (LCD\_FIFOTHRESHOLD: E011\_0718H) specifies the threshold value for the amount of space remaining in the FIFO in the LCD controller.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:26	–	Reserved. If these bits are read, 0 is returned for each bit.
LCDFIFO_UPPER_TH	R/W	25:16	000H	Specify the upper limit of the space remaining in the FIFO in the LCD controller for shifting the frequency speed from high to low.
Reserved	R	15:10	–	Reserved. If these bits are read, 0 is returned for each bit.
LCDFIFO_LOWER_TH	R/W	9:0	000H	Specify the lower limit of the space remaining in the FIFO in the LCD controller for shifting the frequency speed from low to high.

### 3.2.248 Automatic frequency CAM\_FIFO threshold register

This register (CAM\_FIFOTHRESHOLD: E011\_071CH) specifies the threshold value for the amount of space remaining in the FIFO in the CAM module.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:16	–	Reserved. If these bits are read, 0 is returned for each bit.
CAMFIFO_UPPER_TH	R/W	15:8	00H	Specify the upper limit of the space remaining in the FIFO in the CAM module for shifting the frequency speed from low to high.
CAMFIFO_LOWER_TH	R/W	7:0	00H	Specify the lower limit of the space remaining in the FIFO in the CAM module for shifting the frequency speed from high to low.

### 3.2.249 Automatic frequency control domain clock division switch mode register

This register (AUTO\_DMDIVCNG\_MODE: E011\_0730H) specifies the frequency status which is at the time of automatic frequency control domain clock division switch mode use.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								
7	6	5	4	3	2	1	0	
Reserved								

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:17	–	Reserved. If these bits are read, 0 is returned for each bit.
AUTO_DMDIVCNG_STAT	R	16	0	Specify the frequency status which is at the time of automatic frequency control domain clock division switch mode use 0: Normal frequency 1: Low frequency
Reserved	R	15:1	–	Reserved. If these bits are read, 0 is returned for each bit.
AUTO_DMDIVCNG_EN	R/W	0	0	Specify Automatic frequency control domain clock division switch mode 0: Disable 1: Enable The recommendation value : 1

Note : There is a possibility that it's switched for the recommendation value.

### 3.2.250 Automatic frequency control domain clock division switch parameter register

This register (AUTO\_DMDIVCNG\_PARAM: E011\_0734H) specifies the division factor for the Automatic frequency control domain clock .

31	30	29	28	27	26	25	24	
Reserved					QFBDOMAIN_DIV_ADC			
23	22	21	20	19	18	17	16	
HFBDOMAIN_DIV_ADC					FFBDOMAIN_DIV_ADC			
15	14	13	12	11	10	9	8	
FLASHDOMAIN_DIV_ADC					MEMCDOMAIN_DIV_ADC			
7	6	5	4	3	2	1	0	
Reserved					CPUDOMAIN_DIV_ADC			
Name	R/W	Bit No.	After Reset	Description				
Reserved	R	31:28	–	Reserved. If these bits are read, 0 is returned for each bit.				
QFBDOMAIN_DIV_ADC	R/W	27:24	5H	Specify the division factor for the QFB domain clock. The recommendation value : 7H				
HFBDOMAIN_DIV_ADC	R/W	23:20	3H	Specify the division factor for the HFB domain clock. The recommendation value : 7H				
FFBDOMAIN_DIV_ADC	R/W	19:16	1H	Specify the division factor for the FFB domain clock. The recommendation value : 7H				
FLASHDOMAIN_DIV_ADC	R/W	15:12	5H	Specify the division factor for the FLASH domain clock. The recommendation value : 7H				
MEMCDOMAIN_DIV_ADC	R/W	11:8	1H	Specify the division factor for the MEMC domain clock. The recommendation value : 1H				
Reserved	R/W	7:4	0H	Reserved. The recommendation value : 7H				
CPUDOMAIN_DIV_ADC	R/W	3:0	0H	Specify the division factor for the CPU domain clock. The recommendation value : 1H				

- Remark**
- xxxxDOMAIN\_DIV\_ADC = 0H: Undivided
  - xxxxDOMAIN\_DIV\_ADC = 1H: Divided by 2
  - xxxxDOMAIN\_DIV\_ADC = 2H: Divided by 3
  - xxxxDOMAIN\_DIV\_ADC = 3H: Divided by 4
  - xxxxDOMAIN\_DIV\_ADC = 4H: Divided by 6
  - xxxxDOMAIN\_DIV\_ADC = 5H: Divided by 8
  - xxxxDOMAIN\_DIV\_ADC = 6H: Divided by 12
  - xxxxDOMAIN\_DIV\_ADC = 7H: Divided by 16
  - xxxxDOMAIN\_DIV\_ADC = 8H: Divided by 1.5
  - xxxxDOMAIN\_DIV\_ADC = 9H: Divided by 2.5
  - xxxxDOMAIN\_DIV\_ADC = AH: Divided by 5
  - xxxxDOMAIN\_DIV\_ADC = BH: Divided by 10
  - xxxxDOMAIN\_DIV\_ADC = CH to FH: Setting prohibited

**Note : There is a possibility that it's switched for the recommendation value.**

The value set as MEMCDOMAIN\_DIV\_ADC is set as the value with which a frequency of MEMC\_CLK doesn't change. (The frequency of MEMC\_CLK can't be changed.)

It's established so that a frequency of a divided domain clock may meet the following condition.

$$\text{CPU} \geq \text{MEMC} \geq \text{FFB}, \text{QFB} \geq \text{HFB}, \text{FLA}$$

It's established as each item domain clock frequency will be a integral multiple.

### 3.2.251 General-purpose register 0

This register (GENERAL\_REG0: E011\_07C0H) is the general-purpose register.

31	30	29	28	27	26	25	24
GENERAL_REG0							
23	22	21	20	19	18	17	16
GENERAL_REG0							
15	14	13	12	11	10	9	8
GENERAL_REG0							
7	6	5	4	3	2	1	0
GENERAL_REG0							
Name	R/W	Bit No.	After Reset	Description			
GENERAL_REG0	R/W	31:0	0000_0000H	General-purpose register			

### 3.2.252 General-purpose register 1

This register (GENERAL\_REG1: E011\_07C4H) is the general-purpose register.

31	30	29	28	27	26	25	24
GENERAL_REG1							
23	22	21	20	19	18	17	16
GENERAL_REG1							
15	14	13	12	11	10	9	8
GENERAL_REG1							
7	6	5	4	3	2	1	0
GENERAL_REG1							
Name	R/W	Bit No.	After Reset	Description			
GENERAL_REG1	R/W	31:0	0000_0000H	General-purpose register			

### 3.2.253 Power IC mode setting register

This register (LOWPWR: E011\_07F0H) specifies the power IC mode.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							LOWPWR

Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
LOWPWR	R/W	0	0	Specify the power IC mode. 0: Normal mode 1: Power save mode			

**Remark** Even if the LOWPWR bit is set to 1 (to enter the power save mode), the power IC enters normal mode when an interrupt (IRQ or FIQ) is issued for the CPU.

### 3.2.254 PLL power stabilization time setting register

This register (PLLVDDWAIT: E011\_07F4H) specifies the PLL power stabilization time.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								PLLVDDWAIT_TIME
7	6	5	4	3	2	1	0	
PLLVDDWAIT_TIME								
Name	R/W	Bit No.	After Reset	Description				
Reserved	R	31:9	–	Reserved. If these bits are read, 0 is returned for each bit.				
PLLVDDWAIT_TIME	R/W	8:0	000H	Specify the PLL power stabilization time. 000H: 45.776 to 76.293 $\mu$ s *1 001H: 45.776 to 76.293 $\mu$ s *1 002H: 45.776 to 76.293 $\mu$ s *1 003H: 91.545 $\mu$ s 004H: 122.062 $\mu$ s ... 1FFH: 15,594 $\mu$ s				

If the PLL power supply voltage in deep sleep mode is set to 0.7 V, use the PLLVDDWAIT\_TIME bits to specify the time from when the power IC transits from power-save mode to normal mode until PLL3 returns from standby (the voltage rise time).

\*1 : While it's 76.293  $\mu$ s at the most for 45.776  $\mu$ s at the least, PLL3\_STBY terminal isn't released because Neg – Pos - Pos synchronizes 3 steps of stand-by signal of PLL3 by 32.768kHz.

### 3.2.255 P0 power switch, R-FF/R-RAM control register

This register (P0\_POWERSW: E011\_0800H) sets up the power, retention F/F, and RAM in the P0 domain.

31	30	29	28	27	26	25	24
Reserved	P0_LAT	P0_BUN		Reserved	P0_RET	P0_RAMBUN	
23	22	21	20	19	18	17	16
Reserved				P0_PWSW1			
15	14	13	12	11	10	9	8
Reserved				P0_PWSW0			
7	6	5	4	3	2	1	0
Reserved				P0_RAMPD0			

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:30	–	Reserved. If these bits are read, 0 is returned for each bit.
P0_LAT	R/W	29	1	P0 domain LAT signal 0: Retain the status. 1: Do not retain the status.
P0_BUN	R/W	28	1	Specify whether to enable the ISO signal for the P0 domain. 0: Enable 1: Disable
Reserved	R	27:26	–	Reserved. If these bits are read, 0 is returned for each bit.
P0_RET	R/W	25	1	Specify the mode for the RET signal for retention F/F in the P0 domain. 0: Retention mode 1: Normal mode
P0_RAMBUN	R/W	24	1	Specify the mode for the BUN signal for RAM in the P0 domain. 0: Retention or power down mode 1: Normal mode
Reserved	R	23:21	–	Reserved. If these bits are read, 0 is returned for each bit.
P0_PWSW1	R/W	20:16	00H	Specify whether to turn on or off the power for logic circuits in the P0 domain. 0: On 1: Off
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
P0_PWSW0	R/W	12:8	00H	Specify whether to turn on or off the power for RAM in the P0 domain. 0: On 1: Off
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.

(2/2)

Name	R/W	Bit No.	After Reset	Description
P0_RAMPD0	R/W	4:0	00H	Specify the mode for the PD signal for RAM in the P0 domain. 0: Retention mode 1: Power down mode

Only when performing power control of P0 domain by a manual, this register uses.

It usually performs power control using P0 power supply automatic control register (0x0834).

### 3.2.256 PU power switch, R-FF/R-RAM control register

This register (PU\_POWERSW: E011\_0808H) sets up the power, retention F/F, and RAM in the PU domain.

31	30	29	28	27	26	25	24
Reserved		PU_LAT	PU_BUN	Reserved	PU_RET	PU_RAMBUN	
23	22	21	20	19	18	17	16
Reserved				PU_PWSW1			
15	14	13	12	11	10	9	8
Reserved				PU_PWSW0			
7	6	5	4	3	2	1	0
Reserved				PU_RAMPD0			

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:30	–	Reserved. If these bits are read, 0 is returned for each bit.
PU_LAT	R/W	29	1	PU domain LAT signal 0: Retain the status. 1: Do not retain the status.
PU_BUN	R/W	28	1	Specify whether to enable the ISO signal for the PU domain. 0: Enable 1: Disable
Reserved	R	27:26	–	Reserved. If these bits are read, 0 is returned for each bit.
PU_RET	R/W	25	1	Specify the mode for the RET signal for retention F/F in the PU domain. 0: Retention mode 1: Normal mode
PU_RAMBUN	R/W	24	1	Specify the mode for the BUN signal for RAM in the PU domain. 0: Retention or power down mode 1: Normal mode
Reserved	R	23:21	–	Reserved. If these bits are read, 0 is returned for each bit.
PU_PWSW1	R/W	20:16	00H	Specify whether to turn on or off the power for logic circuits in the PU domain. 0: On 1: Off
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
PU_PWSW0	R/W	12:8	00H	Specify whether to turn on or off the power for RAM in the PU domain. 0: On 1: Off
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.

(2/2)

Name	R/W	Bit No.	After Reset	Description
PU_RAMPD0	R/W	4:0	00H	Specify the mode for the PD signal for RAM in the PU domain. 0: Retention mode 1: Power down mode

Only when performing power control of PU domain by a manual, this register uses.

It usually performs power control using PU power supply automatic control register (0x083C).

### 3.2.257 PM power switch, R-FF/R-RAM control register

This register (PM\_POWERSW: E011\_080CH) sets up the power, retention F/F, and RAM in the PM domain.

31	30	29	28	27	26	25	24
Reserved	PM_LAT	PM_BUN		Reserved	PM_RET	PM_RAMBUN	
23	22	21	20	19	18	17	16
Reserved				PM_PWSW1			
15	14	13	12	11	10	9	8
Reserved				PM_PWSW0			
7	6	5	4	3	2	1	0
Reserved				PM_RAMPD0			

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:30	–	Reserved. If these bits are read, 0 is returned for each bit.
PM_LAT	R/W	29	1	PM domain LAT signal 0: Retain the status. 1: Do not retain the status.
PM_BUN	R/W	28	1	Specify whether to enable the ISO signal for the PM domain. 0: Enable 1: Disable
Reserved	R	27:26	–	Reserved. If these bits are read, 0 is returned for each bit.
PM_RET	R/W	25	1	Specify the mode for the RET signal for retention F/F in the PM domain. 0: Retention mode 1: Normal mode
PM_RAMBUN	R/W	24	1	Specify the mode for the BUN signal for RAM in the PM domain. 0: Retention or power down mode 1: Normal mode
Reserved	R	23:21	–	Reserved. If these bits are read, 0 is returned for each bit.
PM_PWSW1	R/W	20:16	00H	Specify whether to turn on or off the power for logic circuits in the PM domain. 0: On 1: Off
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
PM_PWSW0	R/W	12:8	00H	Specify whether to turn on or off the power for RAM in the PM domain. 0: On 1: Off
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.

(2/2)

Name	R/W	Bit No.	After Reset	Description
PM_RAMPD0	R/W	4:0	00H	Specify the mode for the PD signal for RAM in the PM domain. 0: Retention mode 1: Power down mode

Only when performing power control of PM domain by a manual, this register uses.

It usually performs power control using PM power supply automatic control register (0x0840).

### 3.2.258 PL power switch, R-FF/R-RAM control register

This register (PL\_POWERSW: E011\_0810H) sets up the power, retention F/F, and RAM in the PL domain.

31	30	29	28	27	26	25	24
Reserved		PL_LAT	PL_BUN	Reserved	PL_RET	PL_RAMBUN	
23	22	21	20	19	18	17	16
Reserved				PL_PWSW1			
15	14	13	12	11	10	9	8
Reserved				PL_PWSW0			
7	6	5	4	3	2	1	0
Reserved				PL_RAMPD0			

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:30	–	Reserved. If these bits are read, 0 is returned for each bit.
PL_LAT	R/W	29	1	PL domain LAT signal 0: Retain the status. 1: Do not retain the status.
PL_BUN	R/W	28	1	Specify whether to enable the ISO signal for the PL domain. 0: Enable 1: Disable
Reserved	R	27:26	–	Reserved. If these bits are read, 0 is returned for each bit.
PL_RET	R/W	25	1	Specify the mode for the RET signal for retention F/F in the PL domain. 0: Retention mode 1: Normal mode
PL_RAMBUN	R/W	24	1	Specify the mode for the BUN signal for RAM in the PL domain. 0: Retention or power down mode 1: Normal mode
Reserved	R	23:21	–	Reserved. If these bits are read, 0 is returned for each bit.
PL_PWSW1	R/W	20:16	00H	Specify whether to turn on or off the power for logic circuits in the PL domain. 0: On 1: Off
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
PL_PWSW0	R/W	12:8	00H	Specify whether to turn on or off the power for RAM in the PL domain. 0: On 1: Off
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.

(2/2)

Name	R/W	Bit No.	After Reset	Description
PL_RAMPD0	R/W	4:0	00H	Specify the mode for the PD signal for RAM in the PL domain. 0: Retention mode 1: Power down mode

Only when performing power control of PL domain by a manual, this register uses.

It usually performs power control using PL power supply automatic control register (0x0844).

### 3.2.259 P1 power switch, R-FF/R-RAM control register

This register (P1\_POWERSW: E011\_0818H) sets up the power, retention F/F, and RAM in the P1 domain.

31	30	29	28	27	26	25	24
Reserved	P1_LAT	P1_BUN		Reserved	P1_RET	P1_RAMBUN	
23	22	21	20	19	18	17	16
Reserved				P1_PWSW1			
15	14	13	12	11	10	9	8
Reserved				P1_PWSW0			
7	6	5	4	3	2	1	0
Reserved				P1_RAMPD0			

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:30	–	Reserved. If these bits are read, 0 is returned for each bit.
P1_LAT	R/W	29	1	P1 domain LAT signal 0: Retain the status. 1: Do not retain the status.
P1_BUN	R/W	28	1	Specify whether to enable the ISO signal for the P1 domain. 0: Enable 1: Disable
Reserved	R	27:26	–	Reserved. If these bits are read, 0 is returned for each bit.
P1_RET	R/W	25	1	Specify the mode for the RET signal for retention F/F in the P1 domain. 0: Retention mode 1: Normal mode
P1_RAMBUN	R/W	24	1	Specify the mode for the BUN signal for RAM in the P1 domain. 0: Retention or power down mode 1: Normal mode
Reserved	R	23:21	–	Reserved. If these bits are read, 0 is returned for each bit.
P1_PWSW1	R/W	20:16	00H	Specify whether to turn on or off the power for logic circuits in the P1 domain. 0: On 1: Off
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
P1_PWSW0	R/W	12:8	00H	Specify whether to turn on or off the power for RAM in the P1 domain. 0: On 1: Off
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.

(2/2)

Name	R/W	Bit No.	After Reset	Description
P1_RAMPD0	R/W	4:0	00H	Specify the mode for the PD signal for RAM in the P1 domain. 0: Retention mode 1: Power down mode

Only when performing power control of P1 domain by a manual, this register uses.

It usually performs power control using P1 power supply automatic control register (0x084C).

### 3.2.260 P2 power switch, R-FF/R-RAM control register

This register (P2\_POWERSW: E011\_081CH) sets up the power, retention F/F, and RAM in the P2 domain.

31	30	29	28	27	26	25	24
Reserved	P2_LAT	P2_BUN		Reserved	P2_RET	P2_RAMBUN	
23	22	21	20	19	18	17	16
Reserved				P2_PWSW1			
15	14	13	12	11	10	9	8
Reserved				P2_PWSW0			
7	6	5	4	3	2	1	0
Reserved				P2_RAMPD0			

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:30	–	Reserved. If these bits are read, 0 is returned for each bit.
P2_LAT	R/W	29	1	P2 domain LAT signal 0: Retain the status. 1: Do not retain the status.
P2_BUN	R/W	28	1	Specify whether to enable the ISO signal for the P2 domain. 0: Enable 1: Disable
Reserved	R	27:26	–	Reserved. If these bits are read, 0 is returned for each bit.
P2_RET	R/W	25	1	Specify the mode for the RET signal for retention F/F in the P2 domain. 0: Retention mode 1: Normal mode
P2_RAMBUN	R/W	24	1	Specify the mode for the BUN signal for RAM in the P2 domain. 0: Retention or power down mode 1: Normal mode
Reserved	R	23:21	–	Reserved. If these bits are read, 0 is returned for each bit.
P2_PWSW1	R/W	20:16	00H	Specify whether to turn on or off the power for logic circuits in the P2 domain. 0: On 1: Off
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
P2_PWSW0	R/W	12:8	00H	Specify whether to turn on or off the power for RAM in the P2 domain. 0: On 1: Off
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.

(2/2)

Name	R/W	Bit No.	After Reset	Description
P2_RAMPD0	R/W	4:0	00H	Specify the mode for the PD signal for RAM in the P2 domain. 0: Retention mode 1: Power down mode

Only when performing power control of P2 domain by a manual, this register uses.

It usually performs power control using P2 power supply automatic control register (0x0850).

### 3.2.261 PG power switch, R-FF/R-RAM control register

This register (PG\_POWERSW: E011\_0820H) sets up the power, retention F/F, and RAM in the PG domain.

31	30	29	28	27	26	25	24
Reserved	PG_LAT	PG_BUN		Reserved	PG_RET	PG_RAMBUN	
23	22	21	20	19	18	17	16
Reserved				PG_PWSW1			
15	14	13	12	11	10	9	8
Reserved				PG_PWSW0			
7	6	5	4	3	2	1	0
Reserved				PG_RAMPD0			

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:30	–	Reserved. If these bits are read, 0 is returned for each bit.
PG_LAT	R/W	29	1	PG domain LAT signal 0: Retain the status. 1: Do not retain the status.
PG_BUN	R/W	28	1	Specify whether to enable the ISO signal for the PG domain. 0: Enable 1: Disable
Reserved	R	27:26	–	Reserved. If these bits are read, 0 is returned for each bit.
PG_RET	R/W	25	1	Specify the mode for the RET signal for retention F/F in the PG domain. 0: Retention mode 1: Normal mode
PG_RAMBUN	R/W	24	1	Specify the mode for the BUN signal for RAM in the PG domain. 0: Retention or power down mode 1: Normal mode
Reserved	R	23:21	–	Reserved. If these bits are read, 0 is returned for each bit.
PG_PWSW1	R/W	20:16	00H	Specify whether to turn on or off the power for logic circuits in the PG domain. 0: On 1: Off
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
PG_PWSW0	R/W	12:8	00H	Specify whether to turn on or off the power for RAM in the PG domain. 0: On 1: Off
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.

(2/2)

Name	R/W	Bit No.	After Reset	Description
PG_RAMPD0	R/W	4:0	00H	Specify the mode for the PD signal for RAM in the PG domain. 0: Retention mode 1: Power down mode

Only when performing power control of PG domain by a manual, this register uses.

It usually performs power control using PG power supply automatic control register (0x0854).

### 3.2.262 PV power switch, R-FF/R-RAM control register

This register (PV\_POWERSW: E011\_0824H) sets up the power, retention F/F, and RAM in the PV domain.

31	30	29	28	27	26	25	24
Reserved	PV_LAT	PV_BUN		Reserved	PV_RET	PV_RAMBUN	
23	22	21	20	19	18	17	16
Reserved				PV_PWSW1			
15	14	13	12	11	10	9	8
Reserved				PV_PWSW0			
7	6	5	4	3	2	1	0
Reserved				PV_RAMPD0			

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:30	–	Reserved. If these bits are read, 0 is returned for each bit.
PV_LAT	R/W	29	1	PV domain LAT signal 0: Retain the status. 1: Do not retain the status.
PV_BUN	R/W	28	1	Specify whether to enable the ISO signal for the PV domain. 0: Enable 1: Disable
Reserved	R	27:26	–	Reserved. If these bits are read, 0 is returned for each bit.
PV_RET	R/W	25	1	Specify the mode for the RET signal for retention F/F in the PV domain. 0: Retention mode 1: Normal mode
PV_RAMBUN	R/W	24	1	Specify the mode for the BUN signal for RAM in the PV domain. 0: Retention or power down mode 1: Normal mode
Reserved	R	23:21	–	Reserved. If these bits are read, 0 is returned for each bit.
PV_PWSW1	R/W	20:16	00H	Specify whether to turn on or off the power for logic circuits in the PV domain. 0: On 1: Off
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
PV_PWSW0	R/W	12:8	00H	Specify whether to turn on or off the power for RAM in the PV domain. 0: On 1: Off
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.

(2/2)

Name	R/W	Bit No.	After Reset	Description
PV_RAMPD0	R/W	4:0	00H	Specify the mode for the PD signal for RAM in the PV domain. 0: Retention mode 1: Power down mode

Only when performing power control of PV domain by a manual, this register uses.

It usually performs power control using PV power supply automatic control register (0x0858).

### 3.2.263 PR power switch control register

This register (PR\_POWERSW: E011\_0828H) switches the power supplied to the PR domain.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								
7	6	5	4	3	2	1	0	
PR_PWSW1								

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:17	–	Reserved. If these bits are read, 0 is returned for each bit.
PR_BUN	R/W	16	1	Specify whether to enable the ISO signal for the PR domain. 0: Enable 1: Disable
Reserved	R	15:8	–	Reserved. If these bits are read, 0 is returned for each bit.
PR_PWSW1	R/W	7:0	00H	Specify whether to turn on or off the power for logic circuits in the PR domain. 0: On 1: Off

Only when performing power control of PR domain by a manual, this register uses.

It usually performs power control using PR power supply automatic control register (0x085C).

### 3.2.264 Power domain status monitor register

This register (POWER\_STATUS: E011\_082CH) indicates the status of the power in each domain.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved		PR_PWRSTATUS		PV_PWRSTATUS		PG_PWRSTATUS	
15	14	13	12	11	10	9	8
P2_PWRSTATUS		PU_PWRSTATUS		Reserved		P1_PWRSTATUS	
7	6	5	4	3	2	1	0
PL_PWRSTATUS		PM_PWRSTATUS		Reserved		P0_PWRSTATUS	

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:22	–	Reserved. If these bits are read, 0 is returned for each bit.
PR_PWRSTATUS	R	21: 20	0H	Indicates the status of the power in the PR domain. 0H: Normal mode 1H: Retention mode 2H: Power down mode
PV_PWRSTATUS	R	19:18	0H	Indicates the status of the power in the PV domain. 0H: Normal mode 1H: Retention mode 2H: Power down mode
PG_PWRSTATUS	R	17:16	0H	Indicates the status of the power in the PG domain. 0H: Normal mode 1H: Retention mode 2H: Power down mode
P2_PWRSTATUS	R	15:14	0H	Indicates the status of the power in the P2 domain. 0H: Normal mode 1H: Retention mode 2H: Power down mode
PU_PWRSTATUS	R	13:12	0H	Indicates the status of the power in the PU domain. 0H: Normal mode 1H: Retention mode 2H: Power down mode
Reserved	R	11:10	–	Reserved.
P1_PWRSTATUS	R	9:8	0H	Indicates the status of the power in the P1 domain. 0H: Normal mode 1H: Retention mode 2H: Power down mode

(2/2)

Name	R/W	Bit No.	After Reset	Description
PL_PWRSTATUS	R	7:6	0H	Indicates the status of the power in the PL domain. 0H: Normal mode 1H: Retention mode 2H: Power down mode
PM_PWRSTATUS	R	5:4	0H	Indicates the status of the power in the PM domain. 0H: Normal mode 1H: Retention mode 2H: Power down mode
Reserved	R	3:2	–	Reserved. If these bits are read, 0 is returned for each bit.
P0_PWRSTATUS	R	1:0	0H	Indicates the status of the power in the P0 domain. 0H: Normal mode 1H: Retention mode 2H: Power down mode

### 3.2.265 Power switch control sequencer status monitor register

This register (SEQ\_BUSY: E011\_0830H) shows the transition status of power switch control sequencer.

31	30	29	28	27	26	25	24
Reserved				PR_MODE_ACTIVE	PV_MODE_ACTIVE	PG_MODE_ACTIVE	
23	22	21	20	19	18	17	16
P2_MODE_ACTIVE	PU_MODE_ACTIVE	Reserved	P1_MODE_ACTIVE	PL_MODE_ACTIVE	PM_MODE_ACTIVE	Reserved	P0_MODE_ACTIVE
15	14	13	12	11	10	9	8
Reserved				PR_SEQ_BUSY	PV_SEQ_BUSY	PG_SEQ_BUSY	
7	6	5	4	3	2	1	0
P2_SEQ_BUSY	PU_SEQ_BUSY	Reserved	P1_SEQ_BUSY	PL_SEQ_BUSY	PM_SEQ_BUSY	Reserved	P0_SEQ_BUSY

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:27	–	Reserved. If these bits are read, 0 is returned for each bit.
PR_MODE_ACTIVE	R	26	0	Indicates the transition of the PR power control sequencer status. 0: Retention to Normal 1: Normal to Retention
PV_MODE_ACTIVE	R	25	0	Indicates the transition of the PV power control sequencer status. 0: Retention to Normal 1: Normal to Retention
PG_MODE_ACTIVE	R	24	0	Indicates the transition of the PG power control sequencer status. 0: Retention to Normal 1: Normal to Retention
P2_MODE_ACTIVE	R	23	0	Indicates the transition of the P2 power control sequencer status. 0: Retention to Normal 1: Normal to Retention
PU_MODE_ACTIVE	R	22	0	Indicates the transition of the PU power control sequencer status. 0: Retention to Normal 1: Normal to Retention
Reserved	R	21	–	Reserved.
P1_MODE_ACTIVE	R	20	0	Indicates the transition of the P1 power control sequencer status. 0: Retention to Normal 1: Normal to Retention

(2/2)

Name	R/W	Bit No.	After Reset	Description
PL_MODE_ACTIVE	R	19	0	Indicates the transition of the PL power control sequencer status. 0: Retention to Normal 1: Normal to Retention
PM_MODE_ACTIVE	R	18	0	Indicates the transition of the PM power control sequencer status. 0: Retention to Normal 1: Normal to Retention
Reserved	R	17	–	Reserved. If this bit is read, 0 is returned.
P0_MODE_ACTIVE	R	16	0	Indicates the transition of the P0 power control sequencer status. 0: Retention to Normal 1: Normal to Retention
Reserved	R	15:11	–	Reserved. If these bits are read, 0 is returned for each bit.
PR_SEQ_BUSY	R	10	0	Indicates the status of the PR power control sequencer. 0: Stopped 1: Running.
PV_SEQ_BUSY	R	9	0	Indicates the status of the PV power control sequencer. 0: Stopped 1: Running.
PG_SEQ_BUSY	R	8	0	Indicates the status of the PG power control sequencer. 0: Stopped 1: Running.
P2_SEQ_BUSY	R	7	0	Indicates the status of the P2 power control sequencer. 0: Stopped 1: Running.
PU_SEQ_BUSY	R	6	0	Indicates the status of the PU power control sequencer. 0: Stopped 1: Running.
Reserved	R	5	–	Reserved.
P1_SEQ_BUSY	R	4	0	Indicates the status of the P1 power control sequencer. 0: Stopped 1: Running.
PL_SEQ_BUSY	R	3	0	Indicates the status of the PL power control sequencer. 0: Stopped 1: Running.
PM_SEQ_BUSY	R	2	0	Indicates the status of the PM power control sequencer. 0: Stopped 1: Running.
Reserved	R	1	–	Reserved. If this bit is read, 0 is returned.
P0_SEQ_BUSY	R	0	0	Indicates the status of the P0 power control sequencer. 0: Stopped 1: Running.

### 3.2.266 Automatic P0 power control register

This register (P0\_SWON: E011\_0834H) sets up automatic P0 power switching.

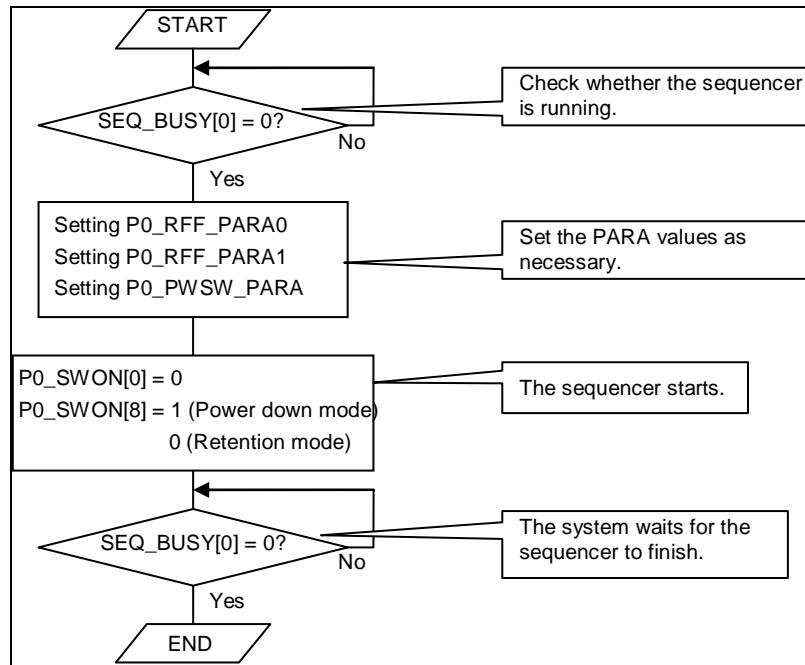
31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							P0_PDON
7	6	5	4	3	2	1	0
Reserved							P0_SWON

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:21	–	Reserved. If these bits are read, 0 is returned for each bit.
Reserved	R	20	–	Reserved. Write in 0B.
Reserved	R	19:9	–	Reserved. If these bits are read, 0 is returned for each bit.
P0_PDON	R/W	8	0	Specify the mode entered after the power is turned off. 0: Retention mode 1: Power down mode
Reserved	R	7:1	–	Reserved. If these bits are read, 0 is returned for each bit.
P0_SWON	R/W	0	1	Control automatic P0 power switching. Read the P0_PWRSTATUS bit to determine completion of the sequence. 0: Start the sequence for turning off the P0 power. 1: Start the sequence for turning on the P0 power. The sequence does not start if the bit is overwritten by the same value.

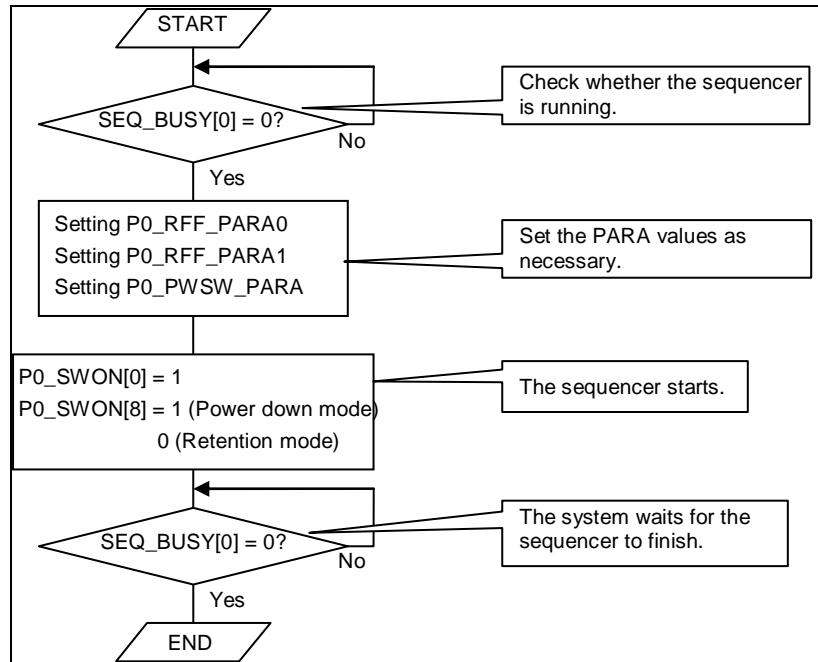
Do not rewrite the parameters and P0\_SWON register while the control sequencer is running (SEQ\_BUSY0 = 1). When making the power supply state PowerDown by a PowerDown control mode (Px\_SWON [8 ]= 1), when returning it to a Normal mode, be sure to begin a power supply SW-On control sequence by a PowerDown control mode (Px\_SWON [8 ]= 1).

It's also same in case of a Retention control mode.

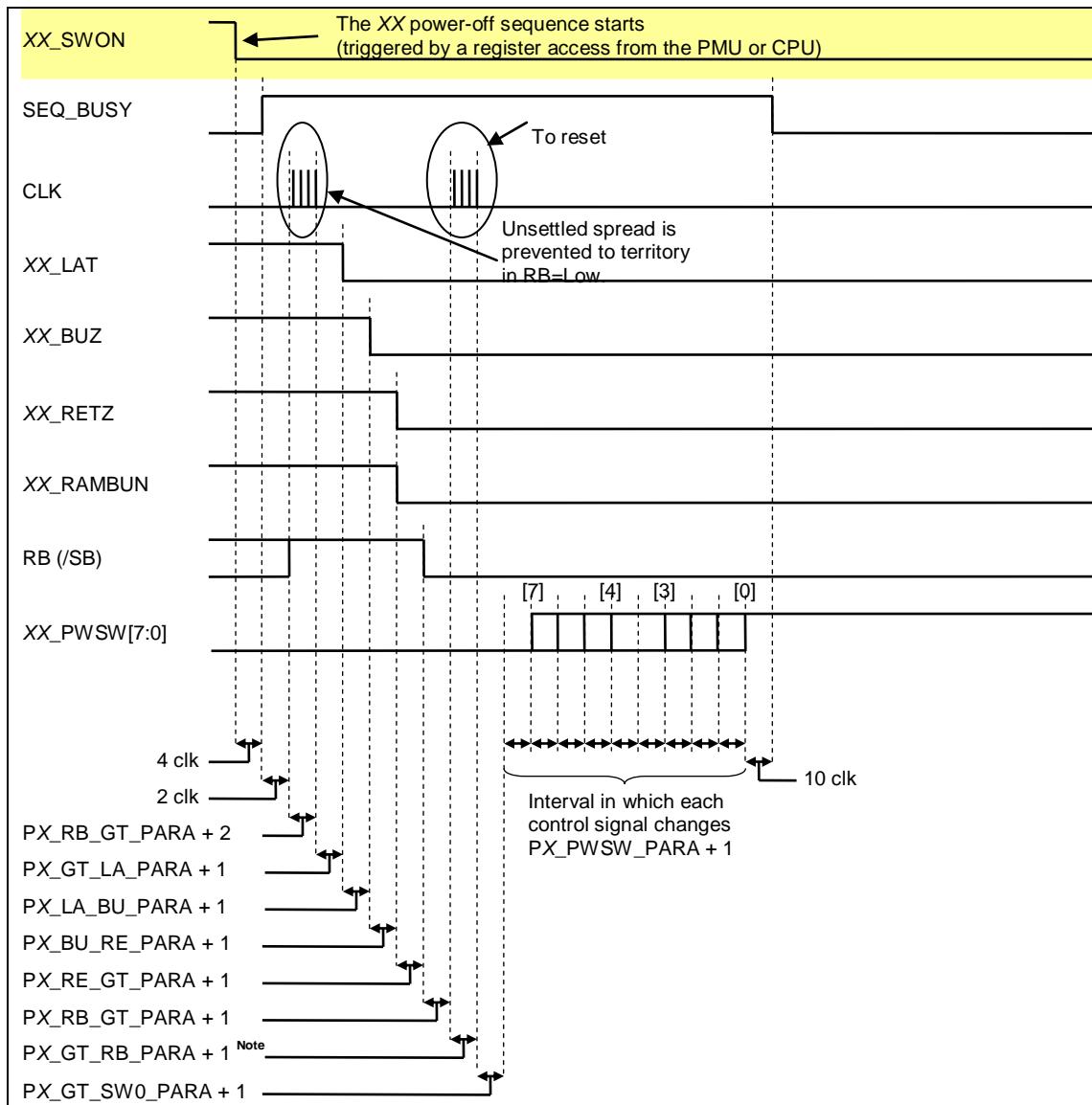
- Turning the power off



- Turning the power on

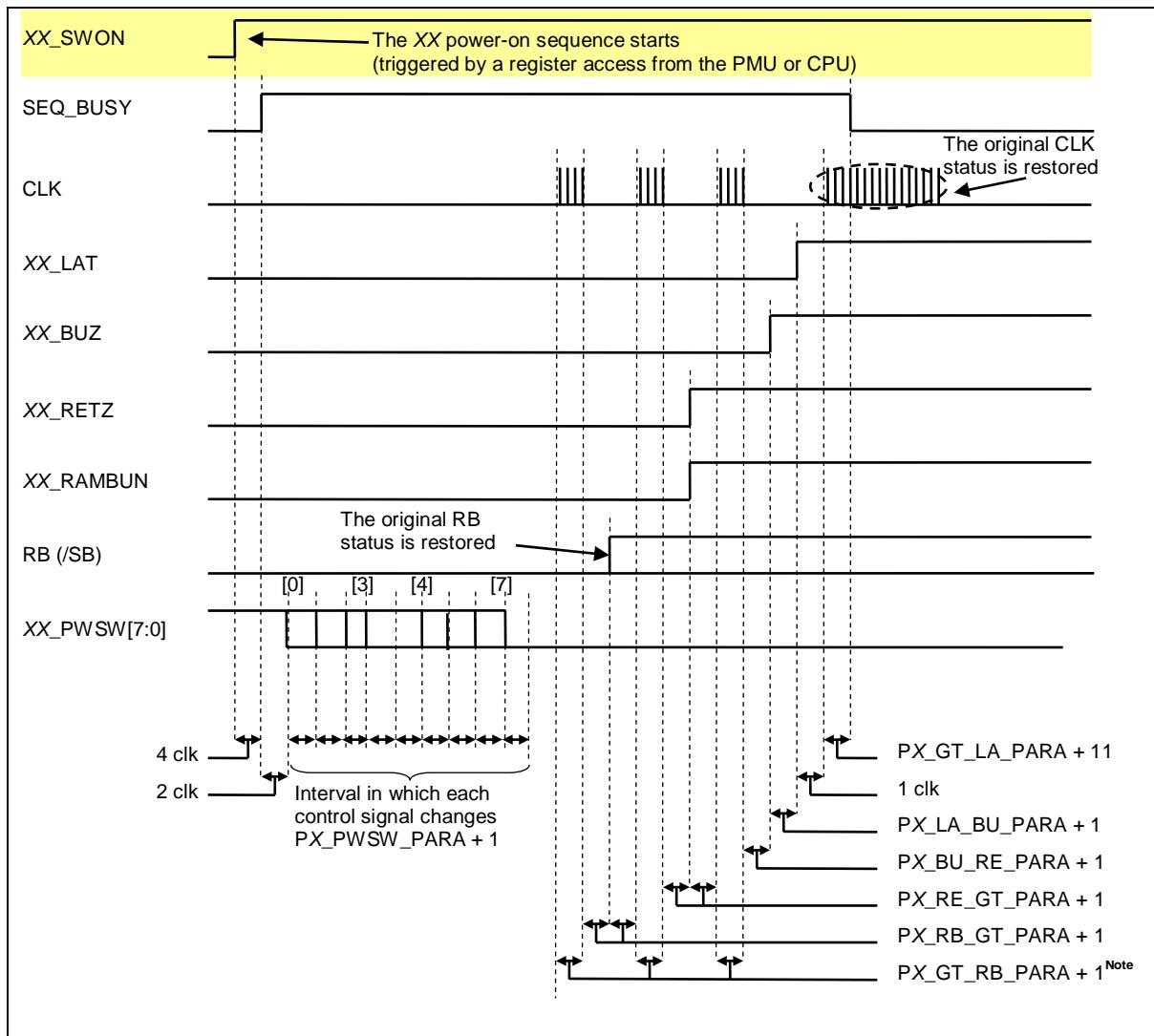


Automatic power switching for the P0, PU, PM, PL, P1, P2, PG, and PV domains (power-off sequence in retention mode)



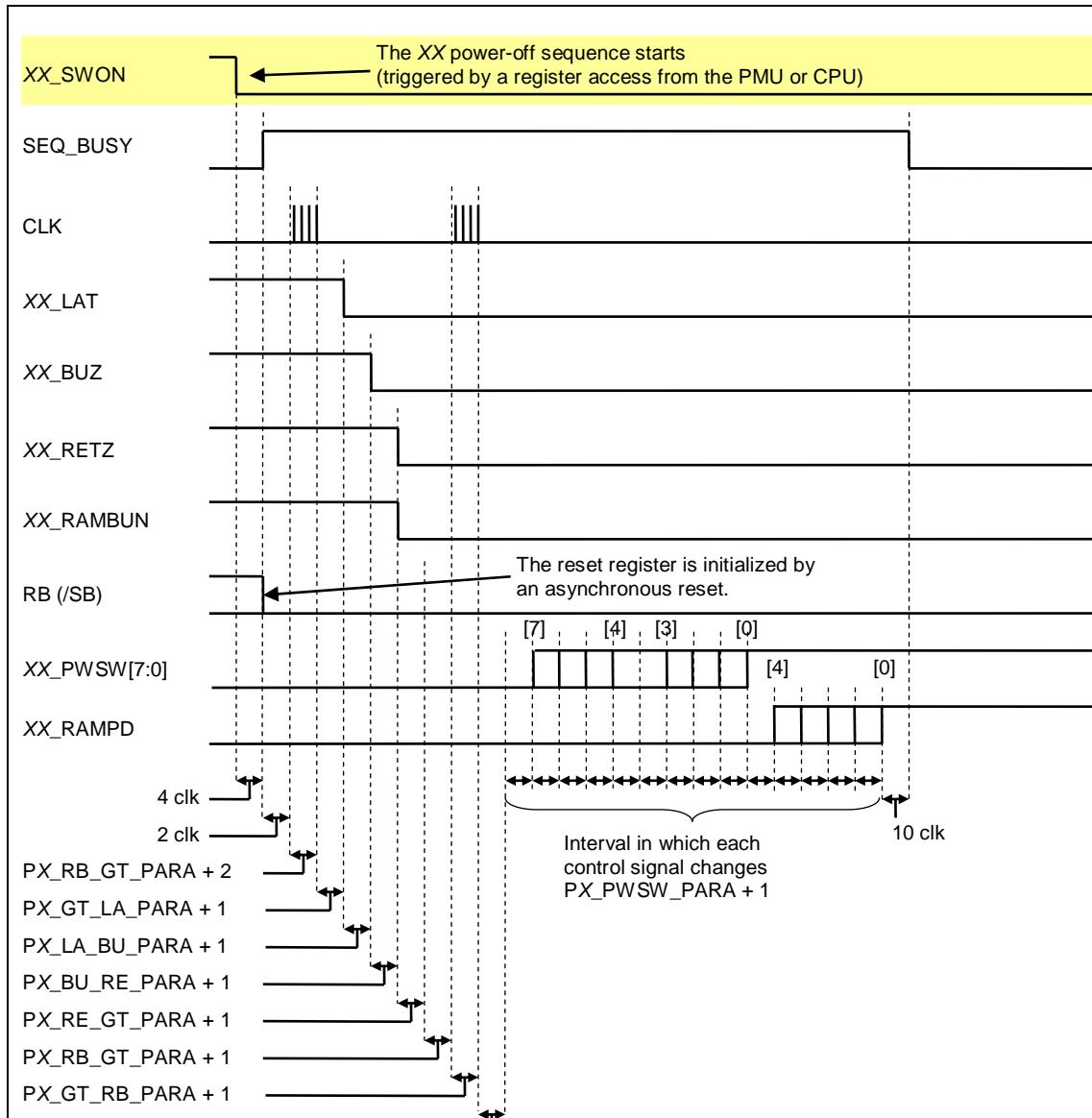
**Note** Because this register is reset in synchronization with the clock, specify a setting for this parameter so that at least 2 clock cycles are secured.

Automatic power switching for P0, PU, PM, PL, P1, P2, PG, and PV domains (power-on sequence in retention mode)

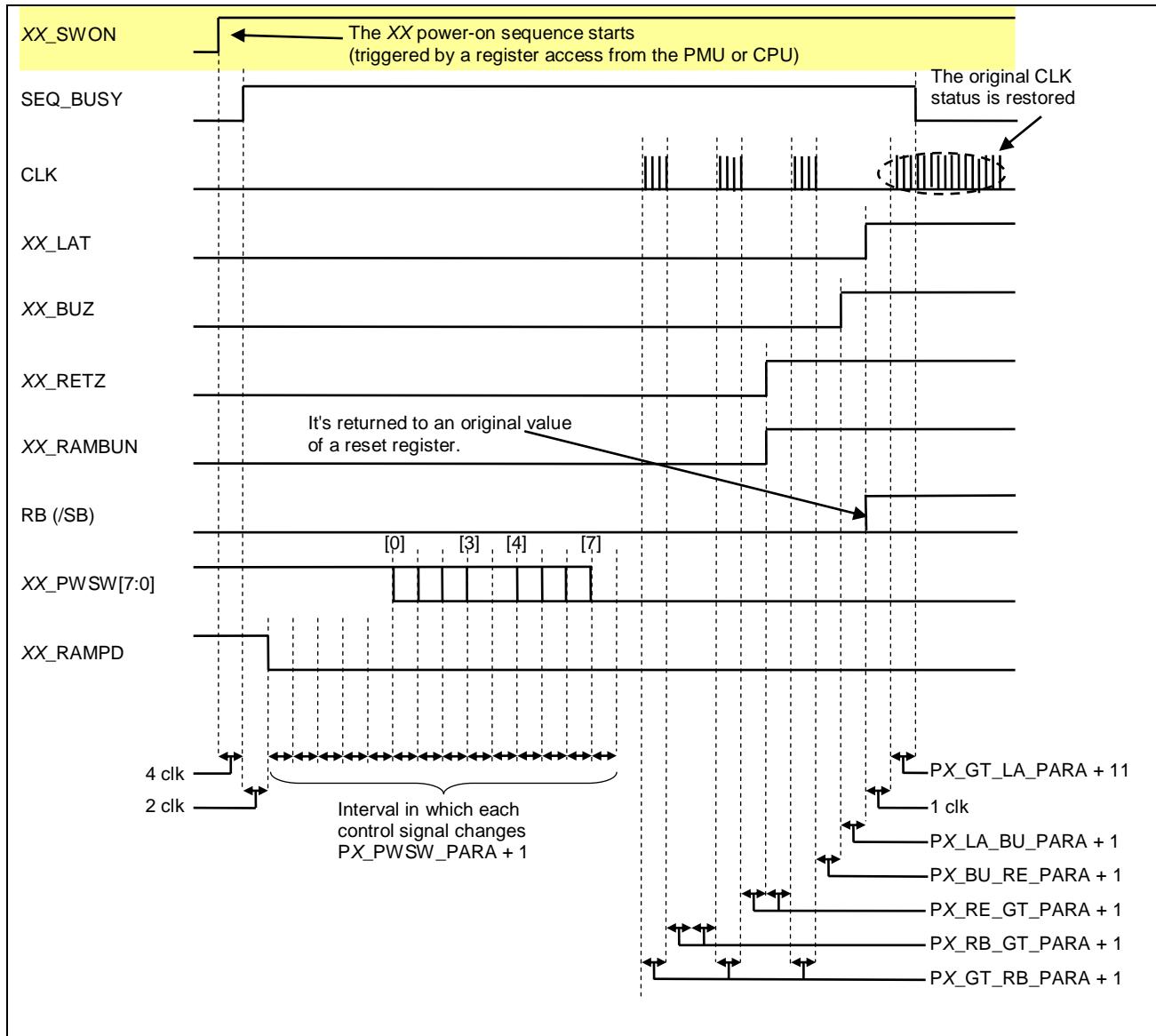


**Note** Because this register is reset in clock-synchronized, specify this parameter so that at least 2 clock cycles are secured.

Automatic power switching for P0, PU, PM, PL, P1, P2, PG, and PV domains (power-off sequence in power down mode)



Automatic power switching for P0, PU, PM, PL, P1, P2, PG, and PV domains (power-on sequence in power down mode)



### 3.2.267 Automatic PU power control register

This register (PU\_SWON: E011\_083CH) sets up automatic PU power switching.

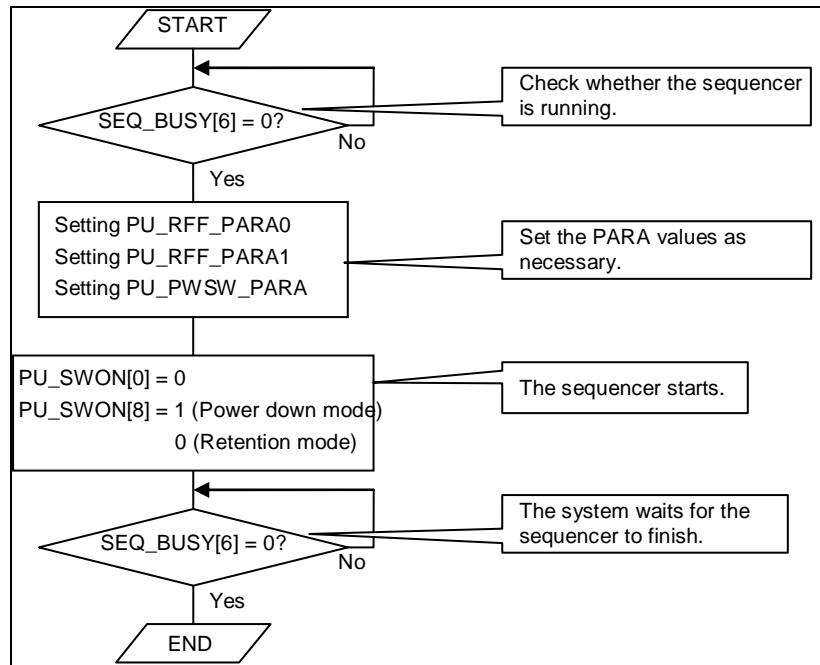
31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								
7	6	5	4	3	2	1	0	
Reserved								
Name	R/W	Bit No.	After Reset	Description				
Reserved	R	31:21	–	Reserved. If these bits are read, 0 is returned for each bit.				
Reserved	R	20	–	Reserved. Write in 0B.				
Reserved	R	19:17	–	Reserved. If these bits are read, 0 is returned for each bit.				
PU_RSTZ_CTREN	R/W	16	0	Specify whether to enable automatic power switching by using a USB reset (USB0RSTZ   USB1RSTZ). 0: Disable automatic power switching. 1: Enable automatic power switching.				
Reserved	R	15:9	–	Reserved. If these bits are read, 0 is returned for each bit.				
PU_PDON	R/W	8	0	Specify the mode entered after the power is turned off. 0: Retention mode 1: Power down mode				
Reserved	R	7:1	–	Reserved. If these bits are read, 0 is returned for each bit.				
PU_SWON	R/W	0	1	Control automatic PU power switching. Read the PU_PWRSTATUS bit to determine completion of the sequence. 0: Start the sequence for turning off the PU power. 1: Start the sequence for turning on the PU power.				

Do not rewrite the parameters and PU\_SWON register while the control sequencer is running (SEQ\_BUSY6 = 1).

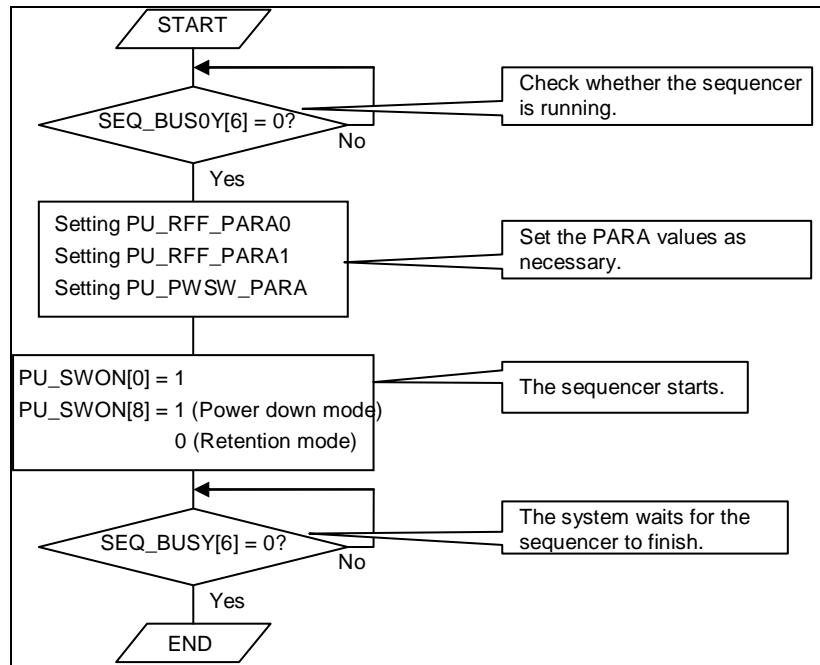
When making the power supply state PowerDown by a PowerDown control mode (Px\_SWON [8 ]= 1), when returning it to a Normal mode, be sure to begin a power supply SW-On control sequence by a PowerDown control mode (Px\_SWON [8 ]= 1).

It's also same in case of a Retention control mode.

- Turning the power off



- Turning the power on



### 3.2.268 Automatic PM power control register

This register (PM\_SWON: E011\_0840H) sets up automatic PM power switching.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							PM_PDON
7	6	5	4	3	2	1	0
Reserved							PM_SWON

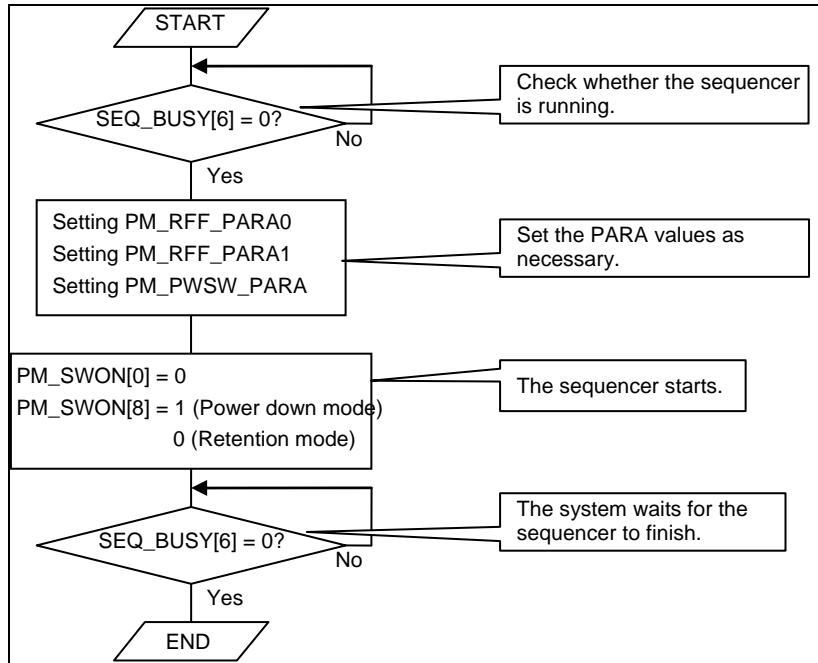
Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:21	–	Reserved. If these bits are read, 0 is returned for each bit.
Reserved	R	20	–	Reserved. Write in 0.
Reserved	R	19:9	–	Reserved. If these bits are read, 0 is returned for each bit.
PM_PDON	R/W	8	0	Specify the mode entered after the power is turned off. 0: Retention mode 1: Power down mode
Reserved	R	7:1	–	Reserved. If these bits are read, 0 is returned for each bit.
PM_SWON	R/W	0	1	Control automatic PM power switching. Read the PM_PWRSTATUS bit to determine completion of the sequence. 0: Start the sequence for turning off the PM power. 1: Start the sequence for turning on the PM power.

Do not rewrite the parameters and PM\_SWON register while the control sequencer is running (SEQ\_BUSY6 = 1).

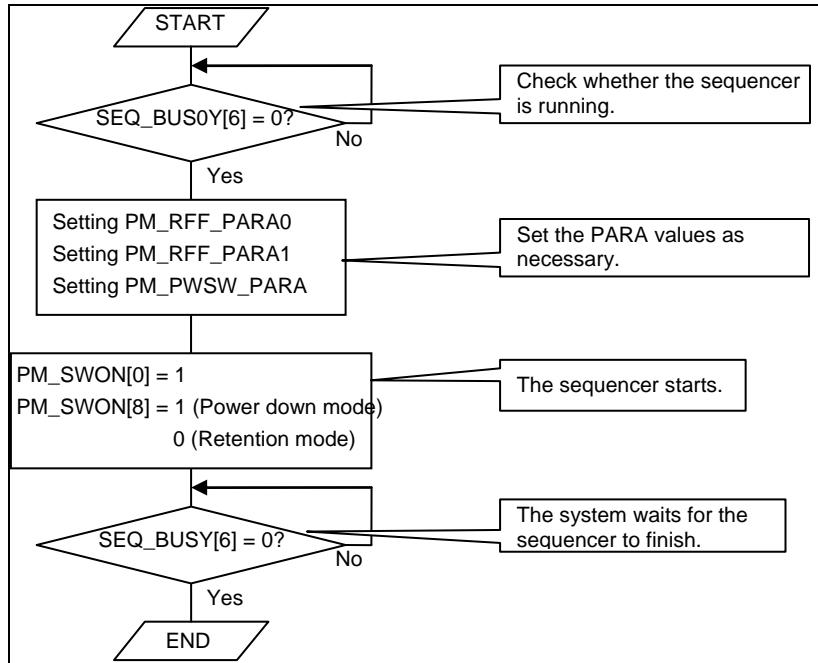
When making the power supply state PowerDown by a PowerDown control mode (Px\_SWON [8] = 1), when returning it to a Normal mode, be sure to begin a power supply SW-On control sequence by a PowerDown control mode (Px\_SWON [8] = 1).

It's also same in case of a Retention control mode.

- Turning the power off



- Turning the power on



### 3.2.269 Automatic PL power control register

This register (PL\_SWON: E011\_0844H) sets up automatic PL power switching.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							PL_PDON
7	6	5	4	3	2	1	0
Reserved							PL_SWON

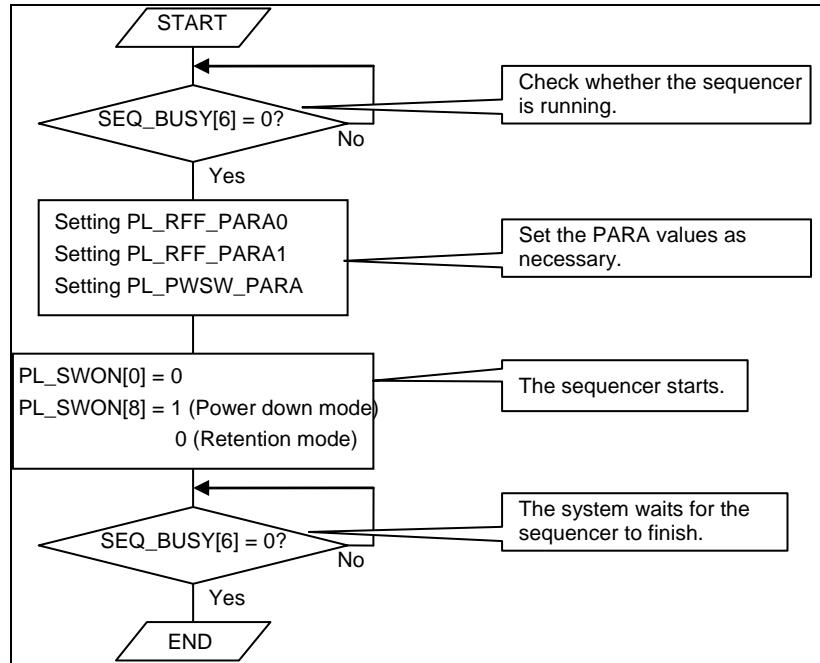
Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:21	–	Reserved. If these bits are read, 0 is returned for each bit.
Reserved	R	20	–	Reserved. Write in 0.
Reserved	R	19:9	–	Reserved. If these bits are read, 0 is returned for each bit.
PL_PDON	R/W	8	0	Specify the mode entered after the power is turned off. 0: Retention mode 1: Power down mode
Reserved	R	7:1	–	Reserved. If these bits are read, 0 is returned for each bit.
PL_SWON	R/W	0	1	Control automatic PL power switching. Read the PL_PWRSTATUS bit to determine completion of the sequence. 0: Start the sequence for turning off the PL power. 1: Start the sequence for turning on the PL power.

Do not rewrite the parameters and PL\_SWON register while the control sequencer is running (SEQ\_BUSY6 = 1).

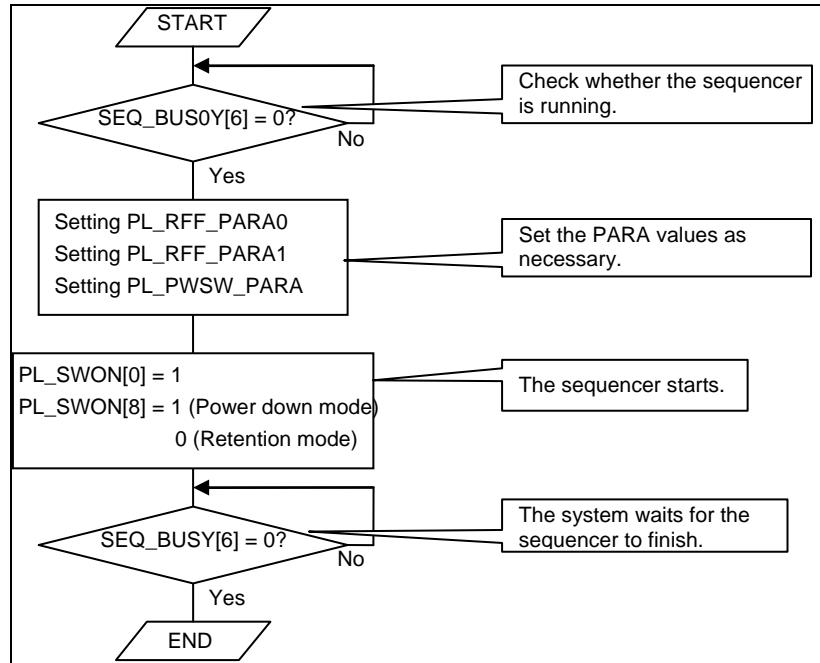
When making the power supply state PowerDown by a PowerDown control mode (Px\_SWON [8 ]= 1), when returning it to a Normal mode, be sure to begin a power supply SW-On control sequence by a PowerDown control mode (Px\_SWON [8 ]= 1).

It's also same in case of a Retention control mode.

- Turning the power off



- Turning the power on



### 3.2.270 Automatic P1 power control register

This register (P1\_SWON: E011\_084CH) sets up automatic P1 power switching.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								P1_PDON
7	6	5	4	3	2	1	0	
Reserved								P1_SWON

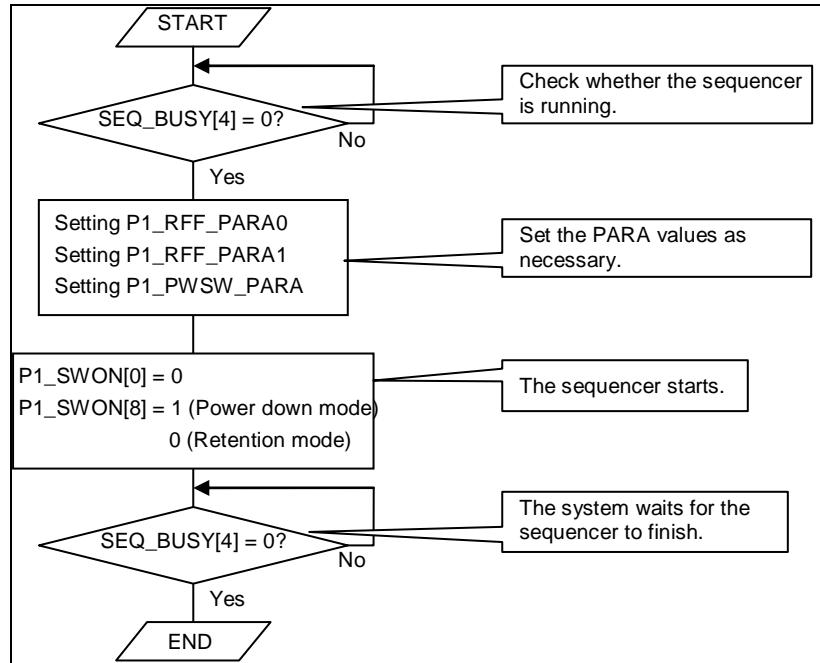
Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:21	–	Reserved. If these bits are read, 0 is returned for each bit.
Reserved	R	20	–	Reserved. Write in 0B.
Reserved	R	19:9	–	Reserved. If these bits are read, 0 is returned for each bit.
P1_PDON	R/W	8	0	Specify the mode entered after the power is turned off. 0: Retention mode 1: Power down mode
Reserved	R	7:1	–	Reserved. If these bits are read, 0 is returned for each bit.
P1_SWON	R/W	0	1	Control automatic P1 power switching. Read the P1_PWRSTATUS bit to determine completion of the sequence. 0: Start the sequence for turning off the P1 power. 1: Start the sequence for turning on the P1 power.

Do not rewrite the parameters and P1\_SWON register while the control sequencer is running (SEQ\_BUSY4 = 1).

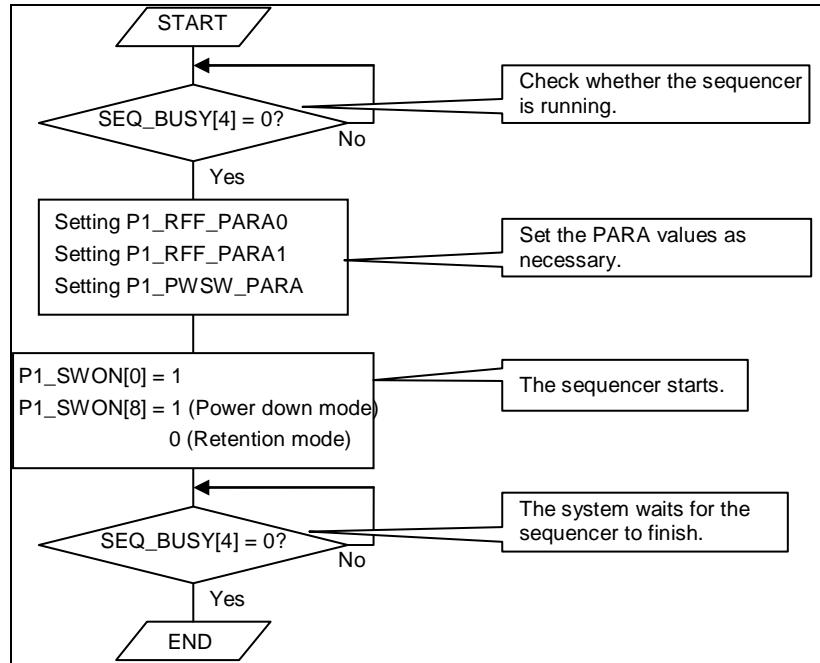
When making the power supply state PowerDown by a PowerDown control mode (Px\_SWON [8 ]= 1), when returning it to a Normal mode, be sure to begin a power supply SW-On control sequence by a PowerDown control mode (Px\_SWON [8 ]= 1).

It's also same in case of a Retention control mode.

- Turning the power off



- Turning the power on



### 3.2.271 Automatic P2 power control register

This register (P2\_SWON: E011\_0850H) sets up automatic P2 power switching.

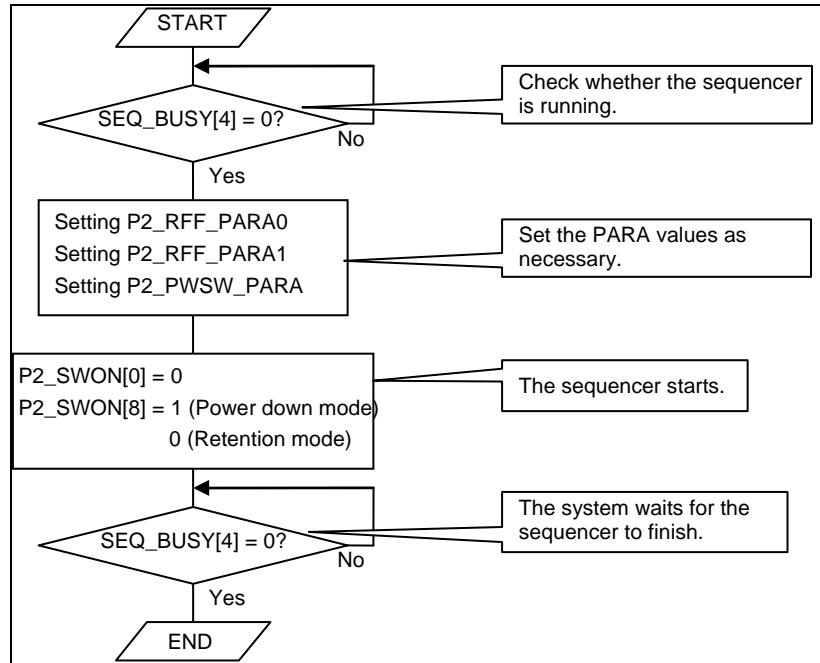
31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							P2_PDON
7	6	5	4	3	2	1	0
Reserved							P2_SWON

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:21	–	Reserved. If these bits are read, 0 is returned for each bit.
Reserved	R	20	–	Reserved. Write in 0.
Reserved	R	19:9	–	Reserved. If these bits are read, 0 is returned for each bit.
P2_PDON	R/W	8	0	Specify the mode entered after the power is turned off. 0: Retention mode 1: Power down mode
Reserved	R	7:1	–	Reserved. If these bits are read, 0 is returned for each bit.
P2_SWON	R/W	0	1	Control automatic P2 power switching. Read the P2_PWRSTATUS bit to determine completion of the sequence. 0: Start the sequence for turning off the P2 power. 1: Start the sequence for turning on the P2 power.

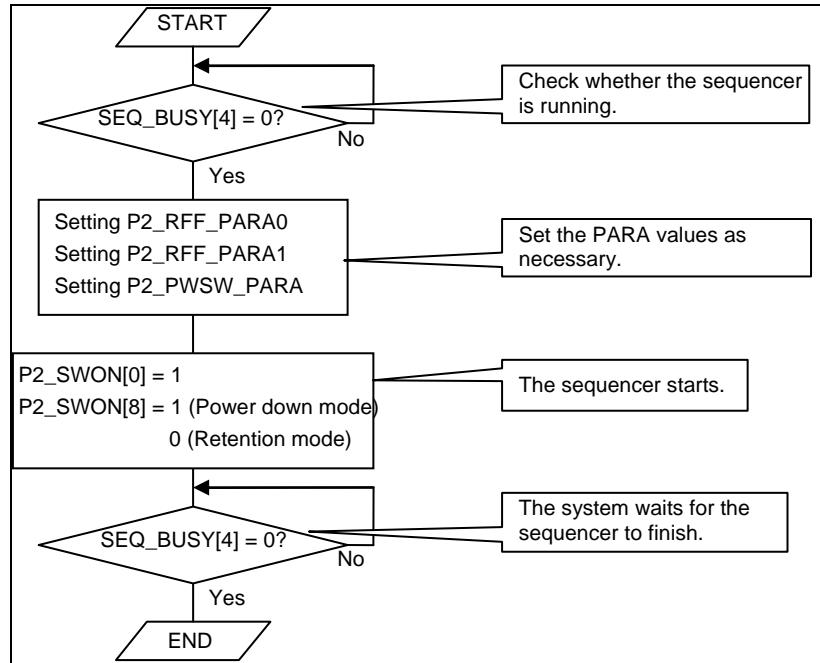
Do not rewrite the parameters and P2\_SWON register while the control sequencer is running (SEQ\_BUSY4 = 1). When making the power supply state PowerDown by a PowerDown control mode (Px\_SWON [8 ]= 1), when returning it to a Normal mode, be sure to begin a power supply SW-On control sequence by a PowerDown control mode (Px\_SWON [8 ]= 1).

It's also same in case of a Retention control mode.

- Turning the power off



- Turning the power on



### 3.2.272 Automatic PG power control register

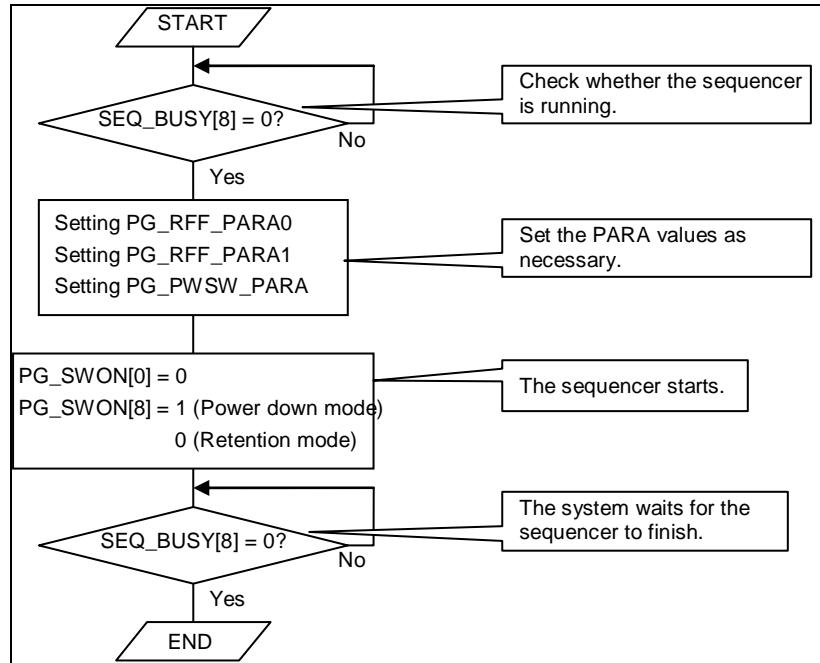
This register (PG\_SWON: E011\_0854H) sets up automatic PG power switching.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								
7	6	5	4	3	2	1	0	
Reserved								
Name	R/W	Bit No.	After Reset	Description				
Reserved	R	31:21	–	Reserved. If these bits are read, 0 is returned for each bit.				
Reserved	R	20	–	Reserved. Write in 0.				
Reserved	R	19:17	–	Reserved. If these bits are read, 0 is returned for each bit.				
PG_RSTZ_CTREN	R/W	16	0	Specify whether to enable automatic power switching by detecting the rising or falling edge of A3DRSTZ. 0: Disable automatic power switching. 1: Enable automatic power switching.				
Reserved	R	15:9	–	Reserved. If these bits are read, 0 is returned for each bit.				
PG_PDON	R/W	8	0	Specify the mode entered after the power is turned off. 0: Retention mode 1: Power down mode				
Reserved	R	7:1	–	Reserved. If these bits are read, 0 is returned for each bit.				
PG_SWON	R/W	0	1	Control automatic PG power switching. Read the PG_PWRSTATUS bit to determine completion of the sequence. 0: Start the sequence for turning off the PG power. 1: Start the sequence for turning on the PG power.				

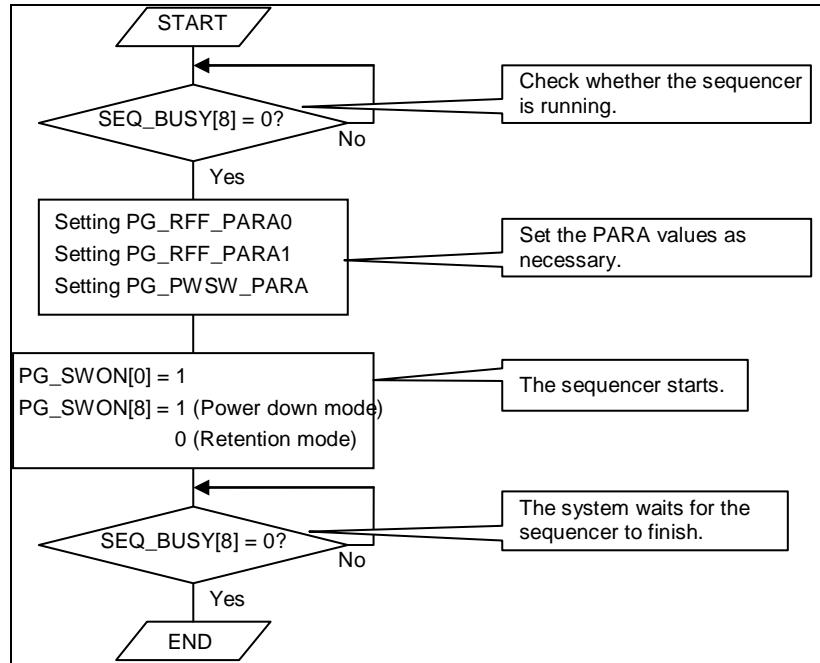
Do not rewrite the parameters and PG\_SWON register while the control sequencer is running (SEQ\_BUSY8 = 1). When making the power supply state PowerDown by a PowerDown control mode (Px\_SWON [8 ]= 1), when returning it to a Normal mode, be sure to begin a power supply SW-On control sequence by a PowerDown control mode (Px\_SWON [8 ]= 1).

It's also same in case of a Retention control mode.

- Turning the power off



- Turning the power on



### 3.2.273 Automatic PV power control register

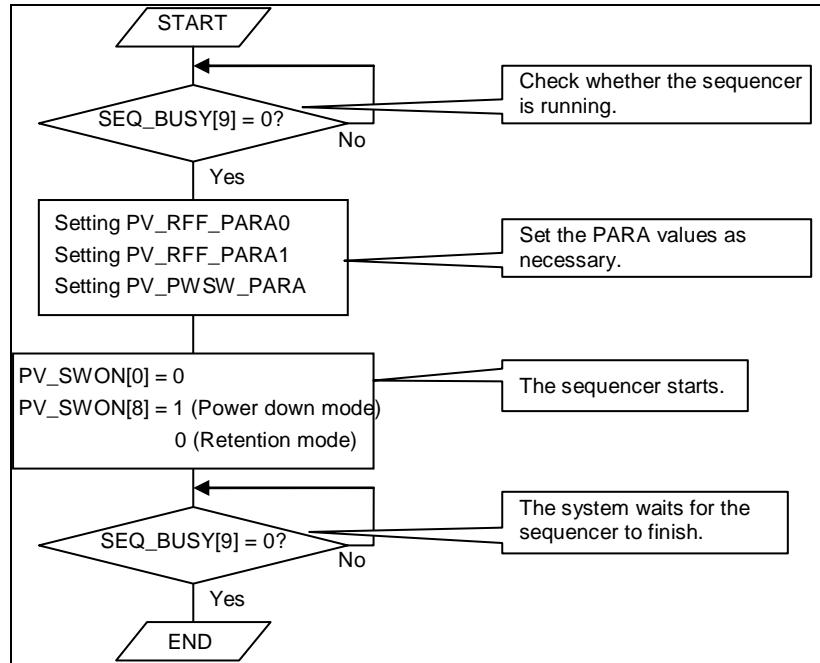
This register (PV\_SWON: E011\_0858H) sets up automatic PV power switching.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								
7	6	5	4	3	2	1	0	
Reserved								
Name	R/W	Bit No.	After Reset	Description				
Reserved	R	31:21	–	Reserved. If these bits are read, 0 is returned for each bit.				
Reserved	R	20	–	Reserved. Write in 0B.				
Reserved	R	19:17	–	Reserved. If these bits are read, 0 is returned for each bit.				
PV_RSTZ_CTREN	R/W	16	0	Specify whether to enable automatic power switching by detecting the rising or falling edge of (AVECRSTZ   AVEARSTZ   AVEPRSTZ). 0: Disable automatic power switching. 1: Enable automatic power switching.				
Reserved	R	15:9	–	Reserved. If these bits are read, 0 is returned for each bit.				
PV_PDON	R/W	8	0	Specify the mode entered after the power is turned off. 0: Retention mode 1: Power down mode				
Reserved	R	7:1	–	Reserved. If these bits are read, 0 is returned for each bit.				
PV_SWON	R/W	0	1	Control automatic PV power switching. Read the PV_PWRSTATUS bit to determine completion of the sequence. 0: Start the sequence for turning off the PV power. 1: Start the sequence for turning on the PV power.				

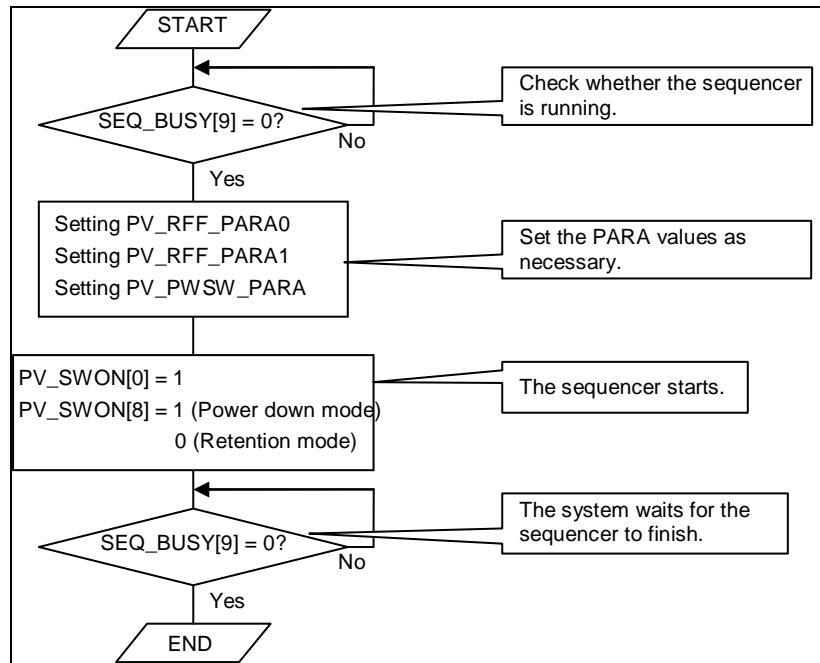
Do not rewrite the parameters and PV\_SWON register while the control sequencer is running (SEQ\_BUSY9 = 1). When making the power supply state PowerDown by a PowerDown control mode (Px\_SWON [8 ]= 1), when returning it to a Normal mode, be sure to begin a power supply SW-On control sequence by a PowerDown control mode (Px\_SWON [8 ]= 1).

It's also same in case of a Retention control mode.

- Turning the power off



- Turning the power on



### 3.2.274 Automatic PR power control register

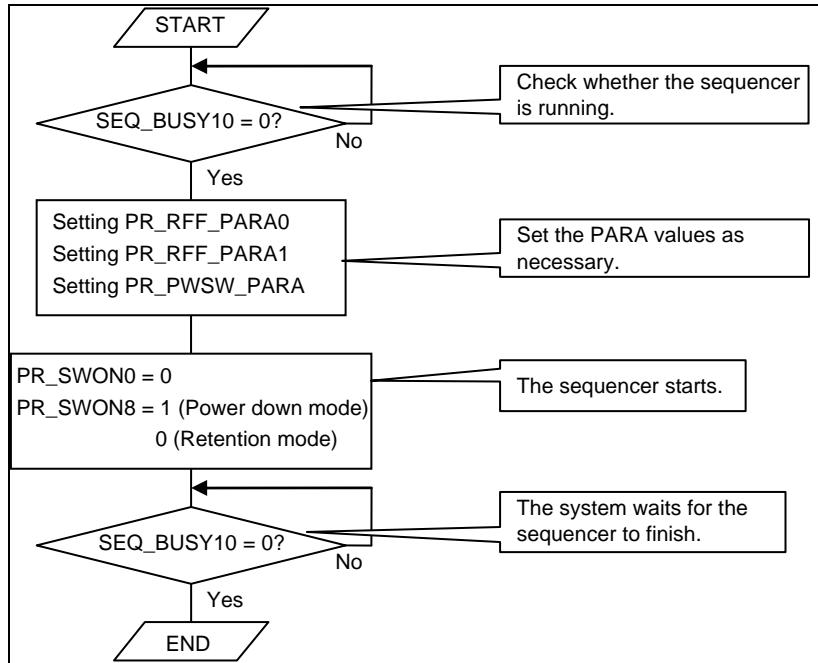
This register (PR\_SWON: E011\_085CH) sets up automatic PR power switching.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								
7	6	5	4	3	2	1	0	
Reserved								
Name	R/W	Bit No.	After Reset	Description				
Reserved	R	31:21	–	Reserved. If these bits are read, 0 is returned for each bit.				
Reserved	R	20	–	Reserved. Write in 0B.				
Reserved	R	19:17	–	Reserved. If these bits are read, 0 is returned for each bit.				
PR_RSTZ_CTREN	R/W	16	0	Specify whether to enable automatic power switching by detecting the rising or falling edge of (AVECRSTZ   AVEARSTZ   AVEPRSTZ). 0: Disable automatic power switching. 1: Enable automatic power switching.				
Reserved	R	15:1	–	Reserved. If these bits are read, 0 is returned for each bit.				
PR_SWON	R/W	0	1	Control automatic PR power switching. Read the PR_PWRSTATUS bit to determine completion of the sequence. 0: Start the sequence for turning off the PR power. 1: Start the sequence for turning on the PR power.				

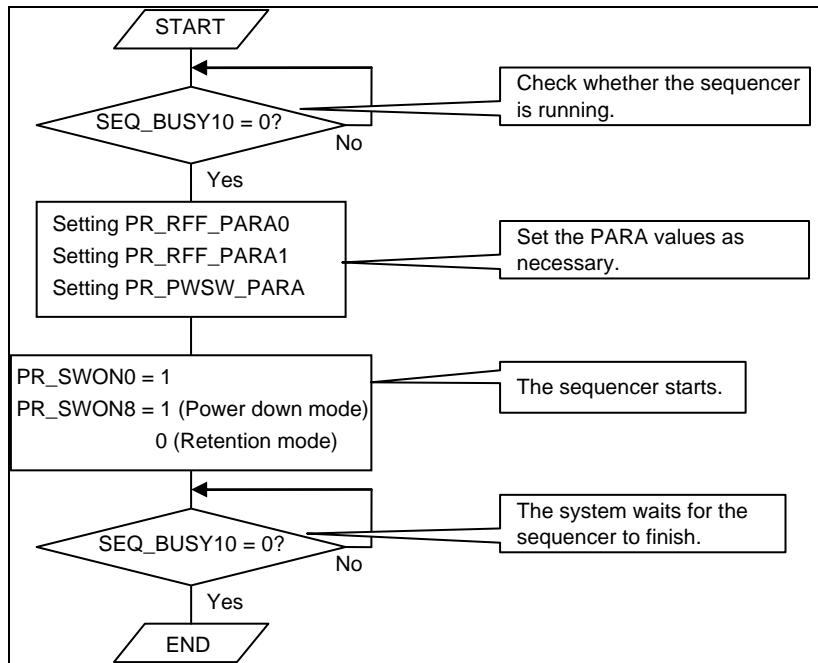
Do not rewrite the parameters and PR\_SWON register while the control sequencer is running (SEQ\_BUSY10 = 1). When making the power supply state PowerDown by a PowerDown control mode (Px\_SWON [8 ]= 1), when returning it to a Normal mode, be sure to begin a power supply SW-On control sequence by a PowerDown control mode (Px\_SWON [8 ]= 1).

It's also same in case of a Retention control mode.

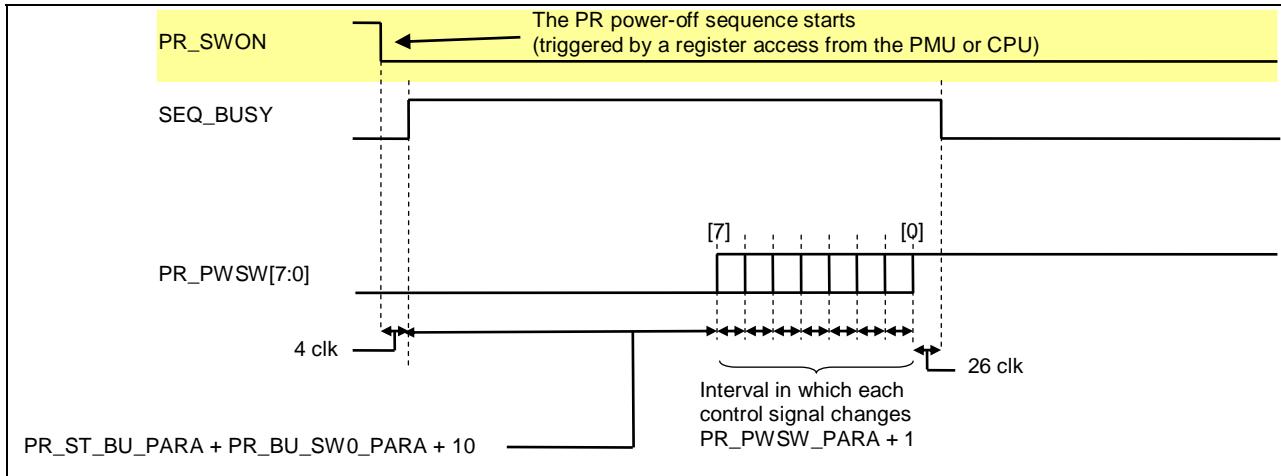
- Turning the power off



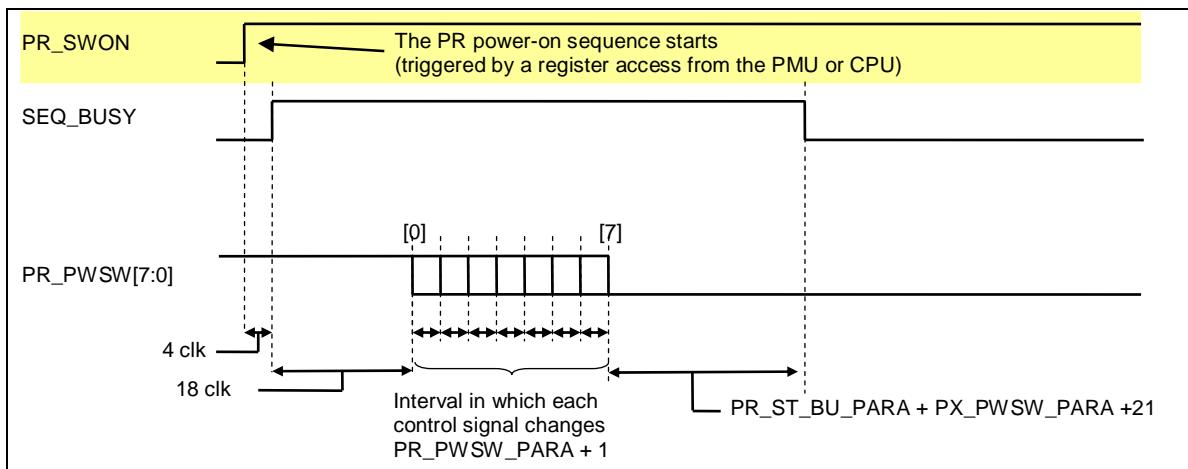
- Turning the power on



Automatic power switching for PR domain (power-off sequence)



Automatic power switching for PR domain (power-on sequence)



### 3.2.275 P0 power RFF/RRAM control signal input interval setting register 0

This register (P0\_RFF\_PARA0: E011\_0860H) specifies the interval of inputting the control signal for the P0 power retention F/F and RAM.

31	30	29	28	27	26	25	24
Reserved		P0_BU_RE_PARA					
23	22	21	20	19	18	17	16
Reserved		P0_LA_BU_PARA					
15	14	13	12	11	10	9	8
Reserved		P0_GT_LA_PARA					
7	6	5	4	3	2	1	0
Reserved		P0_RB_GT_PARA					

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:29	–	Reserved. If these bits are read, 0 is returned for each bit.
P0_BU_RE_PARA	R/W	28:24	04H	For Normal to Retention, specify the interval from P0_BUN↓ to P0_RET↓. For Retention to Normal, specify the interval from P0_BUN↑ to P0_RET↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	23:21	–	Reserved. If these bits are read, 0 is returned for each bit.
P0_LA_BU_PARA	R/W	20:16	04H	For Normal to Retention, specify the interval from P0_LAT↓ to P0_BUN↓. For Retention to Normal, specify the interval from P0_LAT↑ to P0_BUN↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
P0_GT_LA_PARA	R/W	12:8	04H	For Normal to Retention, specify the interval from clock control signal↑ to P0_LAT↓. For Retention to Normal, specify the interval from clock control signal↓ to P0_LAT↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.
P0_RB_GT_PARA	R/W	4:0	04H	For Normal to Retention, specify the interval from RB↑ (SB↓) to clock control signal↑. For Retention to Normal, specify the interval from RB↑ (SB↓) to clock control signal↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)

### 3.2.276 P0 power RFF/RRAM control signal input interval setting register 1

This register (P0\_RFF\_PARA1: E011\_0864H) specifies the interval of inputting the control signal for the P0 power retention F/F and RAM.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved		P0_GT_SW0_PARA						
15	14	13	12	11	10	9	8	
Reserved		P0_GT_RB_PARA						
7	6	5	4	3	2	1	0	
Reserved		P0_RE_GT_PARA						

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:21	–	Reserved. If these bits are read, 0 is returned for each bit.
P0_GT_SW0_PARA	R/W	20:16	04H	For Normal to Retention, specify the interval from GT↓ to PSW (first off)↑. For Retention to Normal, specify the interval from PSW (last on)↓ to GT↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
P0_GT_RB_PARA	R/W	12:8	04H	For Retention to Normal, specify the interval from clock control signal↓ to RB↑ (SB↓). (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.
P0_RE_GT_PARA	R/W	4:0	04H	For Retention to Normal, specify the interval from P0_RET↑ to clock control signal↓. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)

### 3.2.277 P0 power turn-on interval setting register

This register (P0\_PWSW\_PARA: E011\_0868H) specifies the P0 power turn-on interval.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved				P0_PWSW_PARA			
7	6	5	4	3	2	1	0
P0_PWSW_PARA							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:14	–	Reserved. If these bits are read, 0 is returned for each bit.			
P0_PWSW_PARA	R/W	13:0	0085H	Specify the interval to turn on the power corresponding to bits P0_PWSW[15:8]. (Specified value + 1) × HFB cycle time			

### 3.2.278 PU power RFF/RRAM control signal input interval setting register 0

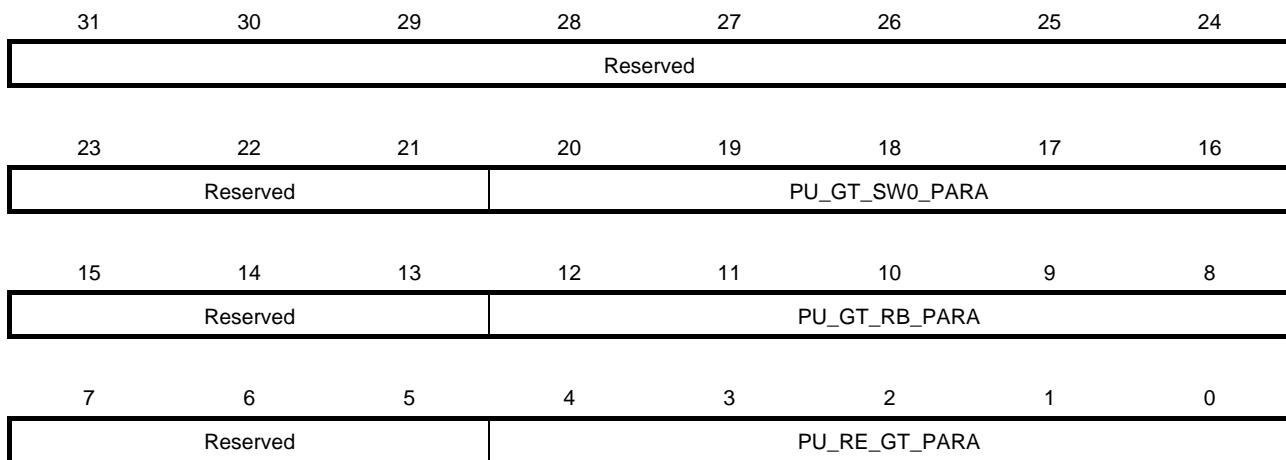
This register (PU\_RFF\_PARA0: E011\_0878H) specifies the interval of inputting the control signal for the PU power retention F/F and RAM.

31	30	29	28	27	26	25	24
Reserved		PU_BU_RE PARA					
23	22	21	20	19	18	17	16
Reserved		PU_LA_BU PARA					
15	14	13	12	11	10	9	8
Reserved		PU_GT_LA PARA					
7	6	5	4	3	2	1	0
Reserved		PU_RB_GT PARA					

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:29	–	Reserved. If these bits are read, 0 is returned for each bit.
PU_BU_RE PARA	R/W	28:24	04H	For Normal to Retention, specify the interval from PU_BUN↓ to PU_RET↓. For Retention to Normal, specify the interval from PU_BUN↑ to PU_RET↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	23:21	–	Reserved. If these bits are read, 0 is returned for each bit.
PU_LA_BU PARA	R/W	20:16	04H	For Normal to Retention, specify the interval from PU_LAT↓ to PU_BUN↓. For Retention to Normal, specify the interval from PU_LAT↑ to PU_BUN↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
PU_GT_LA PARA	R/W	12:8	04H	For Normal to Retention, specify the interval from clock control signal↑ to PU_LAT↓. For Retention to Normal, specify the interval from clock control signal↓ to PU_LAT↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.
PU_RB_GT PARA	R/W	4:0	04H	For Normal to Retention, specify the interval from RB↑ (SB↓) to clock control signal↑. For Retention to Normal, specify the interval from RB↑ (SB↓) to clock control signal↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)

### 3.2.279 PU power RFF/RRAM control signal input interval setting register 1

This register (PU\_RFF\_PARA1: E011\_087CH) specifies the interval of inputting the control signal for the PU power retention F/F and RAM.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:21	–	Reserved. If these bits are read, 0 is returned for each bit.
PU_GT_SW0_PARA	R/W	20:16	04H	For Normal to Retention, specify the interval from GT↓ to PSW (first off)↑. For Retention to Normal, specify the interval from PSW (last on) ↓ to GT↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
PU_GT_RB_PARA	R/W	12:8	04H	For Retention to Normal, specify the interval from clock control signal↓ to RB↑ (SB↓). (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.
PU_RE_GT_PARA	R/W	4:0	04H	For Retention to Normal, specify the interval from PU_RET↑ to clock control signal↓. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)

### 3.2.280 PU power turn-on interval setting register

This register (PU\_PWSW\_PARA: E011\_0880H) specifies the PU power turn-on interval.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved				PU_PWSW_PARA			
7	6	5	4	3	2	1	0
PU_PWSW_PARA							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:14	–	Reserved. If these bits are read, 0 is returned for each bit.			
PU_PWSW_PARA	R/W	13:0	0085H	Specify the interval to turn on the power corresponding to bits PU_PWSW[15:8]. (Specified value + 1) × HFB cycle time			

### 3.2.281 PM power RFF/RRAM control signal input interval setting register 0

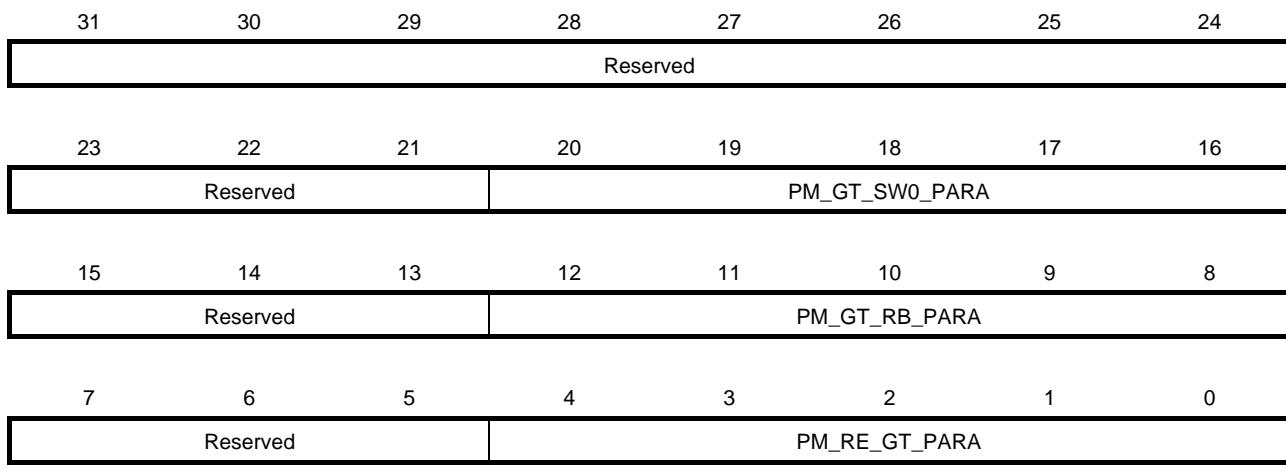
This register (PM\_RFF\_PARA0: E011\_0884H) specifies the interval of inputting the control signal for the PM power retention F/F and RAM.

31	30	29	28	27	26	25	24
Reserved		PM_BU_RE PARA					
23	22	21	20	19	18	17	16
Reserved		PM_LA_BU PARA					
15	14	13	12	11	10	9	8
Reserved		PM_GT_LA PARA					
7	6	5	4	3	2	1	0
Reserved		PM_RB_GT PARA					

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:29	–	Reserved. If these bits are read, 0 is returned for each bit.
PM_BU_RE PARA	R/W	28:24	04H	For Normal to Retention, specify the interval from PM_BUN↓ to PM_RET↓. For Retention to Normal, specify the interval from PM_BUN↑ to PM_RET↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	23:21	–	Reserved. If these bits are read, 0 is returned for each bit.
PM_LA_BU PARA	R/W	20:16	04H	For Normal to Retention, specify the interval from PM_LAT↓ to PM_BUN↓. For Retention to Normal, specify the interval from PM_LAT↑ to PM_BUN↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
PM_GT_LA PARA	R/W	12:8	04H	For Normal to Retention, specify the interval from clock control signal↑ to PM_LAT↓. For Retention to Normal, specify the interval from clock control signal↓ to PM_LAT↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.
PM_RB_GT PARA	R/W	4:0	04H	For Normal to Retention, specify the interval from RB↑ (SB↓) to clock control signal↑. For Retention to Normal, specify the interval from RB↑ (SB↓) to clock control signal↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)

### 3.2.282 PM power RFF/RRAM control signal input interval setting register 1

This register (PM\_RFF\_PARA1: E011\_0888H) specifies the interval of inputting the control signal for the PM power retention F/F and RAM.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:21	–	Reserved. If these bits are read, 0 is returned for each bit.
PM_GT_SW0_PARA	R/W	20:16	04H	For Normal to Retention, specify the interval from GT↓ to PSW (first off)↑. For Retention to Normal, specify the interval from PSW (last on) ↓ to GT↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
PM_GT_RB_PARA	R/W	12:8	04H	For Retention to Normal, specify the interval from clock control signal↓ to RB↑ (SB↓). (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.
PM_RE_GT_PARA	R/W	4:0	04H	For Retention to Normal, specify the interval from PM_RET↑ to clock control signal↓. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)

### 3.2.283 PM power turn-on interval setting register

This register (PM\_PWSW\_PARA: E011\_088CH) specifies the PM power turn-on interval.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved				PM_PWSW_PARA			
7	6	5	4	3	2	1	0
PM_PWSW_PARA							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:14	–	Reserved. If these bits are read, 0 is returned for each bit.			
PM_PWSW_PARA	R/W	13:0	0085H	Specify the interval to turn on the power corresponding to bits PM_PWSW[15:8]. (Specified value + 1) × HFB cycle time			

### 3.2.284 PL power RFF/RRAM control signal input interval setting register 0

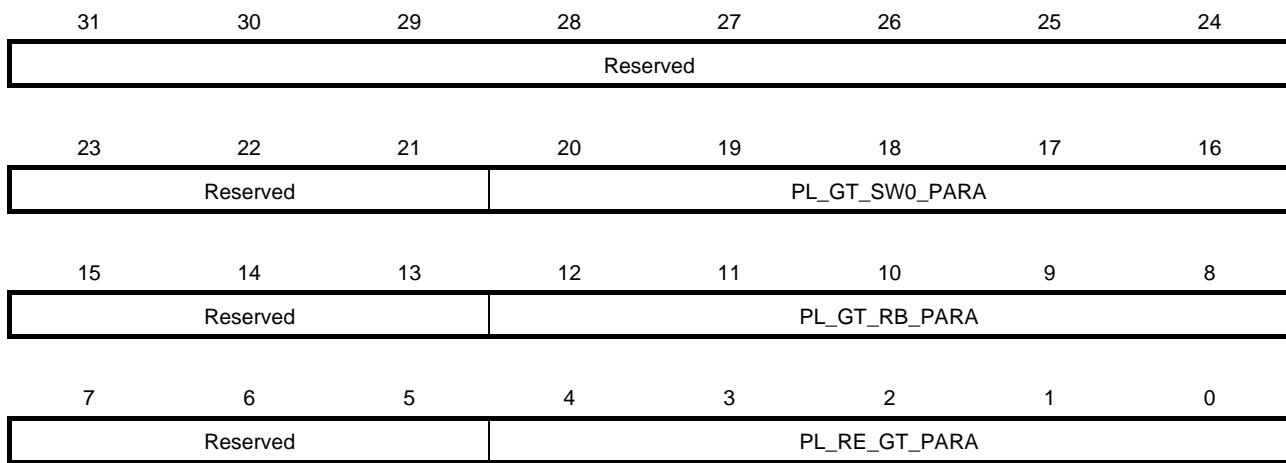
This register (PL\_RFF\_PARA0: E011\_0890H) specifies the interval of inputting the control signal for the PL power retention F/F and RAM.

31	30	29	28	27	26	25	24
Reserved		PL_BU_RE_PARA					
23	22	21	20	19	18	17	16
Reserved		PL_LA_BU_PARA					
15	14	13	12	11	10	9	8
Reserved		PL_GT_LA_PARA					
7	6	5	4	3	2	1	0
Reserved		PL_RB_GT_PARA					

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:29	–	Reserved. If these bits are read, 0 is returned for each bit.
PL_BU_RE_PARA	R/W	28:24	04H	For Normal to Retention, specify the interval from PL_BUN↓ to PL_RET↓. For Retention to Normal, specify the interval from PL_BUN↑ to PL_RET↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	23:21	–	Reserved. If these bits are read, 0 is returned for each bit.
PL_LA_BU_PARA	R/W	20:16	04H	For Normal to Retention, specify the interval from PL_LAT↓ to PL_BUN↓. For Retention to Normal, specify the interval from PL_LAT↑ to PL_BUN↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
PL_GT_LA_PARA	R/W	12:8	04H	For Normal to Retention, specify the interval from clock control signal↑ to PL_LAT↓. For Retention to Normal, specify the interval from clock control signal↓ to PL_LAT↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.
PL_RB_GT_PARA	R/W	4:0	04H	For Normal to Retention, specify the interval from RB↑ (SB↓) to clock control signal↑. For Retention to Normal, specify the interval from RB↑ (SB↓) to clock control signal↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)

### 3.2.285 PL power RFF/RRAM control signal input interval setting register 1

This register (PL\_RFF\_PARA1: E011\_0894H) specifies the interval of inputting the control signal for the PL power retention F/F and RAM.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:21	–	Reserved. If these bits are read, 0 is returned for each bit.
PL_GT_SW0_PARA	R/W	20:16	04H	For Normal to Retention, specify the interval from GT↓ to PSW (first off)↑. For Retention to Normal, specify the interval from PSW (last on) ↓ to GT↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
PL_GT_RB_PARA	R/W	12:8	04H	For Retention to Normal, specify the interval from clock control signal↓ to RB↑ (SB↓). (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.
PL_RE_GT_PARA	R/W	4:0	04H	For Retention to Normal, specify the interval from PL_RET↑ to clock control signal↓. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)

### 3.2.286 PL power turn-on interval setting register

This register (PL\_PWSW\_PARA: E011\_0898H) specifies the PL power turn-on interval.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved				PL_PWSW_PARA			
7	6	5	4	3	2	1	0
PL_PWSW_PARA							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:14	–	Reserved. If these bits are read, 0 is returned for each bit.			
PL_PWSW_PARA	R/W	13:0	0085H	Specify the interval to turn on the power corresponding to bits PL_PWSW[15:8]. (Specified value + 1) × HFB cycle time			

### 3.2.287 P1 power RFF/RRAM control signal input interval setting register 0

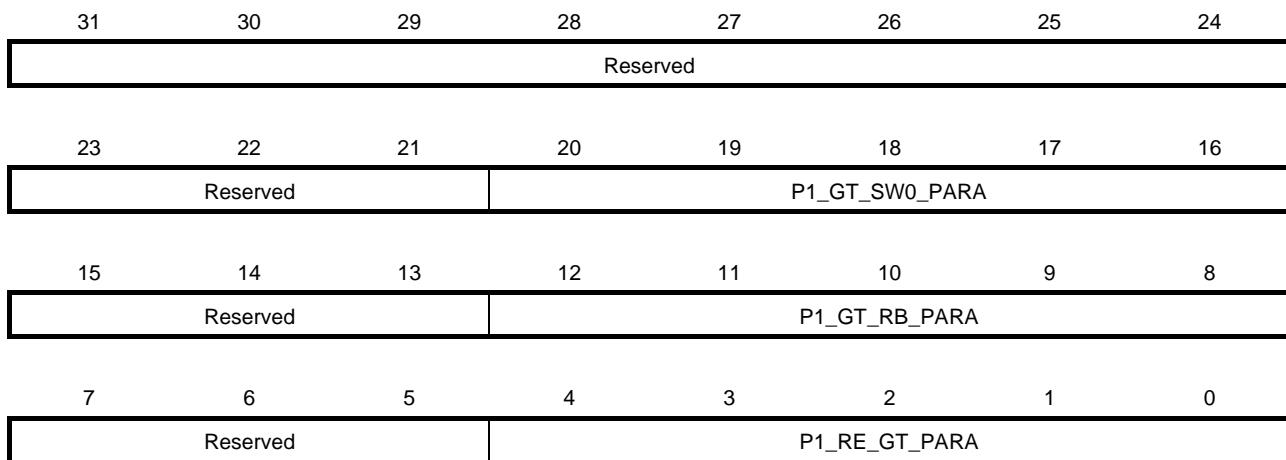
This register (P1\_RFF\_PARA0: E011\_08A8H) specifies the interval of inputting the control signal for the P1 power retention F/F and RAM.

31	30	29	28	27	26	25	24
Reserved		P1_BU_RE_PARA					
23	22	21	20	19	18	17	16
Reserved		P1_LA_BU_PARA					
15	14	13	12	11	10	9	8
Reserved		P1_GT_LA_PARA					
7	6	5	4	3	2	1	0
Reserved		P1_RB_GT_PARA					

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:29	–	Reserved. If these bits are read, 0 is returned for each bit.
P1_BU_RE_PARA	R/W	28:24	04H	For Normal to Retention, specify the interval from P1_BUN↓ to P1_RET↓. For Retention to Normal, specify the interval from P1_BUN↑ to P1_RET↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	23:21	–	Reserved. If these bits are read, 0 is returned for each bit.
P1_LA_BU_PARA	R/W	20:16	04H	For Normal to Retention, specify the interval from P1_LAT↓ to P1_BUN↓. For Retention to Normal, specify the interval from P1_LAT↑ to P1_BUN↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
P1_GT_LA_PARA	R/W	12:8	04H	For Normal to Retention, specify the interval from clock control signal↑ to P1_LAT↓. For Retention to Normal, specify the interval from clock control signal↓ to P1_LAT↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.
P1_RB_GT_PARA	R/W	4:0	04H	For Normal to Retention, specify the interval from RB↑ (SB↓) to clock control signal↑. For Retention to Normal, specify the interval from RB↑ (SB↓) to clock control signal↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)

### 3.2.288 P1 power RFF/RRAM control signal input interval setting register 1

This register (P1\_RFF\_PARA1: E011\_08ACH) specifies the interval of inputting the control signal for the P1 power retention F/F and RAM.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:21	–	Reserved. If these bits are read, 0 is returned for each bit.
P1_GT_SW0_PARA	R/W	20:16	04H	For Normal to Retention, specify the interval from GT↓ to PSW (first off)↑. For Retention to Normal, specify the interval from PSW (last on) ↓ to GT↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
P1_GT_RB_PARA	R/W	12:8	0BH	For Retention to Normal, specify the interval from clock control signal↓ to RB↑ (SB↓). (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.
P1_RE_GT_PARA	R/W	4:0	04H	For Retention to Normal, specify the interval from P1_RET↑ to clock control signal↓. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)

### 3.2.289 P1 power turn-on interval setting register

This register (P1\_PWSW\_PARA: E011\_08B0H) specifies the P1 power turn-on interval.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved				P1_PWSW_PARA			
7	6	5	4	3	2	1	0
P1_PWSW_PARA							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:14	–	Reserved. If these bits are read, 0 is returned for each bit.			
P1_PWSW_PARA	R/W	13:0	0085H	Specify the interval to turn on the power corresponding to bits P1_PWSW[15:8]. (Specified value + 1) × HFB cycle time			

### 3.2.290 P2 power RFF/RRAM control signal input interval setting register 0

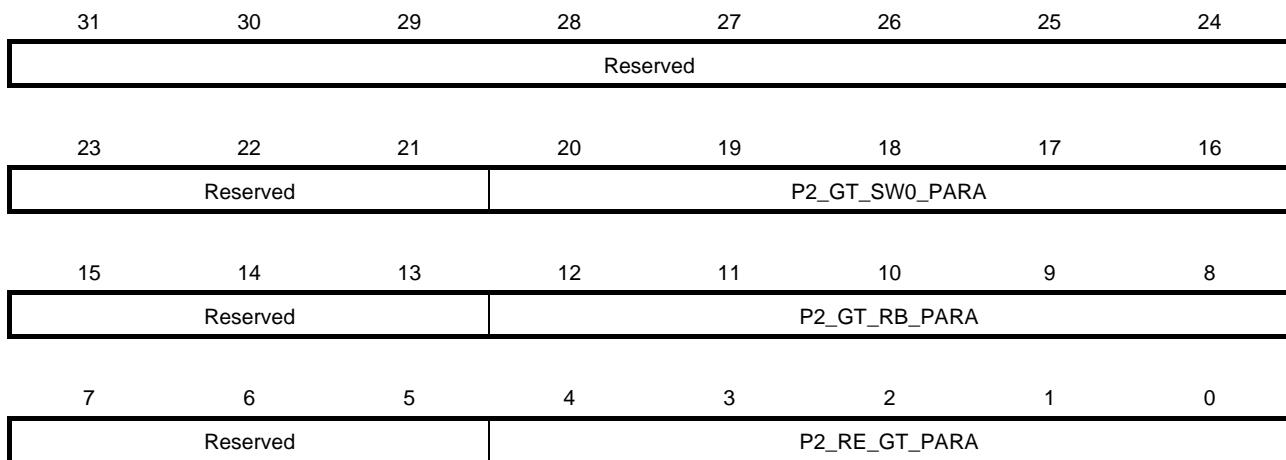
This register (P2\_RFF\_PARA0: E011\_08B4H) specifies the interval of inputting the control signal for the P2 power retention F/F and RAM.

31	30	29	28	27	26	25	24
Reserved		P2_BU_RE_PARA					
23	22	21	20	19	18	17	16
Reserved		P2_LA_BU_PARA					
15	14	13	12	11	10	9	8
Reserved		P2_GT_LA_PARA					
7	6	5	4	3	2	1	0
Reserved		P2_RB_GT_PARA					

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:29	–	Reserved. If these bits are read, 0 is returned for each bit.
P2_BU_RE_PARA	R/W	28:24	04H	For Normal to Retention, specify the interval from P2_BUN↓ to P2_RET↓. For Retention to Normal, specify the interval from P2_BUN↑ to P2_RET↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	23:21	–	Reserved. If these bits are read, 0 is returned for each bit.
P2_LA_BU_PARA	R/W	20:16	04H	For Normal to Retention, specify the interval from P2_LAT↓ to P2_BUN↓. For Retention to Normal, specify the interval from P2_LAT↑ to P2_BUN↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
P2_GT_LA_PARA	R/W	12:8	04H	For Normal to Retention, specify the interval from clock control signal↑ to P2_LAT↓. For Retention to Normal, specify the interval from clock control signal↓ to P2_LAT↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.
P2_RB_GT_PARA	R/W	4:0	04H	For Normal to Retention, specify the interval from RB↑ (SB↓) to clock control signal↑. For Retention to Normal, specify the interval from RB↑ (SB↓) to clock control signal↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)

### 3.2.291 P2 power RFF/RRAM control signal input interval setting register 1

This register (P2\_RFF\_PARA1: E011\_08B8H) specifies the interval of inputting the control signal for the P2 power retention F/F and RAM.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:21	–	Reserved. If these bits are read, 0 is returned for each bit.
P2_GT_SW0_PARA	R/W	20:16	04H	For Normal to Retention, specify the interval from GT↓ to PSW (first off)↑. For Retention to Normal, specify the interval from PSW (last on) ↓ to GT↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
P2_GT_RB_PARA	R/W	12:8	0BH	For Retention to Normal, specify the interval from clock control signal↓ to RB↑ (SB↓). (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.
P2_RE_GT_PARA	R/W	4:0	04H	For Retention to Normal, specify the interval from P2_RET↑ to clock control signal↓. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)

### 3.2.292 P2 power turn-on interval setting register

This register (P2\_PWSW\_PARA: E011\_08BCH) specifies the P2 power turn-on interval.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved				P2_PWSW_PARA			
7	6	5	4	3	2	1	0
P2_PWSW_PARA							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:14	–	Reserved. If these bits are read, 0 is returned for each bit.			
P2_PWSW_PARA	R/W	13:0	0085H	Specify the interval to turn on the power corresponding to bits P2_PWSW[15:8]. (Specified value + 1) × HFB cycle time			

### 3.2.293 PG power RFF/RRAM control signal input interval setting register 0

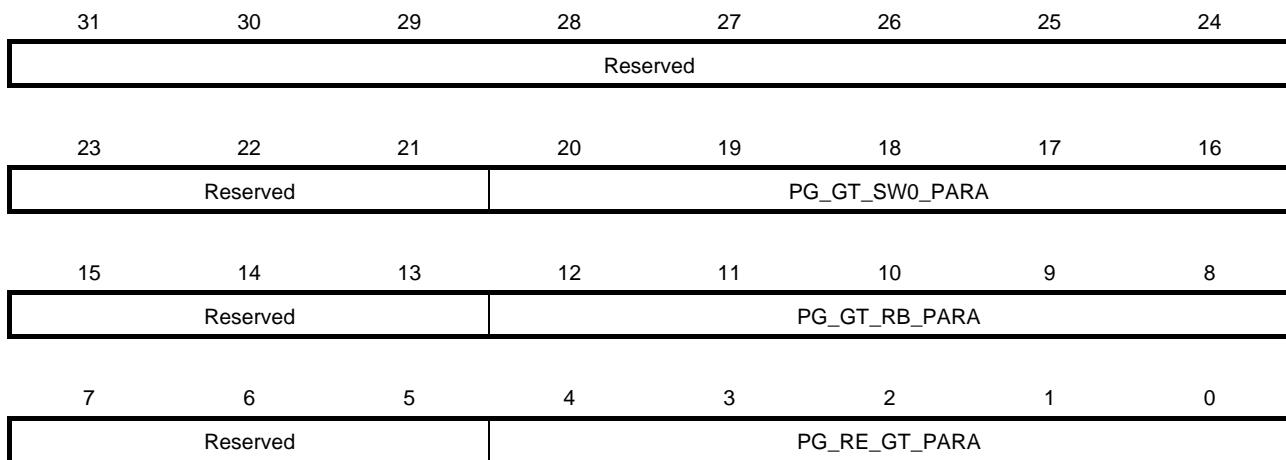
This register (PG\_RFF\_PARA0: E011\_08C0H) specifies the interval of inputting the control signal for the PG power retention F/F and RAM.

31	30	29	28	27	26	25	24
Reserved		PG_BU_RE PARA					
23	22	21	20	19	18	17	16
Reserved		PG_LA_BU PARA					
15	14	13	12	11	10	9	8
Reserved		PG_GT_LA PARA					
7	6	5	4	3	2	1	0
Reserved		PG_RB_GT PARA					

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:29	–	Reserved. If these bits are read, 0 is returned for each bit.
PG_BU_RE PARA	R/W	28:24	04H	For Normal to Retention, specify the interval from PG_BUN↓ to PG_RET↓. For Retention to Normal, specify the interval from PG_BUN↑ to PG_RET↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	23:21	–	Reserved. If these bits are read, 0 is returned for each bit.
PG_LA_BU PARA	R/W	20:16	04H	For Normal to Retention, specify the interval from PG_LAT↓ to PG_BUN↓. For Retention to Normal, specify the interval from PG_LAT↑ to PG_BUN↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
PG_GT_LA PARA	R/W	12:8	04H	For Normal to Retention, specify the interval from clock control signal↑ to PG_LAT↓. For Retention to Normal, specify the interval from clock control signal↓ to PG_LAT↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.
PG_RB_GT PARA	R/W	4:0	04H	For Normal to Retention, specify the interval from RB↑ (SB↓) to clock control signal↑. For Retention to Normal, specify the interval from RB↑ (SB↓) to clock control signal↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)

### 3.2.294 PG power RFF/RRAM control signal input interval setting register 1

This register (PG\_RFF\_PARA1: E011\_08C4H) specifies the interval of inputting the control signal for the PG power retention F/F and RAM.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:21	–	Reserved. If these bits are read, 0 is returned for each bit.
PG_GT_SW0_PARA	R/W	20:16	04H	For Normal to Retention, specify the interval from GT↓ to PSW (first off)↑. For Retention to Normal, specify the interval from PSW (last on) ↓ to GT↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
PG_GT_RB_PARA	R/W	12:8	04H	For Retention to Normal, specify the interval from clock control signal↓ to RB↑ (SB↓). (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.
PG_RE_GT_PARA	R/W	4:0	04H	For Retention to Normal, specify the interval from PG_RET↑ to clock control signal↓. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)

### 3.2.295 PG power turn-on interval setting register

This register (PG\_PWSW\_PARA: E011\_08C8H) specifies the PG power turn-on interval.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved				PG_PWSW_PARA			
7	6	5	4	3	2	1	0
PG_PWSW_PARA							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:14	–	Reserved. If these bits are read, 0 is returned for each bit.			
PG_PWSW_PARA	R/W	13:0	0085H	Specify the interval to turn on the power corresponding to bits PG_PWSW[15:8]. (Specified value + 1) × HFB cycle time			

### 3.2.296 PV power RFF/RRAM control signal input interval setting register 0

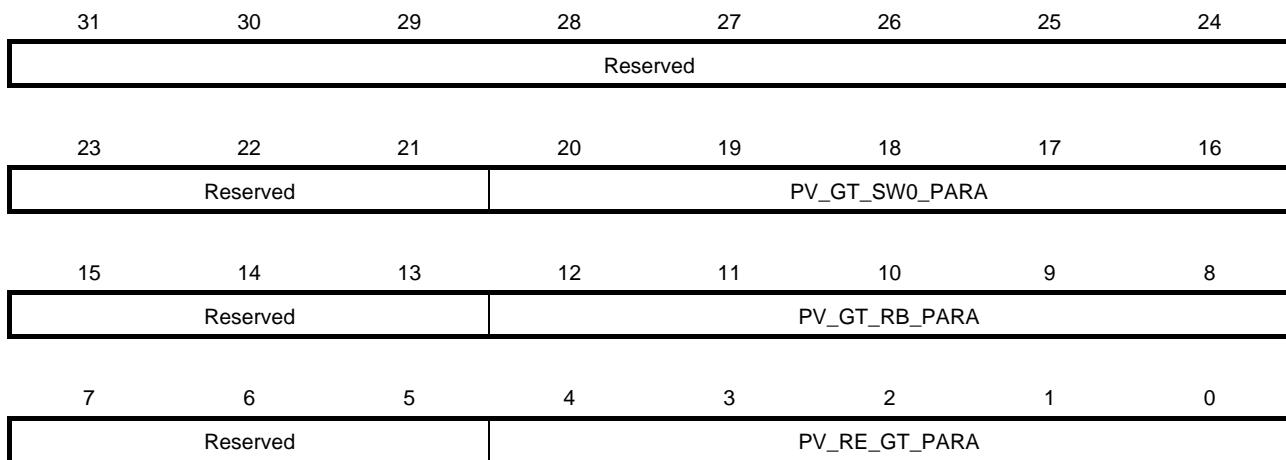
This register (PV\_RFF\_PARA0: E011\_08CCH) specifies the interval of inputting the control signal for the PV power retention F/F and RAM.

31	30	29	28	27	26	25	24
Reserved		PV_BU_RE PARA					
23	22	21	20	19	18	17	16
Reserved		PV_LA_BU PARA					
15	14	13	12	11	10	9	8
Reserved		PV_GT_LA PARA					
7	6	5	4	3	2	1	0
Reserved		PV_RB_GT PARA					

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:29	–	Reserved. If these bits are read, 0 is returned for each bit.
PV_BU_RE PARA	R/W	28:24	04H	For Normal to Retention, specify the interval from PV_BUN↓ to PV_RET↓. For Retention to Normal, specify the interval from PV_BUN↑ to PV_RET↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	23:21	–	Reserved. If these bits are read, 0 is returned for each bit.
PV_LA_BU PARA	R/W	20:16	04H	For Normal to Retention, specify the interval from PV_LAT↓ to PV_BUN↓. For Retention to Normal, specify the interval from PV_LAT↑ to PV_BUN↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
PV_GT_LA PARA	R/W	12:8	04H	For Normal to Retention, specify the interval from clock control signal↑ to PV_LAT↓. For Retention to Normal, specify the interval from clock control signal↓ to PV_LAT↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.
PV_RB_GT PARA	R/W	4:0	04H	For Normal to Retention, specify the interval from RB↑ (SB↓) to clock control signal↑. For Retention to Normal, specify the interval from RB↑ (SB↓) to clock control signal↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)

### 3.2.297 PV power RFF/RRAM control signal input interval setting register 1

This register (PV\_RFF\_PARA1: E011\_08D0H) specifies the interval of inputting the control signal for the PV power retention F/F and RAM.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:21	–	Reserved. If these bits are read, 0 is returned for each bit.
PV_GT_SW0_PARA	R/W	20:16	04H	For Normal to Retention, specify the interval from GT↓ to PSW (first off)↑. For Retention to Normal, specify the interval from PSW (last on) ↓ to GT↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
PV_GT_RB_PARA	R/W	12:8	04H	For Retention to Normal, specify the interval from clock control signal↓ to RB↑ (SB↓). (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.
PV_RE_GT_PARA	R/W	4:0	04H	For Retention to Normal, specify the interval from PV_RET↑ to clock control signal↓. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)

### 3.2.298 PV power turn-on interval setting register

This register (PV\_PWSW\_PARA: E011\_08D4H) specifies the PV power turn-on interval.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved				PV_PWSW_PARA			
7	6	5	4	3	2	1	0
PV_PWSW_PARA							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:14	–	Reserved. If these bits are read, 0 is returned for each bit.			
PV_PWSW_PARA	R/W	13:0	0085H	Specify the interval to turn on the power corresponding to bits PV_PWSW[15:8]. (Specified value + 1) × HFB cycle time			

### 3.2.299 PR power RFF/RRAM control signal input interval setting register 0

This register (PR\_RFF\_PARA0: E011\_08D8H) specifies the interval of inputting the control signal for the PR power retention F/F and RAM.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				PR_ST_BU_PARA			
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:5	–	Reserved. If these bits are read, 0 is returned for each bit.			
PR_ST_BU_PARA	R/W	4:0	04H	For Normal to Power Down, specify the interval from PR_SWON (power turn-off sequence starts) to PR_BUN↓. For Power Down to Normal, specify the interval from PSW (last on) ↓ to PR_BUN↑. (Specified value + 4) × HFB cycle time      (↑: Rise, ↓: Fall)			

### 3.2.300 PR power RFF/RRAM control signal input interval setting register 1

This register (PR\_RFF\_PARA1: E011\_08DCH) specifies the interval of inputting the control signal for the PR power retention F/F and RAM.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				PR_BU_SW0_PARA			

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:5	–	Reserved. If these bits are read, 0 is returned for each bit.
PR_BU_SW0_PARA	R/W	4:0	04H	For Normal to Power Down, specify the interval from PR_BUN↓ to PSW (first off)↑. (Specified value + 4) × HFB cycle time (↑: Rise, ↓: Fall)

### 3.2.301 PR power turn-on interval setting register

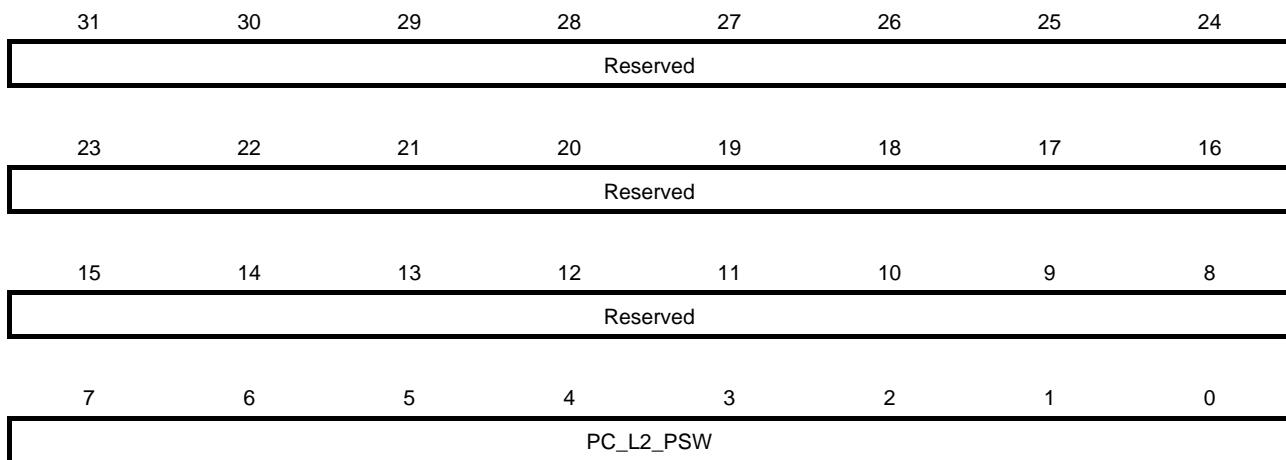
This register (PR\_PWSW\_PARA: E011\_08E0H) specifies the PR power turn-on interval.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved				PR_PWSW_PARA			
7	6	5	4	3	2	1	0
PR_PWSW_PARA							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:14	–	Reserved. If these bits are read, 0 is returned for each bit.
PR_PWSW_PARA	R/W	13:0	0085H	Specify the interval to turn on the power corresponding to bits PR_PWSW[15:8]. (Specified value + 1) × HFB cycle time

### 3.2.302 CPU RAM power switch register

This register (CPU\_PWSW\_L2RAM: E011\_098CH) specifies whether to turn on or off the L2 cache domain power by using the CPU.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:8	–	Reserved. If these bits are read, 0 is returned for each bit.
PC_L2_PSW	R/W	7:0	00H	Specify whether to turn on or off the L2 cache domain power switch. 0 : Cache power sw on 1 : Cache power sw off

The value disappears by power supply off because L2RAM isn't using retention RAM. When turning off a power supply of L2RAM, CLEAN (&INVALIDATE) has to do L2.

### 3.2.303 CPU logic power switch register

This register (CPU\_PWSW\_LOGIC: E011\_0990H) specifies whether to turn on or off the logic circuit power by using the CPU.

31	30	29	28	27	26	25	24
Reserved				PWSW_ARM_LOGIC_NE1_L4			
23	22	21	20	19	18	17	16
PWSW_ARM_LOGIC_NE0_L4				PWSW_ARM_LOGIC_PE1_L3			
15	14	13	12	11	10	9	8
PWSW_ARM_LOGIC_PE0_L3				PWSW_ARM_LOGIC_DS1_L2			
7	6	5	4	3	2	1	0
PWSW_ARM_LOGIC_DS0_L2				PWSW_ARM_LOGIC_HM_L1			

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:28	–	Reserved. If these bits are read, 0 is returned for each bit.
PWSW_ARM_LOGIC_NE1_L4	R/W	27:24	0H	Specify whether to turn on or off the logic power.
PWSW_ARM_LOGIC_NE0_L4	R/W	23:20	0H	Specify whether to turn on or off the logic power.
PWSW_ARM_LOGIC_PE1_L3	R/W	19:16	0H	Specify whether to turn on or off the logic power.
PWSW_ARM_LOGIC_PE0_L3	R/W	15:12	0H	Specify whether to turn on or off the logic power.
PWSW_ARM_LOGIC_DS1_L2	R/W	11:8	0H	Specify whether to turn on or off the logic power.
PWSW_ARM_LOGIC_DS0_L2	R/W	7:4	0H	Specify whether to turn on or off the logic power.
PWSW_ARM_LOGIC_HM_L1	R/W	3:0	0H	Specify whether to turn on or off the logic power.

**Remark** 0: On, 1: Off

### 3.2.304 CPU RAM power switch register

This register (CPU\_PWSW\_L1RAM: E011\_0994H) controls the RAM power switching by the CPU.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved		PWSW_ARM_ETBRAM_HM_L 1		PWSW_ARM_L1RAM_PE1_L3				
15	14	13	12	11	10	9	8	
PWSW_ARM_L1RAM_PE0_L3				PWSW_ARM_L1RAM_DS1_L2				
7	6	5	4	3	2	1	0	
PWSW_ARM_L1RAM_DS0_L2				PWSW_ARM_SCURAM1_HM_ L1	PWSW_ARM_SCURAM0_HM_ L1			

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:22	–	Reserved. If these bits are read, 0 is returned for each bit.
PWSW_ARM_ETBRAM_HM_L1	R/W	21:20	0H	Specify whether to turn on or off the ETBRAM power.
PWSW_ARM_L1RAM_PE1_L3	R/W	19:16	0H	Specify whether to turn on or off the PE1 L1RAM power.
PWSW_ARM_L1RAM_PE0_L3	R/W	15:12	0H	Specify whether to turn on or off the PE0 L1RAM power.
PWSW_ARM_L1RAM_DS1_L2	R/W	11:8	0H	Specify whether to turn on or off the DS1 L1RAM power.
PWSW_ARM_L1RAM_DS0_L2	R/W	7:4	0H	Specify whether to turn on or off the DS0 L1RAM power.
PWSW_ARM_SCURAM1_HM_L1	R/W	3:2	0H	Specify whether to turn on or off the SCU L1RAM power.
PWSW_ARM_SCURAM0_HM_L1	R/W	1:0	0H	Specify whether to turn on or off the SCU L1RAM power.

**Remark** 0: On, 1: Off

### 3.2.305 CPU RAM PD control register

This register (CPU\_SRAM\_PD: E011\_0998H) controls the RAM cell power switching by the CPU.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved	PD_ETBRAM_L0	PD_BTAC_PE_RAM1_L0	PD_BTAC_PERAM0_L0	PD_DC0_DSR_AM1_L0	PD_DC0_DSRAM0_L0	PD_DC1_DSRAM1_L0	PD_DC1_DSRAM0_L0
15	14	13	12	11	10	9	8
PD_DOUTER_DSRAM1_L0	PD_DOUTER_DSRAM0_L0	PD_DT_DSRAM1_L0	PD_DT_DSRAM0_L0	PD_GHB_PERAM1_L0	PD_GHB_PERAM0_L0	PD_IC0_PERAM1_L0	PD_IC0_PERAM0_L0
7	6	5	4	3	2	1	0
PD_IC1_PERAM1_L0	PD_IC1_PERAM0_L0	PD_IT_PERAM1_L0	PD_IT_PERAM0_L0	PD_SCU_DSRAM1_L0	PD_SCU_DSRAM0_L0	PD_TLB_DSRAM1_L0	PD_TLB_DSRAM0_L0

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:23	–	Reserved. If these bits are read, 0 is returned for each bit.
PD_ETBRAM_L0	R/W	22	0	RAM cell power switch
PD_BTAC_PERAM1_L0	R/W	21	0	RAM cell power switch
PD_BTAC_PERAM0_L0	R/W	20	0	RAM cell power switch
PD_DC0_DSRAM1_L0	R/W	19	0	RAM cell power switch
PD_DC0_DSRAM0_L0	R/W	18	0	RAM cell power switch
PD_DC1_DSRAM1_L0	R/W	17	0	RAM cell power switch
PD_DC1_DSRAM0_L0	R/W	16	0	RAM cell power switch
PD_DOUTER_DSRAM1_L0	R/W	15	0	RAM cell power switch
PD_DOUTER_DSRAM0_L0	R/W	14	0	RAM cell power switch
PD_DT_DSRAM1_L0	R/W	13	0	RAM cell power switch
PD_DT_DSRAM0_L0	R/W	12	0	RAM cell power switch
PD_GHB_PERAM1_L0	R/W	11	0	RAM cell power switch
PD_GHB_PERAM0_L0	R/W	10	0	RAM cell power switch
PD_IC0_PERAM1_L0	R/W	9	0	RAM cell power switch
PD_IC0_PERAM0_L0	R/W	8	0	RAM cell power switch
PD_IC1_PERAM1_L0	R/W	7	0	RAM cell power switch
PD_IC1_PERAM0_L0	R/W	6	0	RAM cell power switch
PD_IT_PERAM1_L0	R/W	5	0	RAM cell power switch
PD_IT_PERAM0_L0	R/W	4	0	RAM cell power switch
PD_SCU_DSRAM1_L0	R/W	3	0	RAM cell power switch

(2/2)

Name	R/W	Bit No.	After Reset	Description
PD_SCU_DSRAM0_L0	R/W	2	0	RAM cell power switch
PD_TLB_DSRAM1_L0	R/W	1	0	RAM cell power switch
PD_TLB_DSRAM0_L0	R/W	0	0	RAM cell power switch

### 3.2.306 CPU power switch control register

This register (CPU\_PWSW\_CTRL: E011\_099CH) controls the signals sent from the CPU to BUS1.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				PC_L2_BUN	PC_LAT	PC_BUN	

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:3	–	Reserved. If these bits are read, 0 is returned for each bit.
PC_L2_BUN	R/W	2	1	Specify whether to enable the ISO signal sent from the L2 cache.
PC_LAT	R/W	1	1	Specify whether to enable the LAT signal sent from the CPU to BUS1.
PC_BUN	R/W	0	1	Specify whether to enable the ISO signal sent from the CPU to BUS1.

**Remark** 0: Enable, 1: Disable

### 3.2.307 CPU power status register

This register (CPU\_POWER\_STATUS: E011\_09A0H) shows the CPU power status.

31	30	29	28	27	26	25	24
Reserved						NE1_PWR STATUS	
23	22	21	20	19	18	17	16
Reserved		NE0_PWR STATUS	Reserved			PE1_PWR STATUS	
15	14	13	12	11	10	9	8
Reserved		PE0_PWR STATUS	Reserved			DS1_PWR STATUS	
7	6	5	4	3	2	1	0
Reserved		DS0_PWR STATUS	Reserved			HM_PWR STATUS	

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:25	–	Reserved. If these bits are read, 0 is returned for each bit.
NE1_PWRSTATUS	R	24	0	Indicates the NE1 power status.
Reserved	R	23:21	–	Reserved. If these bits are read, 0 is returned for each bit.
NE0_PWRSTATUS	R	20	0	Indicates the NE0 power status.
Reserved	R	19:17	–	Reserved. If these bits are read, 0 is returned for each bit.
PE1_PWRSTATUS	R	16	0	Indicates the PE1 power status.
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
PE0_PWRSTATUS	R	12	0	Indicates the PE0 power status.
Reserved	R	11:9	–	Reserved. If these bits are read, 0 is returned for each bit.
DS1_PWRSTATUS	R	8	0	Indicates the DS1 power status.
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.
DS0_PWRSTATUS	R	4	0	Indicates the DS0 power status.
Reserved	R	3:1	–	Reserved. If these bits are read, 0 is returned for each bit.
HM_PWRSTATUS	R	0	0	Indicates the HM power status.

**Remark** 0: On, 1: Off

### 3.2.308 CPU power switch sequencer status register

This register (CPU\_SEQ\_BUSY: E011\_09A4H) shows the power switch sequencer transition status.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved	NE1_MODE_ACTIVE	NE0_MODE_ACTIVE	PE1_MODE_ACTIVE	PE0_MODE_ACTIVE	DS1_MODE_ACTIVE	DS0_MODE_ACTIVE	HM_MODE_ACTIVE
7	6	5	4	3	2	1	0
Reserved	NE1_SEQ_BUSY	NE0_SEQ_BUSY	PE1_SEQ_BUSY	PE0_SEQ_BUSY	DS1_SEQ_BUSY	DS0_SEQ_BUSY	HM_SEQ_BUSY

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:15	–	Reserved. If these bits are read, 0 is returned for each bit.
NE1_MODE_ACTIVE	R	14	0	Indicates the transition of the NE1 power switch control sequencer. 0: Off to on 1: On to off
NE0_MODE_ACTIVE	R	13	0	Indicates the transition of the NE0 power switch control sequencer. 0: Off to on 1: On to off
PE1_MODE_ACTIVE	R	12	0	Indicates the transition of the PE1 power switch control sequencer. 0: Off to on 1: On to off
PE0_MODE_ACTIVE	R	11	0	Indicates the transition of the PE0 power switch control sequencer. 0: Off to on 1: On to off
DS1_MODE_ACTIVE	R	10	0	Indicates the transition of the DS1 power switch control sequencer. 0: Off to on 1: On to off
DS0_MODE_ACTIVE	R	9	0	Indicates the transition of the DS0 power switch control sequencer. 0: Off to on 1: On to off
HM_MODE_ACTIVE	R	8	0	Indicates the transition of the HM power switch control sequencer. 0: Off to on 1: On to off
Reserved	R	7	–	Reserved. If this bit is read, 0 is returned.

(2/2)

Name	R/W	Bit No.	After Reset	Description
NE1_SEQ_BUSY	R	6	0	Indicates the NE1 power switch control sequencer. 0: Stopped 1: Running.
NE0_SEQ_BUSY	R	5	0	Indicates the NE0 power switch control sequencer. 0: Stopped 1: Running.
PE1_SEQ_BUSY	R	4	0	Indicates the PE1 power switch control sequencer. 0: Stopped 1: Running.
PE0_SEQ_BUSY	R	3	0	Indicates the PE0 power switch control sequencer. 0: Stopped 1: Running.
DS1_SEQ_BUSY	R	2	0	Indicates the DS1 power switch control sequencer. 0: Stopped 1: Running.
DS0_SEQ_BUSY	R	1	0	Indicates the DS0 power switch control sequencer. 0: Stopped 1: Running.
HM_SEQ_BUSY	R	0	0	Indicates the transition of the HM power switch control sequencer. 0: Stopped 1: Running.

### 3.2.309 QR\_WFE setting register

This register (QR\_WFE: E011\_09B4H) specifies the WFE mode of the QR module.

31	30	29	28	27	26	25	24		
Reserved									
23	22	21	20	19	18	17	16		
Reserved									
15	14	13	12	11	10	9	8		
Reserved									
7	6	5	4	3	2	1	0		
Reserved						DEEPSLEEP_WFE			
Name	R/W	Bit No.	After Reset	Description					
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.					
DEEPSLEEP_WFE	R/W	1:0	0H	A QR mode of WFE is chosen. 0 : LightSleep_QR 1 : DeepSleep_QR [0] CPU0 [1] CPU1					

Before and after CPU0/1 enters WFE, it's possible to change to LightSleep\_QR and DeepSleep\_QR by establishing this register. (Always, selectable)

### 3.2.310 QR\_WFI setting register

This register (QR\_WFI: E011\_09B8H) specifies the WFI mode of the QR module.

31	30	29	28	27	26	25	24		
Reserved									
23	22	21	20	19	18	17	16		
Reserved									
15	14	13	12	11	10	9	8		
Reserved									
7	6	5	4	3	2	1	0		
Reserved						DEEPSLEEP_WFI			
Name	R/W	Bit No.	After Reset	Description					
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.					
DEEPSLEEP_WFI	R/W	1:0	0H	A QR mode of WFI is chosen. 0 : LightSleep_QR 1 : DeepSleep_QR [0] CPU0 [1] CPU1					

Before and after CPU0/1 enters WFI, it's possible to change to LightSleep\_QR and DeepSleep\_QR by establishing this register. (Always, selectable)

### 3.2.311 CPU NEON enable register

This register (CPU\_NEON\_ENABLE: E011\_09BCH) sets the PD\_NE power supply.

31	30	29	28	27	26	25	24		
Reserved									
23	22	21	20	19	18	17	16		
Reserved									
15	14	13	12	11	10	9	8		
Reserved									
7	6	5	4	3	2	1	0		
Reserved						NEON_ENABLE			
Name	R/W	Bit No.	After Reset	Description					
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.					
NEON_ENABLE	R/W	1:0	3H	Control PD_NE power supply. Bit[1] : CPU1 Bit[0] : CPU0 0: Anytime power off. 1: Follow setting of QR_WFE or QR_WFI.					

When not using a NEON order, establish “0” to reduce a leak of PD\_NE.

A power supply of a PD\_NEn is polled by CLKSTOPSIG\_ST (0xE011\_06F0) in case of a NEON power supply change, and it's necessary to confirm that a power supply was switched over. (Except for return about WFE/WFI return factor) this register is always selectable.

### 3.2.312 QR\_DSIDEOFF setting register

This register (QR\_DSIDEOFF: E011\_09C4H) changes PD\_DS to DeepSleep\_QR.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						DSIDE_OFF	
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.			
DSIDE_OFF	R/W	1:0	0	Changes PD_DS to DeepSleep_QR . Bit[1] : CPU1 Bit[0] : CPU0 0: Anytime on. 1: It's changed dynamically			

When CPU was WFI by a SMP mode, it's possible to turn off a power supply of PD\_DS.

When there is a coherent request from other CPU, a power supply of PD\_DS is turned on.

That DSIDEOFF is set as “1”, of a coherent request, a degree, to change power supply on/off, there is a fear that the performance falls.

This register combines with CPU\_COH (0xE011\_0A70) and uses.

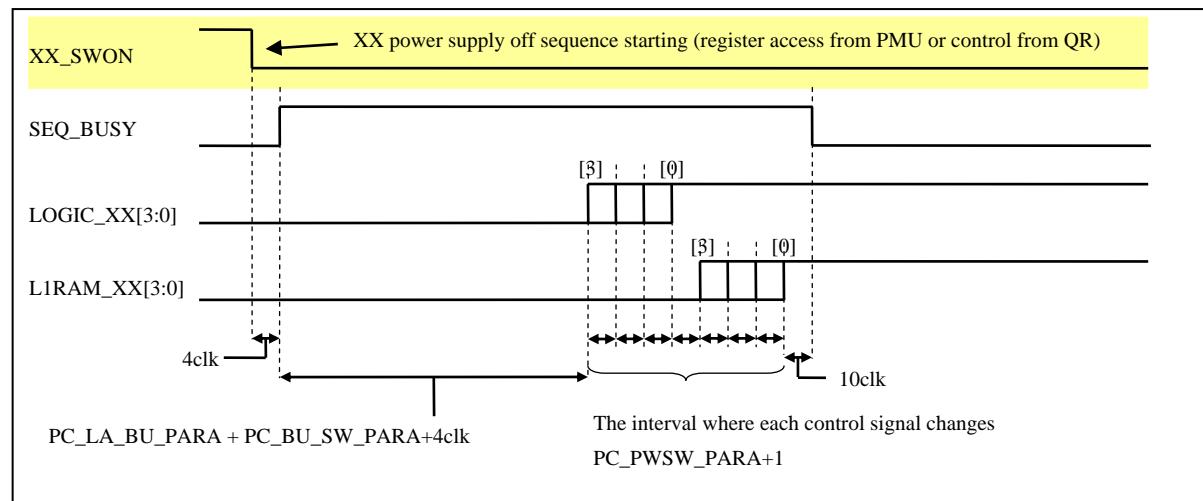
### 3.2.313 CPU DS0 power automatic control register

This register (DS0\_SWON: E011\_09D0H) sets up automatic DS0 power switching.

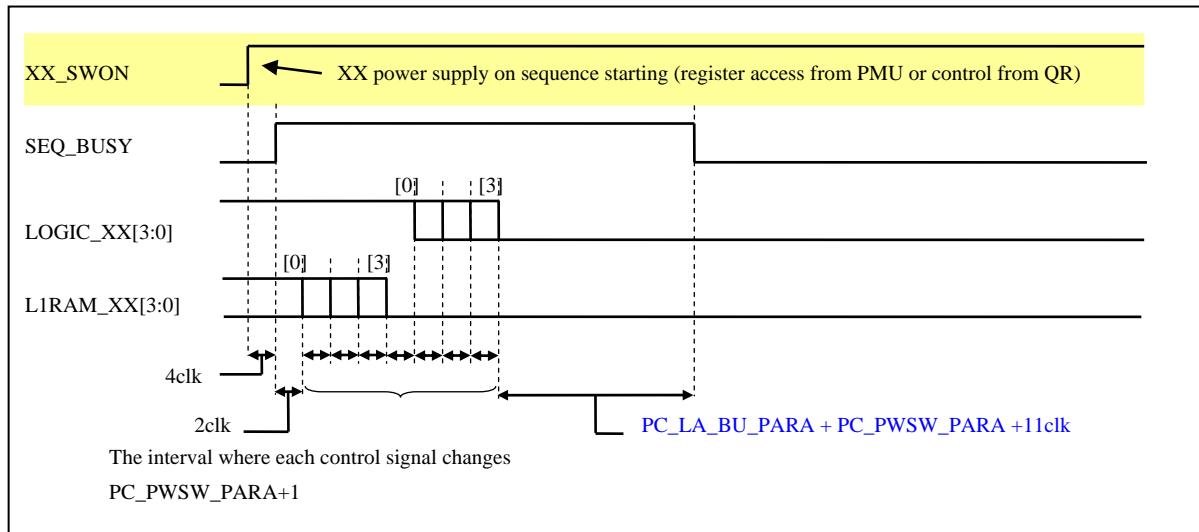
31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								
7	6	5	4	3	2	1	0	
Reserved								DS0_SWON

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
DS0_SWON	R/W	0	1	Control automatic DS0 power switching. Read the DS0_PWSW_STATUS bit to determine completion of the sequence. 0: Start the sequence for turning off the DS0 power. 1: Start the sequence for turning on the DS0 power.

DS0\_L2,DS1\_L2,PE0\_L3,PE1\_L3 power supply SW automatic transfer operation (off Sequence).



DS0\_L2,DS1\_L2,PE0\_L3,PE1\_L3 power supply SW automatic transfer operation (on Sequence).



### 3.2.314 CPU DS1 power automatic control register

This register (DS1\_SWON: E011\_09D4H) sets up automatic DS1 power switching.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							DS1_SWON

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
DS1_SWON	R/W	0	1	Control automatic DS1 power switching. Read the DS1_PWSW_STATUS bit to determine completion of the sequence. 0: Start the sequence for turning off the DS1 power. 1: Start the sequence for turning on the DS1 power.

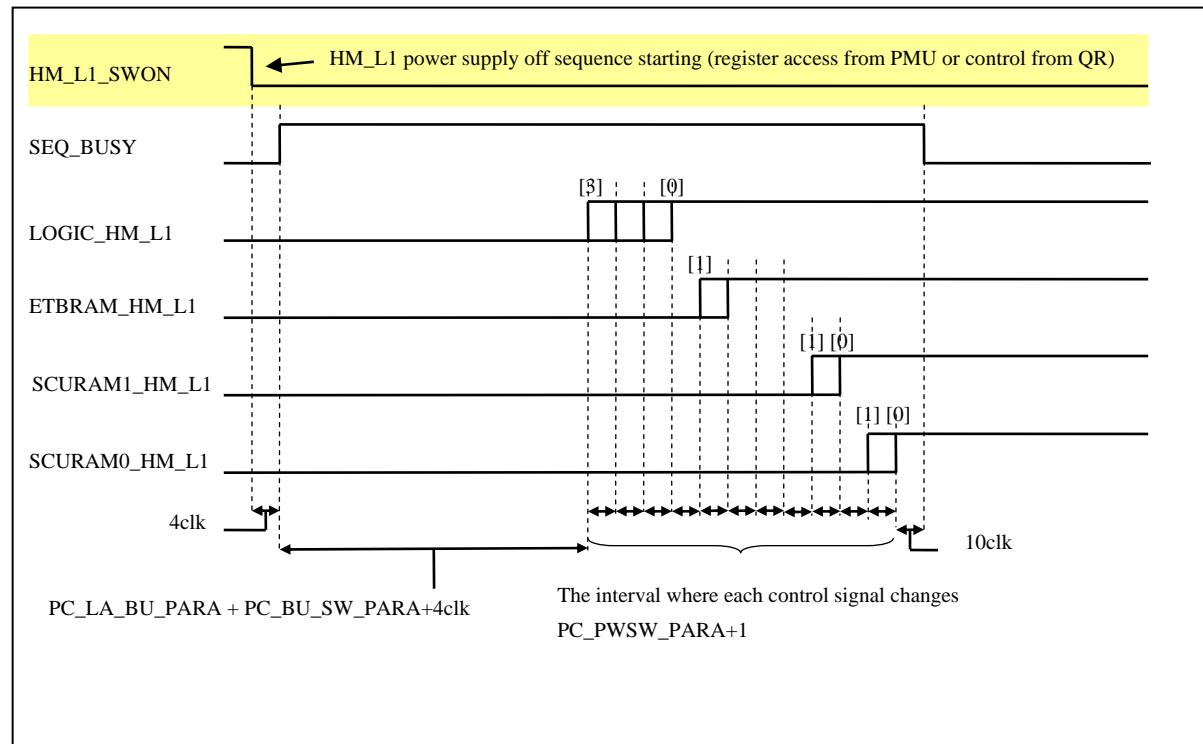
### 3.2.315 CPU HM power automatic control register

This register (HM\_SWON: E011\_09D8H) sets up automatic HM power switching.

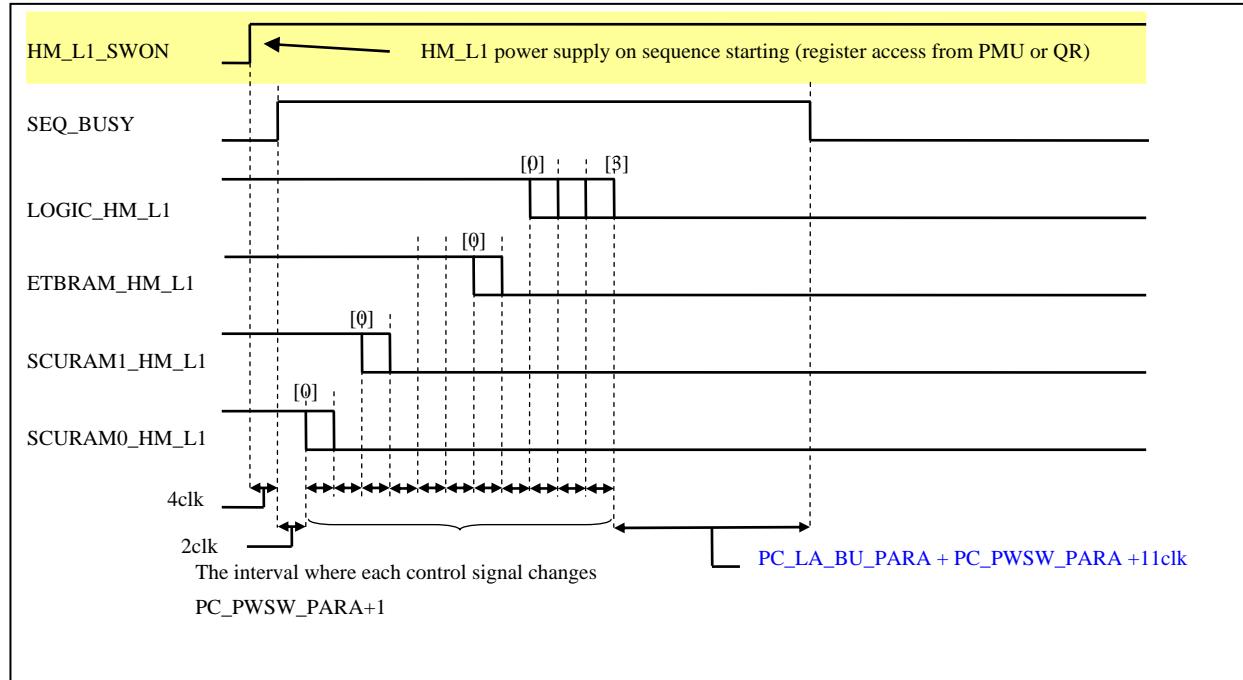
31	30	29	28	27	26	25	24	Reserved
23	22	21	20	19	18	17	16	Reserved
15	14	13	12	11	10	9	8	Reserved
7	6	5	4	3	2	1	0	Reserved
								HM_SWON

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
HM_SWON	R/W	0	1	Control automatic HM power switching. Read the HM_PWSW_STATUS bit to determine completion of the sequence. 0: Start the sequence for turning off the HM power. 1: Start the sequence for turning on the HM power.

HM\_L1 power supply SW automatic transfer operation (off Sequence)



HM\_L1 power supply SW automatic transfer operation (on Sequence)



### 3.2.316 CPU PE0 power automatic control register

This register (PE0\_SWON: E011\_09DCH) sets up automatic PE0 power switching.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								
7	6	5	4	3	2	1	0	
Reserved								PE0_SWON
Name	R/W	Bit No.	After Reset	Description				
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.				
PE0_SWON	R/W	0	1	Control automatic PE0 power switching. Read the PE0_PWSW_STATUS bit to determine completion of the sequence. 0: Start the sequence for turning off the PE0 power. 1: Start the sequence for turning on the PE0 power.				

### 3.2.317 CPU PE1 power automatic control register

This register (PE1\_SWON: E011\_09E0H) sets up automatic PE1 power switching.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							PE1_SWON

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
PE1_SWON	R/W	0	1	Control automatic PE1 power switching. Read the PE1_PWSW_STATUS bit to determine completion of the sequence. 0: Start the sequence for turning off the PE1 power. 1: Start the sequence for turning on the PE1 power.

### 3.2.318 CPU NE0 power automatic control register

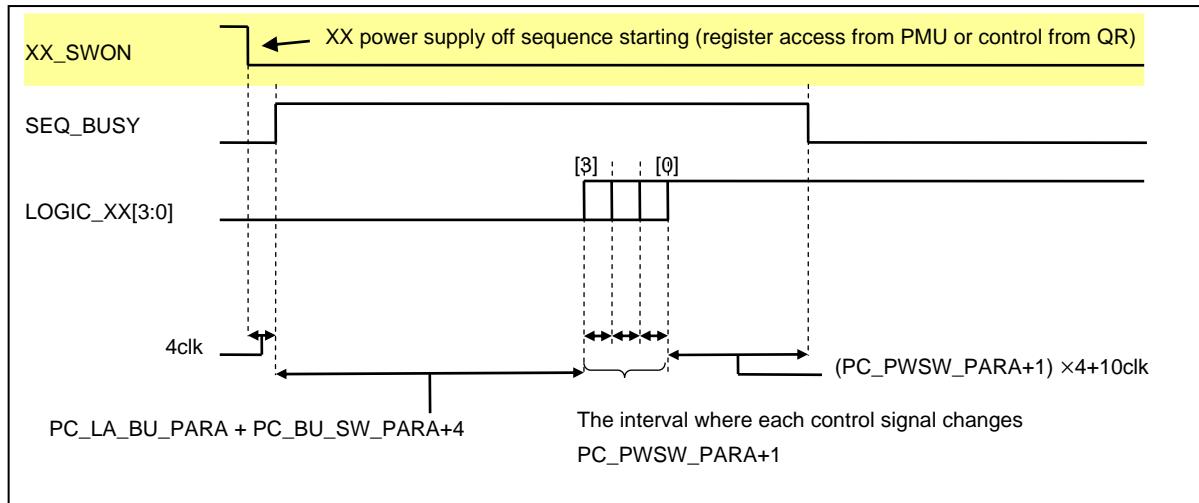
This register (NE0\_SWON: E011\_09E4H) sets up automatic NE0 power switching.

31	30	29	28	27	26	25	24	Reserved
23	22	21	20	19	18	17	16	Reserved
15	14	13	12	11	10	9	8	Reserved
7	6	5	4	3	2	1	0	Reserved
								NE0_SWON

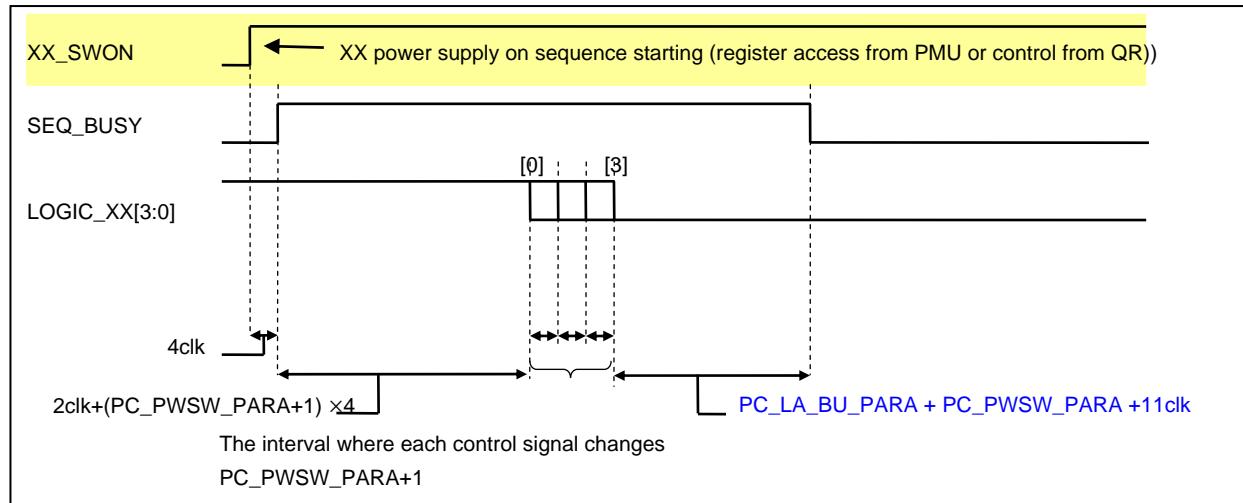
  

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
NE0_SWON	R/W	0	1	Control automatic NE0 power switching. Read the NEO_PWSW_STATUS bit to determine completion of the sequence. 0: Start the sequence for turning off the NE0 power. 1: Start the sequence for turning on the NE0 power.

NE0\_L2 power supply SW automatic transfer operation (off Sequence)



NE0\_L2 power supply SW automatic transfer operation (on Sequence)



### 3.2.319 CPU NE1 power automatic control register

This register (NE1\_SWON: E011\_09E8H) sets up automatic NE1 power switching.

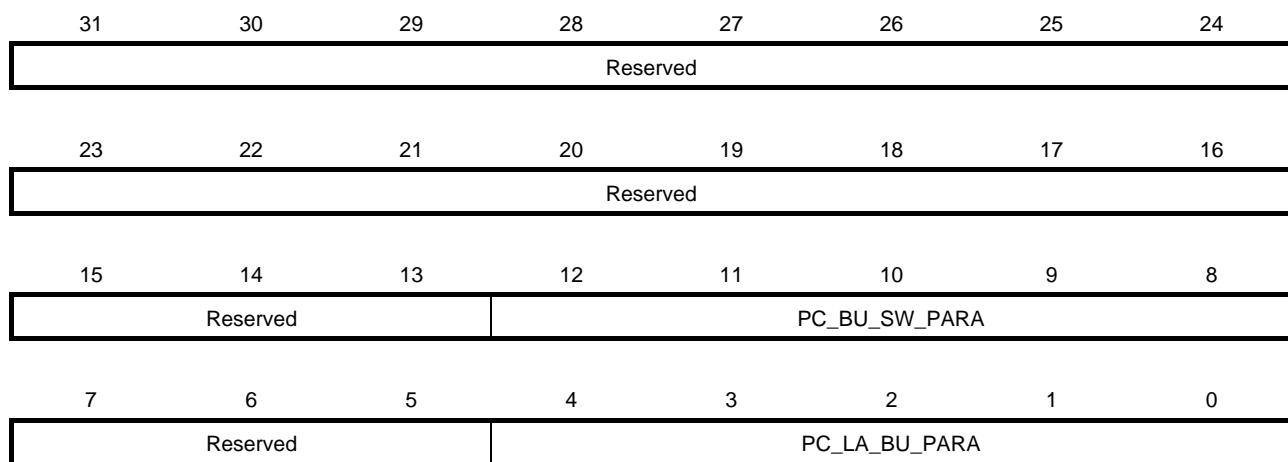
31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							NE1_SWON

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
NE1_SWON	R/W	0	1	Control automatic NE1 power switching. Read the NE1_PWSW_STATUS bit to determine completion of the sequence. 0: Start the sequence for turning off the NE1 power. 1: Start the sequence for turning on the NE1 power.

### 3.2.320 PC power RFF control parameter register 0

This register (PC\_RFF\_PARA0: E011\_09ECH) specifies the interval of inputting the control signal for the PC power retention F/F.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:13	–	Reserved. If these bits are read, 0 is returned for each bit.
PC_BU_SW_PARA	R/W	12:8	04H	For Normal to Retention, specify the interval timer during from PC_BUN↓ to PSW (first off)↑. For Power Down to Normal, specify the interval timer during from PSW (last on) ↓ to PC_BUN↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)
Reserved	R	7:5	–	Reserved. If these bits are read, 0 is returned for each bit.
PC_LA_BU_PARA	R/W	4:0	04H	For Normal to Power Down, specify the interval timer during from PC_LAT↓ to PC_BUN↓. For Power Down to Normal, specify the interval timer during from PC_LAT↑ to PC_BUN↑. (Specified value + 1) × HFB cycle time (↑: Rise, ↓: Fall)

### 3.2.321 PC power switch control parameter register

This register (PC\_PWSW\_PARA: E011\_09F0H) specifies the PC power turn-on interval.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved				PC_PWSW_PARA			
7	6	5	4	3	2	1	0
PC_PWSW_PARA							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:14	–	Reserved. If these bits are read, 0 is returned for each bit.			
PC_PWSW_PARA	R/W	13:0	0085H	Specify the interval to turn on the power for logic circuits and RAM in the PC domain. (Specified value + 1) × HFB cycle time			

### 3.2.322 QR\_WAIT count setting register

This register (QR\_WAITCNT: E011\_09F4H) specifies the asserting period of a retention control signal .

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved	BUZASTWAIT			Reserved	BUZDEASTWAIT			
15	14	13	12	11	10	9	8	
Reserved	NRETAINASTWAIT			Reserved	NRETAINDEASTWAIT			
7	6	5	4	3	2	1	0	
Reserved	RAMBUNASTWAIT			Reserved	RAMBUNDEASTWAIT			
Name	R/W	Bit No.	After Reset	Description				
Reserved	R	31:23	–	Reserved. If these bits are read, 0 is returned for each bit.				
BUZASTWAIT	R/W	22:20	0H	Specify the asserting period of a retention control signal				
Reserved	R	19	–	Reserved. If this bit is read, 0 is returned.				
BUZDEASTWAIT	R/W	18:16	0H	Specify the asserting period of a retention control signal				
Reserved	R	15	–	Reserved. If this bit is read, 0 is returned.				
NRETAINASTWAIT	R/W	14:12	0H	Specify the asserting period of a retention control signal				
Reserved	R	11	–	Reserved. If this bit is read, 0 is returned.				
NRETAINDEASTWAIT	R/W	10:8	0H	Specify the asserting period of a retention control signal				
Reserved	R	7	–	Reserved. If this bit is read, 0 is returned.				
RAMBUNASTWAIT	R/W	6:4	0H	Specify the asserting period of a retention control signal				
Reserved	R	3	–	Reserved. If this bit is read, 0 is returned.				
RAMBUNDEASTWAIT	R/W	2:0	0H	Specify the asserting period of a retention control signal				

### 3.2.323 PMU interrupt source control register

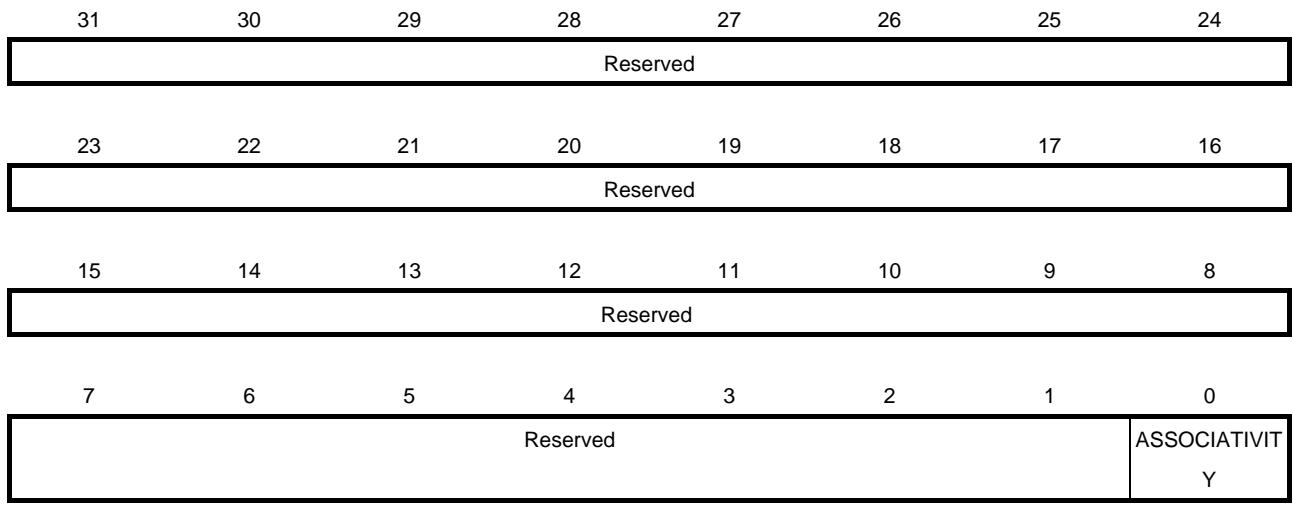
This register (PMU\_INTCTRL: E011\_0A30H) indicates the status of controlling interrupt sources by using the PMU.

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								
7	6	5	4	3	2	1	0	
Reserved								PMU_INTCTRL

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
PMU_INTCTRL	R/W	0	0	Indicates the status of controlling interrupt sources by using the PMU. 0: The PMU is not controlling interrupts. (Interrupt through) 1: The PMU is controlling interrupts. (Masked in PMU) This bit is set to 1 when the PMU starts controlling interrupts for the CPU.

### 3.2.324 CPU ASSOCIATIVITY setting register

This register (CPU\_ASSOCIATIVITY: E011\_0A4CH) specifies the structure of the L2RAM.



Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
ASSOCIATIVITY	R/W	0	0	Specify the structure of the L2RAM 0: 8way 1: 16way The following setting is possible because it's equipped with L2RAM 256 KB. 8way × 16KB = 128KB 8way × 32KB = 256KB 16way × 16KB = 256KB

### 3.2.325 CPU WAYSIZE setting register

This register (CPU\_WAYSIZE: E011\_0A50H) specifies the structure of the L2RAM.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						WAYSIZE	

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:3	–	Reserved. If these bits are read, 0 is returned for each bit.
WAYSIZE	R/W	2:0	010b	Specify the structure of the L2RAM 000: 16KB 001: 16KB 010 : 32KB The following setting is possible because it's equipped with L2RAM 256 KB. 8way × 16KB = 128KB 8way × 32KB = 256KB 16way × 16KB = 256KB

### 3.2.326 CPU CFGADDRSET setting register

This register (CPU\_CFGADDRSET: E011\_0A54H) specifies the PL310.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						CFGBIGEND	CFGADDRFILTEN

Name	R/W	Bit No.	After Reset	Description				
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.				
CFGBIGEND	R/W	1	0	BIGENDIAN setting of PL310. Use by 0 fixing.				
CFGADDRFILTEN	R/W	0	0	PL310 address filter Enable.				

### 3.2.327 CPU CFGADDRFILT setting register

This register (CPU\_CFGADDRFILT: E011\_0A58H) specifies the PL310 filter.

31	30	29	28	27	26	25	24
Reserved				CFGADDRFILTEND			
23	22	21	20	19	18	17	16
CFGADDRFILTEND							
15	14	13	12	11	10	9	8
Reserved				CFGADDRFILTSTART			
7	6	5	4	3	2	1	0
CFGADDRFILTSTART							

Name	R/W	Bit No.	After Reset	Description				
Reserved	R	31:28	–	Reserved. If these bits are read, 0 is returned for each bit.				
CFGADDRFILTEND	R/W	27:16	000H	Specify the END address [31:20] of PL310 filter				
Reserved	R	15:12	–	Reserved. If these bits are read, 0 is returned for each bit.				
CFGADDRFILTSTART	R/W	11:0	000H	Specify the START address [31:20] of PL310 filter				

### 3.2.328 CPU SCU address filter enable register

This register (CPU\_FILTEREN: E011\_0A60H) enables the SCU address filter.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							
FILTEREN							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
FILTEREN	R/W	0	0	SCU address filter enable.			

### 3.2.329 CPU SCU access address setting register

This register (CPU\_FILTERADDR: E011\_0A64H) specifies the SCU filter.

31	30	29	28	27	26	25	24
Reserved				FILTEREND			
23	22	21	20	19	18	17	16
FILTEREND							
15	14	13	12	11	10	9	8
Reserved				FILTERSTART			
7	6	5	4	3	2	1	0
FILTERSTART							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:28	–	Reserved. If these bits are read, 0 is returned for each bit.			
FILTEREND	R/W	27:16	000H	Specify the END address [31:20] of SCU filter			
Reserved	R	15:12	–	Reserved. If these bits are read, 0 is returned for each bit.			
FILTERSTART	R/W	11:0	000H	Specify the START address [31:20] of SCU filter			

### 3.2.330 CPU COHsetting register

This register (CPU\_COH: E011\_0A70H) specifies the COH..

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							DISCOHOFF
7	6	5	4	3	2	1	0
COH_COUNT_VAL							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:9	–	Reserved. If these bits are read, 0 is returned for each bit.			
DICCOHOFF	R/W	8	0	0: This function off. 1 : This function on			
COH_COUNT_VAL	R/W	7:0	00H	The period power supply off doesn't do is set after a coherent request disappears. (At most 0xFF)			

### 3.2.331 ICEREG\_DATA[31:0] read register

This register (ICEREG\_DATA0: E011\_0AE0H) is used to read ICEREG\_DATA.

31	30	29	28	27	26	25	24
ICEREG_DATA0							
23	22	21	20	19	18	17	16
ICEREG_DATA0							
15	14	13	12	11	10	9	8
ICEREG_DATA0							
7	6	5	4	3	2	1	0
ICEREG_DATA0							
Name	R/W	Bit No.	After Reset	Description			
ICEREG_DATA0	R	31:0	0000000H	Use these bits to read ICEREG_DATA[31:0].			

### 3.2.332 ICEREG\_DATA[63:32] read register

This register (ICEREG\_DATA1: E011\_0AE4H) is used to read ICEREG\_DATA.

31	30	29	28	27	26	25	24
ICEREG_DATA1							
23	22	21	20	19	18	17	16
ICEREG_DATA1							
15	14	13	12	11	10	9	8
ICEREG_DATA1							
7	6	5	4	3	2	1	0
ICEREG_DATA1							
Name	R/W	Bit No.	After Reset	Description			
ICEREG_DATA1	R	31:0	00000000H	Use these bits to read ICEREG_DATA[63:32].			

### 3.2.333 ICEREG\_DATA[95:64] read register

This register (ICEREG\_DATA2: E011\_0AE8H) is used to read ICEREG\_DATA.

31	30	29	28	27	26	25	24
ICEREG_DATA2							
23	22	21	20	19	18	17	16
ICEREG_DATA2							
15	14	13	12	11	10	9	8
ICEREG_DATA2							
7	6	5	4	3	2	1	0
ICEREG_DATA2							
Name	R/W	Bit No.	After Reset	Description			
ICEREG_DATA2	R	31:0	00000000H	Use these bits to read ICEREG_DATA[95:64].			

### 3.2.334 ICEREG\_DATA[127:96] read register

This register (ICEREG\_DATA3: E011\_0AECH) is used to read ICEREG\_DATA.

31	30	29	28	27	26	25	24
ICEREG_DATA3							
23	22	21	20	19	18	17	16
ICEREG_DATA3							
15	14	13	12	11	10	9	8
ICEREG_DATA3							
7	6	5	4	3	2	1	0
ICEREG_DATA3							
Name	R/W	Bit No.	After Reset	Description			
ICEREG_DATA3	R	31:0	0000000H	Use these bits to read ICEREG_DATA[127:96].			

### 3.2.335 ICEREG\_DATA[159:128] read register

This register (ICEREG\_DATA4: E011\_0AF0H) is used to read ICEREG\_DATA.

31	30	29	28	27	26	25	24
ICEREG_DATA4							
23	22	21	20	19	18	17	16
ICEREG_DATA4							
15	14	13	12	11	10	9	8
ICEREG_DATA4							
7	6	5	4	3	2	1	0
ICEREG_DATA4							
Name	R/W	Bit No.	After Reset	Description			
ICEREG_DATA4	R	31:0	0000000H	Use these bits to read ICEREG_DATA[159:128].			

### 3.2.336 ICEREG\_DATA[191:160] read register

This register (ICEREG\_DATA5: E011\_0AF4H) is used to read ICEREG\_DATA.

31	30	29	28	27	26	25	24
ICEREG_DATA5							
23	22	21	20	19	18	17	16
ICEREG_DATA5							
15	14	13	12	11	10	9	8
ICEREG_DATA5							
7	6	5	4	3	2	1	0
ICEREG_DATA5							
Name	R/W	Bit No.	After Reset	Description			
ICEREG_DATA5	R	31:0	00000000H	Use these bits to read ICEREG_DATA[191:160].			

### 3.2.337 ICEREG\_DATA[223:192] read register

This register (ICEREG\_DATA6: E011\_0AF8H) is used to read ICEREG\_DATA.

31	30	29	28	27	26	25	24
ICEREG_DATA6							
23	22	21	20	19	18	17	16
ICEREG_DATA6							
15	14	13	12	11	10	9	8
ICEREG_DATA6							
7	6	5	4	3	2	1	0
ICEREG_DATA6							
Name	R/W	Bit No.	After Reset	Description			
ICEREG_DATA6	R	31:0	00000000H	Use these bits to read ICEREG_DATA[223:192].			

### 3.2.338 ICEREG\_DATA[255:224] read register

This register (ICEREG\_DATA7: E011\_0AFCH) is used to read ICEREG\_DATA.

31	30	29	28	27	26	25	24
ICEREG_DATA7							
23	22	21	20	19	18	17	16
ICEREG_DATA7							
15	14	13	12	11	10	9	8
ICEREG_DATA7							
7	6	5	4	3	2	1	0
ICEREG_DATA7							
Name	R/W	Bit No.	After Reset	Description			
ICEREG_DATA7	R	31:0	0000000H	Use these bits to read ICEREG_DATA[255:224].			

### 3.2.339 CP15S disable status register

This register (R\_CP15SDISABLE: E011\_0B00H) indicates the CP15S disabled status.

31	30	29	28	27	26	25	24
Reserved						R_SPUIDEN	
23	22	21	20	19	18	17	16
Reserved		R_SPUNIDEN		Reserved		R_SPIDEN	
15	14	13	12	11	10	9	8
Reserved						R_SPNIDEN	
7	6	5	4	3	2	1	0
Reserved						R_CP15SDISABLE	

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:26	–	Reserved. If these bits are read, 0 is returned for each bit.
R_SPUIDEN	R	25:24	1H	
Reserved	R	23:22	–	Reserved. If these bits are read, 0 is returned for each bit.
R_SPUNIDEN	R	21:20	1H	
Reserved	R	19:18	–	Reserved. If these bits are read, 0 is returned for each bit.
R_SPIDEN	R	17:16	1H	
Reserved	R	15:10	–	Reserved. If these bits are read, 0 is returned for each bit.
R_SPNIDEN	R	9:8	1H	
Reserved	R	7:2	–	Reserved. If these bits are read, 0 is returned for each bit.
R_CP15SDISABLE	R	1:0	0H	For reading CP15SDISABLE

### 3.2.340 SMU control register

This register (SMU\_CONTROL: E011\_100CH) control MEMCCLKFRQA.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved			MEMCCLKFR QA_CTRL	Reserved			

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:16	–	Reserved. If these bits are read, 0 is returned for each bit.
Reserved	R/W	15:5	000H	It can't be changed from defaults.
MEMCCLKFRQA_CTRL	R/W	4	0	The CLK control signal when being automatic frequency control When it's a domain source clock division mode, "1" is set. It's set with a table in NORMALA_DIV in case of a domain clock division mode.
Reserved	R/W	3:0	0H	It can't be changed from defaults.

### 3.2.341 Automatic frequency switch control REQMASK2 register

This register (CKRQMODE\_MASK2: E011\_1010H) specifies whether to switch the clock for each block automatically.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							PDMA_REQ MASK

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
Reserved	R/W	1	0	Reserved.
PDMA_REQMASK	R/W	0	0	Specify whether to enable automatic PDMA frequency switching.

**Remark** 0: Do not enable (setting ignored), 1: Enable

It's automatic frequency control judgment applying in Default.

### 3.2.342 MEMC handshake enable register

This register (MEMCHSENA\_AFRQ: E011\_1018H) specifies MEMC handshake permission during an automatic frequency control

31	30	29	28	27	26	25	24	
Reserved								
23	22	21	20	19	18	17	16	
Reserved								
15	14	13	12	11	10	9	8	
Reserved								
7	6	5	4	3	2	1	0	
Reserved								MEMCHSENA_AFRQ
Name	R/W	Bit No.	After Reset	Description				
Reserved	R	31:16	–	Reserved. If these bits are read, 0 is returned for each bit.				
Reserved	R/W	15:1	0000H	General purpose register				
MEMCHSENA_AFRQ	R/W	0	0	Specify MEMC handshake permission during an automatic frequency control 0 : Prohibition 1 : Permission				

During using Direct Path by LCD, set an automatic frequency control as performed case and  
MEMCHSENA\_AFRQ[0] = 0x1.

### 3.2.343 Chip revision register

This register (CHIP\_REVISION: E011\_2000H) shows the chip revision.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
CHIP_REV_7	CHIP_REV_6	CHIP_REV_5	CHIP_REV_4	CHIP_REV_3	CHIP_REV_2	CHIP_REV_1	CHIP_REV_0

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:8	–	Reserved. If these bits are read, 0 is returned for each bit.
CHIP_REV_7	R	7	0	Chip revision register
CHIP_REV_6	R	6	0	Chip revision register
CHIP_REV_5	R	5	1	Chip revision register
CHIP_REV_4	R	4	1	Chip revision register
CHIP_REV_3	R	3	0	Chip revision register
CHIP_REV_2	R	2	0	Chip revision register
CHIP_REV_1	R	1	0	Chip revision register
CHIP_REV_0	R	0	0	Chip revision register

### 3.2.344 CP15S disable setting register

This register (CP15SDISABLE: E020\_0000H) shows the CP15S disabled status. This register is allowed in the S2 domain.

31	30	29	28	27	26	25	24	
Reserved								SPUIDEN
23	22	21	20	19	18	17	16	
Reserved		SPUNIDEN		Reserved		SPIDEN		
15	14	13	12	11	10	9	8	
Reserved								SPNIDEN
7	6	5	4	3	2	1	0	
Reserved								CP15SDISABLE
Name	R/W	Bit No.	After Reset	Description				
Reserved	R	31:26	–	Reserved. If these bits are read, 0 is returned for each bit.				
SPUIDEN	R	25:24	1H	Setting values other than the initial value is prohibited.				
Reserved	R	23:22	–	Reserved. If these bits are read, 0 is returned for each bit.				
SPUNIDEN	R	21:20	1H	Setting values other than the initial value is prohibited.				
Reserved	R	19:18	–	Reserved. If these bits are read, 0 is returned for each bit.				
SPIDEN	R	17:16	1H	The setting for AFS is used as the initial value. Setting values other than the initial value is prohibited.				
Reserved	R	15:10	–	Reserved. If these bits are read, 0 is returned for each bit.				
SPNIDEN	R	9:8	1H	The setting for AFS is used as the initial value. Setting values other than the initial value is prohibited.				
Reserved	R	7:2	–	Reserved. If these bits are read, 0 is returned for each bit.				
CP15SDISABLE	R	1:0	0H	Setting values other than the initial value is prohibited.				

### 3.2.345 CPU SCU secure register protection setting register

This register (CPU\_CFGSDISABLE: E020\_0004H) specifies SCU secure register protection.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							
CFGSDISABLE							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
CFGSDISABLE	R/W	0	0	Disable writing to the secure registers for the SCU internal interrupt controller registers. After being initialized by PORSTZ and the boot sequence, set this bit to 1.			

### 3.2.346 INT\_TIMSEL control register

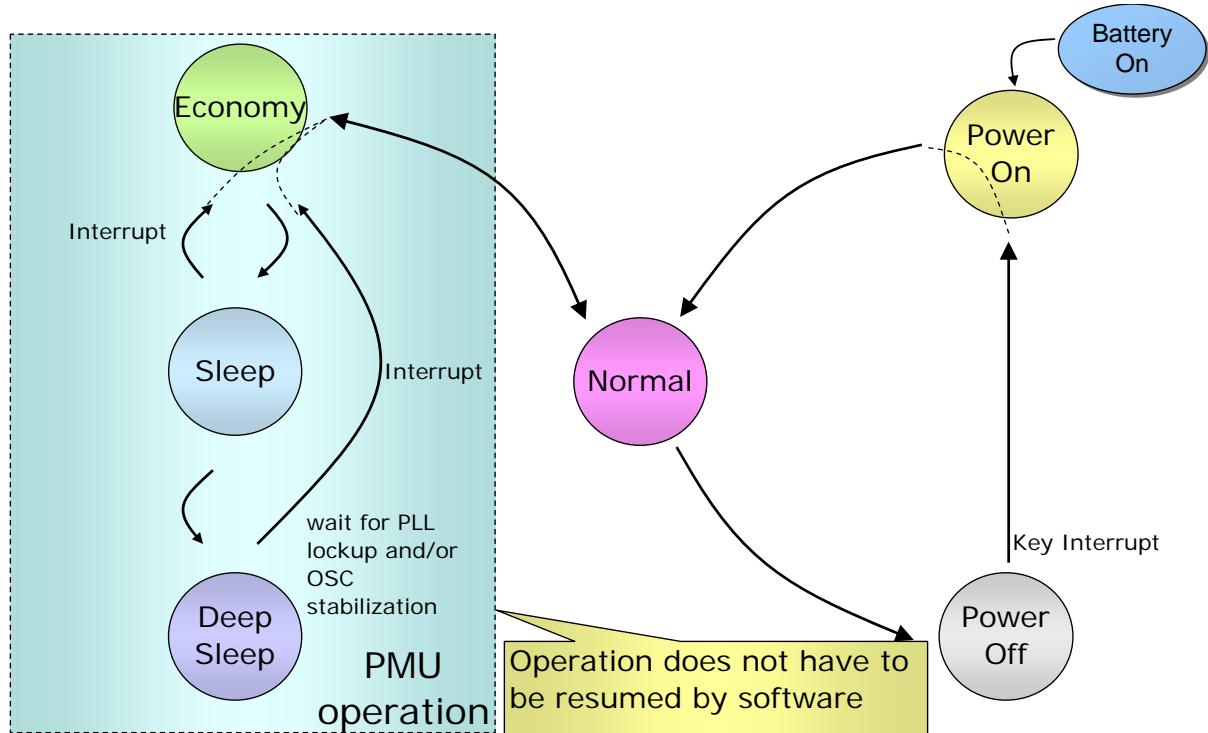
This register (INT\_TIMSEL: E020\_0008H) selects the interrupt timer to use.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							
INT_TIMSEL							
Name	R/W	Bit No.	After Reset	Description			
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.			
INT_TIMSEL	R/W	0	0	Select the interrupt timer to use: the one in the CPU or the one in INTA.			

## 4. Description of Functions

### 4.1 Status Transition

Figure 4-1. EM/EV Power Mode Transition



**Table 4-1. DDR2 Mode: Clock and V<sub>DD</sub> Conditions**

	<b>Power Mode</b>	<b>Power OFF</b>	<b>Deep Sleep</b>	<b>Sleep</b>	<b>Economy</b>	<b>Normal</b>	<b>Power ON</b>			
*value is a division ratio	CPU (Up to 533MHz)	– (WFI(QR) Power OFF)				1-16	16			
	FFB (Full-Freq-Bus) (Up to 266MHz)	– Power OFF	1	1-16	1-16	1-16	16			
	HFB (Half-Freq-Bus) (Up to 133MHz)	– Power OFF	1	1-16	1-16	1-16	16			
	DDR (Up to 266MHz)	Self Refresh (Power OFF)			1-16	1-16	16			
Power Supply	VDD11	OFF	0.75V	1.15V						
	On-chip SW	OFF			1.15V					
	IO	1.8V/3.3V (Always ON)								
	USB	OFF		OFF/3.3V						
Clock source		32.768KHz		OSC	PLL3	PLL1	PLL3			
	PLL1	VDD=0V		Standby		Run	Standby			
	PLL3	VDD=0V		Standby	Run					
	OSC 10-27MHz	Stop		Run			Stop			
LCD mode		Off			LCD direct	Normal/LCD direct				
Audio mode		Off		PCM direct		Normal/PCM direct				

**Table 4-2 LPDDR Mode : Clock and V<sub>DD</sub> Conditions**

	<b>Power Mode</b>	<b>Power OFF</b>	<b>Deep Sleep</b>	<b>Sleep</b>	<b>Economy</b>	<b>Normal</b>	<b>Power ON</b>			
*value is a division ratio	CPU (Up to 533MHz)	– (WFI(QR) Power OFF)				1-16	16			
	FFB (Full-Freq-Bus) (Up to 200MHz)	– Power OFF	1	1-16	1-16	1-16	16			
	HFB (Half-Freq-Bus) (Up to 133MHz)	– Power OFF	1	1-16	1-16	1-16	16			
	DDR (Up to 200MHz)	Self Refresh or Deep Power Down (Power OFF)			1-16	1-16	16			
Power Supply	VDD11	OFF	0.75V	1.15V						
	On-chip SW	OFF			1.15V					
	IO	1.8V/3.3V (Always ON)								
	USB	OFF		OFF/3.3V						
Clock source		32.768KHz		OSC	PLL3	PLL2	PLL3			
	PLL2	VDD=0V		Standby		Run	Standby			
	PLL3	VDD=0V		Standby	Run					
	OSC 10-27MHz	Stop		Run	Run/Stop		Stop			
LCD mode		Off			LCD direct	Normal/LCD direct				
Audio mode		Off		PCM direct		Normal/PCM direct				

## 4.2 PLL's

PLL1:

Clock frequency: 50 to 533 MHz

Used as the internal system clock.

The multiplication ratio is selectable.

(Before changing the multiplication ratio, change the clock source for the other PLLs.)

PLL2:

Clock frequency: 320 to 533 MHz

Used as the main clock in LPDDR mode.

The multiplication ratio is selectable.

(Before changing the multiplication ratio, change the clock source for the other PLLs.)

PLL3:

Clock frequency: 229.376 MHz (fixed)

Used as the system clock for peripherals and runs all the time.

PLL4:

Clock frequency: 320 to 533 MHz

OSC0:

Clock frequency: 10 to 27 MHz

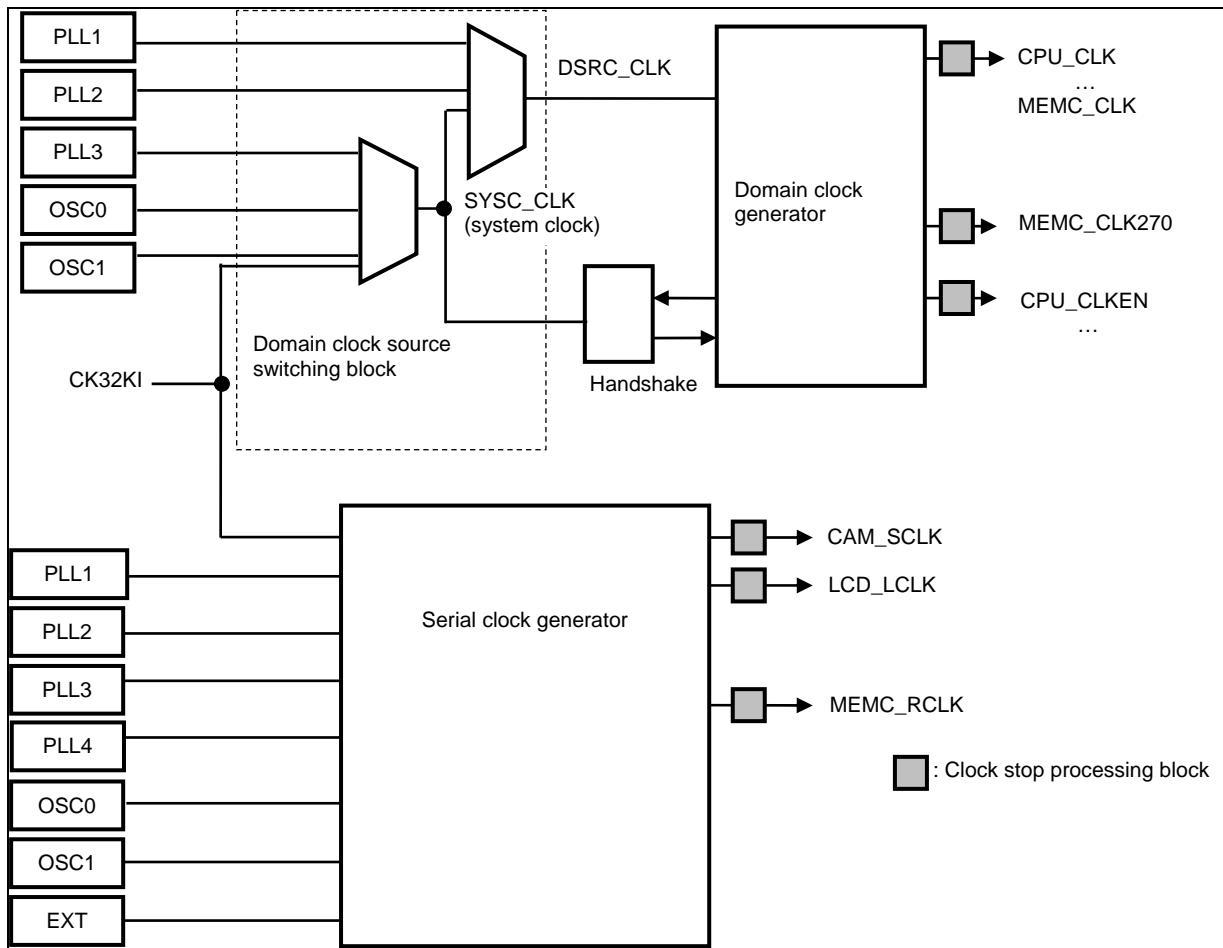
OSC1:

Clock frequency: 24 MHz

OSC1 is fixed to 24MHz in order to generate a clock of 480MHz for USB.

### 4.3 Clock System Overview

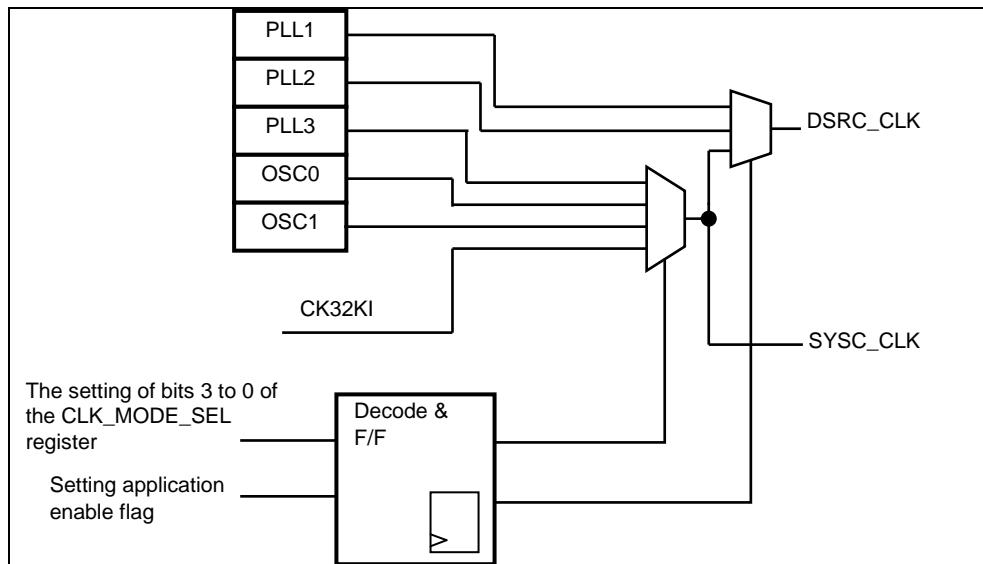
Figure 4-2. Clock System Overview



## 4.4 Domain Clock Source Switching Block

The clock used to generate the domain clock might need to be changed when a status transition occurs. The domain clock source switching block is where this change is executed. A diagram of the domain clock switching block is shown below.

**Figure 4-3. Domain Clock Source Switching Block**



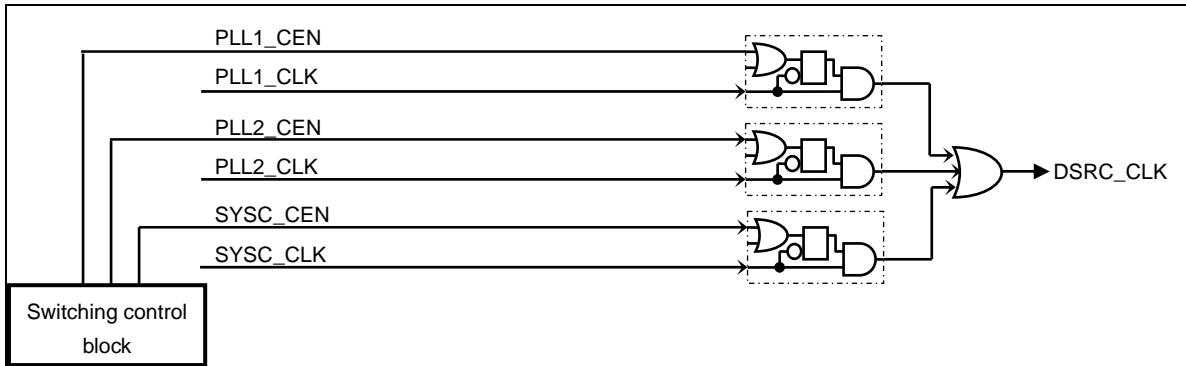
SYSC\_CLK is selected from PLL3\_CLK, OSC0\_CLK, OSC1\_CLK, or CK32KI.

DSRC\_CLK (the clock source for generating the sync clock) is selected in two stages: first by selecting PLL3\_CLK, OSC0\_CLK, OSC1\_CLK, or CK32KI, and then by switching the selected clock with PLL1\_CLK or PLL2\_CLK.

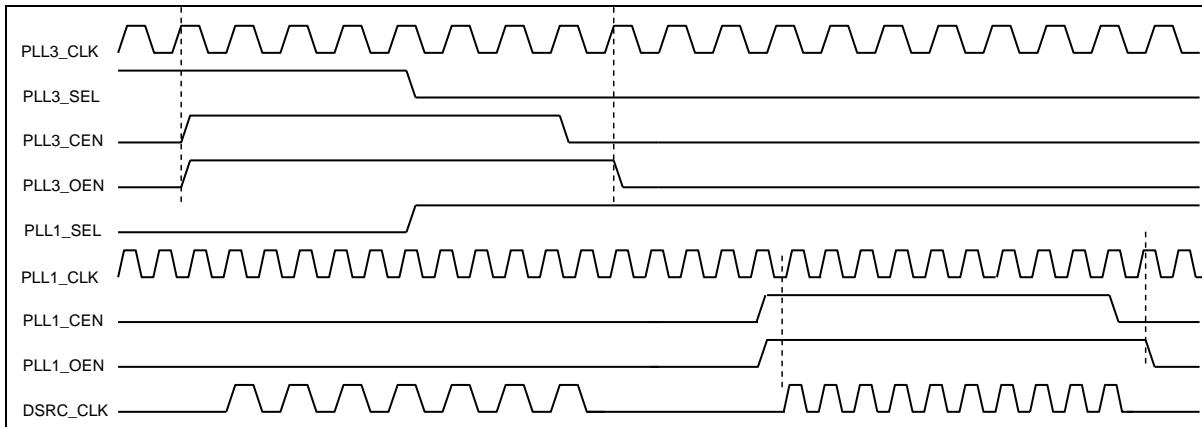
PLL3\_CLK, OSC0\_CLK, OSC1\_CLK, and CK32KI are switched while the clock signal is low after a falling edge has been detected.

The selector in the next stage switches the clock after the clock to be used for SYSC\_CLK has been selected by the selector in the previous stage. This is to ensure that the clock sources are switched in the right order according to the status transitions of EM/EV0; that is, that CK32KI, OSC0\_CLK, and OSC1\_CLK are first switched to PLL3\_CLK, and then PLL3\_CLK is switched to PLL1\_CLK or PLL2\_CLK, and vice versa.

The switching of SYSC\_CLK with PLL1\_CLK and PLL2\_CLK must be controlled so that the CEN signals do not become high level at the same time thus generating a hazard. The way to avoid this is to configure the signals as gating cells with OR logic, as shown below.

**Figure 4-4. Selecting the Source Clock**

A timing chart showing the expected operation of the CEN signals when DSRC\_CLK is switched from the PLL3 clock to the PLL1 clock is shown below.

**Figure 4-5. CEN Signal Timing Chart**

The OEN signals indicate the range in which the clock is actually operating.

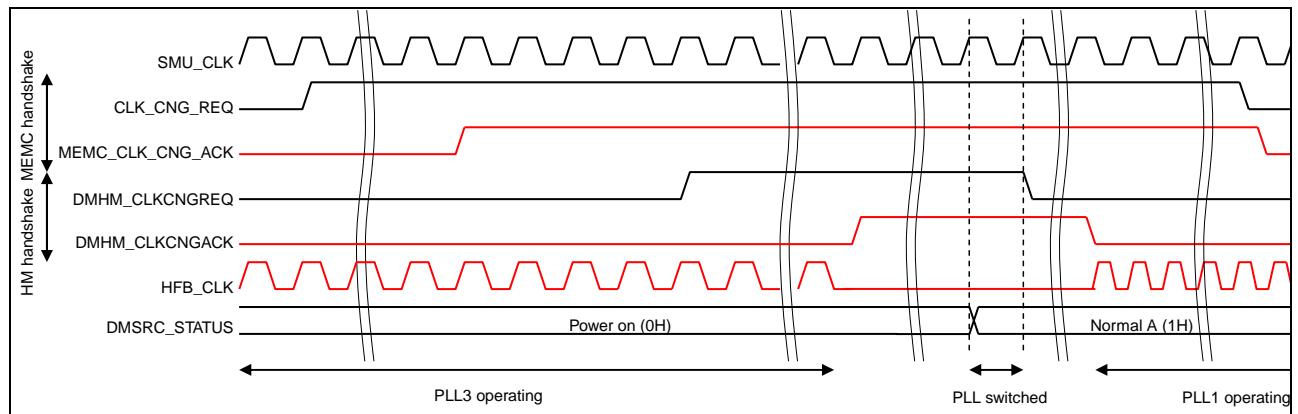
## 4.5 Handshaking When Switching Clocks

When the domain clock source is switched or the frequency (or division factor) is changed, the SMU handshakes with the MEMC macro to stop the MEMC macro accessing the memory during the switchover period.

The SMU also handshakes with the macro in the SMU that generates the domain clock (HM).

The chart below shows the timing of the signals when the clock source is switched from PLL3 to PLL1.

**Figure 4-6. Changing the Clock Source from PLL3 to PLL1**



**CLK\_CNG\_REQ:** Request sent to the MEMC macro asking the macro to prepare to switch the clock source.

**MEMC\_CLK\_CNG\_ACK:** Acknowledgment sent from the MEMC macro indicating that the macro is ready to change the clock source.

**DMHM\_CLKCNGREQ:** Request sent to the HM macro asking the macro to prepare to switch the clock source.

**DMHM\_CLKCNGACK:** Acknowledgment sent from the HM macro indicating that the macro is ready to change the clock source.

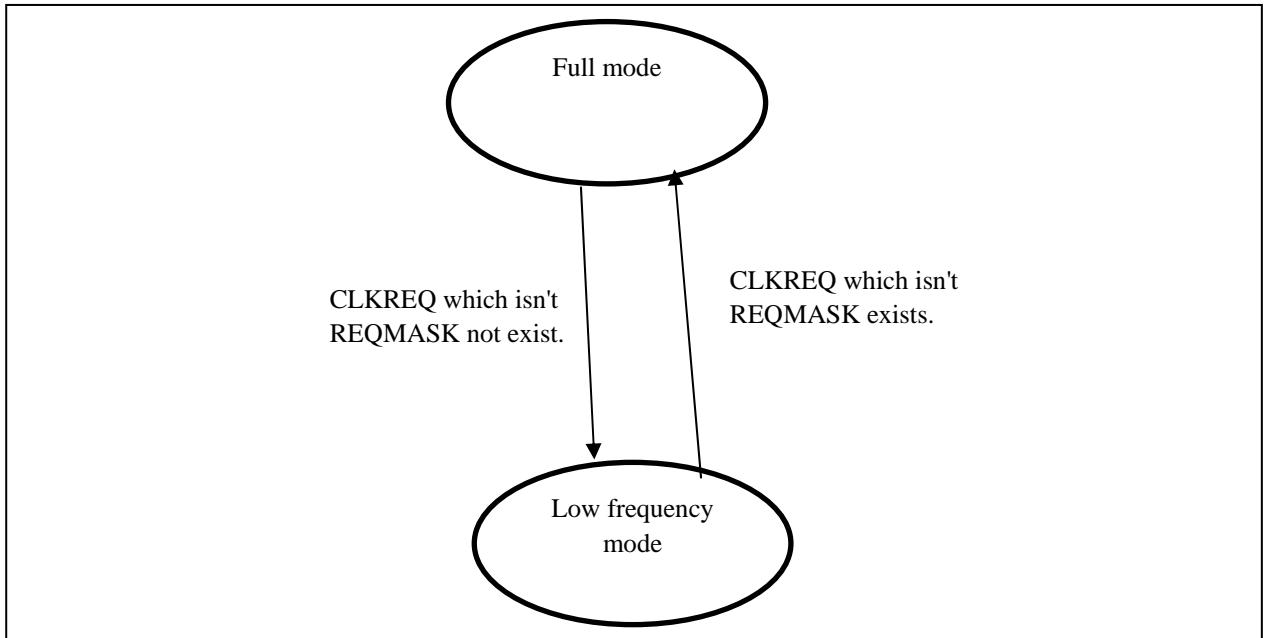
The signals indicated in red in the timing chart are signals that are asynchronous to SMU\_CLK.

The SMU must handshake with HM for at least 235 cycles; that is, at least 235 cycles must elapse between when DMHM\_CLKCNGREQ goes high and when DMHM\_CLKCNGACK goes high, in order to regulate the timing at which the clock is stopped.

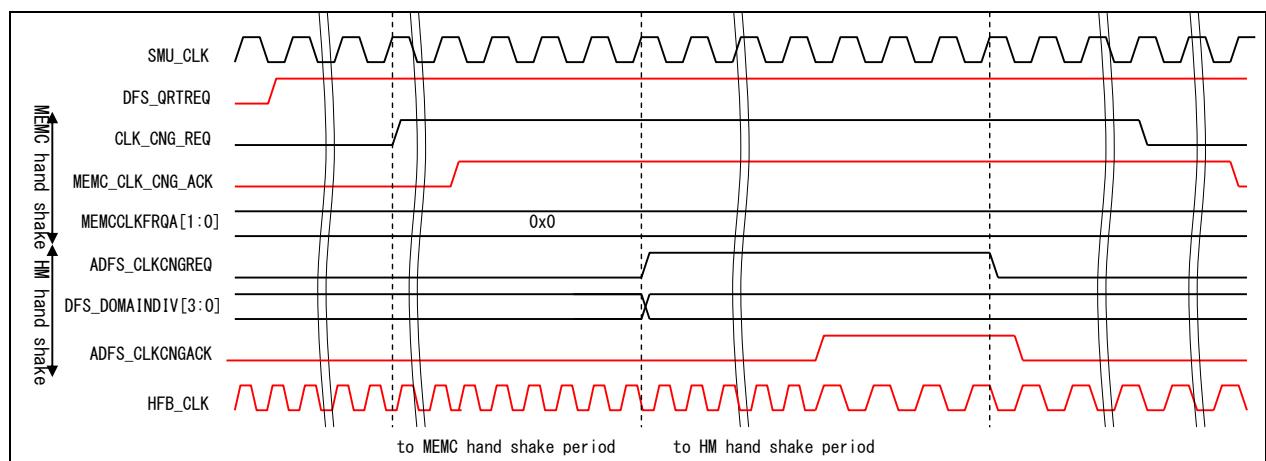
## 4.6 Automatic Frequency Control

To facilitate power saving, the frequencies of all the domain clocks are controlled automatically. When a high clock frequency is not required, the frequency is automatically lowered.

**Figure 4-7. Automatic Frequency Control**



The clock stop is different from a clock source change/a clock division ratio change, and achieved by not doing and changing the division ratio of the shodan ranking of HM. It'll be the following timing chart.



A red line of a timing chart, to SMU\_CLK, asynchronous signal.

#### 4.6.1 Quarter mode

The system runs on the normal frequency when an unmasked CLKREQ signal from a macro becomes active.

When the signal becomes inactive, the source clock is divided by the value specified by the corresponding register and all the domain clock frequencies are lowered.

The signal used to request transition to quarter mode is basically generated as shown below.

It is also possible to stop the system transitioning to quarter mode at certain times by using the 32.768 kHz counter timer.

#### 4.6.2 FIFO mode

In this mode, quarter mode is controlled in accordance with how much space is left in the CAM, and LCD FIFO buffers.

This mode comes into effect when CLK\_MODE\_SEL is specified as normal, automatic frequency switching is enabled, the DFS\_FIFO mode is enabled, and judgment of how much space is left in each FIFO buffer is enabled by DFS\_FIFO\_REQMASK. Threshold values for switching to high-speed and low-speed mode can be set for each of the CAM, and LCD macros (by using the *macro\_FIFOTHRESHOLD* register). The value indicating how much space is left in each FIFO buffer is output to the SMU from each macro.

The condition that a each macro usual frequency at the time of an automatic frequency control returns is as it is the following table.

**Table 4-3 Master side (CKRQMODE\_MASK0)**

Macro	MASK register	High-speed transfer condition logic
CAM	CKRQMODE_MASK0[15]	CAM_CLKREQ
NTS	CKRQMODE_MASK0[14]	NTS_CLKREQ
DTV	CKRQMODE_MASK0[13]	DTV_CLKREQ
A3D	CKRQMODE_MASK0[12]	A3D_IDLE & A3D_RSTZ
AVE	CKRQMODE_MASK0[11]	SYN2_AVE_IDLE & AVE_ARSTZ & AVE_CRSTZ & AVE_PRSTZ
ROT	CKRQMODE_MASK0[9]	ROT_CLKREQ
SIZ	CKRQMODE_MASK0[8]	SIZ_CLKREQ
IMCW	CKRQMODE_MASK0[7]	IMCW_CLKREQ   LCD_IMC_CLKREQ
IMC	CKRQMODE_MASK0[6]	IMC_CLKREQ   LCD_IMC_CLKREQ
LCD	CKRQMODE_MASK0[5]	LCD_CLKREQ   LCD_CCLKREQ
M2M	CKRQMODE_MASK0[4]	M2M_CLKREQ
M2P	CKRQMODE_MASK0[3]	M2P_CLKREQ
P2M	CKRQMODE_MASK0[2]	P2M_CLKREQ
CPU	CKRQMODE_MASK0[0]	SYN2_ALLSTANDBY   QR_CLKREQ

**Table 4-4 Master side (CKRQMODE\_MASK2)**

Macro	MASK register	High-speed transfer condition logic
PDMA	CKRQMODE_MASK2[0]	PDMA_CLKREQ

By defaults value, automatic frequency control judgment applying.

**Table 4-5 Slave side (CKRQMODE\_MASK1)**

Macro	MASK register	High-speed transfer condition logic
USB1	CKRQMODE_MASK1[27]	USB1RSTZ
USB0	CKRQMODE_MASK1[26]	USB0RSTZ
IIC1	CKRQMODE_MASK1[25]	IIC1RSTZ & (IIC1_SCLK_GCC   IIC1_CLK_GCC)
IIC0	CKRQMODE_MASK1[24]	IIC0RSTZ & (IIC0_SCLK_GCC   IIC0_CLK_GCC)
PWM	CKRQMODE_MASK1[22]	PWMRSTZ & (PWM_PCLK_GCC   PWM_PWCLK0_GCC   PWM_PWCLK1_GCC)
AB0	CKRQMODE_MASK1[20]	AB0_BURSTMODE & (AB0_CLKREQ   BUS1_AB0_CLKREQ)
ROM	CKRQMODE_MASK1[19]	ROM_CLKREQ
CFI	CKRQMODE_MASK1[17]	CFIRSTZ & (CFI_CLK_GCC   CFI_HCLK_GCC)
SDC	CKRQMODE_MASK1[15]	SDCRSTZ & (SDC_CLK_GCC   SDC_HCLK_GCC)
SDIO2	CKRQMODE_MASK1[14]	SDIO2RSTZ & (SDIO2_CLK_GCC   SDIO2_HCLK_GCC   SDIO2_SCLK_GCC)
SDIO1	CKRQMODE_MASK1[13]	SDIO1RSTZ & (SDIO1_CLK_GCC   SDIO1_HCLK_GCC   SDIO1_SCLK_GCC)
SDIO0	CKRQMODE_MASK1[12]	SDIO0RSTZ & (SDIO0_CLK_GCC   SDIO0_HCLK_GCC   SDIO0_SCLK_GCC)
UARTSIB_UART3	CKRQMODE_MASK1[10]	USIBU3ARSTZ & (USIB_U3_PCLK_GCC   USIB_U3_SCLK_GCC)
UARTSIB_UART2	CKRQMODE_MASK1[9]	USIBU2ARSTZ & (USIB_U2_PCLK_GCC   USIB_U2_SCLK_GCC)
UARTSIB_UART1	CKRQMODE_MASK1[8]	USIBU1ARSTZ & (USIB_U1_PCLK_GCC   USIB_U1_SCLK_GCC)
USIB_SIO5	CKRQMODE_MASK1[7]	(USIBS5ARSTZ   USIBS5SRSTZ) & (USIB_S5_HCLK_GCC   USIB_S5_PCLK_GCC   USIB_S5_SCLK_GCC)
USIB_SIO4	CKRQMODE_MASK1[6]	(USIBS4ARSTZ   USIBS4SRSTZ) & (USIB_S4_HCLK_GCC   USIB_S4_PCLK_GCC   USIB_S4_SCLK_GCC)
USIB_SIO3	CKRQMODE_MASK1[5]	(USIBS3ARSTZ   USIBS3SRSTZ) & (USIB_S3_HCLK_GCC   USIB_S3_PCLK_GCC   USIB_S3_SCLK_GCC)
USIB_SIO2	CKRQMODE_MASK1[4]	(USIBS2ARSTZ   USIBS2SRSTZ) & (USIB_S2_HCLK_GCC   USIB_S2_PCLK_GCC   USIB_S2_SCLK_GCC)
UARTSIA_UART0	CKRQMODE_MASK1[2]	USIAU0ARSTZ & (USIA_U0_PCLK_GCC   USIA_U0_SCLK_GCC)
USIA_SIO1	CKRQMODE_MASK1[1]	(USIAS1ARSTZ   USIAS1SRSTZ) & (USIA_S1_HCLK_GCC   USIA_S1_PCLK_GCC   USIA_S1_SCLK_GCC)
USIA_SIO0	CKRQMODE_MASK1[0]	(USIAS0ARSTZ   USIAS0SRSTZ) & (USIA_S0_HCLK_GCC   USIA_S0_PCLK_GCC   USIA_S0_SCLK_GCC)

## 4.7 Waiting for the PLL's and Power Supplies to Stabilize

The 32.768 kHz clock counter is used to count the required time when waiting for the operation of PLL1, PLL2, PLL3, PLL4, OSC0 and OSC1 to lock (stabilize), and when waiting for the power supplies to stabilize after the power supply voltage is changed.

## 4.8 Automatic Clock Control

This feature is used to supply a clock automatically when each macro requires a clock. When a clock request signal (CLKREQ) is received from a macro, the SMU supplies the relevant clock to that macro.

The automatic control on/off register and forced clock supply stop register are used to implement this feature.

This feature can also be used to stop supply of a clock to a macro whose operation has been prohibited by the Anti-Fuse setting, supply or stop a clock in retention or power-down mode, and forcibly supply a clock when a reset is applied.

When the operation of a macro has been prohibited by the Anti\_Fuse setting, the automatic clock control feature forcibly stops the clock supply to that macro. However, when or after the areas to which power is supplied, including the macro whose operation has been prohibited, transition to retention or power-down mode, clock supply from the power supply control sequencer is enabled. Clock supply is forcibly stopped again when the power supply status returns to normal mode.

## 4.9 Waiting for AFS to Stabilize

The SMU has a circuit used to ensure that the system waits for the AFS signal to stabilize (which takes 1 ms).

## 4.10 Reset Signal Generation

The reset signal in the SMU (SMU\_ARSTZ) is generated by SRESETB and the stable Fuse signal. This means that even if SRESETB is deasserted, if Fuse has not stabilized, SMU\_ARSTZ will not be deasserted.

Reset hold processing is performed on the CPU\_SYSRSTZ, CPU\_DERSTZ[1:0], and CPU\_CPURSTZ[1:0] signals so that they cannot change from low to high while the RSTHOLD signal is high. However, if the reset control register changed from high to low while the RSTHOLD signal is high, or if the RSTHOLD goes low, reset hold control is disabled.

The SMU supplies the reset signal for each macro.

The reset signal is generated using one of the following methods:

### Method 1

The reset signal is deasserted after a stable Fuse signal has passed through a 3-stage F/F.

Assert the macro reset signal when PODET is asserted.

### Method 2

Assert the macro reset signal when SMU\_ARSTZ is asserted.

Deassert the macro reset signal when SMU\_ARSTZ is deasserted.

### Method 3

Assert the macro reset signal when SMU\_ARSTZ is asserted.

Deassert the macro reset signal 10 clock cycles (at a frequency of  $229.376/16 = 14.336$  MHz when the power is on) after SMU\_ARSTZ is deasserted.

#### Method 4

Assert the macro reset signal when SMU\_ARSTZ is asserted.

Keep the macro reset signal asserted until the CPU writes to the memory, even after SMU\_ARSTZ is deasserted.

#### Reset input:

Pin	Asynchronous Reset Input
PODET (DET1)	External DET signal input
SRESETB (A_RESETZ)	External reset input

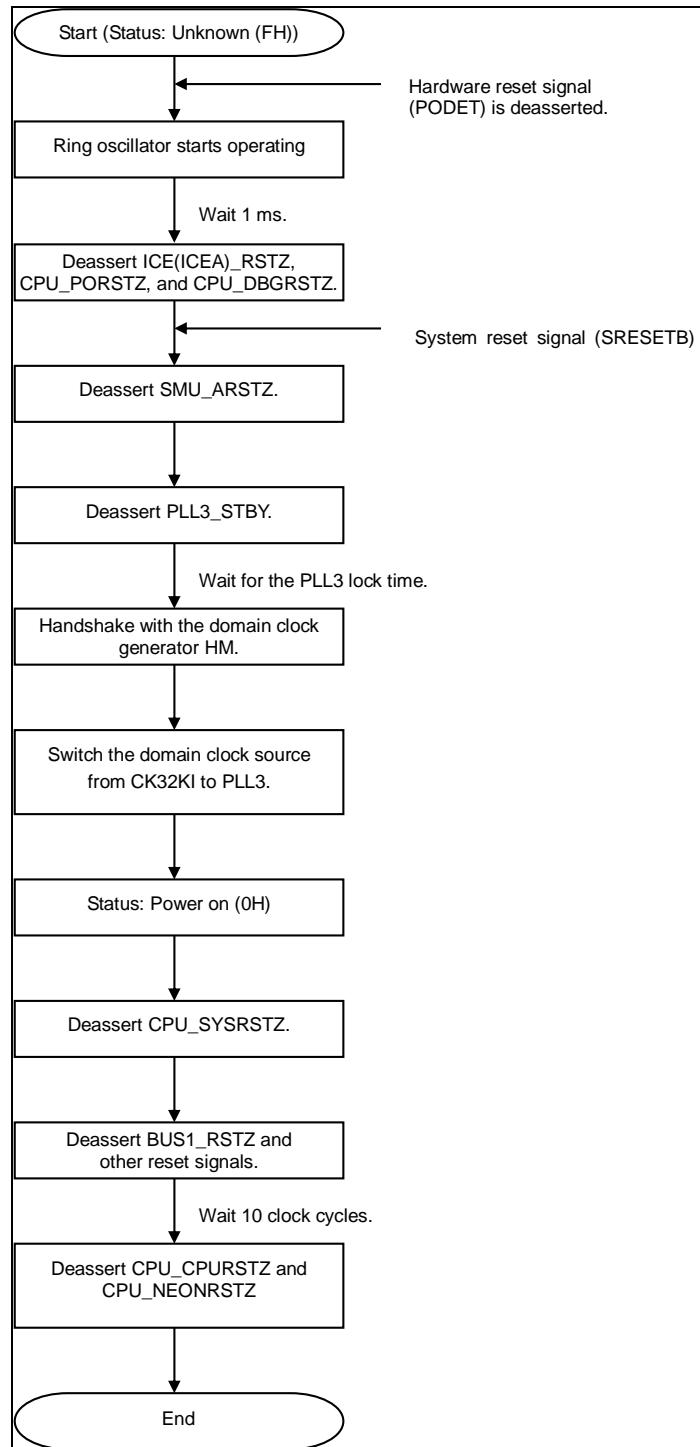
#### Reset output:

Pin Name	Generation Method	Pin Name	Generation Method	Pin Name	Generation Method
PMU_TESTRSTZ	Method 1 only	TW4_RSTZ	Method 4	BUS1_IMCW_RSTZ	Method 4
CHG_RSTZ	DET1 & register value	TG0_RSTZ	Method 4	NTS_RSTZ	Method 4
CHG1_RSTZ	Method 4	USIB_S2_SRSTZ	Method 4	DTV_RSTZ	Method 4
CPU_SYSRSTZ	Method 2	USIB_S2_ARSTZ	Method 4	DTV_ARSTZ	Method 4
CPU_PORSTZ	Method 1	USIB_S3_SRSTZ	Method 4	CAM_RSTZ	Method 4
CPU_CPURSTZ[1:0]	Method 3	USIB_S3_ARSTZ	Method 4	AB0_RSTZ	Method 2
CPU_DERSTZ[1:0]	Method 3	USIB_S4_SRSTZ	Method 4	CFI_RSTZ	Method 4
PMU_RSTZ	Method 4	USIB_S4_ARSTZ	Method 4	SDC_RSTZ	Method 4
SRC_RSTZ	Method 2	USIB_S5_SRSTZ	Method 4	SDIO0_RSTZ	Method 4
INTA_RSTZ	Method 2	USIB_S5_ARSTZ	Method 4	SDIO1_RSTZ	Method 4
ICE_RSTZ	Method 1	USIB_U1_ARSTZ	Method 4	SDIO2_RSTZ	Method 4
ICEA_RSTZ	Method 1	USIB_U2_ARSTZ	Method 4	LCD_ARSTZ	Method 4
GIO_RSTZ	Method 4	USIB_U3_ARSTZ	Method 4	STI_RSTZ	Method 4
USIA_S0_SRSTZ	Method 4	TG1_RSTZ	Method 4	AFS_RSTZ	Method 4
USIA_S0_ARSTZ	Method 4	TG2_RSTZ	Method 4	USB0_RSTZ	Method 4
USIA_S1_SRSTZ	Method 4	TG3_RSTZ	Method 4	USB1_RSTZ	Method 4
USIA_S1_ARSTZ	Method 4	TG4_RSTZ	Method 4	MEMC_RSTZ	Method 4
USIA_U0_ARSTZ	Method 4	TG5_RSTZ	Method 4	LCD_RSTZ	Method 4
TI0_RSTZ	Method 4	AHB_RSTZ	Method 2	CHG1_RSTZ	Method 4
TI1_RSTZ	Method 4	PBL0_RSTZ	Method 2	BUS1_RSTZ	Method 2
TI2_RSTZ	Method 4	PBL1_RSTZ	Method 2	M2M_RSTZ	Method 4
TI3_RSTZ	Method 4	ROT_RSTZ	Method 4	M2P_RSTZ	Method 4
TW0_RSTZ	Method 4	SIZ_RSTZ	Method 4	P2M_RSTZ	Method 4
TW1_RSTZ	Method 4	IMC_RSTZ	Method 4	PDMA_RSTZ	Method 4
TW2_RSTZ	Method 4	IMCW_RSTZ	Method 4	CPU_PRSTDBGZ	Method 1
TW3_RSTZ	Method 4	BUS1_IMC_RSTZ	Method 4		

## 4.11 Turning on the Power

After turning on the power, the following processing is executed when the hardware reset signal is deasserted.

**Figure 4-8. Turning on the Power**



## 4.12 Input Clocks

Clock Name	Domain	Division Setting	Remarks
PLL1_FO	PLL1 clock	Async	–
PLL2_FO	PLL2 clock	Async	–
PLL3_FO	PLL3 clock	Async	–
PLL4_FO	PLL4 clock	Async	–
OSC0_FO	OSC0 clock	Async	–
OSC1_FO	OSC0 clock	Async	–
CK32KI	32.768 kHz clock	Async	–
EXT_CLKI	External input clock	Async	–

## 4.13 Output Clocks

Clock Name		Domain	Division Setting	Remarks
CHG_PCLK	APB clock for CHG	HFB	Same as domain CLK	Dependent on synchronous domain clock frequency
CPU_CLK	CPU clock	CPU	Same as domain CLK	Dependent on synchronous domain clock frequency
CPU_SYSCLK	CPU clock	FFB	Same as domain CLK	Dependent on synchronous domain clock frequency
CPU_SRCCLK	SRC_CLK for CPU	QFB	Same as domain CLK	Dependent on synchronous domain clock frequency
QR_CLK	QR clock for CPU	CPU	8bit	Divided by 1 to 256 of CPU domain clock
SMU_CLK	System clock for SMU	Async	–	–
SMU_PCLK	APB clock for SMU	HFB	Same as domain CLK	Dependent on synchronous domain clock frequency
PMU_CLK	APB clock for PMU	HFB	Same as domain CLK	Dependent on synchronous domain clock frequency
PMU_32K_CLK	WDT clock for PMU	Async	–	–
BUS0_CLK	Bus clock for BUS0	FFB	Same as domain CLK	Dependent on synchronous domain clock frequency
BUS0_PCLK	APB clock for BUS0	HFB	Same as domain CLK	Dependent on synchronous domain clock frequency
SRC_CLK	SRC clock	QFB	Same as domain CLK	Dependent on synchronous domain clock frequency
INTA_CLK	INTA clock	HFB	Same as domain CLK	Dependent on synchronous domain clock frequency
INTA_PCLK	APB clock for INTA	HFB	Same as domain CLK	Dependent on synchronous domain clock frequency
INTA_TCLK	Timer clock for INTA	Async	–	–
ICE_CLK	ICE clock	CPU	Same as domain CLK	CPU domain clock divided by 4
ICE_PCLK	APB clock for ICE	HFB	Same as domain CLK	Dependent on synchronous domain clock frequency
ICE_MST_HCLK	ICE master clock	HFB	Same as domain CLK	Dependent on synchronous domain clock frequency
ICE_TRC_HCLK	ICE trace clock	HFB	Same as domain CLK	Dependent on synchronous domain clock frequency
GIO_CLK	APB clock for GIO	HFB	Same as domain CLK	Dependent on synchronous domain clock frequency
GIO_INT_CLK	GIO interrupt clock for	Async	–	–
USIA_S0_HCLK	Bus clock for SIO0	HFB	Same as domain CLK	Dependent on synchronous domain clock frequency
USIA_S0_PCLK	APB clock for SIO0	HFB	Same as domain CLK	Dependent on synchronous domain clock frequency
USIA_S0_SCLK	Serial clock for SIO0	Async	8 bits	Divided by 1 to 256

Clock Name	Domain	Division Setting	Remarks
USIA_S1_HCLK	Bus clock for SIO1	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
USIA_S1_PCLK	APB clock for SIO1	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
USIA_S1_SCLK	Serial clock for SIO1	Async	8 bits Divided by 1 to 256
USIA_U0_PCLK	APB clock for UART0	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
USIA_U0_SCLK	Serial clock for UART0	Async	8 bits Divided by 1 to 256
TIM_PCLK	APB clock for TIM	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
TI0_CLK	TI0 clock	Async	8 bits Selectable from clock divided by 1 to 256 and thinned 32 kHz clock (only for PLL3)
TI1_CLK	TI1 clock	Async	8 bits Selectable from clock divided by 1 to 256 and thinned 32 kHz clock (only for PLL3)
TI2_CLK	TI2 clock	Async	8 bits Selectable from clock divided by 1 to 256 and thinned 32 kHz clock (only for PLL3)
TI3_CLK	TI3 clock	Async	8 bits Selectable from clock divided by 1 to 256 and thinned 32 kHz clock (only for PLL3)
TW0_CLK	TW0 clock	Async	8 bits Selectable from clock divided by 1 to 256 and thinned 32 kHz clock (only for PLL3)
TW1_CLK	TW1 clock	Async	8 bits Selectable from clock divided by 1 to 256 and thinned 32 kHz clock (only for PLL3)
TW2_CLK	TW2 clock	Async	8 bits Selectable from clock divided by 1 to 256 and thinned 32 kHz clock (only for PLL3)
TW3_CLK	TW3 clock	Async	8 bits Selectable from clock divided by 1 to 256 and thinned 32 kHz clock (only for PLL3)
TW4_CLK	TW4 clock	Async	8 bits Selectable from clock divided by 1 to 256 and thinned 32 kHz clock (only for PLL3)
TG0_CLK	TG0 clock	Async	8 bits Selectable from clock divided by 1 to 256 and thinned 32 kHz clock (only for PLL3)
TG1_CLK	TG1 clock	Async	8 bits Selectable from clock divided by 1 to 256 and thinned 32 kHz clock (only for PLL3)
TG2_CLK	TG2 clock	Async	8 bits Selectable from clock divided by 1 to 256 and thinned 32 kHz clock (only for PLL3)
TG3_CLK	TG3 clock	Async	8 bits Selectable from clock divided by 1 to 256 and thinned 32 kHz clock (only for PLL3)
TG4_CLK	TG4 clock	Async	8 bits Selectable from clock divided by 1 to 256 and thinned 32 kHz clock (only for PLL3)

Clock Name	Domain	Division Setting	Remarks
			for PLL3)
TG5_CLK	TG5 clock	Async	Selectable from clock divided by 1 to 256 and thinned 32 kHz clock (only for PLL3)
STI_PCLK	APB clock for STI	HFB	Same as domain CLK
STI_SCLK	STI clock	Async	–
STI_PCLK_EN	STI clock enable	Async	– Low when using C32K; otherwise high. Dependent on synchronous domain clock frequency.
AFS_PCLK	APB clock for AFS	HFB	Same as domain CLK
AFS_32K_CLK	32K clock for AFS	Async	–
USB0_CLK	USB0 clock	HFB	Same as domain CLK
USB1_CLK	USB1 clock	HFB	Same as domain CLK
MEMC_CLK	Bus clock for MEMC	DDR	Same as domain CLK
MEMC_CLK270	Phase shift clock for MEMC	DQS	Same as domain CLK
MEMC_RCLK	MEMC clock	Async	8 bits Divided by 1 to 256
MEMC_PCLK	APB clock for MEMC	HFB	Same as domain CLK
MEMC_AXCLK_EN	MEMC clock enable	DDR-FFB	Same as domain CLK
MEMC_DPCLK_EN	MEMC clock enable	DDR-FFB	Same as domain CLK
MEMC_PB1CLKEN	MEMC clock enable	DDR-HFB	Same as domain CLK
LCD_CLK	Bus clock for LCD	FFB	Same as domain CLK
LCD_PCLK	APB clock for LCD	HFB	Same as domain CLK
LCD_LCLK	Pixel clock for LCD	Async	8 bits Divided by 1 to 256
LCD_CCLK	Bus clock for LCD	FFB	Same as domain CLK
CHG1_PCLK	APB clock for CHG1	HFB	Same as domain CLK
BUS1_CLK	Bus clock for BUS1	FFB	Same as domain CLK
BUS1_PCLK	APB clock for BUS1	HFB	Same as domain CLK
BUS1_CLKEN	BUS1 clock enable	FFB-HFB	Same as domain CLK
M2M_CLK	Bus clock for M2M	FFB	Same as domain CLK
M2M_PCLK	APB clock for M2M	HFB	Same as domain CLK

Clock Name	Domain	Division Setting	Remarks
M2P_CLK	Bus clock for M2P	FFB	Same as domain CLK Dependent on synchronous domain clock frequency
M2P_CLKEN	M2P clock enable	FFB-HFB	Same as domain CLK Dependent on synchronous domain clock frequency
M2P_PCLK	APB clock for M2P	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
M2P_TCLK	Timer clock for M2P	Async	–
P2M_CLK	Bus clock for P2M	FFB	Same as domain CLK Dependent on synchronous domain clock frequency
P2M_CLKEN	P2M clock enable	FFB-HFB	Same as domain CLK Dependent on synchronous domain clock frequency
P2M_PCLK	APB clock for P2M	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
P2M_TCLK	Timer clock for P2M	Async	–
AHB_CLK	AHB bridge clock for BUS1	FFB	Same as domain CLK Dependent on synchronous domain clock frequency
AHB_HCLK	AHB bridge clock for BUS1	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
AHB_CLKEN	AHB bridge clock enable for BUS1	FFB-HFB	Same as domain CLK Dependent on synchronous domain clock frequency
PBL0_CLK	APB bridge clock for BUS1	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
PBL1_CLK	APB bridge clock for BUS1	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
ROM_CLK	ROM clock	FFB	Same as domain CLK Dependent on synchronous domain clock frequency
ROT_PCLK	APB clock for ROT	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
ROT_CLK	Bus clock for ROT	FFB	Same as domain CLK Dependent on synchronous domain clock frequency
SIZ_CLK	Bus clock for SIZ	FFB	Same as domain CLK Dependent on synchronous domain clock frequency
SIZ_PCLK	APB clock for SIZ	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
IMC_CLK	Bus clock for IMC	FFB	Same as domain CLK Dependent on synchronous domain clock frequency
IMC_PCLK	APB clock for IMC	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
IMCW_CLK	Bus clock for IMCW	FFB	Same as domain CLK Dependent on synchronous domain clock frequency
IMCW_PCLK	APB clock for IMCW	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
NTS_CLK	Bus clock for NTS	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
NTS_PCLK	APB clock for NTS	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
DTV_CLK	DTV clock	HFB	Same as domain CLK Dependent on synchronous domain clock frequency

Clock Name	Domain	Division Setting	Remarks
DTV_PCLK	APB clock for DTV	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
CAM_CLK	Bus clock for CAM	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
CAM_PCLK	APB clock for CAM	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
CAM_SCLK	CAM clock	Async	8 bits Divided by 1 to 256
AB0_CLK	Bus clock for AB0	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
AB0_CLKEN	AB0 clock enable	HFB-FLA	Same as domain CLK Dependent on synchronous domain clock frequency
AB_CLK	Flash memory clock for AB0	FLA	Same as domain CLK Dependent on synchronous domain clock frequency
CFI_CLK	Bus clock for CFI	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
CFI_HCLK	Bus clock for CFI	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
SDC_CLK	SDC clock	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
SDC_HCLK	Bus clock for SDC	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
SDIO0_CLK	SDIO0 clock	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
SDIO0_HCLK	Bus clock for SDIO0	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
SDIO0_SCLK	SDIO0 clock	Async	8 bits Divided by 1 to 256
SDIO1_CLK	SDIO1 clock	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
SDIO1_HCLK	Bus clock for SDIO1	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
SDIO1_SCLK	SDIO1 clock	Async	8 bits Divided by 1 to 256
SDIO2_CLK	SDIO2 clock	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
SDIO2_HCLK	Bus clock for SDIO2	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
SDIO2_SCLK	SDIO2 clock	Async	8 bits Divided by 1 to 256
USIB_S2_HCLK	Bus clock for SIO2	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
USIB_S2_PCLK	APB clock for SIO2	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
USIB_S2_SCLK	Serial clock for SIO2	Async	8 bits Divided by 1 to 256
USIB_S3_HCLK	Bus clock for SIO3	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
USIB_S3_PCLK	APB clock for SIO3	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
USIB_S3_SCLK	Serial clock for SIO3	Async	8 bits Divided by 1 to 256
USIB_S4_HCLK	Bus clock for SIO4	HFB	Same as domain Dependent on synchronous domain

Clock Name	Domain	Division Setting	Remarks
		CLK	clock frequency
USIB_S4_PCLK	APB clock for SIO4	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
USIB_S4_SCLK	Serial clock for SIO4	Async	8 bits Divided by 1 to 256
USIB_S5_HCLK	Bus clock for SIO5	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
USIB_S5_PCLK	APB clock for SIO5	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
USIB_S5_SCLK	Serial clock for SIO5	Async	8 bits Divided by 1 to 256
USIB_U1_PCLK	APB clock for UART1	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
USIB_U1_SCLK	Serial clock for UART1	Async	8 bits Divided by 1 to 256
USIB_U2_PCLK	APB clock for UART2	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
USIB_U2_SCLK	Serial clock for UART2	Async	8 bits Divided by 1 to 256
USIB_U3_PCLK	APB clock for UART3	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
USIB_U3_SCLK	Serial clock for UART3	Async	8 bits Divided by 1 to 256
IIC0_CLK	APB clock for IIC0	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
IIC0_SCLK	IIC0 clock	Async	8 bits Divided by 1 to 256
IIC1_CLK	APB clock for IIC1	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
IIC1_SCLK	IIC1 clock	Async	8 bits Divided by 1 to 256
PWM_PCLK	APB clock for PWM	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
PWM_PWCLK0	PWM clock	Async	8 bits Divided by 1 to 256
PWM_PWCLK1	PWM clock	Async	8 bits Divided by 1 to 256
A3D_MEM_CLK	A3D clock	FFB	Same as domain CLK Dependent on synchronous domain clock frequency
A3D_SYS_CLK	System clock for A3D	HFB	Same as domain CLK Divided by 1 to 256
A3D_CORE_CLK	Core clock for A3D	Async	8 bits Divided by 1 to 256
AVE_CCLK	Core clock for AVE	Async	8 bits Divided by 1 to 256
AVE_ACLK	Bus clock for AVE	FFB	Same as domain CLK Dependent on synchronous domain clock frequency
AVE_PCLK	APB clock for AVE	HFB	Same as domain CLK Dependent on synchronous domain clock frequency
REF_CLKO	REF clock	Async	8 bits Divided by 1 to 256
USB_PCICLK	USB clock	Async	8 bits Divided by 1 to 256
PDMA_CLK	PDMA clock	HFB	Same as domain CLK Dependent on synchronous domain clock frequency

Clock Name	Domain	Division Setting	Remarks
PDMA_CLKEN	PDMA clock enable	FFB-HFB	Same as domain CLK Dependent on synchronous domain clock frequency
BUS1_MEMC_C_LK	MEMC_CLK for BUS1	DDR	Same as domain CLK Dependent on synchronous domain clock frequency
BUS1_CPU_SY_SCLK	CPU_SYSCLK for BUS1	FFB	Same as domain CLK Dependent on synchronous domain clock frequency
BUS1_SRC_CLKEN	SRC_CLKEN for BUS1	FFB-QFB	Same as domain CLK Dependent on synchronous domain clock frequency
BUS1_A3D_ME_M_CLK	A3D_MEM_CLK for BUS1	FFB	Same as domain CLK Dependent on synchronous domain clock frequency
BUS1_AVE_ACLK	AVE_ACLK for BUS1	FFB	Same as domain CLK Dependent on synchronous domain clock frequency
BUS1_IMC_CLK	IMC_CLK for BUS1	FFB	Same as domain CLK Dependent on synchronous domain clock frequency
BUS1_IMCW_C_LK	IMCW_CLK for BUS1	FFB	Same as domain CLK Dependent on synchronous domain clock frequency

REVISION HISTORY	EMMA Mobile EV2 User's Manual: System Management Unit	
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Rev.	Date	Description	
		Page	Summary
1.00	Feb 5, 2010	—	1 <sup>st</sup> revision release
2.00	Jun 7, 2010	—	Incremental update from comments to the 1.0.
3.00	Jun 30, 2010	—	Incremental update from comments to the 2.0. (A change part from the old revision is “★” marked in the page left end.)
4.00	Oct 29, 2010	—	Incremental update from comments to the 3.0. (A change part from the old revision is “★” marked in the page left end.)
5.00	Dec 28, 2010	—	Incremental update from comments to the 4.0. (A change part from the old revision is “★” marked in the page left end.)
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7.00	May 31, 2011	—	Incremental update from comments to the 6.0.
8.00	Dec 21, 2011	—	Incremental update from comments to the 7.0.
		85	Chapter 3.2.103 corrected.
		110	Chapter 3.2.120 corrected. (bit[7:4] recommendation value 7H→0H)
		112	Chapter 3.2.121 corrected. (bit[7:4] recommendation value 7H→0H)
		114	Chapter 3.2.122 corrected. (bit[7:4] recommendation value 7H→0H)
		116	Chapter 3.2.123 corrected. (bit[7:4] recommendation value 7H→0H)
		120	Chapter 3.2.125 corrected. (bit[7:4] recommendation value 7H→0H)
		130	Chapter 3.2.132 added.
		318	Chapter 3.2.340 corrected. (bit[4] Description)
		331～332	Table4-3～4-5 added.
9.00	May 25, 2012	—	Incremental update from comments to the 8.0.
		368	Figure 4-1 corrected.
10.00	Jun 22, 2012	369	Table 4-1, Table 4-2 corrected.
		370	Chapter 4.2 corrected. (PLL1 Clock frequency : 400 to 800MHz → 50 to 533MHz PLL2 Clock frequency : 320 to 500MHz → 320 to 533MHz PLL4 Clock frequency : 320 to 500MHz → 320 to 533MHz OSC0 Clock frequency : 10 to 30MHz → 10 to 27MHz OSC1 Clock frequency : 10 to 30MHz → 24MHz)
11.00	Jul 6, 2012	247	Figure 3-13 corrected. (S0_DUMMY_REG[4] → SMU_CONTROL[4])
		362	Chapter 3.2.340 corrected. (bit[4])
12.00	Aug 22, 2012	—	Incremental update from comments to the 11.00.

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# System Management Unit

EMMA Mobile EV2



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