User's Manual

HD Video Decoder

User's Manual

Multimedia Processor for Mobile Applications
EMMA Mobile ™ EV2

Renesas Electronics
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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the EMMA Mobile EV2. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Data Sheet	Hardware overview and electrical characteristics	EMMA Mobile EV2 Datasheet	R19DS0010EJxxxx
User's manual (1chip)	Hardware whole specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description	EMMA Mobile EV2 User's manual 1chip	R19UH0036EJxxxx
User's manual (module)	Hardware each macro specifications and operation description.	EMMA Mobile EV2 User's manual each module	See below

Document Name	Document No.	Document Name	Document No.
1chip	R19UH0036EJxxxx	DMA Controller	R19UH0043EJxxxx
System Management Unit	R19UH0037EJxxxx	LP-DDR/DDR2 Controller	R19UH0039EJxxxx
Timer	R19UH0054EJxxxx	SD Memory Card Interface	R19UH0061EJxxxx
System Timer	R19UH0055EJxxxx	SDIO Interface	R19UH0042EJxxxx
HD Video Decoder (This manual)	R19UH0056EJxxxx	CF Card Interface	R19UH0062EJxxxx
Rotator	R19UH0057EJxxxx	Unified Serial Interface	R19UH0047EJxxxx
Resizer	R19UH0058EJxxxx	UART interface	R19UH0040EJxxxx
Image Composer	R19UH0038EJxxxx	USB 2.0 Host Controller	R19UH0045EJxxxx
LCD Interface	R19UH0044EJxxxx	USB 2.0 Function Contoller	R19UH0034EJxxxx
ITU-R BT.656 Interface	R19UH0059EJxxxx	IIC Interface	R19UH0052EJxxxx
Digital Terrestrial TV Interface	R19UH0048EJxxxx	General Purpose I/O Interface	R19UH0041EJxxxx
Camera Interface	R19UH0060EJxxxx	Pulse Width Modulation Interface	R19UH0063EJxxxx

4 digits of end shows the version.

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names

Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.

Examples the PM03 bit in the PM0 register

P3_5 pin, VCC pin

(2) Notation of Numbers

The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.

Examples Binary: 11b or 11

Hexadecimal: EFA0h

Decimal: 1234

3. Register Notation

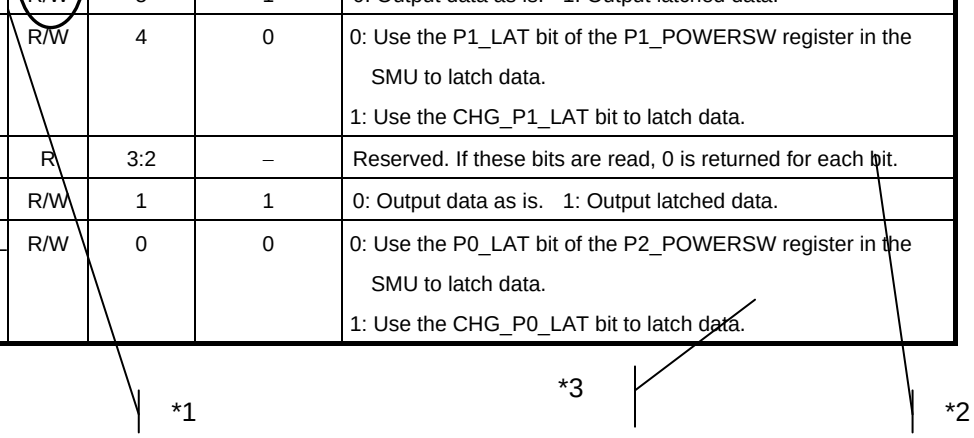
The symbols and terms used in register diagrams are described below.

x.x.x XXX register

This register (XXXXXXX: xxxx_xxxxh) …..

7	6	5	4	3	2	1	0
Reserved		CHG_P1_LAT	LATCH_P1_SEL	Reserved		CHG_P0_LAT	CHG_P0_LAT_SEL

Name	R/W	Bit No.	After Reset	Description
LATCH_P2_SEL	R/W	8	0	0: Use the P2_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P2_LAT bit to latch data.
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P1_LAT	R/W	5	1	0: Output data as is. 1: Output latched data.
LATCH_P1_SEL	R/W	4	0	0: Use the P1_LAT bit of the P1_POWERSW register in the SMU to latch data. 1: Use the CHG_P1_LAT bit to latch data.
Reserved	R	3:2	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P0_LAT	R/W	1	1	0: Output data as is. 1: Output latched data.
CHG_P0_LAT_SEL	R/W	0	0	0: Use the P0_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P0_LAT bit to latch data.



*1

R/W: Read and Write.

R: Read only.

W: Write only.

-: Nothing is assigned.

*2

Reserved bit.

Reserved bit. Set to specified value.

*3

・ Nothing is assigned.

Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.

・ Do not set to a value.

Operation is not guaranteed when a value is set.

・ Function varies according to the operating mode.

The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Register
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

Table of Contents

1. Overview

EM/EV includes a hardware video decoder IP. For EM/EV, an APB3 interface connection is used to allocate the above IP macro to an EM/EV-standard memory map, and the macro name is specified as AVE.
The AVE decodes the elementary streams of various video formats, and then outputs the result to external memory in the YUV420 format.

1.1 Features

- Supported image sizes
  Maximum image size: 1,920 × 1,088 pixels
  Minimum image size: 32 × 16 pixels

- Supported input image formats

Standard	Profile	Level	Resolution
H.264	BP/MP/HP	4.1	1,920 × 1,080
H.263	Profile3		1,920 × 1,080
VC-1	SP/MP/AP	3	1,920 × 1,080
MPEG-4	ASP		1,920 × 1,080[Note 1]
MPEG-2	MP	HL	1,920 × 1,080
DivX (Xvid)	Home Theater		1,920 × 1,080[Note 2]

Notes 1. The standard MPEG-4 resolution is up to 720 × 576.
2. The standard resolution for the DivX Home Theater Profile is up to 720 × 576.

- Output format
  YUV420 (Planar, Semi-planar)

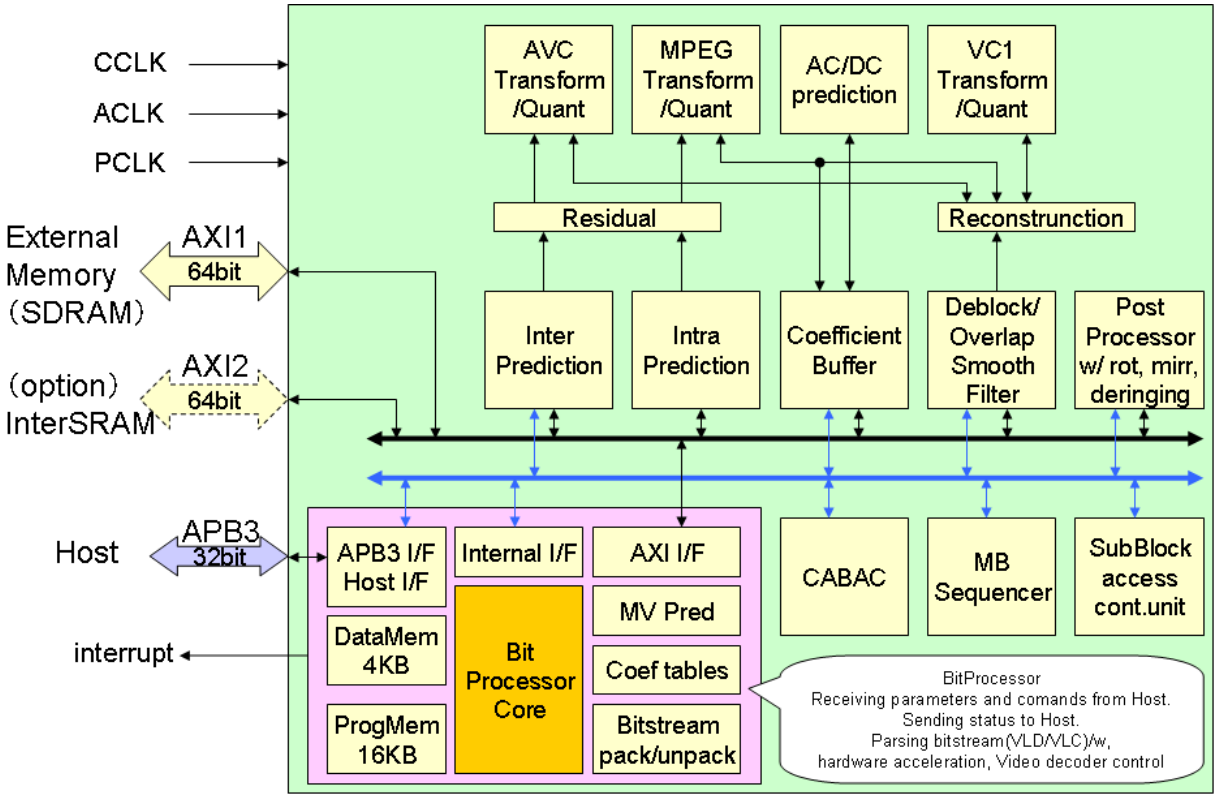
- CPU command interface
  The AMBA-32-bit APB3 interface is used as the bus for accessing control registers from the CPU.

- Memory interface
  The AMBA-64-bit AXI interface is used as the bus for external memory transfers.

- Interrupts
  There is one interrupt output for the host. This interrupt reports information such as the completion of decoding each frame and stream buffer requests.
  A decoding completion interrupt is generated after all the data in the internal buffer is transferred to the external DRAM.

1.2 Block Diagram

Figure 1-1 Block Diagram



2. Registers

- Base address: E029_0000H
- These registers are accessed via the APB bus.
- These registers can be accessed only in 32-bit units. (8-bit and 16-bit accesses are handled as 32-bit accesses.)

3. Description of Functions

3.1 Clocks and Resets

3.1.1 Clocks

The AVE requires that the three clock signals below be input.
These clocks are completely asynchronous and can be run on different frequencies.

Clock Name	Clock Function	Required Frequency (Max.)	Design-Target Frequency	Duty Cycle	Remark
CCLK	Used for core operation	266 MHz	266 MHz	Ignored (because the clock signal is only used while high)	
ACLK	Used for the AXI interface	266 MHz	266 MHz	Ignored (because the clock signal is only used while high)	
PCLK	Used for the APB interface	266 MHz	266 MHz	Ignored (because the clock signal is only used while high)	

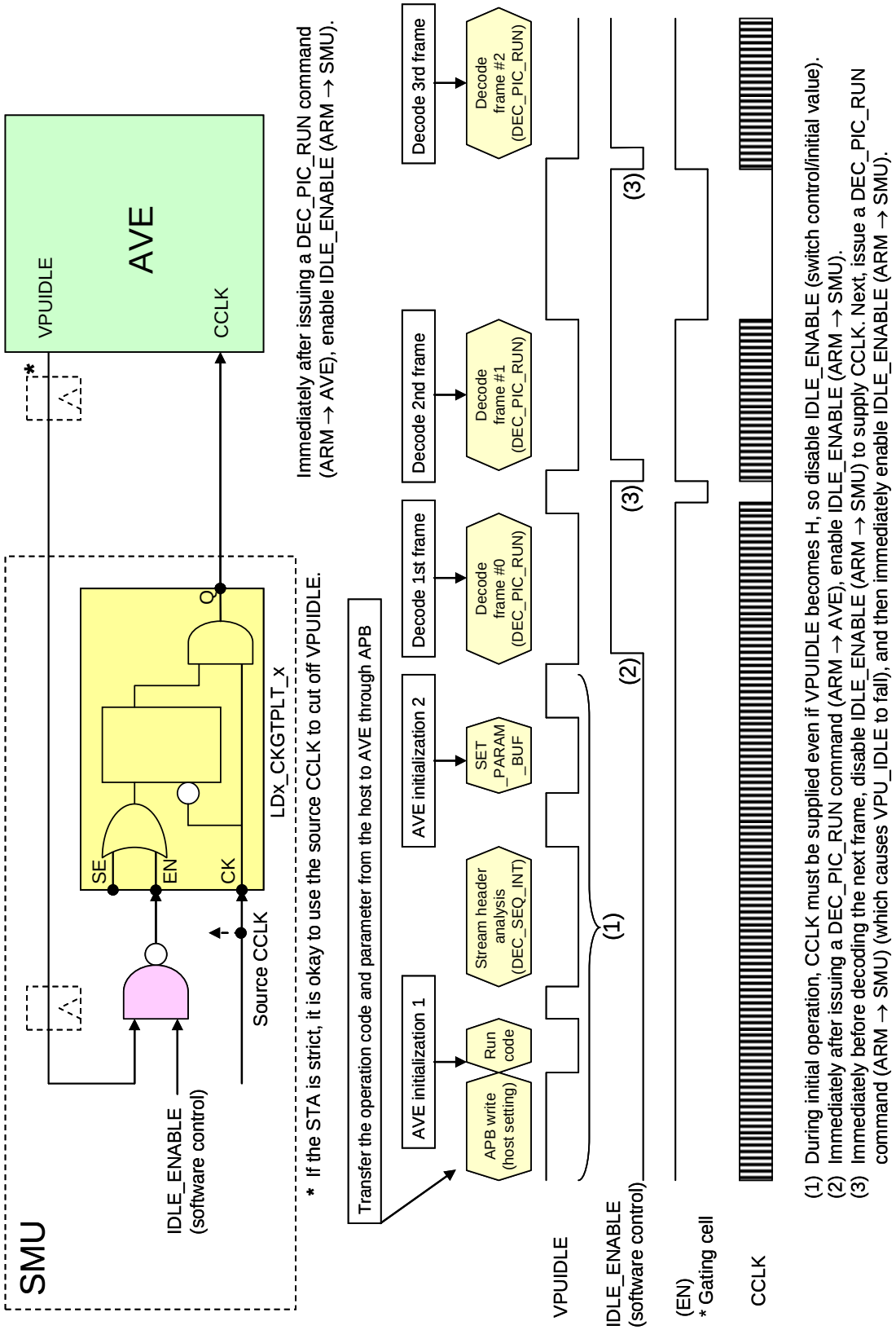
3.1.2 Resets

The AVE requires that the three reset signals below be input.
There are no timing constraints on inputting these signals with respect to the clocks.

Reset Name	Reset Function	Remark
creset_n	Used for the core	Asynchronous reset
areset_n	Used for the AXI interface	Asynchronous reset
preset_n	Used for the APB interface	Asynchronous reset

3.2 VPUIDLE Operation

Figure 3-1. VPUIDLE Operation



3.3 Asynchronous Interface

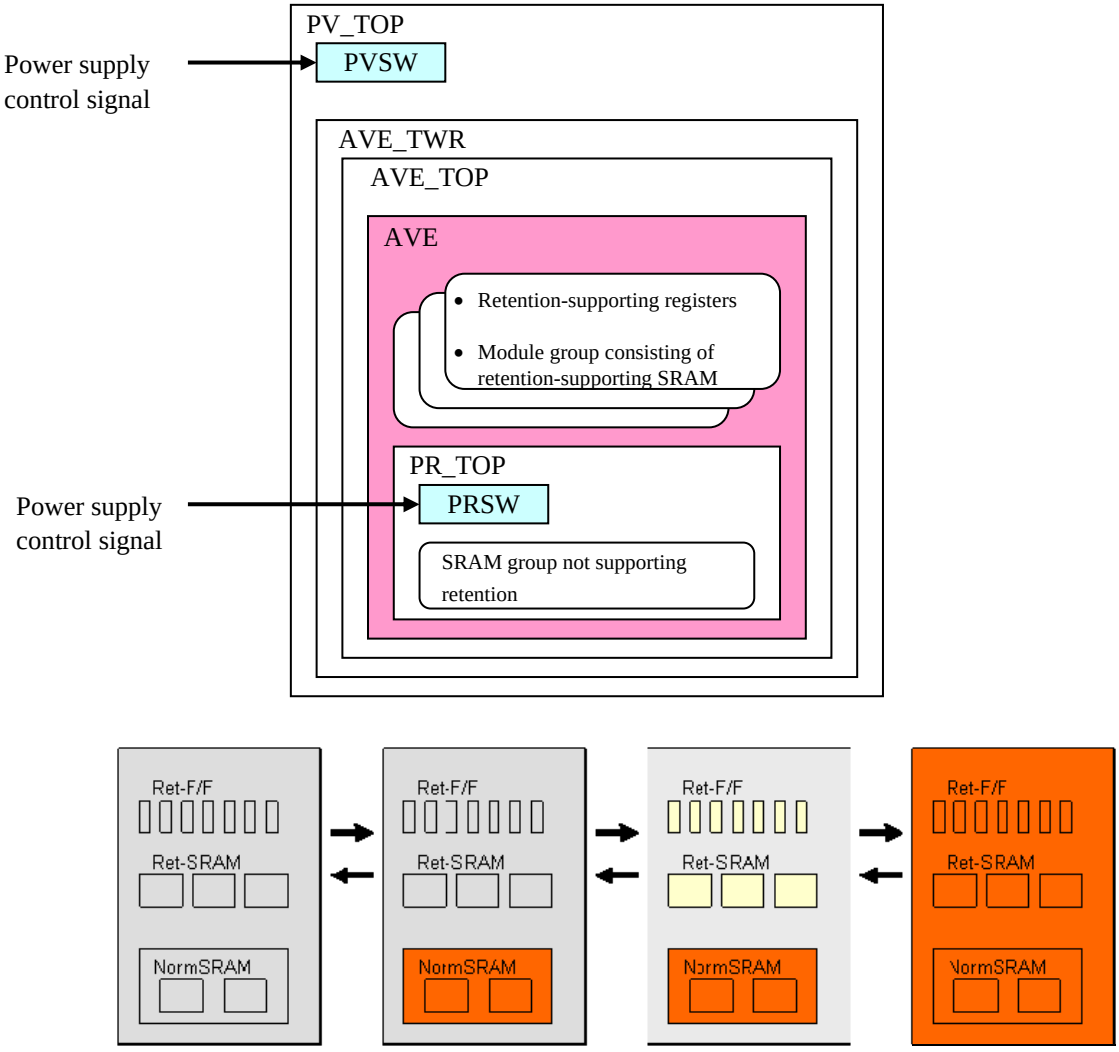
The AVE has three clock input pins, and their signals can be input completely out of sync with each other.
The configurations of asynchronous circuits in the IP core are guaranteed to work by the IP core specifications.

3.4 Changes to the IP Core

3.4.1 Changes to the power supply isolation layer

The AVE uses a wrapper layer set up as a power supply isolation area (PV domain).
The AVE uses registers and SRAM that support retention so register and SRAM values can be retained when the power supply switch is off, but some SRAM cannot retain values and the power domain for such SRAM is therefore separate (the PR domain).

Figure 3-2. Power Supply Isolation Configuration

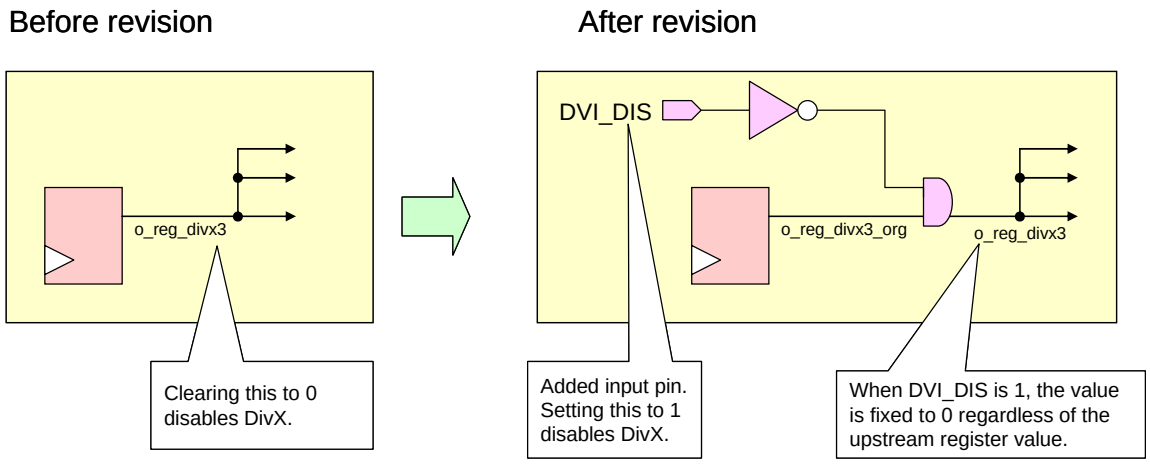


Power Supply Status	All Domains Off	(Power Supply Transition)	Retention	All Domains On
Assumed operation	When AVE is not used	(Power supply transition)	Power saving mode used between frame-decoding operations	When decoding
PR	Off	On	On	On
PV	Off	Off	Retention	On

3.4.2 Addition of logic to disable DivX

The DVI_DIS signal, which can disable DivX at the hardware level, has been added due to royalty considerations. DivX can be disabled by fixing DVI_DIS to high level, without taking action such as connecting to fuse output.

Figure 3-3. Hardware Specifications for the Added DVI_DIS Logic



3.4.3 BUSCLKREQ additions

The logic for four CLK request signals used for AXI has been added for BUS1.

- RBUSCLKREQ0 CLK request for reading from the primary AXI
- WBUSCLKREQ0 CLK request for writing to the primary AXI
- RBUSCLKREQ1 CLK request for reading from the secondary AXI
- WBUSCLKREQ1 CLK request for writing to the secondary AXI

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		Page	Summary
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2.00	Jun 7, 2010	—	Incremental update from comments to the 1.0.
3.00	May 31, 2011	—	APPENDIX deletion.
4.00	Sep 30, 2011	—	Incremental update from comments to the 3.0.

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