User's Manual

Timer

User's Manual

Multimedia Processor for Mobile Applications
EMMA Mobile ™ EV2

Renesas Electronics
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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the EMMA Mobile EV2. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Data Sheet	Hardware overview and electrical characteristics	EMMA Mobile EV2 Datasheet	R19DS0010EJxxxx
User's manual (1chip)	Hardware whole specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description	EMMA Mobile EV2 User's manual 1chip	R19UH0036EJxxxx
User's manual (module)	Hardware each macro specifications and operation description.	EMMA Mobile EV2 User's manual each module	See below

Document Name	Document No.	Document Name	Document No.
1chip	R19UH0036EJxxxx	DMA Controller	R19UH0043EJxxxx
System Management Unit	R19UH0037EJxxxx	LP-DDR/DDR2 Controller	R19UH0039EJxxxx
Timer (This manual)	R19UH0054EJxxxx	SD Memory Card Interface	R19UH0061EJxxxx
System Timer	R19UH0055EJxxxx	SDIO Interface	R19UH0042EJxxxx
HD Video Decoder	R19UH0056EJxxxx	CF Card Interface	R19UH0062EJxxxx
Rotator	R19UH0057EJxxxx	Unified Serial Interface	R19UH0047EJxxxx
Resizer	R19UH0058EJxxxx	UART interface	R19UH0040EJxxxx
Image Composer	R19UH0038EJxxxx	USB 2.0 Host Controller	R19UH0045EJxxxx
LCD Interface	R19UH0044EJxxxx	USB 2.0 Function Controller	R19UH0034EJxxxx
ITU-R BT.656 Interface	R19UH0059EJxxxx	IIC Interface	R19UH0052EJxxxx
Digital Terrestrial TV Interface	R19UH0048EJxxxx	General Purpose I/O Interface	R19UH0041EJxxxx
Camera Interface	R19UH0060EJxxxx	Pulse Width Modulation Interface	R19UH0063EJxxxx

4 digits of end shows the version.

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names

Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.

Examples the PM03 bit in the PM0 register

P3_5 pin, VCC pin

(2) Notation of Numbers

The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.

Examples Binary: 11b or 11

Hexadecimal: EFA0h

Decimal: 1234

3. Register Notation

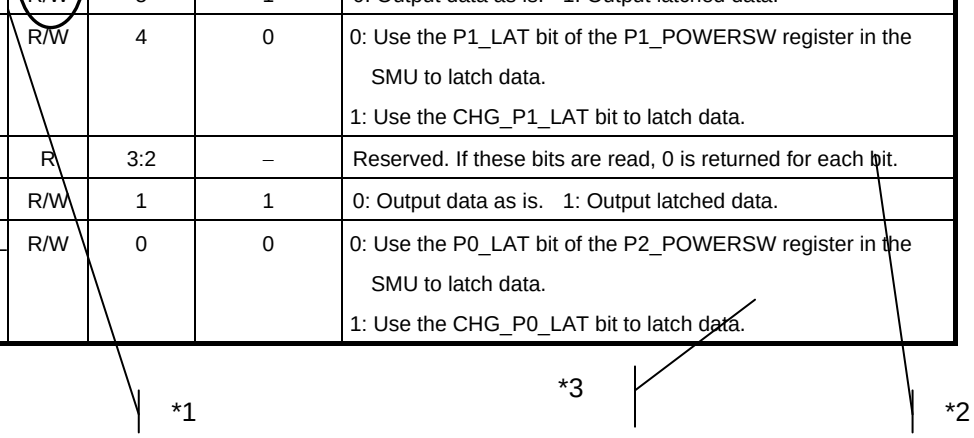
The symbols and terms used in register diagrams are described below.

x.x.x XXX register

This register (XXXXXXX: xxxx_xxxxh) …..

7	6	5	4	3	2	1	0
Reserved		CHG_P1_LAT	LATCH_P1_SEL	Reserved		CHG_P0_LAT	CHG_P0_LAT_SEL

Name	R/W	Bit No.	After Reset	Description
LATCH_P2_SEL	R/W	8	0	0: Use the P2_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P2_LAT bit to latch data.
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P1_LAT	R/W	5	1	0: Output data as is. 1: Output latched data.
LATCH_P1_SEL	R/W	4	0	0: Use the P1_LAT bit of the P1_POWERSW register in the SMU to latch data. 1: Use the CHG_P1_LAT bit to latch data.
Reserved	R	3:2	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P0_LAT	R/W	1	1	0: Output data as is. 1: Output latched data.
CHG_P0_LAT_SEL	R/W	0	0	0: Use the P0_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P0_LAT bit to latch data.



*1

R/W: Read and Write.

R: Read only.

W: Write only.

-: Nothing is assigned.

*2

Reserved bit.

Reserved bit. Set to specified value.

*3

・ Nothing is assigned.

Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.

・ Do not set to a value.

Operation is not guaranteed when a value is set.

・ Function varies according to the operating mode.

The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Register
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

Table of Contents

1. Overview

The timer module (TIM) is a programmable timer counter that enables 32-bit counting (1 to FFFF_FFFFH).

1.1 Features

(1) When a timer counts out (counts up to the user-set count value), the timer count value returns to 0 (0000_0000H) and the timer starts counting again (free-run counting).

(2) The TOUT signal is asserted each time a timer counts out and the TOUT signal is output for two TIN clock cycles.

(3) Once the TIM registers are set up and the timer starts counting, the TIM continues counting as described in (1) as long as the TIN clock is supplied, even if the APB bus clock (PCLK) is stopped.

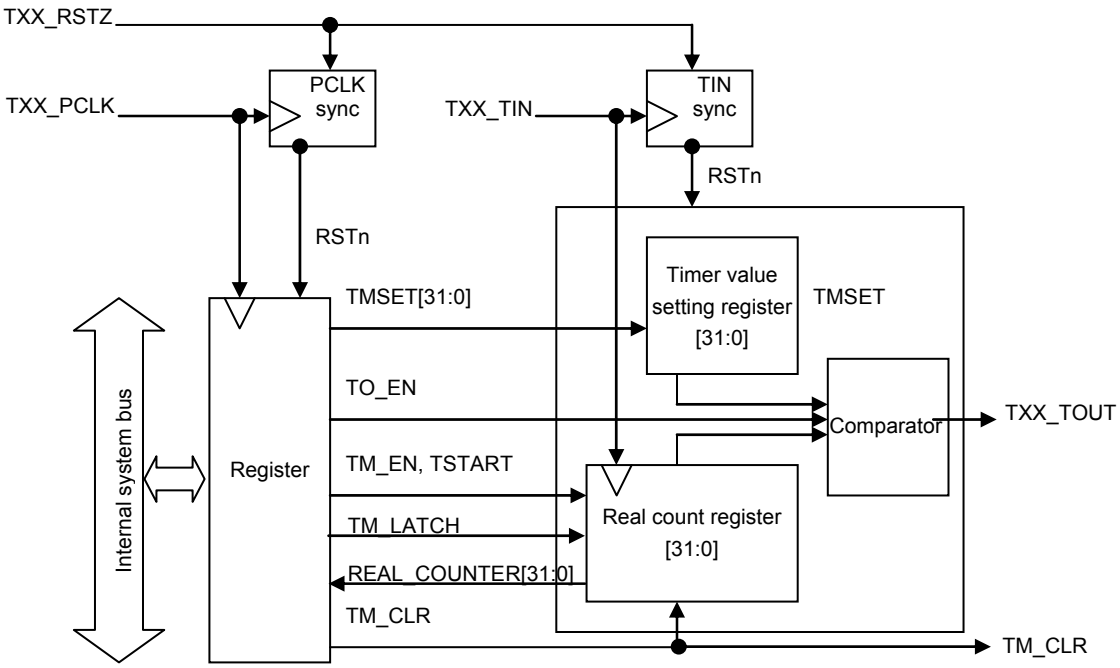
(4) The timer count set value can be changed while the timer is counting.

(5) TIM has 15 functionally equivalent timer modules (TI0 to TI3, TW0 to TW4, and TG0 to TG5).

Tout is connected to an interrupt module (INT).

1.2 Block Diagram

Figure 1-1 Block Diagram



2. Registers

TIM has 256-byte register spaces for each module (TI0 to TI3, TW0 to TW4, and TG0 to TG5), which have different offset addresses.

2.1 Offset Address

PB1_PADDR[31:0]	Module
E000_0000H	TI0
E000_0100H	TI1
E000_0200H	TI2
E000_0300H	TI3
E000_1000H	TW0
E000_1100H	TW1
E000_1200H	TW2
E000_1300H	TW3
E000_1400H	TW4
E000_2000H	TG0
E000_2100H	TG1
E000_2200H	TG2
E000_2300H	TG3
E000_2400H	TG4
E000_2500H	TG5

2.2 Register List

Each TIM register consists of 32 bits.

Address	Register Name	Symbol	R/W	After Reset
00H	Timer operation register	xxx_OP	R/W	0000_0000H
04H	Timer clear register	xxx_CLR	W	0000_0000H
08H	Timer value setting register	xxx_SET	R/W	0000_0000H
0CH	Real count read register	xxx_RCR	R	0000_0000H
10H	Reserved	–	–	–
14H	Timer value setting monitor register	xxx_SCLR	R/W	0000_0000H
18H	One Shot start register	xxx_ONE	W	0000_0000H
1CH	INT asserting period setting register	xxx_INT	R/W	0000_0000H
20H to FCH	Reserved	–	–	–

(xxx = TI0/TI1/TI2/TI3/TW0/TW1/TW2/TW3/TW4/TG0/TG1/TG2/TG3/TG4/TG5)

Operation when a reserved area is accessed:

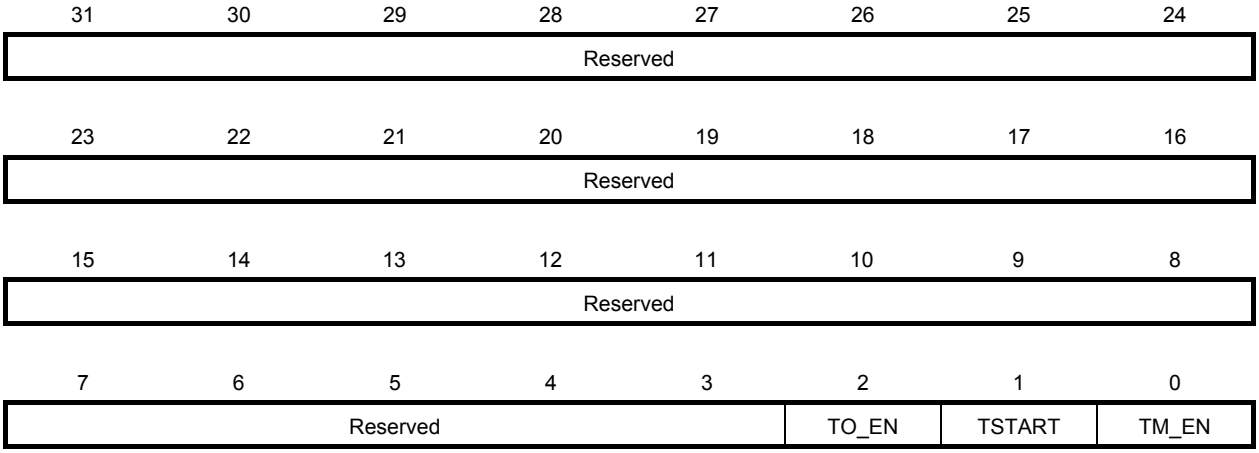
Write: Ignored (invalid)

Read: Zeros are returned.

2.3 Register Details

2.3.1 Timer operation register

This register (xxx_OP: xxxx_0000H) control the timer operations.



Name	R/W	Bit No.	After Reset	Function
Reserved	–	31:3	0000_0000H	Reserved.
TO_EN	R/W	2	0	Specifies whether to assert the TOUT signal. 0: Does not assert the TOUT signal even if timer counting times out. 1: Asserts the TOUT signal when timer counting times out.
TSTART	R/W	1	0	Starts timer counting (valid when TM_EN = 1) 0: Does not start timer counting. (The internal timer count register retains the current value.) 1: Starts timer counting. (The internal timer count register is incremented per TIN clock cycle).
TM_EN	R/W	0	0	Specifies whether to enable the timer operation. 0: Disables the timer operation. The internal timer count register value is reset to 0. 1: Enables the timer operation.

Caution Make sure that the period of enable won't be 5×PCLK+4×TIN under.

2.3.2 Timer clear register

This register (xxx_CLR: xxxx_0004H) clears the internal timer count registers.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved						TCR_CLR	Reserved

Name	R/W	Bit No.	After Reset	Function
Reserved	–	31:2	0000_0000H	Reserved.
TCR_CLR	W	1	0	Clears the internal timer count registers. 0: No operation 1: Clears the internal timer count registers. This bit is automatically cleared to “0”. (Re-setting “0” is unnecessary). For details, see **4.4 Timer count value clear operation**.
Reserved	–	0	0	Reserved.

2.3.3 Timer value setting register

This register (xxx_SET: xxxx_0008H) specifies the value at which the timer counts out.

31	30	29	28	27	26	25	24
TMSET_31	TMSET_30	TMSET_29	TMSET_28	TMSET_27	TMSET_26	TMSET_25	TMSET_24

23	22	21	20	19	18	17	16
TMSET_23	TMSET_22	TMSET_21	TMSET_20	TMSET_19	TMSET_18	TMSET_17	TMSET_16

15	14	13	12	11	10	9	8
TMSET_15	TMSET_14	TMSET_13	TMSET_12	TMSET_11	TMSET_10	TMSET_9	TMSET_8

7	6	5	4	3	2	1	0
TMSET_7	TMSET_6	TMSET_5	TMSET_4	TMSET_3	TMSET_2	TMSET_1	TMSET_0

Name	R/W	Bit No.	After Reset	Function
TMSET_[31:0]	R/W	31:0	0000_0000H	Specifies the value at which the timer counts out. Set a desired value minus 1. Specify a value greater than or equal to 2. When a timer counts out, the TOUT signal is asserted (when TO_EN = 1) and the real count register is reset to 0. For details, see **4.5 Rewriting the Timer Count Value**.

Caution Before setting values in this register, read the TM_SCLR bit of the timer value setting monitor register (xxx_SCLR: xxxx_xx14H), confirm that the LSB of the read value is "0", and then wait for at least two or three TIN clock cycles.

2.3.4 Real count read register

This register (xxx_RCR: xxxx_000CH) is used to read the real count registers (current timer value).

31	30	29	28	27	26	25	24
RCR_31	RCR_30	RCR_29	RCR_28	RCR_27	RCR_26	RCR_25	RCR_24
23	22	21	20	19	18	17	16
RCR_23	RCR_22	RCR_21	RCR_20	RCR_19	RCR_18	RCR_17	RCR_16
15	14	13	12	11	10	9	8
RCR_15	RCR_14	RCR_13	RCR_12	RCR_11	RCR_10	RCR_9	RCR_8
7	6	5	4	3	2	1	0
RCR_7	RCR_6	RCR_5	RCR_4	RCR_3	RCR_2	RCR_1	RCR_0

Name	R/W	Bit No.	After Reset	Function
RCR_[31:0]	R	31:0	0000_0000H	Used to read the real count register values.

2.3.5 Timer value setting monitor register

This register (xxx_SCLR: xxxx_0014H) is used to monitor the timer value setting.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							TM_SCLR

Name	R/W	Bit No.	After Reset	Function
Reserved	–	31:1	0000_0000H	Reserved.
TM_SCLR	R/W	0	0	Monitors the timer value setting. This bit holds 1H until a count value is set to the timer value setting register. After a value is set, this bit is automatically reset to 0H.

Remarks 1. This bit is not automatically reset to 0 when the TM_EN bit of the timer operation register is set to 0.

2.3.6 One Shot start register

This register (xxx_ONE: xxxx_0018H) is used to monitor the timer value setting.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							TM_ONE

Name	R/W	Bit No.	After Reset	Function
Reserved	–	31:1	0000_0000H	Reserved.
TM_ONE	W	0	0	Only a round does a timer count in Write. (The internal timer count register is incremented per clock cycle).

Note : Set a bit of xxx_OP register [1:0] (TM_EN and TSTART) as 0.

2.3.7 INT asserting period setting register

This register (xxx_INT: xxxx_001CH) is interrupt asserting period setting.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							TM_ONE

Name	R/W	Bit No.	After Reset	Function
Reserved	–	31:1	0000_0000H	Reserved.
TM_INT	R/W	0	0	0 : An asserting period of INT is set in 2CLK@Txx_CLK. 1 : An asserting period of INT is set in 8CLK@Txx_CLK.

3. Description of Functions

3.1 Status After Reset

TIM is set as follows after reset.

- TOUT signal level: 0
- Timer count: Stop
- Timer setting register: 0x0000_0000
- Internal timer count register: 0x0000_0000

3.2 Calculation of Timer Count

A wide range of counting is possible by using a combination of input frequency and timer count settings. The following table shows setting examples. The term [seconds] in this table refers to the interval at which the TOUT signal is asserted.

TIN (Input Frequency)	Timer Count Setting Value		
	0000_0000H	0000_FFFFH	FFFF_FFFFH
32.768 kHz	30.52×10^{-6} [seconds]	2 [seconds]	131072 [seconds]
15.616 MHz	64.04×10^{-9} [seconds]	4.20×10^{-3} [seconds]	275.04 [seconds]

Expression: (1/TIN) × (Count setting value + 1)

Example: $1/32.768\ \text{kHz} \times (0000\_FFFFH + 1) = 30.52 \times 10^{E-6} \times 65536 = 2$ [seconds]

3.3 10ms timer

It's possible to use to use 32KHz for a timer clock more as 10ms timer.
But, it's subject to the following restrictions.

- It shift from 10ms to the TOUT space of the each time a little (10.00977ms/9.97925ms).
  But, an error isn't accumulated because 250ms is measured correctly.

- It's a timer clock (PLL3 division /32KHz/32.768KHz) during TIM macro movement, it can't be changed.
  (Movement isn't guaranteed.)

The register setting when using TI0 as 10ms timer, is as follows.

- TI0 register setting (timer setting (TM_SET) register setting)
  0xE000_0008/0x0000_013F（319d）(address/data)

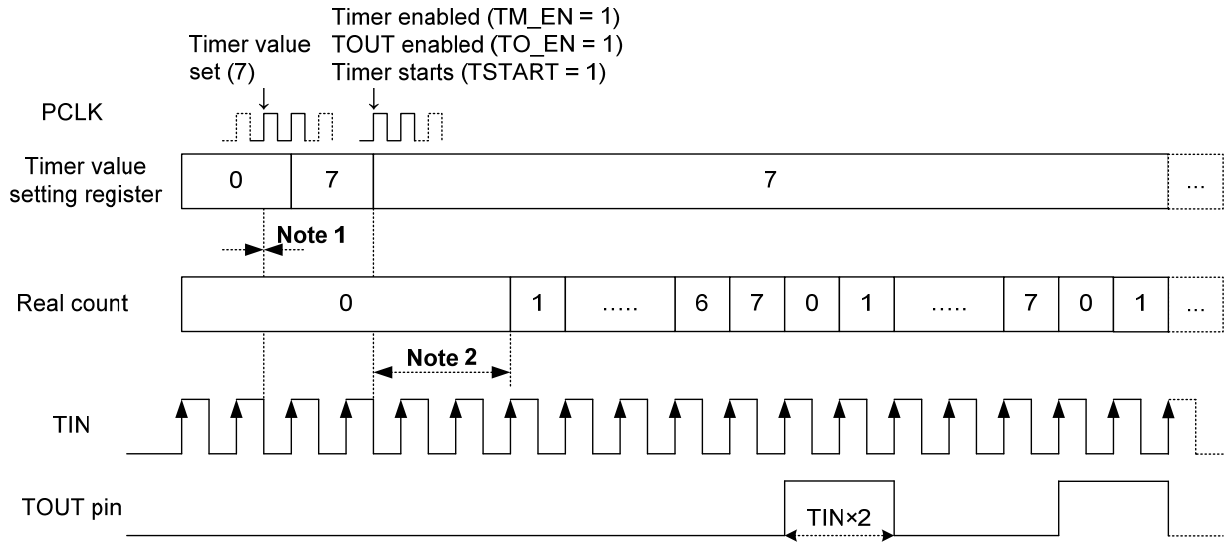
- ASMU register setting (TI0TIM_SEL (setting register for TI0_TIN))
  0xE011_0600/0x0000_0002 (address/data)

4. Usage

4.1 Starting the Timer

(1) Set up the timer value setting register: TM_SET = count value
(2) Enable the timer: TM_EN = 1 (bit 0 of xxx_OP register)
(3) Enable TOUT signal assertion: TO_EN = 1 (bit 2 of xxx_OP register)
(4) Start timer counting: TSTART = 1 (bit 1 of xxx_OP register)

Figure 4-1. Starting the Timer



(Example: When the timer value is set to 7)

<1> Steps (2) to (4) can be performed with a single write.

<2> The TOUT signal is asserted under the following conditions.
(1) The timer value setting register (TM_SET) is set to a value other than “0”
(2) Asserting the TOUT signal is enabled (TO_EN = 1)
(3) The timer is counting (TM_EN = 1, TSTART = 1).

With these settings, the TOUT signal is asserted every 8 TIN clock cycles.
To set the TOUT signal assertion cycle to 8, set the timer value setting register to 7 (8 − 1).

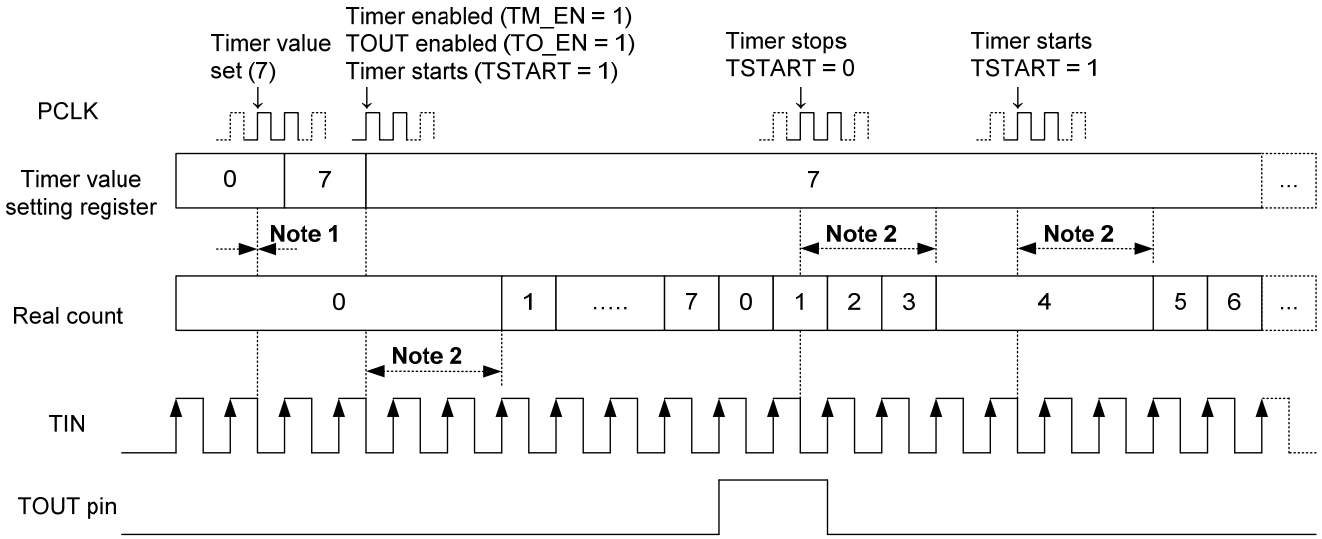
<3> The internal timer count register operates even if the system clock (PCLK) is stopped after the timer starts, as long as the TIN clock is supplied.
The TOUT signal is asserted according to the timer value setting (every 8 clock cycles in this example).

Notes 1. Registers are set in synchronization with PCLK, and real counting occurs in synchronization with TIN. PCLK and TIN are asynchronous.
2. The TSTART, TO_EN, TM_EN, and TM_SET bits are set in synchronization with PCLK. However, because real counting occurs in synchronization with TIN, the setting of the TSTART, TO_EN, TM_EN, and TM_SET bits will not be applied for 2 or 3 TIN cycles. This is the case regardless of whether the timer is set again while it is counting or when it is stopped.

4.2 Pausing the Timer

(1) Stop timer counting (with count values retained): TM_EN = 1, TSTART = 0 (pause for a certain period)
(2) Restart timer counting: TM_EN = 1, TSTART = 1

Figure 4-2. Pausing the Timer



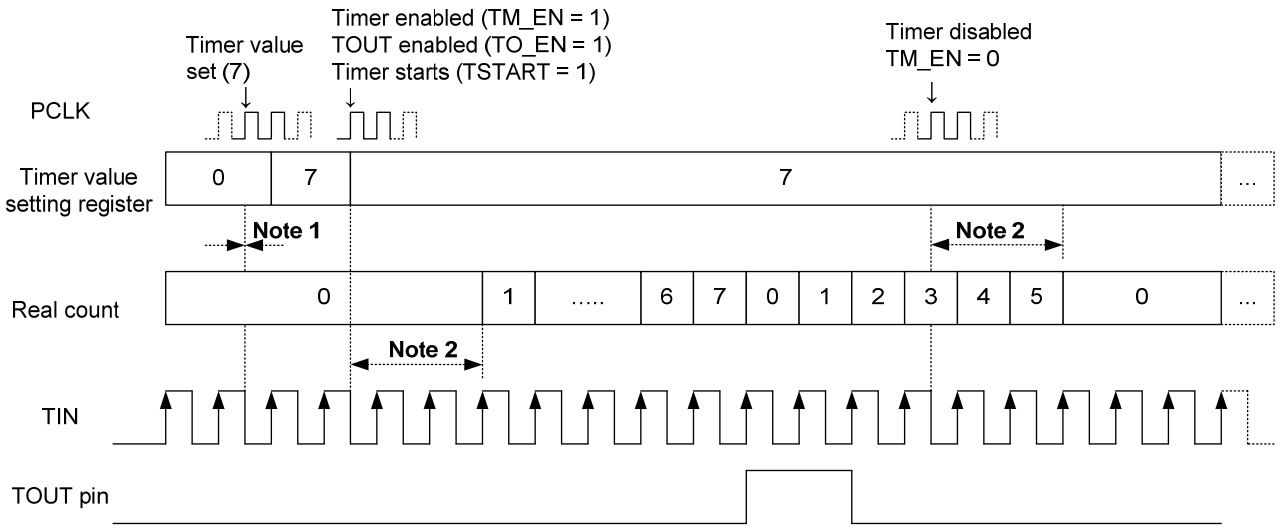
Notes 1. Registers are set in synchronization with APBCLK, and real counting occurs in synchronization with TIN. APBCLK and TIN are asynchronous.

2. The TSTART and TM_EN bits are set in synchronization with PCLK. However, because real counting occurs in synchronization with TIN, the setting of the TSTART and TM_EN bits will not be applied for 2 or 3 TIN cycles. This is the case regardless of whether the timer is set again while it is counting or when it is stopped.

4.3 Stopping the Timer

Stop timer counting (internal count value returns to 0): TM_EN = 0, TSTART = *

Figure 4-3. Stopping the Timer



Notes 1. Registers are set in synchronization with PCLK, and real counting occurs in synchronization with TIN. PCLK and TIN are asynchronous.

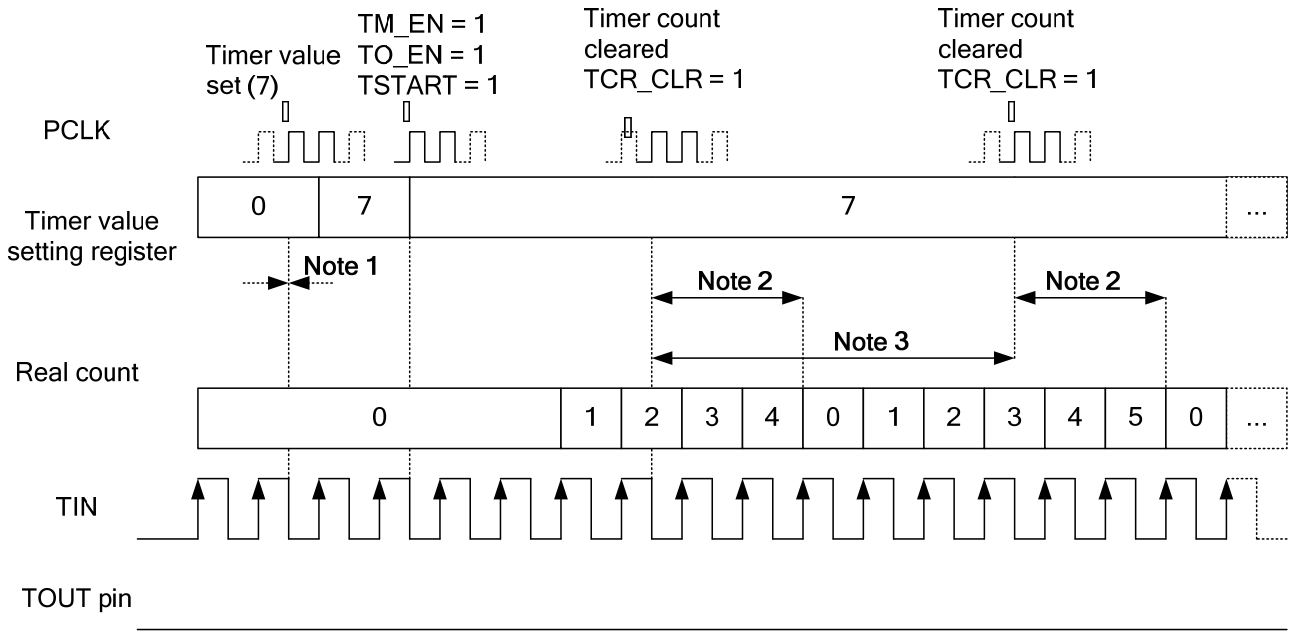
2. The TSTART and TM_EN bits are set in synchronization with PCLK. However, because real counting occurs in synchronization with TIN, the setting of the TSTART and TM_EN bits will not be applied for 2 or 3 TIN cycles. This is the case regardless of whether the timer is set again while it is counting or when it is stopped.

4.4 Clearing the Timer Count Value

The values of the internal timer count register can be cleared to 0 with a single write operation during counting. This operation can be used during clearing of the watchdog timer. (The TOUT signal is not asserted if writing is performed at least once before the timer counts out.)

Clears the timer count: TCR_CLR = 1 (bit 1 of xxx_CLR register)

Figure 4-4. Clearing the Timer Count Value



<1> This bit is automatically cleared to “0” after the timer count value is cleared (TCR_CLR = 1).

Notes 1. Registers are set in synchronization with PCLK, and real counting occurs in synchronization with TIN. PCLK and TIN are asynchronous.

2. After the timer count value is cleared, the timer count is actually cleared one PCLK cycle + two or three TIN cycles later because the value is specified to be cleared in synchronization with PCLK, but is actually cleared in synchronization with TIN.

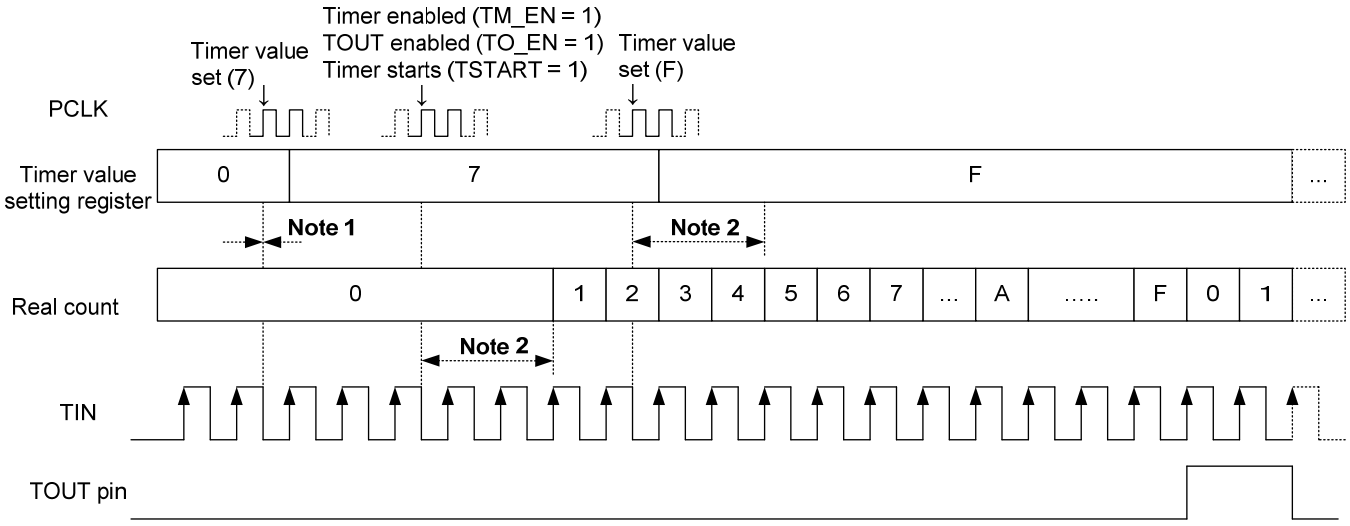
3. When the timer count value is cleared, the signal is output from the register for one PCLK cycle, and clearing takes effect in synchronization with TIN (this takes three cycles). Next, a clear signal in synchronization with TIN is output for one cycle and is synchronized with PCLK again (this takes four cycles). The timer clear register is then cleared to 0, and the clear operation is complete. Therefore, a timer count that is cleared within five PCLK cycles + four TIN cycles is ignored. For the watchdog timer, set the timer value setting register (TM_SET bits) to a value of at least (5 PCLK cycles) + (4 TIN cycles).

4.5 Rewriting the Timer Count Value

The maximum value of real counting can be changed by changing the values of the relevant timer value setting register (TM_SET) while the timer is counting.

(1) Set up the timer value setting register: TM_SET = count value
(2) Enable the timer: TM_EN = 1 (bit 0 of xxx_OP register)
(3) Enable TOUT signal assertion: TO_EN = 1 (bit 2 of xxx_OP register)
(4) Start timer counting: TSTART = 1 (bit 1 of xxx_OP register)
(5) Set up the timer value setting register: TM_SET = count value (count value different from that of (1))

Figure 4-5. Rewriting the Timer Count Value



Notes 1. Registers are set in synchronization with PCLK, and real counting occurs in synchronization with TIN. PCLK and TIN are asynchronous.

2. The TSTART, TO_EN, TM_EN, and TM_SET bits are set in synchronization with PCLK. However, because real counting occurs in synchronization with TIN, the setting of the TSTART, TO_EN, TM_EN, and TM_SET bits will not be applied for 2 or 3 TIN cycles. This is the case regardless of whether the timer is set again while it is counting or when it is stopped.

3. If a value smaller than the real count value is set in the timer value setting register during counting, the timer counts up to FFFF_FFFFH, and then counts up to the preset count value. If this operation causes any problems, read the real count read register and set a value larger than the read value in the timer value setting register.

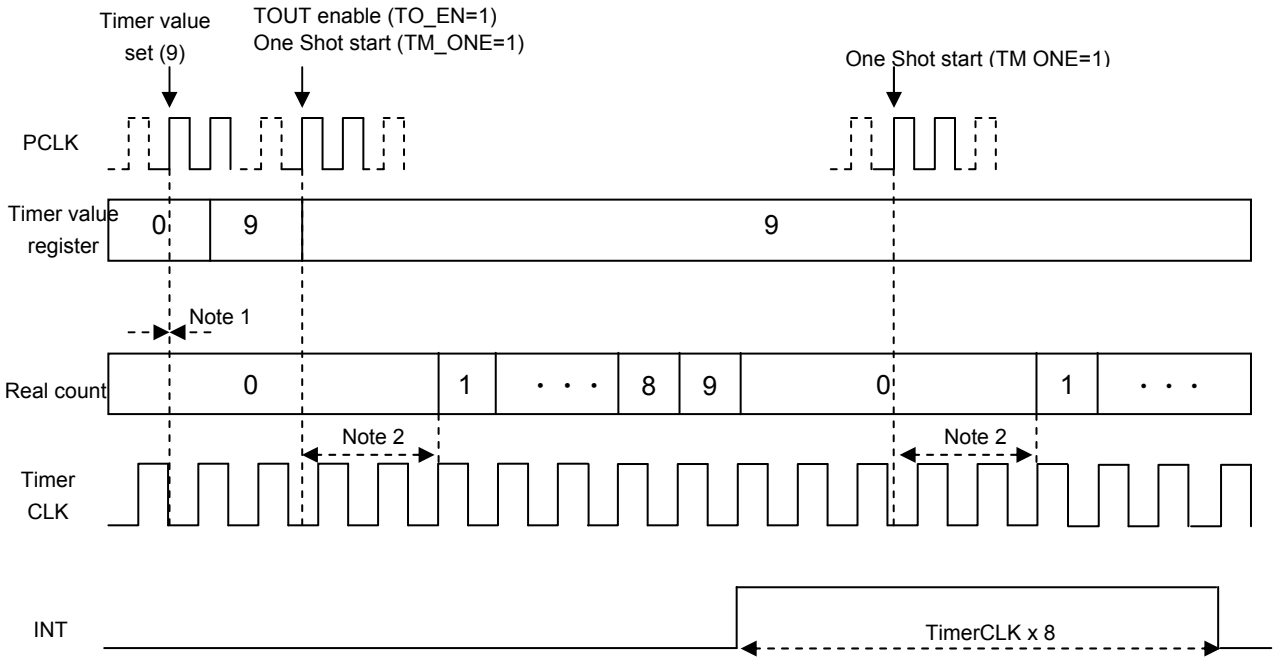
4.6 One shot function

When even going around the price set in a timer setting register, timer movement is suspended.

(1) Set up the timer value setting register: TM_SET = count value
(2) Enable the timer: TM_EN = 0 (bit 0 of xxx_OP register)
(3) Start timer counting: TSTART = 0 (bit 1 of xxx_OP register)
(4) Enable TOUT signal assertion: TO_EN = 1 (bit 2 of xxx_OP register)
(5) Set up the One shot start register: TM_ONE = 1

Example : Timer value = Movement in case of 9 is shown.

Figure 4-6. One shot operation



After Timer Clock asserted a INT terminal in the time which became 10 clocks, a count is suspended. One after a count stop also maintains the value of the timer setting register (TM_SET) and the value of the timer operational register (xxx_OP). When a One Shot start register (TM_ONE) is set once again, a count starts by the One Shot function. After setting a One Shot start register (TM_ONE), when '1' is set in a timer start (TSTART) with a timer and INEBURU of a timer operational register (TM_EN) it doesn't stop at One Shot any more.

(1) The (2) - (4) above-mentioned is possible by once of light operation.
(2) It's when the following 3 conditions were piled, that a INT terminal asserts.
- A timer setting register (TM_SET) is besides the '0'.
- TOUT assert enable setting (TO_EN = 1)
- A timer count is being carried out by the One Shot function (during One Shot start).

(3) When Time Clock is supplied even if he makes them stop PCLK (internal system clock) after a timer start, a timer count register moves.

Notes 1. Registers are set in synchronization with PCLK, and real counting occurs in synchronization with TIN. PCLK and TIN are asynchronous.

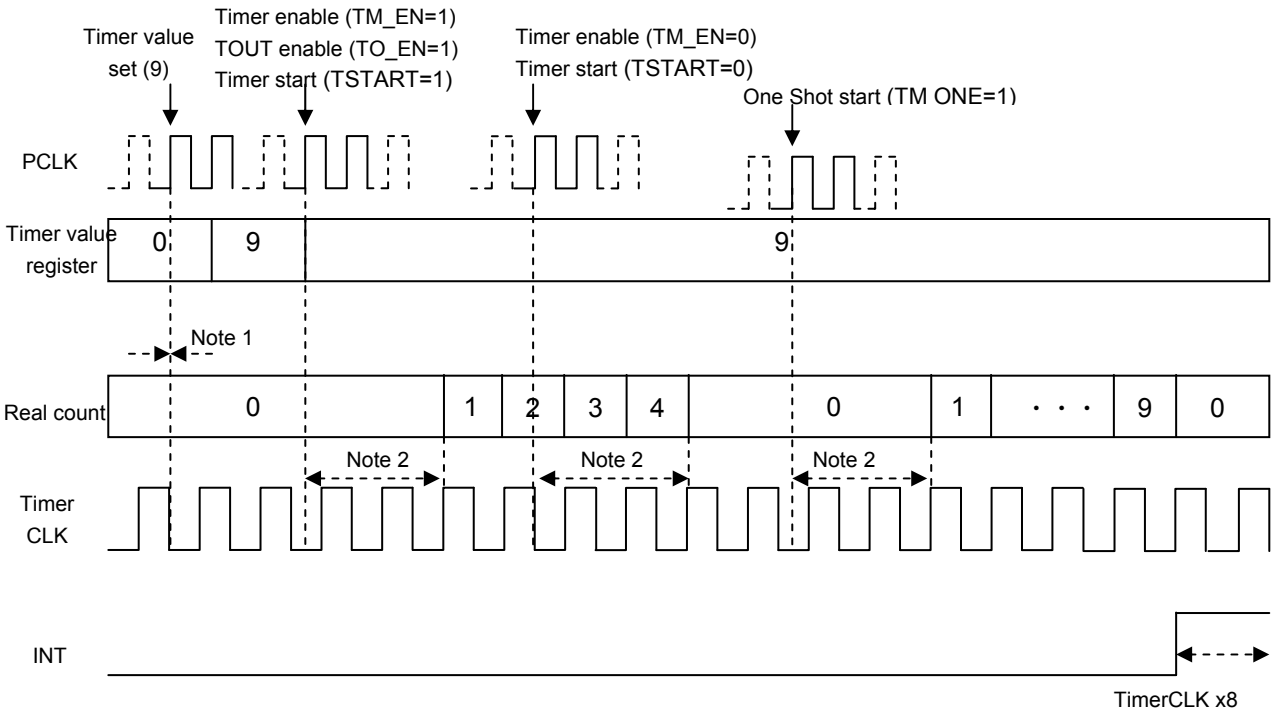
2. The TSTART, TO_EN, TM_EN, and TM_SET bits are set in synchronization with PCLK. However, because real counting occurs in synchronization with TIN, the setting of the TSTART, TO_EN, TM_EN, and TM_SET bits will not be applied for 2 or 3 TIN cycles. This is the case regardless of whether the timer is set again while it is counting or when it is stopped.

4.7 From a repeat timer, change to the One shot function

(1) Set up the timer value setting register: TM_SET = count value
(2) Enable the timer: TM_EN = 1 (bit 0 of xxx_OP register)
(3) Enable TOUT signal assertion: TO_EN = 1 (bit 2 of xxx_OP register)
(4) Start timer counting: TSTART = 1 (bit 1 of xxx_OP register)
Even if a count is certain degree of and finishes.
(5) Timer count stopped (The inner count value returns to 0.) : (TM_EN = 0, TSTART = 0)
(6) Set up the One shot start register: TM_ONE = 1

Example : Timer value = Movement in case of 9 is shown.

Figure 4-7. Change to the One shot function



Even if some degree counts finish after a timer start by 4.1 the starting timer, a timer is stopped, a One Shot start register is set and it's changed to the One Shot function. When changing, the count value is cleared in 0 by timer stop operation, so it isn't necessary to set a timer clear register.

(1) The (2) - (4) above-mentioned is possible by once of light operation.
(2) When Time Clock is supplied even if he makes them stop PCLK (internal system clock) after a timer start, a timer count register moves.

Notes 1. Registers are set in synchronization with PCLK, and real counting occurs in synchronization with TIN. PCLK and TIN are asynchronous.
2. The TSTART, TO_EN, TM_EN, and TM_SET bits are set in synchronization with PCLK. However, because real counting occurs in synchronization with TIN, the setting of the TSTART, TO_EN, TM_EN, and

TM_SET bits will not be applied for 2 or 3 TIN cycles. This is the case regardless of whether the timer is set again while it is counting or when it is stopped.

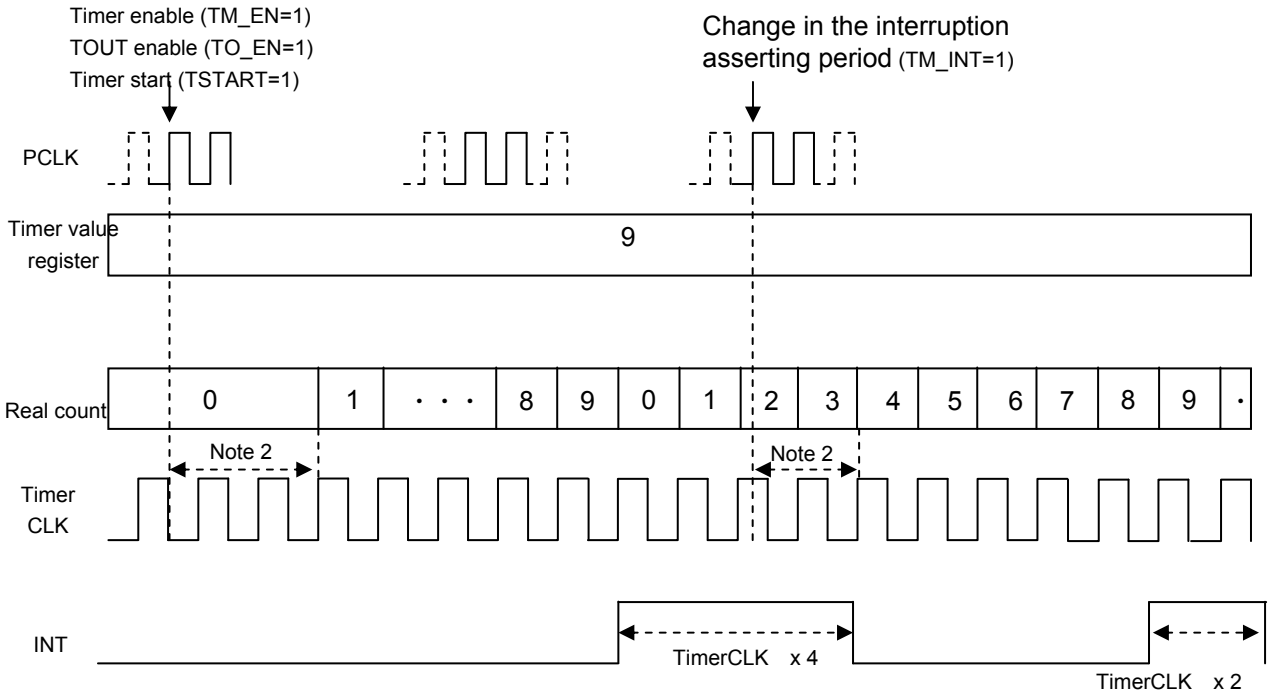
4.8 Change in the interruption asserting period

When an asserting period setting cashier cut in by initialization and asserted (8CLK@TimerClock), and interrupted and cut in and changed the asserting period to 2CLK@TimerClock.

(1) Set up the timer value setting register: TM_SET = count value
(2) Enable the timer: TM_EN = 1 (bit 0 of xxx_OP register)
(3) Enable TOUT signal assertion: TO_EN = 1 (bit 2 of xxx_OP register)
(4) Start timer counting: TSTART = 1 (bit 1 of xxx_OP register)
Interrupting and during asserting.
(5) INT asserting period setting register r: TM_INT = 1

Example : Timer value = Movement in case of 9 is shown.

Figure 4-8. Change in the interruption asserting period



While interruption is effective after a timer start in 4.1, '1' is being set in a INT asserting period setting register. The interruption signal is more effective than 2CLK@Timer Clock, so I synchronize with Timer Clock and invalidate. A period of 2CLK@Timer Clock, it's asserted from the next interruption.

(1) The (2) - (4) above-mentioned is possible by once of light operation.

Notes. The TSTART, TO_EN, TM_EN, and TM_SET bits are set in synchronization with PCLK. However, because real counting occurs in synchronization with TIN, the setting of the TSTART, TO_EN, TM_EN, and TM_SET bits will not be applied for 2 or 3 TIN cycles. This is the case regardless of whether the timer is set again while it is counting or when it is stopped.

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