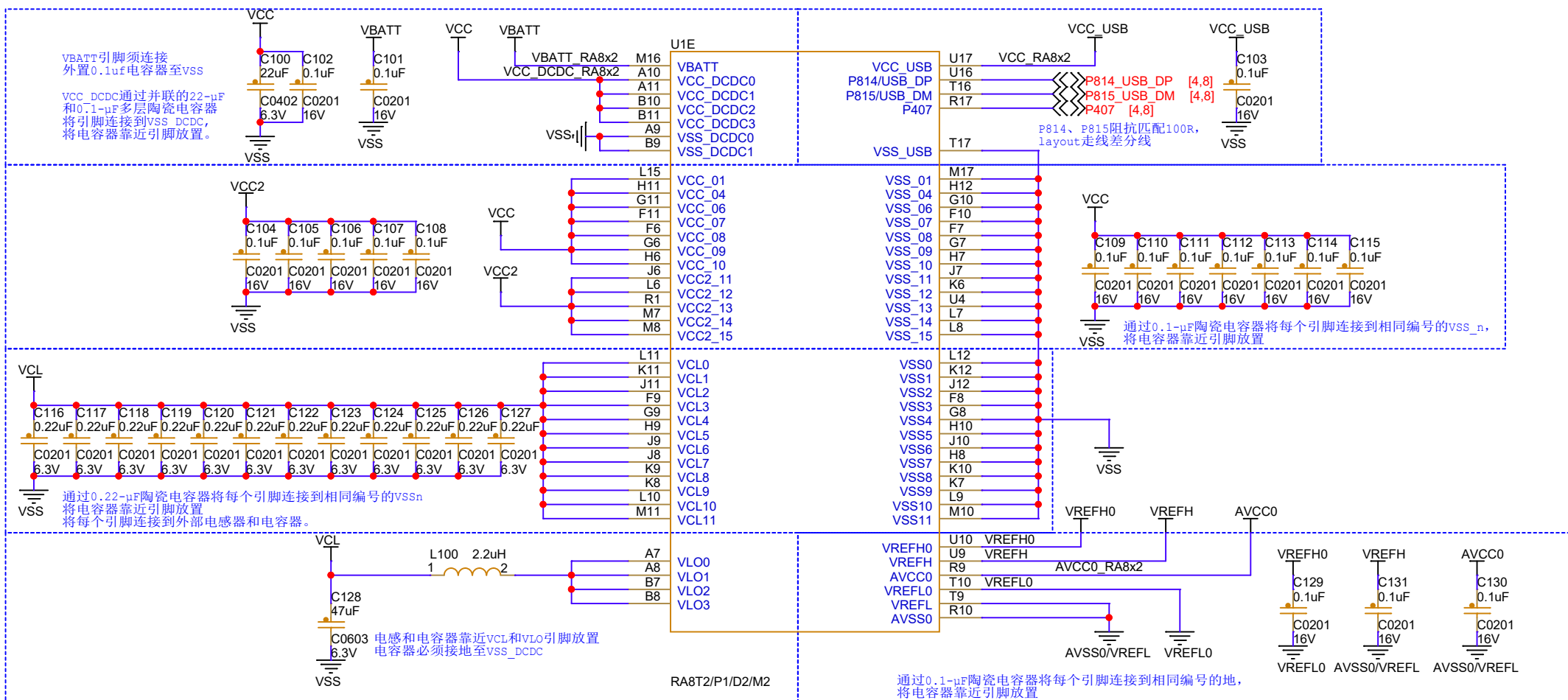


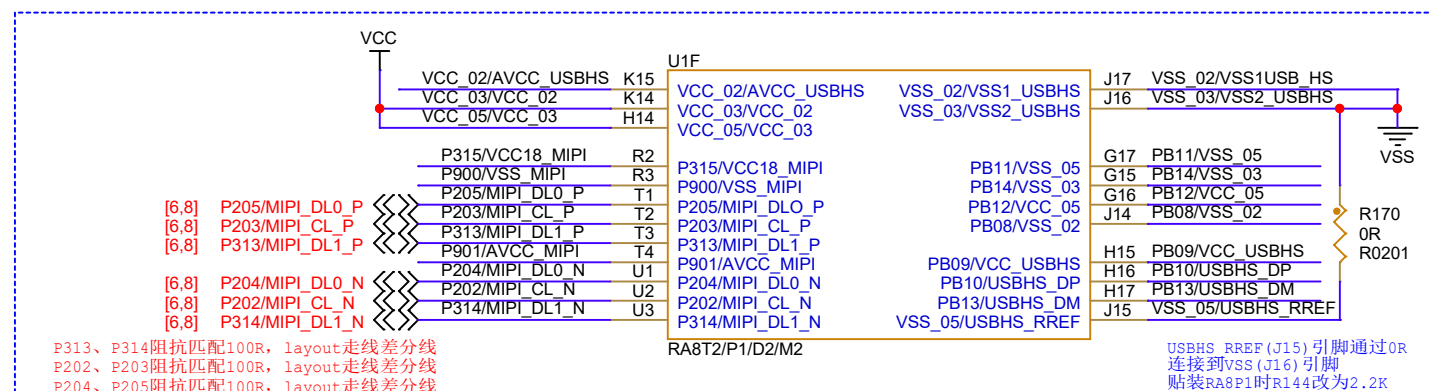
[www.gitee.com/
ramcu/cpk_examples](http://www.gitee.com/ramcu/cpk_examples)

[www.github.com/
renesas/cpk_examples](https://www.github.com/renesas/cpk_examples)

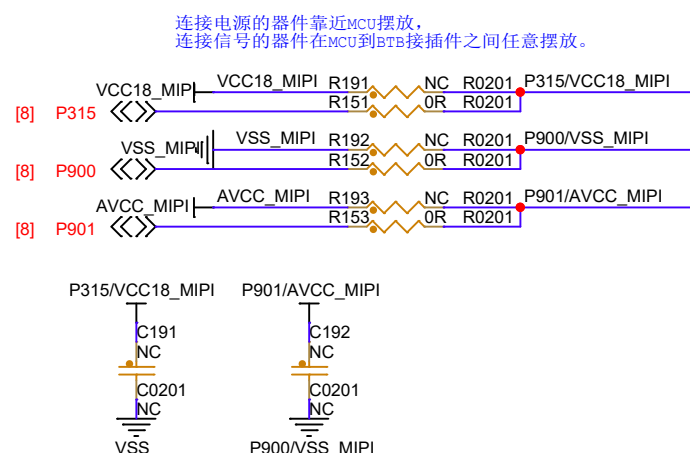


核心板芯片	R7KA8T2L	R7KA8P1K
C168-169	0.1uF	NC
C170	0.1uF	2.2uF
C171-C174	NC	0.1uF
C191-C192	NC	0.1UF
R145-R150	NC	NC
R151-R168	0R	NC
R170	0R	2.20K 1%
L171	NC	120R@100M
R172-R180	NC	0R
R191-R193	NC	0R

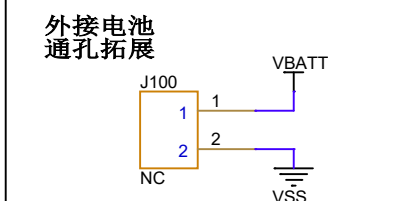
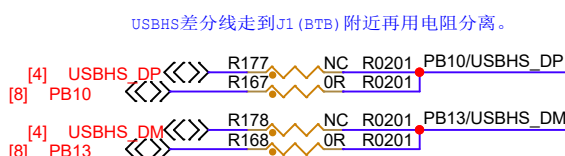
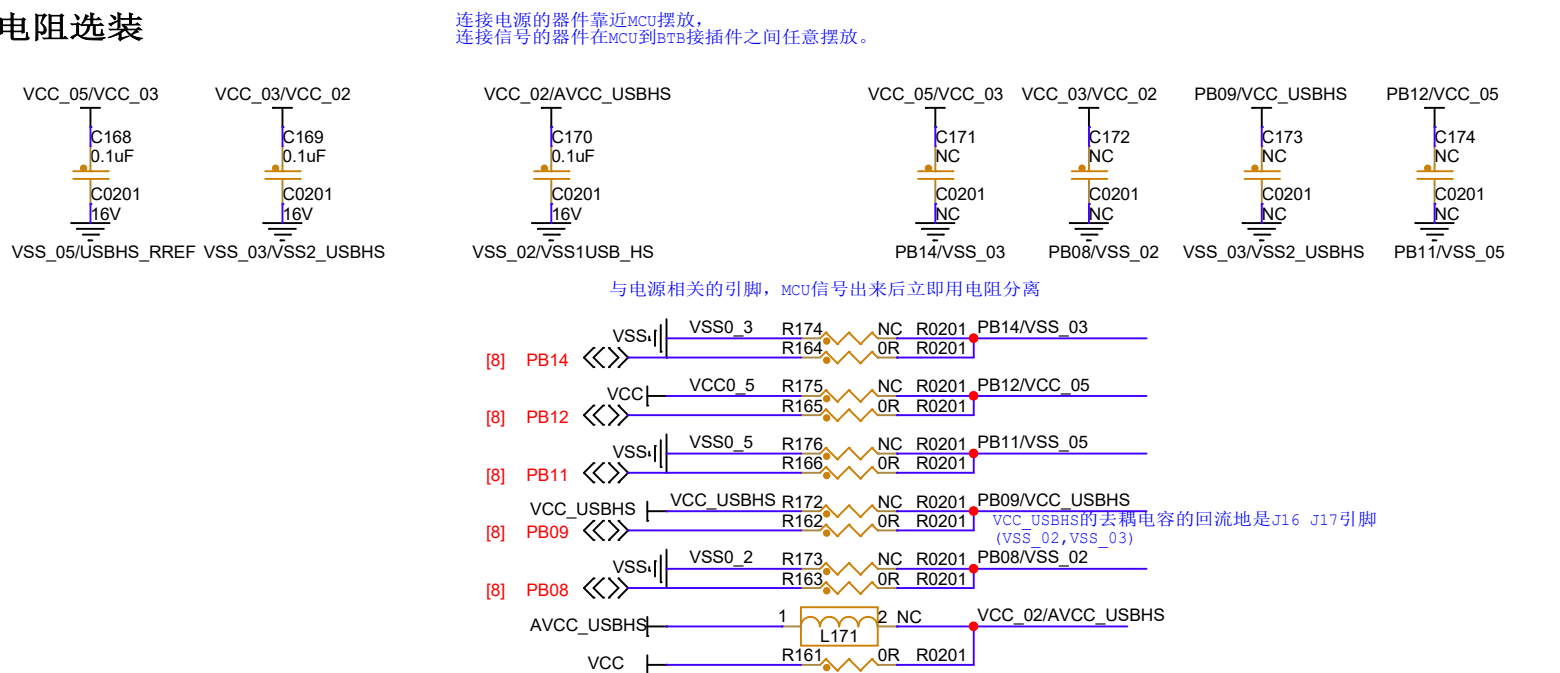
由于RA8P1/D2/M2和RA8T2的部分管脚网络不同，通过选装阻容的方式，应对不同型号的IC贴装。此原理图为贴装RA8T2时的器件贴装。



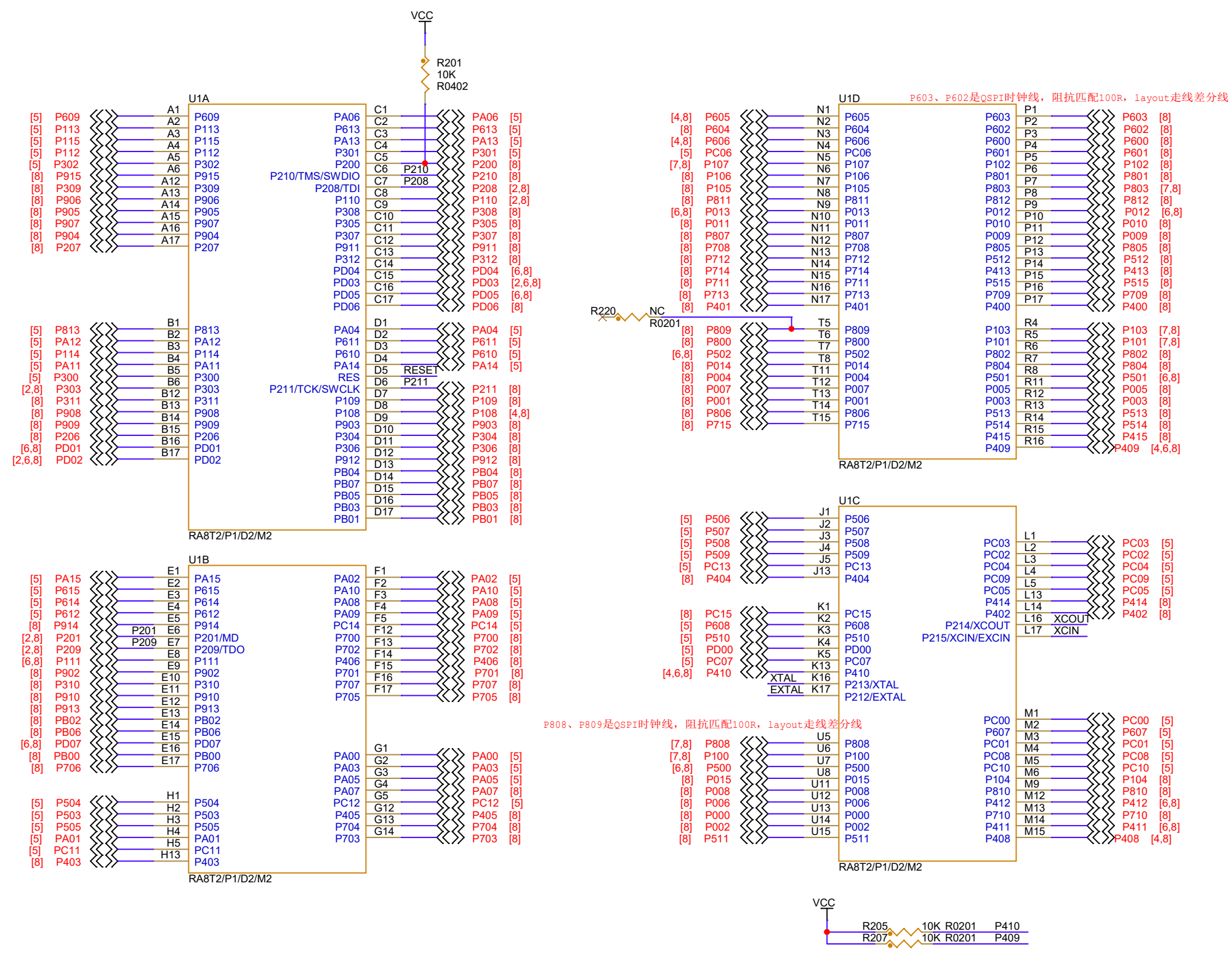
MIPI部分



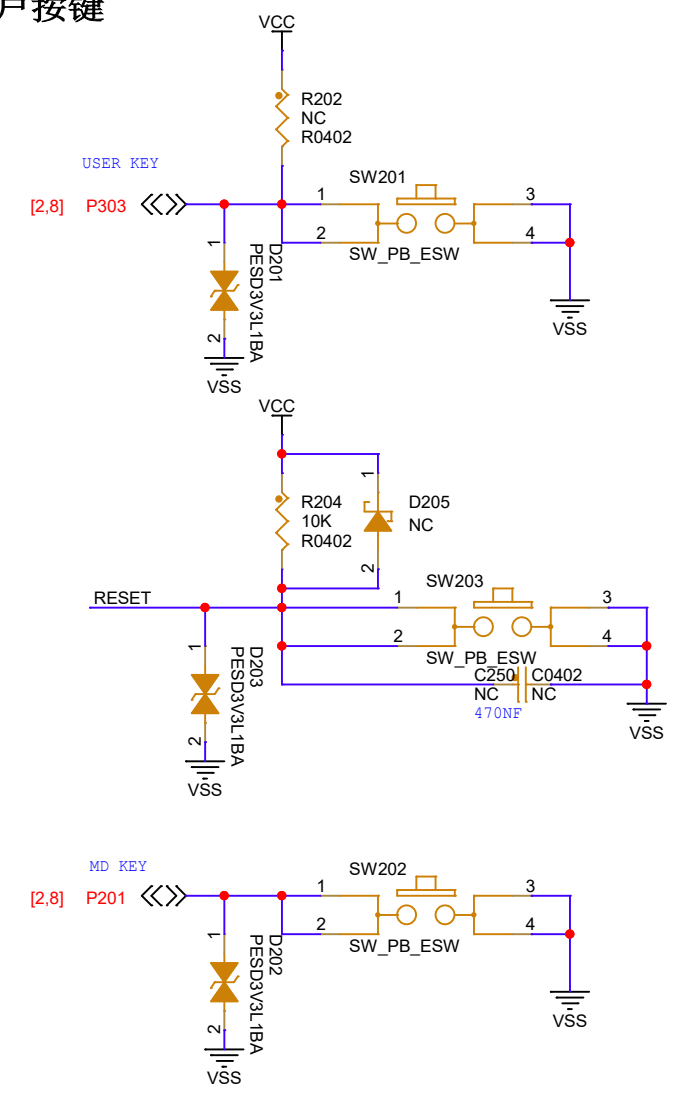
电阻选装



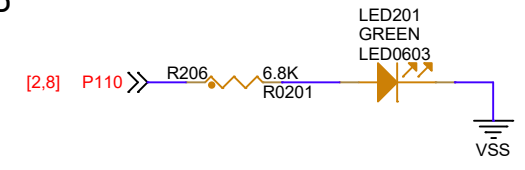
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Title			
CPKNET-RA8T2 核心板			
Size A3	Document Number MCU 电源		Rev V1.1
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用户按键

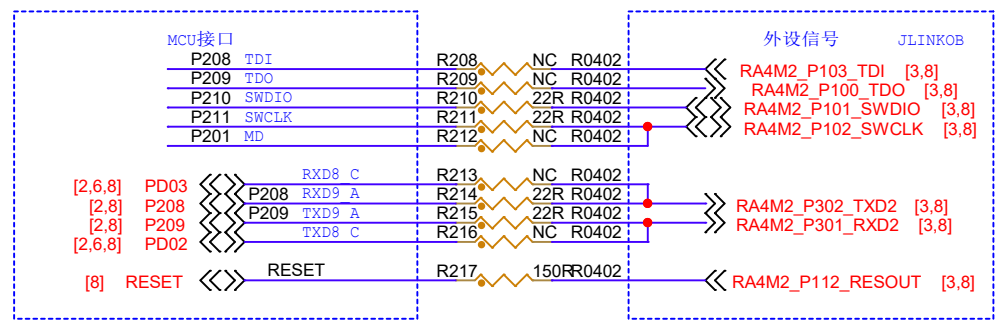


LED

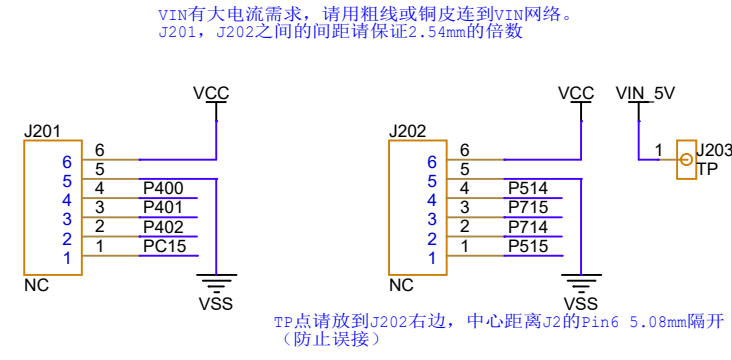


如果使用USB HS，主晶振只能选12/20/24/48MHz

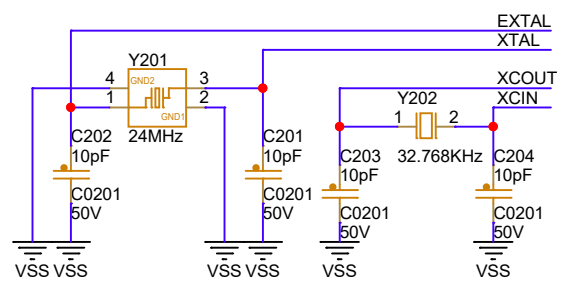
接口信号



通孔拓展

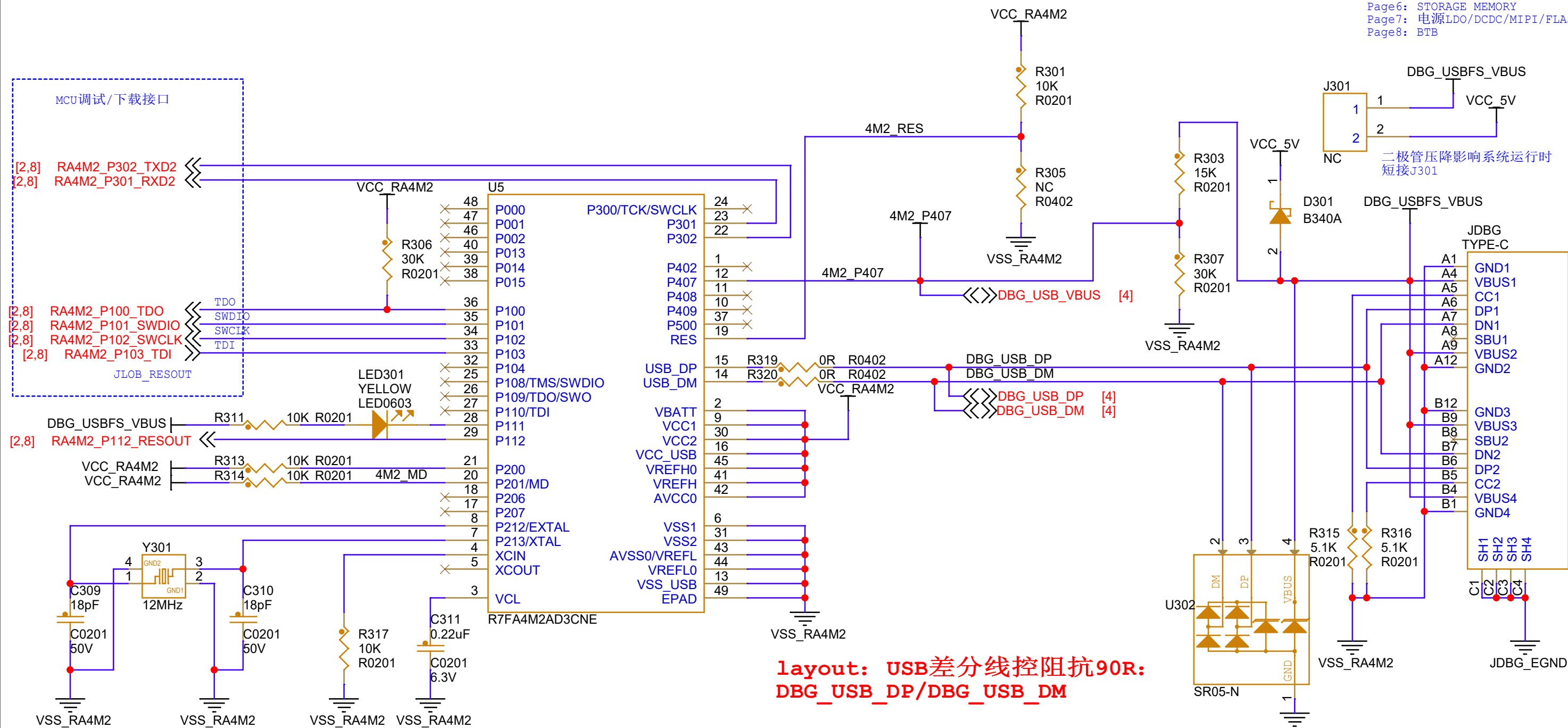


晶振

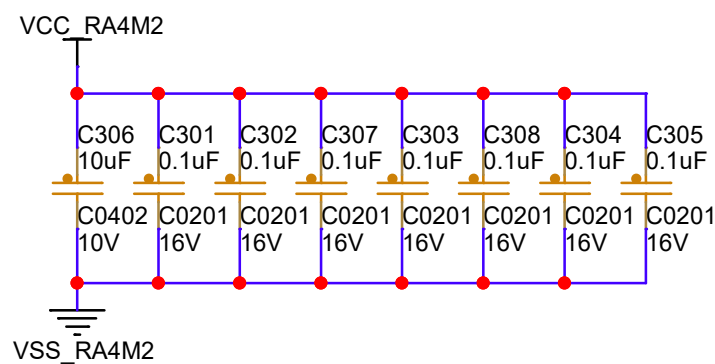


Jlink OB

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Page6: STORAGE MEMORY
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Page8: BTB



注意：R7FA4M2作为JlinkOB使用时，只能使用12MHz晶振



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如果使用USB HS，主晶振只能选12/20/24/48MHz



**layout: USB差分线控阻抗90R:
USB DP/USB DM**

[3] DBG_USB_VBUS <<>> R149 NC R0402 <<>> P407 [1,4,8]

[3] DBG_USB_DP <<>> R147 NC R0402 R145 NC R0402 <<>> P814 USB_DP [1,4,8]

[3] DBG_USB_DM <<>> R148 NC R0402 R146 NC R0402 <<>> P815_USB_DM [1,4,8]

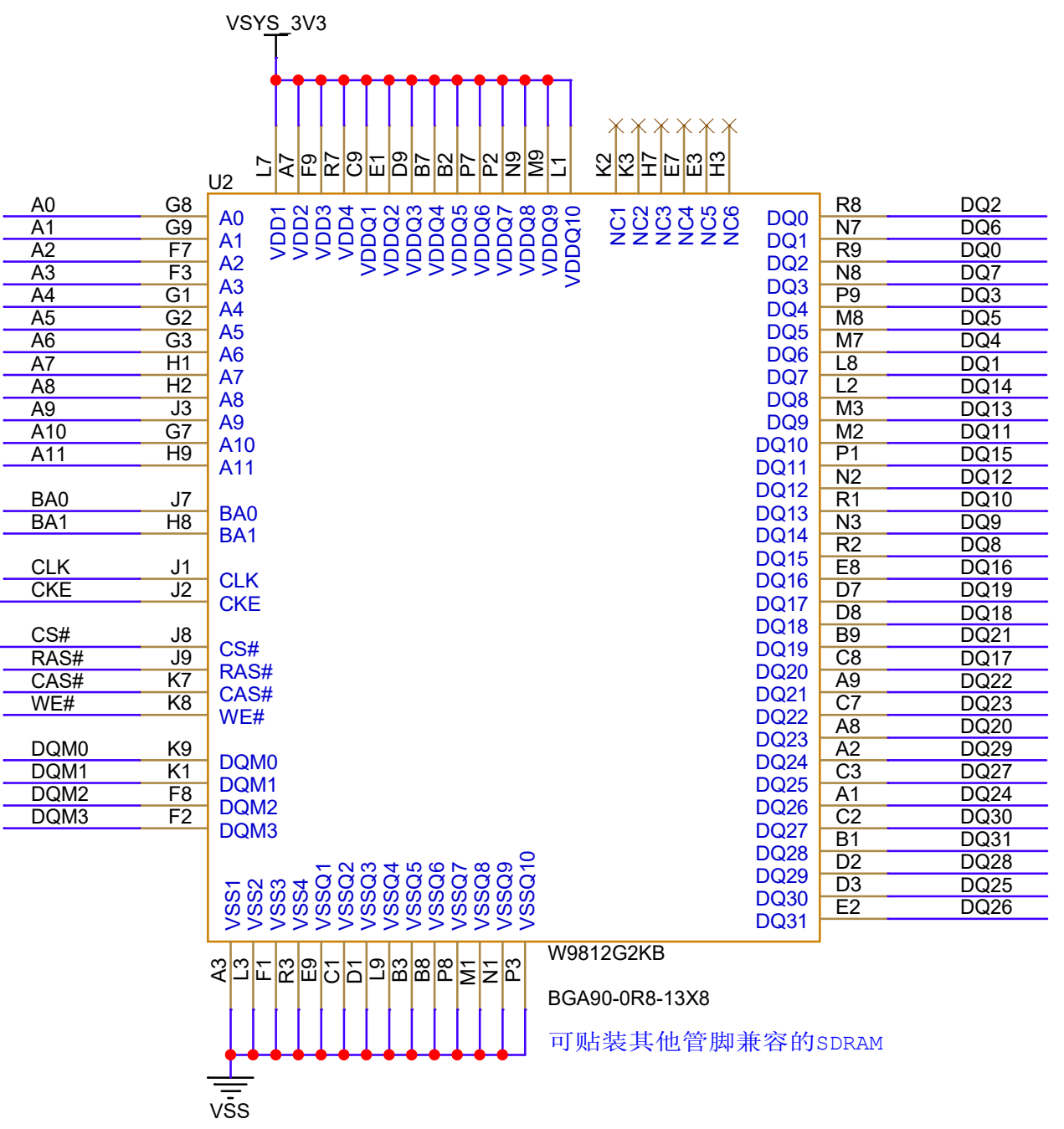
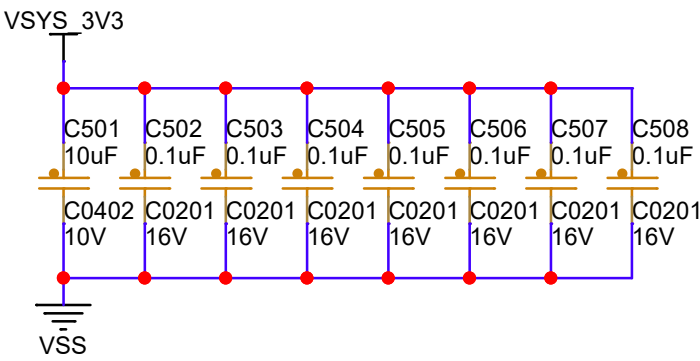
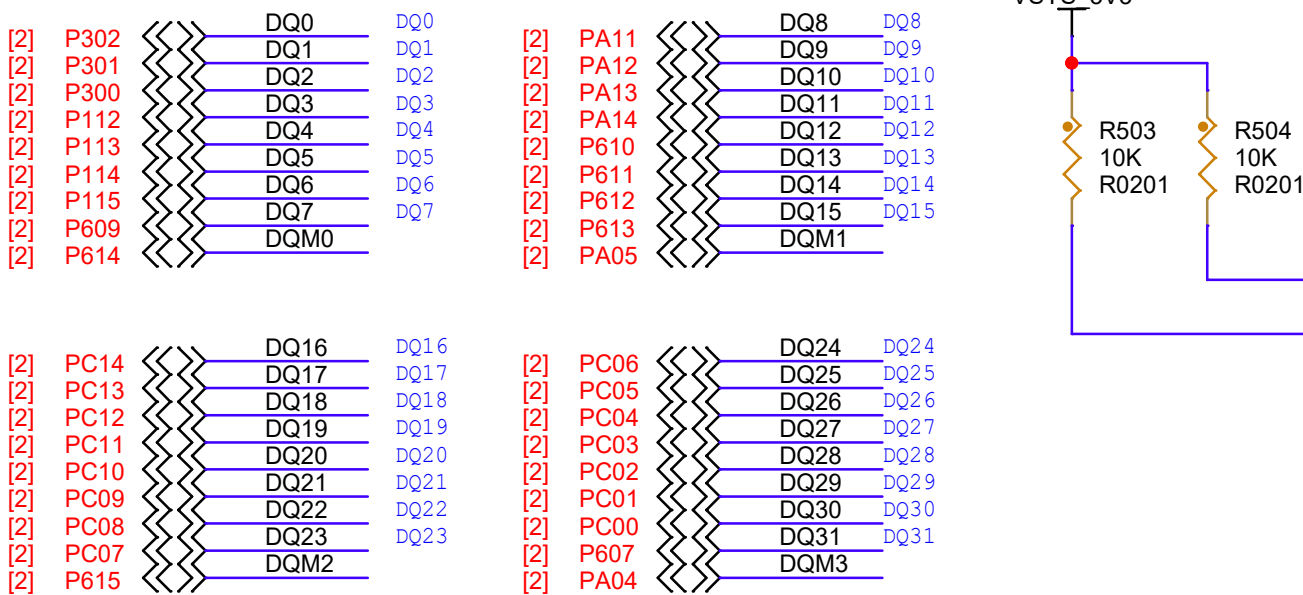
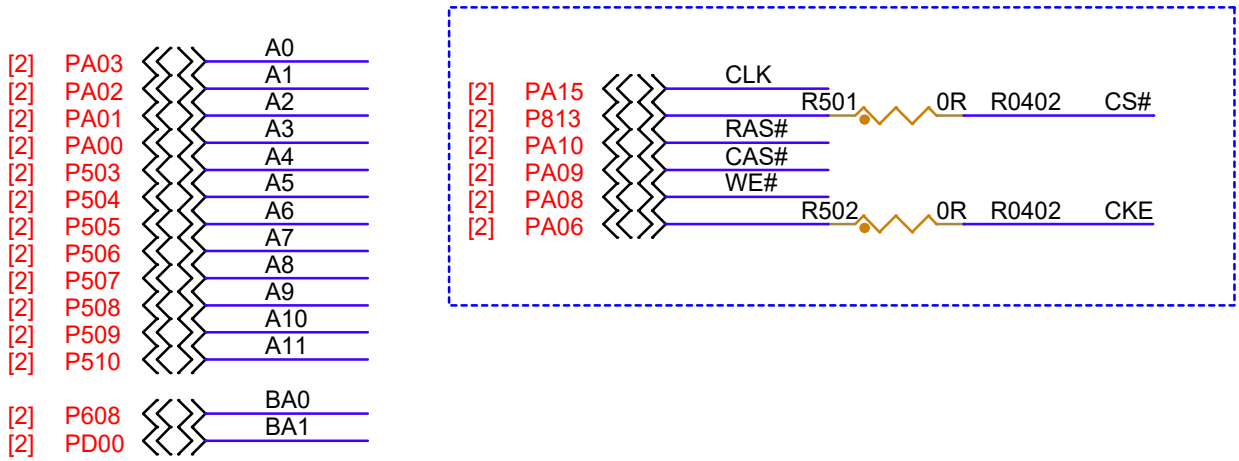
R323 R324靠近J1摆放

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SDRAM

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Page4: USB HS
Page5: SDRAM
Page6: STORAGE MEMORY
Page7: 电源LDO/DCDC/MIPI/FLASH
Page8: BTB

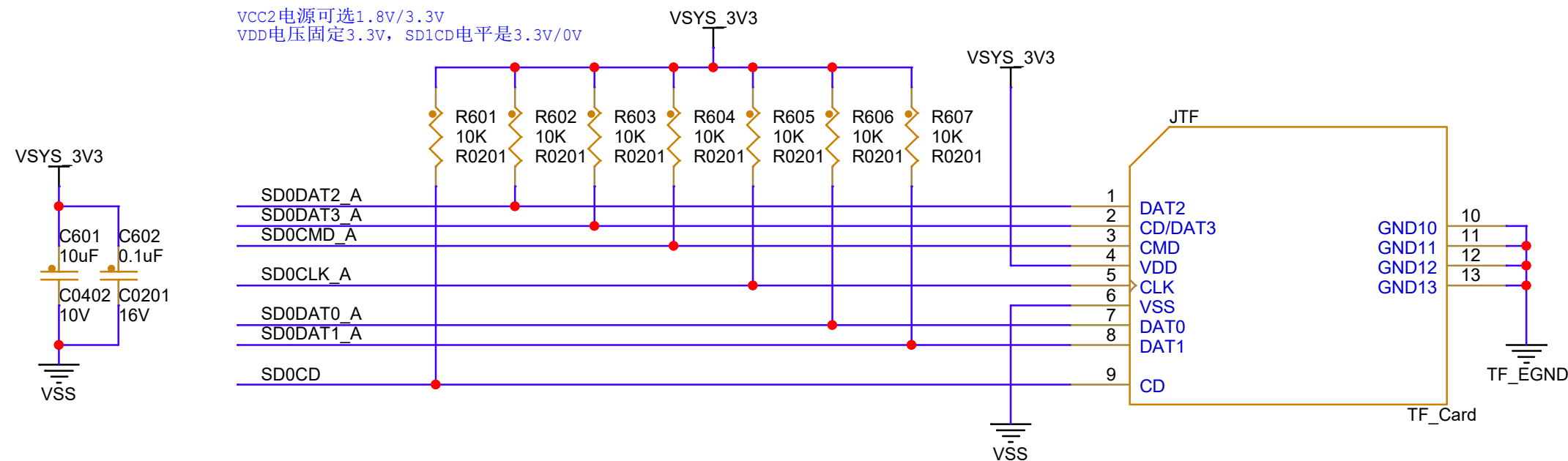
layout: SDRAM走线控阻抗50R:



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Size A4	Document Number SDRAM	Rev V1.1
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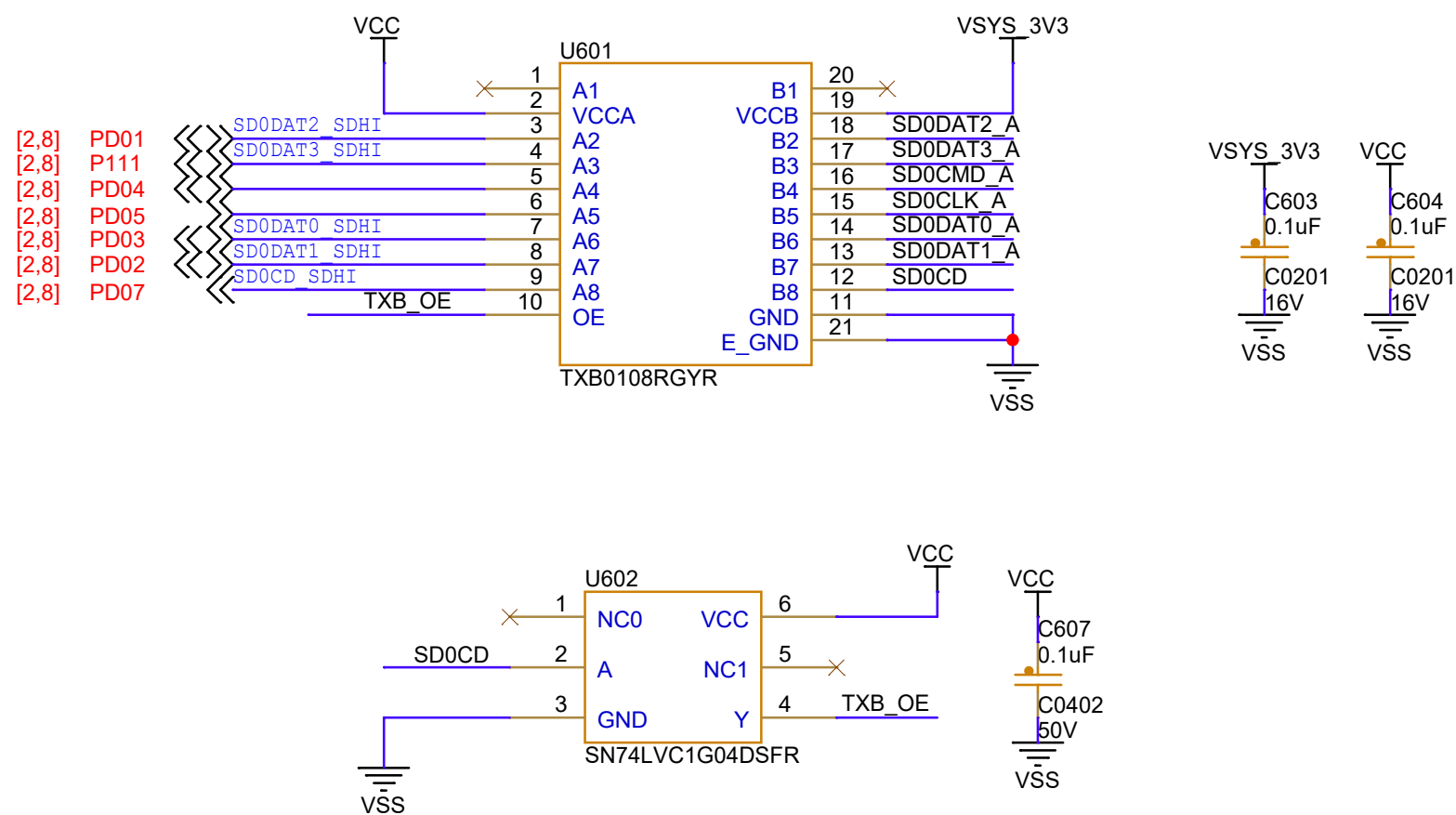
SD卡

VCC2电源可选1.8V/3.3V
VDD电压固定3.3V，SD1CD电平是3.3V/0V

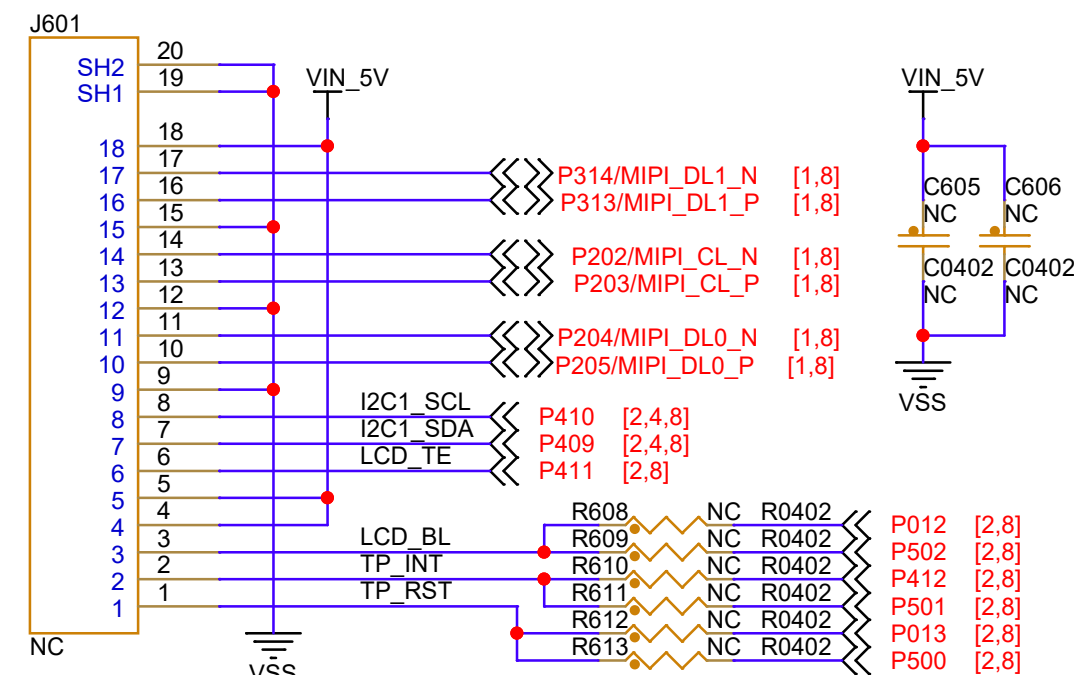


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SD卡电平转换



MIPI接口



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Title

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A4

Document Number

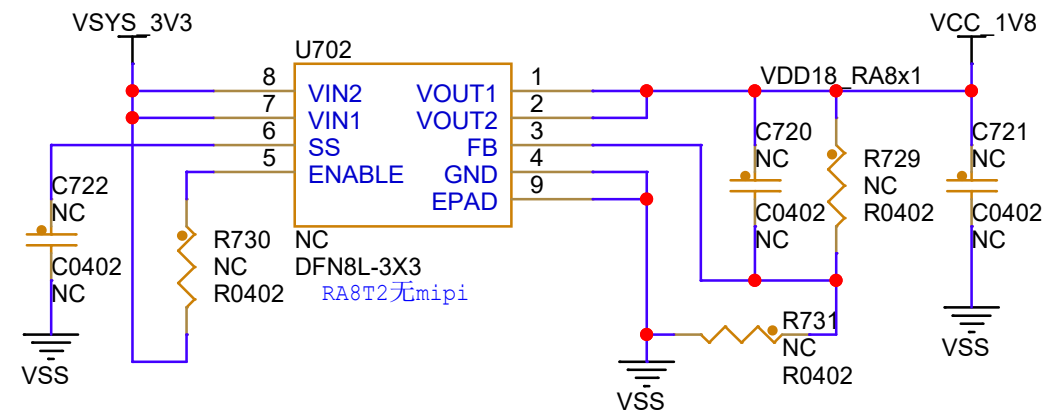
STORAGE MEMORY

Rev
V1.1

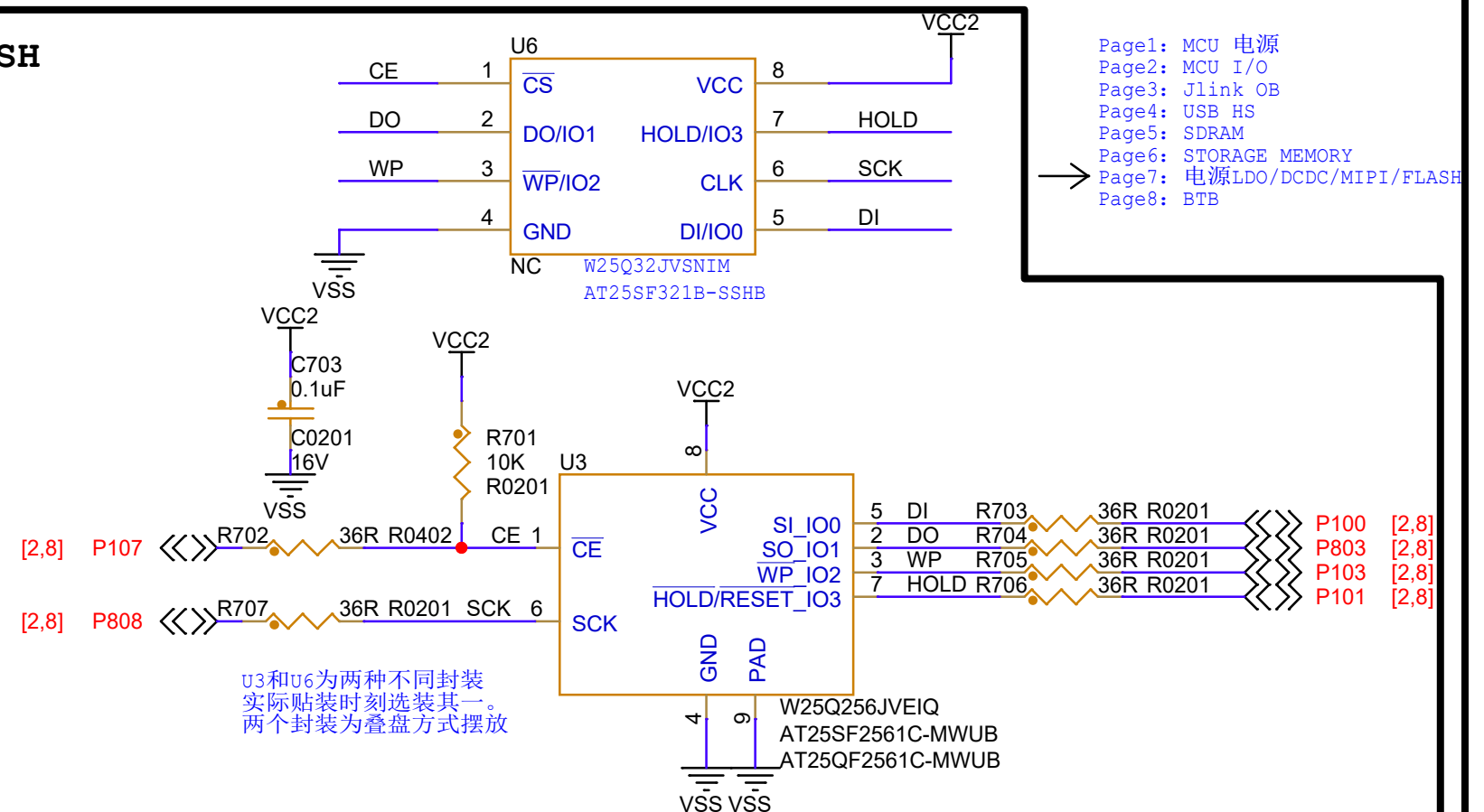
Date: Wednesday, January 07, 2026

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1.8v电源

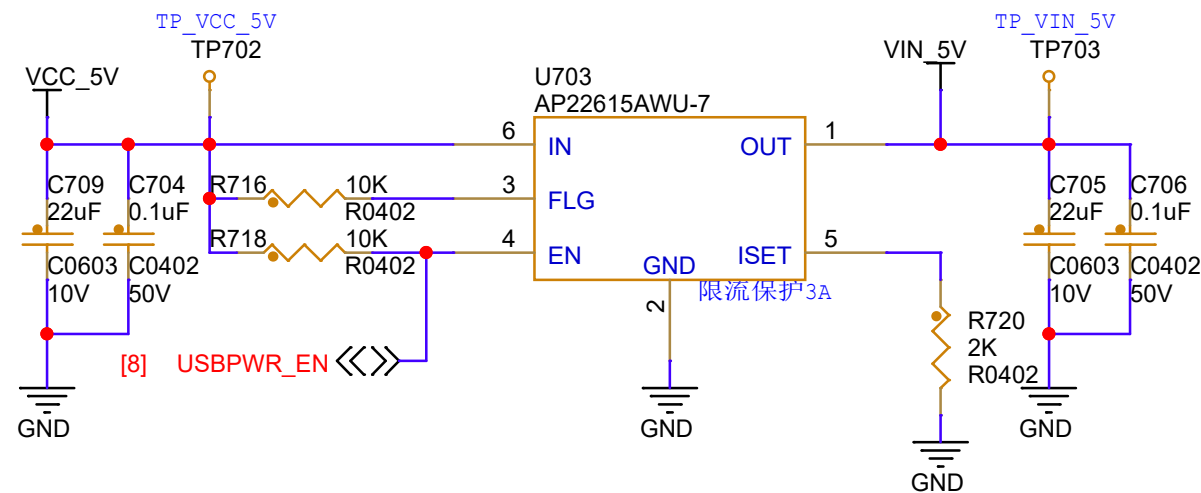


FLASH

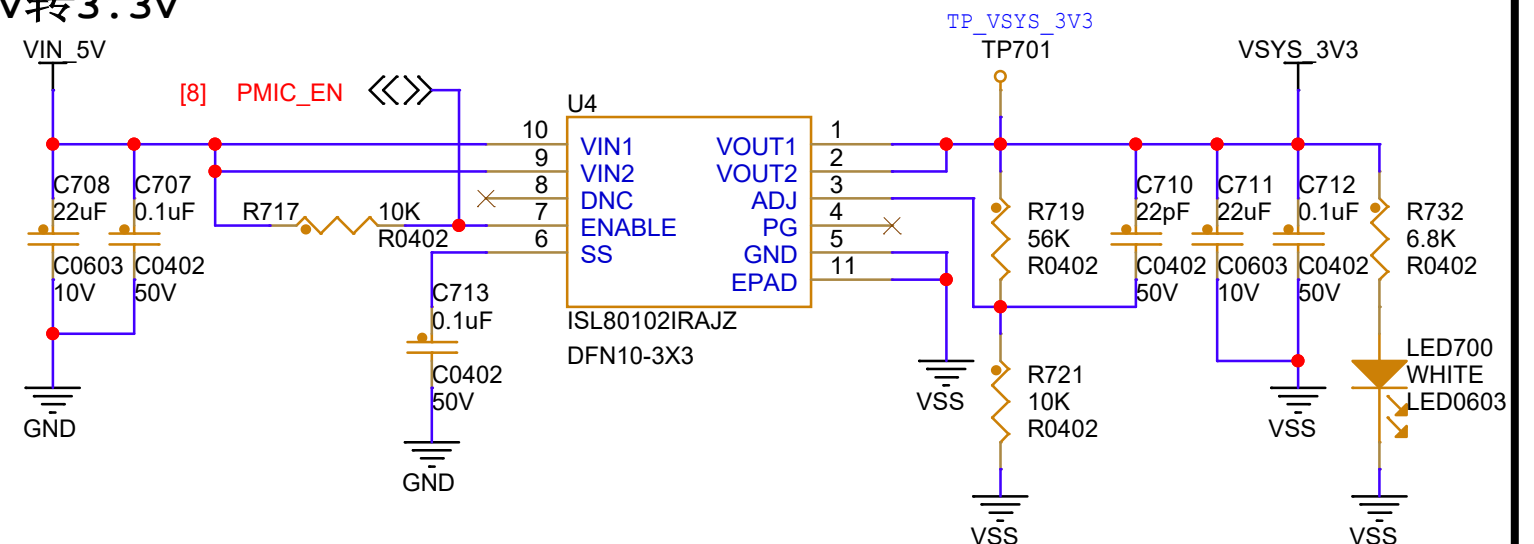


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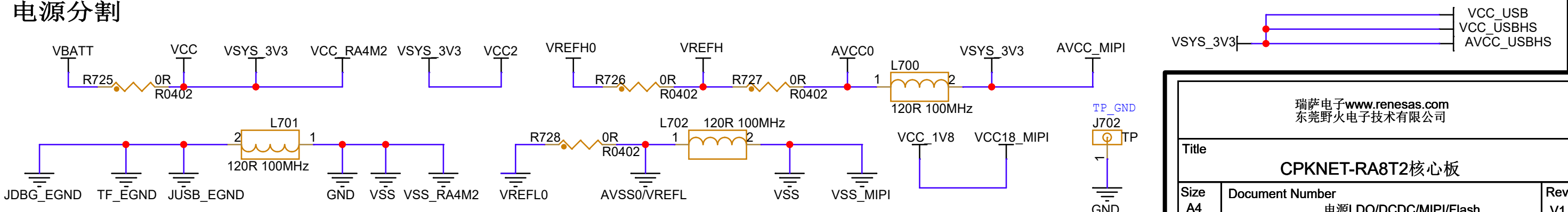
电源保护



5v转3.3v

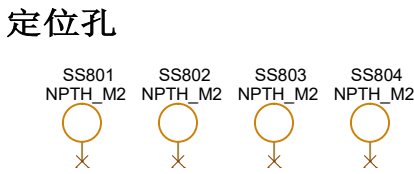
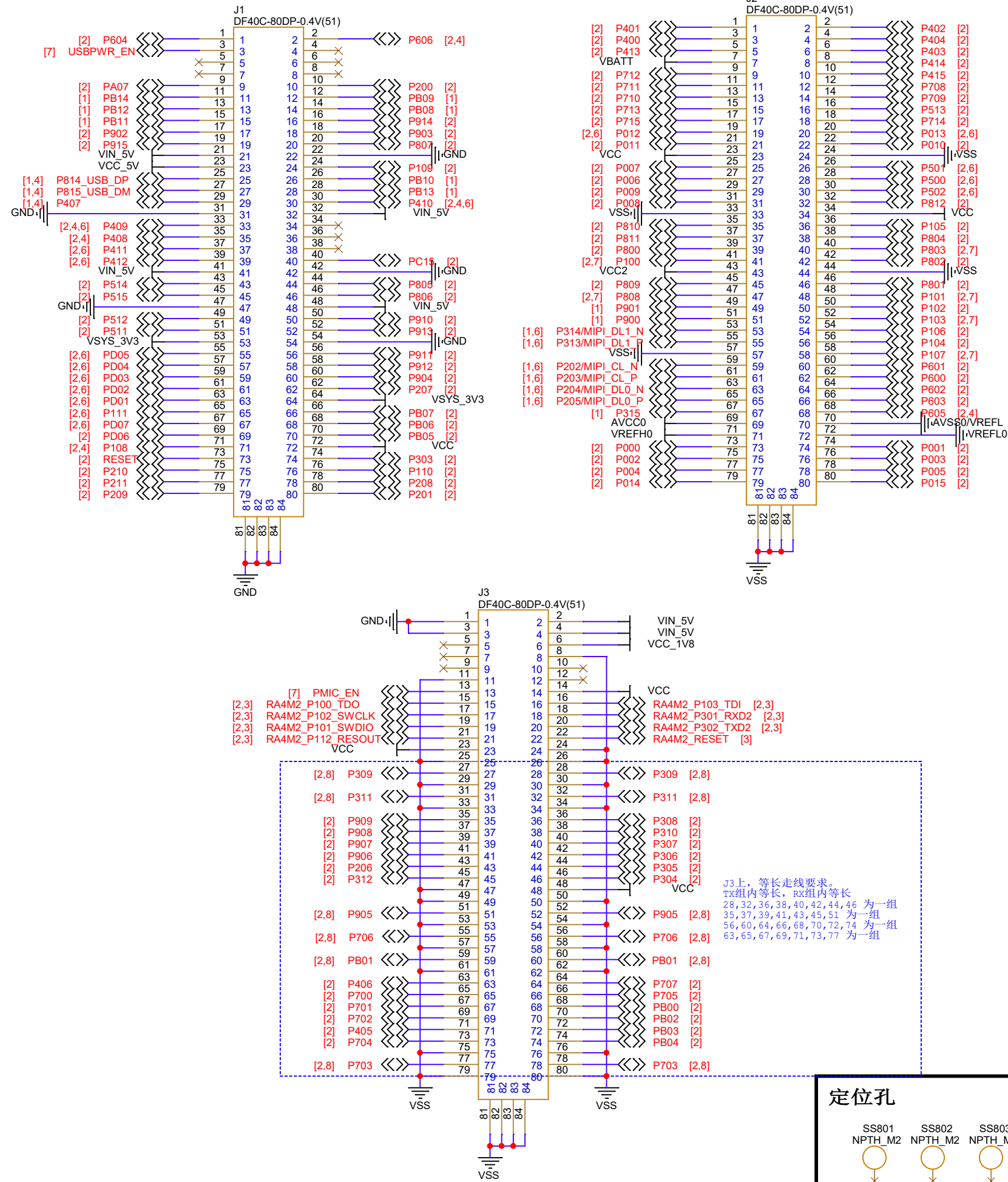


电源分割



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Title		
CPKNET-RA8T2核心板		
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A4	电源LDO/DCDC/MIPI/Flash	V1.1
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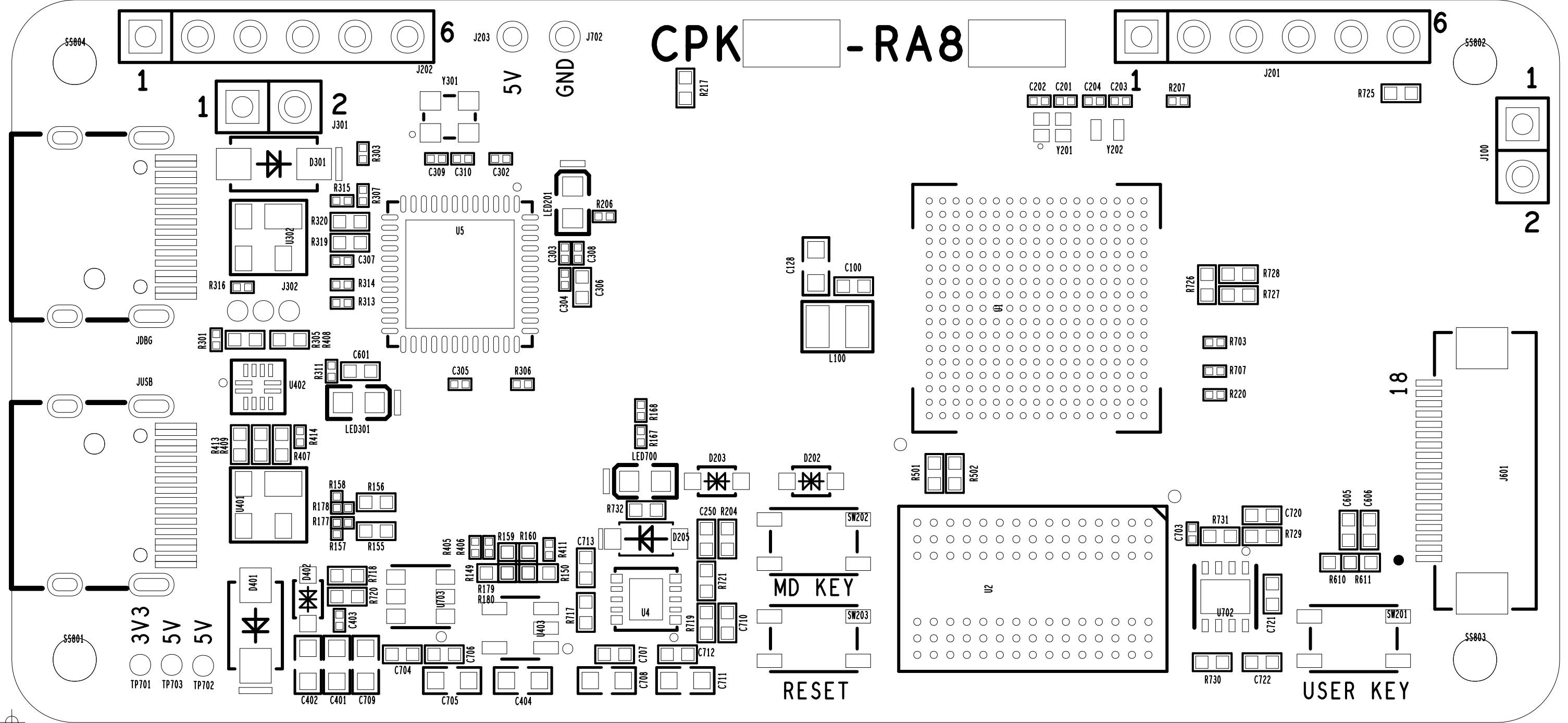
历史版本

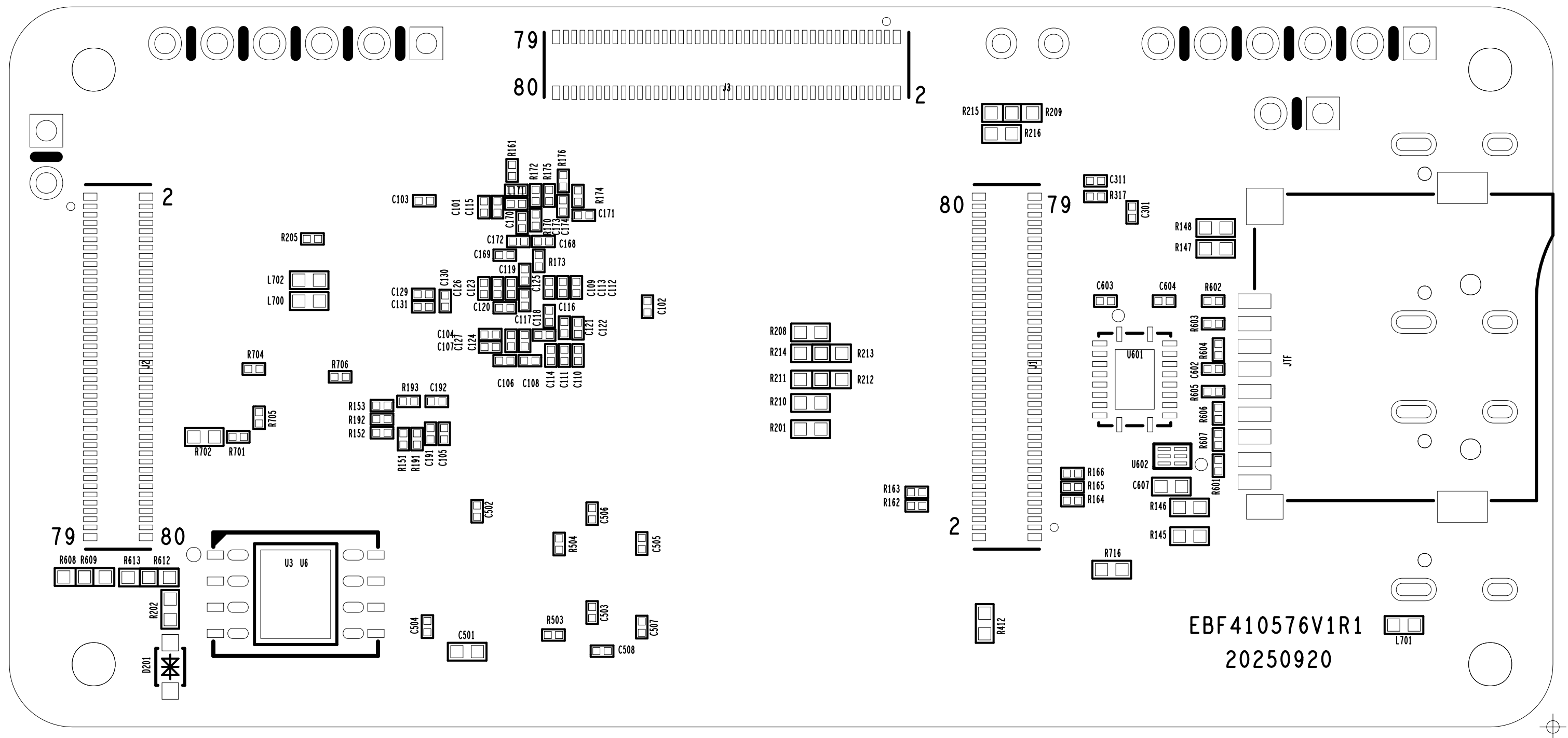
版本号	日期	设计	描述
V1.0	2025-08-28	LPC	初始版本
V1.1	2025-09-17	LPC	修正VCC_USB连接

CPKNET-RA8T2 核心板 原理图

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电源接入点

CPKNET-RA8T2 Power Supply

