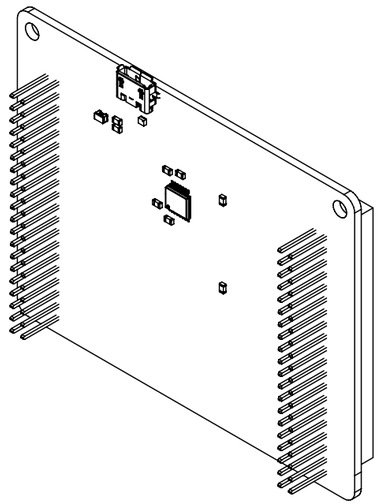
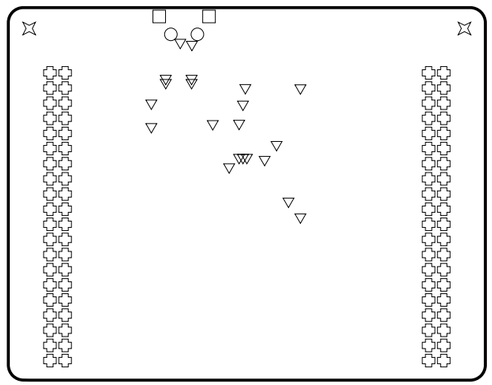
View from Top side (Scale 1:1)



Drill Drawing View (Scale 1:1)



Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
▽	21	0.203mm	Plated	
○	2	0.850mm	Plated	
⌖	80	1.016mm	Plated	
□	2	1.300mm	Plated	
⛝	2	3.175mm	Non-Plated	
	107 Total			

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FABRICATION NOTES

Design Features

Number of Layers: 2
Smallest Via Drill/Pad: See drill table
Impedance Control: NO
Gold Fingers: NO
Silkscreen Color (Top & Bottom): WHITE
Silkscreen to be "Silkscreen Printed"
Soldermask Color (Top & Bottom):
Black soldermask

CMYK 00/00/00/00
RGB 00 00 00
RGB #000000 HEX

Matte Finish
Components that are DNF are not fitted and to be free of solder.

Materials and Ratings

Core Material: FR4 Tg (C min): 170 Td (C min): 330
PAD Finish: ENIG
Finished Board Thickness: See Chart
Finished outer layer Cu min thickness: See Chart
Copper thickness - inner layers: See Chart
ROHS Required: YES
UL94V Rating: UL94V-0
IPC-A-6011/IPC-A-6012 Class: 2 Inspect per IPC-A-600

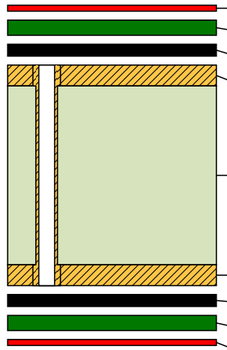
Process and Panelization

Inner Thieving/Balancing OK? YES Keepaway: 2.5mm
Outer Thieving/Balancing OK? NO Keepaway:
Electrical 100% Test Requested: YES
Panelization Requested: YES
Panelization Method: TAB-ROUTE w/Rails

Board Manufacturing Markings

DO NOT ADD ANY ADDITIONAL
No Board Lot
No QC Stamp
No UL94V-0
No ROHS
To be manufactured in a UL Approved Process, using UL Approved Materials, BUT NOT marked with UL LOGOS, Date Codes or PCB Supplier Markings (no additional markings)

Layer Stack Legend



Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.03mm	SM-002	Solder Mask	GTS
PbSn	Top Surface Finish	0.02mm		Surface Finish	
CF-004	**Top Layer**	**0.04mm**		**Signal**	**GTL**
Core		*1.50mm*	*Core-043*	*Dielectric*	
CF-004	**Bottom Layer**	**0.04mm**		**Signal**	**GBL**
PbSn	Bottom Surface Finish	0.02mm		Surface Finish	
Surface Material	Bottom Solder	0.03mm	SM-002	Solder Mask	GBS
	Bottom Overlay			Legend	GBO

Total thickness: 1.66mm

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Transmission Line Structure Table

Impedance Id	Transmission Line	Target Impedance	Calculated Impedance	Trace layer	Wide Trace Width	Narrow Trace Width	Reference layers	Target Tolerance
1	Edge-Coupled Coated Microstrip	90	91.43	Top Layer	0.229mm	0.229mm	Bottom Layer	10%
2	Edge-Coupled Coated Microstrip	90	91.43	Bottom Layer	0.229mm	0.229mm	Top Layer	10%

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