RZ/A3

Initial Program Loader Application Note (Serial Flash Boot Edition)

Introduction

This application note describes the following contents about the reference implementation of Initial Program Loader (called IPL), which is a boot loader for booting user programs from Serial Flash memory connected to RZ/A3 device.

- Description of IPL function
- Description of how to build the development environment
- Description of how to debug
- How to customize when supporting Serial Flash memory that is not supported by default IPL

Target Device

RZ/A3UL

When using this application note with other Renesas Microprocessors, sufficient evaluation is recommended after making modifications to comply with the alternate Microprocessor.

Contents

1. Overview 5
1.1 Glossary 5
1.2 IPL processing overview 6
2. Operating Confirmation Conditions 7
3. Reference Application Notes 8
4. Hardware 8
4.1 Peripheral Functions used 8
4.2 Pins Used List 8
5. Software 9
5.1 Operation overview 9
5.1.1 Operation image of boot process 9
5.1.2 Boot process to launch FSP application on DDR SDRAM 11
5.1.3 Boot process to launch FSP application on Serial Flash memory 13
5.2 Peripheral Function Setting 15
5.2.1 Settings of SPIBSC Register 17
5.3 Memory Map 19
5.4 MMU setting 20
5.5 Interrupt used list 21
5.6 Exception level 21
5.7 Application Header 21
5.8 Data Types 22
5.9 Constants 23
5.10 Structures/Unions 26
5.11 Variables 34
5.12 Function 58
5.12.1 Function List 58
5.12.2 Function Specifications 61
5.12.2.1 IPL control functions 61
5.12.2.2 SPIM controller driver functions 62
5.12.2.3 Serial Flash Memory driver functions 66
5.12.2.4 module control functions 70
5.13 Flow Chart 77
5.13.1 IPL (overall) flow 77
5.13.2 FSP Application Image copy process 80
5.13.3 Setting of Serial Flash memory and SPIBSC 82
6. IPL development environment construction procedure 85
6.1 Procedure for building a development environment for Widows10 PC 85

6.1.1 Installation of IDE (e² studio) for Windows10 85
6.1.1.1 e² studio installation (Windows10) 86
6.1.1.2 Installation of RZ/A FSP packs (Windows10) 94
6.1.2 MSYS2 Installation 95
6.2 Procedure for building a development environment for Ubuntu 22.04 LTS 98
6.2.1 Installation of IDE (e² studio) for Ubuntu 22.04 LTS 98
6.2.1.1 e² studio installation (Ubuntu 22.04 LTS) 98
6.2.1.2 Installation of RZ/A FSP packs (ubuntu 22.04 LTS) 109
6.2.2 Additional Software Installation 110

7. IPL build environment construction procedure 111

8. Execution Environment of IPL 121
8.1 Create Debug Configuration 121
8.2 Connection to SMARC EVK Board 130
8.3 Setting Serial Terminal 132
8.4 Execution procedure of IPL by Serial Flash boot 136

9. Application Example 140
9.1 Execution procedure of IPL by On-chip RAM download 140
9.2 Procedure for writing an FSP application to Serial Flash memory 144
9.3 How to change IPL build environment for custom board 149
9.3.1 How to customize IPL for your Serial Flash memory 149
9.3.1.1 flash_open 158
9.3.1.2 flash_close 161
9.3.1.3 flash_exec_op 162
9.3.1.4 flash_enter_xip 163
9.3.1.5 flash_exit_xip 166
9.3.1.6 flash_read 167
9.3.1.7 flash_write 168
9.3.1.8 flash_erase 173
9.3.1.9 flash_get_write_status 177
9.3.1.10 flash_write_enable 179
9.3.1.11 flash_read_status_reister1 / flash_read_status_register2 181
9.3.1.12 flash_write_status_register2 184
9.3.1.13 flash_set_qe 186
9.3.1.14 flash_erase_4k / flash_erase_32k / flash_erase_64k 189
9.3.2 How to add a board setting 192
9.3.3 How to add a Module for Clock Supply 195
9.3.4 How to add pin setting 197
9.3.5 How to change MMU setting 198

10. Precautions 199

10.1 About DDR SDRAM access prohibited area 199

11. Reference Documents 200

12. Trademarks 201

Revision History 202

1. Overview

IPL is a boot program for RZ/A3 device.

When starting the RZ/A3 device, IPL initializes the peripheral I/O modules, the memory installed on the board, etc., and launches the FSP application.

IPL consists of functions such as peripheral I/O module driver, memory control driver, and FSP application image load module.

1.1 Glossary

Table 1.1 shows the terms related to the operation of IPL explained in this application note.

Table 1.1 The term for IPL operation (1/2)

Term	Description
Initial Program Loader (IPL)	A loader program that launches an FSP Application for the RZ/A3 environment. It is called from the BootROM program to initialize the memory and the peripheral I/O modules installed in boards, then copies the FSP application and jumps to the copy destination according to the application header. IPL is developed based on Arm Trusted Firmware and it is equivalent to BL2 of Arm Trusted Firmware. When changing the Serial Flash memory to be used, the user is requested to create and add the initialization code according to the specifications of the Serial Flash memory to be used, referring to this application note. By default, optimal settings are made for using the Renesas Electronics Serial Flash memory(AT25QL128A).
BootROM Program	The BootROM program is the program that executes first after the device starts, and it copies the next boot program from the memory associated with the boot mode to the On-chip RAM and jumps to the next boot program. IPL is premised on operation in Boot Mode 3 (1.8-V Serial Flash Memory), and the IPL written to the Serial Flash memory is copied to the specified address (H'0001_2000) of the On-chip RAM and the boot process is executed. This program is stored in the RZ/A3's internal ROM, so it does not need to be created by the user.
FSP Application	This is a program consisting of BSP and sample programs to use the functions implemented on the board.
Application Header	A header placed at the beginning of the FSP application, used by the IPL to refer to the destination address or entry point address of the FSP application. Before executing IPL, the FSP application image including the application header must be written to the specified address of the Serial Flash memory. The write destination address of the Application Header can be changed in the IPL build option, and the default is H'2002_0000.
Serial Flash memory driver	The Serial Flash memory driver creates parameters for executing operations that comply with the specifications of the Serial Flash memory and manages the execution order of operations. This driver is implemented with specifications that depend on the Serial Flash memory. If you use a Serial Flash memory other than the one supported by the default IPL, you need to change driver according to the specifications.

Table 1.2 The term for IPL operation (2/2)

Term	Description
Manual Mode	This is the operation mode of the SPI Multi I/O Bus Controller. In this mode, data is read / written by sending Read and Write commands to the Serial Flash memory via serial communication. The default operating mode of the SPI Multi I/O Bus Controller is Manual Mode.
External Address Space Read Mode	This is the operation mode of the SPI Multi I/O Bus Controller. In this mode, the device can read data by performing read access to the address space where the Serial Flash memory is mapped. This mode is enabled by switching the operation mode from Manual Mode.

1.2 IPL processing overview

The outline of IPL processing is described below.

1. Release the reset and supply the clock to the module used for the boot process.
2. Initialize the serial communication interface for debug message output and control the message input/output.
3. Change the settings of SPI Multi I/O Bus Controller.
4. Initialize DDR SDRAM.
5. Copy the FSP Application image from Serial Flash memory to DDR SDRAM.
6. Jump to the entry point of FSP Application on DDR SDRAM.

2. Operating Confirmation Conditions

IPL has been confirmed to run in the following conditions.

Table 2.1 Operating Confirmation Conditions

Item	Contents
MPU	RZ/A3UL
Operating Frequency	CPU clock (Iϕ): 1.0GHz SRAM MCPU clock (I2ϕ): 200MHz Peripheral clock 0 (P0ϕ): 100MHz Peripheral clock 1 / SRAM ACPU clock (P1Φϕ): 200MHz SPI multi I/O main clock (SPI0ϕ): 133.2MHz QSPI0_SPCLK (SPI1ϕ): 66.6MHz
Operating Voltage	Power supply voltage (I/O): 3.3V Power supply voltage (1.8/3.3V switching I/O (SPI_PVDD)):1.8V
Host PC	Windows10 (64bit) installed PC or Ubuntu 22.04 LTS Desktop (64bit) installed PC
Debugger	J-Link Base J-Link Lite (*J-Link Software version: V8.10a)
IDE	e² studio 2025-01
Toolchain	Windows10 PC: gcc-arm-10.3-2021.07-mingw-w64-i686-aarch64-none-elf Ubuntu 22.04 LTS PC: gcc-arm-10.3-2021.07-x86_64-aarch64-none-elf
	Compiler option (Excludes the addition of directory paths Release configuration: -march=armv8-a -mgeneral-regs-only -mstrict-align -ffunction-sections -fdata-sections -ffreestanding -fno-builtin -fno-common -Os -std=gnu99 -fno-stack-protector -Werror -Wall -Wmissing-include-dirs -Wunused -Wdisabled-optimization -Wvla -Wshadow -Wno-unused-parameter -Wredundant-decls -Wunused-but-set-variable -Wmaybe-uninitialized -Wpacked-bitfield-compat -Wshift-overflow=2 -Wlogical-op -Wno-error=deprecated-declarations -Wno-error=cpp Debug configuration: -march=armv8-a -mgeneral-regs-only -mstrict-align -ffunction-sections -fdata-sections -ffreestanding -fno-builtin -fno-common -Os -std=gnu99 -fno-omit-frame-pointer -fno-stack-protector -Werror -Wall -Wmissing-include-dirs -Wunused -Wdisabled-optimization -Wvla -Wshadow -Wno-unused-parameter -Wredundant-decls -Wunused-but-set-variable -Wmaybe-uninitialized -Wpacked-bitfield-compat -Wshift-overflow=2 -Wlogical-op -Wno-error=deprecated-declarations -Wno-error=cpp
Operating Mode	Boot Mode3 (1.8-V Serial Flash Memory)
Board	RZ/A3UL-Evaluation-Board-Kit (QSPI version) (In this document, it is called SMARC EVK board)
Device to use (Function used on the board)	• Serial Flash memory (Store the image of the program) Manufacture's name: Renesas Electronics Model Name: AT25QL128A • DDR4 SDRAM (Used as an execution area for FSP Application) Manufacture's name: Micron Technology Model Name: MT40A512M16LY-062E

3. Reference Application Notes

For additional information associated with this document, refer to the following application notes.

- RZ/A3 Initial Program Loader Application Note (Octa Flash Boot Edition) (R01AN6433EJ)

4. Hardware

This chapter describes the hardware used by IPL.

4.1 Peripheral Functions used

IPL uses the peripheral features shown in Table 4.1.

Table 4.1 Peripheral functions and uses

Peripheral Function	Use
SPI Multi-I/O Bus Controller (SPIBSC)	Set to External Address Space Read Mode and generate a signal for the CPU to read directly from the Serial Flash memory connected to the SPI multi-I/O bus space. IPL uses a driver called "SPIM controller driver" to control SPIBSC
DDR3L/DDR4 SDRAM Memory Controller (MEMC)	Make settings to access DDR3L/DDR4 SDRAM connected to the external bus space.
Clock pulse generator (CPG)	Generate the operating frequency of the RZ/A3. Release the module standby mode of the RZ/A3's peripheral I/O modules.
General Purpose Input Output Port (GPIO)	Switch multiplexed pin functions for SCIFA channel 0 and set the QSPI dedicated pins.
Serial communication interface with FIFO (SCIFA)	Used for message output to the host PC using SCIFA channel 0.
System Counter (SYC)	Generate the count value used by the generic timer built into the Cortex®-A55 core.
Memory Management Unit (MMU)	Generate a translation table that specifies the cache effective area and memory type for the RZ/A address space.

4.2 Pins Used List

Table 4.2 lists the pins used and their functions.

Table 4.2 Pins used and their functions

Pin name	I/O	Function
QSPI0_SPCLK	Output	Clock signal for a Serial Flash memory
QSPI0_IO0	Input/Output	Serial Flash memory data0
QSPI0_IO1	Input/Output	Serial Flash memory data1
QSPI0_IO2	Input/Output	Serial Flash memory data2
QSPI0_IO3	Input/Output	Serial Flash memory data3
QSPI0_SSL	Output	Chip select signal for a Serial Flash memory
QSPI_RESET#	Output	Serial Flash memory reset
QSPI_WP#	Output	Serial Flash memory write protect
SCIF0_RXD	Input	Serial communication receive data signal
SCIF0_TXD	Output	Serial communication transmit data signal

5. Software

This chapter describes the IPL software configuration and functions.

5.1 Operation overview

When the SMARC EVK board is booted in Boot Mode 3 (1.8-V Serial Flash Memory), the Boot ROM program written in the internal ROM will start.

The IPL is copied from the Serial Flash memory located in the SPI multi I/O bus space to the On-chip RAM by the BootROM program and booted.

IPL gets the copy destination address and entry point address of the FSP application image from the application header placed at the beginning of the FSP application.

This chapter describes the case in RZ/A3UL as an example of the boot process.

After that, copy the FSP application to the obtained address and jump to the entry point address.
Please refer to 5.7 Application Header for application header configuration.

5.1.1 Operation image of boot process

Figure 5.1 shows an operation image of the basic boot process.

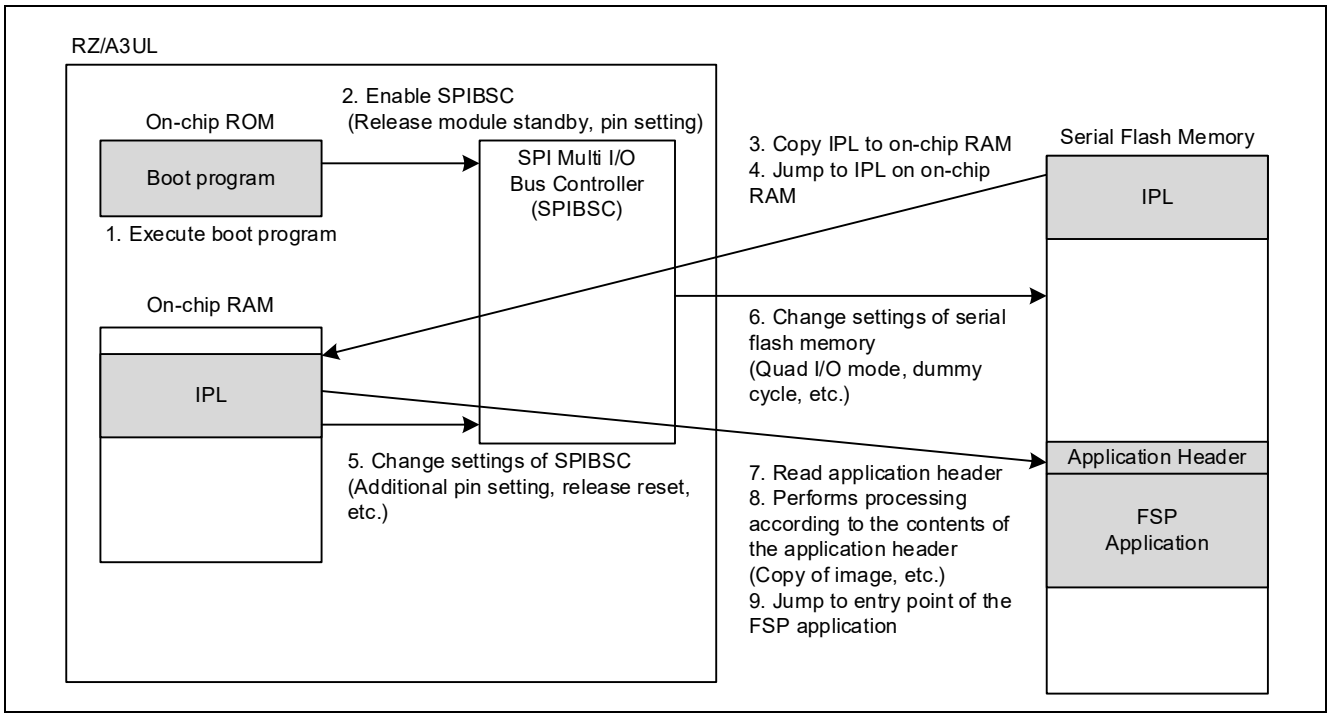


Figure 5.1 Operation image of boot process

Describes the IPL boot process.

1. RZ/A3UL executes the BootROM program after releasing the power-on reset.
2. When the RZ/A3UL operating mode is Boot mode 3, the BootROM program will enable SPIBSC and initialize it.
   The initial setting is that it can access independently of the model of the Serial Flash memory.
3. The BootROM program reads the IPL stored in the start address (*1) of the Serial Flash memory and copies the IPL to the entry point address (*2) on the On-chip RAM.
   Then SPIBSC is reset by the BootROM, and access to the Serial Flash memory will be prohibited.
4. The BootROM program jumps to the IPL entry point (* 2) on the On-chip RAM.
5. IPL makes additional pin settings and resets for SPIBSC for 4-byte access to the Serial Flash memory and changes the settings to the optimum settings for the Serial Flash memory (AT25QL128A) mounted on the SMARC EVK board.
6. A command is issued via the SPIBSC to the Serial Flash memory to change the settings.
7. IPL reads the application header.
8. If the application header specifies a copy destination address for the FSP application, IPL copies it.
   As an example of the process is shown in the following chapter.
9. The IPL follows the contents of the application header and jumps to the entry point of the FSP application.

   (*1) This address will be H'2000_0000 when the external address space read mode is set.
   (*2) The IPL entry point address is H'0001_2000.

5.1.2 Boot process to launch FSP application on DDR SDRAM

Figure 5.2 shows an operation image when an FSP application written to Serial Flash memory is loaded into DDR SDRAM and executed.

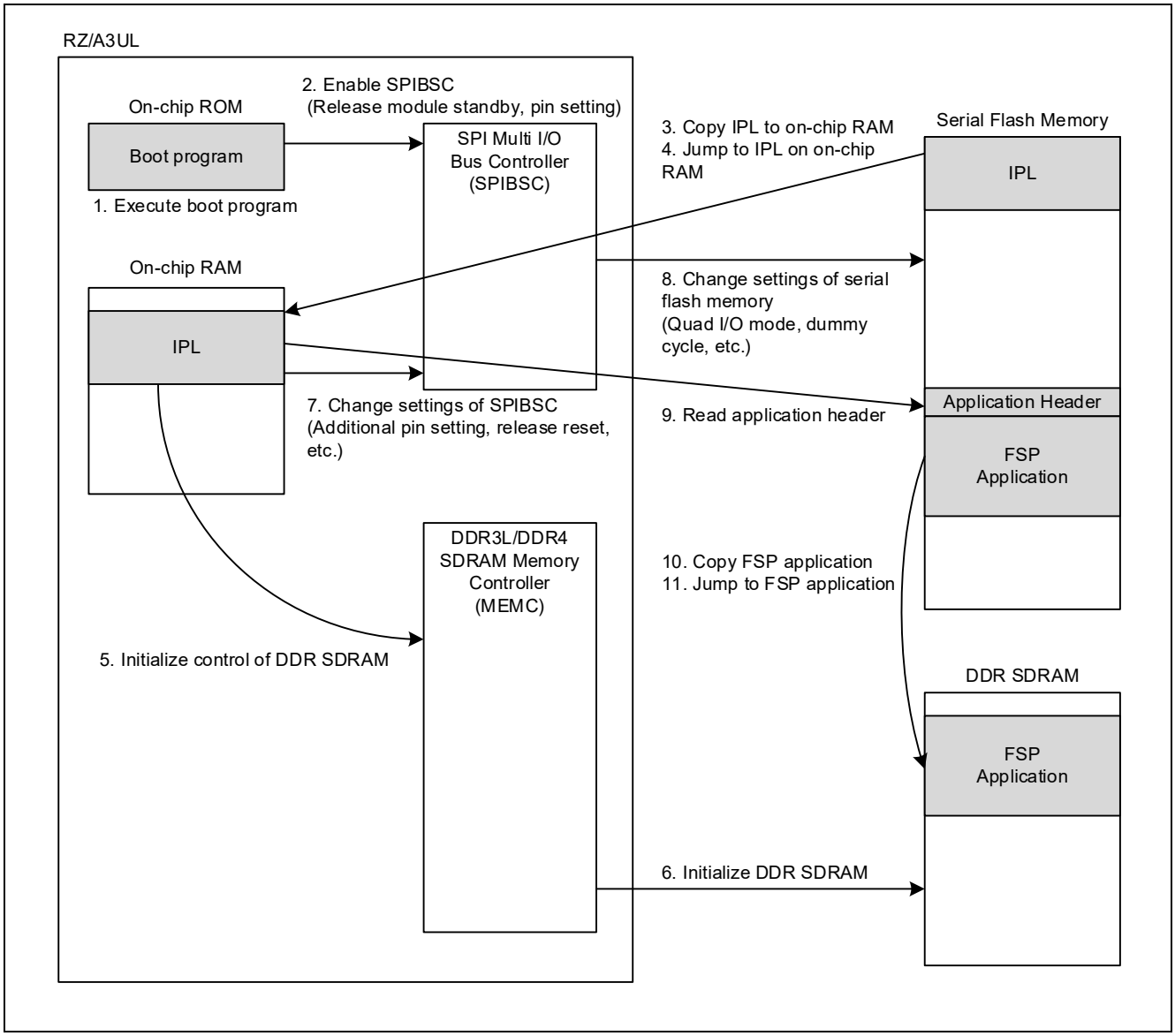


Figure 5.2 Operation image when launching an FSP application on DDR SDRAM

Describes the IPL boot process.

1. RZ/A3UL executes the BootROM program after releasing the power-on reset.
2. When the RZ/A3UL operating mode is Boot mode 3, the BootROM program will enable SPIBSC and initialize it.
   The initial setting is that it can access independently of the model of the Serial Flash memory.
3. The BootROM program reads the IPL stored in the start address of the Serial Flash memory and copies the IPL to the entry point address on the On-chip RAM.
   Then the SPIBSC is reset by BootROM, and access to the Serial Flash memory will be prohibited.
4. The BootROM program jumps to the IPL entry point on the On-chip RAM.
5. IPL initializes MEMC and controls the initial setting of DDR SDRAM.
6. Initialize the DDR SDRAM by controlling the initial setting of MEMC.
7. IPL makes additional pin settings and resets SPIBSC for 4-byte access to the Serial Flash memory and changes the settings to the optimum settings for the Serial Flash memory (AT25QL128A) mounted on the SMARC EVK board.
8. A command is issued via the SPIBSC to Serial Flash memory to change the settings memory.
9. IPL reads the application header.
10. IPL will copy the FSP application to DDR SDRAM according to the contents of the application header.
11. The IPL follows the contents of the application header and jumps to the entry point of the FSP application on DDR SDRAM.

5.1.3 Boot process to launch FSP application on Serial Flash memory

Figure 5.3 shows an operation image when jumping directly to the FSP application written in the Serial Flash memory and executing on it.

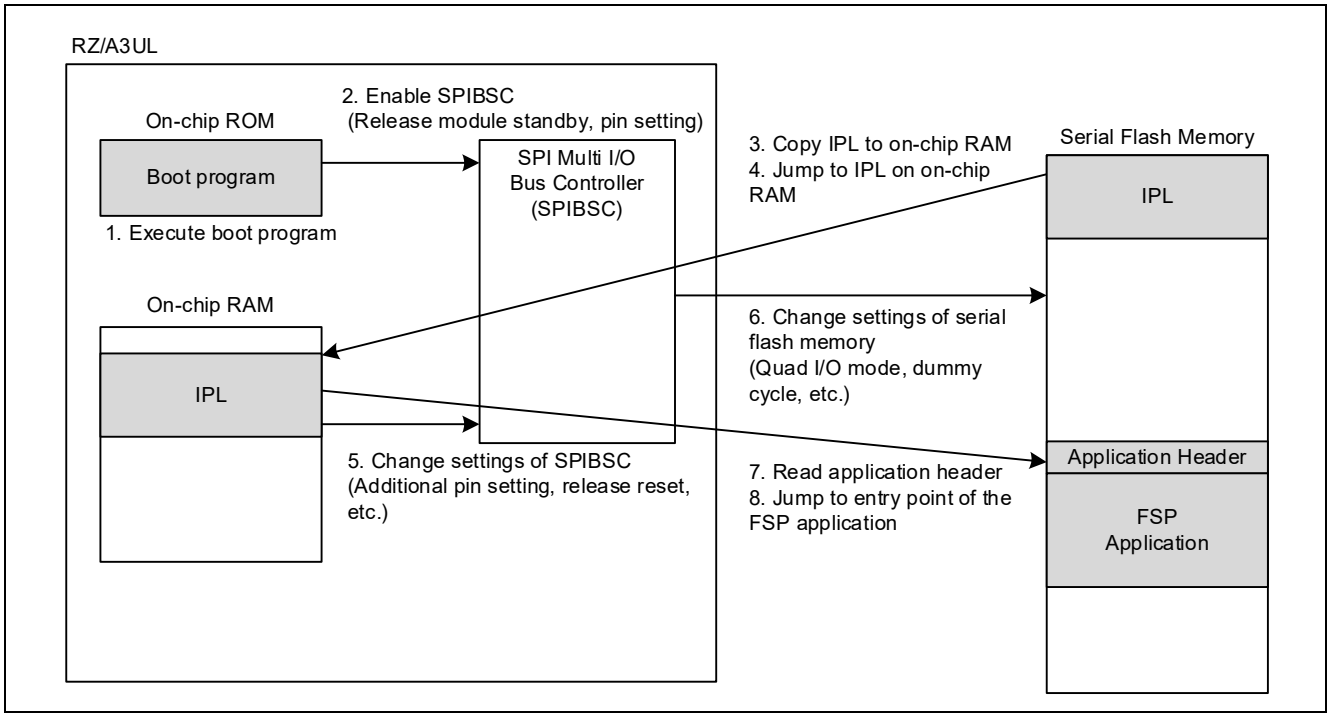


Figure 5.3 Operation image when booting FSP application on Serial Flash memory

Describes the IPL boot process.

1. RZ/A3UL executes the BootROM program after releasing the power-on reset.
2. When the RZ/A3UL operating mode is Boot mode 3, the BootROM program will enable SPIBSC and initialize it.
   The initial setting is that it can be accessed independently of the model of Serial Flash memory.
3. The BootROM program reads the IPL stored in the start address of the Serial Flash memory and copies the IPL to the entry point address on the On-chip RAM.
   Then the SPIBSC is reset by the BootROM, and access to the Serial Flash memory will be prohibited.
4. The BootROM program jumps to the IPL entry point on the On-chip RAM.
5. IPL makes additional pin settings and resets for SPIBSC for 4-byte access to the Serial Flash memory and changes the settings to the optimum settings for the Serial Flash memory (AT25QL128A) mounted on the SMARC EVK board.
6. A command is issued via the SPIBSC to the Serial Flash memory to change the settings.
7. IPL reads the application header.
   If the copy destination address of the FSP application is the same as the stored address, IPL will skip the copy process.
8. IPL will jump to the entry point of the FSP application in Serial Flash memory according to the contents of the application header.

5.2 Peripheral Function Setting

Table 5.1 Lists the settings for Peripheral Functions during execution of IPL.

Table 5.1 Settings for Peripheral Functions (1/2)

Module	Settings
CPG	Set the following operating frequencies. • CPU clock (Iϕ): 1.0GHz Set to 1/1 times the frequency of the PLL1 (FOUT) • Peripheral clock 0 (P0ϕ): 100MHz Set to 1/8 times the frequency of the PLL2 (FOUT1PH0) • Peripheral clock 1 / SRAM ACPU clock (P1ϕ): 200MHz Set to 1/8 times the frequency of the PLL3 (FOUT1PH0) • SRAM MCPU clock (I2ϕ): 200MHz Set to 1/8 times the frequency of the PLL3 (FOUT1PH0) • SPI multi I/O main clock (SPI0ϕ): 133.25MHz Set to 1/8 times the frequency of the PLL3 (FOUT3) • QSPI0_SPCLK: 66.625MHz 1/2 times of SPI0ϕ Supply clock and release reset to the peripherals shown below Release the reset • AXI Bus • Peripheral Bus • On-chip RAM • Internal ROM • DDR SDRAM • OTP • GIC-600 • IA55 • SYSC • SYC • DMAC • WDT • GPIO • SPIBSC • SCIFA (ch0 only) • CoreSight™
SPIBSC	• Command-Address-Data bits 1-4-4 • Opcode "Fast Read Quad I/O" EBh • Address size 3-byte • Additional data 1-byte 0x55 • Dummy cycles 6 QSPI0_SPCLK • SLCH 1.5 QSPI0_SPCLK (22.5ns) • CLSH 1 QSPI0_SPCLK (15ns) • SHSL 7 QSPI0_SPCLK (105ns)

Table 5.2 Settings for Peripheral Functions (2/2)

Module	Settings
GPIO	Set the following shared pin • P6_3: SCIF0_RXD • P6_4: SCIF0_TXD Set the following in P6_3 and P6_4 • Drive capacity: 4mA • Slew rate: Fast • Pull up: None • Pull down: None Set the following for the decided pins of QSPI0_IO0, QSPI0_IO1, QSPI0_IO2, QSPI0_IO3, QSPI0_SPCLK, QSPI0_SSL • Output impedance: 66Ω • Slew rate: Fast • Pull up: None • Pull down: None
SCIFA	Set the following for Ch0 • Operation mode: asynchronous communication mode • Transfer rate: 115200bps • Data length: 8bit • Stop bit length: 1 bit • Parity: None • Flow control: disabled
SYC	Input 24MHz clock to Cortex®-A55 built-in Generic Timer

5.2.1 Settings of SPIBSC Register

Table 5.3 shows the SPIBSC register settings after the initial settings are completed.

These setting values include the results that reflect the settings described in the SPIBSC section in Table 5.1 Peripheral Function Settings.

Table 5.3 SPIBSC register setting value after initial setting (1/2)

Register	Settings
IOn output level while idle	
CMNCR.MOIIO0	B'11 (Hi-Z)
CMNCR.MOIIO1	B'11 (Hi-Z)
CMNCR.MOIIO2	B'11 (Hi-Z)
CMNCR.MOIIO3	B'11 (Hi-Z)
IOn output level while 1 bit transfer	
CMNCR.IO0FV	B'11 (Hi-Z)
CMNCR.IO2FV	B'01 (High)
CMNCR.IO3FV	B'01 (High)
Data bus size	
CMNCR.BSZ	B'00 (Single Serial Flash memory connected)
Clock delay	
SSLDR.SCKDL	B'000 (1.5 QSPI0_SPCLK)
SSL negation delay	
SSLDR.SLNDL	B'000 (1 QSPI0_SPCLK)
Next access delay	
SSLDR.SPNDL	B'110 (7 QSPI0_SPCLK)
SSL negation	
DRCR.SSLE	B'1 (Negated when the accessed address is not in sequential)
Read burst	
DRCR.RBE	B'1 (Burst enable)
Burst length	
DRCR.RBURST	B'00111 (8 data unit: 64 byte)
Command	
DRCMR.CMD	0xEB (Fast Read Quad I/O operation for AT25QL128A)
Optional command	
DRCMR.OCMD	0x00 (Not used)
Extended external address valid range	
DREAR.EAC	B'000
Extended upper address value	
DREAR.EAV	0x00
Option data	
DROPR.OPD3	0x55 (Settings to prevent transition to continuous read mode in AT25QL128A)
DROPR.OPD2	0x00
DROPR.OPD1	0x00
DROPR.OPD0	0x00

Table 5.4 SPIBSC register setting value after initial setting (2/2)

Register	Settings
Option data enable DRENR.OPDE	B'1000 (Outs OPD3)
Address enable DRENR.ADE	B'0111 (Outs address [23:0])
Optional command enable DRENR.OCDE	B'0 (Suppress OCMD)
Command enable DRENR.CDE	B'1 (Outs CMD)
Dummy cycle enable DRENR.DME	B'1 (Has dummy cycle)
Data read bit size DRENR.DRDB	B'10 (4 bit)
Option data bit size DRENR.OPDB	B'10 (4 bit)
Address bit size DRENR.ADB	B'10 (4 bit)
Optional command bit size DRENR.OCDB	B'00 (Not used)
Command bit size DRENR.CDB	B'00 (1 bit)
Amount of dummy cycle DRDMCR.DMCYC	B'00011 (4 cycles)
Address DDR enable DRDRENR.ADDRE	B'0 (SDR)
Option data DDR enable DRDRENR.OPDRE	B'0 (SDR)
Data read DDR enable DRDRENR.DRDRE	B'0 (SDR)
Device selection PHYCNT.PHYMEM	B'00 (SDR)
Clock timing switching PHYCNT.CKSEL	B'11
High-speed response mode PHYCNT.HS	B'0 (Disable)
DDR operation timing PHYOFFSET1.DDRTMG	B'11 (SDR)
Serial Flash memory operation timing PHYOFFSET2.OCTTMG	B'100 (Using Serial Flash memory)

5.3 Memory Map

Figure 5.4 shows the RZ/A3UL address space and the memory map of the SMARC EVK board.

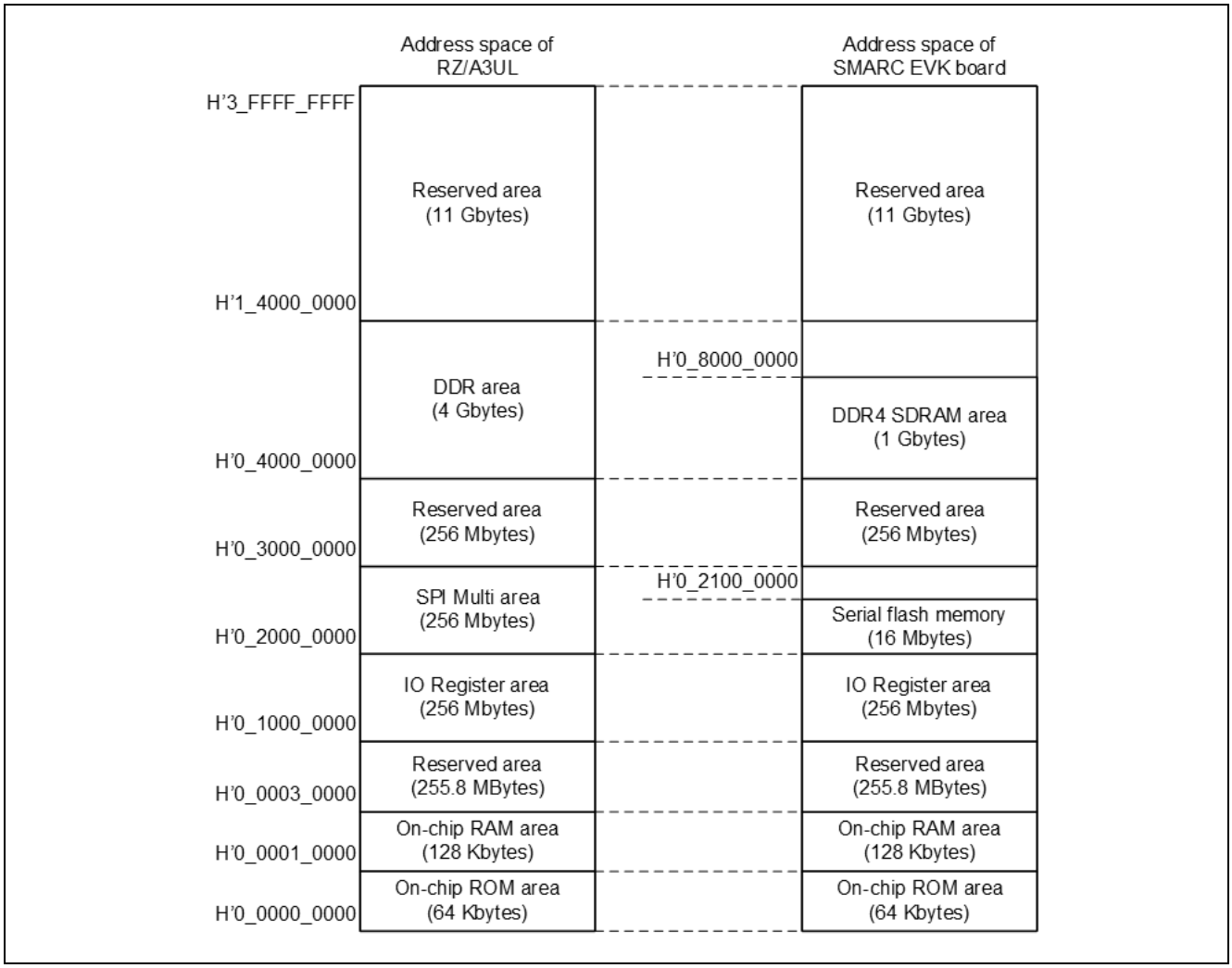


Figure 5.4 Memory MAP

5.4 MMU setting

Figure 5.5 shows the IPL MMU settings.

The MMU is disabled when jumping to the FSP Application.

Make the optimum settings in the FSP application if necessary.

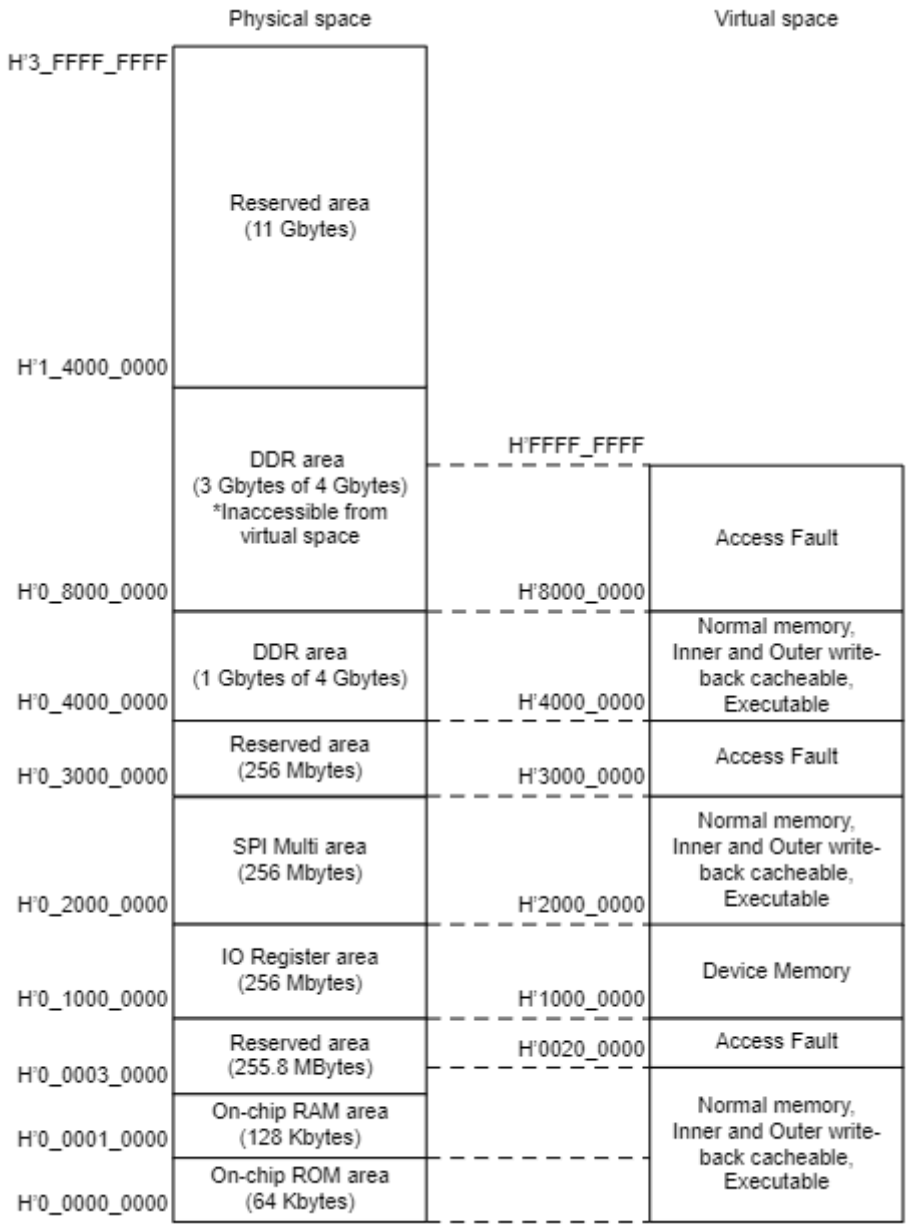


Figure 5.5 MMU setting

5.5 Interrupt used list

IPL does not use interrupt.

5.6 Exception level

IPL operates at exception level EL3.

It also jumps to the FSP Application in the state of EL3.

5.7 Application Header

IPL obtains the save address, copy destination address and entry point of the FSP Application image according to the application header written to the Serial Flash memory, copies the image, and jumps to the FSP Application.

IPL loads the application header from the address set in "FSP_BASE" in the make option.

Write the application header in advance in the format shown in the figure from the address set in "FSP_BASE" before executing IPL.

If "FSP_BASE" is not specified in the make command, H'2002_0000 is set as the default value. The header structure is shown below.

Table 5.5 Application Header

offset	size	Description
+0h	QWORD(8bytes)	FSP entry address
+8h	QWORD(8bytes)	Inverted FSP entry point address This is used to check if the header data is correct
+10h	QWORD(8bytes)	Address to copy the FSP image payload If FSP image payload does not need to transfer, this field must be set FSP payload address (FSP_BASE + 200h)
+18h	QWORD(8bytes)	Inverted address to copy the FSP image payload This is used to check if the header data is correct
+20h	QWORD(8bytes)	FSP image payload size
+28h	QWORD(8bytes)	Inverted FSP image payload size This is used to check if the header data is correct
+30h	-	Reserved (as 0)
+1E0h	String (MAX 32 bytes)	Signature "RZ FSP Application" and fill gap as 0
+200h later	-	FSP image payload

5.8 Data Types

Table 5.6 lists the data types used in IPL.

Table 5.6 Data Types used in the IPL

Symbol	Description
bool	Boolean type. Value is true (1) or false (0)
char	8-bit character.
int	Fast integer signed, 32-bit integer in the IPL.
int8_t	8-bit integer, signed (defined in standard library stdint.h)
int16_t	16-bit integer, signed (defined in standard library stdint.h)
int32_t	32-bit integer, signed (defined in standard library stdint.h)
int64_t	64-bit integer, signed (defined in standard library stdint.h)
uint8_t	8-bit integer, unsigned (defined in standard library stdint.h)
uint16_t	16-bit integer, unsigned (defined in standard library stdint.h)
uint32_t	32-bit integer, unsigned (defined in standard library stdint.h)
uint64_t	64-bit integer, unsigned (defined in standard library stdint.h)
unsigned long long	64-bit integer, unsigned
unsigned int	32-bit integer, unsigned
size_t	64-bit integer, unsigned
uintptr_t	Unsigned integer type with pointer type size, 64-bit unsigned integer in the IPL.

5.9 Constants

Table 5.7 to Table 5.9 lists the constants used in IPL.
Table 5.7 to Table 5.9 lists only constants used in the RZ/A3UL platform boot process.
Please refer to https://trustedfirmware-a.readthedocs.io/en/latest/ for constants related to behavior of Arm Trusted Firmware.

Table 5.7 Constants used in the IPL (1/3)

Constant	Setting Value	Description
RZ_IPL_VERSION_STRING	"v2.0.0"	IPL version
CPG_OFF	(0)	Flag to set ON/OFF of CPG register Set the register to off (disable)
CPG_ON	(1)	Flag to set ON/OFF of CPG register Set the register to on (enable)
CPG_T_CLK	(0)	Flag that specifies the type of CPG register to set Set a value in the clock register
CPG_T_RST	(1)	Flag that specifies the type of CPG register to set Set a value in the reset register
CPG_SEL_PLL1_ON_OFF	(0)	Number for specifying the element of the source clock selector setting table of PLL Specify selector for PLL1
CPG_SEL_PLL2_1_ON_OFF	(1)	Number for specifying the element of the source clock selector setting table of PLL Specify selector for PLL2_1
CPG_SEL_PLL2_2_ON_OFF	(2)	Number for specifying the element of the source clock selector setting table of PLL Specify selector for PLL2_2
CPG_SEL_PLL3_1_ON_OFF	(3)	Number for specifying the element of the source clock selector setting table of PLL Specify selector for PLL3_1
CPG_SEL_PLL3_2_ON_OFF	(4)	Number for specifying the element of the source clock selector setting table of PLL Specify selector for PLL3_2
CPG_SEL_PLL3_3_ON_OFF	(5)	Number for specifying the element of the source clock selector setting table of PLL Specify selector for PLL3_3
CPG_SEL_PLL5_1_ON_OFF	(6)	Number for specifying the element of the source clock selector setting table of PLL Specify selector for PLL5_1
CPG_SEL_PLL5_3_ON_OFF	(7)	Number for specifying the element of the source clock selector setting table of PLL Specify selector for PLL5_3
CPG_SEL_PLL5_4_ON_OFF	(8)	Number for specifying the element of the source clock selector setting table of PLL Specify selector for PLL5_4
CPG_SEL_PLL6_1_ON_OFF	(9)	Number for specifying the element of the source clock selector setting table of PLL Specify selector for PLL6_1
CPG_SEL_GPU1_1_ON_OFF	(10)	Number for specifying the element of the source clock selector setting table of PLL Specify selector for GPU1_1

Table 5.8 Constants used in the IPL (2/3)

Constant	Setting Value	Description
CPG_SEL_GPU1_2_ON_OFF	(11)	Number for specifying the element of the source clock selector setting table of PLL Specify selector for GPU1_2
CPG_SEL_GPU2_ON_OFF	(12)	Number for specifying the element of the source clock selector setting table of PLL Specify selector for GPU2
PFC_OFF	(0)	PFC disable setting flag
PFC_ON	(1)	PFC enable setting flag
XSPI_CLOCK_SPIM	(0)	Clock setting flag for Serial Flash memory
XSPI_CLOCK_OCTA	(1)	Clock setting flag for Octa Flash memory/Octa RAM
CPG_CLOCK_SPIM	(20)	CPG clock ID for Serial Flash memory
CPG_CLOCK_OCTA	(61)	CPG clock ID for Octa Flash memory/Octa RAM
DEFAULT_SPI_FREQUENCY	(1000000)	Default operating frequency of Serial Flash memory
RESET_DURATION_US	(10)	SPI device reset time (10usec)
WRITE_STATUS_OK	(0)	xSPI device write status Successful write to xSPI device
WRITE_STATUS_IN_PROGRESS	(1)	xSPI device write status While writing to the xSPI device
WRITE_STATUS_PROTECTED	(2)	xSPI device write status xSPI devices are write protected
WRITE_STATUS_FAIL	(3)	xSPI device write status Write failure to xSPI device
WRITE_STATUS_SUSPENDED	(4)	xSPI device write status Write suspend to xSPI device
SPI_FORM_1_1_1	(0)	Command executes at 1-1-1 form
SPI_FORM_1_1_2	(1)	Command executes at 1-1-2 form
SPI_FORM_1_2_2	(2)	Command executes at 1-2-2 form
SPI_FORM_2_2_2	(3)	Command executes at 2-2-2 form
SPI_FORM_1_1_4	(4)	Command executes at 1-1-4 form
SPI_FORM_1_4_4	(5)	Command executes at 1-4-4 form
SPI_FORM_4_4_4	(6)	Command executes at 4-4-4 form
SPI_FORM_1_1_8	(7)	Command executes at 1-1-8 form
SPI_FORM_1_8_8	(8)	Command executes at 1-8-8 form
SPI_FORM_8_8_8	(9)	Command executes at 8-8-8 form
XSPI_FEATURE_FORM112	(1 << 0)	The driver supports 1-1-2 form.
XSPI_FEATURE_FORM122	(1 << 1)	The driver supports 1-2-2 form.
XSPI_FEATURE_FORM222	(1 << 2)	The driver supports 2-2-2 form.
XSPI_FEATURE_DUAL	(0x07)	The driver supports 1-1-2, 1-2-2, and/or 2-2-2 form(s).
XSPI_FEATURE_FORM114	(1 << 3)	The driver supports 1-1-4 form.
XSPI_FEATURE_FORM144	(1 << 4)	The driver supports 1-4-4 form.
XSPI_FEATURE_FORM444	(1 << 5)	The driver supports 4-4-4 form.
XSPI_FEATURE_QUAD	(0x38)	The driver supports 1-1-4, 1-4-4, and/or 4-4-4 form(s).

Table 5.9 Constants used in the IPL (3/3)

Constant	Setting Value	Description
XSPI_FEATURE_FORM118	(1 << 6)	The driver supports 1-1-4 form.
XSPI_FEATURE_FORM188	(1 << 7)	The driver supports 1-8-8 form.
XSPI_FEATURE_FORM888	(1 << 8)	The driver supports 8-8-8 form.
XSPI_FEATURE_OCTAL	(0x1C0)	The driver supports 1-1-8, 1-8-8, and/or 8-8-8 form(s).
XSPI_FEATURE_XIP_READ	(1 << 12)	The driver supports read access.
XSPI_FEATURE_XIP_WRITE	(1 << 13)	The driver supports write access.
XSPI_FEATURE_DDROP	(1 << 14)	The driver supports DDR for op code.
XSPI_FEATURE_DDR	(1 << 15)	The driver supports DDR for address and/or data.
XSPI_FEATURE_OCTARAM	(1 << 16)	Octa RAM addressing (RAS/CAS) supported.
XSPI_FLAGS_SEQUENTIAL_DDR	(1u << 0)	Enable inverted order for DDR transfer
XSPI_FLAGS_FORCE_STROBE	(1u << 1)	Force to use data strobe signal for timing reference
XSPI_FLAGS_DATA_ACCESS	(1u << 2)	Force to use data access method for exec_op
RZ_NOFIP	(0)	How to load the Application image Use the Application Header when loading the Application image
RZ_FIP	(1)	How to load the Application image: Use FIP format image when loading Application image
RZ_APP_PAYLOAD_OFFSET	(0x200)	Offset to payload data in Application header
RZA_MMU_ATTR_NON_CACHEABLE	(0x44)	MMU descriptor normal memory, non-cacheable memory attribute
RZA_MMU_ATTR_DEVICE	(0x04)	MMU descriptor device memory attribute
RZA_MMU_ATTR_IWBWA_OWBWA _NTR	(0xFF)	MMU descriptor normal memory, cacheable memory attribute
RZA_MMU_ATTRIBUTE_ACCESS_FAULT	(0x00000000)	MMU descriptor Access Fault
RZA_MMU_ATTRIBUTE_CONFIG _END	(0xFFFFFFFF)	End of MMU configuration table setting

5.10 Structures/Unions

Table 5.10 lists the structures/unions used in IPL.
Table 5.10 lists only structures/unions used in the RZ/A3UL platform boot process.

Please refer to https://trustedfirmware-a.readthedocs.io/en/latest/ for structures/unions related to behavior of Arm Trusted Firmware.

Table 5.10 List of structures used in the IPL

Structure/Union	Description	Detail
fsp_app_header_t	Structure to store the Application Header	Refer to Table 5.11
qspiflash_at25_ctrl_t	Structure to store the control information of AT25QL128A	Refer to Table 5.12
qspiflash_at25_ext_t	Structure to store the extended information of AT25QL128A	Refer to Table 5.13
spiflash_ctrl_t	Structure to store the control information of Serial Flash memory driver	Refer to Table 5.14
spiflash_ext_t	Structure to store the extended information of Serial Flash memory driver	Refer to Table 5.15
spim_ctrl_t	Structure to store the control information of xSPI module	Refer to Table 5.16
spim_ext_t	Structure to store the extended information of xSPI module	Refer to Table 5.17
xspidevice_info_t	Structure to store the device information of xSPI device	Refer to Table 5.18
xspidevice_cfg_t	Structure to store the configure information of xSPI device	Refer to Table 5.19
xspidevice_api_t	Structure to store the API functions that control xSPI device	Refer to Table 5.20
xspidevice_instance_t	Structure to store the instance that control xSPI device	Refer to Table 5.21
xspi_cfg_t	Structure to store the configure information of xSPI interface	Refer to Table 5.22
xspi_op_t	Structure to store the operation of xSPI interface	Refer to Table 5.23
xspi_api_t	Structure to store the API functions of the xSPI interface	Refer to Table 5.25
xspi_instance_t	Structure to store the instance of the xSPI interface	Refer to Table 5.26
CPG_SETUP_DATA	A structure that stores the startup setting data of the CPG register	Refer to Table 5.27
CPG_REG_SETTING	A structure that stores the set values for the CPG registers	Refer to Table 5.28
CPG_PLL_SETDATA_146	Structure to save setting parameters for PLL1/4/6	Refer to Table 5.29
CPG_PLL_SETDATA_235	Structure to save setting parameters for PLL2/3/5	Refer to Table 5.30
cpg_spi_clk_table	Structure to store clock setting parameters for Serial Flash memory	Refer to Table 5.31
PFC_REG_UINT8	A structure that stores the setting parameters for the 8byte width PFC register	Refer to Table 5.32
PFC_REG_UINT32	A structure that stores the setting parameters for the 32byte width PFC register	Refer to Table 5.33
PFC_REG_UINT64	A structure that stores the setting parameters for the 64byte width PFC register	Refer to Table 5.34
PFC_REGS	A structure that stores the set values for the PFC registers	Refer to Table 5.35
rz_mmu_pgtbl_cfg_t	Structure that stores MMU page table configuration parameters	Refer to Table 5.36

Table 5.11 Application Header structure (fsp_app_header_t)

Member	Description
uint64_t entry_addr	FSP entry point address
uint64_t entry_addr_inv	Inverted FSP entry point address
uint64_t dest_addr	Address to copy the FSP image payload
uint64_t dest_addr_inv	Inverted address to copy the FSP image payload
uint64_t payload_size	FSP image payload size
uint64_t payload_size_inv	Inverted FSP image payload size
uint8_t padding[432]	Reserved
uint8_t signature[32]	Signature
uint8_t app_payload_start	Application image payload

Table 5.12 AT25QL128A control structure (qspiflash_at25_ctrl_t)

Member	Description
bool opened	Opened or not
const xspi_instance_t * xspi	xSPI control driver instance

Table 5.13 AT25QL128A extended information structure (qspiflash_at25_ext_t)

Member	Description
-	Member not defined because extended information is not used in default IPL

Table 5.14 Serial Flash memory control structure (spiflash_ctrl_t)

Member	Description
bool opened	Opened or not
const xspi_instance_t * xspi	xSPI control driver instance
bool address_is_4b	Flag to use 4bit command

Table 5.15 Serial Flash memory extended information structure (spiflash_ext_t)

Member	Description
bool address_is_4b	Flag to use 4bit command

Table 5.16 xSPI module control structure (spim_ctrl_t)

Member	Description
bool opened	Opened or not
uintptr_t reg_base	Pointer to register base address
uintptr_t mmap_base	Pointer to base address of area allocated in External Space Address Read Mode
size_t mmap_size	Size allocated in Eternal Space Address Read Mode (as byte)
uint8_t channel	Channel number (0 based)

Table 5.17 xSPI module extended information structure (spim_ext_t)

Member	Description
bool voltage_is_3300mv	Specify the target voltage is 3.3V Only affected is FORCE_VOLTAGE_SETTING is defined as true. Default: false (1.8v)

Table 5.18 xSPI device information structure (xspidevice_info_t)

Member	Description
uint32_t capacity	Amount of memory by bytes.
uint32_t minimum_erase_size	Minimum erase size by bytes.
char decide_vendor[32]	Device vendor name.
char device_product[32]	Device product name.

Table 5.19 xSPI device configure structure (xspidevice_cfg_t)

Member	Description
xspi_instance_t *xspi	Associated xSPI instance.
void const *extend	device specific configuration data.

Table 5.20 xSPI device API function structure (xspidevice_api_t)

Member	Description
int (* open)(xspidevice_ctrl_t * ctrl, xspidevice_cfg_t const * cfg)	Open function
int (* close)(xspidevice_ctrl_t * ctrl)	Close function
int (* exec_op)(xspidevice_ctrl_t * ctrl, xspi_op_t const * op, bool is_write)	Operation Execution function
int (* enter_xip)(xspidevice_ctrl_t * ctrl)	Entering in-place access mode function
int (* exit_xip)(xspidevice_ctrl_t * ctrl)	Exiting in-place access mode function
int (* get_info)(xspidevice_ctrl_t * ctrl, xspidevice_info_t * info)	Getting device information function
int (* read)(xspidevice_ctrl_t * ctrl, void * buffer, size_t address, size_t length)	Read function
int (* write)(xspidevice_ctrl_t * ctrl, void const * buffer, size_t address, size_t length)	Write function
int (* erase)(xspidevice_ctrl_t * ctrl, size_t address, size_t length)	Erase function
enum xspidevice_write_status (* get_write_status)(xspidevice_ctrl_t * ctrl)	Getting write status function

Table 5.21 xSPI device instance structure (xspidevice_instance_t)

Member	Description
xspidevice_ctrl_t * ctrl	Control parameter
xspidevice_cfg_t const * cfg	Configuration parameter
xspidevice_api_t const * api	API functions

Table 5.22 xSPI interface control structure (xspi_cfg_t)

Member	Description
uint8_t channel	Channel number
uintptr_t base	Pointer to register base address
void const * extend	IP specific configuration data

Table 5.23 xSPI interface operation structure (xspi_op_t) (1/2)

Member	Description
xspi_transfer_form_t form	Specify the form to send this operation It is possible to set the parameters shown in the following SPI_FORM_X_Y_Z format X, Y, and Z indicate the number of I/O data lines used when transferring the following information in operation X: Operation Code Y: Address Z: Data SPI_FORM_1_1_1 SPI_FORM_1_1_2 SPI_FORM_1_2_2 SPI_FORM_2_2_2 SPI_FORM_1_4_4 SPI_FORM_4_4_4 SPI_FORM_1_1_8 SPI_FORM_1_8_8 SPI_FORM_8_8_8
uint16_t op	Operation code (high side used as second byte)
uint8_t op_size	Operation code size (0 to 2)
bool op_is_ddr	If true, the op-code phase sends as DDR The Serial Flash memory driver does not support DDR format Even if true is set, serial transfer is performed in SDR format
uint32_t address	Address on Serial Flash memory
uint8_t address_size	Address size (0 to 4)
bool address_is_ddr	If true, the address phase sends as DDR The Serial Flash memory driver does not support DDR format Even if true is set, serial transfer is performed in SDR format.
uint8_t additional_size	Additional data size as bytes after the address phase If address_is_ddr is true, this cycle is also as DDR, and this size must be zero or even
uint32_t additional_value	Additional data value • [0-byte] Not used • [1-byte] Use b0-b7 as value • [2-byte] Use b8-b15 as 1st value and b0-b7 as 2nd value • [3-byte] Use b16-b23 as 1st value, b8-b15 as 2nd value and b0-b7 as 3rd value • [4-byte] Use b24-b31 as 1st value, b16-b23 as 2nd value, b8-b15 as 3rd value and b0-b7 as 4th value
uint8_t dummy_cycles	Dummy cycles as the SPCLK count after additional data phase. This cycle does not include additional data phase size.
size_t transfer_size	Transfer size as bytes (ignored for External Space Address Read Mode configuration)
void* transfer_buffer	Transfer buffer pointer (ignored for External Space Address Read Mode configuration)
bool transfer_is_ddr	Whether the transfer phase is DDR. The Serial Flash memory driver does not support DDR format Even if true is set, serial transfer is performed in SDR format

Table 5.24 xSPI interface operation structure (xspi_op_t) (2/2)

Member	Description
uint8_t transfer_flag	Additional transfer flags These flags can be bitwise-or' d • b0: Enable inverted order for DDR transfer (0: w1 w0 w3 w2, 1: w0 w1 w2 w3) • b1: Force to use of data strobe for timing reference If not specified, operation executes as register access • b2: Force to use of data strobe signal for timing reference
uint8_t force_idle_level_mask	Whether or not to force each IO level during idle state Not all controllers support it The idle state does not include the dummy cycle. The dummy cycle is always Hi-Z • b0: Ignored b1 – b7: 0: Always Hi-Z, 1: Forcibly outs the force_idle_level_value's state
uint8_t force_idle_level_value	IO level during idle state Only active if force_idle_mask of the same position is 1 • b0: Ignored b1 – b7: 0: Low, 1: High
uint8_t slch_value	SSL Low to Clock High delay cycles as the SPCLK count (also known as CS# Active Setup Time)
uint8_t clsh_value	Clock Low to SSL High delay cycles as the SPCLK count (also known as CS# Active Hold Time)
uint8_t shsl_value	SSL High to SSL Low delay cycles as the SPCLK count (also known as CS# Deselect Time)

Table 5.25 xSPI interface API function structure (xspi_api_t)

Member	Description
int (* open)(xspi_ctrl_t * ctrl, xspi_cfg_t const * const cfg)	Open function
int (* close)(xspi_ctrl_t * const ctrl)	Close function
int (* post_init)(xspi_ctrl_t * const ctrl)	Post initialization function
int (* exec_op)(xspi_ctrl_t * const ctrl, xspi_op_t const * const op, bool is_write)	Operation Execution function
int (* configure_xip)(xspi_ctrl_t * const ctrl, xspi_op_t const * const rop, xspi_op_t const * const wop)	Configure for in-place access mode function
int (* start_xip)(xspi_ctrl_t * const ctrl)	Start in-place access mode function
int (* stop_xip)(xspi_ctrl_t * const ctrl)	Stop in-place access mode function
int (* run_manual_calibration)(xspi_ctrl_t * const ctrl)	Manual calibration function
int (* enable_auto_calibration)(xspi_ctrl_t * const ctrl)	Enable auto calibration function
int (* disable_auto_calibration)(xspi_ctrl_t * const ctrl)	Disable auto calibration function
int (* set_frequency)(xspi_ctrl_t * const ctrl, int frequency_hz)	Setting SPI frequency function
int (* inv_mmap)(xspi_ctrl_t * const ctrl)	Invalidate cache for entire MMAP function
int (* clean_mmap)(xspi_ctrl_t * const ctrl)	Clean cache for entire MMAP function
uintptr_t (* get_mmap_base)(xspi_ctrl_t * const ctrl)	Getting MMAP base address
size_t (* get_mmap_size)(xspi_ctrl_t * const ctrl)	Getting MMAP size

Table 5.26 xSPI interface instance structure (xspi_instance_t)

Member	Description
xspi_ctrl_t * ctrl	Pointer to the control structure for instance
xspi_cfg_t const * cfg	Pointer to the configuration structure for instance
xspi_api_t const * api	Pointer to the API structure for instance

Table 5.27 CPG setup data structure (CPG_SETUP_DATA)

Member	Description
uintptr_t reg	Pointer to CPG register
uintptr_t mon	CPG monitor register corresponding to the register specified by "reg"
uint32_t val	Setting value to CPG register
uint32_t type	Select the type of register to be set from the following CPG_T_CLK (clock operation) CPG_T_RST (reset operation)

Table 5.28 CPG register setting structure (CPG_REG_SETTING)

Member	Description
uintptr_t reg	Pointer to CPG register
uint32_t val	Setting value to CPG register

Table 5.29 PLL1/4/6 setting structure (CPG_PLL_SETDATA_146)

Member	Description
CPG_REG_SETTING clk1_dat	Register setting to CPG_SAMPLL1/4/6_CLK1
CPG_REG_SETTING clk2_dat	Register setting to CPG_SAMPLL1/4/6_CLK2
CPG_REG_SETTING stby_dat	Register setting to CPG_SAMPLL1/4/6_STBY

Table 5.30 PLL2/3/5 setting structure (CPG_PLL_SETDATA_235)

Member	Description
CPG_REG_SETTING clk1_dat	Register setting to CPG_SAMPLL5_CLK1 CPG_SAMPLL2/3_CLK1 register is not implemented in RZ/A3UL
CPG_REG_SETTING clk2_dat	Register setting to CPG_SAMPLL5_CLK2 CPG_SAMPLL2/3_CLK2 register is not implemented in RZ/A3UL
CPG_REG_SETTING clk2_dat	Register setting to CPG_SAMPLL5_CLK3 CPG_SAMPLL2/3_CLK3 register is not implemented in RZ/A3UL
CPG_REG_SETTING clk4_dat	Register setting to CPG_SAMPLL5_CLK4 CPG_SAMPLL2/3_CLK2 register is not implemented in RZ/A3UL
CPG_REG_SETTING clk5_dat	Register setting to CPG_SAMPLL5_CLK5 CPG_SAMPLL2/3_CLK2 register is not implemented in RZ/A3UL
CPG_REG_SETTING stby_dat	Register setting to CPG_SAMPLL5_STBY CPG_SAMPLL2/3_STBY register is not implemented in RZ/A3UL

Table 5.31 spi clock table structure (cpg_spi_clk_table)

Member	Description
int frequency	Frequency setting
uint8_t selector	Source clock selector setting
uint8_t divider	Clock divide rate setting

Table 5.32 PFC 8byte register setting structure (PFC_REG_UINT8)

Member	Description
int flag	PFC ON / OFF setting
uintptr_t reg	Pointer to PFC register
uint8_t val	Setting value to PFC register

Table 5.33 PFC 32byte register setting structure (PFC_REG_UINT32)

Member	Description
int flag	PFC ON / OFF setting
uintptr_t reg	Pointer to PFC register
uint32_t val	Setting value to PFC register

Table 5.34 PFC 64byteregister setting structure (PFC_REG_UINT64)

Member	Description
int flag	PFC ON / OFF setting
uintptr_t reg	Pointer to PFC register
uint64_t val	Setting value to PFC register

Table 5.35 PFC register setting structure (PFC_REGS)

Member	Description
PFC_REG_UINT8 pmc	Setting to PMC register
PFC_REG_UINT32 pfc	Setting to PFC register
PFC_REG_UINT64 iolh	Setting to IOLH register
PFC_REG_UINT64 pupd	Setting to PUPD register
PFC_REG_UINT64 sr	Setting to SR register
PFC_REG_UINT64 ien	Setting to IEN register

Table 5.36 MMU page table setting structure (rza_mmu_pgtbl_cfg_t)

Member	Description
uint64_t vaddress	Virtual address (0x200000 aligned address)
uint64_t paddress	Physical address (0x200000 aligned address)
uint64_t size	Page size (0x200000 aligned address)
uint64_t attribute	Memory attribute

5.11 Variables

Table 5.37 lists the variables used in IPL.
Table 5.37 lists only structures/unions used in the RZ/A3UL platform boot process.

Table 5.37 List of variables used in the IPL

variable name	Description	Detail
xspi_api_t spim_api	xSPI control driver API function table	Refer to Table 5.38
xspidevice_api_t qspiflash_at25_api	AT25QL128A driver API function table	Refer to Table 5.39
xspi_op_t op_write_enable	Write Enable operation table (H'06)	Refer to Table 5.40
xspi_op_t op_read_status1	Read Status Register-1 operation table (H'05)	Refer to Table 5.41
xspi_op_t op_read_status2	Read Status Register-2 operation table (H'35)	Refer to Table 5.42
xspi_op_t op_write_status2	Write Status Register-2 operation table (H'31)	Refer to Table 5.43
xspi_op_t rop	Fast Read Quad I/O operation table (H'EB)	Refer to Table 5.44
xspi_op_t op_page_program	Quad Page Program operation table (H'33)	Refer to Table 5.45
xspi_op_t op_erase_4k	4Kbytes Block Erase operation table (H'20)	Refer to Table 5.46
xspi_op_t op_erase_32k	32Kbytes Block Erase operation table (H'52)	Refer to Table 5.47
xspi_op_t op_erase_64k	64Kbytes Block Erase operation table (H'D8)	Refer to Table 5.48
CPG_PLL_SETDATA_146 cpg_pll4_setdata	PLL4 operation setting parameters	Refer to Table 5.49
CPG_PLL_SETDATA_146 cpg_pll6_setdata	PLL6 operation setting parameters	Refer to Table 5.50
CPG_SETUP_DATA early_setup_tbl[]	CPG setting table for modules used for IPL initialization	Refer to Table 5.51
CPG_SETUP_DATA cpg_clk_on_tbl[]	CPG setting table for clock supplying module	Refer to Table 5.52, Table 5.53, Table 5.54
CPG_SETUP_DATA cpg_reset_tbl[]	CPG setting table for modules to be released from reset	Refer to Table 5.55, Table 5.56, Table 5.57
CPG_REG_SETTING cpg_static_select_tbl[]	Clock selector register table that stops clock supply when register settings are changed	Refer to Table 5.58
CPG_REG_SETTING cpg_dynamic_select_tbl[]	Table of clock selector registers whose settings can be changed while the clock is being supplied	Refer to Table 5.59
PFC_REGS pfc_mux_reg_tbl[]	Pin setting table for modules used in boot processing	Refer to Table 5.60
PFC_REGS fc_qspi_reg_tbl[]	Serial Flash memory pin setting table	Refer to Table 5.61, Table 5.62
rza_mmu_pgtbl_cfg_t g_mmu_pagetable_array[]	MMU setting table	Refer to Table 5.63

Table 5.38 xSPI control driver API function table (spim_api)

Member	Setting value	Description
open	spim_open	xSPI control driver open function
close	spim_close	xSPI control driver close function
post_init	spim_post_init	xSPI control driver post initialization function
exec_op	spim_exec_op	xSPI control driver operation function
configure_xip	spim_configure_xip	xSPI control driver External Space Address Read Mode setting function
start_xip	spim_start_xip	xSPI control driver External Space Address Read Mode start function
stop_xip	spim_stop_xip	xSPI control driver External Space Address Read Mode stop function
run_manual_calibration	spim_run_manual_calibration	xSPI control driver manual calibration function
enable_auto_calibration	spim_enable_auto_calibration	xSPI control driver auto calibration enable function
disable_auto_calibration	spim_disable_auto_calibration	xSPI control driver auto calibration disable function
set_frequency	spim_set_frequency	xSPI control driver operation frequency setting function
clean_mmap	spim_clean_mmap	xSPI control driver cache clean function
inv_mmap	spim_inv_mmap	xSPI control driver cache invalid function
get_mmap_base	spim_get_mmap_base	xSPI control driver memory map region address get function
get_mmap_size	spim_get_mmap_size	xSPI control driver memory map region size get function

Table 5.39 AT25QL128A driver API function table (qspiflash_at25_api)

Member	Setting value	Description
open	flash_open	AT25QL128A open function
close	flash_close	AT25QL128A close function
exec_op	flash_exec_op	AT25QL128A operation function
enter_xip	flash_enter_xip	AT25QL128A External Space Address Read Mode start function
exit_xip	flash_exit_xip	AT25QL128A External Space Address Read Mode stop function
get_info	flash_get_info	AT25QL128A information get function
read	flash_read	AT25QL128A read function
write	flash_write	AT25QL128A write function
erase	flash_erase	AT25QL128A erase function
get_write_status	flash_get_write_status	AT25QL128A write status get function

Table 5.40 Operation table: "Write Enable" (op_write_enable)

Member	Setting value	Description
form	SPI_FORM_1_1_1	Command bit width: 1bit Address bit width: 1bit Data bit width: 1bit
op	0x06	Command code "Write Enable"
op_size	1	Command size
op_is_ddr	false	Command transfer method (SDR)
address	0	Address
address_is_ddr	false	Address transfer method (SDR)
address_size	0	Address size
additional_value	0	Option data
additional_size	0	Option data size
dummy_cycles	0	Number of dummy cycles
transfer_buffer	NULL	Data buffer
transfer_is_ddr	false	Data transfer method (SDR)
transfer_size	0	Data size
force_idle_level_mask	0x08	Keep IO3/HOLD pin to High
force_idle_level_value	0x08	Keep IO3/HOLD pin to High
slch_value	0	Clock Delay SSLDR register SCKDL bit value
clsh_value	0	SSL Negation Delay CHSH: 5ns, CLSH=5ns - 1/SPI frequency = -10ns SSLDR register SLNDL bit value
shsl_value	6	Next Access Delay SSLDR register SPNDL bit value

Table 5.41 Operation table: "Read Status Register-1" (op_read_status1)

Member	Setting value	Description
form	SPI_FORM_1_1_1	Command bit width: 1bit Address bit width: 1bi Data bit width: 1bit
op	0x05	Command code "Read Status Register-1"
op_size	1	Command size
op_is_ddr	false	Command transfer method (SDR)
address	0	Address
address_is_ddr	false	Address transfer method (SDR)
address_size	0	Address size
additional_value	0	Option data
additional_size	0	Option data size
dummy_cycles	0	Number of dummy cycles
transfer_buffer	NULL	Data buffer This parameter is updated to the address of the buffer from which the register value is read when communicating with Serial Flash memory
transfer_is_ddr	false	Data transfer method (SDR)
transfer_size	1	Data size
force_idle_level_mask	0x08	Keep IO3/HOLD pin to High
force_idle_level_value	0x08	Keep IO3/HOLD pin to High
slch_value	0	Clock Delay SSLDR register SCKDL bit value
clsh_value	0	SSL Negation Delay CHSH: 5ns, CLSH=5ns - 1/SPI frequency = -10ns SSLDR register SLNDL bit value
shsl_value	6	Next Access Delay SSLDR register SPNDL bit value

Table 5.42 Operation table: "Read Status Register-2" (op_read_status2)

Member	Setting value	Description
form	SPI_FORM_1_1_1	Command bit width: 1bit Address bit width: 1bit Data bit width: 1bit
op	0x35	Command code "Read Status Register-2"
op_size	1	Command size
op_is_ddr	false	Command transfer method (SDR)
address	0	Address
address_is_ddr	false	Address transfer method (SDR)
address_size	0	Address size
additional_value	0	Option data
additional_size	0	Option data size
dummy_cycles	0	Number of dummy cycles
transfer_buffer	NULL	Data buffer This parameter is updated to the address of the buffer from which the register value is read when communicating with Serial Flash memory
transfer_is_ddr	false	Data transfer method (SDR)
transfer_size	1	Data size
force_idle_level_mask	0x08	Keep IO3/HOLD pin to High
force_idle_level_value	0x08	Keep IO3/HOLD pin to High
slch_value	0	Clock Delay SSLDR register SCKDL bit value
clsh_value	0	SSL Negation Delay CHSH: 5ns, CLSH=5ns - 1/SPI frequency = -10ns SSLDR register SLNDL bit value
shsl_value	6	Next Access Delay SSLDR register SPNDL bit value

Table 5.43 Operation table: "Write Status Register-2" (op_write_status2)

Member	Setting value	Description
form	SPI_FORM_1_1_1	Command bit width: 1bit Address bit width: 1bit Data bit width: 1bit
op	0x31	Command code "Write Status Register-2"
op_size	1	Command size
op_is_ddr	false	Command transfer method (SDR)
address	0	Address
address_is_ddr	false	Address transfer method (SDR)
address_size	0	Address size
additional_value	0	Option data
additional_size	0	Option data size
dummy_cycles	0	Number of dummy cycles
transfer_buffer	NULL	Data buffer This parameter is updated to the address of the buffer that stores the set value to the register when communicating with Serial Flash memory
transfer_is_ddr	false	Data transfer method (SDR)
transfer_size	1	Data size
force_idle_level_mask	0x08	Keep IO3/HOLD pin to High
force_idle_level_value	0x08	Keep IO3/HOLD pin to High
slch_value	0	Clock Delay SSLDR register SCKDL bit value
clsh_value	0	SSL Negation Delay CHSH: 5ns, CLSH=5ns - 1/SPI frequency = -10ns SSLDR register SLNDL bit value
shsl_value	6	Next Access Delay SSLDR register SPNDL bit value

Table 5.44 Operation table: "Fast Read Quad I/O"(rop)

Member	Setting value	Description
form	SPI_FORM_1_4_4	Command bit width: 1bit Address bit width: 4bit Data bit width: 4bit
op	0xEB	Command code "Fast Read Quad I/O"
op_size	1	Command size
op_is_ddr	false	Command transfer method (SDR)
address	0	Address
address_is_ddr	false	Address transfer method (SDR)
address_size	3	Address size
additional_value	0x55555555	Option data
additional_size	1	Option data size
dummy_cycles	4	Number of dummy cycles
transfer_buffer	NULL	Data buffer This parameter is not used in IPL because data is not read by serial communication
transfer_is_ddr	false	Data transfer method (SDR)
transfer_size	0	Data size This value is updated when communicating with Serial Flash memory
force_idle_level_mask	0x08	Keep IO3/HOLD pin to High
force_idle_level_value	0x08	Keep IO3/HOLD pin to High
slch_value	0	Clock Delay SSLDR register SCKDL bit value
clsh_value	0	SSL Negation Delay CHSH: 5ns, CLSH=5ns - 1/SPI frequency = -10ns SSLDR register SLNDL bit value
shsl_value	6	Next Access Delay SSLDR register SPNDL bit value

Table 5.45 Operation table: "Quad Page Program" (op_page_program)

Member	Setting value	Description
form	SPI_FORM_1_4_4	Command bit width: 1bit Address bit width: 4bit Data bit width: 4bit
op	0x33	Command code "Quad Page Program"
op_size	1	Command size
op_is_ddr	false	Command transfer method (SDR)
address	0	Address
address_is_ddr	false	Address transfer method (SDR)
address_size	3	Address size
additional_value	0	Option data
additional_size	0	Option data size
dummy_cycles	0	Number of dummy cycles
transfer_buffer	NULL	Data buffer This parameter is updated to the address of the buffer that stores the write data to the memory when communicating with Serial Flash memory
transfer_is_ddr	false	Data transfer method (SDR)
transfer_size	0	Data size This value is updated when communicating with the Serial Flash memory
slch_value	0	Clock Delay SSLDR register SCKDL bit value
clsh_value	0	SSL Negation Delay CHSH: 5ns, CLSH=5ns - 1/SPI frequency = -10ns SSLDR register SLNDL bit value
shsl_value	6	Next Access Delay SSLDR register SPNDL bit value

Table 5.46 Operation table: "4 Kbytes Block Erase" (op_erase_4k)

Member	Setting value	Description
form	SPI_FORM_1_1_1	Command bit width: 1bit Address bit width: 1bit Data bit width: 1bit
op	0x20	Command code "Block Erase (4kbytes)"
op_size	1	Command size
op_is_ddr	false	Command transfer method (SDR)
address	0	Address
address_is_ddr	false	Address transfer method (SDR)
address_size	3	Address size
additional_value	0	Option data
additional_size	0	Option data size
dummy_cycles	0	Number of dummy cycles
transfer_buffer	NULL	Data buffer
transfer_is_ddr	false	Data transfer method (SDR)
transfer_size	0	Data size
force_idle_level_mask	0x08	Keep IO3/HOLD pin to High
force_idle_level_value	0x08	Keep IO3/HOLD pin to High
slch_value	0	Clock Delay SSLDR register SCKDL bit value
clsh_value	0	SSL Negation Delay CHSH: 5ns, CLSH=5ns - 1/SPI frequency = -10ns SSLDR register SLNDL bit value
shsl_value	6	Next Access Delay SSLDR register SPNDL bit value

Table 5.47 Operation table: "32 Kbytes Block Erase" (op_erase_32k)

Member	Setting value	Description
form	SPI_FORM_1_1_1	Command bit width: 1bit Address bit width: 1bit Data bit width: 1bit
op	0x52	Command code "Block Erase (32kbytes)"
op_size	1	Command size
op_is_ddr	false	Command transfer method (SDR)
address	0	Address
address_is_ddr	false	Address transfer method (SDR)
address_size	3	Address size
additional_value	0	Option data
additional_size	0	Option data size
dummy_cycles	0	Number of dummy cycles
transfer_buffer	NULL	Data buffer
transfer_is_ddr	false	Data transfer method (SDR)
transfer_size	0	Data size
force_idle_level_mask	0x08	Keep IO3/HOLD pin to High
force_idle_level_value	0x08	Keep IO3/HOLD pin to High
slch_value	0	Clock Delay SSLDR register SCKDL bit value
clsh_value	0	SSL Negation Delay CHSH: 5ns, CLSH=5ns - 1/SPI frequency = -10ns SSLDR register SLNDL bit value
shsl_value	6	Next Access Delay SSLDR register SPNDL bit value

Table 5.48 Operation table: "64 Kbytes Block Erase" (op_erase_64k)

Member	Setting value	Description
form	SPI_FORM_1_1_1	Command bit width: 1bit Address bit width: 1bit Data bit width: 1bit
op	0xD8	Command code " Block Erase (64kbytes)"
op_size	1	Command size
op_is_ddr	false	Command transfer method (SDR)
address	0	Address
address_is_ddr	false	Address transfer method (SDR)
address_size	3	Address size
additional_value	0	Option data
additional_size	0	Option data size
dummy_cycles	0	Number of dummy cycles
transfer_buffer	NULL	Data buffer
transfer_is_ddr	false	Data transfer method (SDR)
transfer_size	0	Data size
force_idle_level_mask	0x08	Keep IO3/HOLD pin to High
force_idle_level_value	0x08	Keep IO3/HOLD pin to High
slch_value	0	Clock Delay SSLDR register SCKDL bit value
clsh_value	0	SSL Negation Delay CHSH: 5ns, CLSH=5ns - 1/SPI frequency = -10ns SSLDR register SLNDL bit value
shsl_value	6	Next Access Delay SSLDR register SPNDL bit value

Table 5.49 PLL4 operation setting parameters (cpg_pll4_setdata)

Member	Setting value	Description
clk1_dat.reg	CPG_PLL4_CLK1	CPG_PLL4_CLK1 register
clk1_dat.val	0xFAE13203	PLL4 = 1600MHz setting Please refer to chapter "PLLn (SSCG) Output Clock Setting Register 1 (CPG_SAMPLLn_CLK2) (n = 1, 4, or 6)" of A3UL Group User's Manual: Hardware for details
clk1_dat.reg	CPG_PLL4_CLK2	CPG_PLL4_CLK2 register
clk1_dat.val	0x00081000	PLL4 = 1600MHz setting Please refer to chapter "PLLn (SSCG) Output Clock Setting Register 2 (CPG_SAMPLLn_CLK2) (n = 1, 4, or 6)" of A3UL Group User's Manual: Hardware for details
stby_dat.reg	CPG_PLL4_STBY	CPG_PLL4_STBY register
stby_dat.val	0x00010001	PLL4 active setting

Table 5.50 PLL6 operation setting parameters (cpg_pll6_setdata)

Member	Setting value	Description
clk1_dat.reg	CPG_PLL6_CLK1	CPG_PLL6_CLK1 register
clk1_dat.val	0x00003Eb3	PLL4 = 500MHz setting Please refer to chapter "PLLn (SSCG) Output Clock Setting Register 1 (CPG_SAMPLLn_CLK2) (n = 1, 4, or 6)" of A3UL Group User's Manual: Hardware for details
clk1_dat.reg	CPG_PLL6_CLK2	CPG_PLL6_CLK2 register
clk1_dat.val	0x00082D02	PLL4 = 500MHz setting Please refer to chapter "PLLn (SSCG) Output Clock Setting Register 2 (CPG_SAMPLLn_CLK2) (n = 1, 4, or 6)" of A3UL Group User's Manual: Hardware for details
stby_dat.reg	CPG_PLL6_STBY	CPG_PLL6_STBY register
stby_dat.val	0x00010001	PLL6 active setting

Table 5.51 CPG setting table for modules used for IPL initialization (early_setup_tbl)

Member	Setting value	Description
early_setup_tbl[0].reg	CPG_CLKON_SYC	CPG_CLKON_SYC register
early_setup_tbl[0].mon	CPG_CLKMON_SYC	CPG_CLKMON_SYC register
early_setup_tbl[0].val	0x00010001	Clock supply setting
early_setup_tbl[0].type	CPG_T_CLK	Set the clock control register
early_setup_tbl[1].reg	CPG_RST_SYC	CPG_RST_SYC register
early_setup_tbl[1].mon	CPG_RSTMON_SYC	CPG_RSTMON_SYC register
early_setup_tbl[1].val	0x00010001	Reset release setting
early_setup_tbl[1].type	CPG_T_RST	Set the release control register

Table 5.52 CPG setting table for clock supplying module (cpg_clk_on_tbl) (1/3)

Member	Setting value	Description
cpg_clk_on_tbl[0].reg	CPG_CLKON_CM33	CPG_CLKON_CM33 register
cpg_clk_on_tbl[0].mon	CPG_CLKMON_CM33	CPG_CLKMON_CM33 register
cpg_clk_on_tbl[0].val	0x00030000	Clock supply setting
cpg_clk_on_tbl[0].type	CPG_T_CLK	Set the clock control register
cpg_clk_on_tbl[1].reg	CPG_CLKON_MHU	CPG_CLKON_MHU register
cpg_clk_on_tbl[1].mon	CPG_CLKMON_MHU	CPG_CLKMON_MHU register
cpg_clk_on_tbl[1].val	0x00010000	Clock supply setting
cpg_clk_on_tbl[1].type	CPG_T_CLK	Set the clock control register
cpg_clk_on_tbl[2].reg	CPG_CLKON_DMAC_REG	CPG_CLKON_DMAC_REG register
cpg_clk_on_tbl[2].mon	CPG_CLKMON_DMAC_REG	CPG_CLKMON_DMAC_REG register
cpg_clk_on_tbl[2].val	0x00030003	Clock supply setting
cpg_clk_on_tbl[2].type	CPG_T_CLK	Set the clock control register
cpg_clk_on_tbl[-3].reg	CPG_CLKON_OSTM	CPG_CLKON_OSTM register
cpg_clk_on_tbl[3].mon	CPG_CLKMON_OSTM	CPG_CLKMON_OSTM register
cpg_clk_on_tbl[3].val	0x00060000	Clock supply setting
cpg_clk_on_tbl[3].type	CPG_T_CLK	Set the clock control register
cpg_clk_on_tbl[4].reg	CPG_CLKON_MTU	CPG_CLKON_MTU register
cpg_clk_on_tbl[4].mon	CPG_CLKMON_MTU	CPG_CLKMON_MTU register
cpg_clk_on_tbl[4].val	0x00010000	Clock supply setting
cpg_clk_on_tbl[4].type	CPG_T_CLK	Set the clock control register
cpg_clk_on_tbl[5].reg	CPG_CLKON_POE3	CPG_CLKON_POE3 register
cpg_clk_on_tbl[5].mon	CPG_CLKMON_POE3	CPG_CLKMON_POE3 register
cpg_clk_on_tbl[5].val	0x00010000	Clock supply setting
cpg_clk_on_tbl[5].type	CPG_T_CLK	Set the clock control register
cpg_clk_on_tbl[6].reg	CPG_CLKON_WDT	CPG_CLKON_WDT register
cpg_clk_on_tbl[6].mon	CPG_CLKMON_WDT	CPG_CLKMON_WDT register
cpg_clk_on_tbl[6].val	0x00030000	Clock supply setting
cpg_clk_on_tbl[6].type	CPG_T_CLK	Set the clock control register
cpg_clk_on_tbl[7].reg	CPG_CLKON_DDR	CPG_CLKON_DDR register
cpg_clk_on_tbl[7].mon	CPG_CLKMON_DDR	CPG_CLKMON_DDR register
cpg_clk_on_tbl[7].val	0x00030000	Clock supply setting
cpg_clk_on_tbl[7].type	CPG_T_CLK	Set the clock control register
cpg_clk_on_tbl[8].reg	CPG_CLKON_SDHI	CPG_CLKON_SDHI register
cpg_clk_on_tbl[8].mon	CPG_CLKMON_SDHI	CPG_CLKMON_SDHI register
cpg_clk_on_tbl[8].val	0x00FF00FF	Clock supply setting
cpg_clk_on_tbl[8].type	CPG_T_CLK	Set the clock control register
cpg_clk_on_tbl[9].reg	CPG_CLKON_ISU	CPG_CLKON_ISU register
cpg_clk_on_tbl[9].mon	CPG_CLKMON_ISU	CPG_CLKMON_ISU register
cpg_clk_on_tbl[9].val	0x00030000	Clock supply setting
cpg_clk_on_tbl[9].type	CPG_T_CLK	Set the clock control register
cpg_clk_on_tbl[10].reg	CPG_CLKON_CRU	CPG_CLKON_CRU register
cpg_clk_on_tbl[10].mon	CPG_CLKMON_CRU	CPG_CLKMON_CRU register
cpg_clk_on_tbl[10].val	0x001F0000	Clock supply setting
cpg_clk_on_tbl[10].type	CPG_T_CLK	Set the clock control register

Table 5.53 CPG setting table for clock supplying module (cpg_clk_on_tbl) (2/3)

Member	Setting value	Description
cpg_clk_on_tbl[11].reg	CPG_CLKON_LCDC	CPG_CLKON_LCDC register
cpg_clk_on_tbl[11].mon	CPG_CLKMON_LCDC	CPG_CLKMON_LCDC register
cpg_clk_on_tbl[11].val	0x00030000	Clock supply setting
cpg_clk_on_tbl[11].type	CPG_T_CLK	Set the clock control register
cpg_clk_on_tbl[12].reg	CPG_CLKON_SSI	CPG_CLKON_SSI register
cpg_clk_on_tbl[12].mon	CPG_CLKMON_SSI	CPG_CLKMON_SSI register
cpg_clk_on_tbl[12].val	0x00FF0000	Clock supply setting
cpg_clk_on_tbl[12].type	CPG_T_CLK	Set the clock control register
cpg_clk_on_tbl[13].reg	CPG_CLKON_SRC	CPG_CLKON_SRC register
cpg_clk_on_tbl[13].mon	CPG_CLKMON_SRC	CPG_CLKMON_SRC register
cpg_clk_on_tbl[13].val	0x00010000	Clock supply setting
cpg_clk_on_tbl[13].type	CPG_T_CLK	Set the clock control register
cpg_clk_on_tbl[14].reg	CPG_CLKON_USB	CPG_CLKON_USB register
cpg_clk_on_tbl[14].mon	CPG_CLKMON_USB	CPG_CLKMON_USB register
cpg_clk_on_tbl[14].val	0x000F0000	Clock supply setting
cpg_clk_on_tbl[14].type	CPG_T_CLK	Set the clock control register
cpg_clk_on_tbl[15].reg	CPG_CLKON_ETH	CPG_CLKON_ETH register
cpg_clk_on_tbl[15].mon	CPG_CLKMON_ETH	CPG_CLKMON_ETH register
cpg_clk_on_tbl[15].val	0x00030000	Clock supply setting
cpg_clk_on_tbl[15].type	CPG_T_CLK	Set the clock control register
cpg_clk_on_tbl[16].reg	CPG_CLKON_I2C	CPG_CLKON_I2C register
cpg_clk_on_tbl[16].mon	CPG_CLKMON_I2C	CPG_CLKMON_I2C register
cpg_clk_on_tbl[16].val	0x000F0000	Clock supply setting
cpg_clk_on_tbl[16].type	CPG_T_CLK	Set the clock control register
cpg_clk_on_tbl[17].reg	CPG_CLKON_SCIF	CPG_CLKON_SCIF register
cpg_clk_on_tbl[17].mon	CPG_CLKMON_SCIF	CPG_CLKMON_SCIF register
cpg_clk_on_tbl[17].val	0x001F0001	Clock supply setting
cpg_clk_on_tbl[17].type	CPG_T_CLK	Set the clock control register
cpg_clk_on_tbl[18].reg	CPG_CLKON_SSI	CPG_CLKON_SSI register
cpg_clk_on_tbl[18].mon	CPG_CLKMON_SSI	CPG_CLKMON_SSI register
cpg_clk_on_tbl[18].val	0x00030000	Clock supply setting
cpg_clk_on_tbl[18].type	CPG_T_CLK	Set the clock control register
cpg_clk_on_tbl[19].reg	CPG_CLKON_IRDA	CPG_CLKON_IRDA register
cpg_clk_on_tbl[19].mon	CPG_CLKMON_IRDA	CPG_CLKMON_IRDA register
cpg_clk_on_tbl[19].val	0x00010000	Clock supply setting
cpg_clk_on_tbl[19].type	CPG_T_CLK	Set the clock control register
cpg_clk_on_tbl[20].reg	CPG_CLKON_RSPI	CPG_CLKON_RSPI register
cpg_clk_on_tbl[20].mon	CPG_CLKMON_RSPI	CPG_CLKMON_RSPI register
cpg_clk_on_tbl[20].val	0x00070000	Clock supply setting
cpg_clk_on_tbl[20].type	CPG_T_CLK	Set the clock control register
cpg_clk_on_tbl[21].reg	CPG_CLKON_CANFD	CPG_CLKON_CANFD register
cpg_clk_on_tbl[21].mon	CPG_CLKMON_CANFD	CPG_CLKMON_CANFD register
cpg_clk_on_tbl[21].val	0x00010000	Clock supply setting
cpg_clk_on_tbl[21].type	CPG_T_CLK	Set the clock control register
cpg_clk_on_tbl[22].reg	CPG_CLKON_GPIO	CPG_CLKON_GPIO register
cpg_clk_on_tbl[22].mon	CPG_CLKMON_GPIO	CPG_CLKMON_GPIO register
cpg_clk_on_tbl[22].val	0x00010001	Clock supply setting
cpg_clk_on_tbl[22].type	CPG_T_CLK	Set the clock control register

Table 5.54 CPG setting table for clock supplying module (cpg_clk_on_tbl) (3/3)

Member	Setting value	Description
cpg_clk_on_tbl[23].reg	CPG_CLKON_ADC	CPG_CLKON_ADC register
cpg_clk_on_tbl[23].mon	CPG_CLKMON_ADC	CPG_CLKMON_ADC register
cpg_clk_on_tbl[23].val	0x00030000	Clock supply setting
cpg_clk_on_tbl[23].type	CPG_T_CLK	Set the clock control register
cpg_clk_on_tbl[24].reg	CPG_CLKON_TSU	CPG_CLKON_TSU register
cpg_clk_on_tbl[24].mon	CPG_CLKMON_TSU	CPG_CLKMON_TSU register
cpg_clk_on_tbl[24].val	0x00010000	Clock supply setting
cpg_clk_on_tbl[24].type	CPG_T_CLK	Set the clock control register

Table 5.55 CPG setting table for modules to be released from reset (cpg_reset_tbl) (1/3)

Member	Setting value	Description
cpg_reset_tbl[0].reg	CPG_RSTON_CM33	CPG_RSTON_CM33 register
cpg_reset_tbl[0].mon	CPG_RSTMON_CM33	CPG_RSTMON_CM33 register
cpg_reset_tbl[0].val	0x00070000	Reset release setting
cpg_reset_tbl[0].type	CPG_T_RST	Set the release control register
cpg_reset_tbl[1].reg	CPG_RSTON_MHU	CPG_RSTON_MHU register
cpg_reset_tbl[1].mon	CPG_RSTMON_MHU	CPG_RSTMON_MHU register
cpg_reset_tbl[1].val	0x00010000	Reset release setting
cpg_reset_tbl[1].type	CPG_T_RST	Set the release control register
cpg_reset_tbl[2].reg	CPG_RSTON_DMAC_REG	CPG_RSTON_DMAC_REG register
cpg_reset_tbl[2].mon	CPG_RSTMON_DMAC_REG	CPG_RSTMON_DMAC_REG register
cpg_reset_tbl[2].val	0x00030003	Reset release setting
cpg_reset_tbl[2].type	CPG_T_RST	Set the release control register
cpg_reset_tbl[3].reg	CPG_RSTON_OSTM	CPG_RSTON_OSTM register
cpg_reset_tbl[3].mon	CPG_RSTMON_OSTM	CPG_RSTMON_OSTM register
cpg_reset_tbl[3].val	0x00060000	Reset release setting
cpg_reset_tbl[3].type	CPG_T_RST	Set the release control register
cpg_reset_tbl[4].reg	CPG_RSTON_MTU	CPG_RSTON_MTU register
cpg_reset_tbl[4].mon	CPG_RSTMON_MTU	CPG_RSTMON_MTU register
cpg_reset_tbl[4].val	0x00010000	Reset release setting
cpg_reset_tbl[4].type	CPG_T_RST	Set the release control register
cpg_reset_tbl[5].reg	CPG_RSTON_POE3	CPG_RSTON_POE3 register
cpg_reset_tbl[5].mon	CPG_RSTMON_POE3	CPG_RSTMON_POE3 register
cpg_reset_tbl[5].val	0x00010000	Reset release setting
cpg_reset_tbl[5].type	CPG_T_RST	Set the release control register
cpg_reset_tbl[6].reg	CPG_RSTON_WDT	CPG_RSTON_WDT register
cpg_reset_tbl[6].mon	CPG_RSTMON_WDT	CPG_RSTMON_WDT register
cpg_reset_tbl[6].val	0x00030000	Reset release setting
cpg_reset_tbl[6].type	CPG_T_RST	Set the release control register
cpg_reset_tbl[7].reg	CPG_RSTON_DDR	CPG_RSTON_DDR register
cpg_reset_tbl[7].mon	CPG_RSTMON_DDR	CPG_RSTMON_DDR register
cpg_reset_tbl[7].val	0x007F0000	Reset release setting
cpg_reset_tbl[7].type	CPG_T_RST	Set the release control register
cpg_reset_tbl[8].reg	CPG_RSTON_SDHI	CPG_RSTON_SDHI register
cpg_reset_tbl[8].mon	CPG_RSTMON_SDHI	CPG_RSTMON_SDHI register
cpg_reset_tbl[8].val	0x00030003	Reset release setting
cpg_reset_tbl[8].type	CPG_T_RST	Set the release control register
cpg_reset_tbl[9].reg	CPG_RSTON_ISU	CPG_RSTON_ISU register
cpg_reset_tbl[9].mon	CPG_RSTMON_ISU	CPG_RSTMON_ISU register
cpg_reset_tbl[9].val	0x00030000	Reset release setting
cpg_reset_tbl[9].type	CPG_T_RST	Set the release control register
cpg_reset_tbl[10].reg	CPG_RSTON_CRU	CPG_RSTON_CRU register
cpg_reset_tbl[10].mon	CPG_RSTMON_CRU	CPG_RSTMON_CRU register
cpg_reset_tbl[10].val	0x00070000	Reset release setting
cpg_reset_tbl[10].type	CPG_T_RST	Set the release control register

Table 5.56 CPG setting table for modules to be released from reset (cpg_reset_tbl) (2/3)

Member	Setting value	Description
cpg_reset_tbl[11].reg	CPG_RSTON_LCDC	CPG_RSTON_LCDC register
cpg_reset_tbl[11].mon	CPG_RSTMON_LCDC	CPG_RSTMON_LCDC register
cpg_reset_tbl[11].val	0x00010000	Reset release setting
cpg_reset_tbl[11].type	CPG_T_RST	Set the release control register
cpg_reset_tbl[12].reg	CPG_RSTON_SSIF	CPG_RSTON_SSIF register
cpg_reset_tbl[12].mon	CPG_RSTMON_SSIF	CPG_RSTMON_SSIF register
cpg_reset_tbl[12].val	0x000F0000	Reset release setting
cpg_reset_tbl[12].type	CPG_T_RST	Set the release control register
cpg_reset_tbl[13].reg	CPG_RSTON_SRC	CPG_RSTON_SRC register
cpg_reset_tbl[13].mon	CPG_RSTMON_SRC	CPG_RSTMON_SRC register
cpg_reset_tbl[13].val	0x00010000	Reset release setting
cpg_reset_tbl[13].type	CPG_T_RST	Set the release control register
cpg_reset_tbl[14].reg	CPG_RSTON_USB	CPG_RSTON_USB register
cpg_reset_tbl[14].mon	CPG_RSTMON_USB	CPG_RSTMON_USB register
cpg_reset_tbl[14].val	0x000F0000	Reset release setting
cpg_reset_tbl[14].type	CPG_T_RST	Set the release control register
cpg_reset_tbl[15].reg	CPG_RSTON_ETH	CPG_RSTON_ETH register
cpg_reset_tbl[15].mon	CPG_RSTMON_ETH	CPG_RSTMON_ETH register
cpg_reset_tbl[15].val	0x00030000	Reset release setting
cpg_reset_tbl[15].type	CPG_T_RST	Set the release control register
cpg_reset_tbl[16].reg	CPG_RSTON_I2C	CPG_RSTON_I2C register
cpg_reset_tbl[16].mon	CPG_RSTMON_I2C	CPG_RSTMON_I2C register
cpg_reset_tbl[16].val	0x000F0000	Reset release setting
cpg_reset_tbl[16].type	CPG_T_RST	Set the release control register
cpg_reset_tbl[17].reg	CPG_RSTON_SCIF	CPG_RSTON_SCIF register
cpg_reset_tbl[17].mon	CPG_RSTMON_SCIF	CPG_RSTMON_SCIF register
cpg_reset_tbl[17].val	0x001F0001	Reset release setting
cpg_reset_tbl[17].type	CPG_T_RST	Set the release control register
cpg_reset_tbl[18].reg	CPG_RSTON_SCI	CPG_RSTON_SCI register
cpg_reset_tbl[18].mon	CPG_RSTMON_SCI	CPG_RSTMON_SCI register
cpg_reset_tbl[18].val	0x00030000	CPG_RSTON_SCI register
cpg_reset_tbl[18].type	CPG_T_RST	CPG_RSTMON_SCI register
cpg_reset_tbl[19].reg	CPG_RSTON_IRDA	CPG_RSTON_IRDA register
cpg_reset_tbl[19].mon	CPG_RSTMON_IRDA	CPG_RSTMON_IRDA register
cpg_reset_tbl[19].val	0x00010000	Reset release setting
cpg_reset_tbl[19].type	CPG_T_RST	Set the release control register
cpg_reset_tbl[20].reg	CPG_RSTON_RSPI	CPG_RSTON_RSPI register
cpg_reset_tbl[20].mon	CPG_RSTMON_RSPI	CPG_RSTMON_RSPI register
cpg_reset_tbl[20].val	0x00070000	Reset release setting
cpg_reset_tbl[20].type	CPG_T_RST	Set the release control register
cpg_reset_tbl[21].reg	CPG_RSTON_CANFD	CPG_RSTON_CANFD register
cpg_reset_tbl[21].mon	CPG_RSTMON_CANFD	CPG_RSTMON_CANFD register
cpg_reset_tbl[21].val	0x00030000	Reset release setting
cpg_reset_tbl[21].type	CPG_T_RST	Set the release control register
cpg_reset_tbl[22].reg	CPG_RSTON_GPIO	CPG_RSTON_GPIO register
cpg_reset_tbl[22].mon	CPG_RSTMON_GPIO	CPG_RSTMON_GPIO register
cpg_reset_tbl[22].val	0x00070007	Reset release setting
cpg_reset_tbl[22].type	CPG_T_RST	Set the release control register

Table 5.57 CPG setting table for modules to be released from reset (cpg_reset_tbl) (3/3)

Member	Setting value	Description
cpg_reset_tbl[23].reg	CPG_RSTON_ADC	CPG_RSTON_ADC register
cpg_reset_tbl[23].mon	CPG_RSTMON_ADC	CPG_RSTMON_ADC register
cpg_reset_tbl[23].val	0x00030000	Reset release setting
cpg_reset_tbl[23].type	CPG_T_RST	Set the release control register
cpg_reset_tbl[24].reg	CPG_RSTON_TSU	CPG_RSTON_TSU register
cpg_reset_tbl[24].mon	CPG_RSTMON_TSU	CPG_RSTMON_TSU register
cpg_reset_tbl[24].val	0x00030000	Reset release setting
cpg_reset_tbl[24].type	CPG_T_RST	Set the release control register

Table 5.58 Clock selector register table that stops clock supply (cpg_static_select_tbl)

Member	Setting value	Description
cpg_static_select_tbl[0].reg	CPG_PL3A_DDIV	CPG_PL3A_DDIV register
cpg_static_select_tbl[0].val	0x01000100	PLL3 clock divide rate setting
cpg_static_select_tbl[1].reg	CPG_PL3_SSEL	CPG_PL3_SSEL register
cpg_static_select_tbl[1].val	0x01000000	PLL3 source clock setting

Table 5.59 Clock selector register table that continues clock supply (cpg_dynamic_select_tbl)

Member	Setting value	Description
cpg_dynamic_select_tbl[0].reg	CPG_PL4_DSEL	CPG_PL4_DSEL register
cpg_dynamic_select_tbl[0].val	0x00010001	PLL4 clock divide rate setting
cpg_dynamic_select_tbl[1].reg	CPG_PL2SDHI_DSEL	CPG_PL2SDHI_DSEL register
cpg_dynamic_select_tbl[1].val	0x00110022	PLL2 source clock setting

Table 5.60 Pin setting table for modules used in boot processing (pfc_mux_reg_tbl)

Member	Setting value	Description
pfc_mux_reg_tbl[0].pmc.flag	PFC_ON	PFC enable flag
pfc_mux_reg_tbl[0].pmc.reg	PFC_PMC10	PFC_PMC10 register
pfc_mux_reg_tbl[0].pmc.val	0x0F	Register setting value
pfc_mux_reg_tbl[0].pfc.flag	PFC_ON	PFC enable flag
pfc_mux_reg_tbl[0].pfc.reg	PFC_PFC10	PFC_PFC10 register
pfc_mux_reg_tbl[0].pfc.val	0x00001111	Register setting value
pfc_mux_reg_tbl[0].iolh.flag	PFC_OFF	PFC disable flag
pfc_mux_reg_tbl[0].iolh.reg	PFC_IOLH10	PFC_IOLH10 register
pfc_mux_reg_tbl[0].iolh.val	0x0000000001010101	Register setting value
pfc_mux_reg_tbl[0].pupd.flag	PFC_OFF	PFC disable flag
pfc_mux_reg_tbl[0].pupd.reg	PFC_PUPD10	PFC_PUPD10 register
pfc_mux_reg_tbl[0].pupd.val	0x0000000000000000	Register setting value
pfc_mux_reg_tbl[0].sr.flag	PFC_OFF	PFC disable flag
pfc_mux_reg_tbl[0].sr.reg	PFC_SR10	PFC_SR10 register
pfc_mux_reg_tbl[0].sr.val	0x0000000001010101	Register setting value
pfc_mux_reg_tbl[0].ien.flag	PFC_OFF	PFC disable flag
pfc_mux_reg_tbl[0].ien.reg	NULL	PFC_IEN register NULL is defined for this member because PFC_IEN10 is not implemented
pfc_mux_reg_tbl[0].ien.val	0	Register setting value
pfc_mux_reg_tbl[1].pmc.flag	PFC_ON	PFC enable flag
pfc_mux_reg_tbl[1].pmc.reg	PFC_PMC16	PFC_PMC16 register
pfc_mux_reg_tbl[1].pmc.val	0x18	Register setting value
pfc_mux_reg_tbl[1].pfc.flag	PFC_ON	PFC enable flag
pfc_mux_reg_tbl[1].pfc.reg	PFC_PFC16	PFC_PFC16 register
pfc_mux_reg_tbl[1].pfc.val	0x00066000	Register setting value
pfc_mux_reg_tbl[1].iolh.flag	PFC_OFF	PFC disable flag
pfc_mux_reg_tbl[1].iolh.reg	PFC_IOLH16	PFC_IOLH16 register
pfc_mux_reg_tbl[1].iolh.val	0x0000000101000000	Register setting value
pfc_mux_reg_tbl[1].pupd.flag	PFC_OFF	PFC disable flag
pfc_mux_reg_tbl[1].pupd.reg	PFC_PUPD16	PFC_PUPD16 register
pfc_mux_reg_tbl[1].pupd.val	0x0000000000000000	Register setting value
pfc_mux_reg_tbl[1].sr.flag	PFC_OFF	PFC disable flag
pfc_mux_reg_tbl[1].sr.reg	PFC_SR16	PFC_SR16 register
pfc_mux_reg_tbl[1].sr.val	0x0000000101000000	Register setting value
pfc_mux_reg_tbl[1].ien.flag	PFC_OFF	PFC disable flag
pfc_mux_reg_tbl[1].ien.reg	NULL	PFC_IEN register NULL is defined for this member because PFC_IEN16 is not implemented
pfc_mux_reg_tbl[1].ien.val	0	Register setting value

Table 5.61 Serial flash memory pin setting table (pfc_qspi_reg_tbl) (1/2)

Member	Setting value	Description
pfc_mux_reg_tbl[0].pmc.flag	PFC_OFF	PFC enable flag
pfc_mux_reg_tbl[0].pmc.reg	NULL	PFC_PMC register NULL is defined for this member because PFC_PMC0A is not implemented
pfc_mux_reg_tbl[0].pmc.val	0	Register setting value
pfc_mux_reg_tbl[0].pfc.flag	PFC_OFF	PFC enable flag
pfc_mux_reg_tbl[0].pfc.reg	NULL	PFC_PFC register NULL is defined for this member because PFC_PFC0A is not implemented
pfc_mux_reg_tbl[0].pfc.val	0	Register setting value
pfc_mux_reg_tbl[0].iolh.flag	PFC_ON	PFC disable flag
pfc_mux_reg_tbl[0].iolh.reg	PFC_IOLH0A	PFC_IOLH0A register
pfc_mux_reg_tbl[0].iolh.val	0x0000010101010101	Register setting value
pfc_mux_reg_tbl[0].pupd.flag	PFC_ON	PFC disable flag
pfc_mux_reg_tbl[0].pupd.reg	PFC_PUPD0A	PFC_PUPD0A register
pfc_mux_reg_tbl[0].pupd.val	0x0000000000000000	Register setting value
pfc_mux_reg_tbl[0].sr.flag	PFC_ON	PFC disable flag
pfc_mux_reg_tbl[0].sr.reg	PFC_SR0A	PFC_SR0A register
pfc_mux_reg_tbl[0].sr.val	0x0000010101010101	Register setting value
pfc_mux_reg_tbl[0].ien.flag	PFC_OFF	PFC disable flag
pfc_mux_reg_tbl[0].ien.reg	NULL	PFC_IEN register NULL is defined for this member because PFC_IEN0A is not implemented
pfc_mux_reg_tbl[0].ien.val	0	Register setting value
pfc_mux_reg_tbl[1].pmc.flag	PFC_OFF	PFC enable flag
pfc_mux_reg_tbl[1].pmc.reg	NULL	PFC_PMC register NULL is defined for this member because PFC_PMC0B is not implemented
pfc_mux_reg_tbl[1].pmc.val	0	Register setting value
pfc_mux_reg_tbl[1].pfc.flag	PFC_OFF	PFC enable flag
pfc_mux_reg_tbl[1].pfc.reg	NULL	PFC_PFC register NULL is defined for this member because PFC_PFC0B is not implemented
pfc_mux_reg_tbl[1].pfc.val	0	Register setting value
pfc_mux_reg_tbl[1].iolh.flag	PFC_ON	PFC disable flag
pfc_mux_reg_tbl[1].iolh.reg	PFC_IOLH0B	PFC_IOLH0B register
pfc_mux_reg_tbl[1].iolh.val	0x0000010101010101	Register setting value
pfc_mux_reg_tbl[1].pupd.flag	PFC_ON	PFC disable flag
pfc_mux_reg_tbl[1].pupd.reg	PFC_PUPD0B	PFC_PUPD0B register
pfc_mux_reg_tbl[1].pupd.val	0x0000000000000000	Register setting value
pfc_mux_reg_tbl[1].sr.flag	PFC_ON	PFC disable flag
pfc_mux_reg_tbl[1].sr.reg	PFC_SR0B	PFC_SR0B register
pfc_mux_reg_tbl[1].sr.val	0x0000010101010101	Register setting value

Table 5.62 Serial flash memory pin setting table (pfc_qspi_reg_tbl) (2/2)

Member	Setting value	Description
pfc_mux_reg_tbl[1].ien.flag	PFC_OFF	PFC disable flag
pfc_mux_reg_tbl[1].ien.reg	NULL	PFC_IEN register NULL is defined for this member because PFC_IEN0B is not implemented
pfc_mux_reg_tbl[1].ien.val	0	Register setting value
pfc_mux_reg_tbl[2].pmc.flag	PFC_OFF	PFC enable flag
pfc_mux_reg_tbl[2].pmc.reg	NULL	PFC_PMC register NULL is defined for this member because PFC_PMC0C is not implemented
pfc_mux_reg_tbl[2].pmc.val	0	Register setting value
pfc_mux_reg_tbl[2].pfc.flag	PFC_OFF	PFC enable flag
pfc_mux_reg_tbl[2].pfc.reg	NULL	PFC_PFC register NULL is defined for this member because PFC_PFC0C is not implemented
pfc_mux_reg_tbl[2].pfc.val	0	Register setting value
pfc_mux_reg_tbl[2].iolh.flag	PFC_ON	PFC disable flag
pfc_mux_reg_tbl[2].iolh.reg	PFC_IOLH0C	PFC_IOLH0C register
pfc_mux_reg_tbl[2].iolh.val	0x0000000000000101	Register setting value
pfc_mux_reg_tbl[2].pupd.flag	PFC_ON	PFC disable flag
pfc_mux_reg_tbl[2].pupd.reg	PFC_PUPD0C	PFC_PUPD0C register
pfc_mux_reg_tbl[2].pupd.val	0x0000000000000000	Register setting value
pfc_mux_reg_tbl[2].sr.flag	PFC_ON	PFC disable flag
pfc_mux_reg_tbl[2].sr.reg	PFC_SR0C	PFC_SR0C register
pfc_mux_reg_tbl[2].sr.val	0x0000000000000000	Register setting value
pfc_mux_reg_tbl[2].ien.flag	PFC_OFF	PFC disable flag
pfc_mux_reg_tbl[2].ien.reg	NULL	PFC_IEN register NULL is defined for this member because PFC_IEN0C is not implemented
pfc_mux_reg_tbl[2].ien.val	0	Register setting value

Table 5.63 MMU setting table (g_mmu_pagetable_array[]) (1/2)

Member	Setting value	Description
g_mmu_pagetable_array[0].vaddress	0x00000000	Virtual address setting
g_mmu_pagetable_array[0].paddess	0x00000000	Physical address setting
g_mmu_pagetable_array[0].size	0x00200000	Virtual memory size
g_mmu_pagetable_array[0].attribute	RZA_MMU_ATTRIBUTE_NORMAL_CACHEABLE	Memory attribute setting: Normal Memory、Cache Enable (Write back)
g_mmu_pagetable_array[1].vaddress	0x00200000	Virtual address setting
g_mmu_pagetable_array[1].paddess	0x00200000	Physical address setting
g_mmu_pagetable_array[1].size	0x0FE00000	Virtual memory size
g_mmu_pagetable_array[1].attribute	RZA_MMU_ATTRIBUTE_ACCESS_FAULT	Memory attribute setting: Access Fault
g_mmu_pagetable_array[2].vaddress	0x10000000	Virtual address setting
g_mmu_pagetable_array[2].paddess	0x10000000	Physical address setting
g_mmu_pagetable_array[2].size	0x10000000	Virtual memory size
g_mmu_pagetable_array[2].attribute	RZA_MMU_ATTRIBUTE_DEVICE	Memory attribute setting: Device Memory
g_mmu_pagetable_array[3].vaddress	0x20000000	Virtual address setting
g_mmu_pagetable_array[3].paddess	0x20000000	Physical address setting
g_mmu_pagetable_array[3].size	0x10000000	Virtual memory size
g_mmu_pagetable_array[3].attribute	RZA_MMU_ATTRIBUTE_NORMAL_CACHEABLE	Memory attribute setting: Normal Memory、Cache Enable (Write back)
g_mmu_pagetable_array[4].vaddress	0x30000000	Virtual address setting
g_mmu_pagetable_array[4].paddess	0x30000000	Physical address setting
g_mmu_pagetable_array[4].size	0x10000000	Virtual memory size
g_mmu_pagetable_array[4].attribute	RZA_MMU_ATTRIBUTE_ACCESS_FAULT	Memory attribute setting: Access Fault
g_mmu_pagetable_array[5].vaddress	0x40000000	Virtual address setting
g_mmu_pagetable_array[5].paddess	0x40000000	Physical address setting
g_mmu_pagetable_array[5].size	0x40000000	Virtual memory size
g_mmu_pagetable_array[5].attribute	RZA_MMU_ATTRIBUTE_NORMAL_CACHEABLE	Memory attribute setting: Normal Memory、Cache Enable (Write back)

Table 5.64 MMU setting table (g_mmu_pagetable_array[]) (2/2)

Member	Setting value	Description
g_mmu_pagetable_array[6].vaddress	0x80000000	Virtual address setting
g_mmu_pagetable_array[6].paddess	0x80000000	Physical address setting
g_mmu_pagetable_array[6].size	0x80000000	Virtual memory size
g_mmu_pagetable_array[6].attribute	RZA_MMU_ATTRIBUTE_ACCESS_FAULT	Memory attribute setting: Access Fault
g_mmu_pagetable_array[7].vaddress	0xC0000000	Virtual address setting
g_mmu_pagetable_array[7].paddess	0xC0000000	Physical address setting
g_mmu_pagetable_array[7].size	0xC0000000	Virtual memory size
g_mmu_pagetable_array[7].attribute	RZA_MMU_ATTRIBUTE_ACCESS_FAULT	Memory attribute setting: Access Fault
g_mmu_pagetable_array[8].vaddress	0xFFFFFFFF	Dummy address
g_mmu_pagetable_array[8].paddess	0xFFFFFFFF	Dummy address
g_mmu_pagetable_array[8].size	0xFFFFFFFF	Dummy size
g_mmu_pagetable_array[8].attribute	RZA_MMU_ATTRIBUTE_CONFIG_END	End of MMU configure table

5.12 Function

This chapter shows the functions implemented in IPL.

This chapter only describes the functions used in the RZ/A3UL platform boot process.

5.12.1 Function List

Table 5.65 - Table 5.68 list the functions used in the RZ/A3UL platform boot process.

Table 5.65 List of IPL control functions

Function name	Description
bl2_el3_early_platform_setup	Initial settings for Renesas platforms
bl2_el3_plat_arch_setup	MMU settings for Renesas platforms
bl2_platform_setup	Memory settings for Renesas platforms
rz_io_setup	Initialize the FSP application image storage destination memory
panic	Jump to panic handler

Table 5.66 List of SPIM controller driver functions

Function name	Description
xspi_setup	Initialize Serial Flash memory
spim_open	Initialize SPIBSC driver
spim_close	Close SPIBSC driver
spim_post_init	Post-processing of SPIBSC driver initialization
spim_exec_op	Execute operation to Serial Flash memory
spim_configure_xip	External Address Space Read Mode setting
spim_start_xip	External Address Space Read Mode start
spim_stop_xip	External Address Space Read Mode finish
spim_run_manual_calibration	Execute manual calibration for Serial Flash memory
spim_enable_auto_calibration	Enable auto calibration for Serial Flash memory
spim_disable_auto_calibration	Disable auto calibration for Serial Flash memory
spim_set_frequency	Sets the maximum operating frequency of the Serial Flash memory
spim_clean_mmap	Clean read cache of Serial Flash memory
spim_inv_mmap	Invalidate read cache of Serial Flash memory
spim_get_mmap_base	Get base address where Serial Flash memory is mapped
spim_get_mmap_size	Get the size of the region where the Serial Flash memory is mapped
spim_get_features	Get the operation format supported by the SPIBSC driver

Table 5.67 List of Serial Flash memory driver functions

Function name	Description
flash_open	Initialize the Serial Flash memory
flash_close	Close setting to the Serial Flash memory
flash_exec_op	Execute operation to Serial Flash memory
flash_enter_xip	External Address Space Read Mode start
flash_exit_xip	External Address Space Read Mode finish
flash_get_info	Get the Serial Flash memory information
flash_read	Data read from the Serial Flash memory
flash_write	Data write to the Serial Flash memory
flash_erase	Data erase of Serial Flash memory
flash_get_write_status	Get write status of the Serial Flash memory
flash_write_enable	Set write enable to Serial Flash memory
flash_read_status_register1	Read lower 8bit of status register of the Serial Flash memory
flash_read_status_register2	Read higher 8bit of status register of the Serial Flash memory
flash_write_status_register2	Write higher 8bit of status register of the Serial Flash memory
flash_set_qe	Set Quad Enable bit of status register of the Serial Flash memory
flash_erase_4k	Erase the Serial Flash memory in units of 4Kbytes
flash_erase_32k	Erase the Serial Flash memory in units of 32Kbytes
flash_erase_64k	Erase the Serial Flash memory in units of 64Kbytes

Table 5.68 List of module control functions

Function name	Description
syc_init	Initialize the Cortex®-A55 built-in Generic Timer
generic_delay_timer_init	Initialize timer management parameters
pfc_setup	Set up pin
pfc_mux_setup	Set up pin of SCIF
pfc_qspi_setup	Set up pin of SPIBSC
cpg_setup	Set up CPG
cpg_ctrl_clkrst	Write processing to the clock control register and reset control register
cpg_selector_on_off	Clock ON/OFF setting for modules whose clocks are managed by the source clock selector
cpg_pll_start_146	Start process of PLL1/PLL4/PLL6
cpg_pll_setup	Set up PLL
cpg_div_sel_setup	Write process to Division Ratio Setting register and Source Clock Setting register
cpg_div_sel_static_setup	Setting of Static Switching Frequency Dividers and Selector
cpg_div_sel_dynamic_setup	Setting of Dynamic Switching Frequency Dividers and Selector
cpg_clk_on_setup	Clock supply setting for each module
cpg_reset_setup	Reset release setting for each module
cpg_active_ddr	DDR PHY clock and reset release settings
cpg_reset_ddr_mc	DDR Memory Controller clock and reset release setting
cpg_early_setup	Clock supply and reset release to modules required for pre-processing of platform boot process
cpg_wdtrst_sel_setup	Watchdog Timer module reset release processing
cpu_cpg_setup	Clock division ratio setting for CPU
cpg_search_spi_clk_table	Search the register setting table corresponding to the clock frequency supplied to the Serial Flash memory
cpg_research_spi_clk_table	Search for clock frequency value supplied to Serial Flash memory
cpg_stop_xspi_clock	Clock stop processing for Serial Flash memory
cpg_start_xspi_clock	Clock supply processing to Serial Flash memory
cpg_set_xspi_clock	Serial flash memory clock frequency setting processing
cpg_get_xspi_clock	Get the clock frequency supplied to the Serial Flash memory
wait_until_32	Processing to wait for the end of clock setting
console_rzg2l_register	Console output setting
console_set_scope	Set enable state for console output
plat_get_bl_image_load_info	Get load information of the FSP Application image
plat_get_next_bl_params	Get parameter information of the FSP Application image
rz_check_fsp_header	Check the Application Header
rz_update_descs	Update descriptor parameters
rz_print_descs	Print descriptor parameters
ddr_setup	Initial setting of DDR SDRAM

5.12.2 Function Specifications

This chapter shows the specification of functions.

5.12.2.1 IPL control functions

The functions related to IPL control are listed below.

bl2_el3_early_platform_setup	
Outline	Perform initial settings for Renesas platform
Declaration	void bl2_el3_early_platform_setup (u_register_t arg1, u_register_t arg2, u_register_t arg3, u_register_t arg4)
Description	Initial settings related to hardware such as clocks, pins, general-purpose timers, console output, etc.
Arguments	arg1 :no use it arg2 :no use it arg3 :no use it arg4 :no use it
Return value	None

bl2_el3_plat_arch_setup	
Outline	Set MMU for Renesas platforms
Declaration	void bl2_el3_plat_arch_setup (void)
Description	Set MMU for Renesas platforms.
Arguments	None
Return value	None

bl2_platform_setup	
Outline	Performs memory settings for Renesas platforms
Declaration	void bl2_platform_setup (void)
Description	Initialize memory for Renesas platform and copy FSP application image.
Arguments	None
Return value	None

rz_io_setup	
Outline	Initialize the FSP application image storage destination memory
Declaration	void rz_io_setup (void)
Description	Initializes the Serial Flash memory where the FSP application image is stored. Additionally, this function checks the boot mode. If the boot mode is set to something other than boot mode 3, the IPL will start an infinite loop and stop the boot process.
Arguments	None
Return value	None

panic	
Outline	Jump to panic handler
Declaration	void panic (void)
Description	When an error occurs, jump to panic handler which stops processing by infinite loop. This function is called when an unrecoverable error occurs.
Arguments	None
Return value	None

5.12.2.2 SPIM controller driver functions

The SPIM control driver functions that control the SPIBSC are shown below.

xspi_setup	
Outline	Initialize the Serial Flash memory
Declaration	void xspi_setup (void)
Description	This function calls the API function corresponding to the Serial Flash memory and initializes the memory.
Arguments	None
Return value	None

spim_open	
Outline	Initialize the SPIBSC driver
Declaration	int spim_open (xspi_ctrl_t * ctrl, xspi_cfg_t const * const cfg)
Description	Initialize the SPIBSC driver.
Arguments	*ctrl : Pointer to the control structure for instance *cfg : Pointer to the configuration structure for instance
Return value	0 : Initialization is complete -1 : Initialization is failed

spim_close	
Outline	Close the SPIBSC driver
Declaration	int spim_close (xspi_ctrl_t * ctrl)
Description	Close the SPIBSC driver.
Arguments	*ctrl : Pointer to the control structure for instance
Return value	0 : Close process is complete -1 : Close process is failed

spim_post_init	
Outline	Perform post-processing of SPIBSC driver initialization
Declaration	void spim_post_init (xspi_ctrl_t * ctrl)
Description	Perform post-processing of SPIBSC driver initialization. Processing in this function is not implemented in this version.
Arguments	*ctrl : Pointer to the control structure for instance
Return value	0 : This value is always returned

spim_exec_op	
Outline	Issue the operation to Serial Flash memory
Declaration	int spim_exec_op (xspi_ctrl_t * const ctrl, xspi_op_t const * const op, bool is_write)
Description	Issue the operation to Serial Flash memory.
Arguments	*ctrl : Pointer to the control structure for instance *op : Pointer to xSPI interface operation structure is_write : Specifies the transmission/reception direction of the operation(0=read、1=write)
Return value	0 : Issue the operation is complete -1 : Issue the operation is failed

spim_configure_xip	
Outline	Set the External Address Space Read Mode
Declaration	int spim_configure_xip (xspi_ctrl_t * const ctrl, xspi_op_t const * const rop, xspi_op_t const * const wop)
Description	Set the External Address Space Read Mode
Arguments	*ctrl : Pointer to the control structure for instance *rop : Pointer to operation structure for read *wop : Pointer to operation structure for write
Return value	0 : Setting is complete -1 : Setting is failed

spim_start_xip	
Outline	Start the External Address Space Read Mode
Declaration	int spim_start_xip (xspi_ctrl_t * const ctrl)
Description	Start the External Address Space Read Mode.
Arguments	*ctrl : Pointer to the control structure for instance
Return value	0 : This value is always returned

spim_stop_xip	
Outline	Stop the External Address Space Read Mode
Declaration	int spim_stop_xip (xspi_ctrl_t * const ctrl)
Description	Stop the External Address Space Read Mode.
Arguments	*ctrl : Pointer to the control structure for instance
Return value	0 : This value is always returned

spim_run_manual_calibration	
Outline	Execute calibration for the Serial Flash memory
Declaration	int spim_run_manual_calibration (xspi_ctrl_t * const ctrl)
Description	Execute Calibration for the Serial Flash memory.
Arguments	*ctrl : Pointer to the control structure for instance
Return value	0 : Calibration is complete -1 : Calibration is failed

spim_enable_auto_calibration	
Outline	Enable auto calibration for Serial Flash memory
Declaration	int spim_enable_auto_calibration (xspi_ctrl_t * const ctrl)
Description	Enable auto calibration for Serial Flash memory. Processing in this function is not implemented in this version.
Arguments	*ctrl : Pointer to the control structure for instance
Return value	-1 : This value is always returned

spim_disable_auto_calibration	
Outline	Disable auto calibration for Serial Flash memory
Declaration	int spim_disable_auto_calibration (xspi_ctrl_t * const ctrl)
Description	Disable auto calibration for Serial Flash memory. Processing in this function is not implemented in this version.
Arguments	*ctrl : Pointer to the control structure for instance
Return value	-1 : This value is always returned

spim_set_frequency	
Outline	Sets the maximum operating frequency of the Serial Flash memory
Declaration	int spim_set_frequency (xspi_ctrl_t * const ctrl, int frequency_hz)
Description	Sets the maximum operating frequency of the Serial Flash memory.
Arguments	*ctrl : Pointer to the control structure for instance frequency_hz : Maximum operating frequency of the Serial Flash memory
Return value	0 : This value is always returned

spim_clean_mmap	
Outline	Clean read cache of the Serial Flash memory
Declaration	int spim_clean_mmap (xspi_ctrl_t * const ctrl)
Description	Clean read cache of the Serial Flash memory. Processing in this function is not implemented in this version.
Arguments	*ctrl : Pointer to the control structure for instance
Return value	0 : This value is always returned

spim_inv_mmap	
Outline	Invalidate read cache of the Serial Flash memory
Declaration	int spim_inv_mmap (xspi_ctrl_t * const ctrl)
Description	Invalidate read cache of the Serial Flash memory.
Arguments	*ctrl : Pointer to the control structure for instance
Return value	0 : This value is always returned

spim_get_mmap_base	
Outline	Get the base address where the Serial Flash memory is mapped
Declaration	uintptr_t spim_get_mmap_base (xspi_ctrl_t * const ctrl)
Description	Get the base address to which the Serial Flash memory is mapped.
Arguments	*ctrl : Pointer to the control structure for instance
Return value	Positive number: Base address where the Serial Flash memory is mapped

spim_get_mmap_size	
Outline	Get the size of the area where the Serial Flash memory is mapped
Declaration	uintptr_t spim_get_mmap_size (xspi_ctrl_t * const ctrl)
Description	Get the size of the area where the Serial Flash memory is mapped.
Arguments	*ctrl : Pointer to the control structure for instance
Return value	Positive number: the size of the area where the Serial Flash memory is mapped

spim_get_features	
Outline	Get the operation format supported by the SPIBSC driver
Declaration	uint32_t spim_get_features (xspi_ctrl_t * const ctrl)
Description	Get the operation format supported by the SPIBSC driver
Arguments	*ctrl : Pointer to the control structure for instance
Return value	Positive number::Returns the OR of the following bit values
	XSPI_FEATURE_XIP_READ : The driver supports read access.
	XSPI_FEATURE_XIP_WRITE : The driver supports write access.
	XSPI_FEATURE_FORM112 : The driver supports 1-1-2 form.
	XSPI_FEATURE_FORM122 : The driver supports 1-2-2 form.
	XSPI_FEATURE_FORM222 : The driver supports 2-2-2 form.
	XSPI_FEATURE_DUAL : The driver supports 1-1-2, 1-2-2, and/or 2-2-2 form(s).
	XSPI_FEATURE_FORM114 : The driver supports 1-1-4 form.
	XSPI_FEATURE_FORM144 : The driver supports 1-4-4 form.
	XSPI_FEATURE_FORM444 : The driver supports 4-4-4 form.
	XSPI_FEATURE_QUAD : The driver supports 1-1-4, 1-4-4, and/or 4-4-4 form(s).
	XSPI_FEATURE_FORM118 : The driver supports 1-1-8 form.
	XSPI_FEATURE_FORM188 : The driver supports 1-8-8 form.
	XSPI_FEATURE_FORM888 : The driver supports 8-8-8 form.
	XSPI_FEATURE_OCTAL : The driver supports 1-1-8, 1-8-8, and/or 8-8-8 form(s).
	XSPI_FEATURE_DDROP : The driver supports DDR for op code.
	XSPI_FEATURE_DDR : The driver supports DDR for address and/or data.
	XSPI_FEATURE_OCTARAM : Octa RAM addressing (RAS/CAS) supported.

5.12.2.3 Serial Flash Memory driver functions

This chapter shows the Serial Flash memory driver functions for controlling the Serial Flash memory.

flash_open	
Outline	Initialize the Serial Flash memory
Declaration	int flash_open (xspidevice_ctrl_t * ctrl, xspidevice_cfg_t const * cfg)
Description	Initialize the Serial Flash memory.
Arguments	*ctrl : Pointer to xSPI device control structure
	*cfg : Pointer to xSPI device configure structure
Return value	0 : Initialization is complete
	-1 : Initialization is failed

flash_close	
Outline	Close the Serial Flash memory
Declaration	int flash_close (xspidevice_ctrl_t * ctrl)
Description	Close the Serial Flash memory.
Arguments	*ctrl : Pointer to xSPI device control structure
Return value	0 : Close process is complete
	-1 : Close process is failed

flash_exec_op	
Outline	Execute operation to Serial Flash memory
Declaration	void flash_exec_op (xspidevice_ctrl_t * ctrl, xspi_op_t const * op, bool is_write)
Description	Execute operation to Serial Flash memory.
Arguments	*ctrl :Pointer to xSPI device control structure
	*op : Pointer to xSPI interface operation structure
	is_write :Specifies the transmission/reception direction of the operation(0=read、1=write)
Return value	0 : Execute the operation is complete
	-1 : Execute the operation is failed

flash_enter_xip	
Outline	Set the External Address Space Read Mode to the Serial Flash memory
Declaration	int flash_enter_xip (xspidevice_ctrl_t * ctrl)
Description	Set the External Address Space Read Mode to the Serial Flash memory and start it.
Arguments	*ctrl : Pointer to the control structure for instance
Return value	0 : Setting is complete
	-1 : Setting is failed

flash_exit_xip	
Outline	Finish the External Address Space Read Mode
Declaration	int flash_exit_xip (xspi_ctrl_t * const ctrl)
Description	Finish the External Address Space Read Mode
Arguments	*ctrl : Pointer to the control structure for instance
Return value	0 : This value is always returned

flash_get_info	
Outline	Get the information of the Serial Flash memory
Declaration	int flash_get_info (xspidevice_ctrl_t * ctrl, xspidevice_info_t * info)
Description	Get the information of the Serial Flash memory.
Arguments	*ctrl : Pointer to the control structure for instance * info : Information of the Serial Flash memory
Return value	0 : This value is always returned

flash_read	
Outline	Data read from the Serial Flash memory
Declaration	int flash_read (xspi_ctrl_t * const ctrl, void * buffer, size_t address, size_t length)
Description	Data read from the Serial Flash memory.
Arguments	*ctrl : Pointer to the control structure for instance * buffer : Pointer to buffer to store read data address: Data read source address Specify the offset address in the Serial Flash memory for this argument length : Read data size
Return value	0 : This value is always returned

flash_write	
Outline	Data write to the Serial Flash memory
Declaration	int flash_write (xspi_ctrl_t * const ctrl, void const * buffer, size_t address, size_t length)
Description	Data write to the Serial Flash memory.
Arguments	*ctrl : Pointer to the control structure for instance * buffer : Pointer to buffer where write data is stored address: Data write destination address Specify the offset address in the Serial Flash memory for this argument length : Write data size
Return value	0 : Data write is success -1 : Data write is failed

flash_erase	
Outline	Erase the Serial Flash memory
Declaration	int flash_erase (xspidevice_ctrl_t * ctrl, size_t address, size_t length)
Description	Data erase the Serial Flash memory. Data erase is performed with addresses and sizes in units of 4 Kbytes.
Arguments	*ctrl : Pointer to the control structure for instance address: Start address for data erase Specify the offset address in the Serial Flash memory for this argument. If a value other than a multiple of 4Kbytes is set, the address obtained by aligning the specified address with 4Kbytes will be the start address of the erase area. length : erase size If a value other than 4Kbyte aligned size is set in this argument, it erases the data up to the 4Kbyte aligned address including the specified range.
Return value	0 : Data erase is success -1 : Data erase is failed.

flash_get_write_status	
Outline	Gets the write status of the Serial Flash memory
Declaration	int flash_get_write_status (xspidevice_ctrl_t * ctrl)
Description	Gets the write status of the Serial Flash memory.
Arguments	*ctrl : Pointer to the control structure for instance
Return value	WRITE_STATUS_FAIL : Data write is failed WRITE_STATUS_IN_PROGRESS : Data write in progress WRITE_STATUS_OK : Data write is complete

flash_write_enable	
Outline	Sets Write enable to Serial Flash memory
Declaration	int flash_write_enable (qspiflash_at25_ctrl_t * myctrl)
Description	Set Write enable to Serial Flash memory
Arguments	*myctrl : Pointer to the control structure for instance
Return value	0 : Operation success -1 : Operation Failed

flash_read_status_register1	
Outline	Gets the status register of the Serial Flash memory
Declaration	int flash_read_status_register1 (qspiflash_at25_ctrl_t * myctrl)
Description	Gets the lower bit of the status register of the Serial Flash memory
Arguments	*myctrl : Pointer to the control structure for instance
Return value	Positive number : Operation success, and status register value -1 : Operation Failed

flash_read_status_register2	
Outline	Gets the status register of the Serial Flash memory
Declaration	int flash_read_status_register2 (qspiflash_at25_ctrl_t * myctrl)
Description	Gets the higher bit of the status register of the Serial Flash memory
Arguments	*myctrl : Pointer to the control structure for instance
Return value	Positive number : Operation success, and status register value -1 : Operation Failed

flash_get_write_status	
Outline	Set value to higher 8bit of Status Register
Declaration	int flash_write_status_register2(qspiflash_at25_ctrl_t * myctrl, uint8_t status)
Description	Set value to higher 8bit of Status Register
Arguments	*myctrl : Pointer to the control structure for instance status : Setting value to Status Register
Return value	0 : Operation success -1 : Operation Failed

flash_set_qe	
Outline	Set the QE bit of Status Register
Declaration	int flash_set_qe(qspiflash_at25_ctrl_t * myctrl)
Description	Set the QE bit of Status Register
Arguments	*myctrl : Pointer to the control structure for instance
Return value	0 : Operation success
	-1 : Operation Failed

flash_erase_4k	
Outline	Erase data by 4Kbytes
Declaration	int flash_erase_4k (qspiflash_at25_ctrl_t * myctrl)
Description	Erase data by 4Kbytes
Arguments	*myctrl : Pointer to the control structure for instance
Return value	0 : Operation success
	-1 : Operation Failed

flash_erase_32k	
Outline	Erase data by 32Kbytes
Declaration	int flash_erase_32k (qspiflash_at25_ctrl_t * myctrl)
Description	Erase data by 32Kbytes
Arguments	*myctrl : Pointer to the control structure for instance
Return value	0 : Operation success
	-1 : Operation Failed

flash_erase_64k	
Outline	Erase data by 64Kbytes
Declaration	int flash_erase_64k (qspiflash_at25_ctrl_t * myctrl)
Description	Erase data by 64Kbytes
Arguments	*myctrl : Pointer to the control structure for instance
Return value	0 : Operation success
	-1 : Operation Failed

5.12.2.4 module control functions

The module control functions that control each module are shown below.

syc_init	
Outline	Initialize the Cortex®-A55 built-in Generic Timer
Declaration	void syc_init (unsigned int freq)
Description	Initialize the Cortex®-A55 built-in Generic Timer and start count
Arguments	freq : Frequency of the counter
Return value	None

generic_delay_timer_init	
Outline	Initialize timer management parameters
Declaration	void generic_delay_timer_init (void)
Description	Timer parameter is initialized. By executing the syc_init() function and this function, the following wait functions can be executed. functionudelay() : Wait in usec unit. functionmdelay() : Wait in msec unit.
Arguments	None
Return value	None

pfc_setup	
Outline	Set up the pin
Declaration	void pfc_setup (void)
Description	Set up pin setting of SCIF and SPIBSC.
Arguments	None
Return value	None

pfc_mux_setup	
Outline	Set up pin setting of SCIF
Declaration	void pfc_mux_setup (void)
Description	Set up pin setting of SCIF and SPIBSC. Set the P6 pin as SCIF0.
Arguments	None
Return value	None

pfc_qspi_setup	
Outline	Set up pin setting of SPIBSC
Declaration	void pfc_qspi_setup (void)
Description	Set up pin setting of SPIBSC.
Arguments	None
Return value	None

cpg_setup	
Outline	Set up CPG
Declaration	void cpg_setup (void)
Description	Set up CPG.
Arguments	None
Return value	None

cpg_ctrl_clkrst	
Outline	Execute write processing to the clock control register and reset control register
Declaration	void cpg_ctrl_clkrst (CPG_SETUP_DATA const *array、uint32_t num)
Description	Execute write processing to the clock control register and reset control register.
Arguments	*array : Pointer to CPG setup data table num : Number of elements in CPG setup data table
Return value	None

cpg_selector_on_off	
Outline	Clock ON/OFF setting for modules whose clocks are managed by the source clock selector
Declaration	void cpg_selector_on_off (uint32_t sel, uint8_t flag)
Description	The source clock selector simultaneously turns ON/OFF the clocks of the modules to which the clock is to be supplied. Call this function to turn the clock on/off before and after changing the source clock selector.
Arguments	sel : Specifies the source clock selector to change flag : Set the clock ON/OFF
Return value	None

cpg_pll_start_146	
Outline	Start process of PLL1/PLL4/PLL6
Declaration	void cpg_pll_start_146 (CPG_PLL_SETDATA_146 *pdata)
Description	By operating the registers of PLL1/PLL4/PLL6, the frequency is set, standby is released, and PLL operation is started.
Arguments	*pdata : Pointer to PLL1/4/6 setting table
Return value	None

cpg_pll_setup	
Outline	Set up PLL setting
Declaration	void cpg_pll_setup (void)
Description	Reset the PLL4/PLL6 and set the frequency, start the PLL operation.
Arguments	None
Return value	None

cpg_div_sel_setup	
Outline	Write to Division Ratio Setting Register and Source Clock Setting Register.
Declaration	void cpg_div_sel_setup (CPG_REG_SETTING *tbl, uint32_t size)
Description	Write to Division Ratio Setting Register and Source Clock Setting Register.
Arguments	*tbl : Pointer to CPG register setting table size : Size of CPG register setting table
Return value	None

cpg_div_sel_static_setup	
Outline	Perform Static Switching Frequency Dividers and Selector settings.
Declaration	void cpg_div_sel_static_setup (void)
Description	Perform Static Switching Frequency Dividers and Selector settings. Set the registers registered in cpg_static_select_tbl.
Arguments	None
Return value	None

cpg_div_sel_dynamic_setup	
Outline	Perform Dynamic Switching Frequency Dividers and Selector settings.
Declaration	void cpg_div_sel_dynamic_setup (void)
Description	Perform Dynamic Switching Frequency Dividers and Selector settings. Set the registers registered in cpg_dynamic_select_tbl.
Arguments	None
Return value	None

cpg_clk_on_setup	
Outline	Execute clock supply settings for each module
Declaration	void cpg_clk_on_setup (void)
Description	Execute clock supply settings for each module. Set the registers registered in cpg_clk_on_tbl.
Arguments	None
Return value	None

cpg_reset_setup	
Outline	Execute reset release setting for each module
Declaration	void cpg_reset_setup (void)
Description	Execute reset release setting for each module. Set the registers registered in cpg_reset_tbl.
Arguments	None
Return value	None

cpg_active_ddr	
Outline	Execute DDR PHY clock and reset release settings
Declaration	void cpg_active_ddr (void (*disable_phy)(void))
Description	Execute DDR PHY clock and reset release settings.
Arguments	*disable_phy : Pointer to disable_phy_clk function
Return value	None

cpg_reset_ddr_mc	
Outline	Execute DDR memory controller clock and reset release settings
Declaration	void cpg_active_ddr (void (*disable_phy)(void))
Description	Execute DDR memory controller clock and reset release settings.
Arguments	*disable_phy : Pointer to disable_phy_clk function
Return value	None

cpg_early_setup	
Outline	Executes clock supply to modules required for preprocessing of platform settings and reset release settings
Declaration	void cpg_early_setup (void)
Description	Executes clock supply to modules required for preprocessing of platform settings and reset release settings. This function sets the registers registered in early_setup_tbl.
Arguments	None
Return value	None

cpg_wdtrst_sel_setup	
Outline	Execute reset release setting of Watchdog Timer module
Declaration	void cpg_wdtrst_sel_setup (void)
Description	Execute reset release setting of Watchdog Timer module.
Arguments	None
Return value	None

cpu_cpg_setup	
Outline	Execute clock division ratio setting to CPU
Declaration	void cpu_cpg_setup (void)
Description	Set the clock division ratio to the CPU to 1/1.
Arguments	None
Return value	None

cpg_search_spi_clk_table	
Outline	Search the clock frequency register setting table corresponding to the clock frequency supplied to the Serial Flash memory
Declaration	int cpg_search_spi_clk_table (int frequency)
Description	Search the element number corresponding to the clock frequency supplied to the Serial Flash memory from the clock frequency register setting table.
Arguments	frequency : Clock frequency
Return value	Positive number: Element number of register setting table -1 : The element number corresponding to the clock frequency does not exist in the table

cpg_research_spi_clk_table	
Outline	Search for clock frequency value supplied to Serial Flash memory
Declaration	int cpg_search_spi_clk_table (uint8_t selector, uint8_t divider)
Description	Searches for the clock frequency to be supplied to the Serial Flash memory from the clock selector and divider settings set in the CPG register.
Arguments	selector : Source clock selector setting divider : Divider setting
Return value	Positive number: Clock frequency -1 : No parameters in table for clock selector and divider settings

cpg_stop_xspi_clock	
Outline	Stop supplying clock to Serial Flash memory
Declaration	void cpg_stop_xspi_clock (xspi_clock spi)
Description	Stop supplying clock to Serial Flash memory.
Arguments	spi : Specifies the type of Serial Flash memory XSPI_CLOCK_SPIM: Serial Flash memory XSPI_CLOCK_OCTA: Octa Flash memory
Return value	None

cpg_start_xspi_clock	
Outline	Start supplying clock to Serial Flash memory
Declaration	void cpg_start_xspi_clock (xspi_clock spi)
Description	Start supplying clock to Serial Flash memory.
Arguments	spi : Specifies the type of Serial Flash memory XSPI_CLOCK_SPIM: Serial Flash memory XSPI_CLOCK_OCTA: Octa Flash memory
Return value	None

cpg_set_xspi_clock	
Outline	Execute clock setting processing for Serial Flash memory
Declaration	void cpg_set_xspi_clock (xspi_clock spi, int frequency_hz)
Description	Execute clock setting processing for Serial Flash memory.
Arguments	spi : Specifies the type of Serial Flash memory XSPI_CLOCK_SPIM: Serial Flash memory XSPI_CLOCK_OCTA: Octa Flash memory frequency_hz : Clock frequency
Return value	None

cpg_get_xspi_clock	
Outline	Get the clock frequency supplied to the Serial Flash memory
Declaration	int cpg_get_xspi_clock (xspi_clock spi)
Description	Get the clock frequency supplied to the Serial Flash memory.
Arguments	spi : Specifies the type of Serial Flash memory XSPI_CLOCK_SPIM: Serial Flash memory XSPI_CLOCK_OCTA: Octa Flash memory
Return value	positive number: Clock frequency -1 : Failed to get clock frequency

wait_until_32	
Outline	Wait for completion of clock setting
Declaration	int wait_until_32 (uintptr_t addr, uint32_t mask, uint32_t test)
Description	This function reads the CPG monitor register and waits until the clock setting is reflected and the clock stabilizes.
Arguments	addr : CPG monitor register mask : Bitmask to read test : Expected read value of CPG monitor register
Return value	None

console_rzg2l_register	
Outline	Configuring console output
Declaration	int console_rzg2l_register- (uintptr_t baseaddr, uint32_t clock, uint32_t baud, console_t *console)
Description	Perform the SCIF settings used for console output. After setting, it is possible to output to the console with printf().
Arguments	baseaddr : SCIF register base address of the channel used clock : Input clock frequency for SCIF module baud : Baud rate setting to console output *console : Parameter of console output This parameter is automatically set when this function is executed
Return value	1 : Console output setting success 0 : Console output registration failure

console_set_scope	
Outline	Set the valid state of the console output
Declaration	void console_set_scope (console_t *console, unsigned int scope)
Description	Set the state in which console output processing is enabled.
Arguments	*console : Console output parameter Set parameters obtained by console_rzg2l_register() scope : Sets the state that enables console output processing Please set (CONSOLE_FLAG_BOOT | CONSOLE_FLAG_CRASH) in the IPL
Return value	None

plat_get_bl_image_load_info	
Outline	Get FSP application image load information
Declaration	bl_load_info_t *plat_get_bl_image_load_info(void)
Description	Get FSP application image load information.
Arguments	None
Return value	Positive number: Pointer to FSP application image load information

plat_get_next_bl_params	
Outline	Get FSP application image parameter information
Declaration	bl_params_t *plat_get_next_bl_params (void)
Description	Get FSP application image parameter information.
Arguments	None
Return value	Positive number: Pointer to FSP application image parameter information

rz_check_fsp_header	
Outline	Perform application header check
Declaration	int rz_check_fsp_header (fsp_app_header_t *header)
Description	Check the contents of the application header. This function will return an error if: - entry_addr != entry_addr_inv - dest_addr != dest_addr_inv - payload_size != payload_size_inv - The image copy area address is outside the On-chip RAM or DDR SDRAM area.
Arguments	*header : Pointer to Application Header
Return value	0 : Application header parameters are valid values -1 : Application header parameters are invalid values

rz_update_descs	
Outline	Update the descriptor parameter with the content obtained from the application header
Declaration	void rz_update_descs (fsp_app_header_t *header)
Description	Update the descriptor parameter with the content obtained from the application header. IPL controls the jump destination address of the FSP application by this descriptor.
Arguments	*header : Pointer to Application Header
Return value	None

rz_load_fsp	
Outline	Load FSP application image
Declaration	void rz_load_fsp (void)
Description	The application header is read and checked, and the FSP application is copied according to its contents and the descriptor is updated. If the application header check fails, the IPL will go into an infinite loop and stop the boot process.
Arguments	None
Return value	None

rz_print_descs	
Outline	Parameters of the descriptor are printed to the console
Declaration	void rz_print_descs (void)
Description	Parameters of the descriptor are printed to the console.
Arguments	None
Return value	None

ddr_setup	
Outline	Initialize DDR SDRAM
Declaration	void ddr_setup (void)
Description	Initializes DDR SDRAM and enables read/write access to DDR SDRAM.
Arguments	None
Return value	None

5.13 Flow Chart

5.13.1 IPL (overall) flow

Figure 5.6, Figure 5.7, Figure 5.8 show the flowchart of IPL (overall)

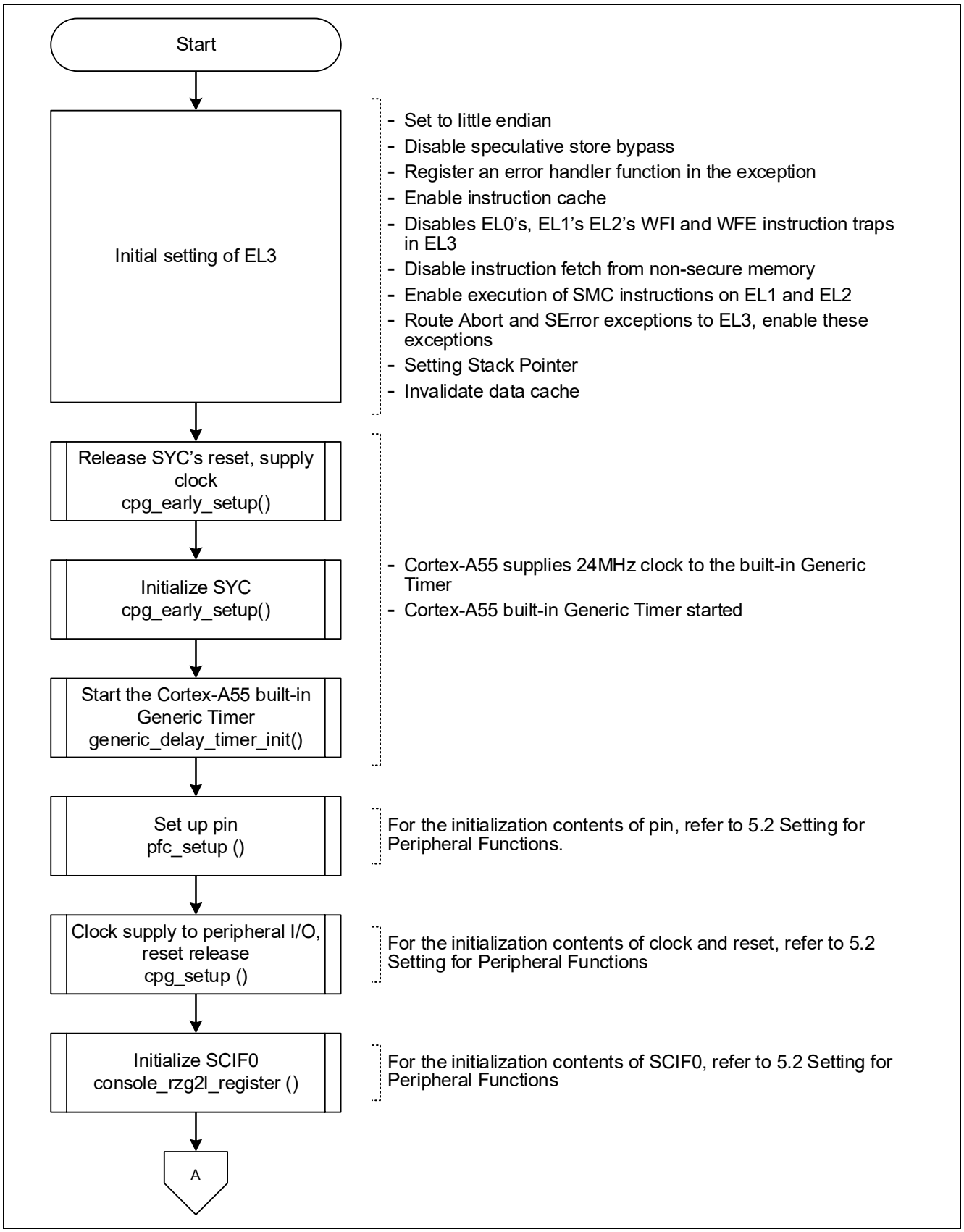


Figure 5.6 IPL Flow Chart part (1/3)

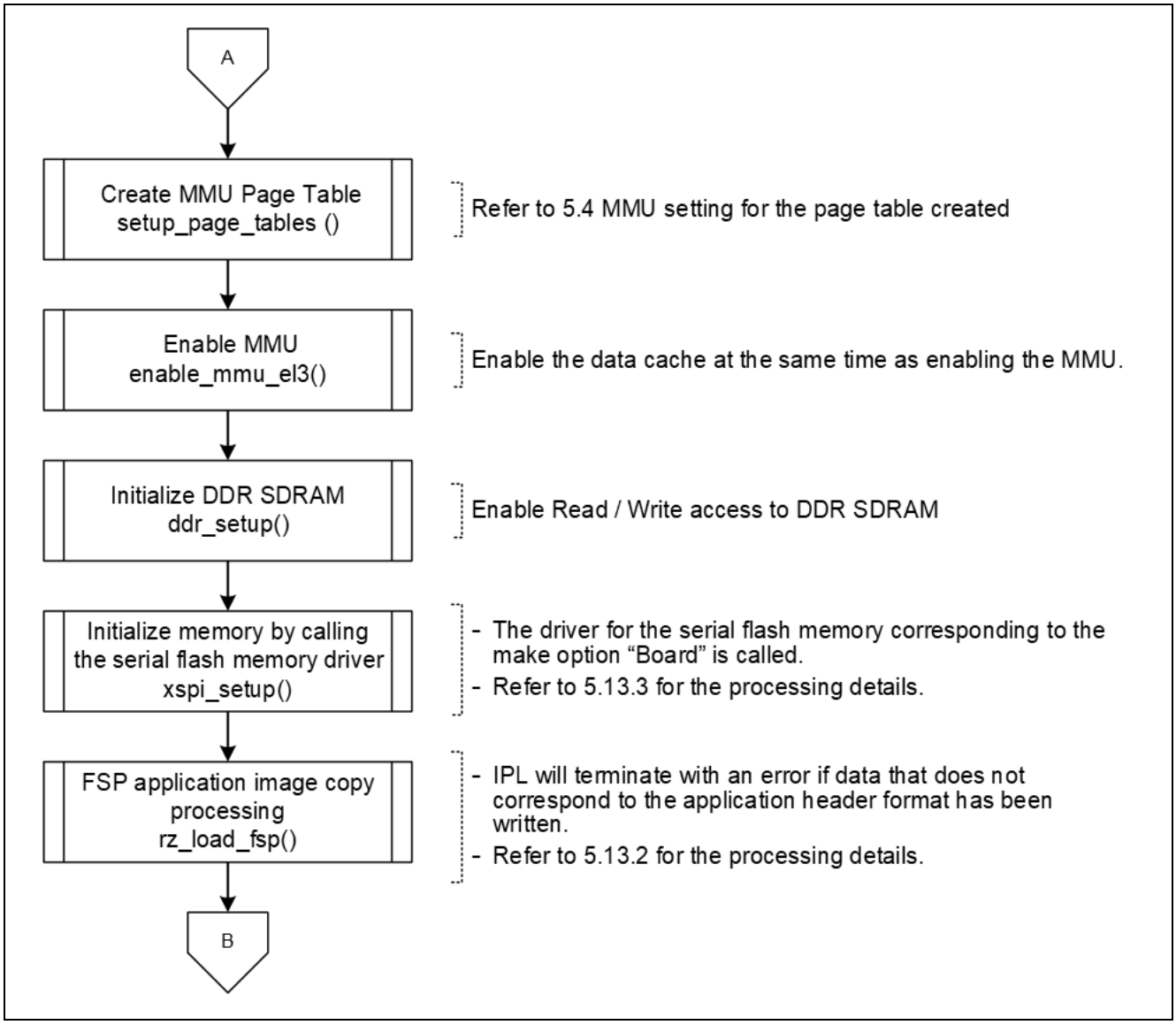


Figure 5.7 IPL Flow Chart part (2/3)

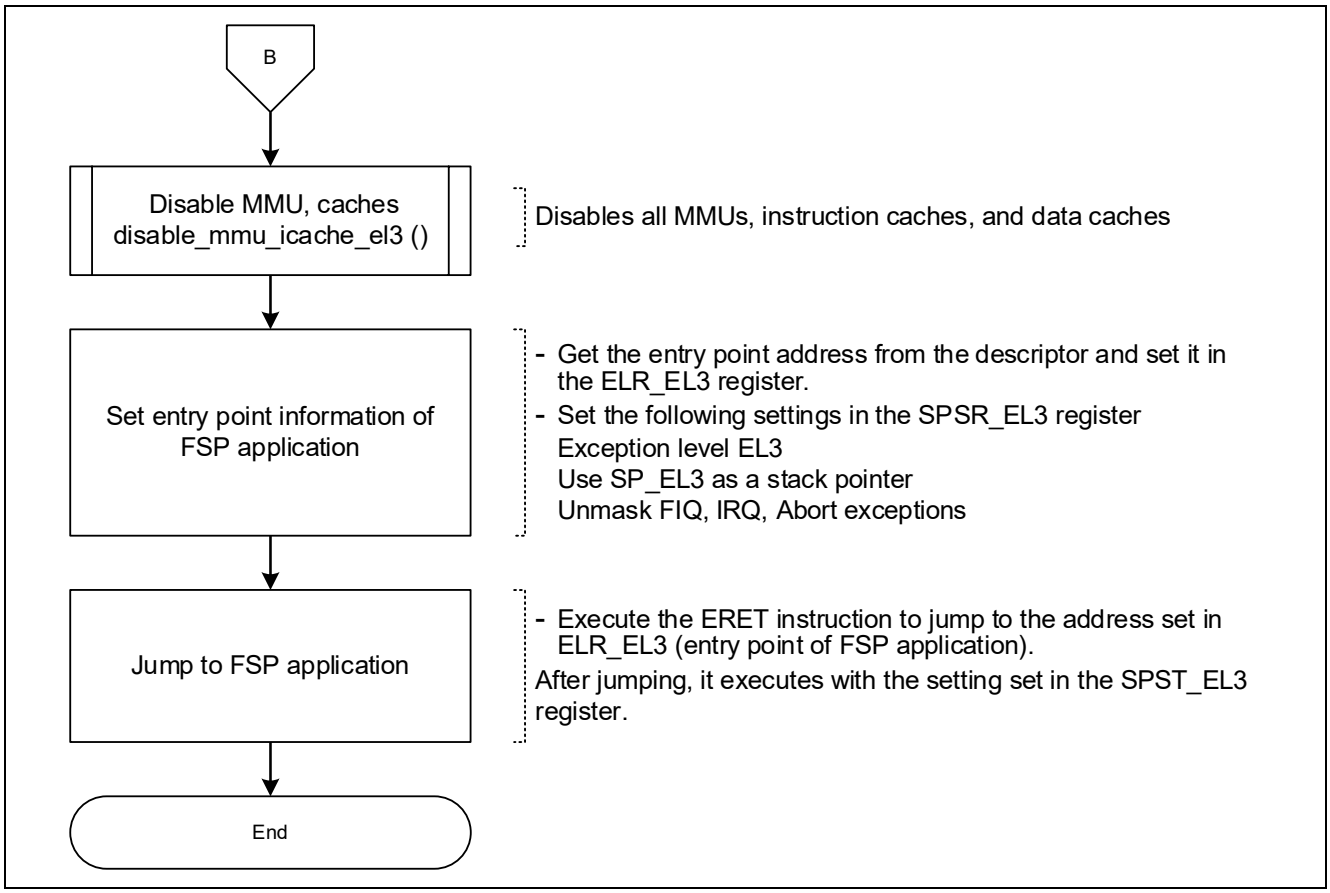


Figure 5.8 IPL Flow Chart part (3/3)

5.13.2 FSP Application Image copy process

Figure 5.9 and Figure 5.10 show the flow chart of the FSP Application image copy process.

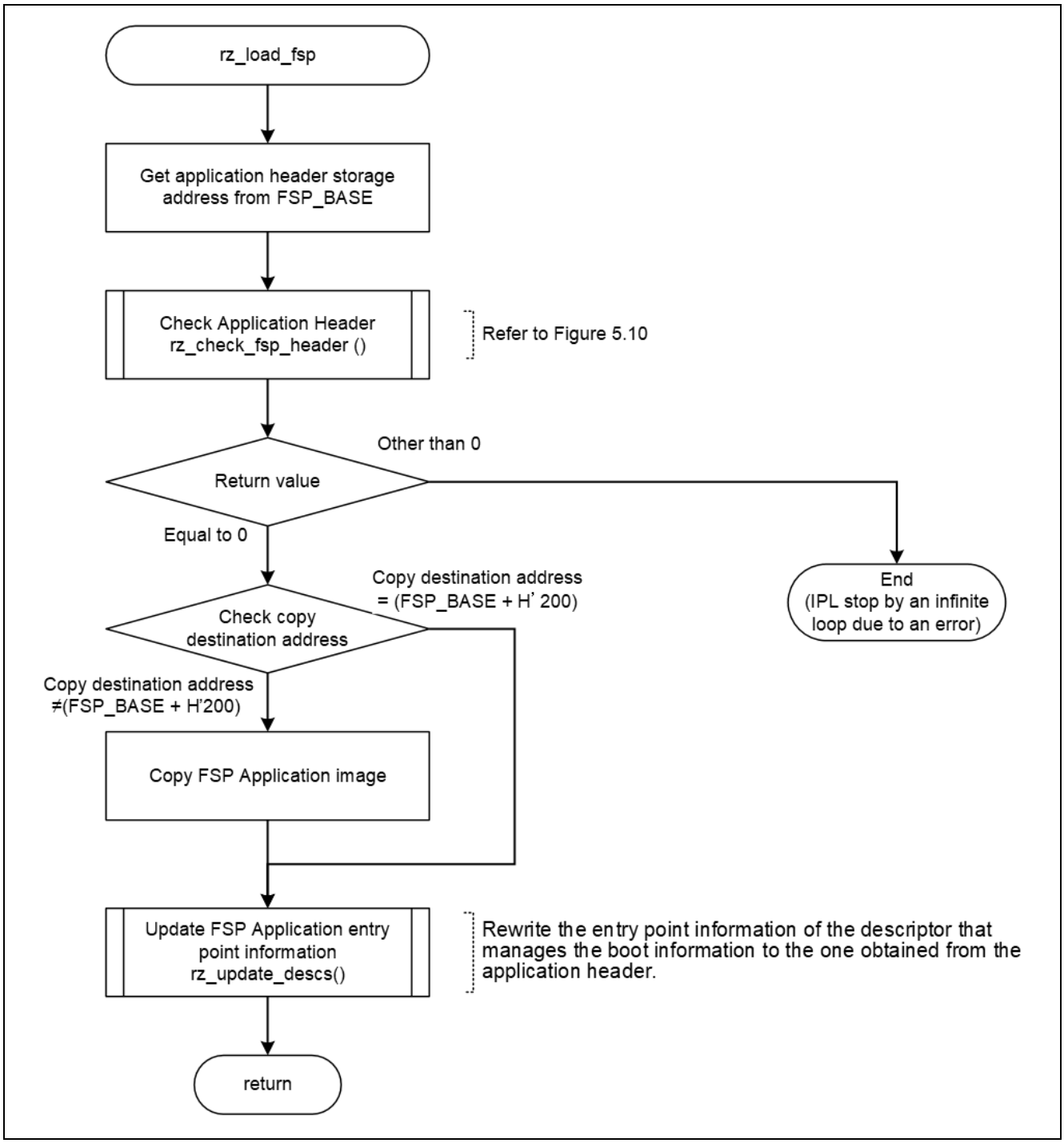


Figure 5.9 Flow Chart of rz_load_fsp()

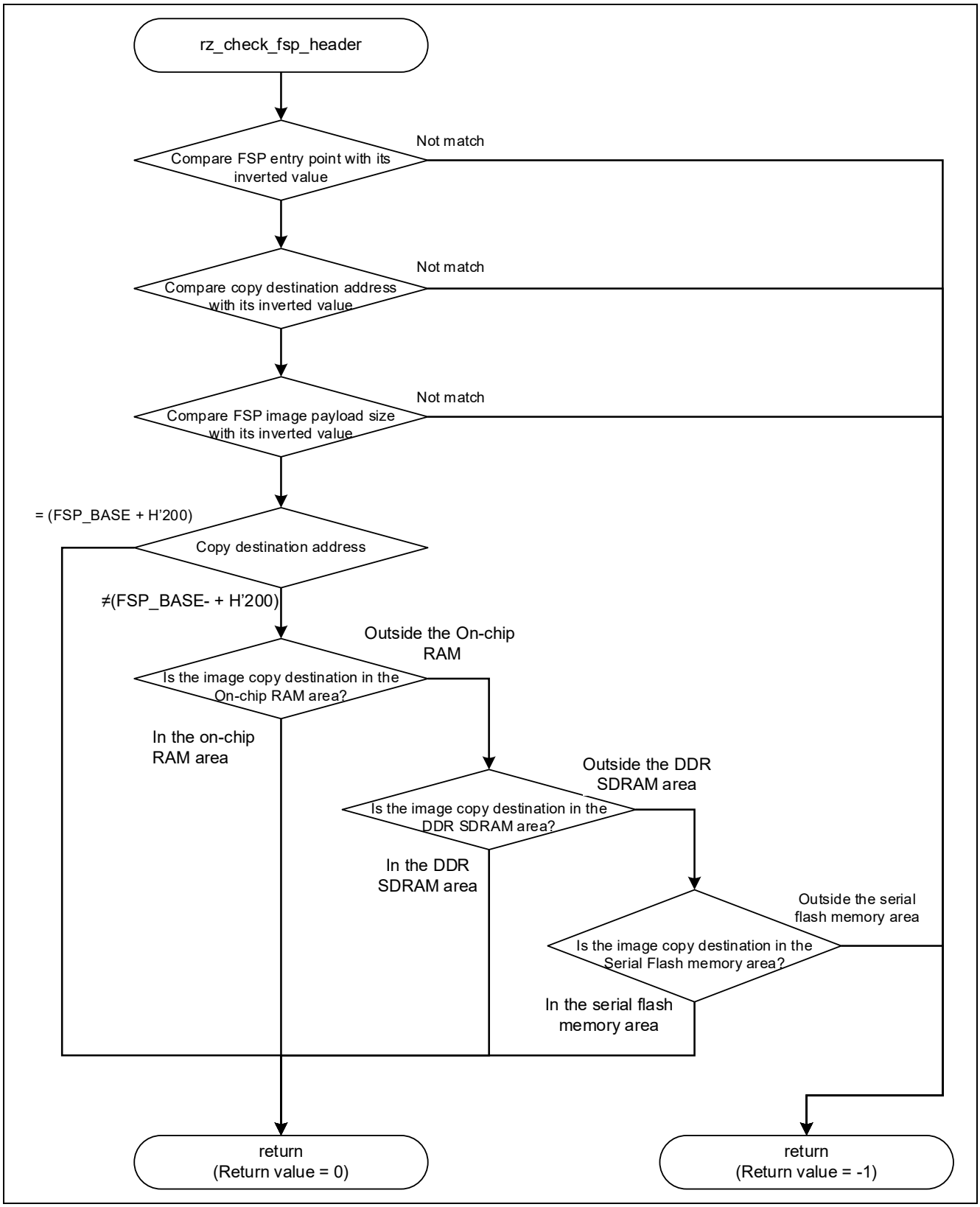


Figure 5.10 Flow Chart of rz_check_fsp_header()

5.13.3 Setting of Serial Flash memory and SPIBSC

In this IPL, the Renesas Electronics Serial Flash memory (AT25QL128A) is set so that it can be accessed by XIP (Execute in place) via SPIBSC.

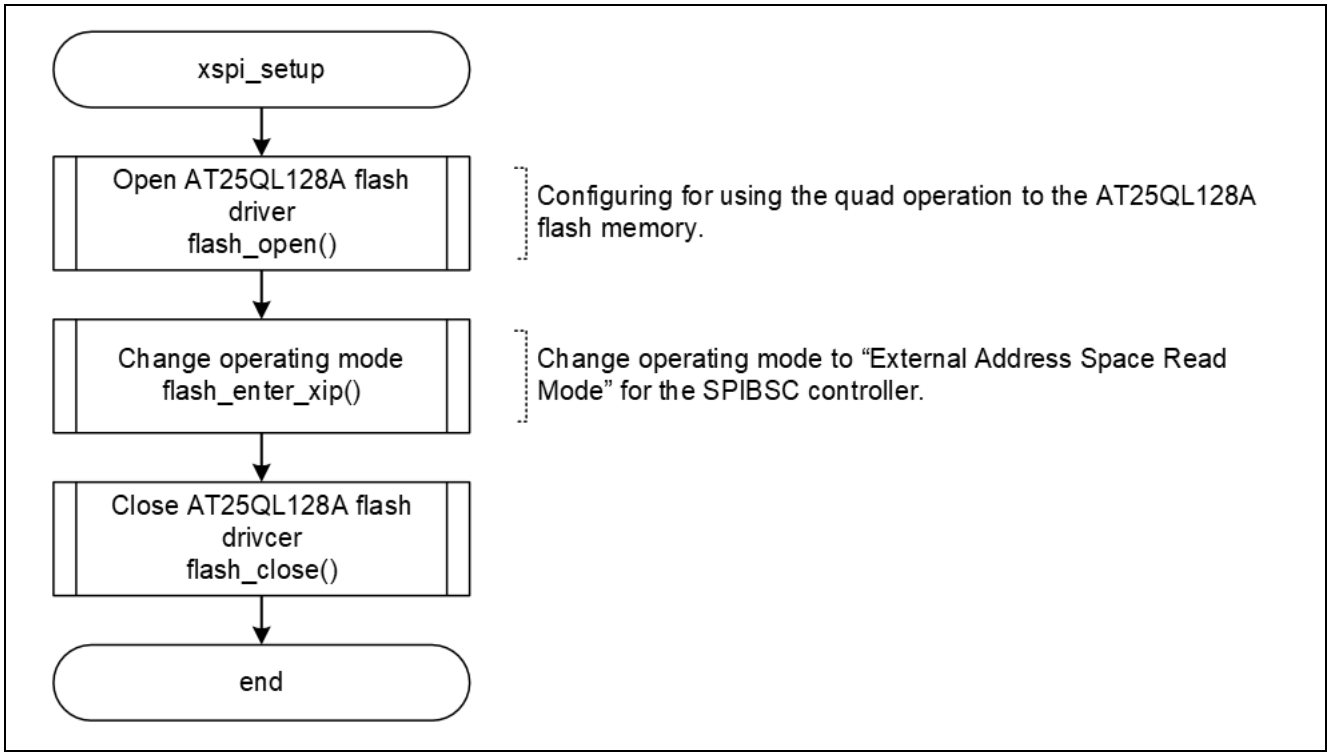


Figure 5.11 Flowchart of xspi_setup()

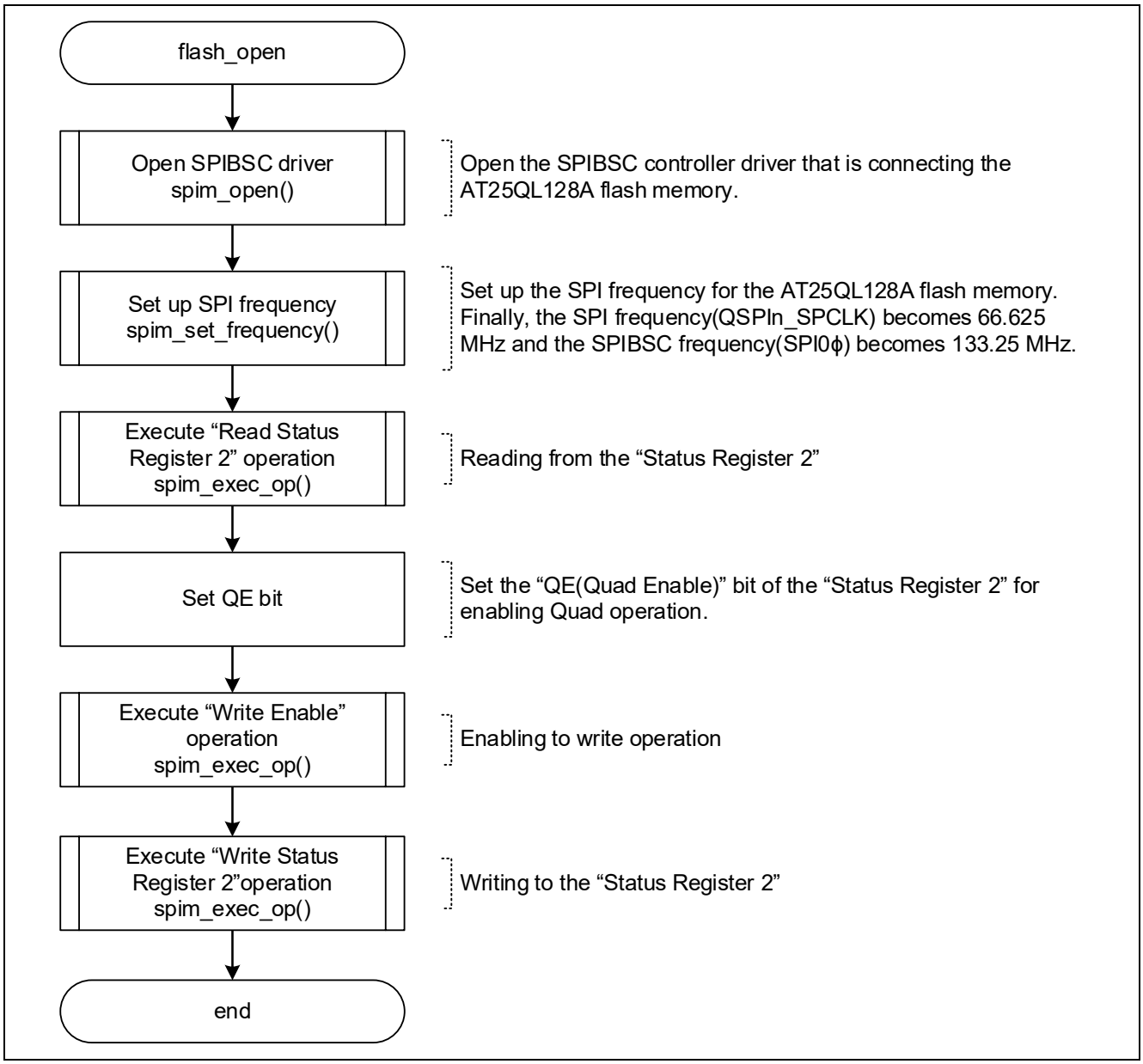


Figure 5.12 Flowchart of flash_open()

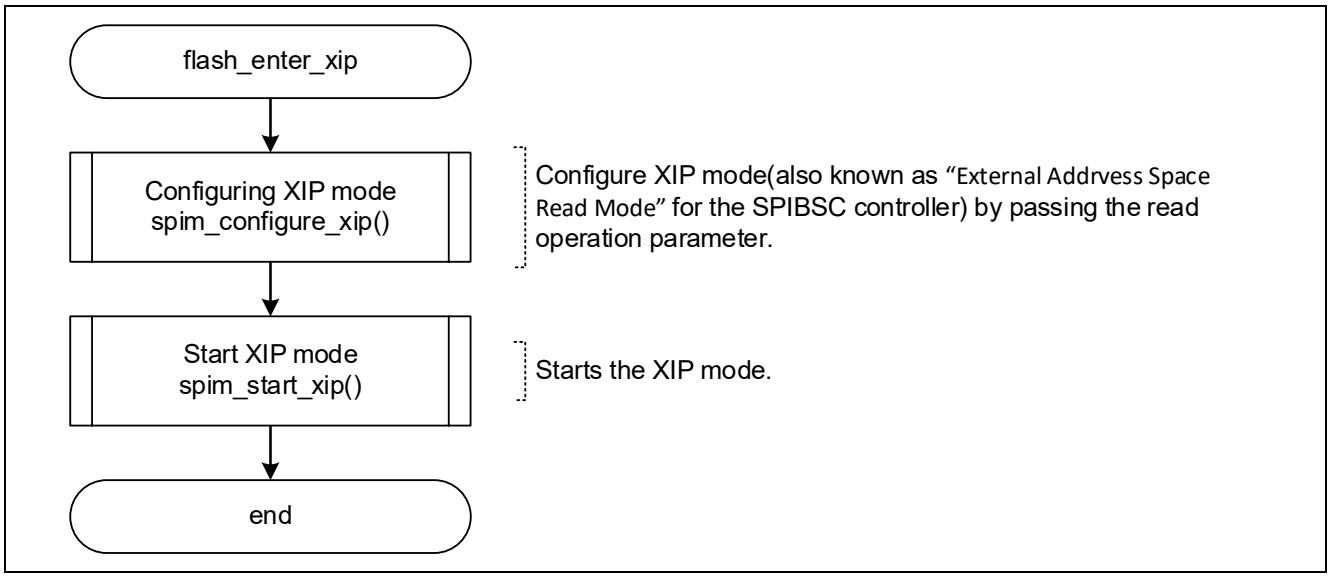


Figure 5.13 Flowchart of flash_enter_xip()

6. IPL development environment construction procedure

This chapter describes the procedure for building the IPL development environment.

6.1 Procedure for building a development environment for Widows10 PC

The procedure for building a development environment for the Windows10 environment is shown below.

6.1.1 Installation of IDE (e² studio) for Windows10

IPL uses e² studio as the development environment.

This chapter shows the installation procedure for Windows10.

Please download the e² studio installer from the Renesas Electronics web page below.

The toolchain is included in the e² studio installer.

The toolchain is installed while you install e² studio.

https://www.renesas.com/jp/ja/software-tool/e-studio

RZ/A3 FSP packs are required to build an IPL execution environment in e² studio. Please download from the following website.

https://github.com/renesas/rza-fsp/releases

6.1.1.1 e² studio installation (Windows10)

1. Double click the e2 studio installer to launch the e2 studio installation wizard. Then, select the [Custom Install] option and click the [Next] button.

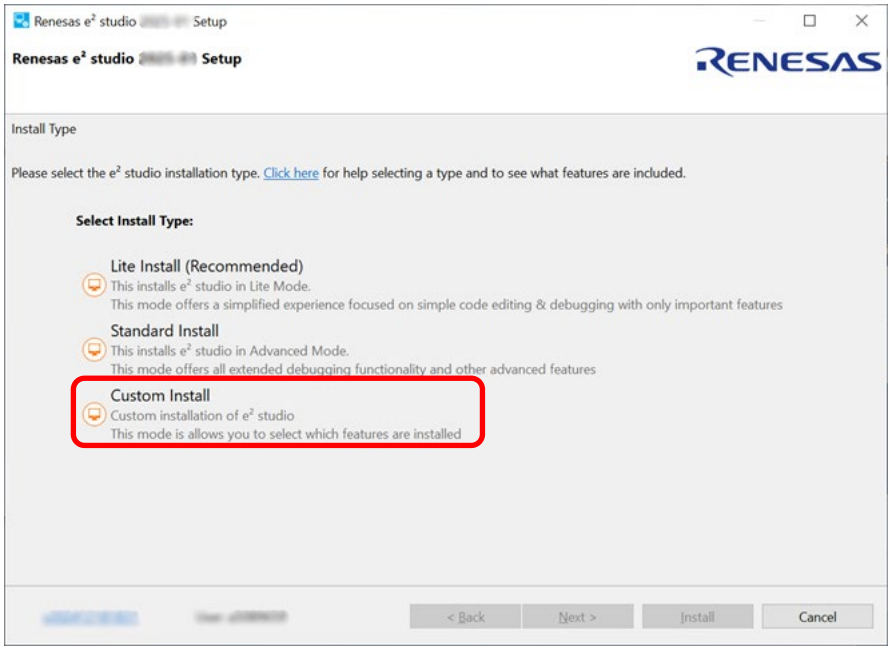


Figure 6.1 e2 studio installation wizard

Note: If you are using a multi-user environment, you may receive a prompt to confirm whether you want to install it for the current user only or for all users.

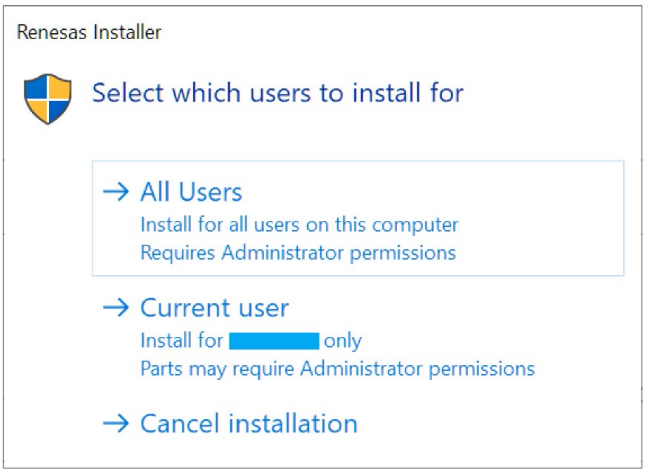


Figure 6.2: Select User for Installation

Note: If e² studio had been installed in your PC, the option to modify, remove the existing version or install e² studio to a different location will be displayed.
In this case, please select [Install].

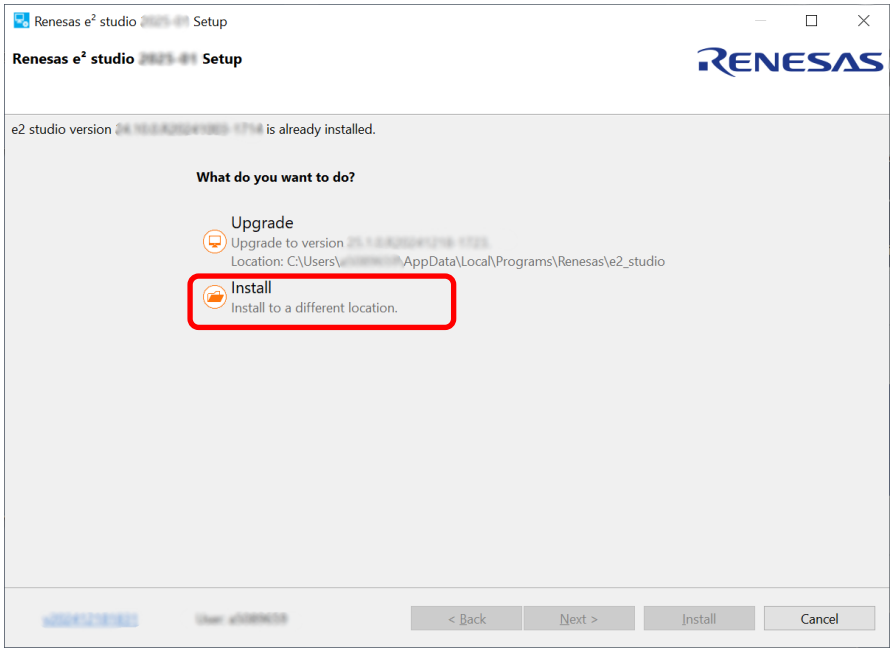


Figure 6.3 e² studio installation wizard

2. "Welcome" page
   User can change the install folder by clicking [Change...]. Click [Next] to continue.

Notes: 1. If you would like to have multiple versions of e² studio, please specify new folder here.
2. Multi-byte characters cannot be used for e² studio installation folder name.

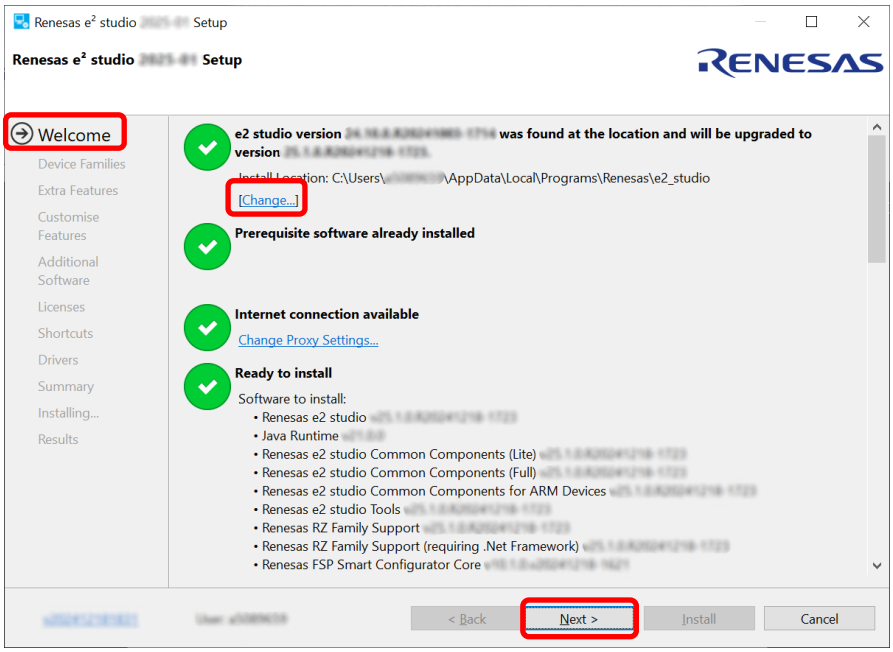


Figure 6.4 Installation of e² studio – Welcome page

3. "Device Families"
   You can select the device families to install. Select [RZ] Device Families to install.
   Click the [Next] button to continue.

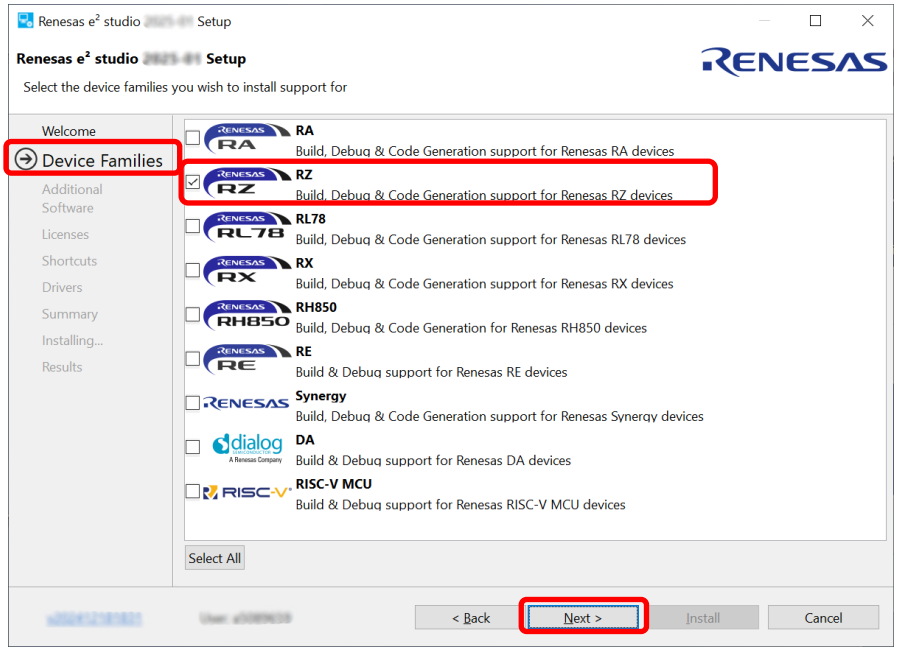


Figure 6.5 Installation of e² studio – Device Families

4. "Extra Features"
   Select Extra Features (i.e., Language packs, SVN & Git support, RTOS support...) to be installed.
   For non-English language users, please select Language packs at this step if needed.
   This document describes an example of using e² studio terminal, so please check [Terminals].
   Click the [Next] button to continue.

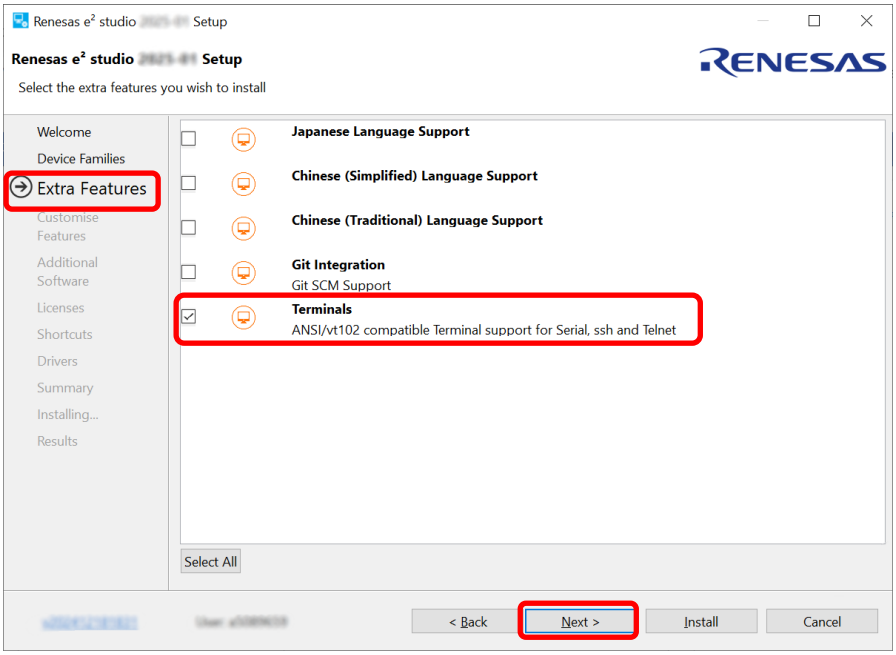


Figure 6.6 Installation of e² studio – Extra Features

5. "Customize Features"
   Be sure to select [Renesas FSP Smart Configurator Core].

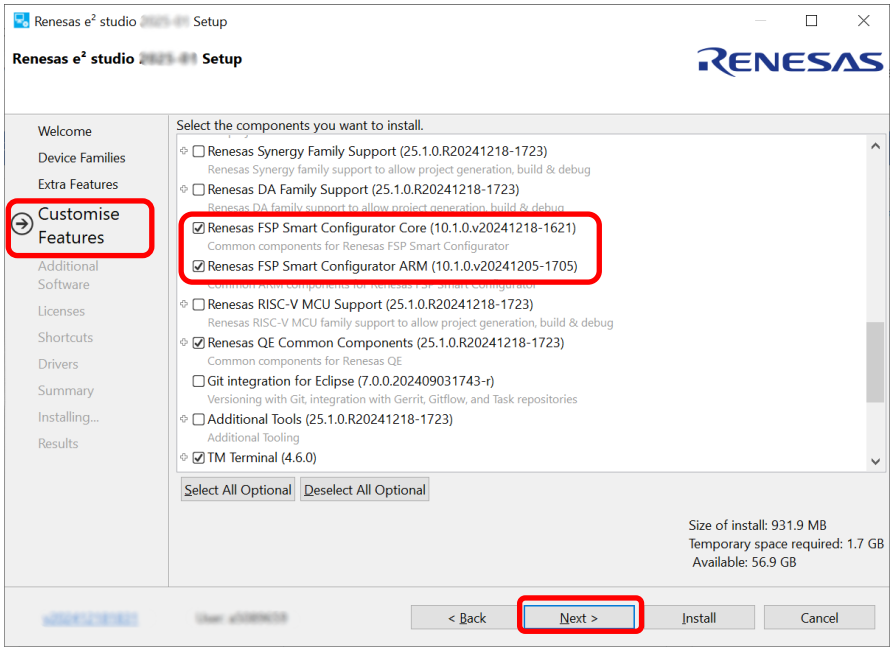


Figure 6.7 Installation of e² studio – Features

6. "Additional Software"
   Select additional software (i.e., compilers, utilities, QE…) to be installed.
   Add the following items if they are not checked, and click [Next] to continue:

   - GCC ARM A-Profile (AArch64 bare-metal) 10.3.2021.07

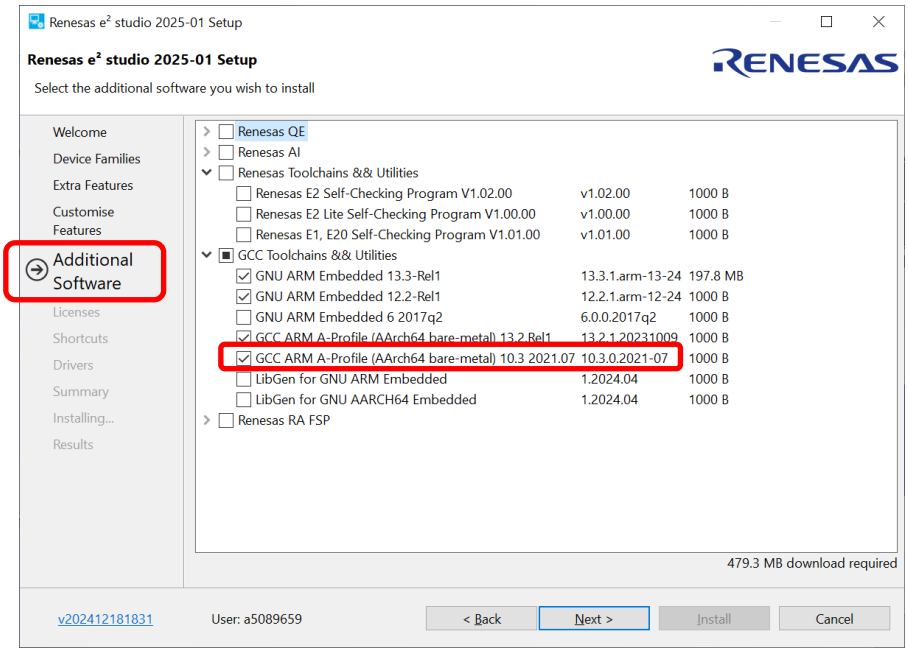


Figure 6.8 Installation of e² studio – Additional Software

7. "License Agreement"
   Please read and accept the software license agreement, then click the [Next] button. Note that acceptance of the license agreement is mandatory; without it, the installation process cannot proceed.

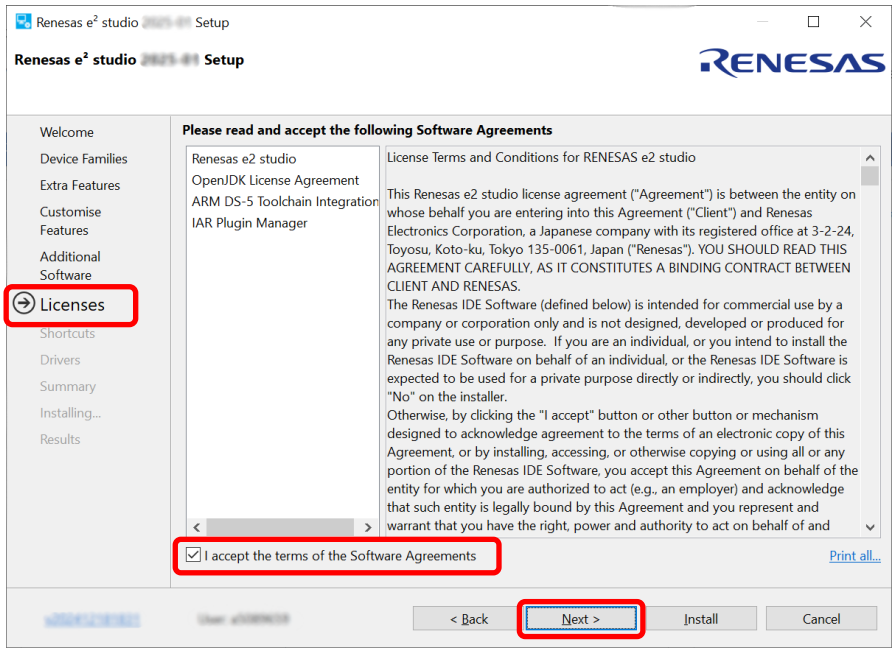


Figure 6.9 Installation of e² studio – Licenses

8. "Shortcuts"
   Select shortcut name for start menu and click [Next] button to continue.

Note:

If e2 studio was installed in another location, it is recommended to rename it to distinguish from the other e2 studio(s).

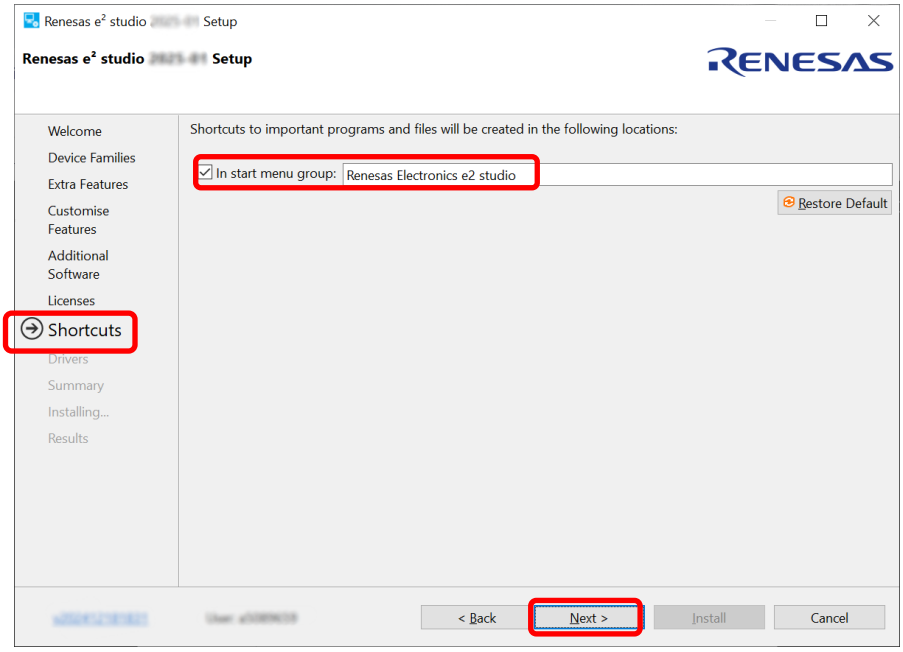


Figure 6.10 Installation of e² studio – Shortcuts

9. "Summary"
   Components list to be installed is shown.
   Please confirm the contents and click the [Install] button to install the Renesas e² studio IDE.

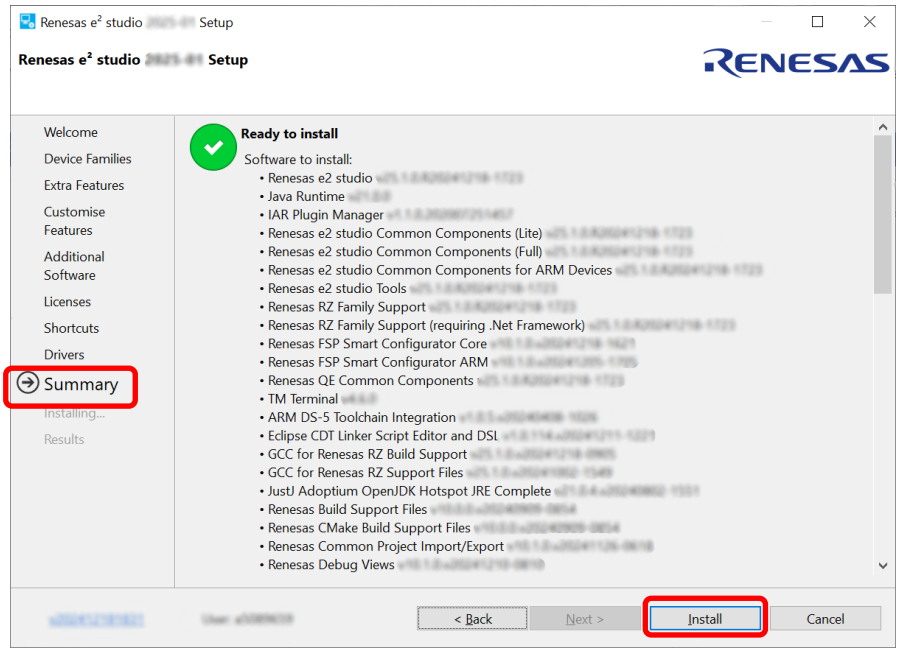


Figure 6.11 Installation of e² studio – Summary

10. "Installing"
    The installation is performed. Depending on selected items of additional software, new dialog prompts may appear during the installation process.

11."Results"

Click the [OK] button to complete the installation.

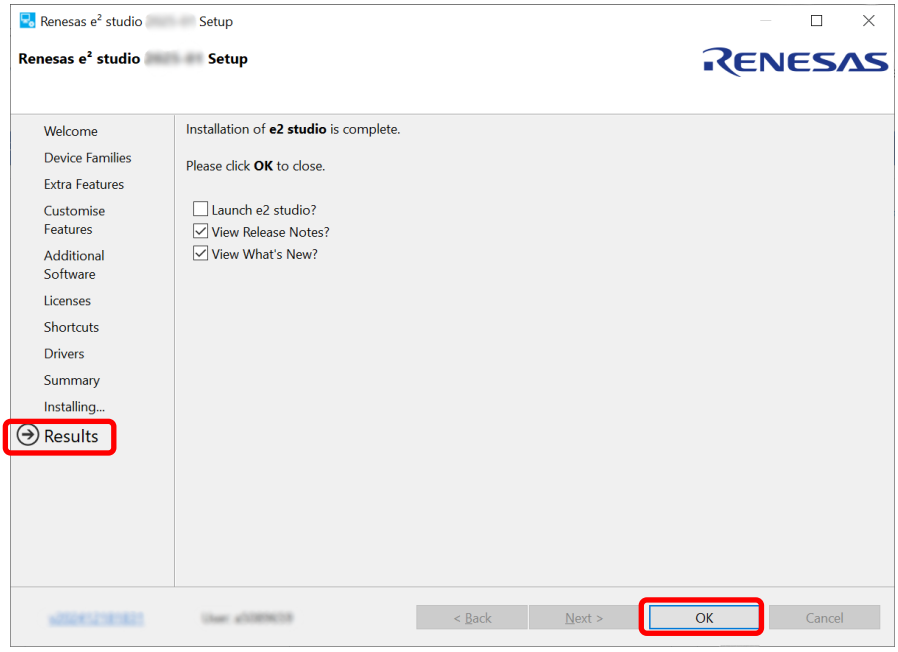


Figure 6.12 Result Page

6.1.1.2 Installation of RZ/A FSP packs (Windows10)

Install the FSP packs for use in the RZ/A3 IPL environment.

1. Exit e² studio
2. Extract FSP Packs.
3. Copy the extracted FSP Packs (named "internal") to the e² studio installation folder as shown below:
   "C:\Renesas\e2_studio\internal\projectgen\rz_fsp\rza\packs"

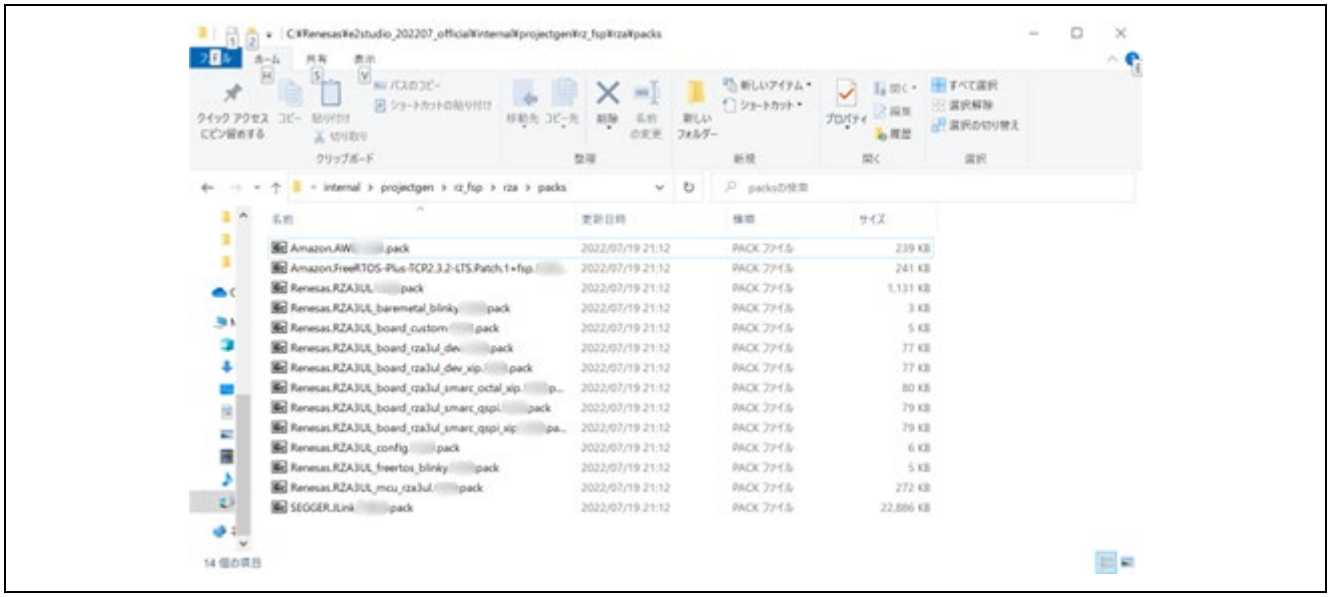


Figure 6.13 Installed packs folder (Windows10)

4. Please re-launch e² studio
   Then packs will be reflected in the development environment.

6.1.2 MSYS2 Installation

You must install a tool called MSYS2 to build the IPL in Windows10 environment.

1. Download MSYS2 from "Installation" on the following website.
   Please install by following the procedure described in "Installation".
   https://www.msys2.org/
   This document describes the case where MSYS2 is installed in the following folder.
   c:\msys64

2. Install the make command on MSYS2.
   Open the start menu and start "MSYS2 MSYS".

Figure 6.14 Launch MSYS2

3. A command window will appear.
   Enter "pacman -S make" on command window the make command on MSYS2.

Figure 6.15 Make command installation (1)

4. Enter ‘y’ when "Proceed with installation" [Y / n] "is output.

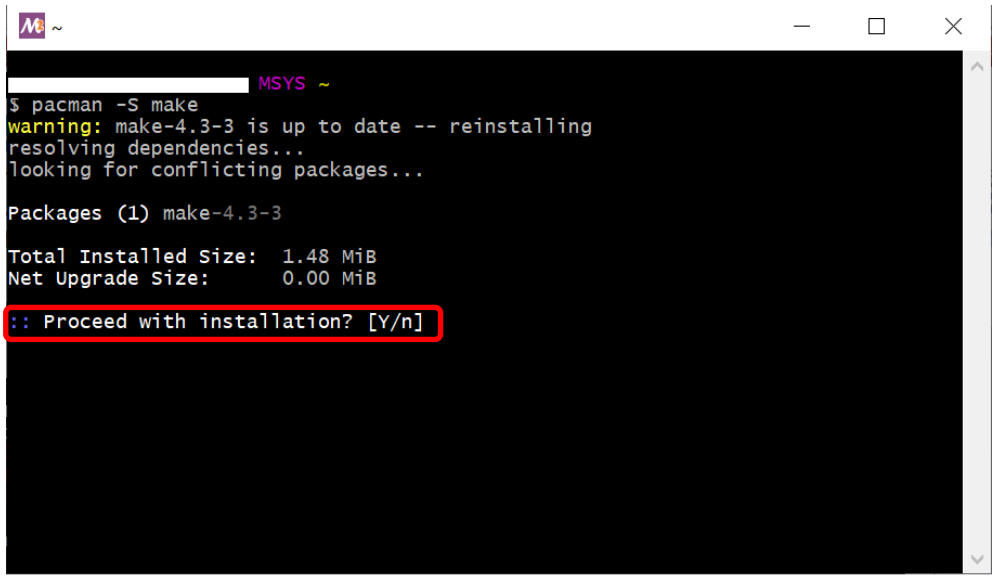


Figure 6.16 Make command installation (2)

5. The make installation is completed.

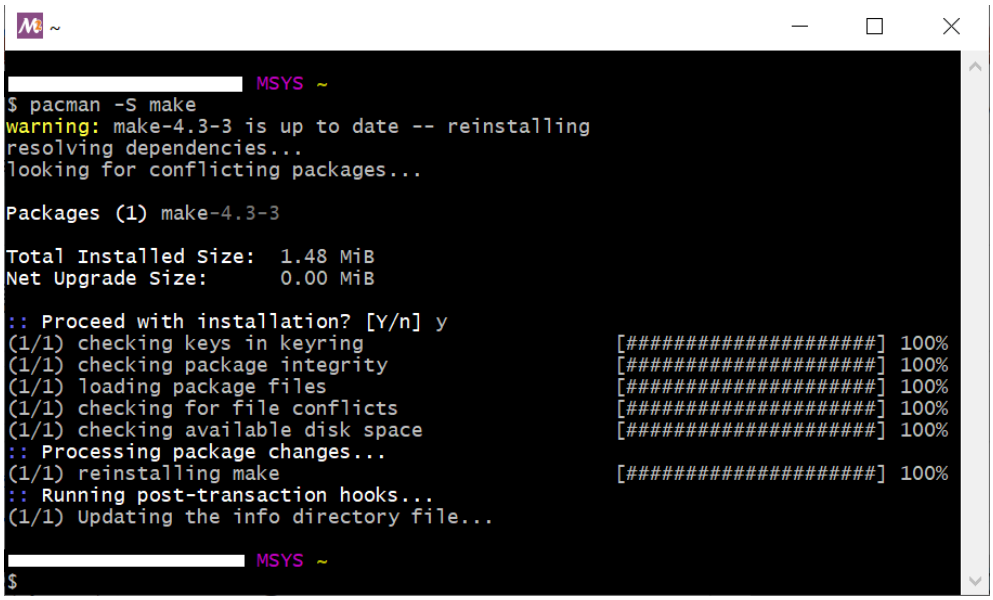


Figure 6.17 Make command installation (3)

6.2 Procedure for building a development environment for Ubuntu 22.04 LTS

The procedure for building a development environment for Ubuntu 22.04 LTS Desktop environment is shown below.

6.2.1 Installation of IDE (e² studio) for Ubuntu 22.04 LTS

IPL uses e² studio as the development environment.

This chapter shows the installation procedure for Ubuntu LTS 22.04.

Please download the e² studio installer from the Renesas Electronics web page below.

The toolchain is included in the e² studio installer.

The toolchain is installed while you install e² studio.

https://www.renesas.com/jp/ja/software-tool/e-studio

RZ/A3 FSP packs are required to build an IPL execution environment in e² studio. Please download from the following website.

https://github.com/renesas/rza-fsp/releases

6.2.1.1 e² studio installation (Ubuntu 22.04 LTS)

1. Execute the following command to give execute permission to the e² studio installer.
   Then, run the installer.
   The command is an example when the e² studio installer
   (file name: "e2studio_installer-2025-01_linux_host.run") is saved in the "~/Downloads" folder.
   Please change the command according to your environment.

```
$ cd ~/Downloads
$ sudo chmod +x e2studio_installer-2025-01_linux_host.run
$ ./e2studio_installer-2025-01_linux_host.run
```

2. User needs to select Install Type as shown below.
   In this material, it is expected that [Custom Install] is selected.
   Then, click [Next >] to continue.

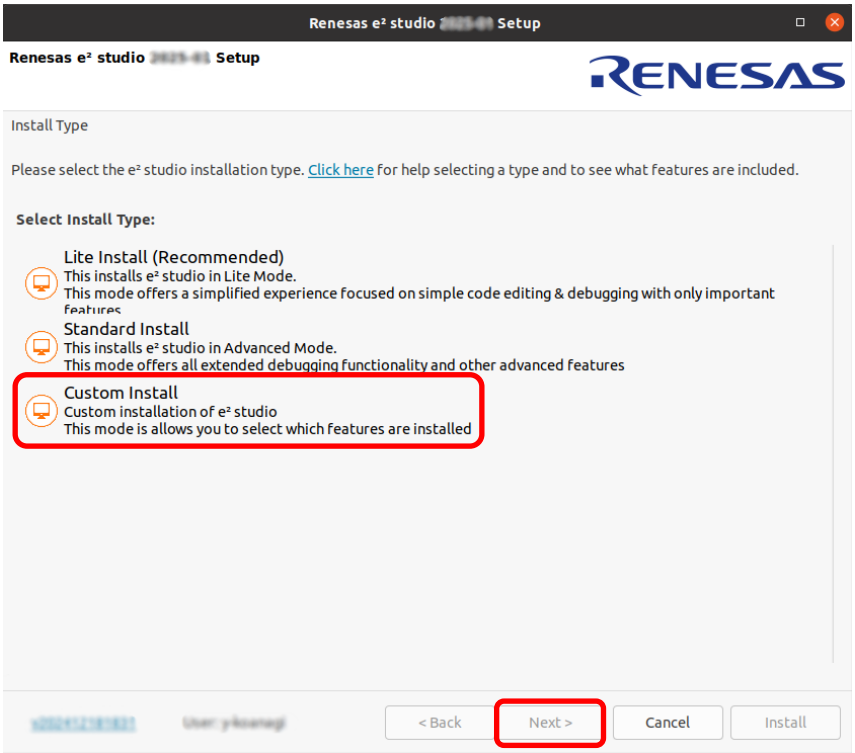


Figure 6.18 Installation of e² studio – Welcome page

3. "Welcome" page
   User can change the install folder by clicking [Change...]. Click [Next] to Click [Next] to continue.

Notes: 1. If you would like to have multiple versions of e² studio, please specify new folder here.
2. Multi-byte characters cannot be used for e² studio installation folder name.

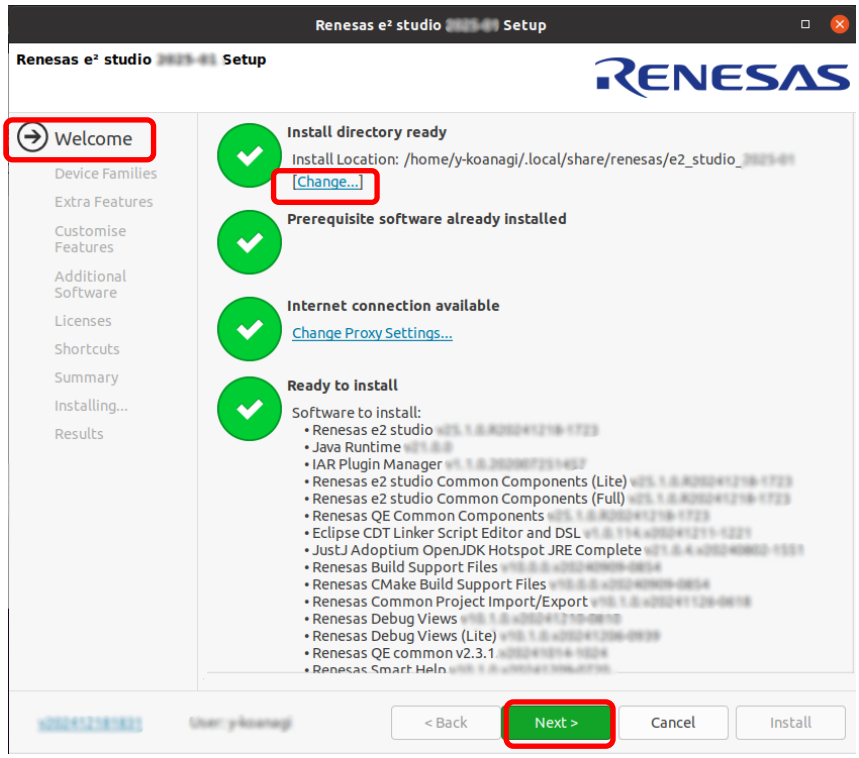


Figure 6.19 Installation of e² studio – Welcome page

4. "Device Families"
   You can select the device families to install.
   Select [RZ] Device Families to install.
   Click the [Next] button to continue.

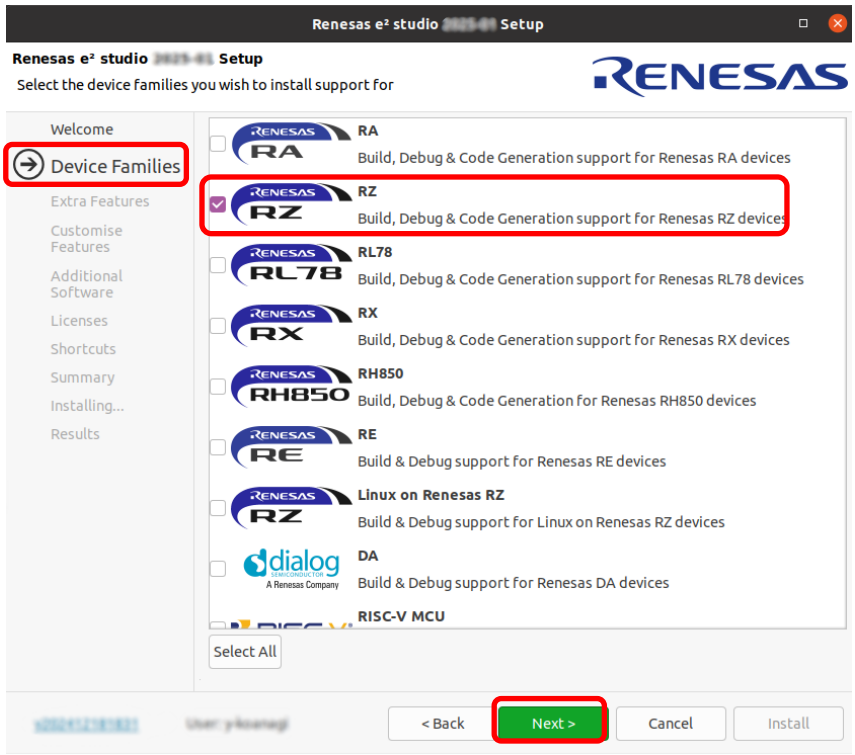


Figure 6.20 Installation of e² studio – Device Families

5. "Extra Features"
   Select Extra Features (i.e., Language packs, SVN & Git support, RTOS support...) to be installed.
   For non-English language users, please select Language packs at this step if needed.
   This document describes an example of using e² studio terminal, so please check [Terminals].
   Click the [Next] button to continue.

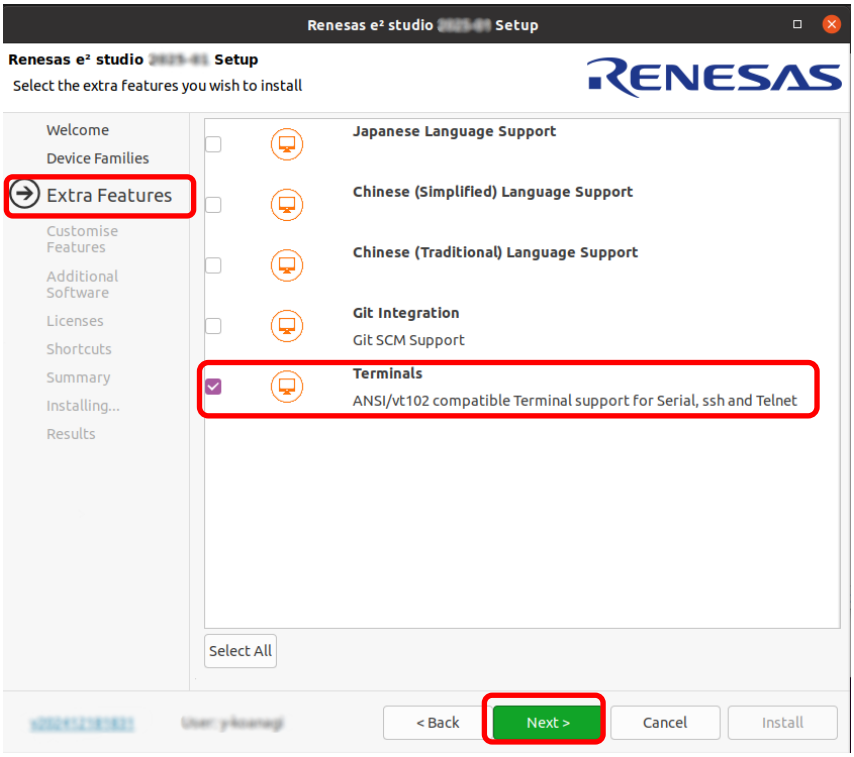


Figure 6.21 Installation of e² studio – Extra Features

6. "Customize Features"
   Select the components to install and click the [Next] button to continue. Be sure that [Renesas FSP Smart Configurator Core] is certainly selected.

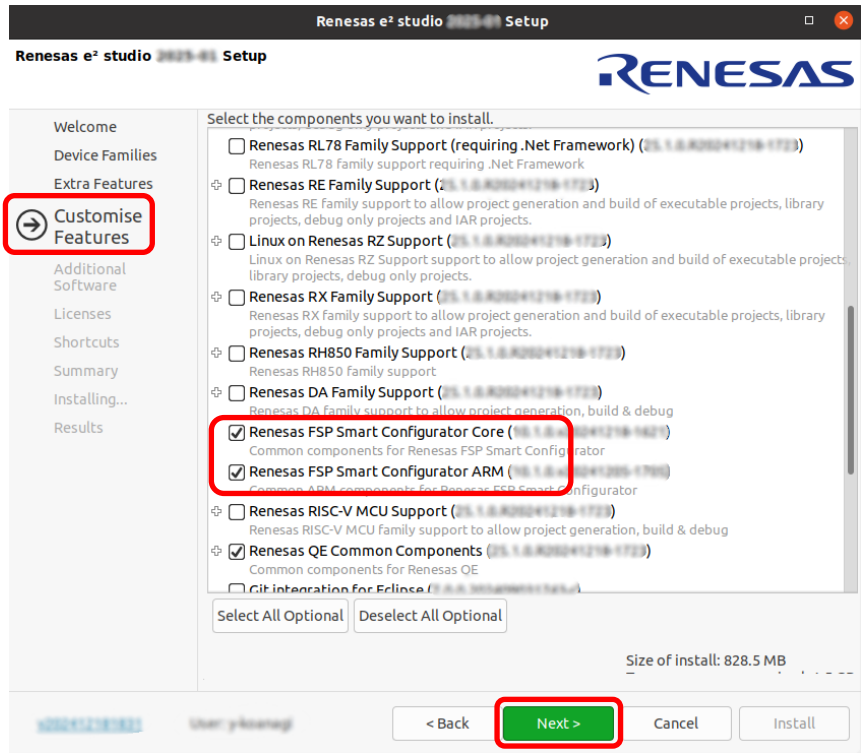


Figure 6.22 Installation of e² studio – Features

7. "Additional Software"
   Select additional software (i.e., compilers, utilities…) to be installed.
   Add the following items if they are not checked, and click [Next] to continue:

   - GCC ARM A-Profile (AArch64 bare-metal) 10.3.2021.07

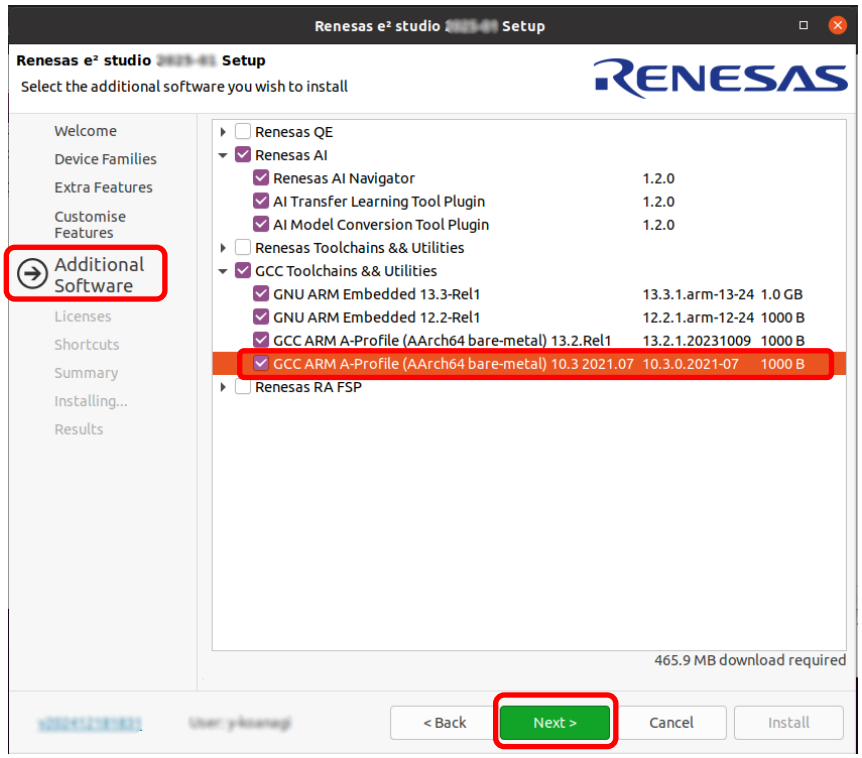


Figure 6.23 Installation of e² studio – Additional Software

8. "License Agreement"
   Please read and accept the software license agreement, then click the [Next] button. Note that acceptance of the license agreement is mandatory; without it, the installation process cannot proceed.

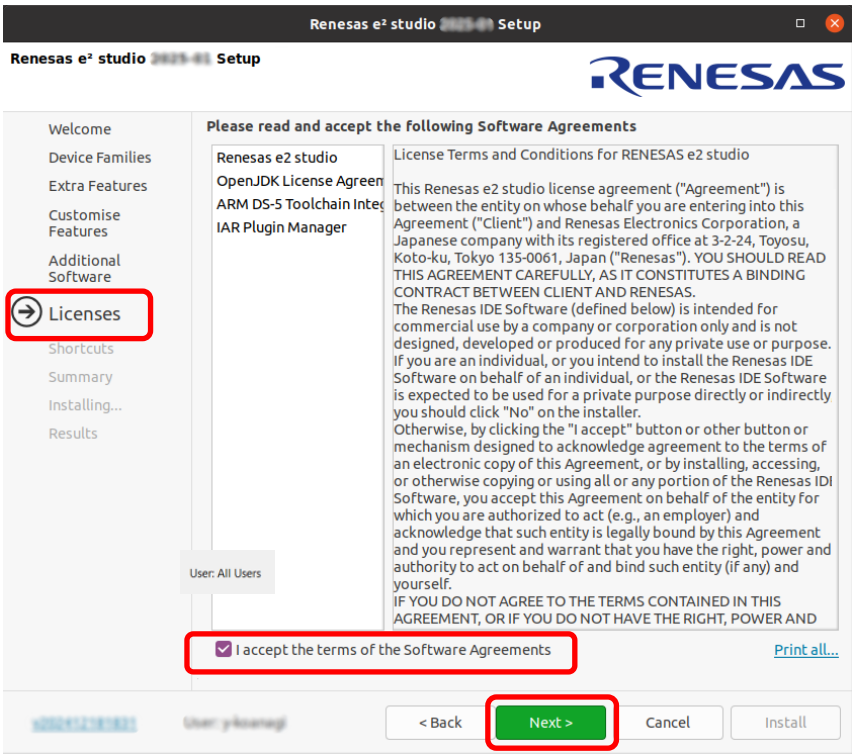


Figure 6.24 Installation of e² studio – Licenses

9. "Shortcuts"
   Check "In the Application launcher" to register for the launcher and click [Next] button to continue.

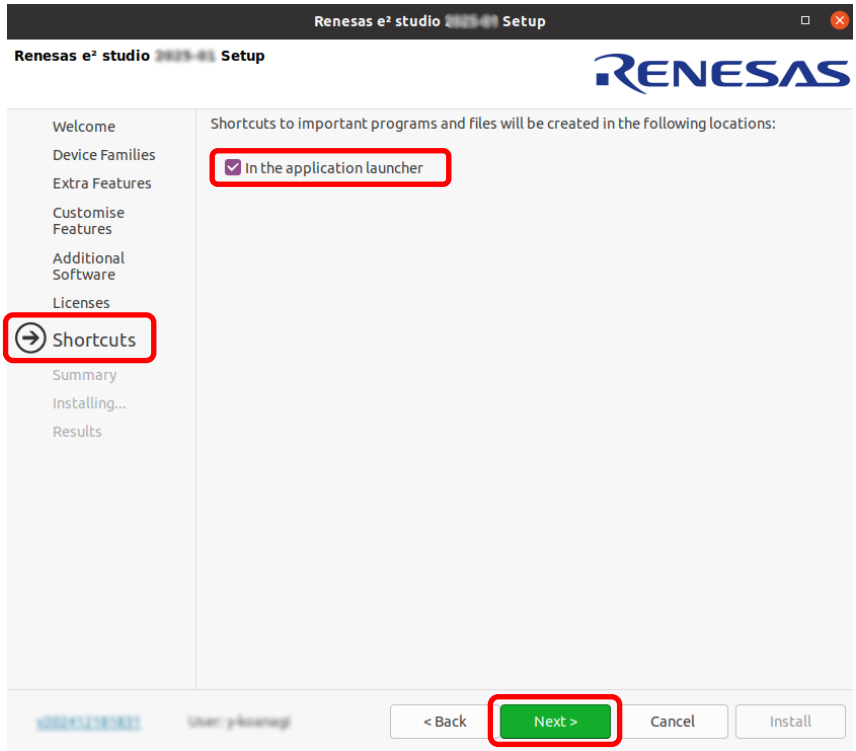


Figure 6.25 Installation of e² studio – Shortcuts

10."Summary"

Components list to be installed is shown.

Please confirm the contents and click the [Install] button to install the Renesas e² studio IDE.

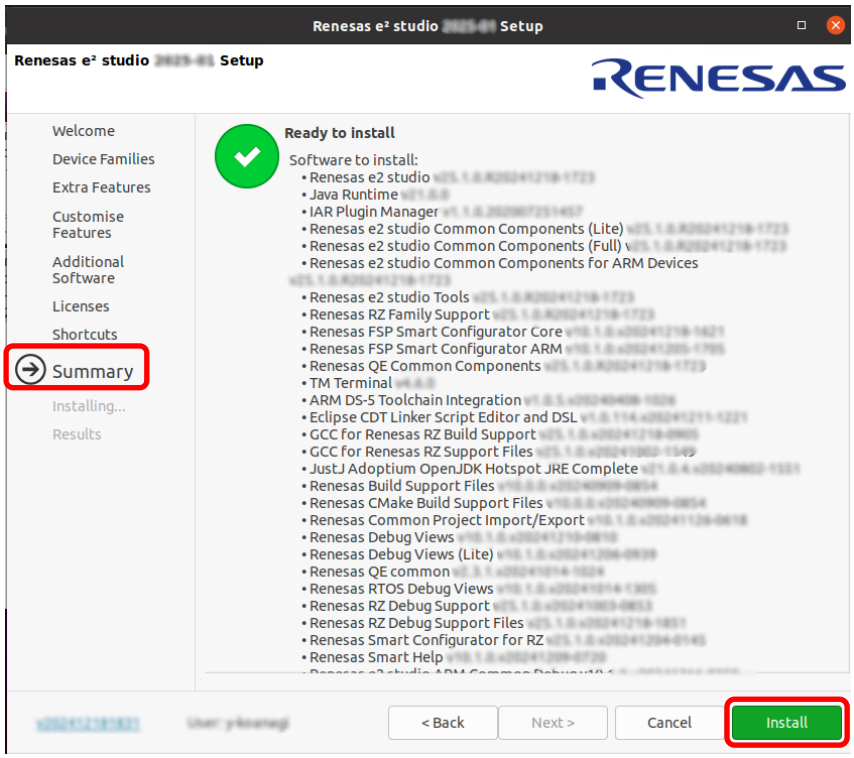


Figure 6.26 Installation of e² studio – Summary

11."Installing"

The installation is performed. Depending on selected items of additional software, new dialog prompts may appear during the installation process.

12."Results"

Click the [OK] button to complete the installation.

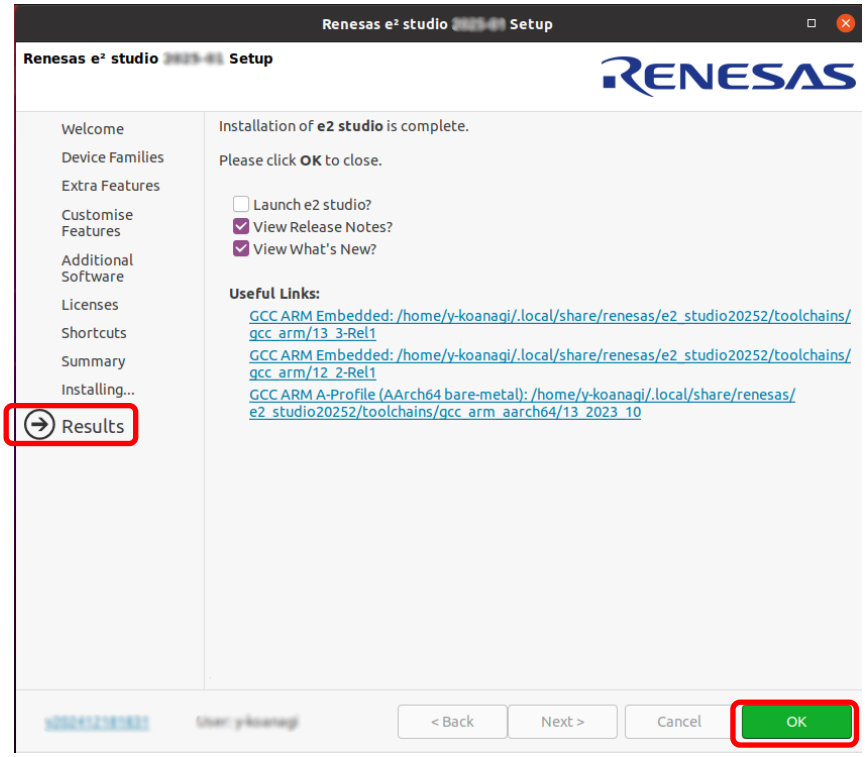


Figure 6.27 Results Page

6.2.1.2 Installation of RZ/A FSP packs (ubuntu 22.04 LTS)

Install the FSP packs for use in the RZ/A3 IPL environment.

1. Exit e² studio
2. Extract FSP Packs.
3. Copy the extracted FSP Packs (named "internal") to the e² studio installation folder as shown below:
   "~/.local/share/Renesas/e2_studio/internal/projectgen/rz_fsp/rza/packs"

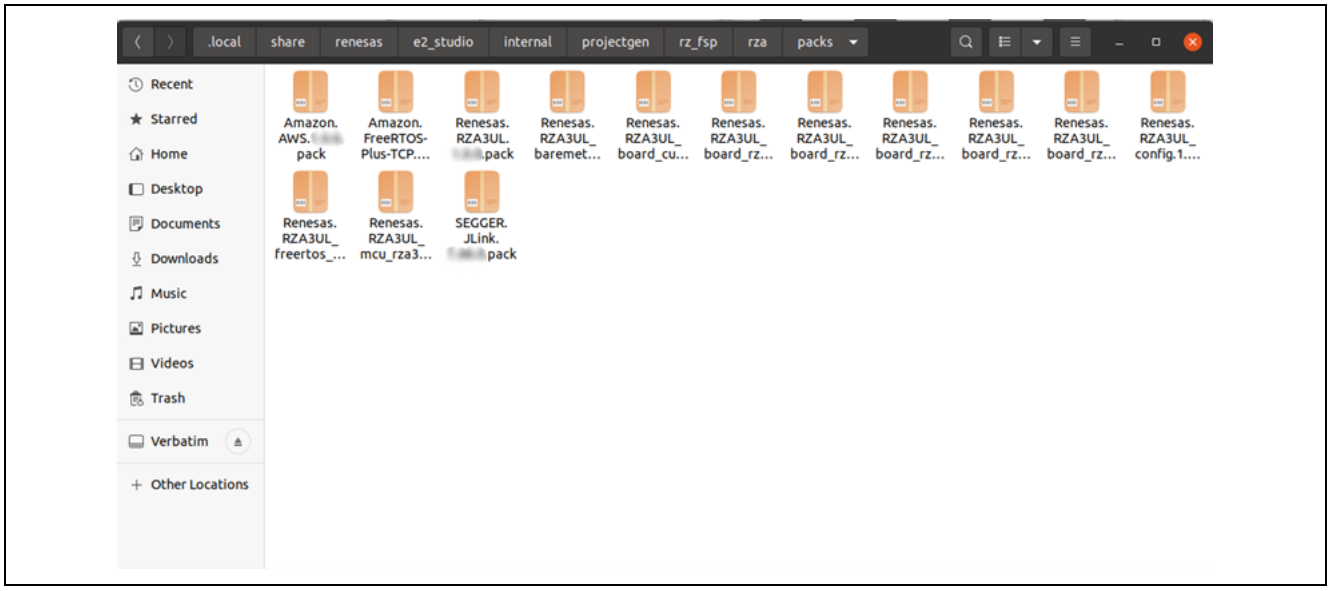


Figure 6.28 Installed packs folder (Ubuntu 22.04 LTS)

4. Please re-launch e² studio
   Then packs will be reflected in the development environment.

6.2.2 Additional Software Installation

You must install some additional software to build the IPL in ubuntu 22.04 LTS.

1. Execute the following command to install libncurses5.

```
$ sudo apt-get install libncurses5 libncurses5:i386
```

2. Download the Segger J-Link driver file from the "Linux" -> "64-bit DEB installer" link on the following website.

   https://www.segger.com/downloads/jlink/

3. Execute the following command to install driver file.
   The command is an example when the name of the driver file is "JLink_Linux_V810a_x86_64 .deb ".
   Change the argument according to the file name.

```
$ sudo dpkg -i JLink_Linux_v810a_x86_64.deb
```

   If you get unmet dependencies error, please do the following.

```
$ sudo apt-get -f install
$ sudo dpkg -i JLink_Linux_v810a_x86_64.deb
```

4. If your PC does not have libpython3.10 installed, install it.

```
$ sudo apt-get install libpython3.10
```

7. IPL build environment construction procedure

This chapter describes the procedure for building the IPL build environment for RZ/A3UL.

The procedure is the same for both Windows 10 version and Ubuntu 22.04 LTS version.

1. Get the IPL source code from the GitHub page shown below.
   This document shows an example when the obtained source code is saved in "C:\work\RZA3UL_IPL".
   (Please notice that the build might fail if the folder's path is too long.)
   renesas/rza-initial-program-loader (github.com)

2. Launch e² studio.
   Click [Browse] and specify "C:\work" for the workspace on e² studio launcher

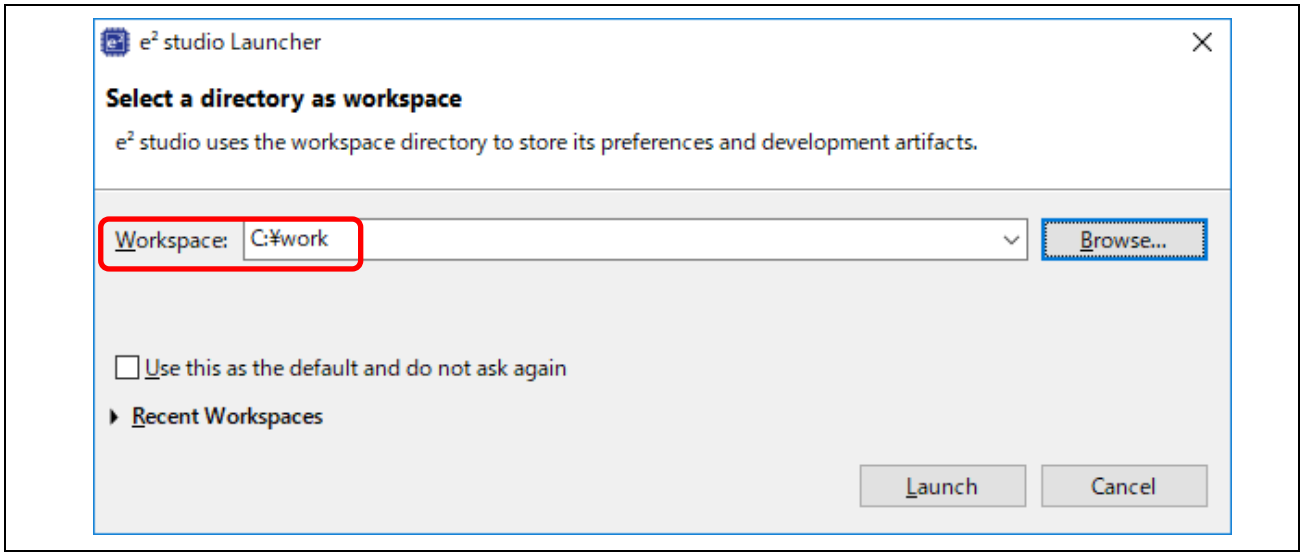


Figure 7.1 Launch e² studio (1)

3. In the Logging/Reporting dialog that is displayed when e² studio is started.
   Please confirm the descriptions, put a check to description that match your privacy policy, and click [Apply].

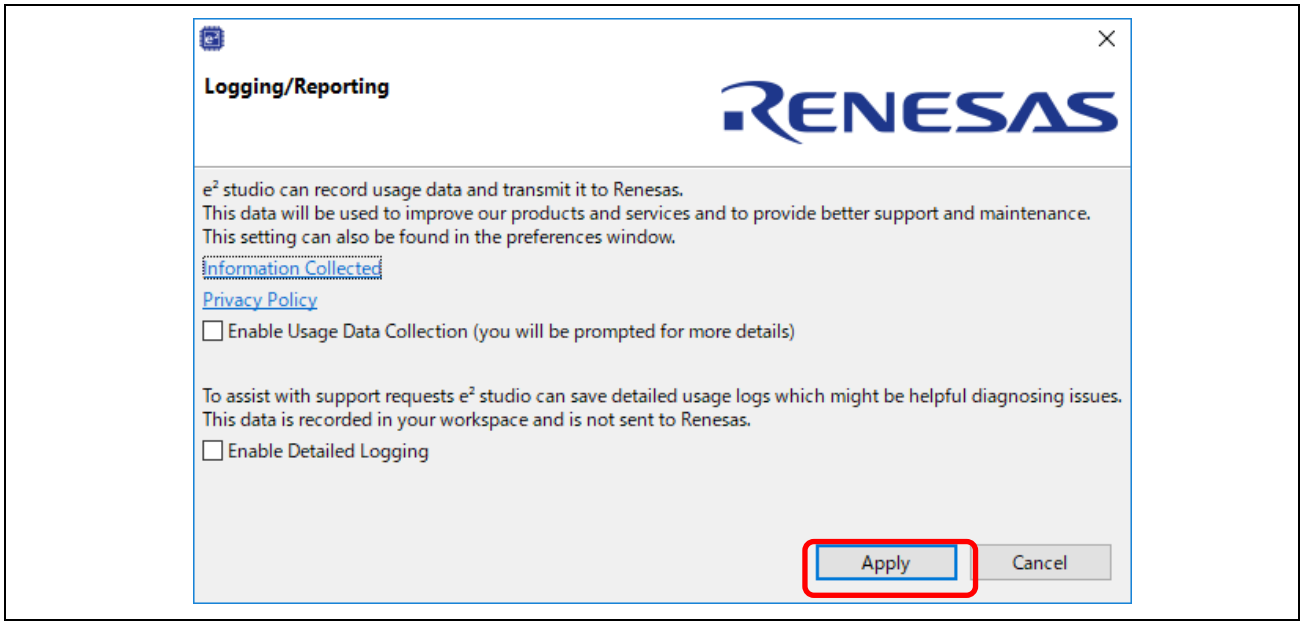


Figure 7.2 Launch e² studio (2)

4. When e² studio starts, click [Hide] to bring up the main window.

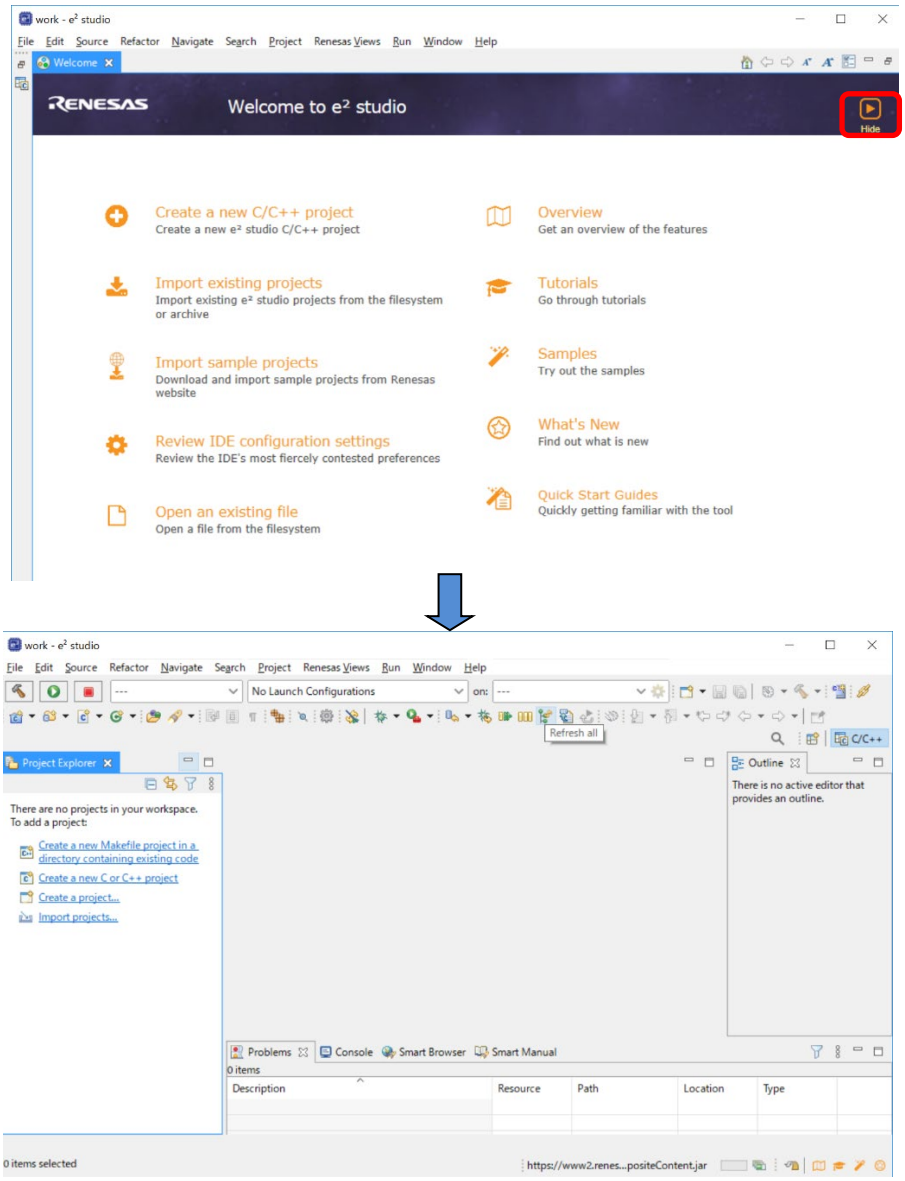


Figure 7.3 Launch e² studio (3)

5. Click [File] -> [New] -> [Makefile Project with Existing Code] in main window.

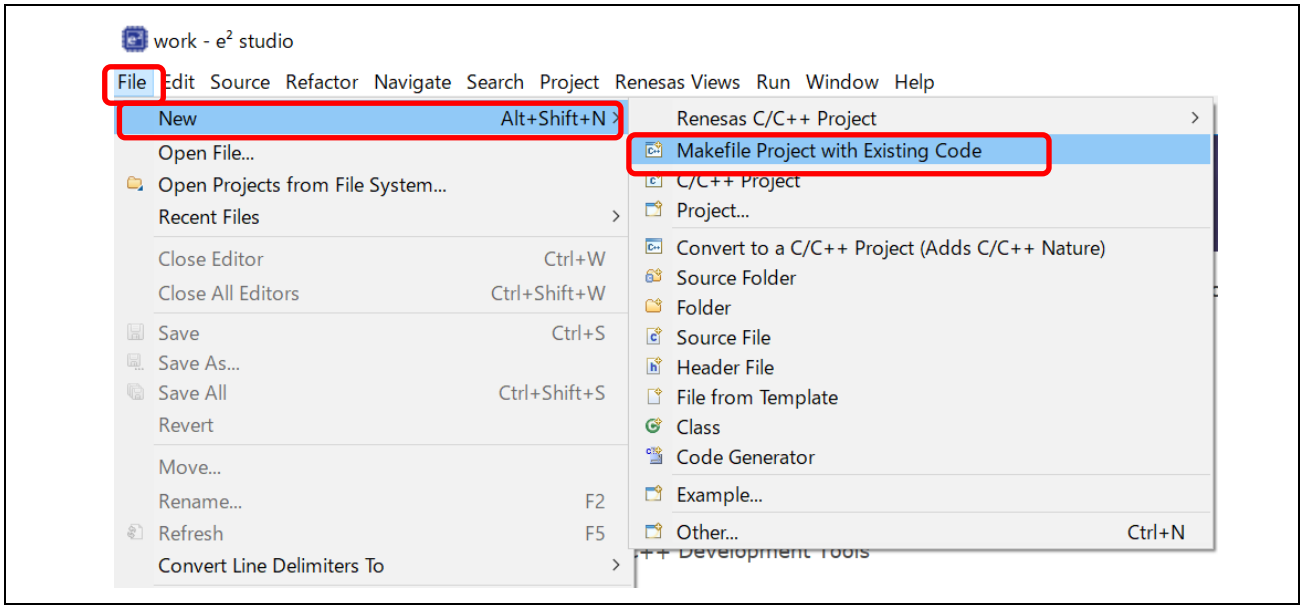


Figure 7.4 Create project (1)

6. Click Browse and choose "C:\work\RZA3UL_IPL", the folder where you unzipped the IPL.
   Then the folder path will be registered in the Existing Code Location field.
7. Select [GCC for Renesas RZ (A-Profile AArch64 bare-metal)] in the Toolchain for Indexer Settings and click [Finish].

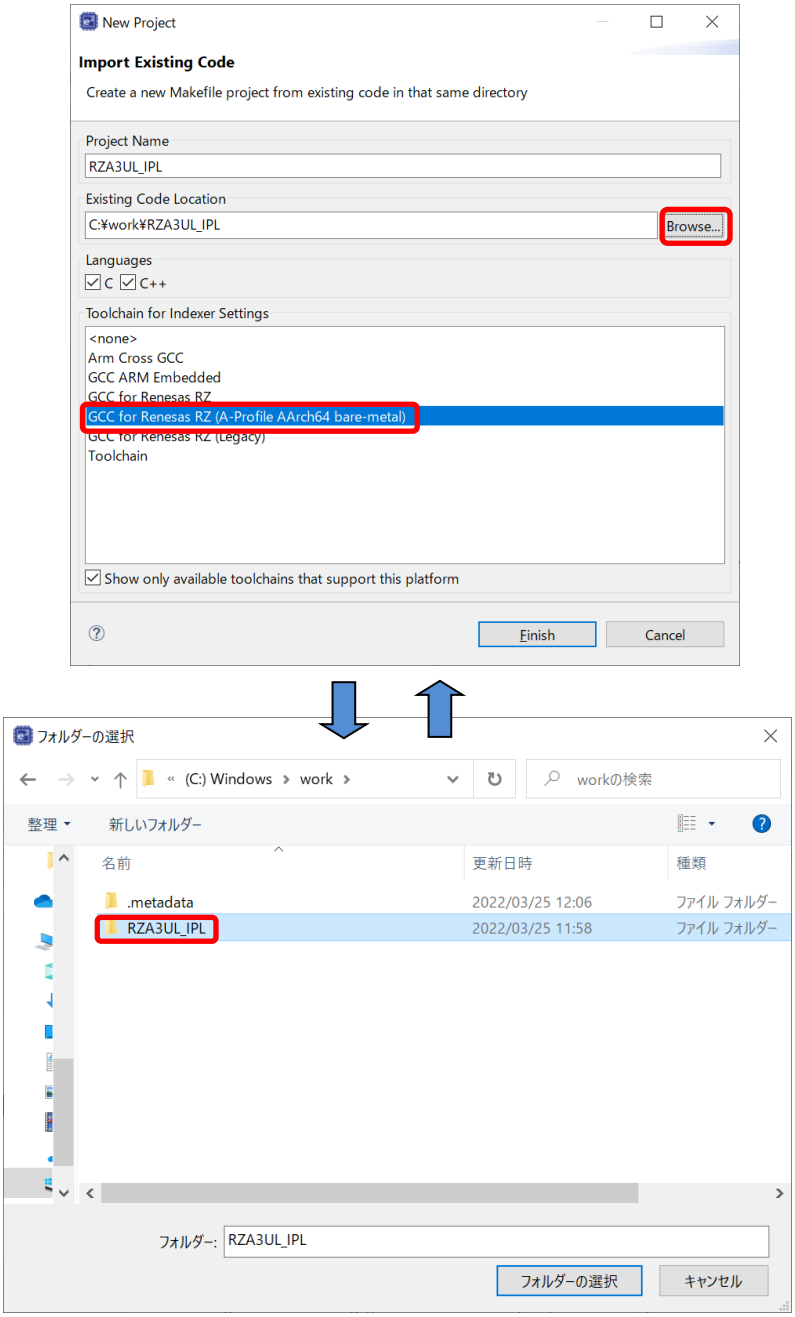


Figure 7.5 Create project (2)

8. Right-click the [RZA3UL_IPL] project generated in Project Explorer and click [Properties].

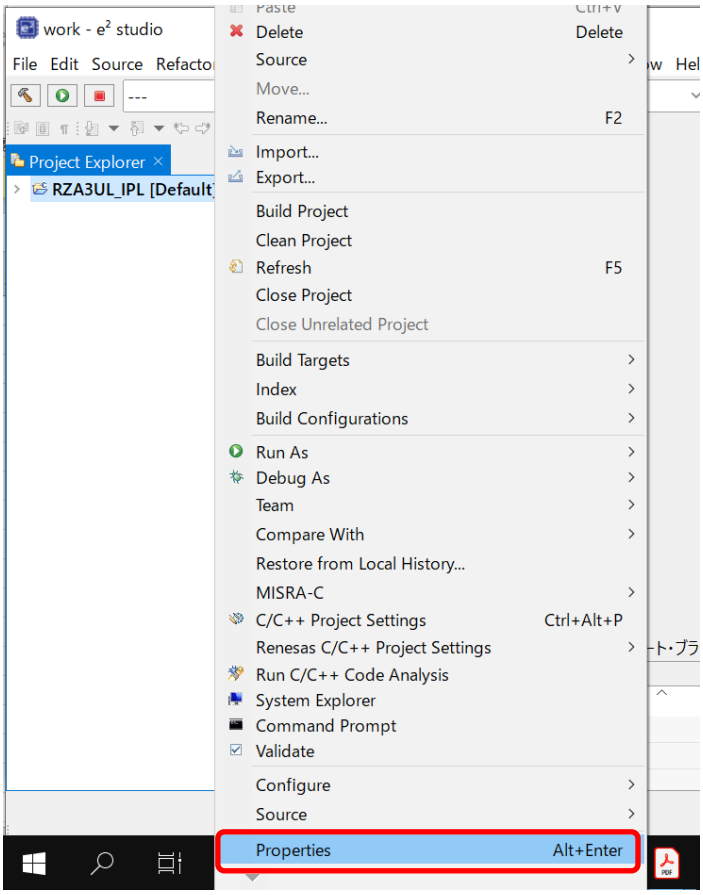


Figure 7.6 Create project (3)

9. Open [C / C ++ Build] -> [Tool Chain Editor] in Properties for [RZA3UL_IPL] and enter the build command.
   Select [GNU Make Builder] in "Current Builder", then click [Apply and Close].

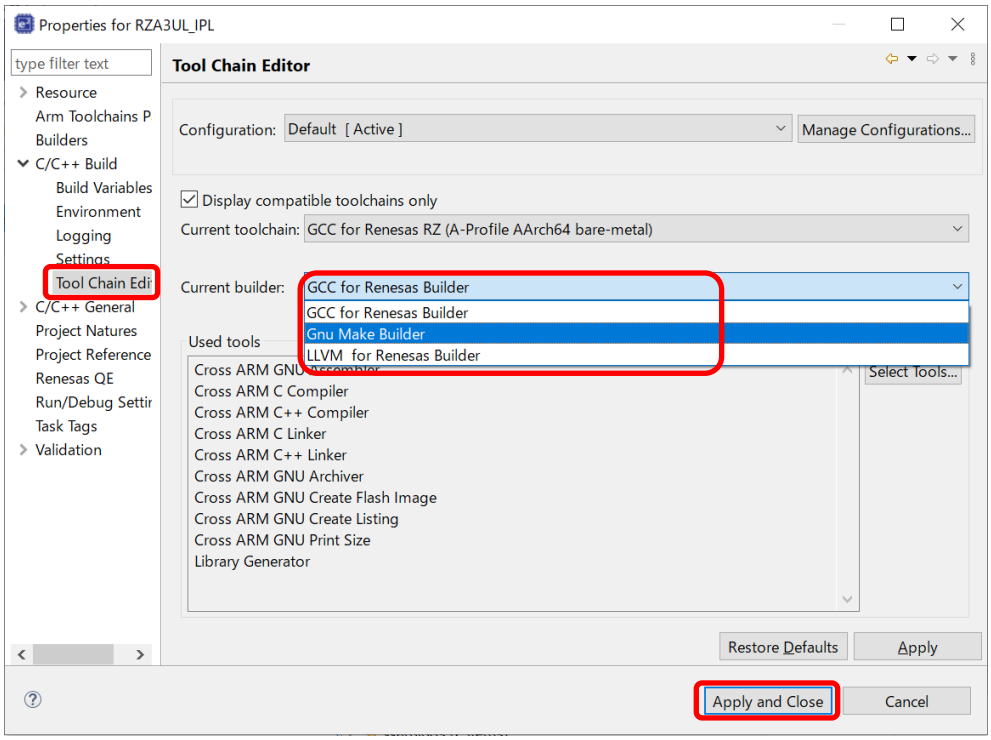


Figure 7.7 Create project (4)

10. Open [C/C ++ Build] -> [Behavior] in Properties for RZA3UL_IPL and enter the build command.
    Check "Use custom build arguments" and set the make option "PLAT=a3ul BOARD=a3ul_smarc_qspi" in the "Build arguments" field, so build and clean will execute with the same make option.
    If you want to use different make options for build and clean, set the make options in the "Build" and "Clean" fields respectively.
    Then click [Apply].

Notes: 1. Options can be added and changed.
They are explained in the Table 7.1.
2. This description is the setting when the same make option is specified for Build and Clean.
If you want to use different make options for build and clean, set the make options in the "Build" and "Clean" fields respectively.

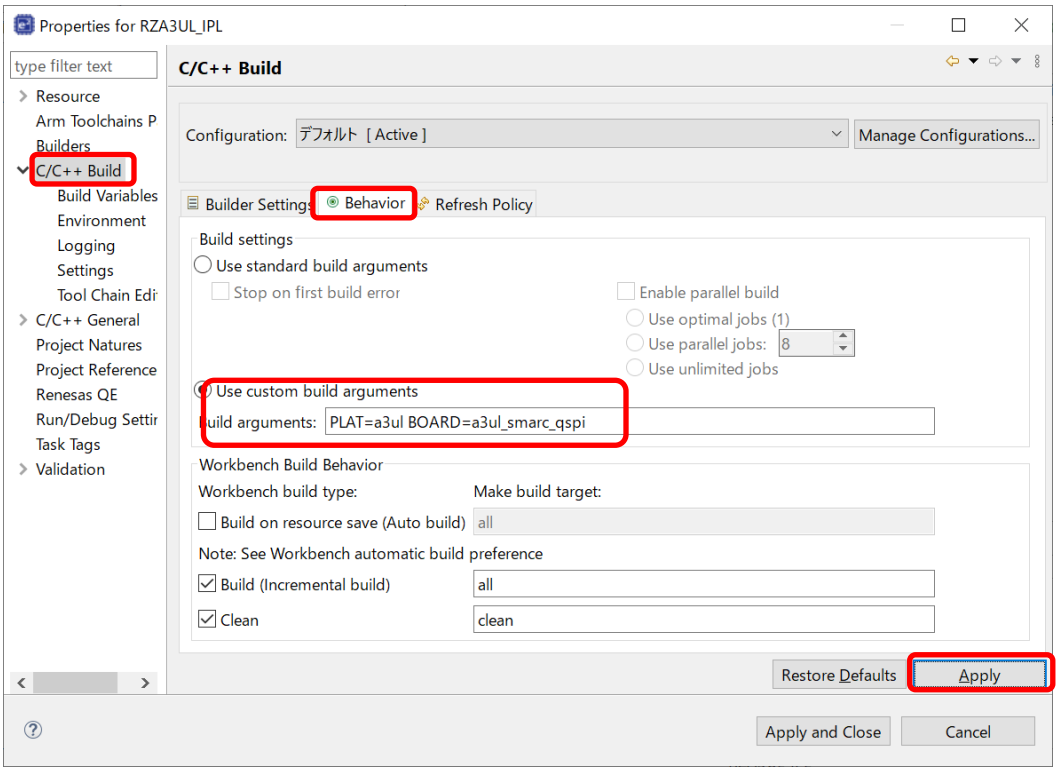


Figure 7.8 Build Command

Table 7.1 Make Option

Name	Explanation	Setting Example
PLAT	Set the platform This option cannot be omitted	a3ul: for RZ/A3UL, this option can't be changed
BOARD	Set the board This option cannot be omitted	a3ul_smarc_qspi: RZ/A3UL-Evaluation-Board-Kit (QSPI version)
DEBUG	Select debug/release build	1: debug build 0: release build This option can be omitted. In that case a release build is executed.
FSP_BASE	Indicates the start address of the application header	0x20020000 If you do not set this option, 0x20020000 is automatically set as the default value.

11. Open [C / C ++ Build]-> [Environment] in Properties for [RZA3UL_IPL] and enter the Environment variables.
    When you click [Add], the new variable window will appear.
    Set the environment variables of the combinations shown in the Table 7.2 (Windows10) or Table 7.3 (Ubuntu 22.04 LTS) in the Name and Value fields, then click [Apply].

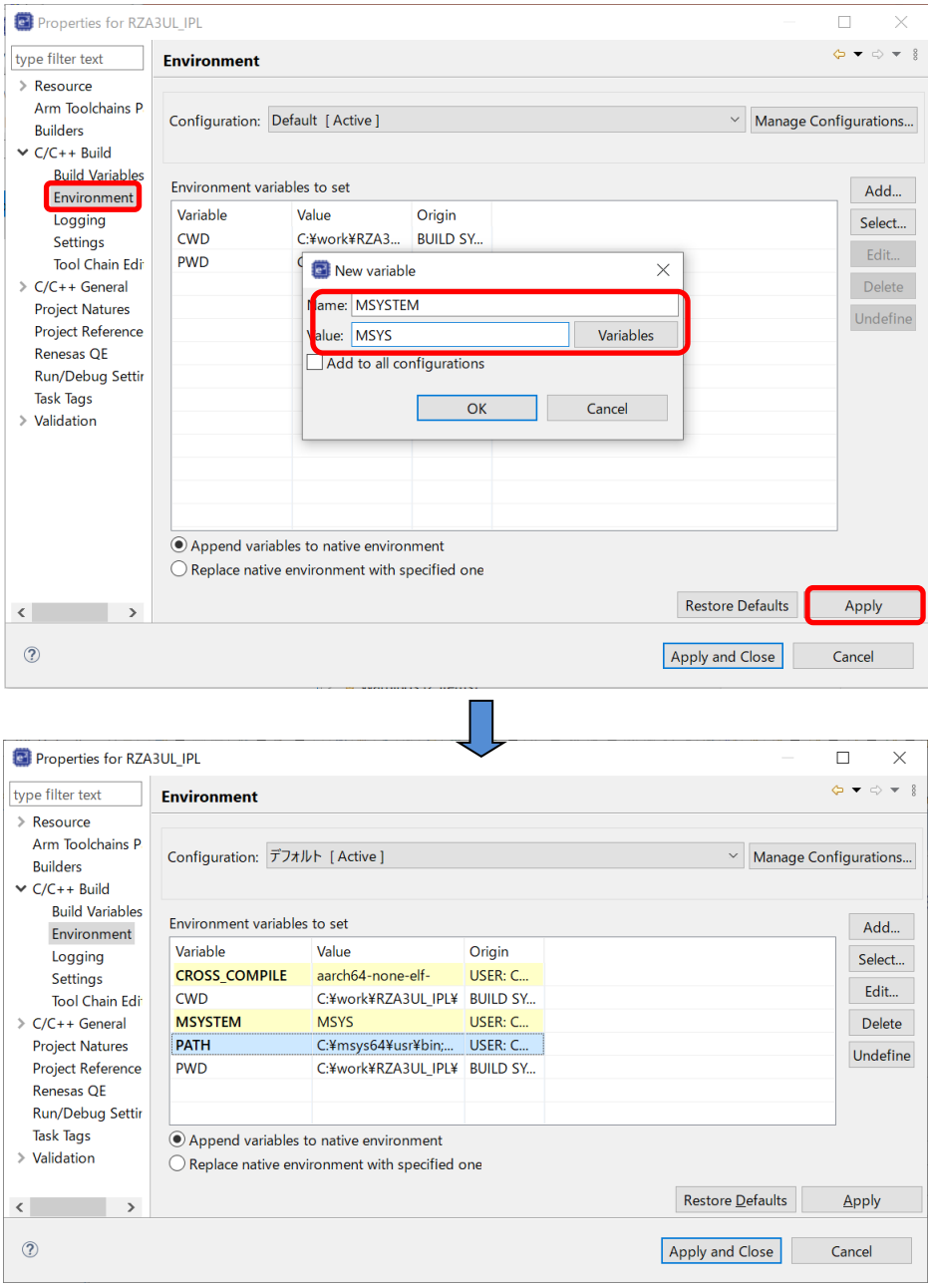


Figure 7.9 Build Environment

Table 7.2 Environment Variables (Windows10 PC)

Name	Value
CROSS_COMPILE	aarch64-none-elf-
MSYSTEM	MSYS
PATH	C:\msys64\usr\bin;C:\Renesas\e2studio\toolchains\gcc_arm_aarch64\10_2021_07\gcc-arm-10.3-2021.07-mingw-w64-i686-aarch64-none-elf\bin (Notes1, 2)

Notes: 1. Chane value to match the MSYS2 installation folder.
2. Toolchain will be installed under the e² studio installation folder.
Please set the path to that folder.

Table 7.3 Environment Variables (Ubuntu 22.04 LTS PC)

Name	Value
CROSS_COMPILE	aarch64-none-elf-
PATH	/home/username/.local/share/renesas/e2_studio/toolchains/gcc_arm_aarch64/10_2021_07/gcc-arm-10.3-2021.07-x86_64-aarch64-none-elf/bin (Note)

Note: Toolchain will be installed under the e² studio installation folder.
Please set the path to folder.

12.Right-click [RZA3UL_IPL] and click [Build Project] to run the build.
If you want to clean it, click [Clean Project].

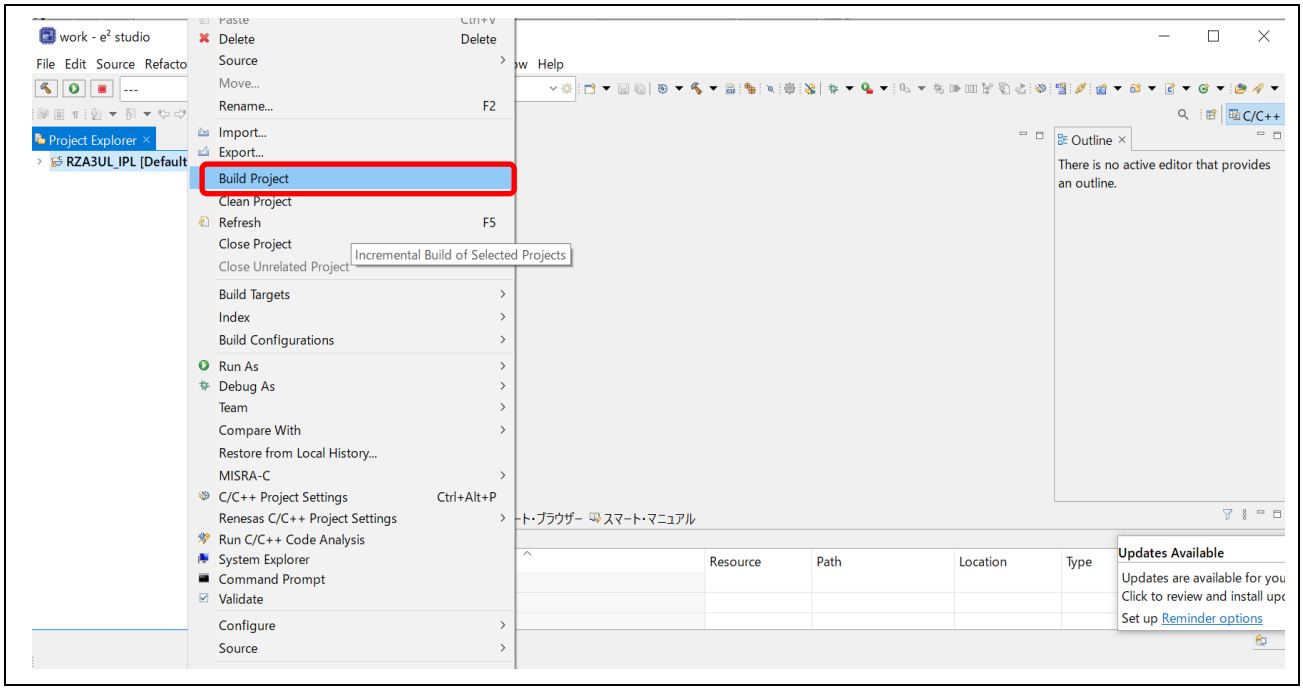


Figure 7.10 Build Environment

If the build is successful, the following files will be generated in "RZA3UL_IPL\build\a3ul\release".

rza3ul_smarc_qspi_ipl.dump:
This file shows the disassembled data of the IPL code.

rza3ul_smarc_qspi_ipl.map:
Map file of IPL.

rza3ul_smarc_qspi_ipl.bin:
Raw Binary image of IPL.

rza3ul_smarc_qspi_ipl.elf:
Executable file of IPL.
It is used to download and run the IPL to On-chip RAM in e² studio.

rza3ul_smarc_qspi_ipl.srec:
Motorola S format file of IPL.
By writing to the Serial Flash memory, automatic boot is performed when the SMARC EVK board is reset.
The IPL write destination address (H'2000_0000) is registered in this file itself.
When using the download function of e² studio, the registered address is referenced and written to the memory, so the offset address specified in e² studio is H'0000_0000.
When writing an IPL to the board using Flash Writer, specify the write destination offset address according to specification of it.

bl2.bin、rz_bl2_xspi.env、rz_bl2_xspi_def.c:
Temporary file when building

8. Execution Environment of IPL

8.1 Create Debug Configuration

This chapter shows how to create a Debug configuration to run IPL for RZ/A3UL.

The procedure is the same for both Windows 10 version and Ubuntu 22.04 LTS version.

1. Right-click on RZA3UL_IPL and select [Debug AS] -> [Debug Configurations].

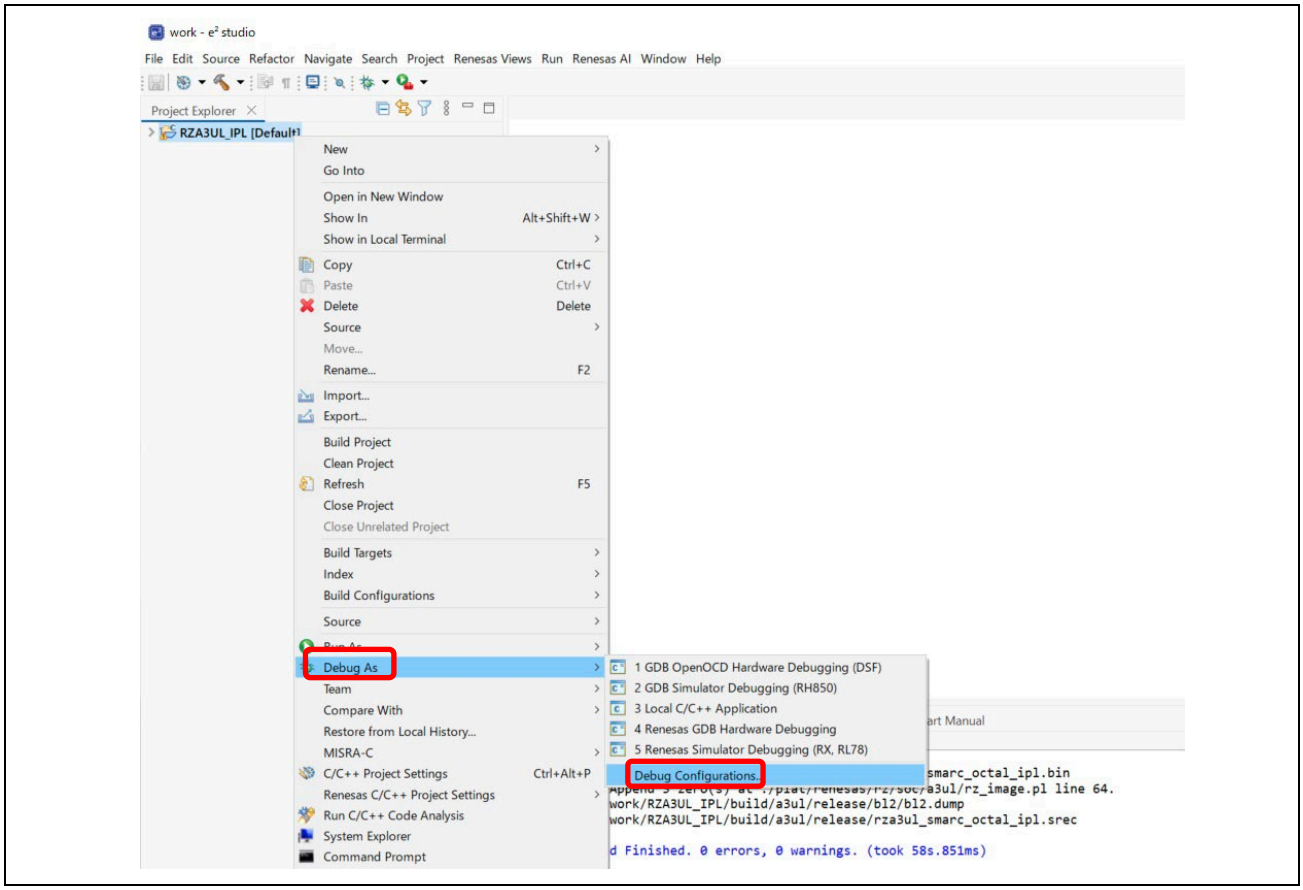


Figure 8.1 Create Debug Configuration (1)

2. In the "Debug Configurations" window, double-click [Renesas GDB Hardware Debugging] to create a Debug Configuration template for the RZA3UL_IPL.

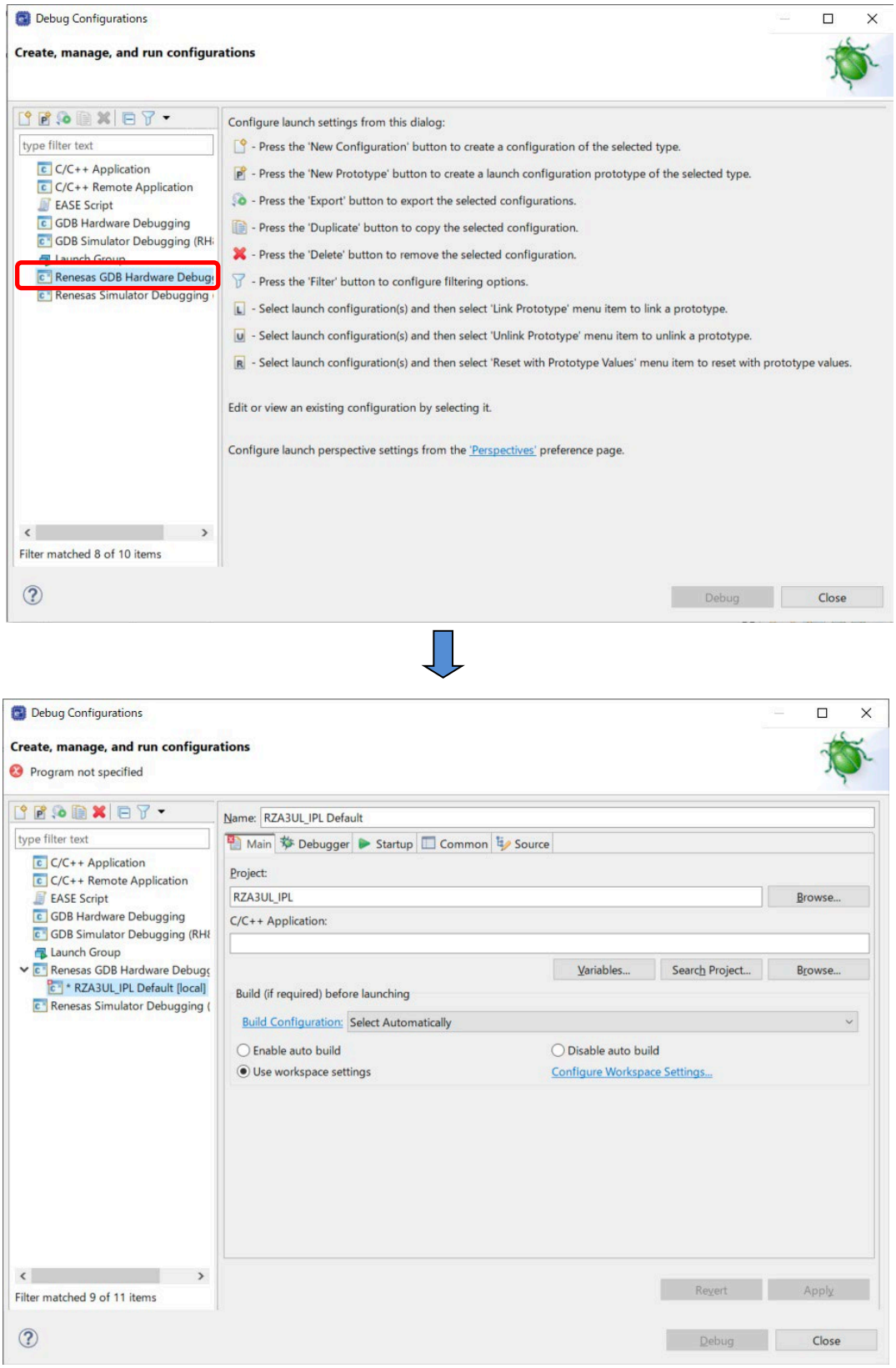


Figure 8.2 Create Debug Configuration (2)

3. Add device connection settings to the debug configuration template for RZA3UL_IPL.
   Click [Search Project] on the Main tab and select [rza3ul_smarc_qspi_ipl.elf] on the Program Selection window.
   Furthermore, after selecting "Use Active" in [Build Configuration], click [Apply].

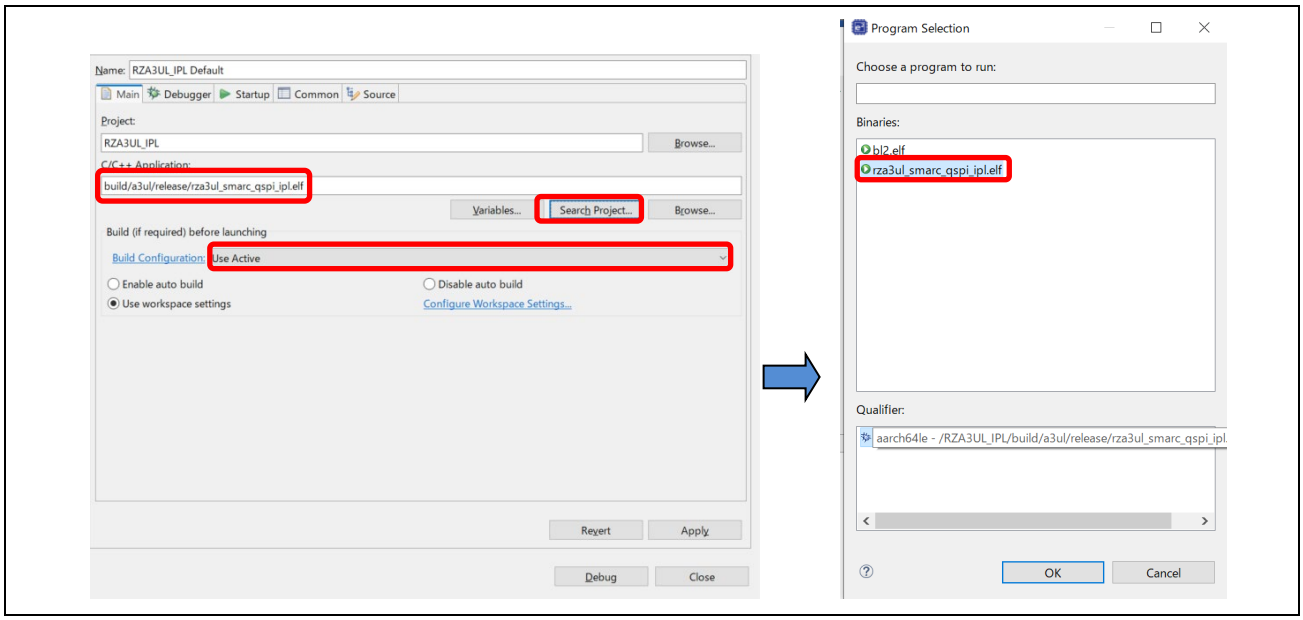


Figure 8.3 Create Debug Configuration (3)

4. Go to the [Debugger] tab.
   Select [J-Link ARM] in the Debug Hardware field.
   Click […] next to Target Device and select [RZ/A3UL] -> [R9A07G063U02GBG] on the Device Selection window.
   Currently, set "aarch64-elf-gdb" in the GDB command field of the GDB settings tab.

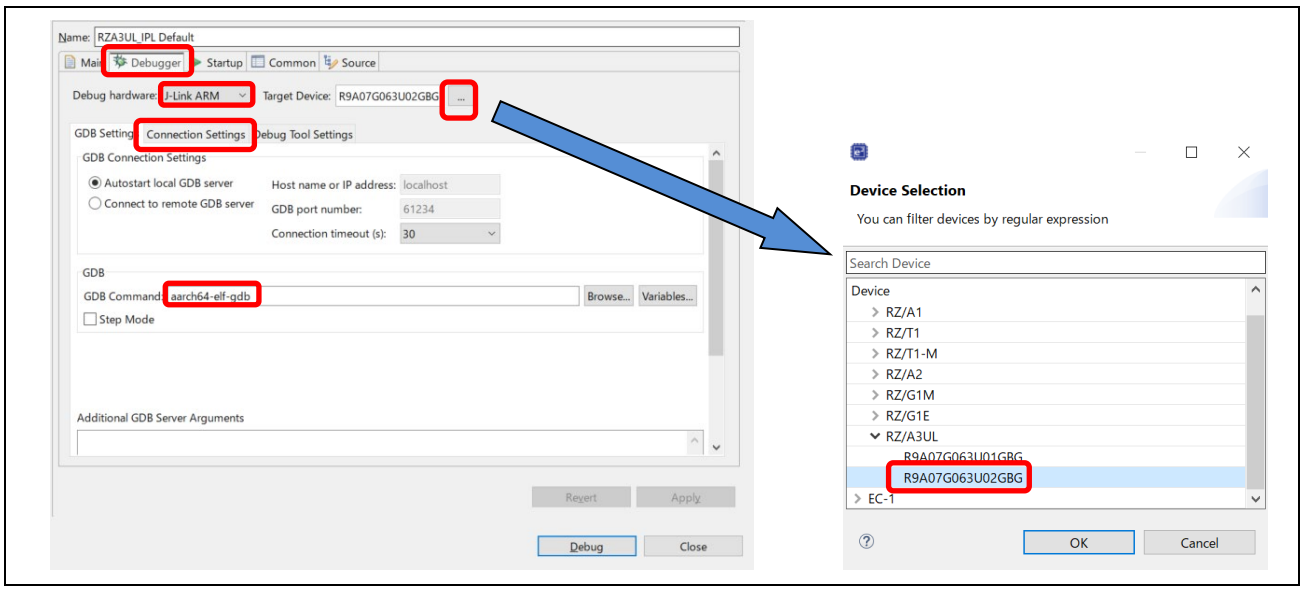


Figure 8.4 Create Debug Configuration (4)

5. Go to the "Debugger" -> "Connection Settings" tab.
   Set "Reset at the beginning of connection" to [Yes].
   If you use J-Link Lite, set SWD to [Type].
   If you use other J-Link models, please set [JTAG] or [SWD] to "Type" according to the specification.
   Then, set "Reset at the beginning of connection" to [Yes].

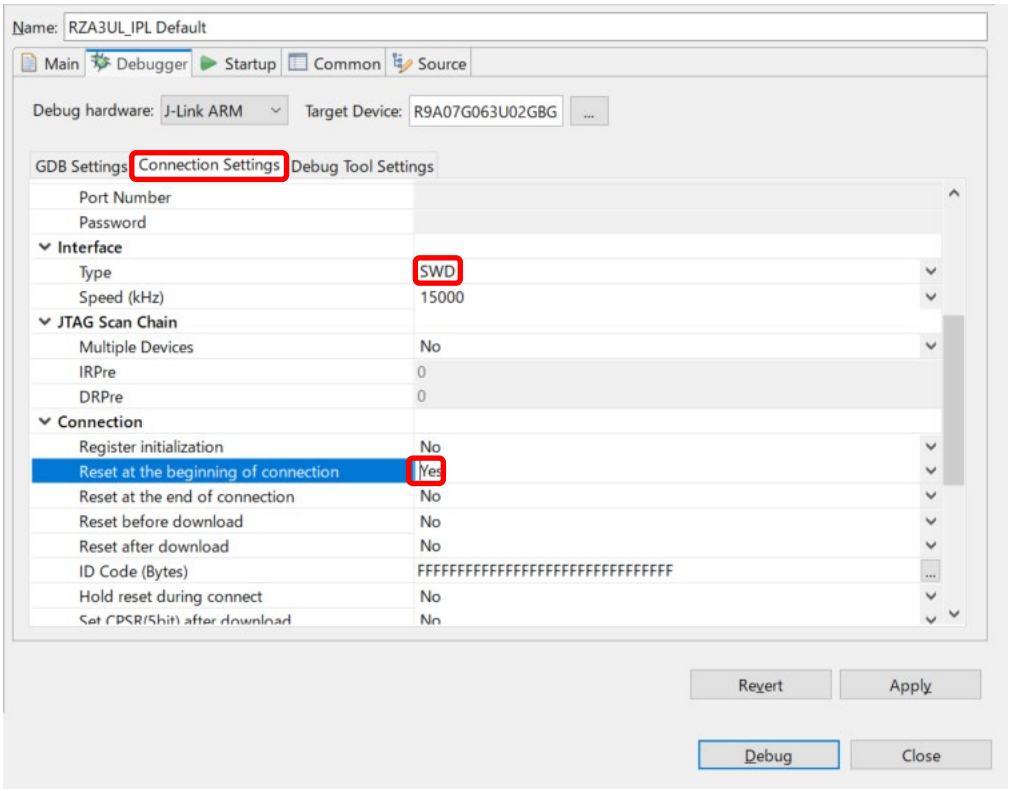


Figure 8.5 Create Debug Configuration (5)

6. Go to the "Debugger"-> "Debug Tool Settings" tab.
   Set "Reset After Reload" to [No].
   Set "Flash Bus Type" to [SPIBSC] and "Flash Memory Type" to [SerialFlash].
   Set "Run Break Time Measurement" to [No].

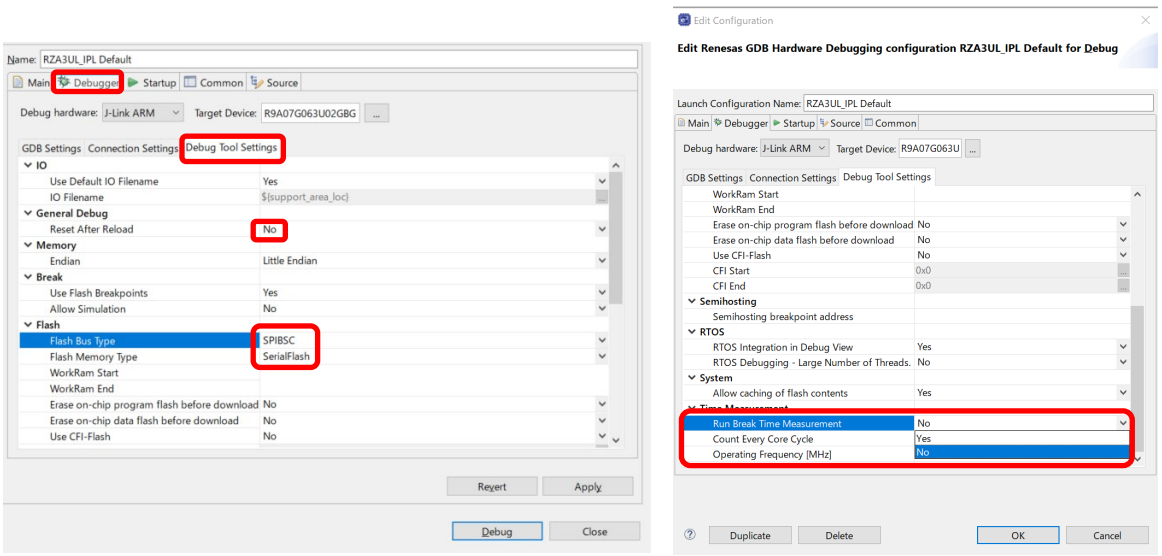


Figure 8.6 Create Debug Configuration (6)

7. Go to "Startup" tab
   Set "On connect" of "Program Binary" to [No].

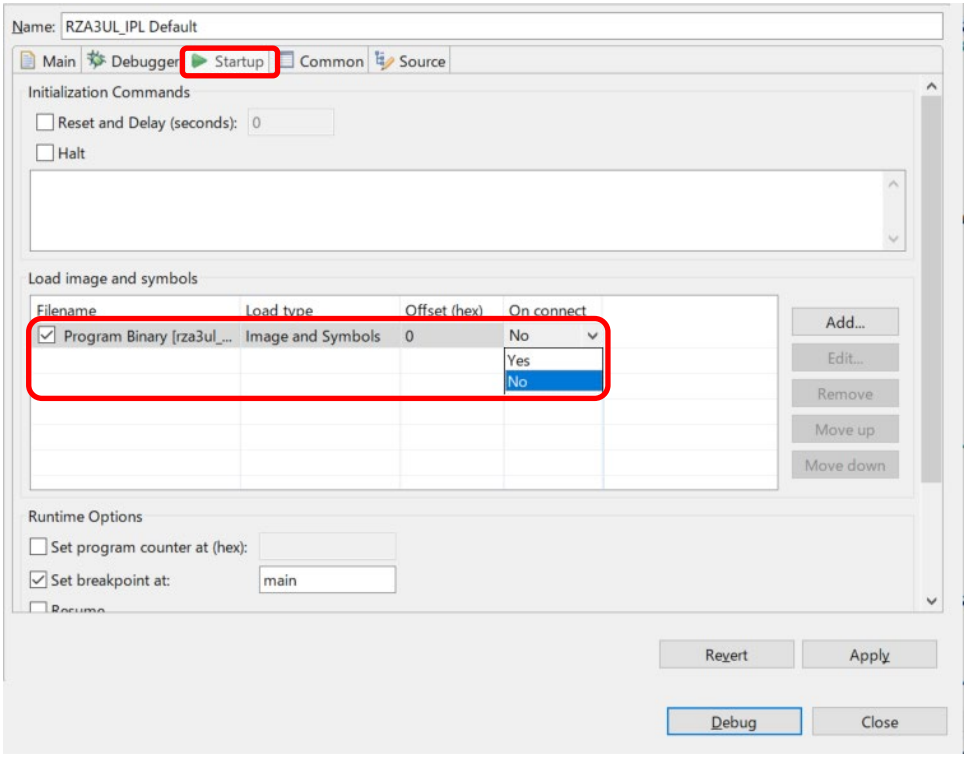


Figure 8.7 Create Debug Configuration (7)

8. Click [Add] to bring up the Add download module window.
   Next click [Workspace], select [RZA3UL_IPL\build\a3ul\release\rza3ul_smarc_qspi_ipl.srec], and then click [OK] to return.
   Then, rza3ul_smarc_qspi_ipl.srec is registered in Load image and symbols.

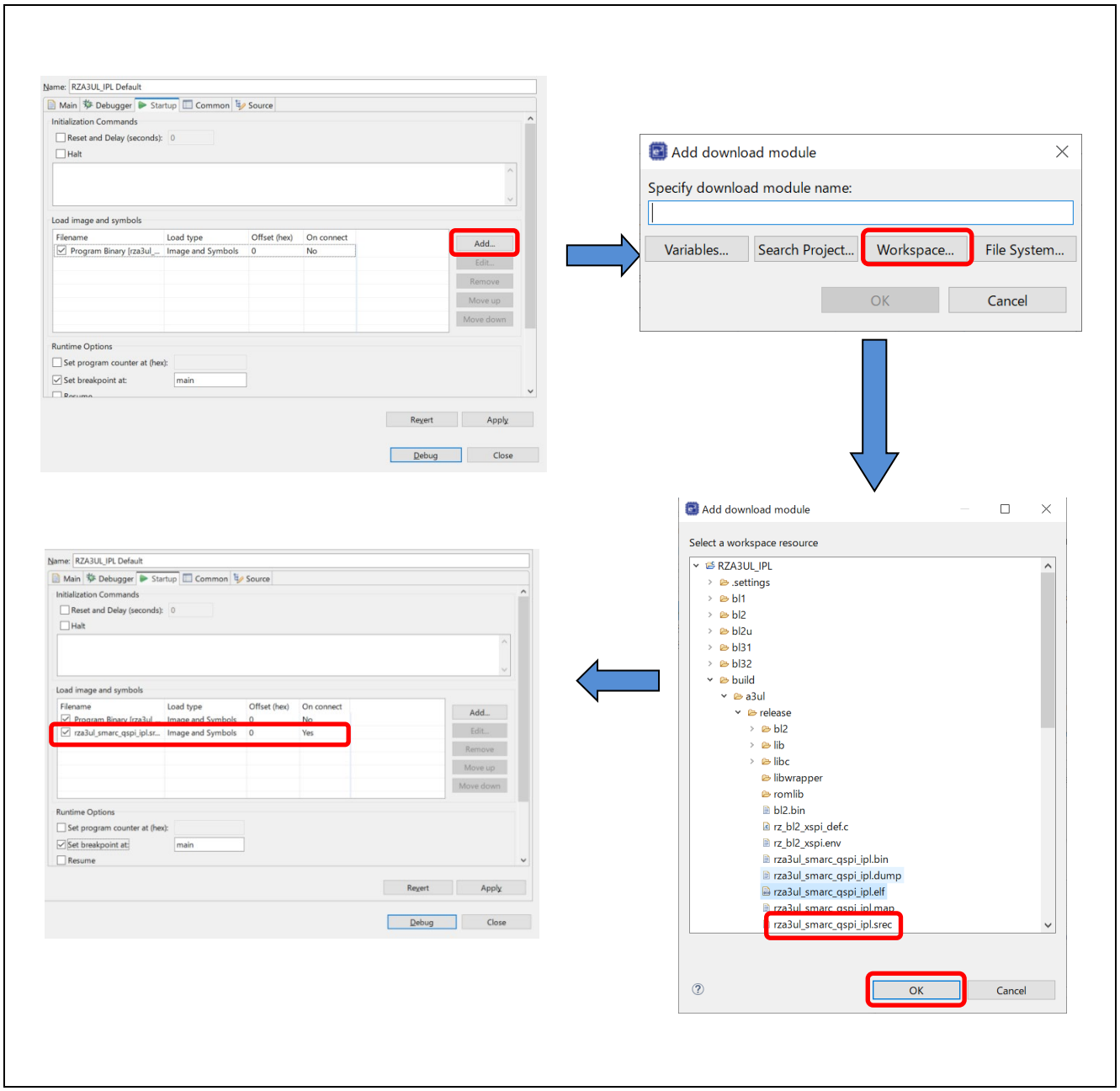


Figure 8.8 Create Debug Configuration (8)

9. Since the IPL write destination address H'2000_0000 is set in the registered rza3ul_smarc_qspi_ipl.srec itself, set [0] to "Offset(hex)".
   With this setting, the IPL image will be written to H'2000_0000 at the start of debugging.
   Also, set" On connect" to [No] and uncheck "Set breakpoint at".

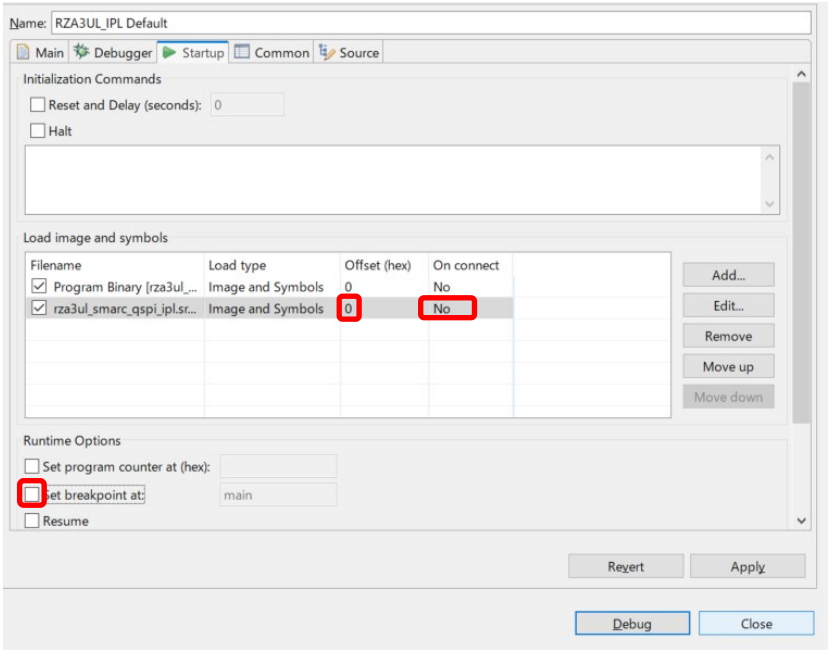


Figure 8.9 Create Debug Configuration of Serial Flash (9)

10.Go to the Common tab and set Save as to Share file:, and set the path to [\RZA3UL_IPL].
Also, uncheck "Launch in background".
After completing these settings, click [Apply] -> [Close] to complete the settings.

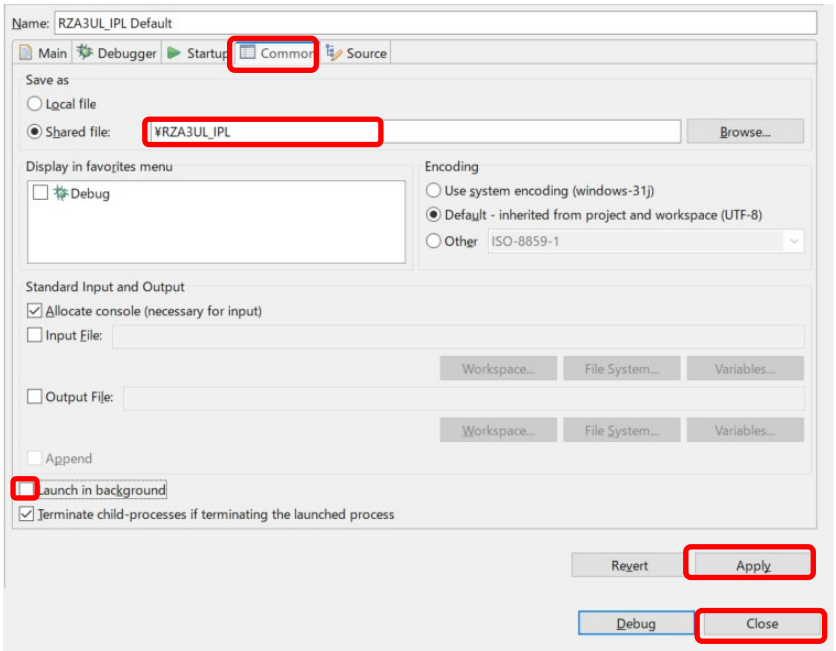


Figure 8.10 Create Debug Configuration (10)

8.2 Connection to SMARC EVK Board

Describes how to connect to the SMARC EVK board.

Figure 8.11 shows the appearance of the SMARC EVK board.

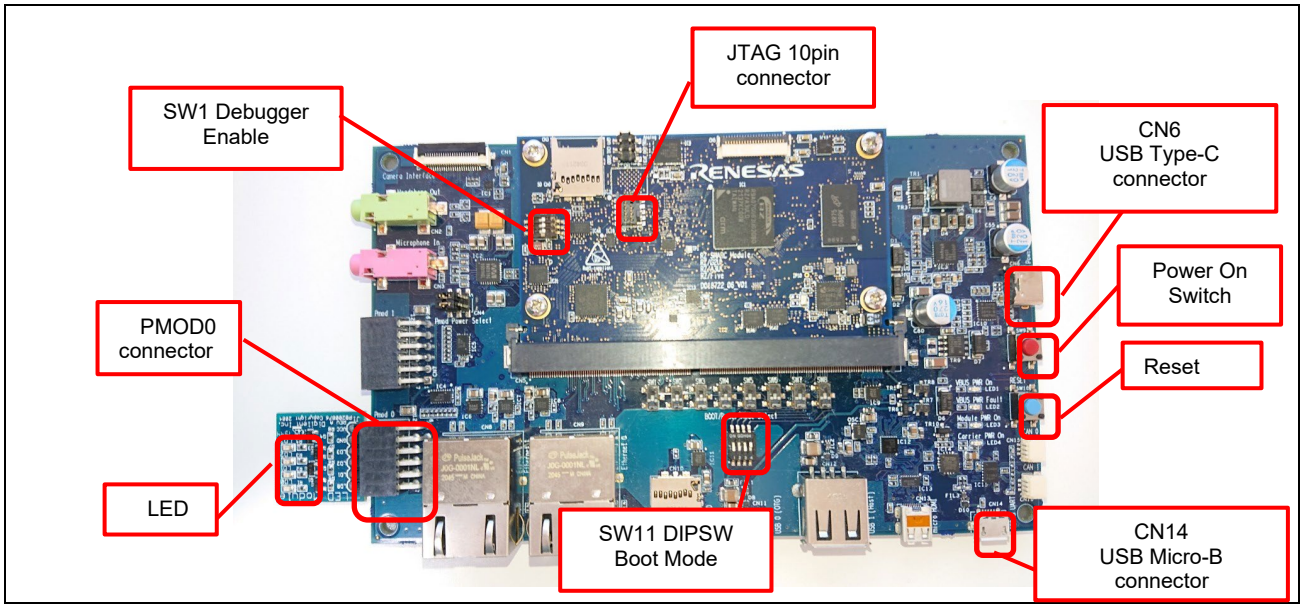


Figure 8.11 SMARC EVK Board

1. Connect the LED board to the PMOD0 connector.
   As shown in Figure 8.12, connect to terminals 7 to 12.

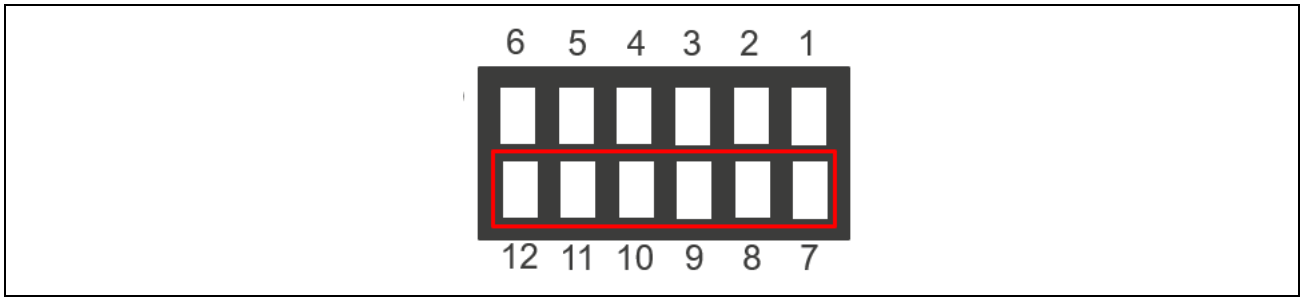


Figure 8.12 PMOD Connector

2. Connect CN14 and Windows 10 PC with a USB cable.
3. Connect J-Link Base 11.0 to the JTAG 10pin connector.
   In addition, connect J-Link Base 11.0 to the host PC with a USB cable.
4. Connect CN6 and USB-PD Power Charger.

5. Set SW1-1 to OFF as shown in Figure 8.13 to enable connectivity with the debugger.
   If you start the board without connecting to J-Link Base, set SW1-1 to ON.

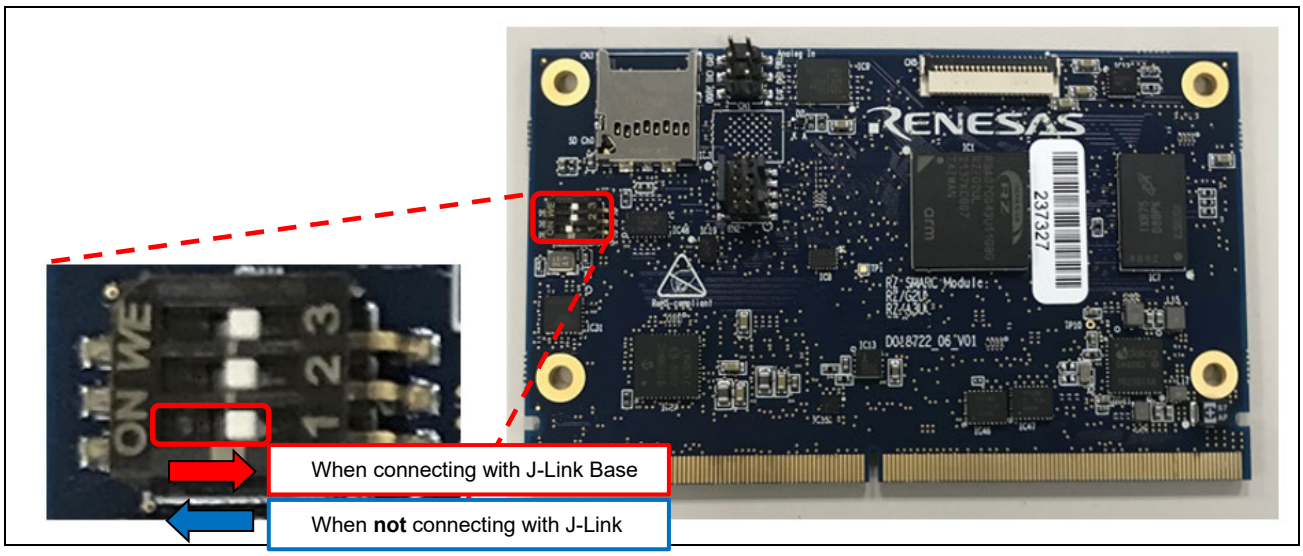


Figure 8.13 SW1 setting

6. Set Boot Mode to Boot Mode3 (1.8-V Serial Flash Memory) by setting SW11-1, SW11-2, SW11-3 as shown in Figure 8.14.

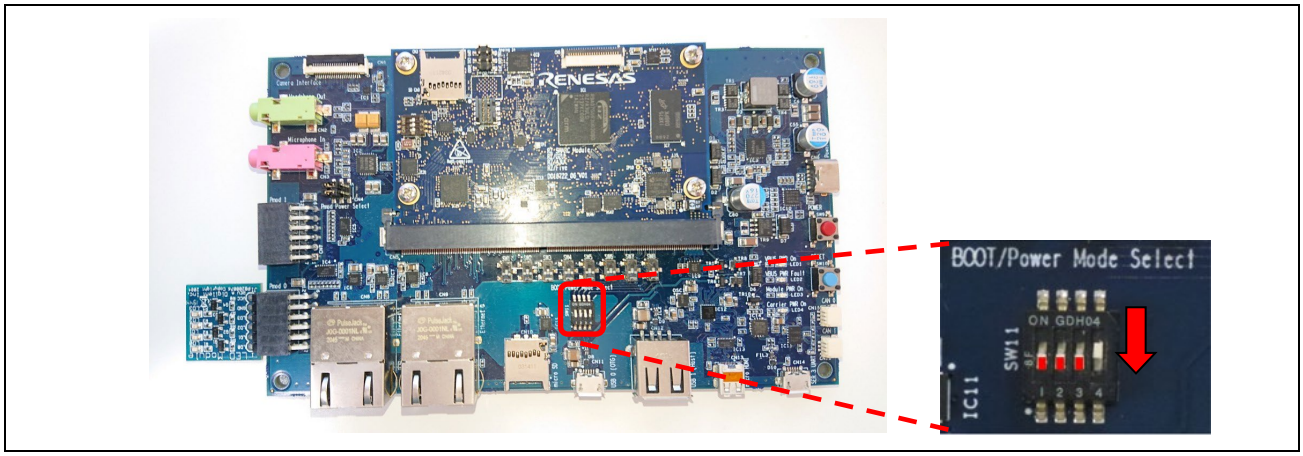


Figure 8.14 SW11 setting

8.3 Setting Serial Terminal

This section describes the procedure for setting the serial terminal to check the message output by IPL.

The procedure is the same for both Windows 10 version and Ubuntu 22.04 LTS version.

1. Set the SMARC EVK board operating mode to Boot Mode3 (1.8-V Serial Flash Memory) and turn on the power.
2. Launch e² studio.
3. Click [Window] -> [Show View] -> [Terminal].

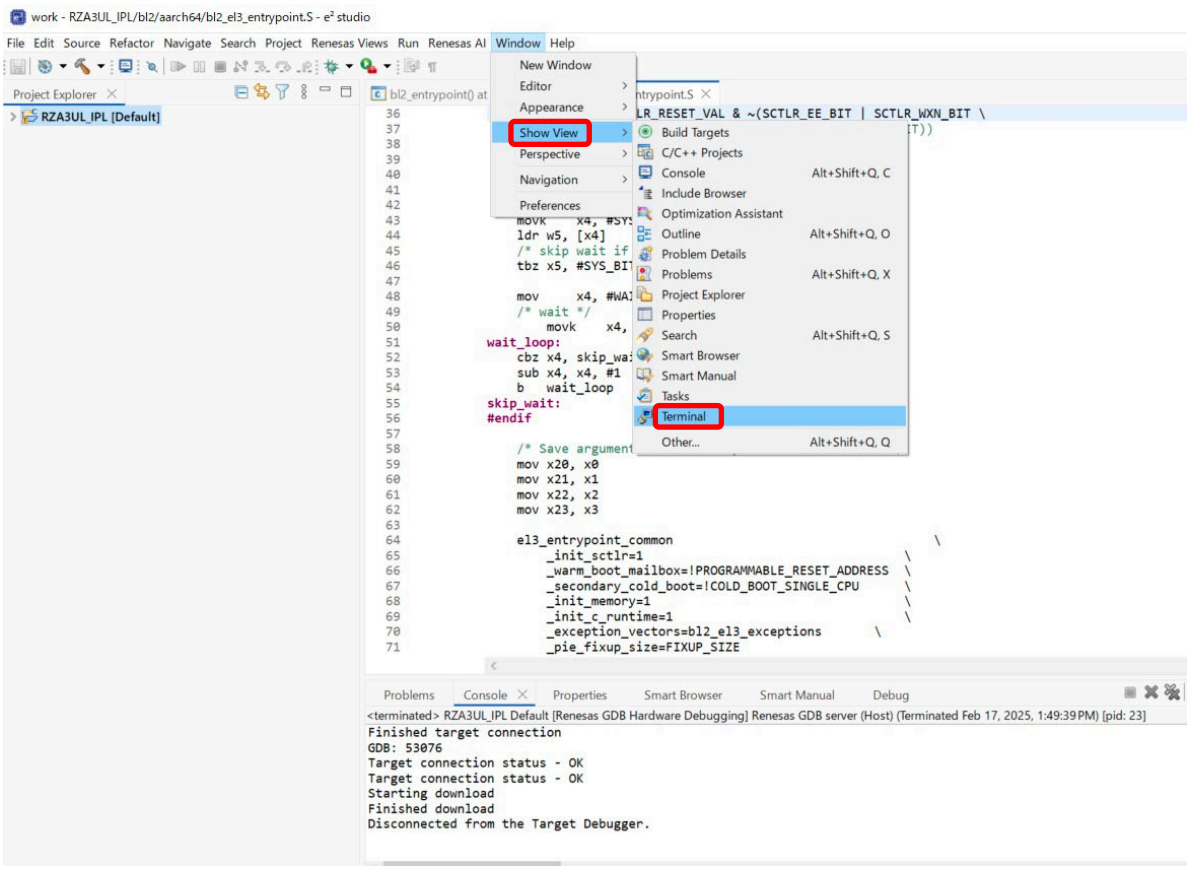


Figure 8.15 Setting Serial Terminal (1)

4. The Terminal window will open.
   Please click the mark.

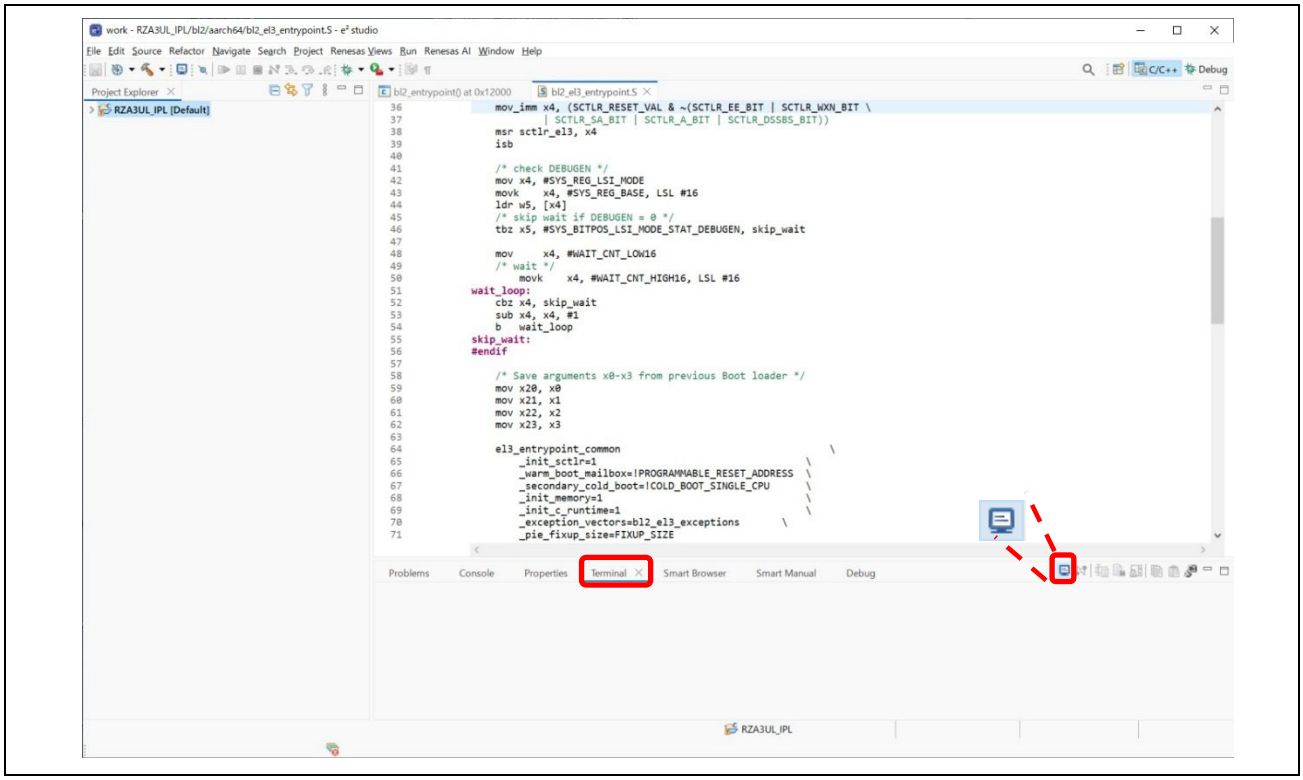


Figure 8.16 Setting Serial Terminal (2)

5. The Lunch Terminal window will bring up.
   Set the parameters as shown in Figure 8.17 on a Windows 10 PC and Figure 8.18 on an Ubuntu 22.04 LTS PC and click OK.
   "Serial port" is a PC environment-dependent port.
   Please configure the settings according to your environment.

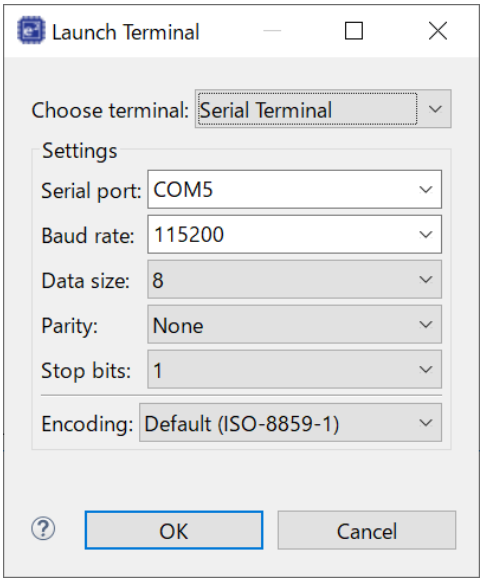


Figure 8.17 Parameter of Serial Terminal (Windows10)

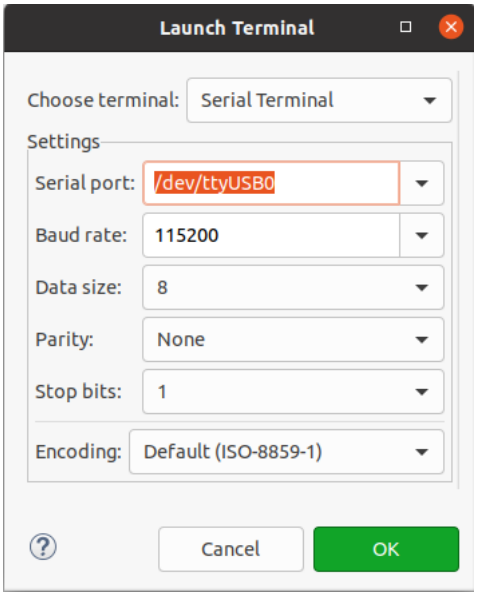


Figure 8.18 Parameter of Serial Terminal (Ubuntu 22.04 LTS)

6. Start the Serial Terminal.

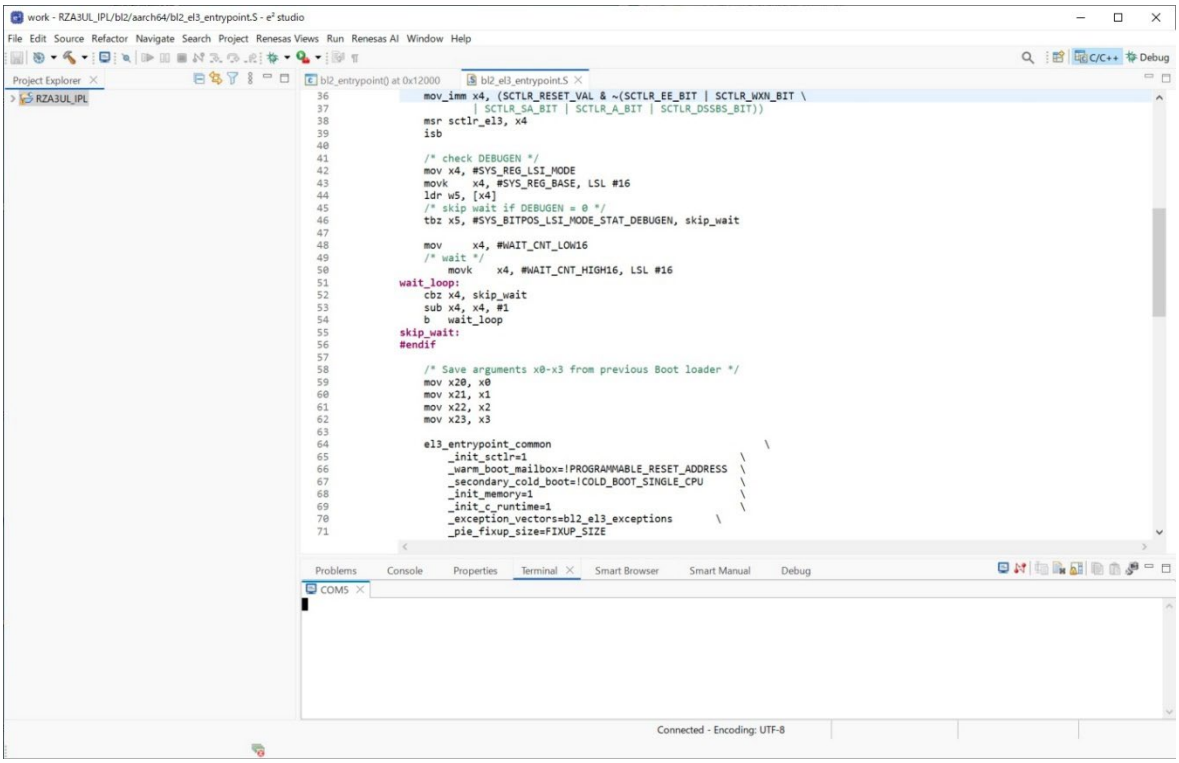


Figure 8.19 Setting Serial Terminal (3)

8.4 Execution procedure of IPL by Serial Flash boot

The procedure for writing the IPL to the Serial Flash memory and executing the IPL is shown below.

1. As the FSP application must be written to the Serial Flash memory to confirm the boot operation by IPL, if the FSP application is not written to the Serial Flash memory, write it.
   For the write procedure, refer to 9.2 Procedure for writing an FSP application to Serial Flash memory.
2. Set the SMARC EVK board operating mode to Boot Mode3 (1.8-V Serial Flash Memory) and turn on the power.
3. Right-click on RZA3UL_IPL and select [Debug AS] -> [Debug Configurations].
   Then, open configuration generated in 8.1 Create Debug Configuration (hereinafter referred to as RZA3UL_IPL Default configuration) to bring up the setting window.

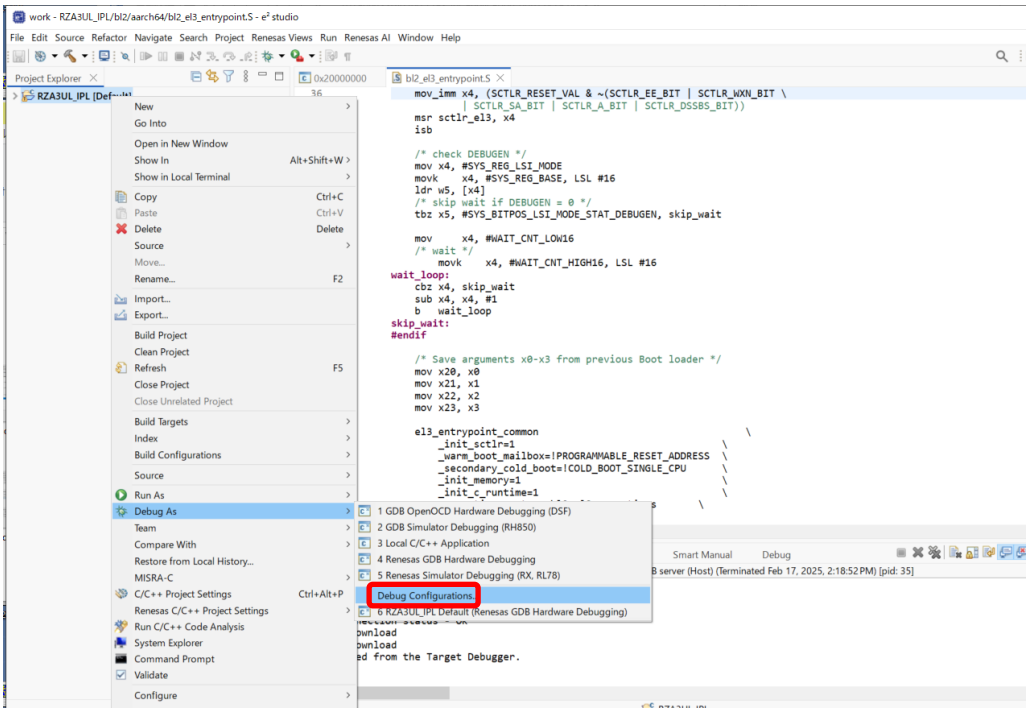


Figure 8.20 Change Debug Configuration of Serial Flash (1)

4. Go to the "Startup" tab and set "On connect" for "rza3ul_smarc_qspi_ipl.srec" to Yes.
   Also, set "On connect" in "Program Binary" to [No].
   Then, click [Apply] to complete the setting, and click [Debug] to start the device connection..

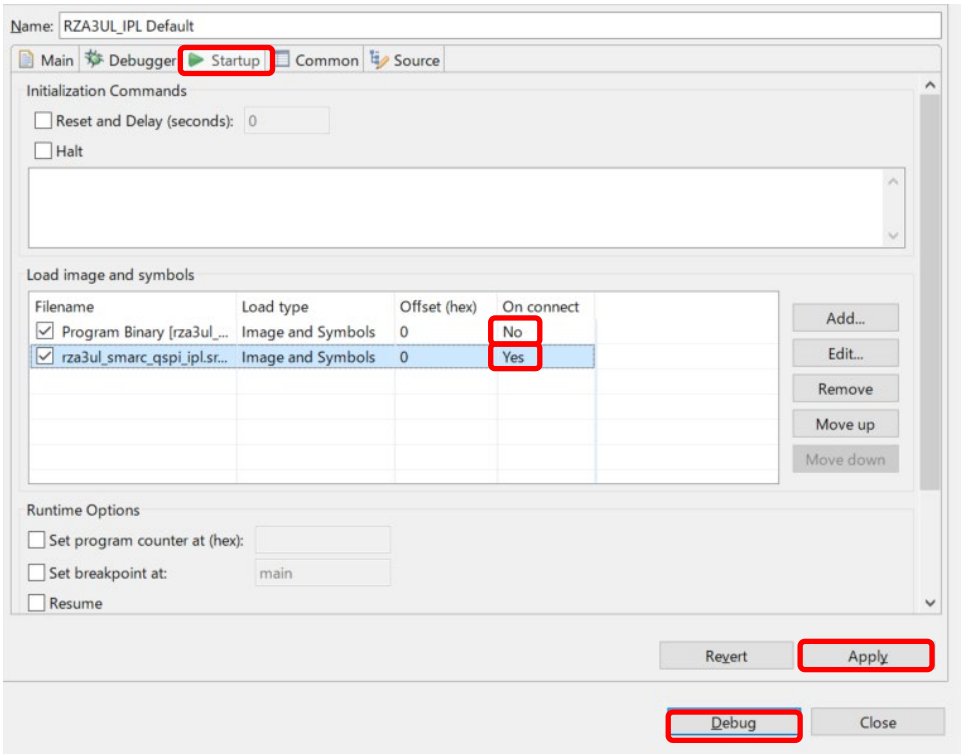


Figure 8.21 Change Debug Configuration of Serial Flash (2)

5. Writing to the Serial Flash memory is performed.
   After the write is complete, the perspective for the debug control will be launched.

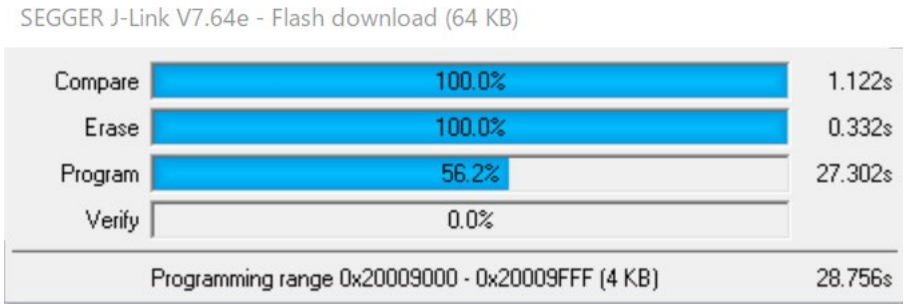


Figure 8.22 Execution of IPL on Serial Flash memory (1)

6. If "Confirm Perspective Switch" is displayed during the launch of the perspective, press [Switch] button.

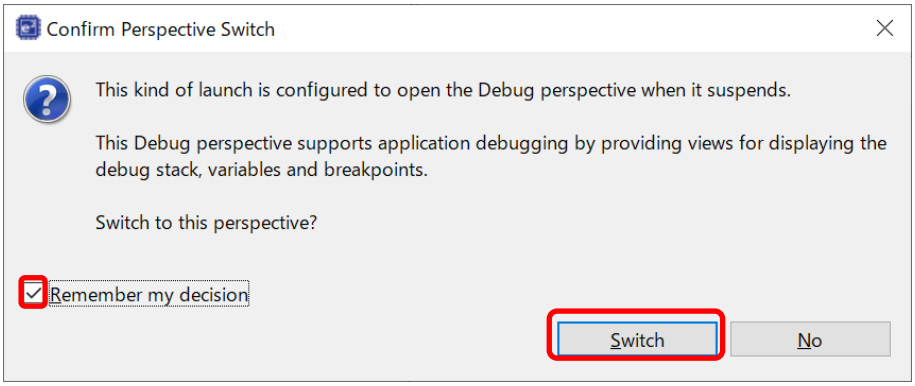


Figure 8.23 Execution of IPL on Serial Flash memory (2)

7 After writing to the Serial Flash, click ■ mark in the perspective to disconnect from the SMARC EVK board.
After that, press the RESET button on the SMARC EVK board to execute the IPL.
At this time, the log shown in Figure 8.26 is displayed on Terminal.
In addition, the program written in the Serial Flash memory starts and the LED of the SMARC EVK board blinks as shown in Figure 8.26.

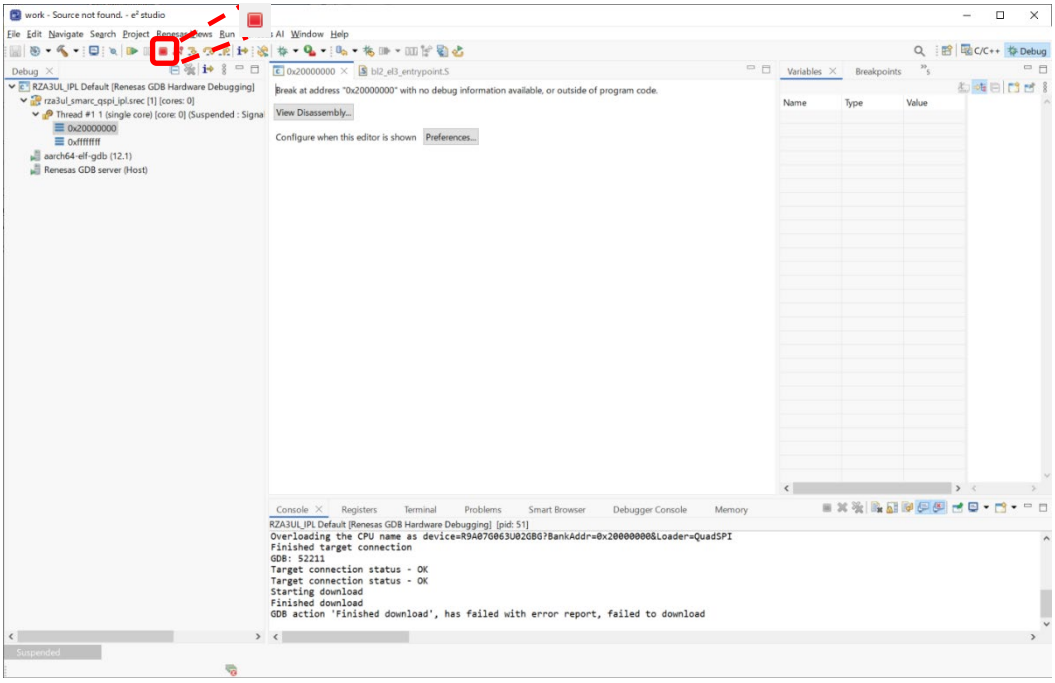


Figure 8.24 Execution of IPL (3)

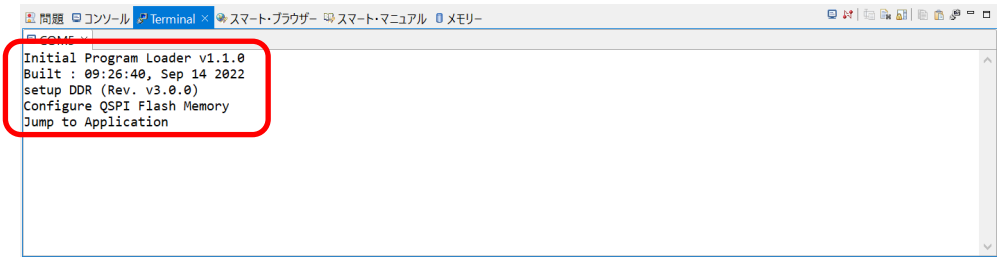


Figure 8.25 IPL execution log

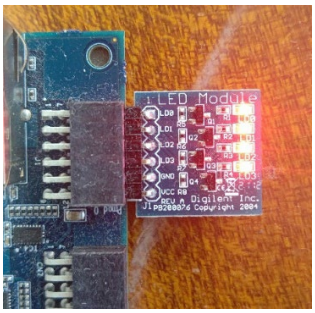


Figure 8.26 LED blinking

9. Application Example

This chapter shows application examples for applying IPL to various environments.

9.1 Execution procedure of IPL by On-chip RAM download

This chapter describes the procedure for writing and executing the IPL to the On-chip RAM for the purpose of facilitating the operation check when customizing the IPL for RZ/A3UL.

1. As the FSP application must be written to the Serial Flash memory to confirm the boot operation by IPL, if the FSP application is not written to the Serial Flash memory, write it.
   For the write procedure, refer to 9.2 Procedure for writing an FSP application to Serial Flash memory.
2. Set the SMARC EVK board operating mode to Boot Mode3 (1.8-V Serial Flash Memory) and turn on the power.
3. Right-click on RZA3UL_IPL and select [Debug AS] -> [Debug Configurations].
   Then, open RZA3UL_IPL Default configuration.

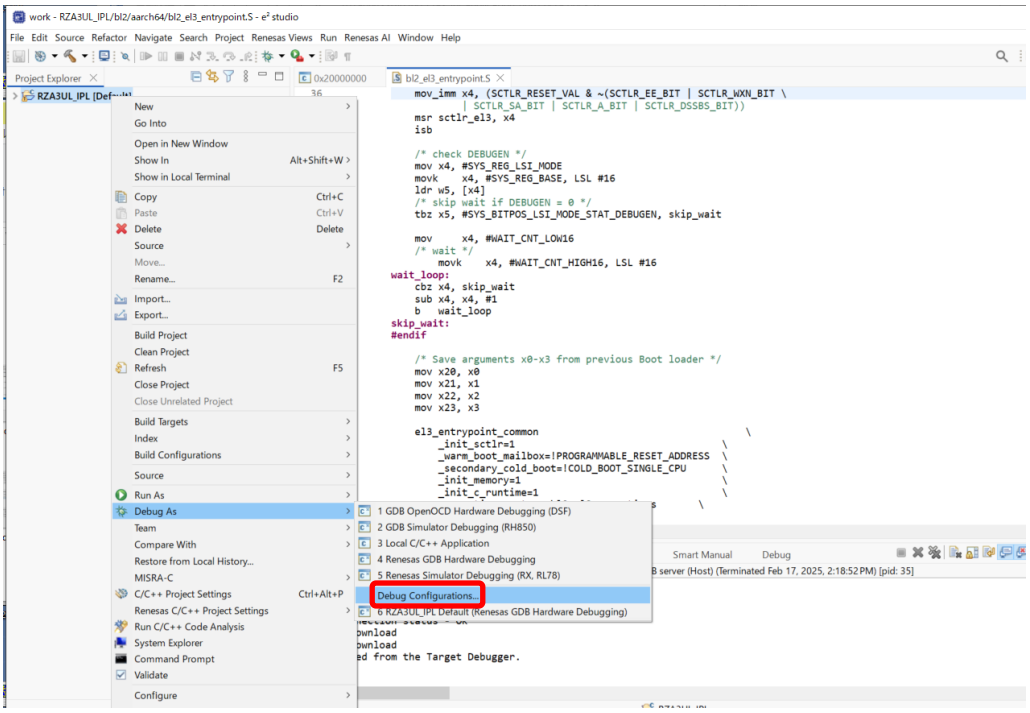


Figure 9.1 Change Debug Configuration of On-chip RAM (1)

4. Go to the "Debugger" -> "Connection Settings" tab and set " Reset at the beginning of connection" to [No].

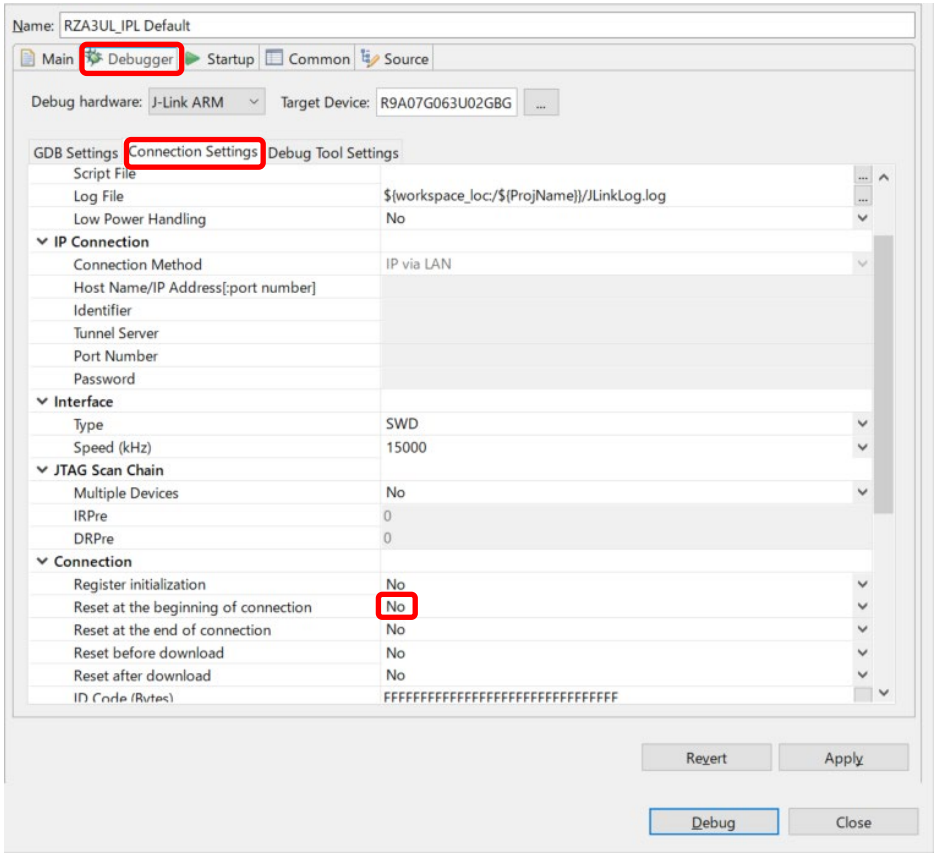


Figure 9.2 Change Debug Configuration of On-chip RAM (2)

5. Go to the "Startup" tab and set "On connect" for "Program Binary" to [Yes].
   Also, set "On connect" in "rza3ul_smarc_qspi_ipl.srec" to [No].
   Then, click [Apply] to complete the setting, and click [Debug] to launch the program.
   This will bring up a perspective for the debug control.

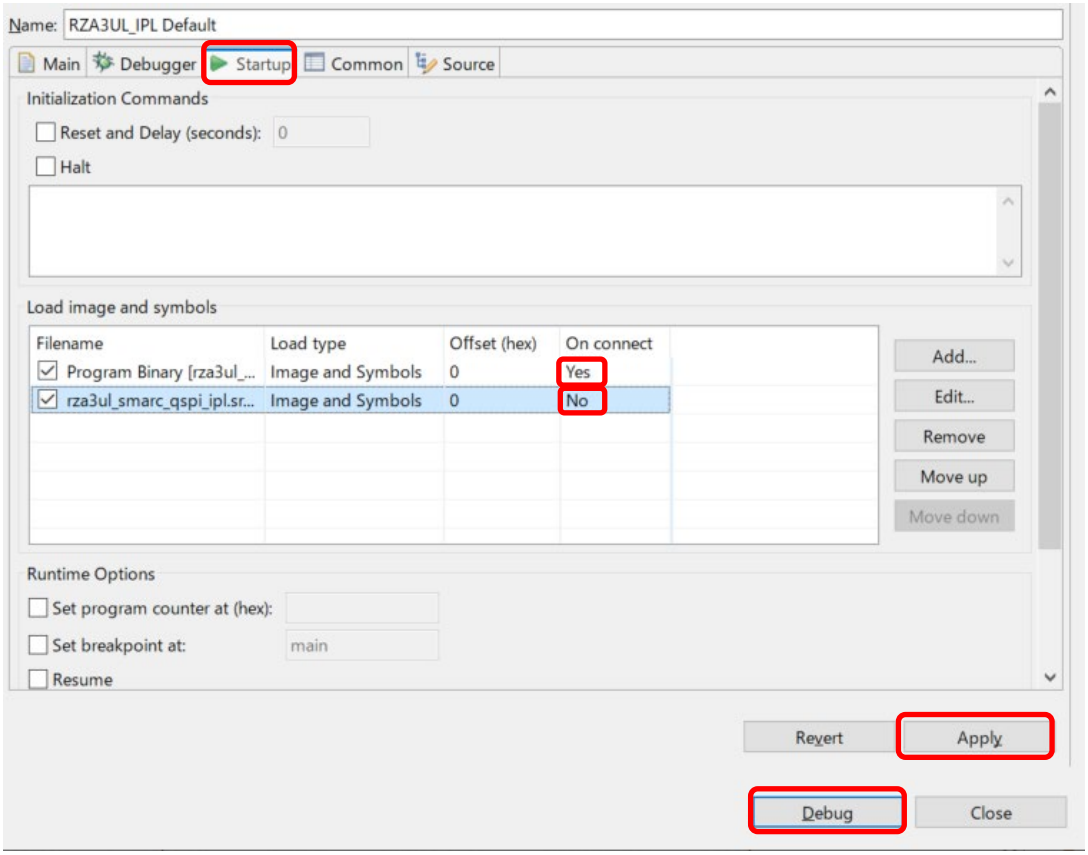


Figure 9.3 Change Debug Configuration of On-chip RAM (3)

6. Click mark in the perspective to perform the IPL.
   The IPL will start executing and the log shown in Figure 9.5 will be displayed in the terminal.
   At this time, the FSP application written on the Serial Flash memory starts, and the LED of the SMARC EVK board blinks as shown in Figure 9.6.

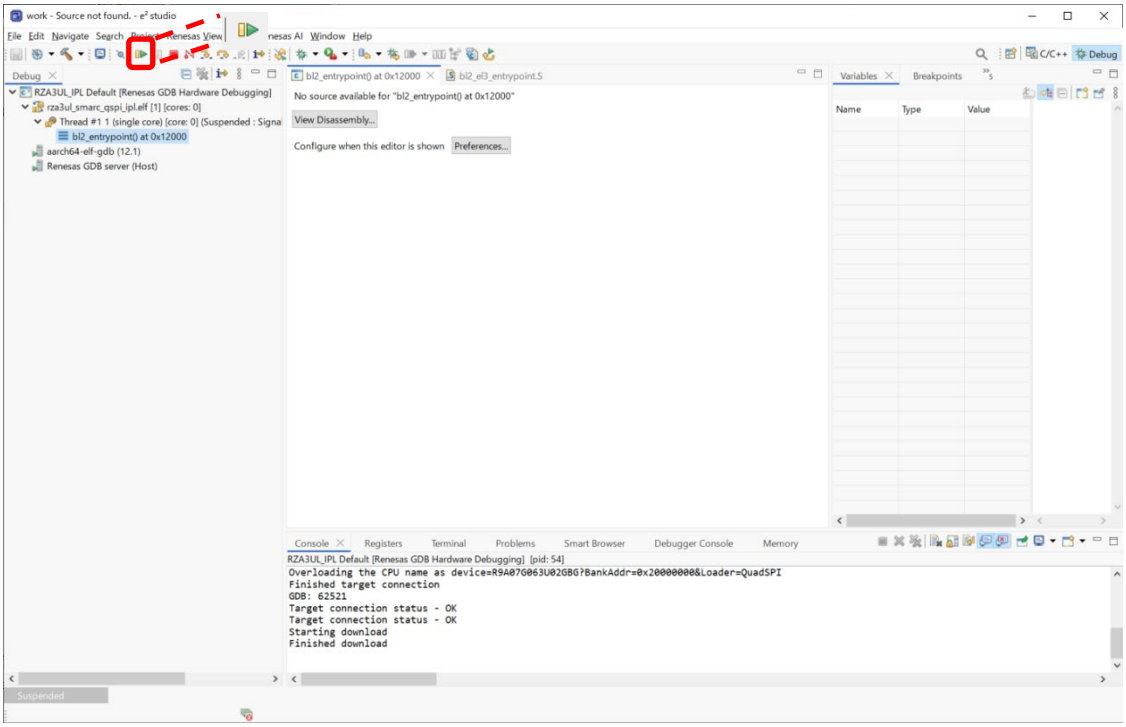


Figure 9.4 Execution of IPL (4)

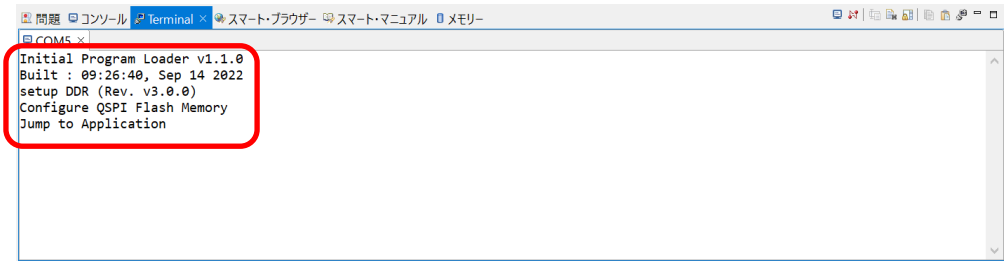


Figure 9.5 IPL execution log

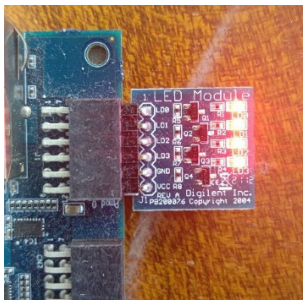


Figure 9.6 LED blinking

9.2 Procedure for writing an FSP application to Serial Flash memory

This chapter describes the procedure for writing an FSP application to Serial Flash memory.

Refer to the Getting Started with RZ/A Flexible Software Package (R01AN6499EJ) for building the FSP application.

This chapter shows an example of saving the FSP application binary file in C:\work.

1. Set the SMARC EVK board operating mode to Boot Mode3 (1.8-V Serial Flash Memory) and turn on the power.
2. Right-click on RZA3UL_IPL and select [Debug AS] -> [Debug Configurations].
   Then, open RZA3UL_IPL Default configuration.

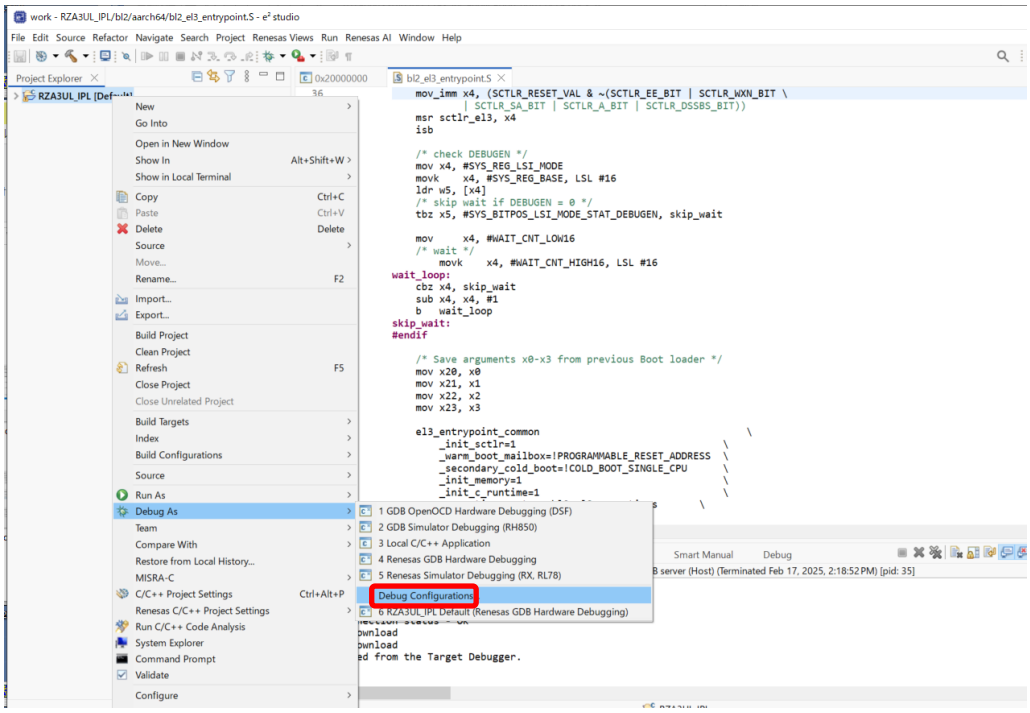


Figure 9.7 Procedure of writing FSP Application (1)

3. Edit Configuration will be launched.
   Set the "On connect" of all registered images to [No], set the image not to be downloaded when connecting to the SMARC EVK board.
   Then, click [Apply] to complete the setting, and click [Debug] to launch the program.

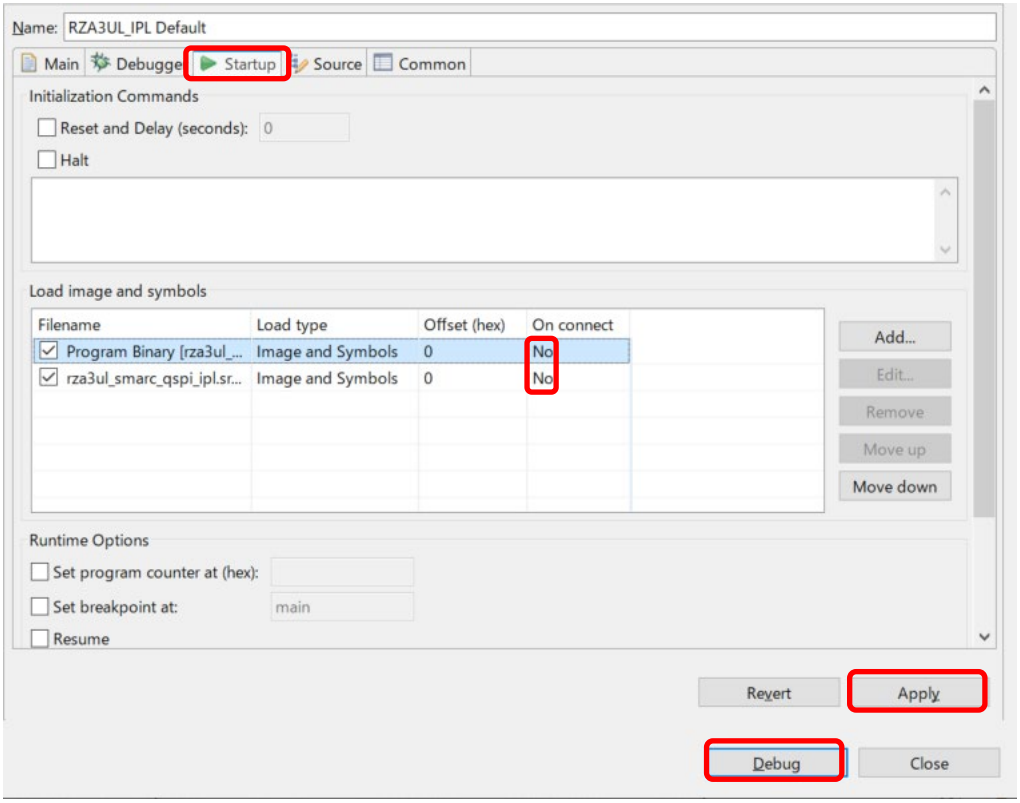


Figure 9.8 Procedure of writing FSP Application (2)

4. If "Confirm Perspective Switch" is displayed during the perspective launch, press [Switch] button.

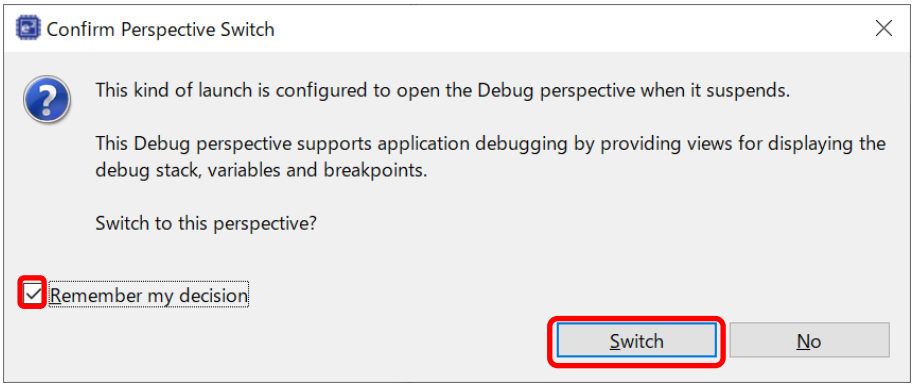


Figure 9.9 Procedure of writing FSP Application (3)

5. The board is connected, and the perspective is launched.
   Click Load Ancillary file .

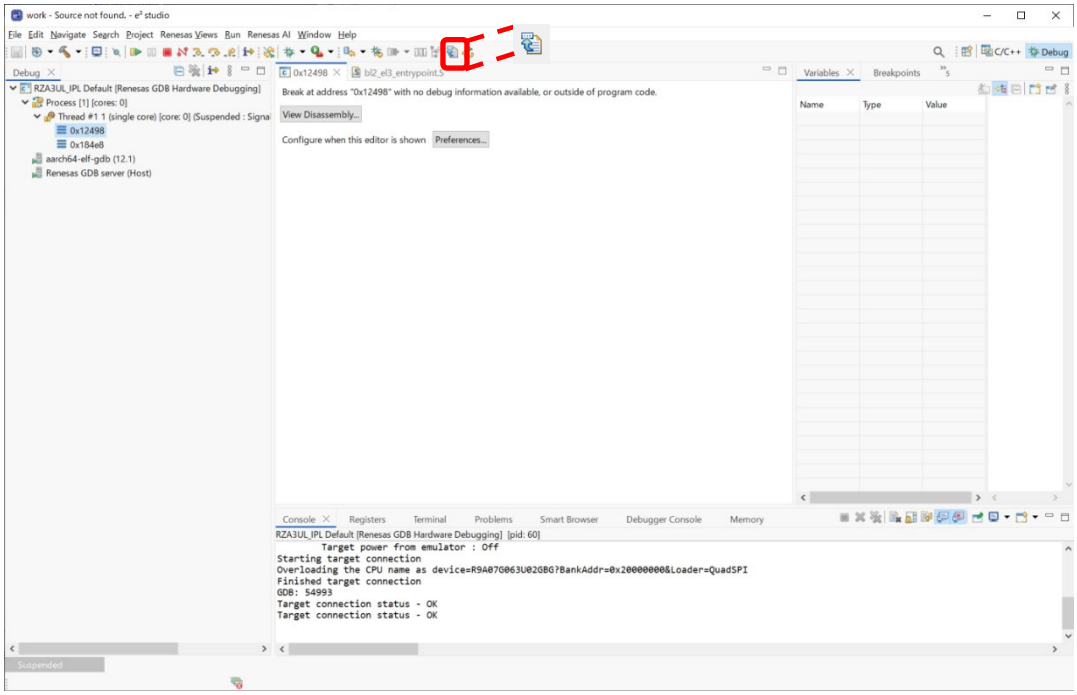


Figure 9.10 Procedure of writing FSP Application (4)

6. The Load Ancillary File window will be launched.
   Click [File System] and select C:\work\RZA3UL_CA55_BLINKY.srec.
   Also, uncheck "Load as raw binary image".
   Click [OK] to write to the Serial Flash memory.

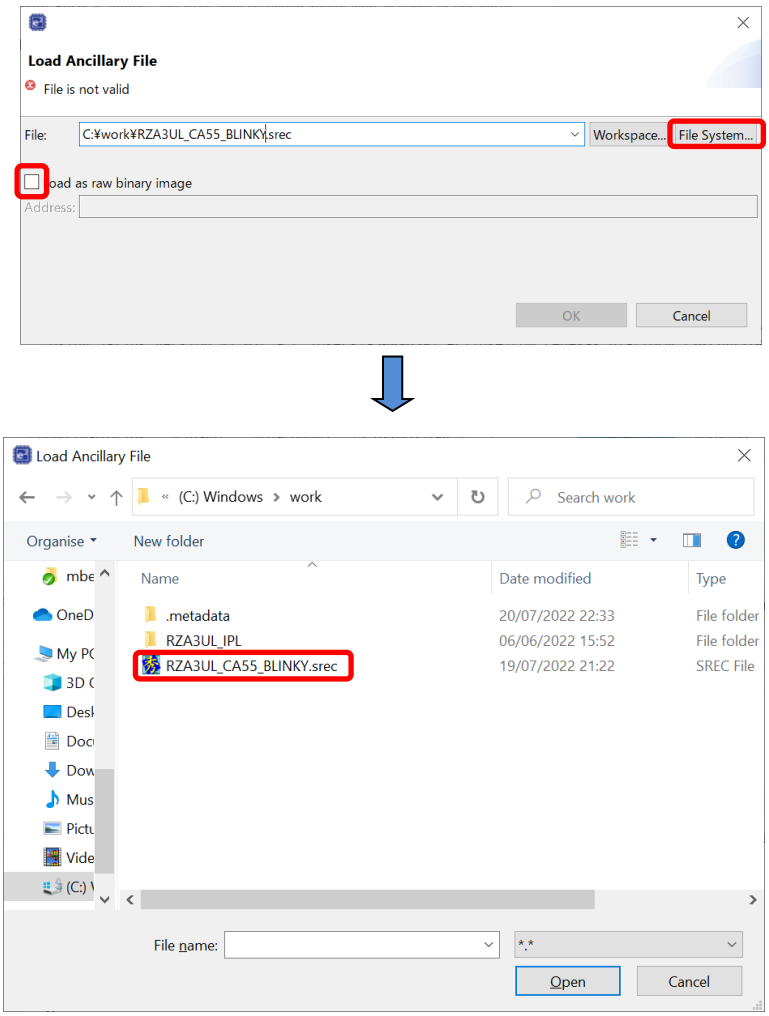


Figure 9.11 Procedure of writing FSP Application (5)

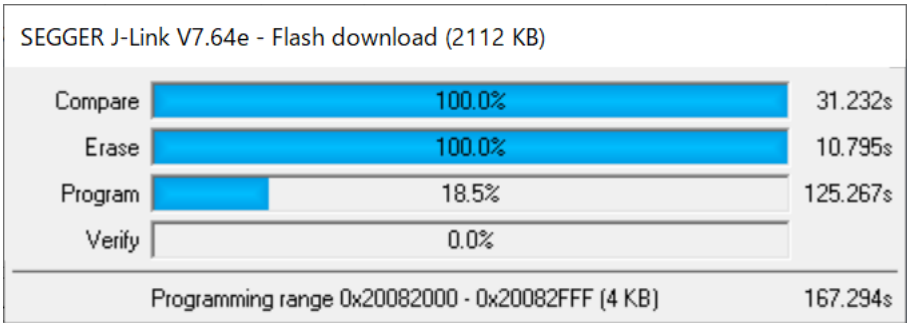


Figure 9.12 Procedure of writing FSP Application (6)

7. After writing, click ■ mark to disconnect from the SMARC EVK board.

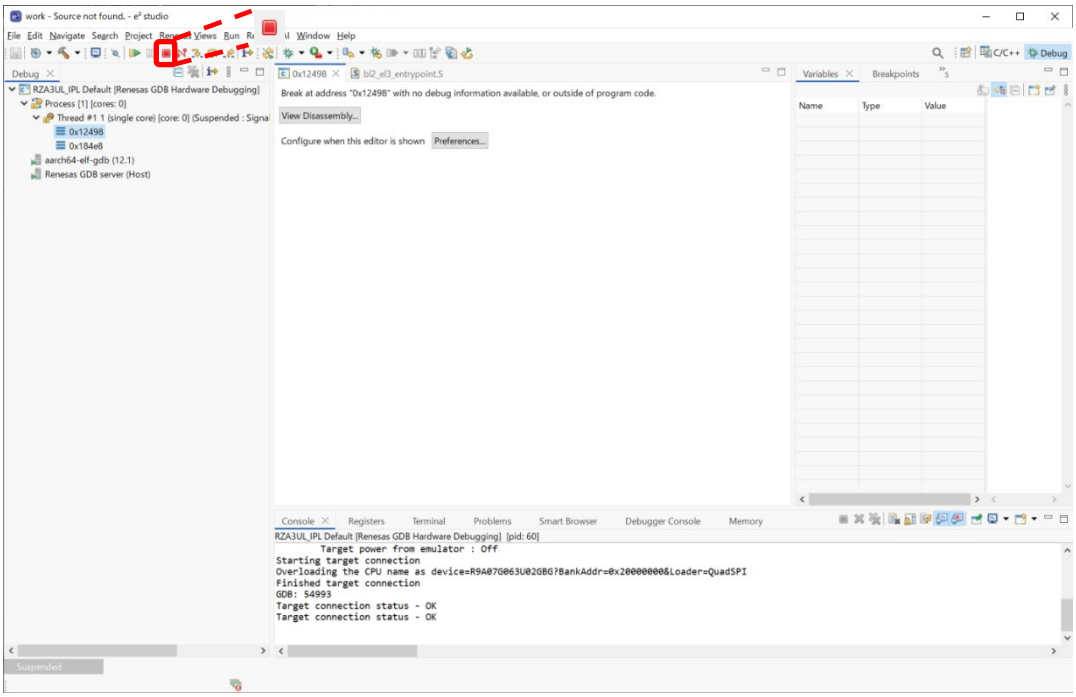


Figure 9.13 Procedure of writing FSP Application (7)

9.3 How to change IPL build environment for custom board

This chapter describes the IPL build environment construction procedure for boards other than SMARC EVK boards (hereafter referred to as custom boards).

The IPL build environment for custom board is created by modifying the SMARC EVK build environment.

The chapters listed below will show you how to do that.

- How to add Serial Flash memory used by IPL (Chapter 9.3.1)
- Specifications of functions that control Serial Flash memory and how to change functions when memory is changed (Chapter 9.3.1.1 to Chapter 9.3.1.14)
- How to add settings for boards other than the SMARC EVK board to IPL (Chapter 9.3.2)
- How to add clock supply settings for mounted modules (Chapter 9.3.3)
- How to add pin settings (Chapter 9.3.4)
- How to add MMU settings (Chapter 9.3.5)

9.3.1 How to customize IPL for your Serial Flash memory

This chapter describes how to customize the IPL according to your Serial Flash memory.

First, the method of controlling the Serial Flash memory in IPL is shown.

The IPL is implemented with the Serial Flash memory driver and the SPIBSC driver to control the Serial Flash memory.

The Serial Flash memory driver manages the execution of operations of the Serial Flash memory.

The SPIBSC driver is a driver for controlling serial communication between RZ/A3 and Serial Flash memory.

The Serial Flash memory driver creates an operation table consisting of parameters for executing Serial Flash memory operations and passes it to the SPIBSC driver.

The SPIBSC driver controls HW according to the operation table passed as an argument from the Serial Flash memory driver and performs serial communication.

Since the Serial Flash memory driver is a Serial Flash memory-dependent implementation, it must be changed according to your Serial Flash memory.

The SPIBSC driver implementation, on the other hand, does not rely on Serial Flash memory.

Therefore, there is no need to change even when changing the Serial Flash memory.

Figure 9.14 shows the operation image diagram of each driver.

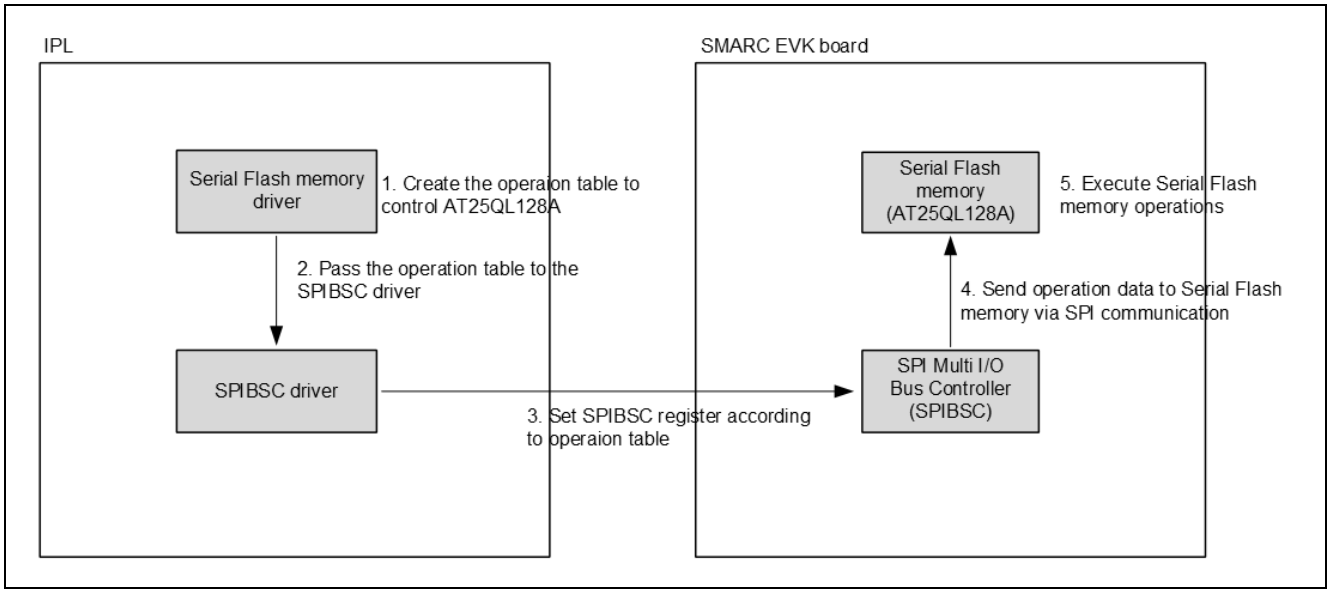


Figure 9.14 Operating image of Serial Flash memory driver and SPIBSC driver

1. The Serial Flash memory driver creates an operation table corresponding to your memory.
2. The Serial Flash memory driver calls the SPIBSC driver.
   At this time, the operation table is passed to the SPIBSC driver.
3. The SPIBSC driver sets the SPIBSC register according to the received operation table parameters.
4. SPIBSC performs serial communication with the Serial Flash memory according to the settings made in step3 and sends operation data to the Serial Flash memory.
5. The Serial Flash memory controls itself according to the received operation data.

Figure 9.15 shows the relationship between operation table parameters and transfer formats.

As an example of an operation table, Figure 9.16 shows AT25QL128A read command operation table setting values.

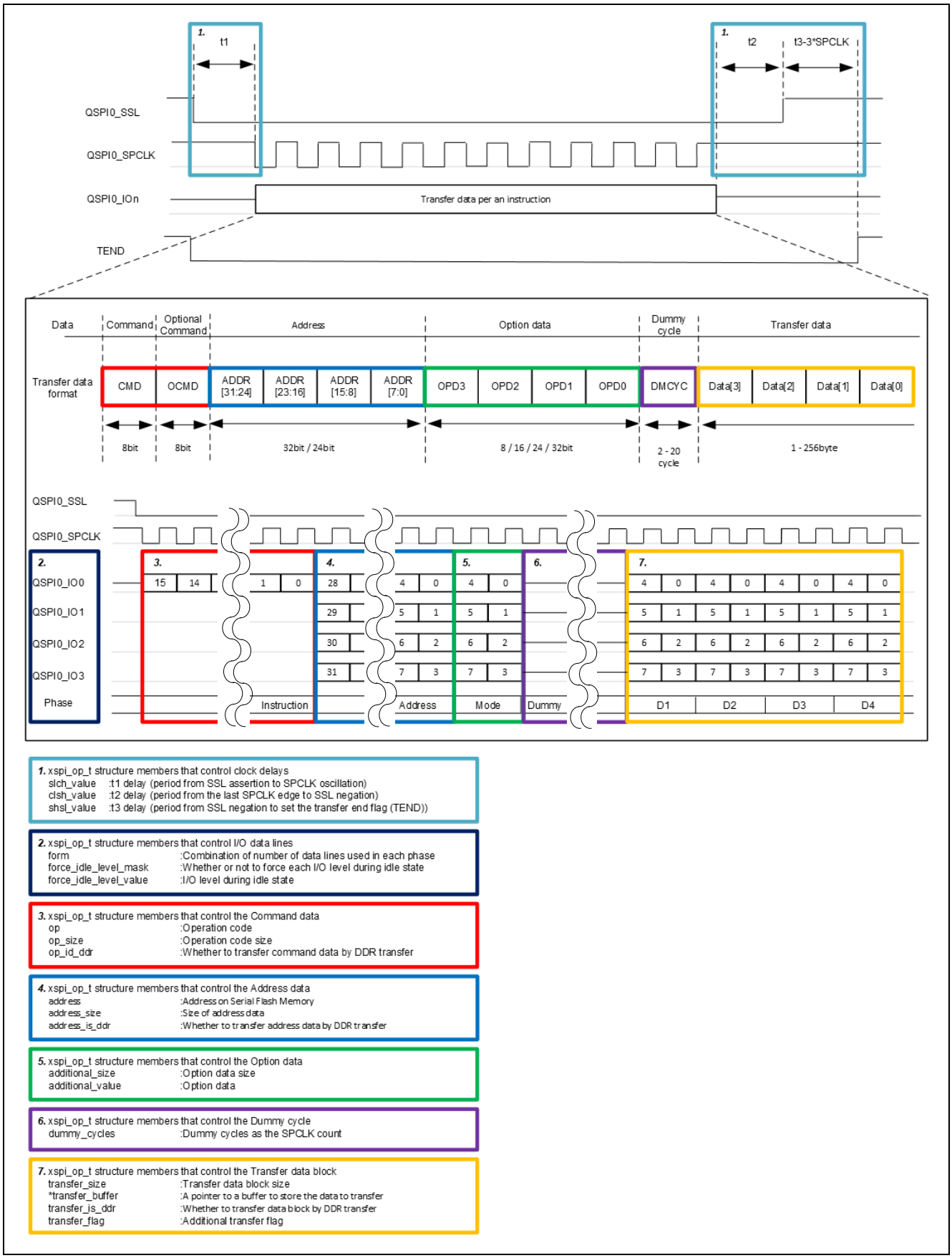


Figure 9.15 Correspondence between the member of xspi_op_t structure and the transfer format

Setting example
Fast Read Quad I/O command (0xEB) of the AT25QL128A
This is defined in the source code as variable "rop"

form	:SPI_FORM_1_4_4
op	:0xEB
op_size	:1
op_id_ddr	:false
address	:0
address_size	:3
address_is_ddr	:false
additional_size	:1
additional_value	:0x55555555
dummy_cycles	:4
transfer_size	:user-specified size
*transfer_buffer	:user-specified address
transfer_is_ddr	:false
transfer_flag	:0
force_idle_level_mask	:0x08
force_idle_level_value	:0x08
slch_value	:0
clsh_value	:0
shsl_value	:6

Setting member description.
Similar to the on in Figure 9.17

1. xspi_op_t structure members that control clock delays

slch_value	:t1 delay (period from SSL assertion to SPCLK oscillation)
clsh_value	:t2 delay (period from the last SPCLK edge to SSL negation)
shsl_value	:t3 delay (period from SSL negation to set the transfer end flag (TEND))

2. xspi_op_t structure members that control I/O data lines

form	:Combination of number of data lines used in each phase
force_idle_level_mask	:Whether or not to force each I/O level during idle state
force_idle_level_value	:I/O level during idle state

3. xspi_op_t structure members that control the Command data

op	:Operation code
op_size	:Operation code size
op_id_ddr	:Whether to transfer command data by DDR transfer

4. xspi_op_t structure members that control the Address data

address	:Address on Serial Flash Memory
address_size	:Size of address data
address_is_ddr	:Whether to transfer address data by DDR transfer

5. xspi_op_t structure members that control the Option data

additional_size	:Option data size
additional_value	:Option data

6. xspi_op_t structure members that control the Dummy cycle

dummy_cycles	:Dummy cycles as the SPCLK count

7. xspi_op_t structure members that control the Transfer data block

transfer_size	:Transfer data block size
*transfer_buffer	:A pointer to a buffer to store the data to transfer
transfer_is_ddr	:Whether to transfer data block by DDR transfer
transfer_flag	:Additional transfer flag

Figure 9.16 Setting example of parameters corresponding to transfer format

Shows how to add the Serial Flash memory driver for the new Serial Flash memory.

1. Open the "c:\work\RZA3UL_IPL\plat\renesas\rz\common\drivers\xspidevice" folder, copy the "qspiflash_at25" folder and rename it to any name.
   From step2 onwards, the user will change the file name and structure name to correspond to the folder name decided in this step.
   This time, rename the folder name to "qspiflash_custom".

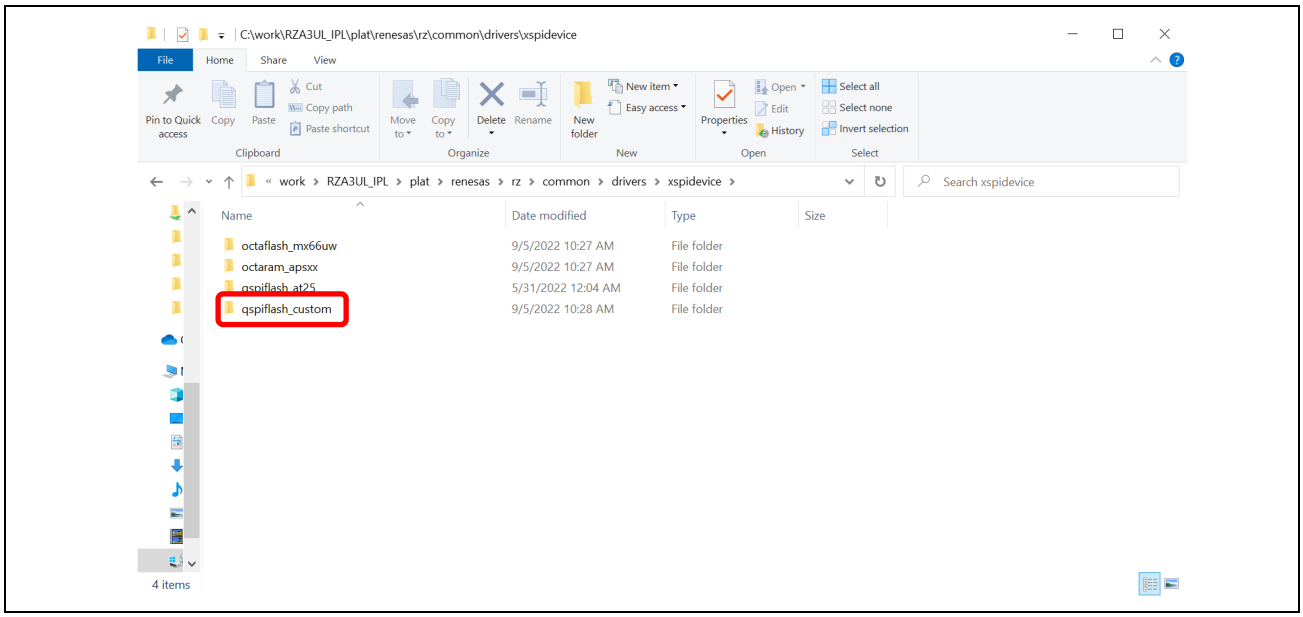


Figure 9.17 Rename Serial Flash memory driver folder

2. Open "qspiflash_custom" folder and change "qspiflash_at25.c", "qspiflash_at25_api.h" to "qspiflash_custom.c", "qspiflash_custom_api.h".

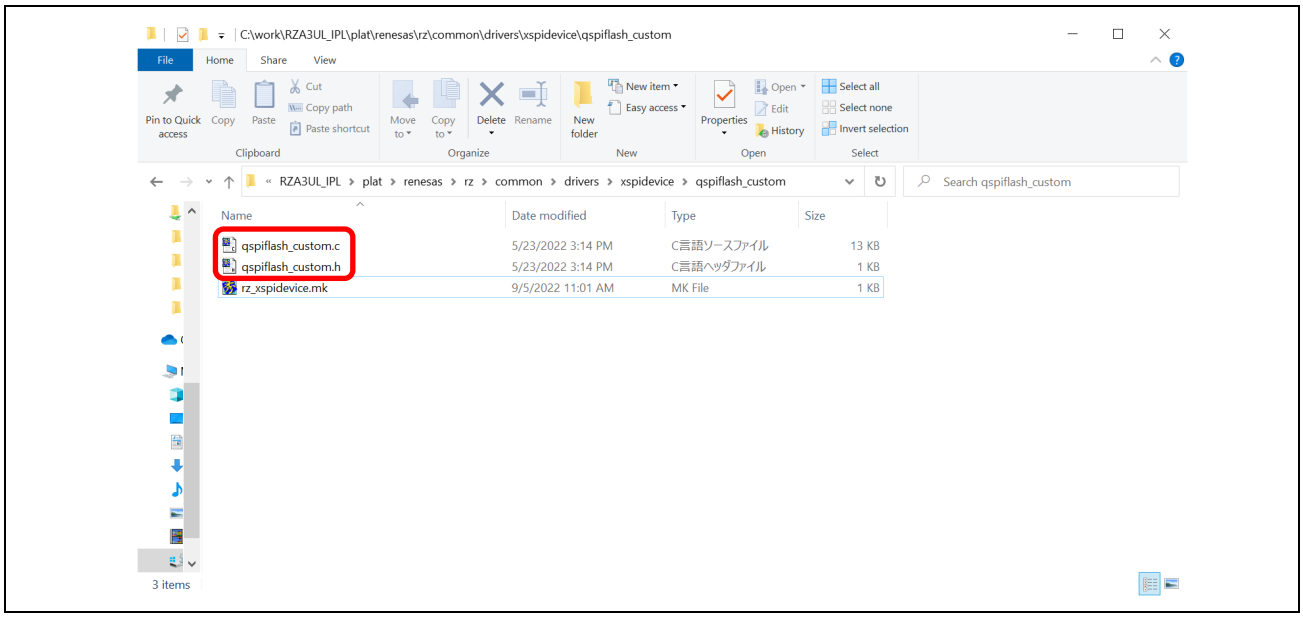


Figure 9.18 Rename Serial Flash memory driver files

3. Open "rz_xspidevice.mk" and change "_XSPI_DEVICE:=qspiflash_at25" on line 6 to "_XSPI_DEVICE:=qspiflash_custom".

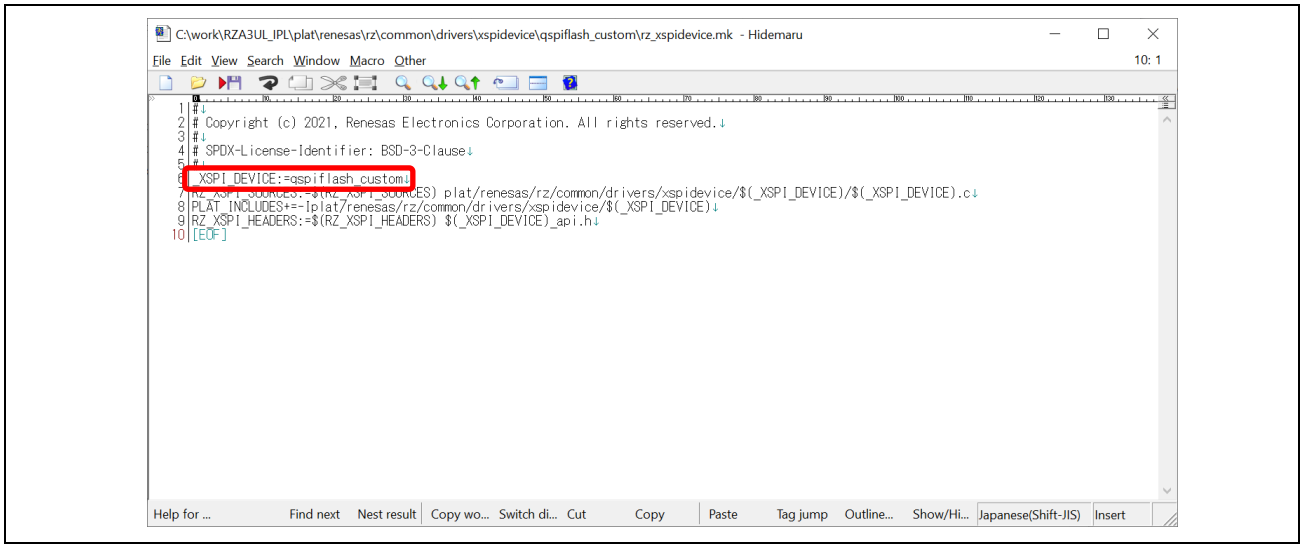
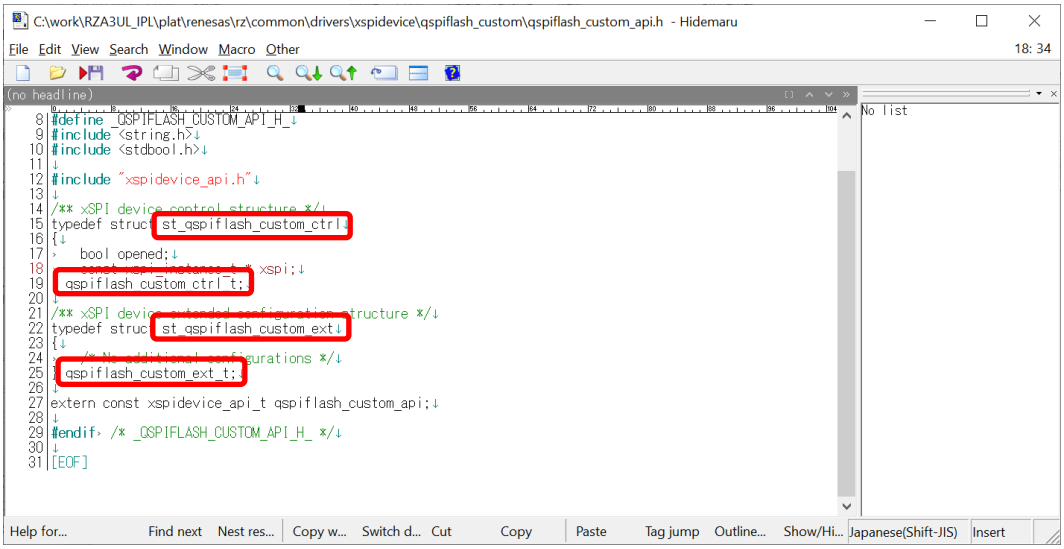


Figure 9.19 Change Serial Flash memory driver Makefile

4. Open "qspiflash_custom_api.h" and replace all structure definitions of "xx_qspiflash_at25_xx" with "xx_qspiflash_custom_xx".



Note: The qspiflash_custom_ext_t structure is for extended settings.
If the members corresponding to the parameters required for your Serial Flash memory are not provided in the qspiflash_custom_t structure, add those members as extended settings.

Figure 9.20 Change Serial Flash memory driver structs name

5. Open qspiflash_custom.c and replace the included header with "qspiflash_custom_api.h".
   Also, reflect the structure name replaced in step 4.

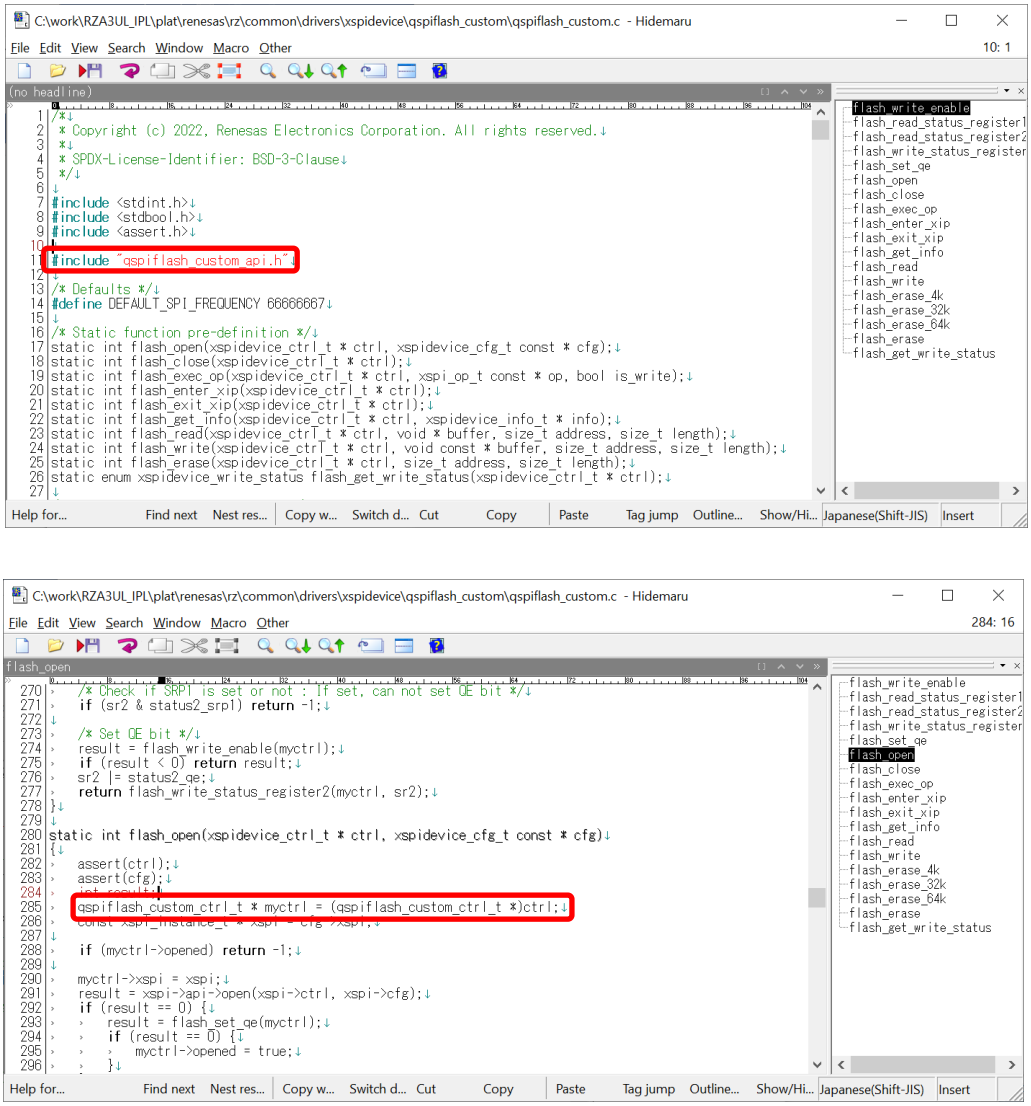


Figure 9.21 Change Serial Flash memory driver source code

6. Change the implementation of API functions in Table 9.1 and Sub functions in Table 9.2 according to your Serial Flash memory.
   9.3.1.1 to 9.3.1.14 show the specifications of each function implemented in the default IPL and the change points when changing the Serial Flash memory.
   Please refer to these and change the implementation of each function.

Table 9.1 API Function

Function Name	Description
flash_open	Serial Flash memory driver open function
flash_close	Serial Flash memory driver close function
flash_exec_op	Serial Flash memory driver operation function
flash_enter_xip	Serial Flash memory driver External Space Address Read Mode start function
flash_exit_xip	Serial Flash memory driver External Space Address Read Mode stop function
flash_read	Serial Flash memory driver read function
flash_write	Serial Flash memory driver write function
flash_erase	Serial Flash memory driver erase function
flash_get_write_status	Serial Flash memory driver write status get function

Table 9.2 Sub Function

Function Name	Description
flash_write_enable	Set write enable to Serial Flash memory
flash_read_status_register1	Read lower 8bit of status register of the Serial Flash memory
flash_read_status_register2	Read higher 8bit of status register of the Serial Flash memory
flash_write_status_register2	Write higher 8bit of status register of the Serial Flash memory
flash_set_qe	Set Quad Enable bit of status register of the Serial Flash memory
flash_erase_4k	Erase the Serial Flash memory in units of 4Kbytes
flash_erase_32k	Erase the Serial Flash memory in units of 32Kbytes
flash_erase_64k	Erase the Serial Flash memory in units of 64Kbytes

7. Add the added Serial Flash memory driver to the board settings.
   Refer to Chapter 9.3.2 for how to add.

9.3.1.1 flash_open

flash_open() is a function that initializes the Serial Flash memory so that it can be accessed.

flash_open() implemented by default IPL initializes to access AT25QL128A mounted on the SMARC EVK board.

flash_open		
Outline	Initialize the Serial Flash memory	
Declaration	int flash_open (xspidevice_ctrl_t * ctrl, xspidevice_cfg_t const * cfg)	
Description	- Set SPCLK frequency - Set the Serial Flash memory registers and access settings for the Serial Flash memory - Set opened flag	
Arguments	*ctrl	: Pointer to xSPI device control structure
	*cfg	: Pointer to xSPI device configure structure
Return value	0	: Initialization is complete
	-1	: Initialization is failed
Note	-	

Figure 9.22 shows a flowchart of the flash_open() implementation in the default IPL.

The processing that changes the implementation when changing the Serial Flash memory is shown below.

- P1 Clock frequency setting change
- P2 Serial Flash memory register setting

These are shown as P1, P2 in the flow chart as implementation change points.

The details of the processing are explained after the flow chart.

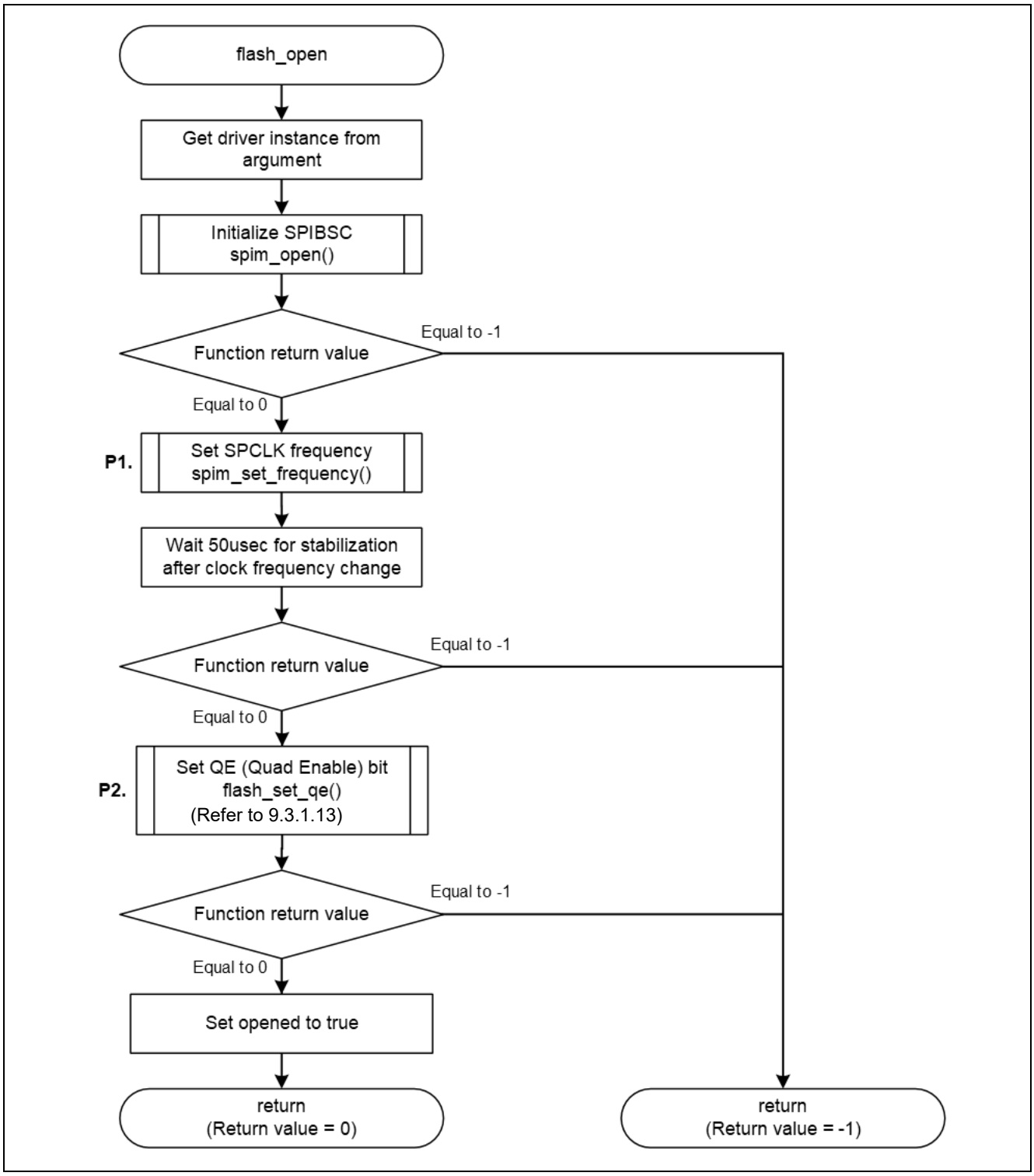


Figure 9.22 Flowchart of flash_open

P1. Clock Frequency setting change

flash_open sets the operating clock frequency of the Serial Flash memory.

The defined value of DEFAULT_SPI_FREQUENCY in L14 of qspiflash_custom.c shown in Figure 9.23 is used for the operating clock frequency.

Set this define value to the optimum value for your Serial Flash memory.

The maximum value that can be set is 100000000 (100MHz) and the minimum value is 3125000 (3.125MHz).

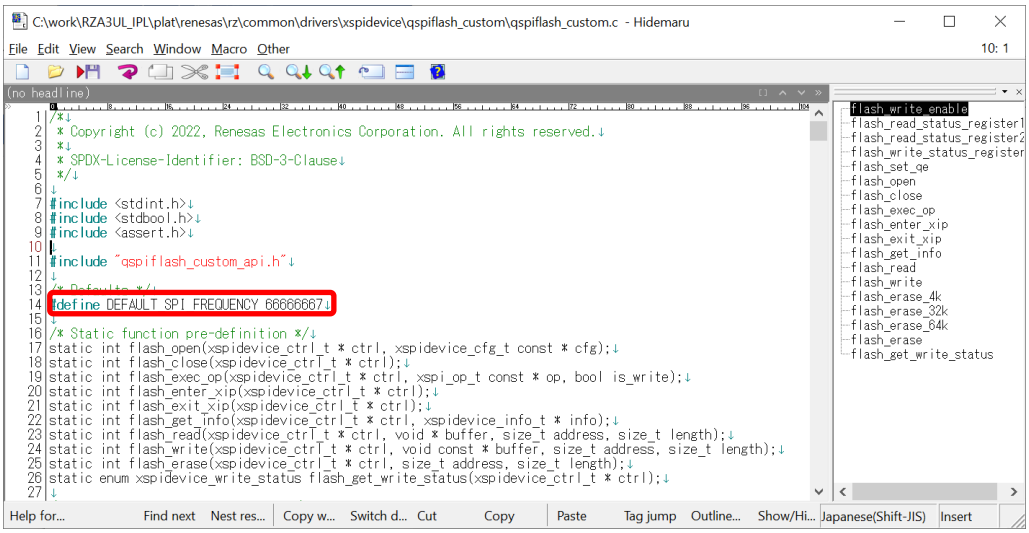


Figure 9.23 Change operation clock frequency

P2. Serial Flash memory register setting

In AT25QL128A, QE bit of Status Register shown in Table 9.3 must be set to enable Quad operation.

The QE bit of the Status Register is set by the subfunction flash_set_qe() function.

Refer to 9.3.1.13 when changing the QE bit setting method.

Table 9.3 QE bit of AT25QL128A Status Register (BIT15 – Bit 8)

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
SUS	CMP	-	-	-	-	QE	SRP1
Suspend Status	Complement Protect	Reserved	Reserved	Reserved	Reserved	Quad Enable	Register Protect1

The settings required for initialization differ depending on your Serial Flash memory.

Set the Serial Flash memory registers according to the specifications.

In particular, most Serial Flash memories require dummy cycle settings for initialization. (No setting required for AT25QL128A)

For Serial Flash memory that requires dummy cycle setting, create a sub function to set the dummy cycle.

Then refer to P2 and implement the setting to the register in that function.

9.3.1.2 flash_close

flash_close() is a function to terminate the Serial Flash memory driver.

flash_close() implemented in the default IPL only clears the opened flag, which indicates the open state of the driver.

Therefore, it is possible to access Serial Flash memory even after executing flash_close().

flash_close		
Outline	Close the Serial Flash memory	
Declaration	int flash_close (xspidevice_ctrl_t * ctrl)	
Description	- Clear opened flag	
Arguments	*ctrl	: Pointer to xSPI device control structure
Return value	0	: Close process is complete
	-1	: Close process is failed
Note	-	

Figure 9.24 shows a flowchart of the flash_close() implementation in the default IPL.

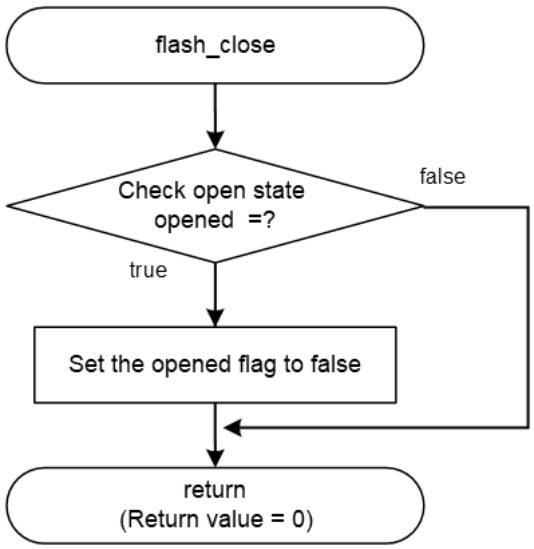


Figure 9.24 Flowchart of flash_close

9.3.1.3 flash_exec_op

flash_exec_op() is a function to send operation information to be executed by Serial Flash memory.

The flash_exec_op() implemented in the default IPL is called from the function shown below and sends the operation data to be executed by the AT25QL128A mounted on the SMARC EVK board.

- flash_write()
- flash_write_enable()
- flash_read_status_register1()
- flash_read_status_register2()
- flash_write_status_register2()
- flash_erase_4k()
- flash_erase_32k()
- flash_erase_64k()

flash_exec_op	
Outline	Execute operation to Serial Flash memory
Declaration	void flash_exec_op (xspidevice_ctrl_t * ctrl, xspi_op_t const * op, bool is_write)
Description	- Pass operation table *op to spim_exec_op() to transfer operation data
Arguments	*ctrl : Pointer to xSPI device control structure *op : Pointer to xSPI interface operation structure is_write : Specifies the transmission/reception direction of the operation (0=read、1=write)
Return value	0 : Execute the operation is complete -1 : Execute the operation is failed
Note	-

Figure 9.25 shows a flowchart of the flash_exec_op() implementation in the default IPL.

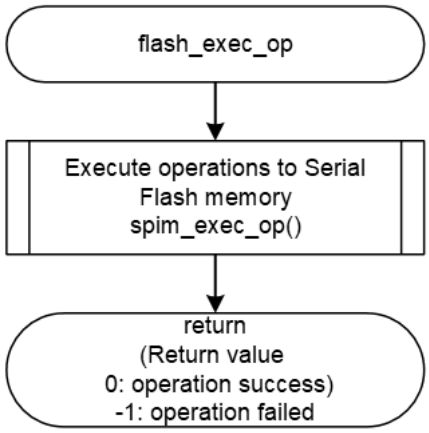


Figure 9.25 Flowchart of flash_exec_op

9.3.1.4 flash_enter_xip

flash_enter_xip() is a function that changes the read access method of SPIBSC from Manual Mode to External Space Address Read Mode.

In External Space Address Read Mode, data can be read by read access to the Serial Flash memory area (H'20000000) in the memory space shown in Figure 5.4.

In External Space Address Read Mode, when read access is made to the Serial Flash memory area, the SPIBSC automatically performs serial communication and data is read.

At this time, the Read operation registered in SPIBSC is used for serial communication.

flash_enter_xip() implemented in the default IPL registers the Read operation of AT25QL128A mounted on the SMARC EVK board to SPIBSC.

flash_enter_xip	
Outline	Set the External Address Space Read Mode to the Serial Flash memory
Declaration	int flash_enter_xip (xspidevice_ctrl_t * ctrl)
Description	- Register Read operation to SPIBSC - Set SPCLK frequency - Change the Read access method to External Space Address Read Mode
Arguments	*ctrl : Pointer to the control structure for instance
Return value	0 : Setting is complete -1 : Setting is failed
Note	-

Figure 9.26 shows a flowchart of the flash_enter_xip() implementation in the default IPL.

The processing that changes the implementation when changing the Serial Flash memory is shown below.

- P1 Register Read operation
- P2. Clock frequency setting change

These are shown as P1, P2 in the flow chart as implementation change points.

The details of the processing are explained after the flow chart.

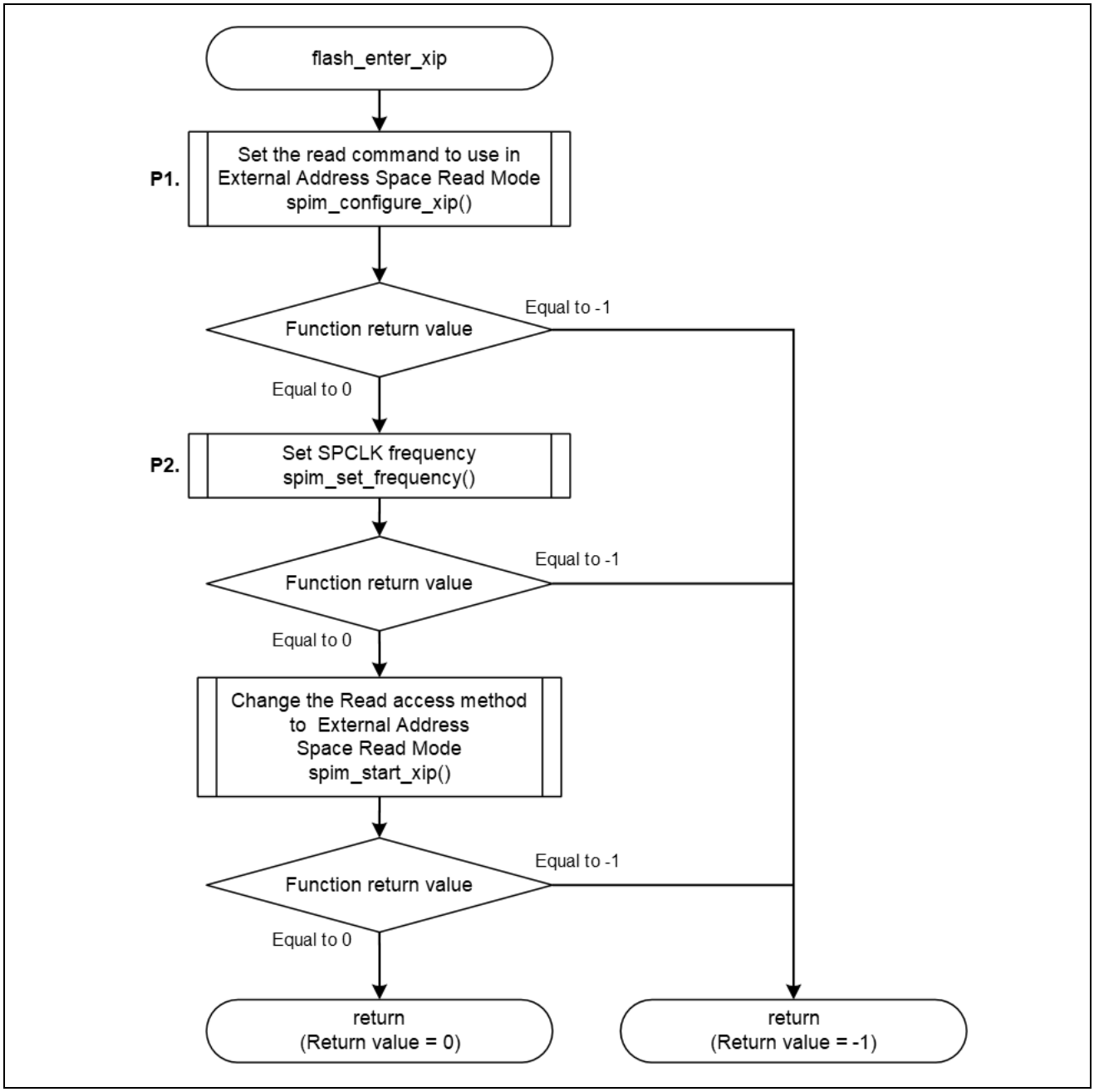


Figure 9.26 Flowchart of flash_enter_xip

P1. Register Read operation

Register the Read operation used in External Space Address Read Mode in the argument rop of spim_config_xip().

The Serial Flash memory driver implemented in the default IPL uses the Fast Read quad I/O operation (code: 0xEB) as the Read operation.

Table 9.4 shows the rop settings when using the Fast Read quad I/O operation.

When changing the Serial Flash memory, rewrite rop to the contents corresponding to the Read operation of your Serial Flash memory.

Table 9.4 rop setting contents when using Fast Read quad I/O(0xEB)

Member	Setting value	Description
form	SPI_FORM_1_4_4	Number of I/O line used for command: 1line Number of I/O line used for address: 4line Number of I/O line used for data: 4line
op	0xEB	Command code "Fast Read Quad I/O"
op_size	1	Command size = 1byte
op_is_ddr	false	Command transfer method (SDR)
address	0	Address is not set because bus access is translated
address_is_ddr	false	Address transfer method (SDR)
address_size	3	24bit address
additional_value	0x55555555	Option data
additional_size	1	Option data size
dummy_cycles	4	Dummy cycles = 4 cycles
transfer_buffer	NULL	Buffer pointer is not set because bus access is translated
transfer_is_ddr	false	Data transfer method (SDR)
transfer_size	0	Transfer data size is not set because bus access is translated
force_idle_level_mask	0x08	Keep IO3/HOLD pin to High during idle state
force_idle_level_value	0x08	Keep IO3/HOLD pin to High during idle state
slch_value	0	Clock Delay = 1.5cycle
clsh_value	0	SSL Negation Delay = 1cycle
shsl_value	6	Next Access Delay = (7 – 3) cycle

P2. Clock frequency setting change

The defined value of DEFAULT_SPI_FREQUENCY in L14 of qspiflash_custom.c shown in Figure 9.23 is used for the operating clock frequency.

Set this define value to the optimum value for your Serial Flash memory.

The maximum value that can be set is 100000000 (100MHz) and the minimum value is 3125000 (3.125MHz)

9.3.1.5 flash_exit_xip

flash_exit_xip() is a function that changes the read access method of SPIBSC from External Space Address Read Mode to Manual Mode.

flash_exit_xip	
Outline	Finish the External Address Space Read Mode
Declaration	int flash_exit_xip (xspi_ctrl_t * const ctrl)
Description	- Change the Read access method to Manual Mode
Arguments	*ctrl : Pointer to the control structure for instance
Return value	0 : This value is always returned
Note	-

Figure 9.27 shows a flowchart of the flash_exit_xip() implementation in the default IPL.

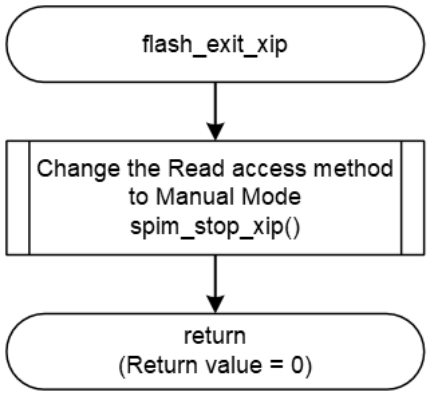


Figure 9.27 Flowchart of flash_exit_xip

9.3.1.6 flash_read

flash_read() is a function to read data from Serial Flash memory.

At IPL, Serial Flash memory operates in External Space Address Read Mode.

Therefore, flash_read() implemented in the default IPL directly reads data from the space where Serial Flash memory is mapped (0x20000000 or later) without serial communication processing of the Read operation.

flash_read	
Outline	Data read from the Serial Flash memory
Declaration	int flash_read (xspi_ctrl_t * const ctrl, void * buffer, size_t address, size_t length)
Description	- Get address information where Serial Flash memory is mapped - Copy data from the Serial Flash memory to the buffer prepared by the application that called this function
Arguments	*ctrl : Pointer to the control structure for instance * buffer : Pointer to buffer to store read data address: Data read source address Specify the offset address in the Serial Flash memory for this argument length : Read data size
Return value	0 : This value is always returned
Note	-

Figure 9.28 shows a flowchart of the flash_read() implementation in the default IPL.

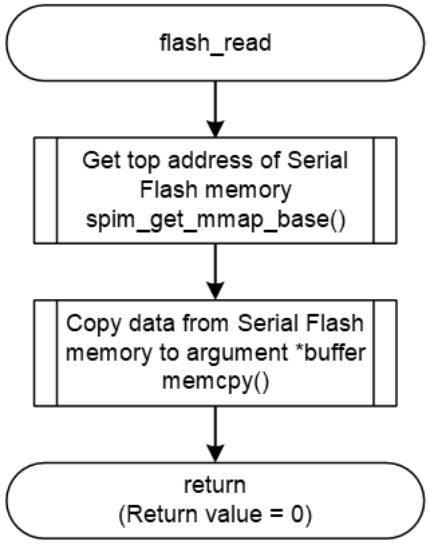


Figure 9.28 Flowchart of flash_read

9.3.1.7 flash_write

flash_write() is a function to write data to Serial Flash memory.

flash_write() implemented in the default IPL writes data by sending the Write operation of the AT25QL128A mounted on the SMARC EVK board.

flash_write	
Outline	Data write to the Serial Flash memory
Declaration	int flash_write (xspi_ctrl_t * const ctrl, void const * buffer, size_t address, size_t length)
Description	- Checking the write status - Waiting for the end of the write process - Release write protection - Updating the write operation table - Write data by sending write operation data to Serial Flash memory
Arguments	*ctrl : Pointer to the control structure for instance * buffer : Pointer to buffer where write data is stored address: Data write destination address Specify the offset address in the Serial Flash memory for this argument length : Write data size
Return value	0 : Data write is success -1 : Data write is failed
Note	Processing of this function is disabled at the default IPL. To enable it, refer to Figure 9.29 and rewrite RZ_XSPIFLASH_DISABLE_WRITE:=1 in rz_xspi_common.mk L13 to RZ_XSPIFLASH_DISABLE_WRITE:=0 and rebuild.

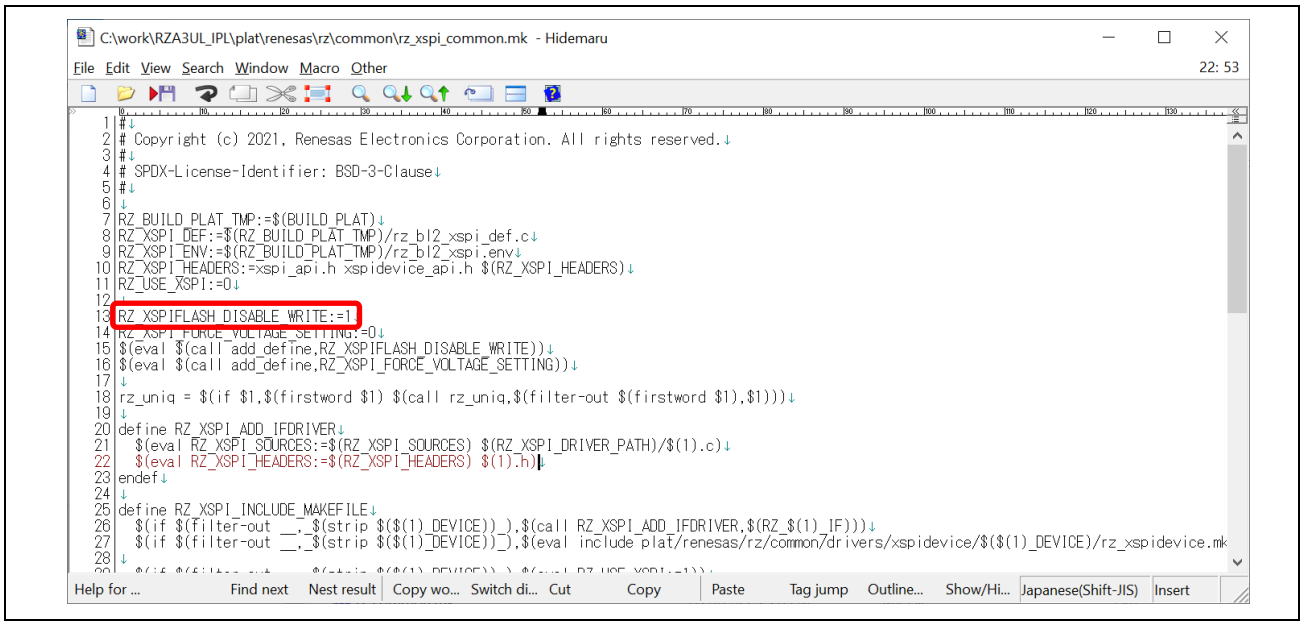


Figure 9.29 Change build switch for write function

Figure 9.30 and Figure 9.31 show the flowchart of the flash_write() implementation in the default IPL.

The processing that changes the implementation when changing the Serial Flash memory is shown below.

- P1. Wait process of write completion
- P2. Release write protect
- P3. Setting of Write operation table

These are shown as P1 to P3 in the flow chart as implementation change points.

The details of the processing are explained after the flow chart.

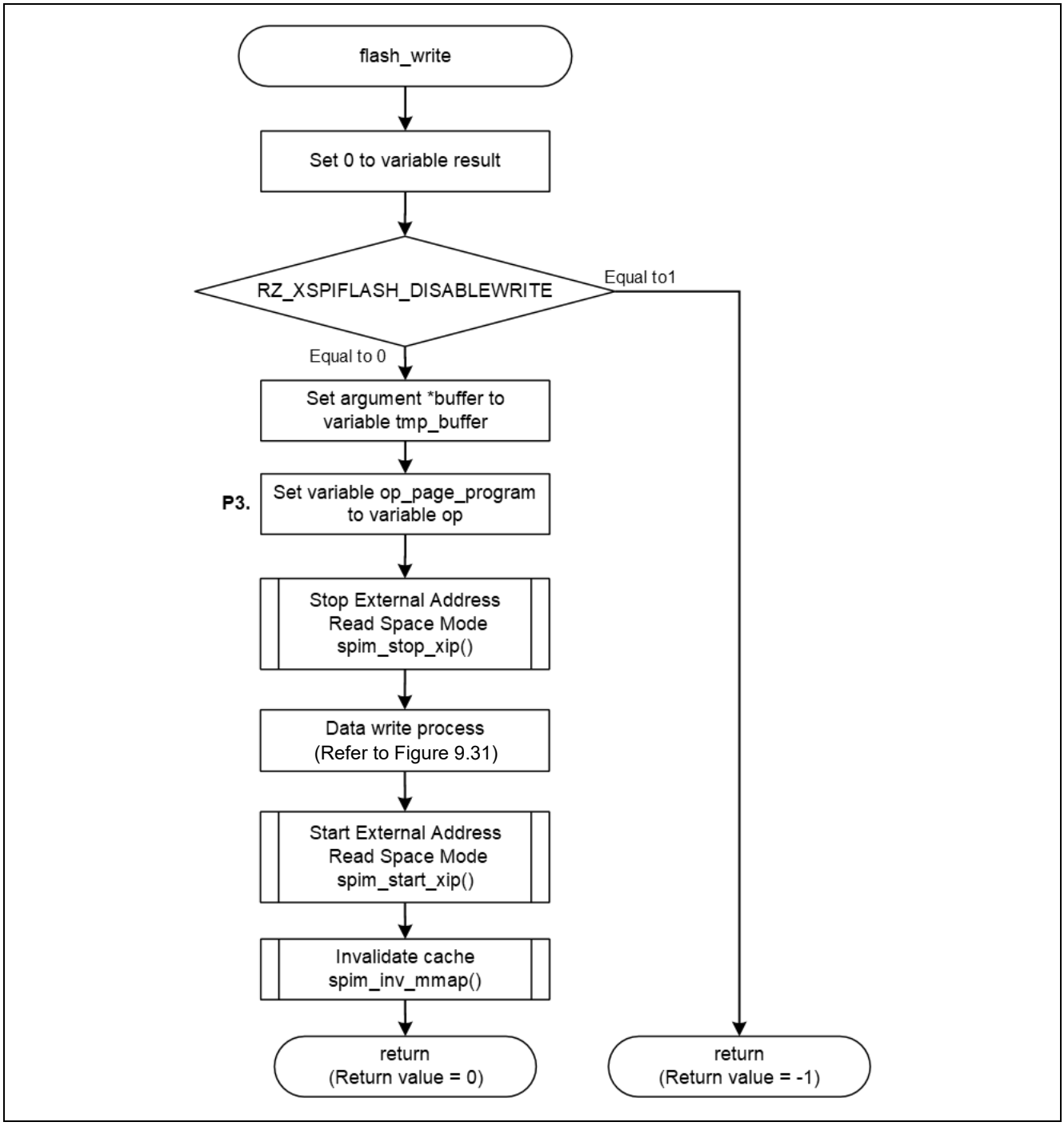


Figure 9.30 Flowchart of flash_write

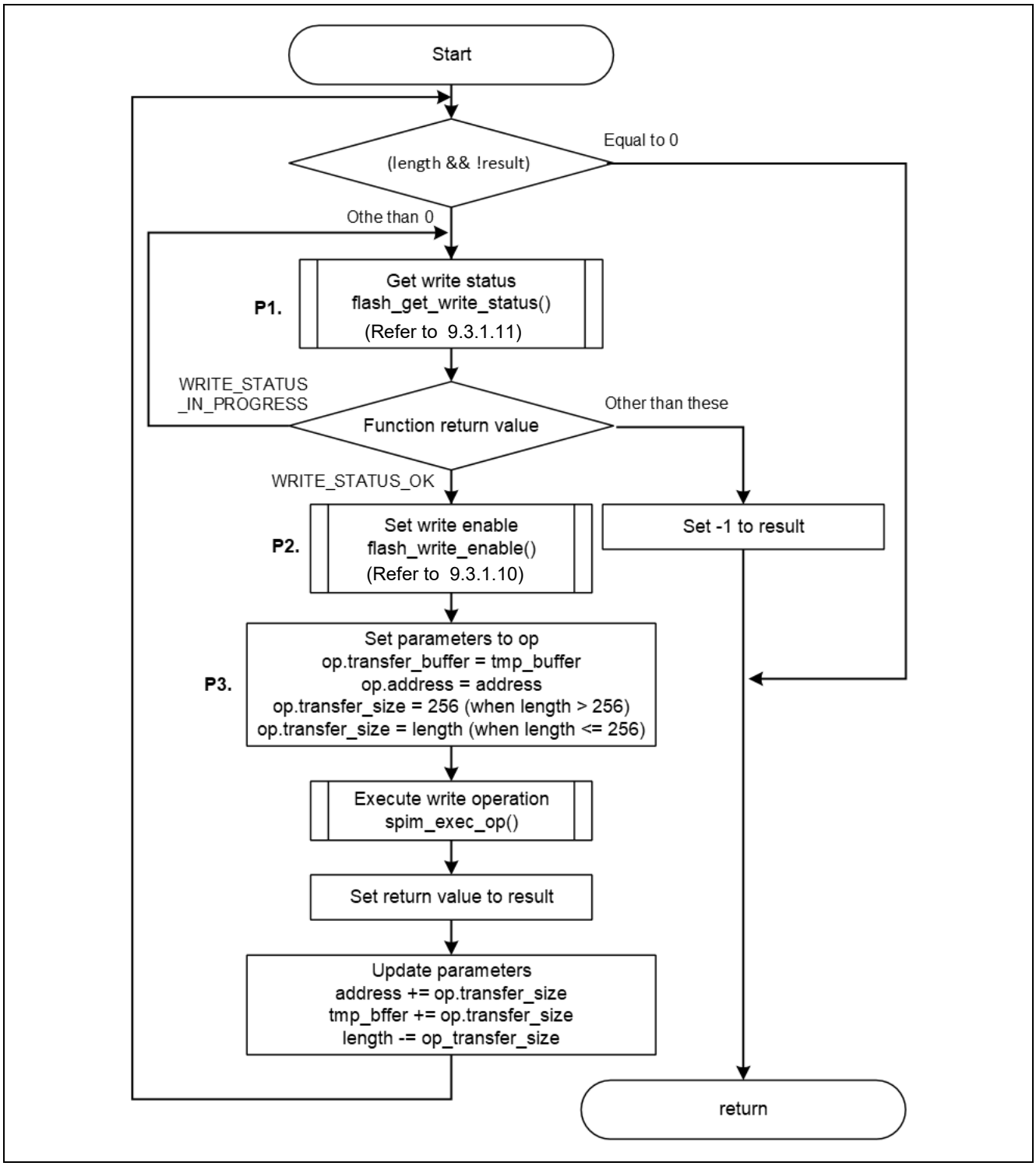


Figure 9.31 Flowchart of Data write process

P1.Wait process of write completion

Since the next data cannot be received while the Serial Flash memory is writing the data received by serial communication or erasing the data, IPL must check the write status and wait for the end.

The sub function flash_get_write_status() for getting the write status for the AT25QL128A is implemented in the Serial Flash memory driver implemented in the default IPL.

Since the method of checking the write status depends on the Serial Flash memory specifications, it is necessary to change the implementation of the function when changing the memory.

Please refer to 9.3.1.9 for change of checking method of write status.

P2. Release Write Protect

Most of Serial Flash memories require release of write protect when writing data or erasing data.

The Serial Flash memory driver implemented in the default IPL provides a sub function flash_write_enable() that release Write Protect for AT25QL128A.

Since the write protect release method depends on the specifications of the Serial Flash memory, it is necessary to change the implementation of the function when changing the memory.

Please refer to 9.3.1.10 for change of write protect release method.

P3. Setting Write operation table

When writing data to Serial Flash memory, data is written by sending a Write command.

The Serial Flash memory driver implemented in the default IPL sets the AT25QL128A's Quad Page program operation (code: 0x33) to the variable op_page_program as the Write operation and sends it.

Table 9.5shows the settings of op_page_program_dopi when using Quad Page program.

When changing the Serial Flash memory, refer to Table 9.5 and rewrite the setting contents of op_page_program to the contents corresponding to the Write operation of your Serial Flash memory.

Note that the write destination address and the size of data that can be written with one write operation are limited by the operations implemented in the Serial Flash memory.

The Page program operation requires writing to start from a 256 byte aligned address.

Also, with this operation, the write data size per write is up to 256 byte, so flash_write() repeatedly transfers data in units of 256 byte.

Similarly, adjust the write destination address and transfer data size per transfer according to the specifications of the Write operation that uses it

Table 9.5 op_page_program setting contents when using Quad Page Program (0x33)

Member	Setting value	Description
form	SPI_FORM_1_4_4	Number of I/O line used for command: 1line Number of I/O line used for address: 4line Number of I/O line used for data: 4line
op	0x33	Command code "Quad Page Program"
op_size	1	Command size = 1byte
op_is_ddr	false	Command transfer method (SDR)
address	address	Address is Serial Flash memory address to data write It is updated in the function
address_is_ddr	false	Address transfer method (SDR)
address_size	3	24bit address
additional_value	0	No option data
additional_size	0	No option data
dummy_cycles	0	Dummy cycles = 0 cycles
transfer_buffer	tmp_buffer	tmp_buffer is buffer address of write data It is updated in the function
transfer_is_ddr	false	Data transfer method (SDR)
transfer_size	length	length is remaining size of write data It is updated in the function
force_idle_level_mask	0x08	Keep IO3/HOLD pin to High during idle state
force_idle_level_value	0x08	Keep IO3/HOLD pin to High during idle state
slch_value	0	Clock Delay = 1.5cycle
clsh_value	0	SSL Negation Delay = 1cycle
shsl_value	6	Next Access Delay = (7 – 3) cycle

9.3.1.8 flash_erase

flash_erase() is a function to erase data from Serial Flash memory.

flash_erase() implemented in the default IPL erase data by sending the Erase operation of the AT25QL128A mounted on the SMARC EVK board

flash_erase	
Outline	Erase the Serial Flash memory
Declaration	int flash_erase (xspidevice_ctrl_t * ctrl, size_t address, size_t length)
Description	- Checking the write status - Waiting for the end of the write process - Release write protection - Updating the erase operation table - Erase data by sending erase operation data to Serial Flash memory
Arguments	*ctrl : Pointer to the control structure for instance address: Start address for data erase Specify the offset address in the Serial Flash memory for this argument. If a value other than a multiple of 4Kbytes is set, the address obtained by aligning the specified address with 4Kbytes will be the start address of the erase area. length : erase size If a value other than 4Kbyte aligned size is set in this argument, it erases the data up to the 4Kbyte aligned address including the specified range.
Return value	0 : Data erase is success -1 : Data erase is failed.
Note	Processing of this function is disabled at the default IPL. To enable it, refer to Figure 9.29 and rewrite RZ_XSPIFLASH_DISABLE_WRITE:=1 in rz_xspi_common.mk L13 to RZ_XSPIFLASH_DISABLE_WRITE:=0 and rebuild.

Figure 9.32 and Figure 9.33 show the flowchart of the flash_erase() implementation in the default IPL.

The processing that changes the implementation when changing the Serial Flash memory is shown below.

- P1. Wait process of write completion
- P2. Release Write Protect
- P3. Send Erase operation

These are shown as P1 to P3 in the flow chart as implementation change points.

The details of the processing are explained after the flow chart.

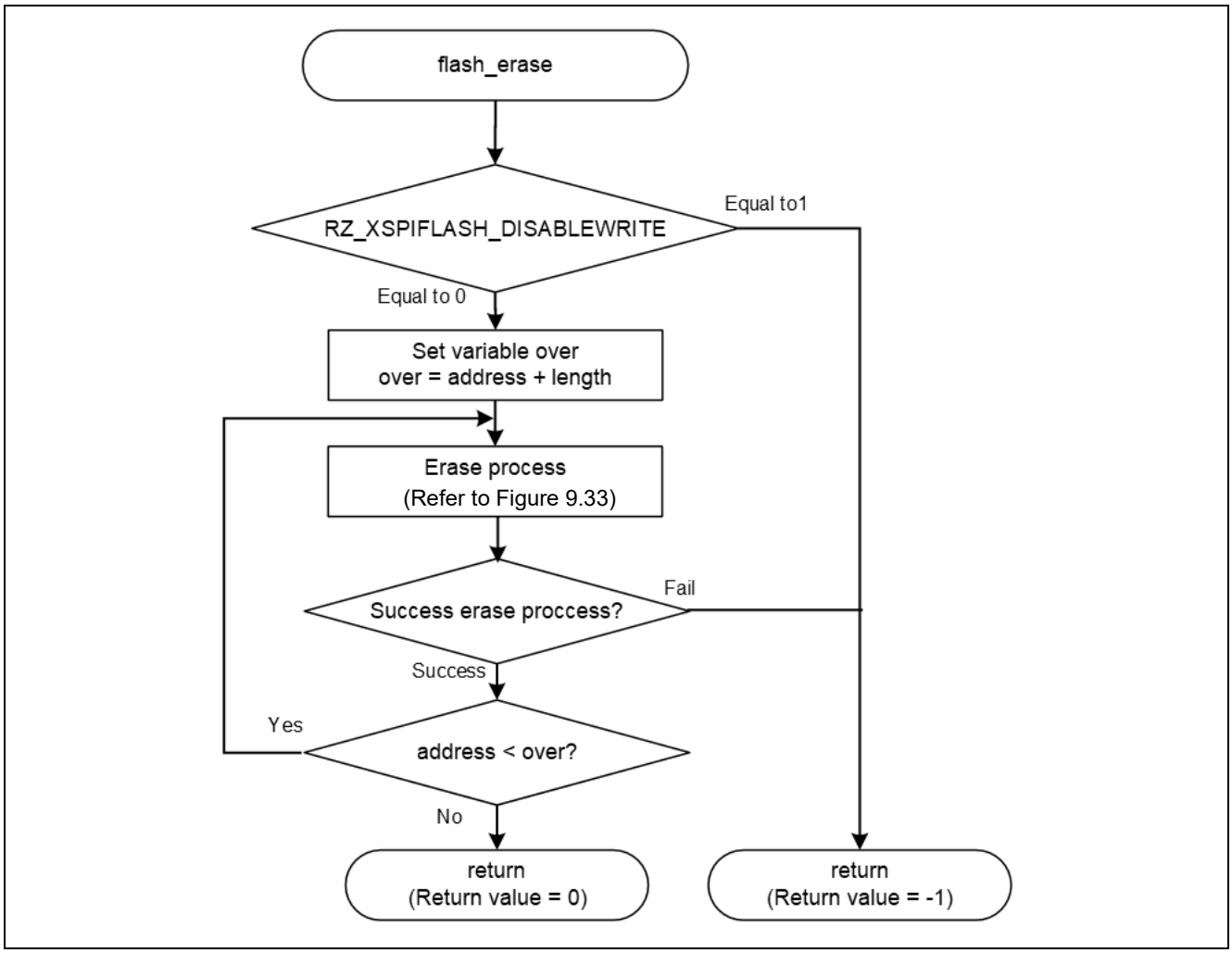


Figure 9.32 Flowchart of flash_erase

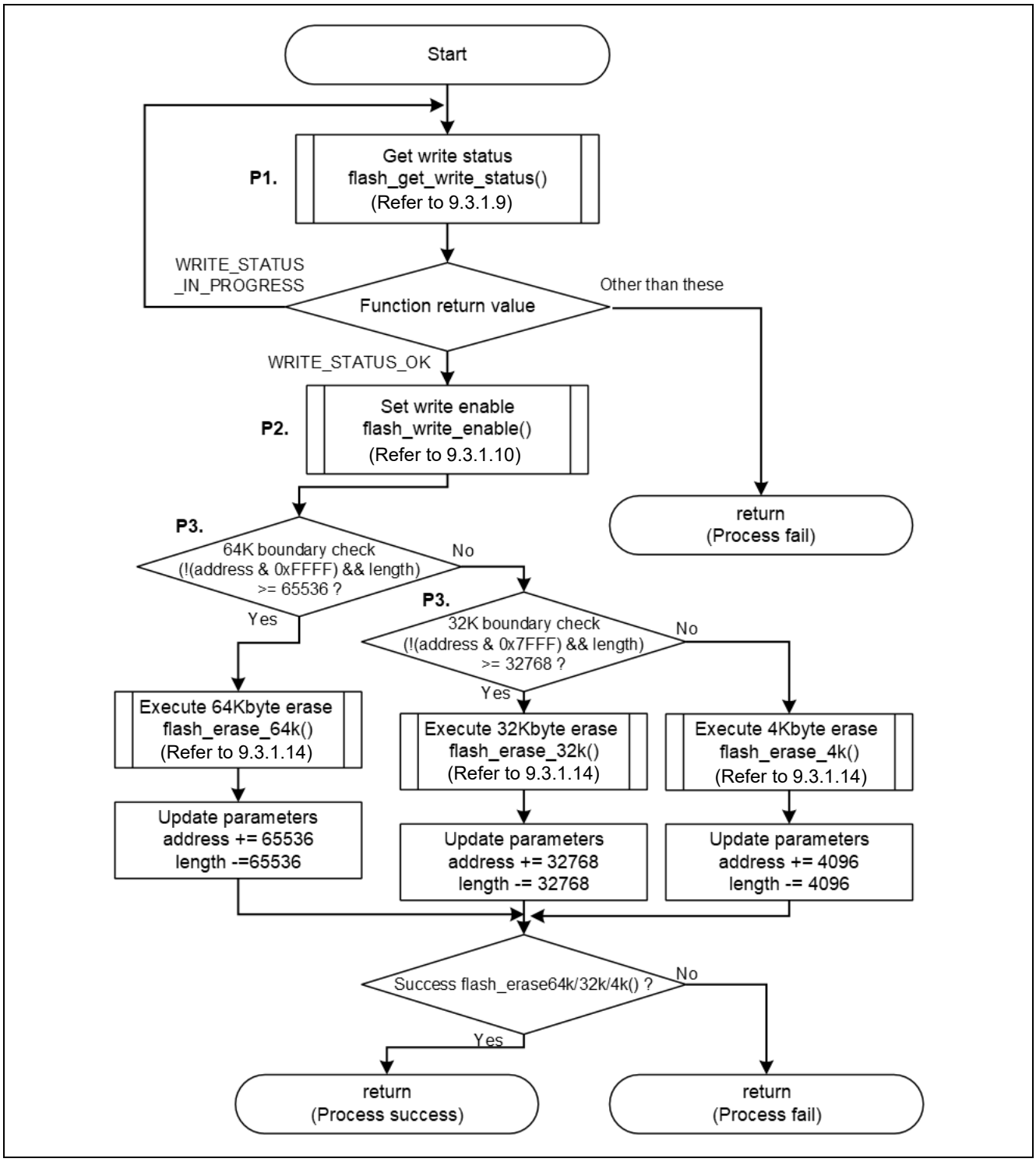


Figure 9.33 Flowchart of Erase process

P1. Wait process of write completion

Since the next data cannot be received while the Serial Flash memory is writing the data received by serial communication or erasing the data, IPL must check the write status and wait for the end.

The sub function flash_get_write_status() for getting the write status for the AT25QL128A is implemented in the Serial Flash memory driver implemented in the default IPL.

Since the method of checking the write status depends on the Serial Flash memory specifications, it is necessary to change the implementation of the function when changing the memory.

Please refer to 9.3.1.9 for change of checking method of write status.

P2. Release Write Protect

Most of Serial Flash memories require release of write protect when writing data or erasing data.

The Serial Flash memory driver implemented in the default IPL provides a sub function flash_write_enable() that release Write Protect for AT25QL128A.

Since the write protect release method depends on the specifications of the Serial Flash memory, it is necessary to change the implementation of the function when changing the memory.

Please refer to 9.3.1.10 for change of write protect release method.

3. Send Erase Operation

When erasing data to Serial Flash memory, data is erased by sending a Erase command.

The AT25QL128A provides an Erase operation in 4Kbyte units (Block erase (4kbytes)), Erase operation in 32Kbyte units (Block erase (32kbytes)) and Erase operation in 64Kbyte units (Block erase (64kbytes)).

Therefore, the Serial Flash memory driver implemented in the default IPL switches the Erase operation to be executed according to the remaining erase size as shown below.

- Remaining Erase size is 64Kbyte or more: Block erase (64kbytes)
- Remaining Erase size is 32Kbyte or more and less than 64Kbyte: Block erase (32kbytes)
- Remaining Erase size is less than 32Kbyte: Block erase (4kbytes)

These erase operations are executed by the sub functions flash_erase_4k() / flash_erase_32k() / flash_erase_64k() corresponding to each operation.

Refer to 9.3.1.14 for how to change the erase operation execution process.

The size unit that can be erased depends on the operations implemented in the Serial Flash memory.

Adjust the erase unit of the program according to the erase unit of the erase operation provided by your Serial Flash memory.

9.3.1.9 flash_get_write_status

flash_get_write_status() is a function to get the write status of the Serial Flash memory.

flash_get_write_status() implemented in the default IPL checks the write status by reading the Status Register of the AT25QL128A mounted on the SMARC EVK board.

flash_get_write_status	
Outline	Gets the write status of the Serial Flash memory
Declaration	int flash_get_write_status (xspidevice_ctrl_t * ctrl)
Description	- Read Status Register - Return from a function with a return value that depends on the value of the Status Register
Arguments	*ctrl : Pointer to the control structure for instance
Return value	WRITE_STATUS_FAIL : Data write is failed WRITE_STATUS_IN_PROGRESS : Data write in progress WRITE_STATUS_OK : Data write is complete
Note	-

Figure 9.34 shows a flowchart of the flash_get_write_status() implementation in the default IPL.

The processing that changes the implementation when changing the Serial Flash memory is shown below.

- P1 Read status register

This is shown as P1 in the flow chart as implementation change points.

The details of the processing are explained after the flow chart.

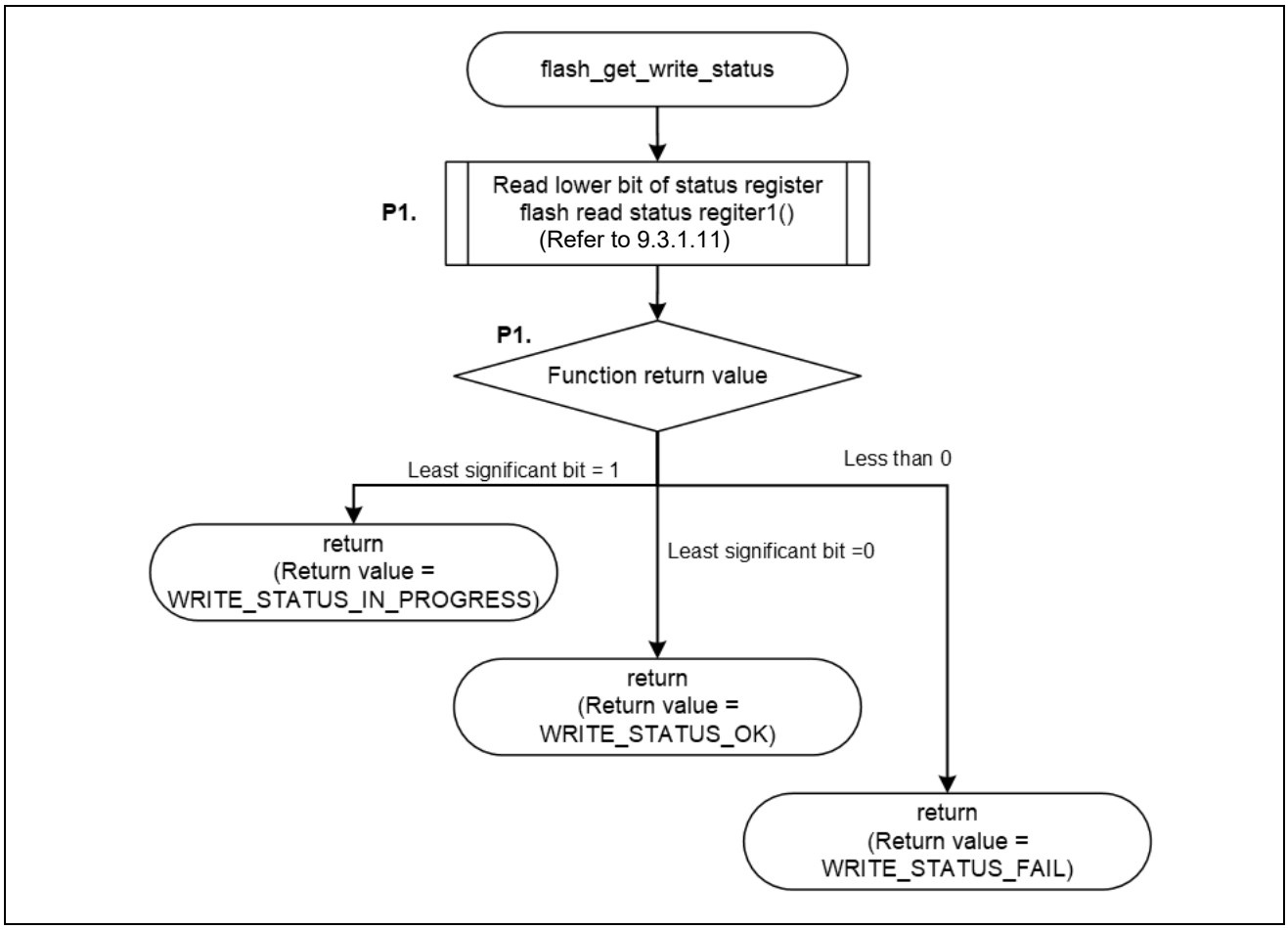


Figure 9.34 Flowchart of flash_get_write_status

P1. Read Status Register

AT25QL128A has Status Register shown in Table 9.6.

The BUSY bit in this register indicates whether it is in Write (Erase) or idle.

Therefore, the Serial Flash memory driver implemented at default IPL reads the Status Register.

If the value of the Status Register is checked and the WIP bit is 1, a return value indicating that processing is in progress is returned, and if it is 0, a return value indicating that processing has ended is returned.

The default IPL provides a sub-function flash_read_status_register1() that reads the Status Register of the AT25QL128A.

Refer to 9.3.1.9 for how to read the Status Register.

When changing the Serial flash memory, read the register corresponding to the AT25QL128A Status Register and change the source code so that the bit indicating the Erase or Write status is checked to determine the status.

Table 9.6 BUSY bit of AT25QL128A Status Register (BIT7 – Bit 0)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
SRP	SEC	TB	BP2	BP1	BP0	WEL	BUSY
Status Register Protect 0	Selector Protect	Top/Bottom Write Protect	Block Protect	Block Protect	Block Protect	Write Enable Latch	Erase or Write in Progress

9.3.1.10 flash_write_enable

flash_write_enable() implemented in the default IPL release Write Protect by sending the Write Enable operation of the AT25QL128A mounted on the SMARC EVK board.

flash_write_enable	
Outline	Set Write enable to AT25QL128A
Declaration	int flash_write_enable (qspiflash_at25_ctrl_t * myctrl)
Description	- Send Write Enable operation to Serial Flash memory
Arguments	*myctrl : Pointer to the control structure for instance
Return value	0 : Operation success
	-1 : Operation Failed
Note	-

Figure 9.35 shows a flowchart of the flash_write_enable() implementation in the default IPL.

The processing that changes the implementation when changing the Serial Flash memory is shown below.

- P1 Send Write Enable operation

This is shown as P1 in the flow chart as implementation change points.

The details of the processing are explained after the flow chart.

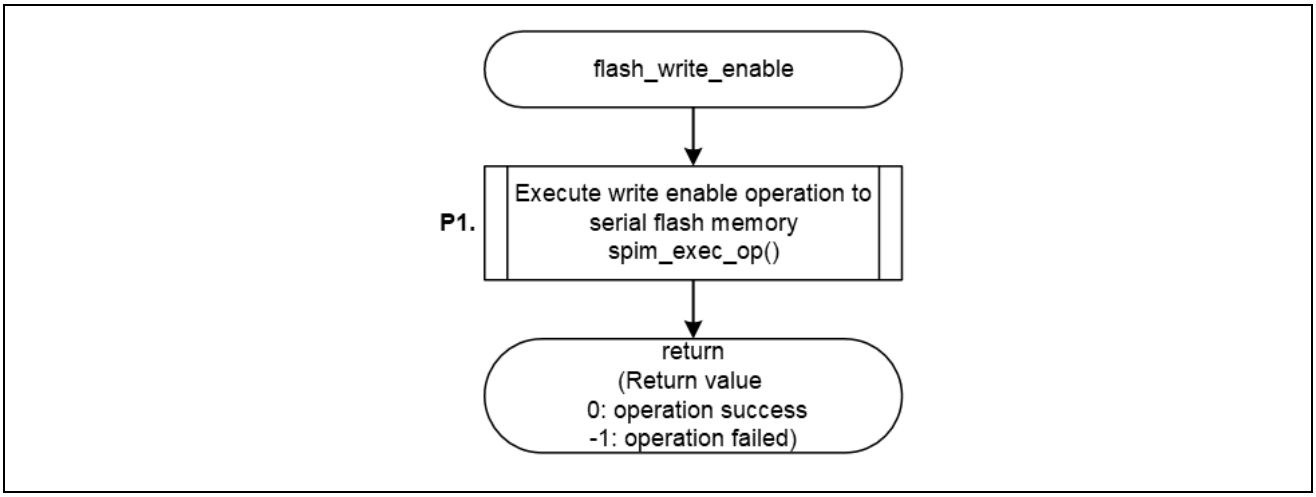


Figure 9.35 Flowchart of flash_write_enable

P1. Send Write Enable operation

The Write Enable setting to the Serial Flash memory is performed by sending the Write Enable command.

The Serial Flash memory driver implemented in the default IPL sets the AT25QL128A Write Enable command (code: 0x06) to the variable op_write_enable as the Write Enable operation, and the Write Enable information is sent by serial communication.

Table 9.7 shows the op_write_enable settings when using the Write Enable operation.

When changing the Serial Flash memory, refer to Table 9.7 and rewrite the setting contents of op_write_enable to the contents equivalent to the Write Enable operation of your Serial Flash memory.

In addition, there are Serial Flash memories that require register access in a specific procedure when executing Write Enable.

In such cases, execute the operation transfer flow according to the determined procedure.

Table 9.7 op_write_enable setting contents when using Write Enable (0x06)

Member	Setting value	Description
form	SPI_FORM_1_1_1	Number of I/O line used for command: 1 line Number of I/O line used for address: 1 line Number of I/O line used for data: 1 line
op	0x06	Command code "Write Enable"
op_size	1	Command size = 1byte
op_is_ddr	false	Command transfer method (SDR)
address	0	No address
address_is_ddr	false	Address transfer method (SDR)
address_size	0	No address
additional_value	0	No option data
additional_size	0	No option data
dummy_cycles	0	Dummy cycles = 0 cycles
transfer_buffer	NULL	No data
transfer_is_ddr	false	Data transfer method (SDR)
transfer_size	0	No data
force_idle_level_mask	0x08	Keep IO3/HOLD pin to High during idle state
force_idle_level_value	0x08	Keep IO3/HOLD pin to High during idle state
slch_value	0	Clock Delay = 1.5cycle
clsh_value	0	SSL Negation Delay = 1cycle
shsl_value	6	Next Access Delay = (7 – 3) cycle

9.3.1.11 flash_read_status_reister1 / flash_read_status_register2

flash_read_status_reister1() / flash_read_status_reister2() are the function to read Status Register value of AT25QL128A mounted on the SMARC EVK board.

These functions implemented in the default IPL read value from Status Register by sending the Read Status Register operation of the AT25QL128A.

The AT25QL128A Status Register is a 16bit register, and flash_read_status_reister1() reads the value of the lower 8 bits of the Status Register by sending the Read Status Register1 operation.

flash_read_status_reister2() reads the value of the upper 8 bits of the Status Register by sending a Read Status Register2 operation.

These functions are similar in function definition and process flow.

flash_read_status_register1 / flash_read_status_register2	
Outline	Gets the status register of the Serial Flash memory
Declaration	int flash_read_status_register1(qspiflash_at25_ctrl_t * myctrl) int flash_read_status_register2(qspiflash_at25_ctrl_t * myctrl)
Description	- Send Read Status Register operation to Serial Flash memory and get register value
Arguments	*myctrl : Pointer to the control structure for instance
Return value	Positive Number: Operation success, and status register value -1 : Operation Failed
Note	-

Figure 9.36 shows a flowchart of the flash_read_status_register1() implementation in the default IPL.

The processing that changes the implementation when changing the Serial Flash memory is shown below.

- P1 Send Read Status Register 1/ Read Status Register2 operation

This is shown as P1 in the flow chart as implementation change points.

The details of the processing are explained after the flow chart.

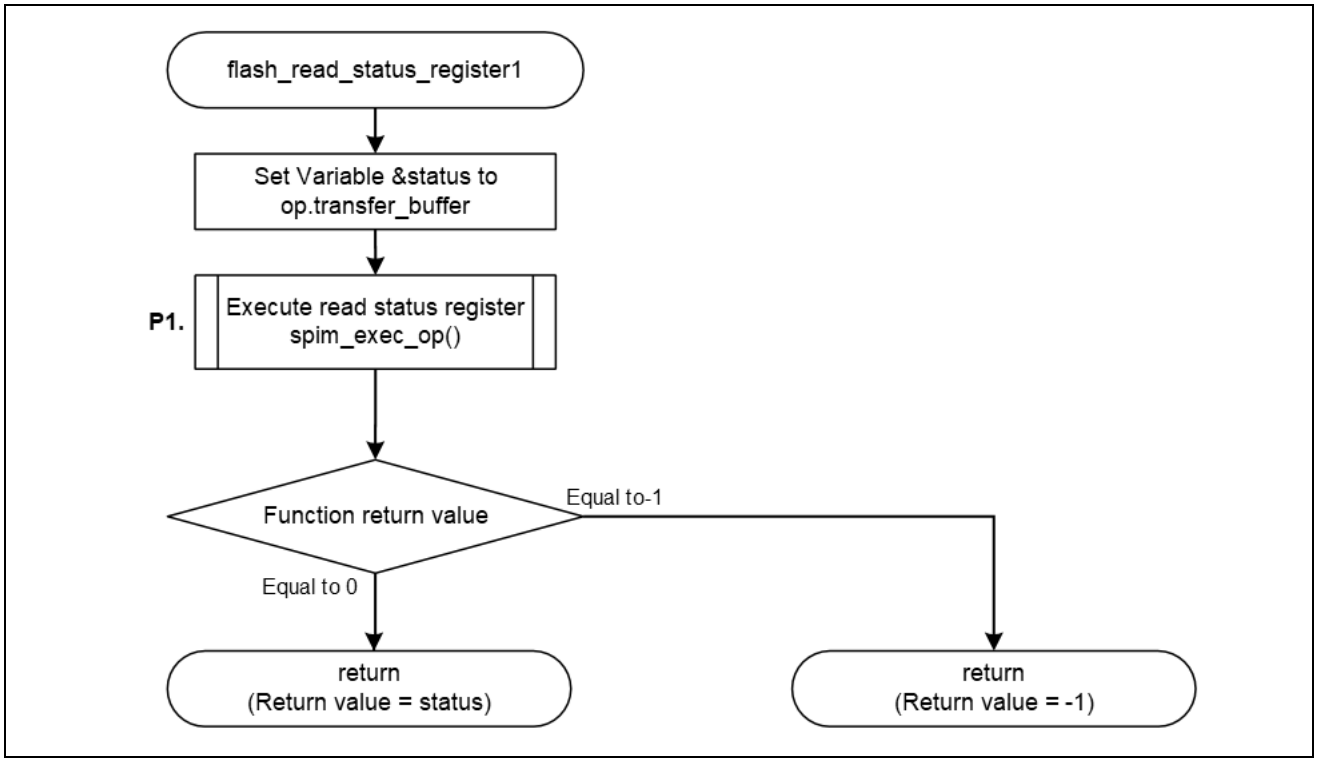


Figure 9.36 Flowchart of flash_read_status_register1

P1. Send Read Status Register1 / Read Status Register2 operation

Send the Read Status Register operation to get the Status Register value from the Serial Flash memory.

The flash_read_status_regster1() function sets the Read Status Register1 command (0x05) to the variable op_read_status1, the flash_read_status_regster2() function sets the Read Status Register2 command (0x35) to the variable op_read_status2, and each function sends the Read Status Register operation.

Table 9.8 shows the settings of op_read_status1 when using the Read Status Register1 operation, and Table 9.9 shows the settings of op_read_status2 when using the Read Status Register2 operation.

When changing the Serial Flash memory, rewrite the variable members according to the specifications of the command equivalent to the AT25QL128A's Read Status Register operation implemented in your Serial Flash memory.

Table 9.8 op_read_status1 setting contents when using Read Status Register1 (0x05)

Member	Setting value	Description
form	SPI_FORM_1_1_1	Number of I/O line used for command: 1 line Number of I/O line used for address: 1 line Number of I/O line used for data: 1 line
op	0x05	Command code "Read Status Register1"
op_size	1	Command size = 1byte
op_is_ddr	false	Command transfer method (SDR)
address	0	No address
address_is_ddr	false	Address transfer method (SDR)
address_size	0	No address
additional_value	0	No option data
additional_size	0	No option data
dummy_cycles	0	Dummy cycles = 0 cycles
transfer_buffer	&status	Set pointer of argument status in function
transfer_is_ddr	false	Data transfer method (SDR)
transfer_size	1	Higher 8bit of Status Register
force_idle_level_mask	0x08	Keep IO3/HOLD pin to High during idle state
force_idle_level_value	0x08	Keep IO3/HOLD pin to High during idle state
slch_value	0	Clock Delay = 1.5cycle
clsh_value	0	SSL Negation Delay = 1cycle
shsl_value	6	Next Access Delay = (7 – 3) cycle

Table 9.9 op_read_status2 setting contents when using Read Status Register2 (0x35)

Member	Setting value	Description
form	SPI_FORM_1_1_1	Number of I/O line used for command: 1 line Number of I/O line used for address: 1 line Number of I/O line used for data: 1 line
op	0x35	Command code "Read Status Register2"
op_size	1	Command size = 1byte
op_is_ddr	false	Command transfer method (SDR)
address	0	No address
address_is_ddr	false	Address transfer method (SDR)
address_size	0	No address
additional_value	0	No option data
additional_size	0	No option data
dummy_cycles	0	Dummy cycles = 0 cycles
transfer_buffer	&status	Set pointer of argument status in function
transfer_is_ddr	false	Data transfer method (SDR)
transfer_size	1	Lower 8bit of Status Register
force_idle_level_mask	0x08	Keep IO3/HOLD pin to High during idle state
force_idle_level_value	0x08	Keep IO3/HOLD pin to High during idle state
slch_value	0	Clock Delay = 1.5cycle
clsh_value	0	SSL Negation Delay = 1cycle
shsl_value	6	Next Access Delay = (7 – 3) cycle

9.3.1.12 flash_write_status_register2

flash_write_status_reister2() is a function that writes value to the upper 8bits of the AT25QL128A Status Register.

flash_write_status_reister2() implemented in the default IPL write value to the register by sending the Write Status Register2 operation of the AT25QL128A mounted on the SMARC EVK board.

flash_write_status_register2	
Outline	Set value to higher 8bit of Status Register
Declaration	int flash_write_status_register2(qspiflash_at25_ctrl_t * myctrl, uint8_t status)
Description	- Send Write Status Register2 operation and write value to Status Register
Arguments	*myctrl : Pointer to the control structure for instance
	status : Setting value to Status Register
Return value	0 : Operation success
	-1 : Operation Failed
Note	-

Figure 9.37 shows a flowchart of the flash_write_status_register2() implementation in the default IPL.

The processing that changes the implementation when changing the Serial Flash memory is shown below.

- P1 Send Write Status Register2 operation

This is shown as P1 in the flow chart as implementation change points.

The details of the processing are explained after the flow chart.

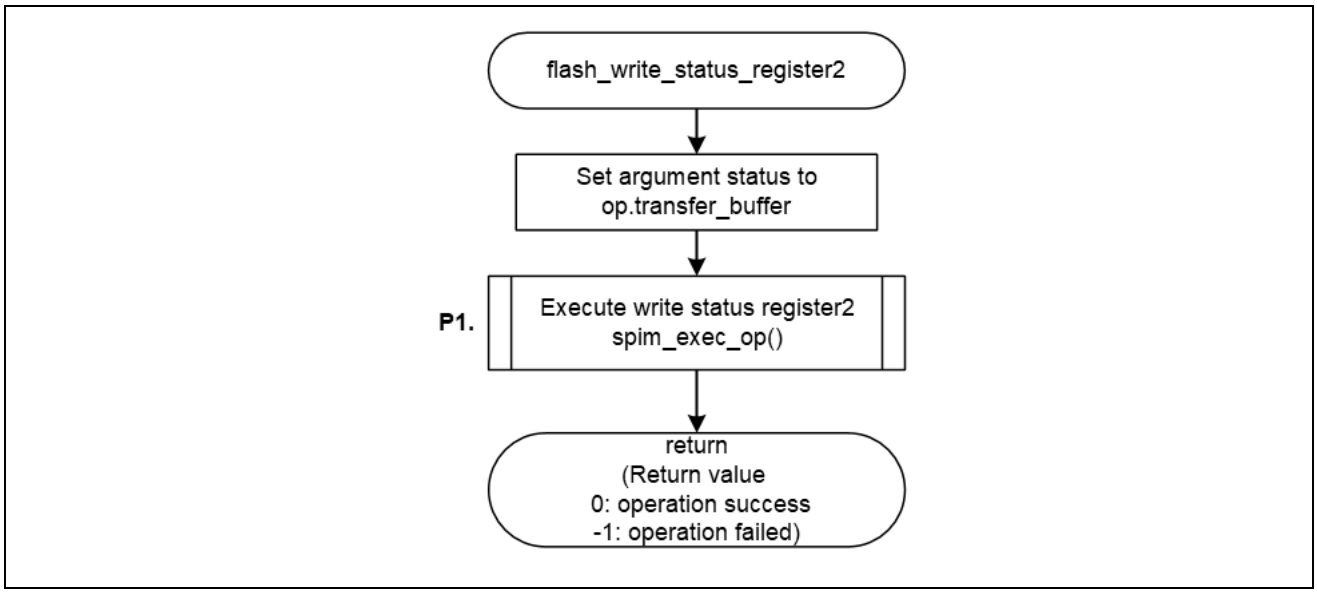


Figure 9.37 Flowchart of flash_write_status_register2

P1. Send Write Status Register2 operation

Send a Write Status Register command to write the value to the Status Register.

The flash_write_status_regster2() function sets the Write Status Register2 command (0x31) to the variable op_write_status2 and sends the Write Status Register operation.

Table 9.10 shows the settings of op_write_status2 when using the Write Status Register2 operation.

When changing the Serial Flash memory, rewrite the variable members according to the specifications of the operation equivalent to the AT25QL128A Write Status Register2 operation implemented in your Serial Flash memory.

Table 9.10 op_write_status2 setting contents when using Write Status Register2 (0x31)

Member	Setting value	Description
form	SPI_FORM_1_1_1	Number of I/O line used for command: 1line Number of I/O line used for address: 1line Number of I/O line used for data: 1line
op	0x05	Command code "Write Status Register2"
op_size	1	Command size = 1byte
op_is_ddr	false	Command transfer method (SDR)
address	0	No address
address_is_ddr	false	Address transfer method (SDR)
address_size	0	No address
additional_value	0	No option data
additional_size	0	No option data
dummy_cycles	0	Dummy cycles = 0 cycles
transfer_buffer	&status	Set pointer of argument status in function
transfer_is_ddr	false	Data transfer method (SDR)
transfer_size	1	Lower 8bit of Status Register
force_idle_level_mask	0x08	Keep IO3/HOLD pin to High during idle state
force_idle_level_value	0x08	Keep IO3/HOLD pin to High during idle state
slch_value	0	Clock Delay = 1.5cycle
clsh_value	0	SSL Negation Delay = 1cycle
shsl_value	6	Next Access Delay = (7 – 3) cycle

9.3.1.13 flash_set_qe

flash_set_qe() is a function that set Quad Enable bit of AT25QL128A.

flash_set_qe() implemented in the default IPL sets Quad Enable bit by Writing value to Status Register of the MX66UW1G45G mounted on the SMARC EVK board.

flash_set_qe	
Outline	Set the QE bit of Status Register
Declaration	int flash_set_qe(qspiflash_at25_ctrl_t * myctrl)
Description	- Read Status Register value - Check Quad Enable bit - Check Write Protect of Status Register - Release Write Protect - Change Quad Enable mode
Arguments	*myctrl : Pointer to the control structure for instance
Return value	0 : Operation success -1 : Operation Failed
Note	-

Figure 9.38 show the flowchart of the flash_set_qe() implementation in the default IPL.

The processing that changes the implementation when changing the Serial Flash memory is shown below.

- P1. Check Quad Enable
- P2. Release Write Protect
- P3. Change mode of Quad Enable

These are shown as P1 to P3 in the flow chart as implementation change points.

The details of the processing are explained after the flow chart.

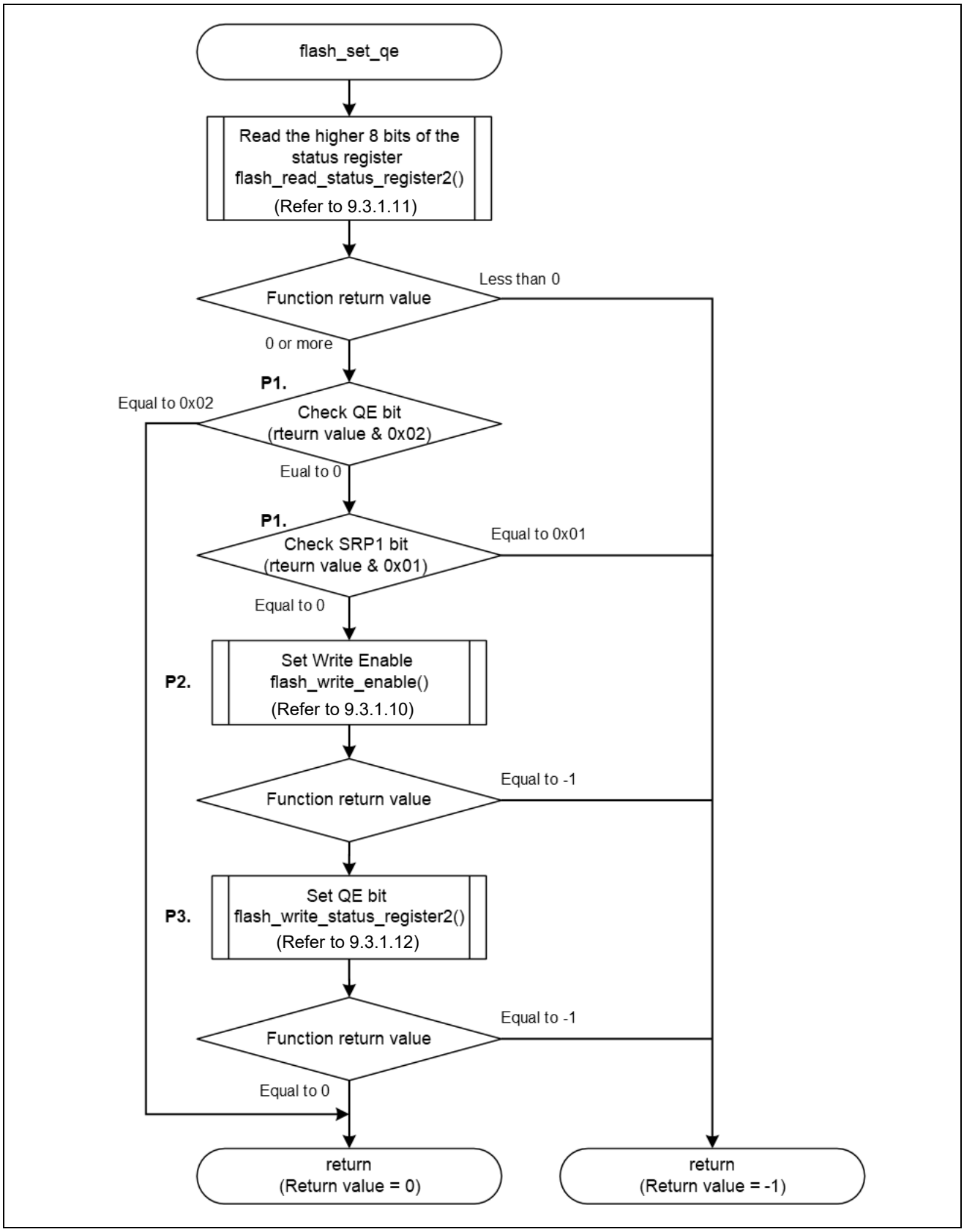


Figure 9.38 Flowchart of flash_set_qe

P1. Check Quad Enable

The flash_set_qe() function once obtains the Status Register value shown in Table 9.11 and skips processing if the QE bit has already been set.

Also, if the SRP1 bit is set, the Status Register is protected and cannot be changed, so the function terminates as an error.

The bits used to determine these processing branches vary depending on the implementation of the Serial Flash memory.

Therefore, when changing the Serial Flash memory, use the bits implemented in your Serial Flash memory that correspond to the SRP1 bit and QE bit to check.

To get the Status Register, execute flash_read_status_register2().

Refer to 9.3.1.11 for processing details.

Table 9.11 QE bit and SRP1 bit of AT25QL128A Status Register (BIT15 – Bit 8)

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
SUS	CMP	-	-	-	-	QE	SRP1
Suspend Status	Complement Protect	Reserved	Reserved	Reserved	Reserved	Quad Enable	Register Protect1

P2. Release Write Protect

AT25QL128A must release write protect when writing to Status Register.

The Serial Flash memory driver implemented in the default IPL provides a sub function flash_write_enable() that release Write Protect for AT25QL128A.

Since the write protect release method depends on the specifications of the Serial Flash memory, it is necessary to change the implementation of the function when changing the memory.

Please refer to 9.3.1.10 for change of write protect release method.

P3. Change mode of Quad Enable

By passing 0x02 as the register write value to the sub-function flash_write_status_register2() that writes to the Status Register, it writes to the Status Register and sets the QE bit.

Similarly, when changing the Serial Flash memory, set appropriate values for the registers mounted in that memory and perform register operations.

Please refer to 9.3.1.12 for changing the writing method to the Status Register.

For the AT25QL128A, writing 1 to the SRP1 bit protects the Status Register from being written and disables rewriting.

Be sure to set 0 when writing to the Status Register in processing for the AT25QL128A.

9.3.1.14 flash_erase_4k / flash_erase_32k / flash_erase_64k

flash_erase_4k() / flash_erase_32k() / flash_erase_64k() are functions to erase data in units of 4Kbyte, 32Kbyte, and 64Kbyte respectively from AT25QL128A implemented in SMARC EVK board.

flash_erase_4k() / flash_erase_32k() / flash_erase_64k() implemented in the default IPL send Block Erase(4kbytes), Block Erase(32kbytes), Block Erase(64kbytes) commands of AT25QL128A to erase data.

These functions are similar in function definition and process flow.

flash_erase_4k / flash_erase_32k / flash_erase_64k	
Outline	Erase data by 4Kbytes / 32Kbytes / 64Kbytes
Declaration	int flash_erase_4k(qspiflash_at25_ctrl_t * myctrl) int flash_erase_32k(qspiflash_at25_ctrl_t * myctrl) int flash_erase_64k(qspiflash_at25_ctrl_t * myctrl)
Description	- Check size of data to be erased - Updating the erase operation table - Erase data by sending erase operation
Arguments	*myctrl : Pointer to the control structure for instance
Return value	0 : Operation success -1 : Operation Failed
Note	-

Figure 9.39 shows a flowchart of the flash_erase_4k() / flash_erase_32k() / flash_erase_64k() implementation in the default IPL.

The processing that changes the implementation when changing the Serial Flash memory is shown below.

- P1 Change parameter of Erase operation table

This is shown as P1 in the flow chart as implementation change points.

The details of the processing are explained after the flow chart.

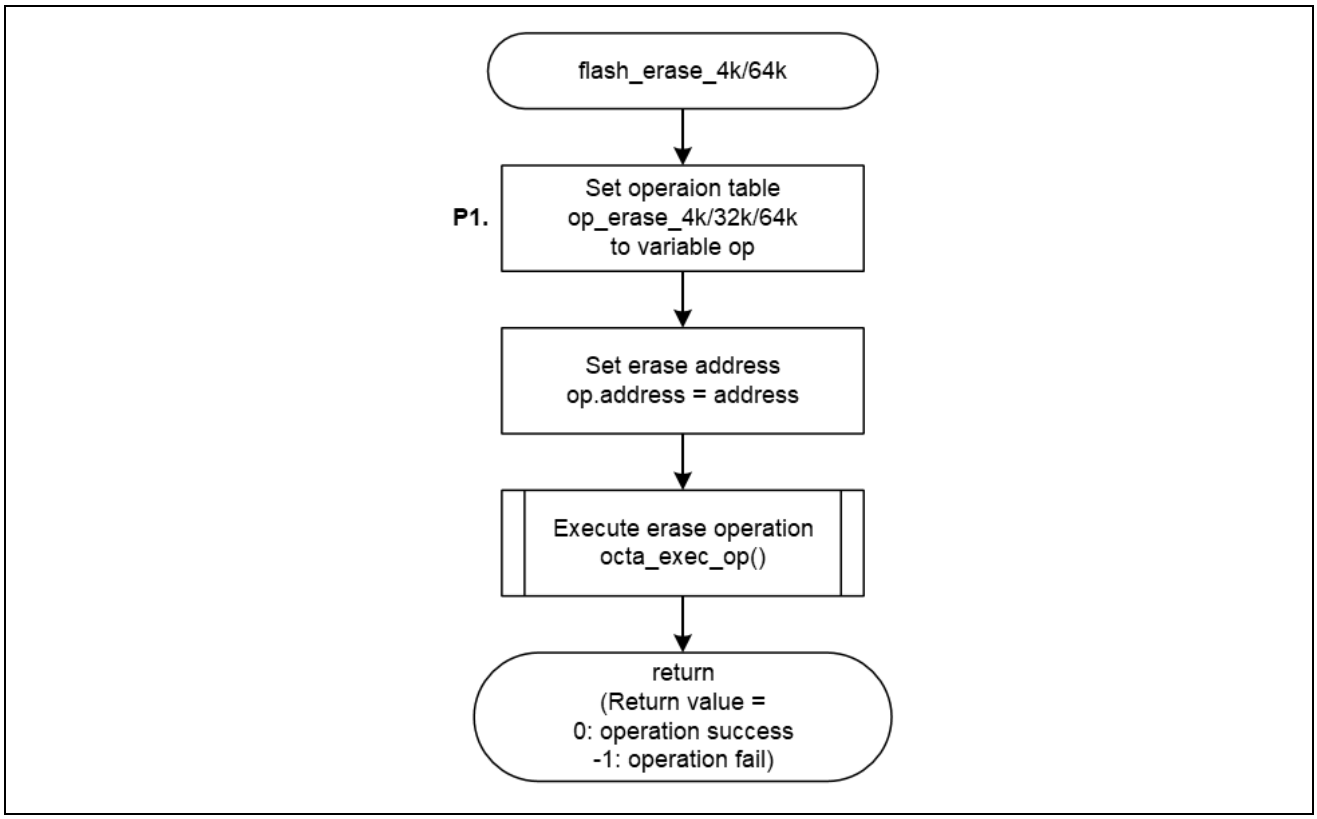


Figure 9.39 Flowchart of flash_erase_4k/32k/64k

P1. Change parameter of Erase operation table

In the erase processing of the Serial Flash memory, data is erased by sending the Erase operation.

The flash_erase_4k() function implemented in the default IPL sets the Block Erase command (4kbytes) (0x20) to the variable op_erase_4k and sends the operation.

Similarly, in the flash_erase_32k() function, set the Block Erase command (32kbytes) (0x52) to the variable op_erase_32k and send the operation.

Similarly, in the flash_erase_64k() function, set the Block Erase command (64kbytes) (0xD8) to the variable op_erase_64k and send the operation.

By doing this, the data is erased by sending the Erase command in each function.

Table 9.12 shows the op_erase_4k settings when using the 4Kbytes Block Erase operation, Table 9.13 shows the op_erase_32k settings when using the 32Kbytes Block Erase operation, and Table 9.14 shows the op_erase_64k settings when using the 64Kbytes Block Erase operation.

When changing the Serial Flash memory, rewrite each variable to the contents corresponding to the Erase operation implemented in that memory.

Table 9.12 op_erase_4k setting contents when using Block Erase (4kbytes) operation (0x20)

Member	Setting value	Description
form	SPI_FORM_1_1_1	Number of I/O line used for command: 1 line Number of I/O line used for address: 1 line Number of I/O line used for data: 1 line
op	0x20	Command code "Block Erase (4kbytes)"
op_size	1	Command size = 1byte
op_is_ddr	false	Command transfer method (SDR)
address	address	Set address of argument
address_is_ddr	false	Address transfer method (SDR)
address_size	3	24bit address
additional_value	0	No option data
additional_size	0	No option data
dummy_cycles	0	Dummy cycles = 0 cycles
transfer_buffer	NULL	No data
transfer_is_ddr	false	Data transfer method (SDR)
transfer_size	0	No data
force_idle_level_mask	0x08	Keep IO3/HOLD pin to High during idle state
force_idle_level_value	0x08	Keep IO3/HOLD pin to High during idle state
slch_value	0	Clock Delay = 1.5cycle
clsh_value	0	SSL Negation Delay = 1cycle
shsl_value	6	Next Access Delay = (7 – 3) cycle

Table 9.13 op_erase_32k setting contents when using Block Erase (32kbytes) operation (0x52)

Member	Setting value	Description
form	SPI_FORM_1_1_1	Number of I/O line used for command: 1 line Number of I/O line used for address: 1 line Number of I/O line used for data: 1 line
op	0x52	Command code "Block Erase (32kbytes)"
op_size	1	Command size = 1byte
op_is_ddr	false	Command transfer method (SDR)
address	address	Set address of argument
address_is_ddr	false	Address transfer method (SDR)
address_size	3	24bit address
additional_value	0	No option data
additional_size	0	No option data
dummy_cycles	0	Dummy cycles = 0 cycles
transfer_buffer	NULL	No data
transfer_is_ddr	false	Data transfer method (SDR)
transfer_size	0	No data
force_idle_level_mask	0x08	Keep IO3/HOLD pin to High during idle state
force_idle_level_value	0x08	Keep IO3/HOLD pin to High during idle state
slch_value	0	Clock Delay = 1.5cycle
clsh_value	0	SSL Negation Delay = 1cycle
shsl_value	6	Next Access Delay = (7 – 3) cycle

Table 9.14 op_erase_64k setting contents when using Block Erase (64kbytes) operation (0xD8)

Member	Setting value	Description
form	SPI_FORM_1_1_1	Number of I/O line used for command: 1 line Number of I/O line used for address: 1 line Number of I/O line used for data: 1 line
op	0xD8	Command code "Block Erase (64kbytes)"
op_size	1	Command size = 1byte
op_is_ddr	false	Command transfer method (SDR)
address	address	Set address of argument
address_is_ddr	false	Address transfer method (SDR)
address_size	3	24bit address
additional_value	0	No option data
additional_size	0	No option data
dummy_cycles	0	Dummy cycles = 0 cycles
transfer_buffer	NULL	No data
transfer_is_ddr	false	Data transfer method (SDR)
transfer_size	0	No data
force_idle_level_mask	0x08	Keep IO3/HOLD pin to High during idle state
force_idle_level_value	0x08	Keep IO3/HOLD pin to High during idle state
slch_value	0	Clock Delay = 1.5cycle
clsh_value	0	SSL Negation Delay = 1cycle
shsl_value	6	Next Access Delay = (7 – 3) cycle

9.3.2 How to add a board setting

1. Open the c:\work\RZA3UL_IPL\plat\renesas\rz\board folder, copy the "a3ul_smarc_qspi" folder and rename it to any name.
   This time, rename the folder name to "a3ul_custom_board_qspi".

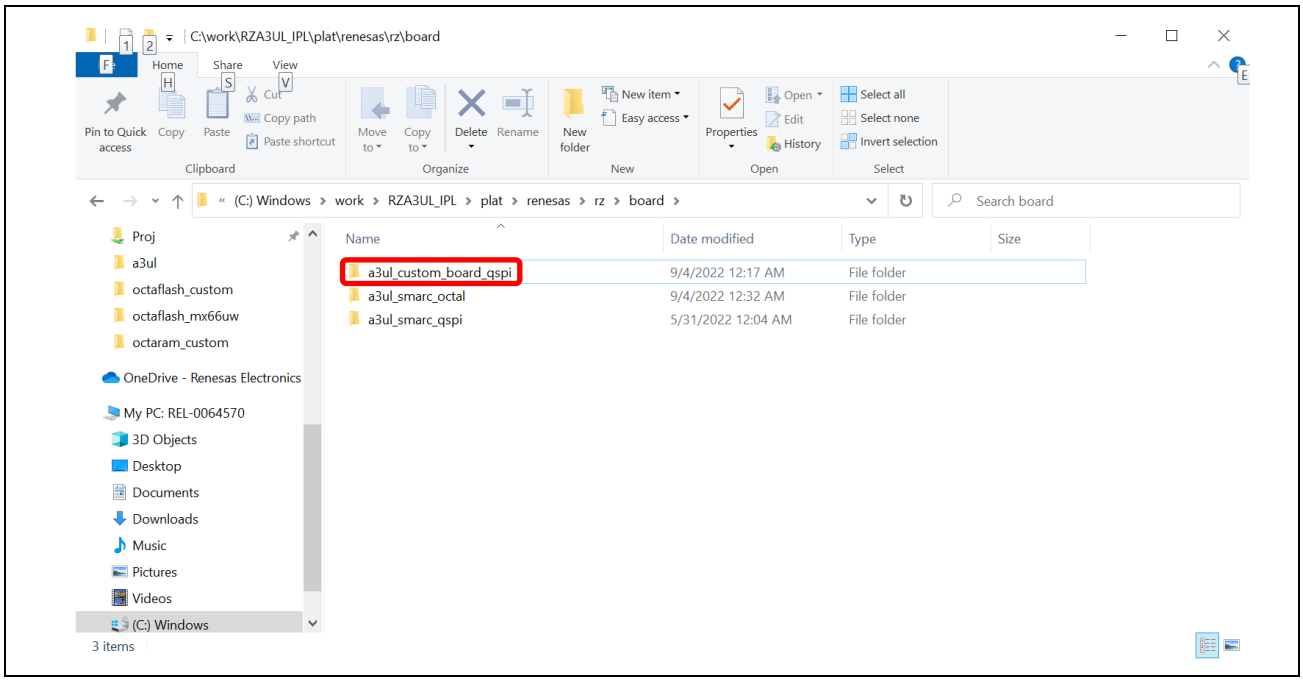


Figure 9.40 Rename board setting folder

2. Open "a3ul_custom_board_qspi" folder and open "rz_board.mk".
   Register the folder name of the Serial Flash memory driver added in Chapter 9.3.1
   This time, rewrite "_XSPI0_DEVICE:=qspiflash_at25" on line 7 to "_XSPI0_DEVICE:=qspiflash_custom".

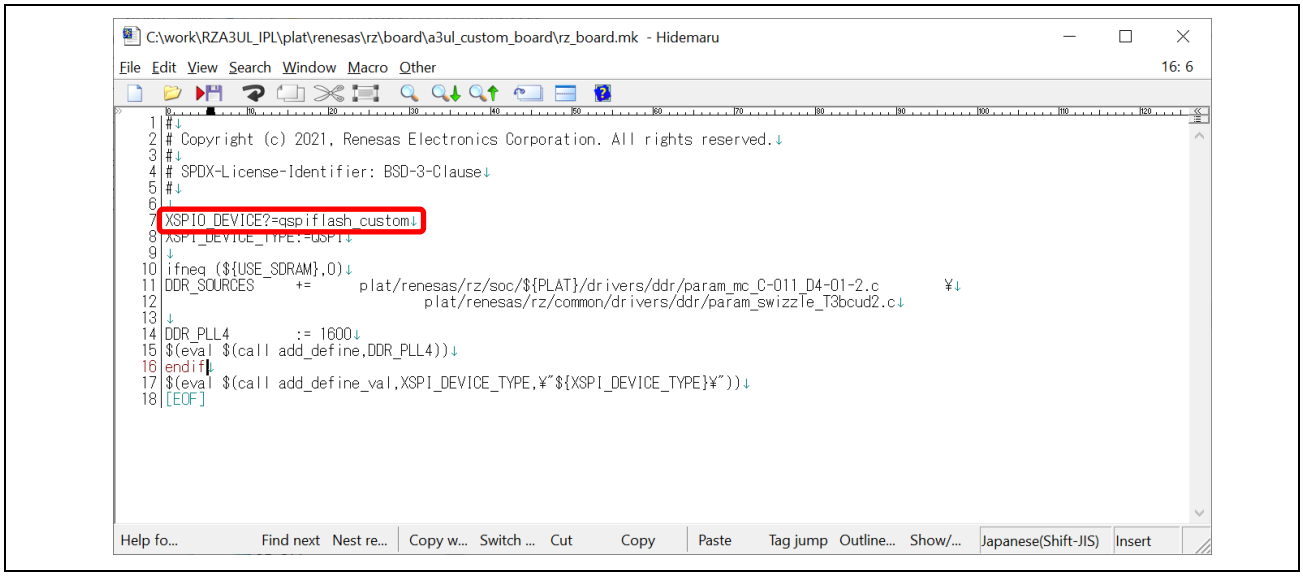


Figure 9.41 Change board setting Makefile

3. Launch e² studio.
   Then refer to step 10 of chapter 7. IPL build environment construction procedure to launch Properties for RZA3UL_IPL and move to the [Behavior] tab.
   Change the BOARD value set in the "Build arguments" field to "a3ul_custom_board_qspi".
   After this, running the build as usual will generate an IPL for your custom board.

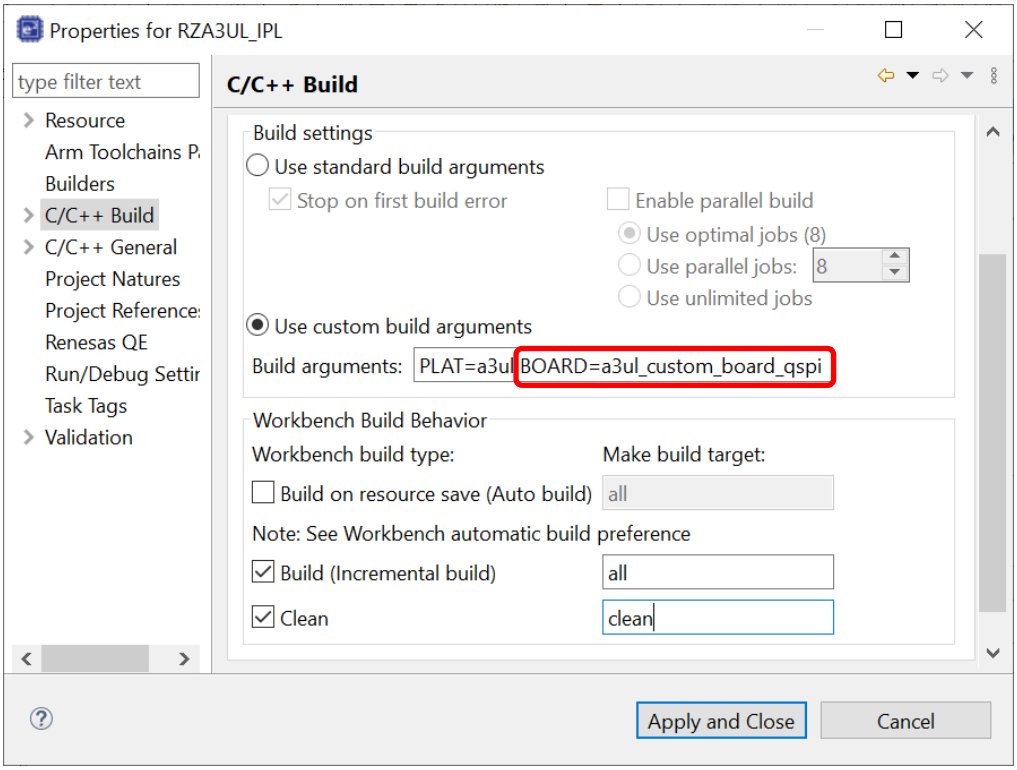
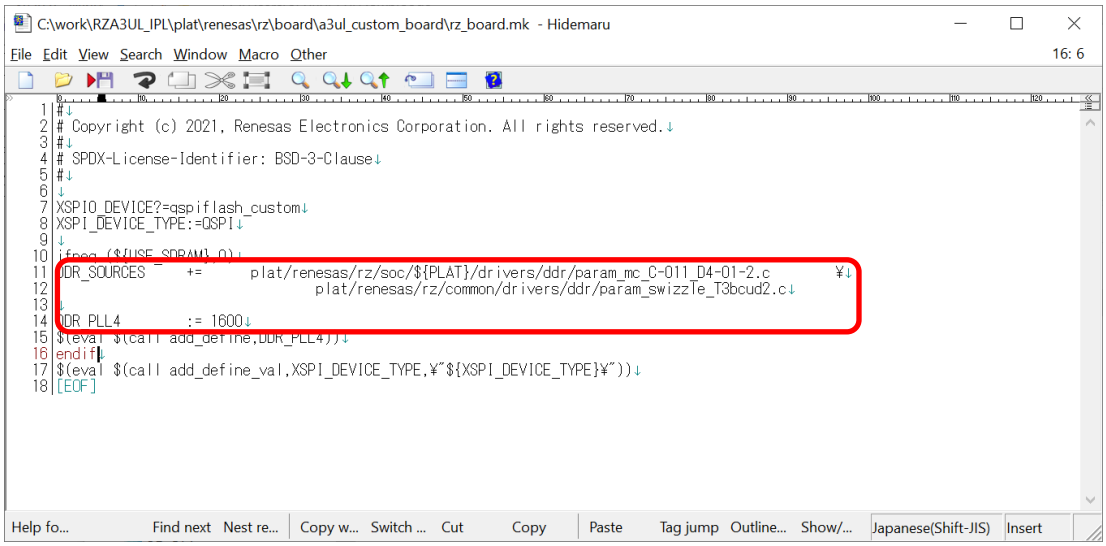


Figure 9.42 Change project setting

Note: When changing DDR SDRAM, set the parameter file corresponding to DDR SDRAM to DDR_SORCEUS in rz_board.mk, and set the operating clock frequency of DDR SDRAM to DDR_PLL4.
Please contact Renesas Electronics for the parameter file corresponding to your DDR SDRAM.



Note: When changing DDR SDRAM, set the parameter file corresponding to DDR SDRAM to DDR_SOURCES in rz_board.mk, and set the operating clock frequency of DDR SDRAM to DDR_PLL4.
Please contact Renesas Electronics for the parameter file corresponding to your DDR SDRAM.

Figure 9.43 Information of DDR SDRAM setting

9.3.3 How to add a Module for Clock Supply

In IPL, clocks are supplied to the modules shown in the CPG column of Table 5.1, resets are released, and the modules are made available.

This chapter describes how to add the settings when adding a module that supplies clocks and resets.

1. Open "c:\work\RZA3UL_IPL\plat\renesas\rz\common\drivers\cpg.c".
2. Add the setting table of the module to be supplied with the clock to "cpg_clk_on_tbl[]".

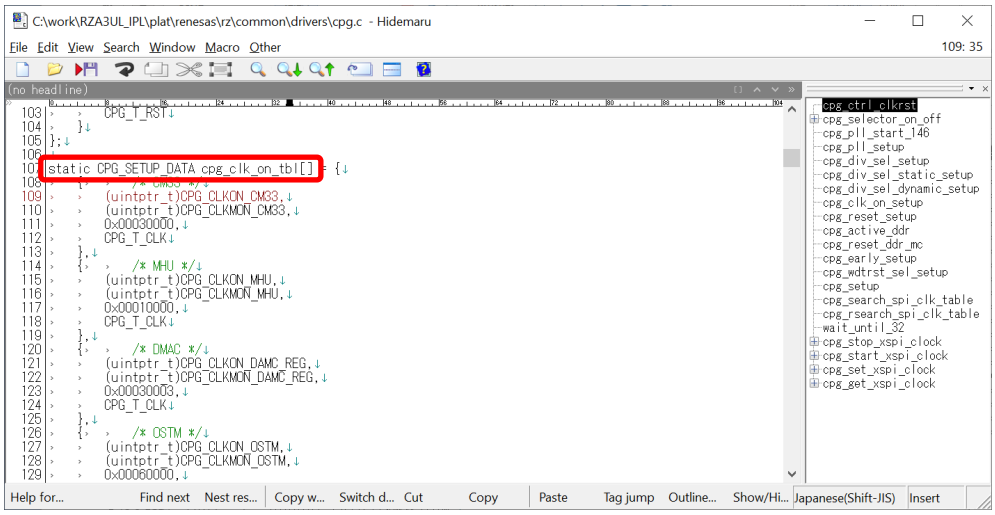


Figure 9.44 Information of cpg_clk_om_tbl[]

3. The setting table has the following format.

```
{
    reg,
    mon,
    val,
    type
}
```

reg: Sets the Clock Control Register address of the module supplying the clock.
mon: Sets the Clock Monitor Register address corresponding to the register set in reg.
val: Sets the value to write to the register set in reg.
type: Set CPG_T_CLK.
For details of Clock Control Register and Clock Monitor Register, refer to RZ/A3UL Group User's Manual: Hardware (R01UH0973EJ).

4. Add the setting table of the module to be reset to "cpg_reset_tbl[]".

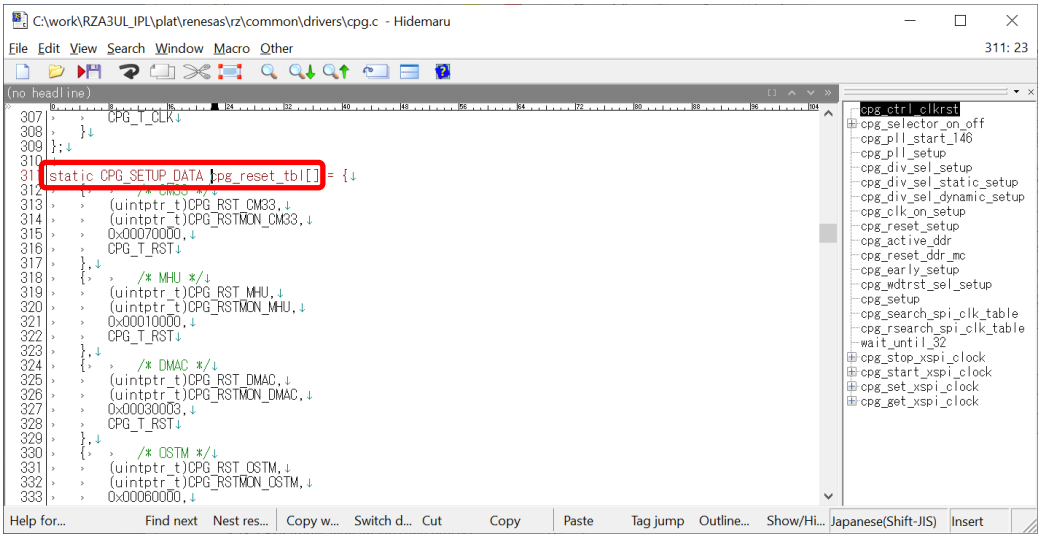


Figure 9.45 Information of cpg_reset_tbl[]

5. The format of the setting table is the same as "cpg_clk_on_tbl[]".
The values to be set are as follows.
reg: Sets the Reset Control Register address of the module to be reset.
mon: Sets the Reset Monitor Register address corresponding to the register set in reg.
val: Sets the value to write to the register set in reg.
type: Set CPG_T_RST.
For details of Reset Control Register and Reset Monitor Register, refer to RZ/A3UL Group User's Manual: Hardware (R01UH0973EJ).

9.3.4 How to add pin setting

In IPL, the pin setting shown in the GPIO column of Table 5.1 is performed.

This chapter shows how to add pin settings.

1. Open "c:\work\RZA3UL_IPL\plat\renesas\rz\common\drivers\pfc.c".
2. Add the pin setting table to "pfc_mux_reg_tbl[]".

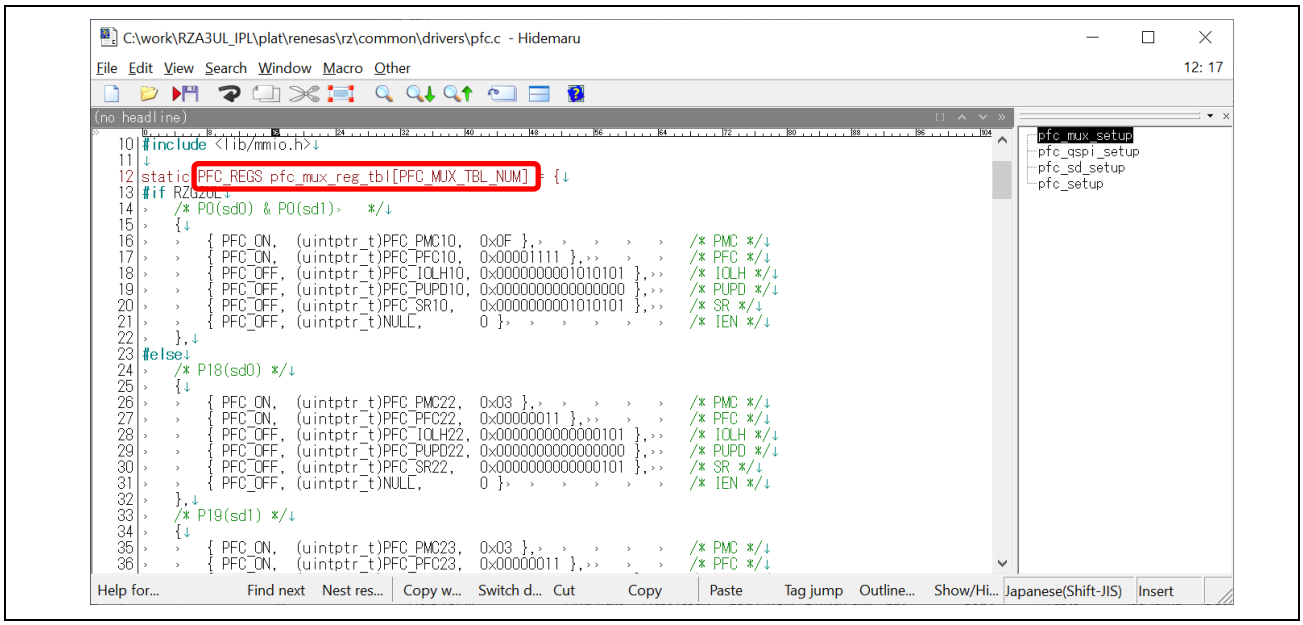


Figure 9.46 Information of pfc_mux_reg_tbl[]

3. The setting table has the following format.

```
{
    {pmc.flag,   pmc.reg,   pmc.val },
    {pfc.flag,   pfc.reg,   pfc.val },
    {iolh.flag,  iolh.reg,  iolh.val },
    {pupd.flag,  pupd.reg,  pupd.val },
    {sr.flag,    sr.reg,    sr.val },
    {ien.flag,   ien.reg,   ien.val }
}
```

   "XXX" below indicates PMCn, PFCn, IOLHn, PUPDn, SRn, IENn registers.
   XXX.flag: Set PFC_ON to change the register value registered in the table. Set PFC_OFF if you do not want to change the register value.
   XXX.reg: Set the address of the register to which the parameter is to be set.
   XXX.val: Sets the value to write to the register set in reg.
   For details of each register, refer to RZ/A3UL Group User's Manual: Hardware (R01UH0973EJ).
4. Open pfc_regs.h and increase the value of PFC_MUX_TBL_NUM by the number of added tables.

9.3.5 How to change MMU setting

This chapter shows how to change MMU settings.

1. Open "c:\work\RZA3UL_IPL\plat\renesas\rz\common\bl2_plat_setup.c".
2. Rewrite the MMU setting table of "g_mmu_pagetable_array[]".

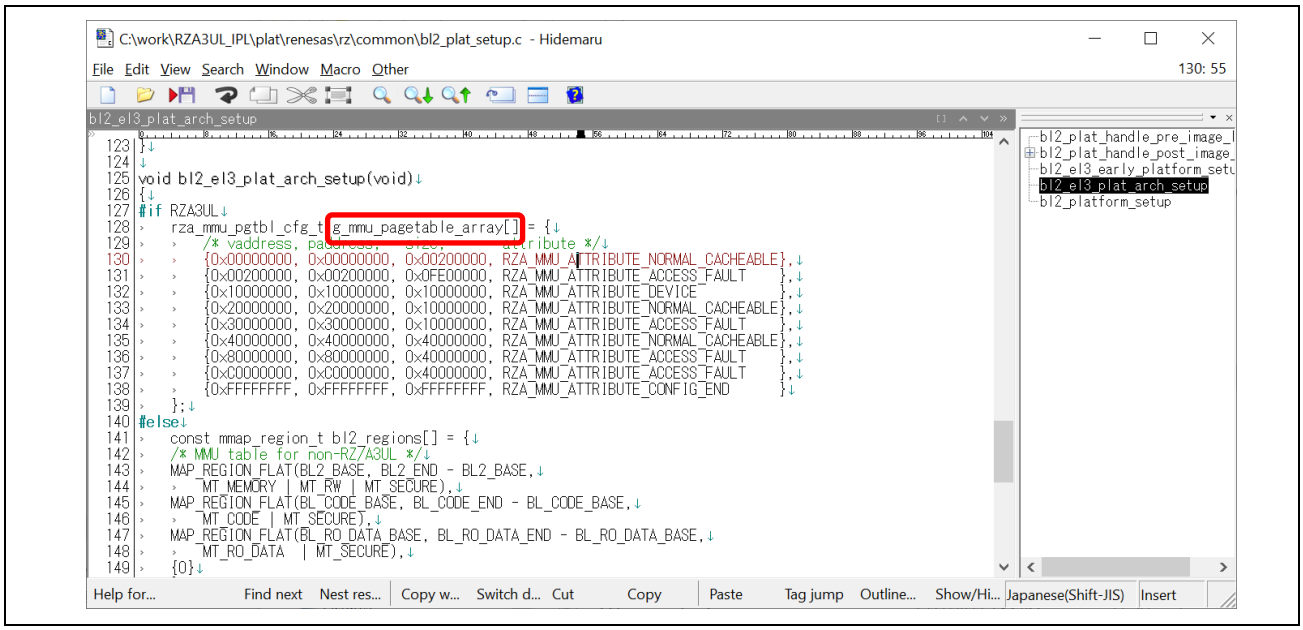


Figure 9.47 Information of g_mmu_pagetable_array[]

3. Each line in "g_mmu_pagetable_array[]" is the setting for each block in the virtual address space, and consists of the following format.

```
{
    {vaddress,  paddress,  size, attribute },
    ...
    {0xFFFFFFFF, 0xFFFFFFFF, 0xFFFFFFFF, RZA_MMU_ATTRIBUTE_CONFIG_END }
}
```

vaddress: Sets the starting address of the virtual address space. Sets a 2Mbyte aligned address.
paddress: Sets the starting address of the physical address space. Sets a 2Mbyte aligned address.
size: Sets the size of block. Sets a 2Mbyte aligned size.
Attribute: Memory attribute. The following parameters can be specified.

RZA_MMU_ATTRIBUTE_NORMAL_CACHEABLE: Normal Memory, Cache enable (Write-back)
RZA_MMU_ATTRIBUTE_NORMAL_UNCACHE: Normal Memory, Cache disable
RZA_MMU_ATTRIBUTE_DEVICE: Device Memory
RZA_MMU_ATTRIBUTE_ACCESS_FAULT: Areas where access is prohibited
This attribute is set for areas that are not set in the MMU setting table.
RZA_MMU_ATTRIBUTE_CONFIG_END: Indicates the end of MMU configuration
This attribute is set to the last element of the MMU setting table.

10. Precautions

10.1 About DDR SDRAM access prohibited area

Test data for DDR SDRAM initialization is stored in the DDR SDRAM area shown below.

If you overwrite the test data, you may not be able to access DDR SDRAM correctly.

Therefore, access to this area is prohibited.

- Access prohibited address:
- 0x40000000 - 0x4000003F

11. Reference Documents

User's Manual: Hardware

RZ/A3UL Group User's Manual: Hardware (R01UH0973EJ)
(Please get the latest version from the Renesas Electronics website)

RZ/G2UL, RZ/A3UL, RZ/FIVE SMARC Module Board User's Manual: Hardware (R01UH0990EJ)
(Please get the latest version from the Renesas Electronics website)

RZ SMARC Series Carrier Board User's Manual: Hardware (R01UH0990EJ)
(Please get the latest version from the Renesas Electronics website)

Getting Started with RZ/A Flexible Software Package (R01AN6499EJ)
(Please get the latest version from the Renesas Electronics website)

Arm® Architecture Reference Manual for A-profile architecture
(Please get the latest version from the Arm website)

Arm® Cortex®-A Series Programmer's Guide for ARMv8-A Version:1.0
(Please get the latest version from the Arm website)

Arm® Cortex®-A55 Core Technical Reference Manual Revision; r2p0
(Please get the latest version from the Arm website)

Technical Update/Technical News
(Please get the latest information from the Renesas Electronics website)

User's Manual: Integrated Development Environment
(Please get the latest version from the Renesas Electronics website)

12. Trademarks

The company names and product names in this document are trade names, trademarks or registered trademarks of their respective companies.

- Arm, Cortex and CoreSight are registered trademarks or trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

Revision History

Rev.	Date	Description	
		Page	Summary
1.0.0	Jul. 28. 22	-	First edition issued.
1.1.0	Sep.30.22	6	Table 2.1 Updated Debugger information.
		7	Chapter 3. Add information of RZ/A3UL Initial Program Loader Application Note (Octa Flash Boot Edition).
		8	Table 4.2 Modify information of pin.
		11	Chapter 5.1.2 Added a new chapter.
		20	Figure 5.5 Modify figure.
		22	Chapter 5.8 Added a new chapter.
		23	Chapter 5.9 Added a new chapter.
		26	Chapter 5.10 Added a new chapter.
		34	Chapter 5.11 Added a new chapter.
		58	Chapter 5.12 Added a new chapter.
		90	Chapter 6.1.1.2 Delete chapter.
		90	Chapter 6.1.1.3 Delete chapter.
		103	Chapter 6.1.2.2 Delete chapter.
		103	Chapter 6.1.2.3 Delete chapter.
		104	Chapter 6.2.2 Updated driver information of J-link.
		124	Figure 8.13 Added SW1 setting when J-Link is not connected.
		144	Chapter 9.3 Added a new chapter.
		163	Chapter 12 Added a new chapter.
1.2.0	Dec.26.22	-	Changed from the document for RZ/A3UL IPL to the document for RZ/A3 IPL.
		1	Introduction Added document summary list.
		5	Table 1.1 Added description of Serial Flash Memory Driver.
		6	Table 1.2 Added description of Manual Mode.

Rev.	Date	Description	
		Page	Summary
1.2.0	Dec.26.22	7	Table 2.1 Added QSPI0_SOCLK information. Updated information for IPL v1.2.0.
		20	Figure 5.4 Modified Serial Flash memory area address.
		32	Table 5.23 Added information that the Serial Flash driver does not support the format.
		81	Figure5.6 Modified the chapter numbers of the functions described in each flow chart.
		86	6.1.1.1 Update installation procedure of e² studio 2022-10.
		98	6.2.1.1 Update installation procedure of e² studio 2022-10.
		123	Figure 8.5 Added setting of "Reset Before Run". Added information about J-Link interface type.
		124	Figure 8.6 Added informatin about Flash memory. Change Reset setting after reloading to No.
		140	Figure 9.2 Added setting of "Reset Before Run".
		150	9.3 Added the outline of the contents explained in Chapter 9.3.
		150	9.3.1 Added a description of the serial transfer method and transfer format to the Serial Flash memory.
		159	9.3.1.1 to 9.3.1.14 Added the new chapters describing the Serial Flash memory driver functions.
		201	10.1 Removed chapter 10.1 from the previous version.
2.0.0	Feb.28.25	9	Table 2.1 Update information of Operation Confirmation Conditions.
		87	6.1.1.1 Update installation procedure of e² studio for Windows.
		99	6.2.1.1 Update installation procedure of e² studio for Linux.
		121	8.1 Updated the procedure for creating Debug Configuration using new e² studio GUI.
		132	8.3 Updated setup procedure to use the new e² studio GUI.
		136	8.4 Updated execution procedure to use the new e² studio GUI.
		140	9.1 Updated execution procedure to use the new e² studio GUI.
		144	9.2 Updated writing procedure to use the new e² studio GUI.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION ("Vulnerability Issues"). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit: www.renesas.com/contact/.

© 2025 Renesas Electronics Corporation. All rights reserved.