Application Report

Layer Design for Reducing Radiated EMI of DC to DC Buck-Boost Converters

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ABSTRACT

The following application note gives guidelines for improving EMI performance for PCB design of TPS63xxx. The main radiation sources for non-inverting buck-boost converters are briefly explained. The arguments for three different solutions are put forward. The effectiveness of these solutions is validated by anechoic chamber measurements.

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1 Introduction

Meeting clearly defined emission standards is a critical requirement for releasing new products to the market. Today however, almost half of these products end up failing the emission standards. These failures translate to significant delay and can quickly increase the final cost of the product. This report illustrates rule-of-thumb solutions for PCB integration of TPS63xxx that can be implemented to improve EMI performance.

2 EMI Sources

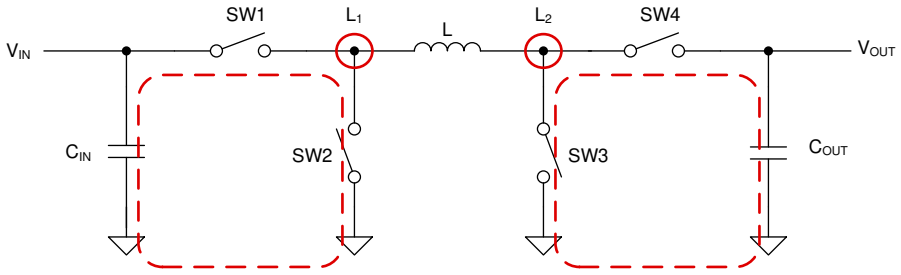

Figure 2-1. EMI Sources in Non-inverting Buck-boost Converter

Figure 2-1 highlights the main sources of EMI in a non-inverting buck-boost converter.

The first EMI source is the hot loop located between input capacitor (C_{IN}) and SW2. The second loop responsible for EMI is the loop located between output capacitor (C_{OUT}) and SW3. The loops occurrence differs dependent on the converter operating mode. In Figure 2-1, the left loop exists during buck mode operation while the right most loop, during boost mode operation. Due to the switching logic, these loops will have high rates of change in current over time (di/dt). Taking into account the equivalent series inductance (ESL) of a capacitor and the equation of voltage over inductor Equation 1, it can be seen that these hot loops can give rise to unwanted voltages (v_L).

$$v_L = L \times \frac{di}{dt} \tag{1}$$

The switching nodes L_1 and L_2 are another EMI source. Depending on the operation mode, L_1 for buck and L_2 for boost, these nodes experience high changes in voltage over time (dv/dt). A change in voltage can give rise to undesired currents in a capacitor as shown by Equation 2. Keeping in mind that capacitances can develop between inductor windings, the occurrence of parasitic currents (i^2C) is possible.

$$i_C = C \times \frac{dv}{dt} \tag{2}$$

Besides the parasitic capacitance of the inductor, another capacitance also exists between the node and the ground layer. This capacitance is described by Equation 3 and it is strongly influenced by the distance (d) between the layer on which the node is located and the closest ground layer as well as by the area of the parallel plates (A). ε_0 and ε_r are the permittivity of free space (ε_0=8.85 pF/m) and the relative permittivity of the medium between the two plates.

$$C = \frac{\varepsilon_0 \times \varepsilon_r \times A}{d} \tag{3}$$

The following sections will introduce tested solutions that reduce radiations. The proposed solutions are accompanied by measurements that prove their effectiveness. The measurements were conducted in accordance to the CISPR 16-2-3 standards and regulations referenced in Section 7.

3 Device Optimization

Figure 3-1 shows the circuit of a typical application of TPS63070. This circuit is used in this application note. The starting PCB layout concept is the recommended Webench layout for PCB built provided by Texas Instruments.

Please note that the Webench layout is not optimized for best EMI performance, but for the ability to place different size components.

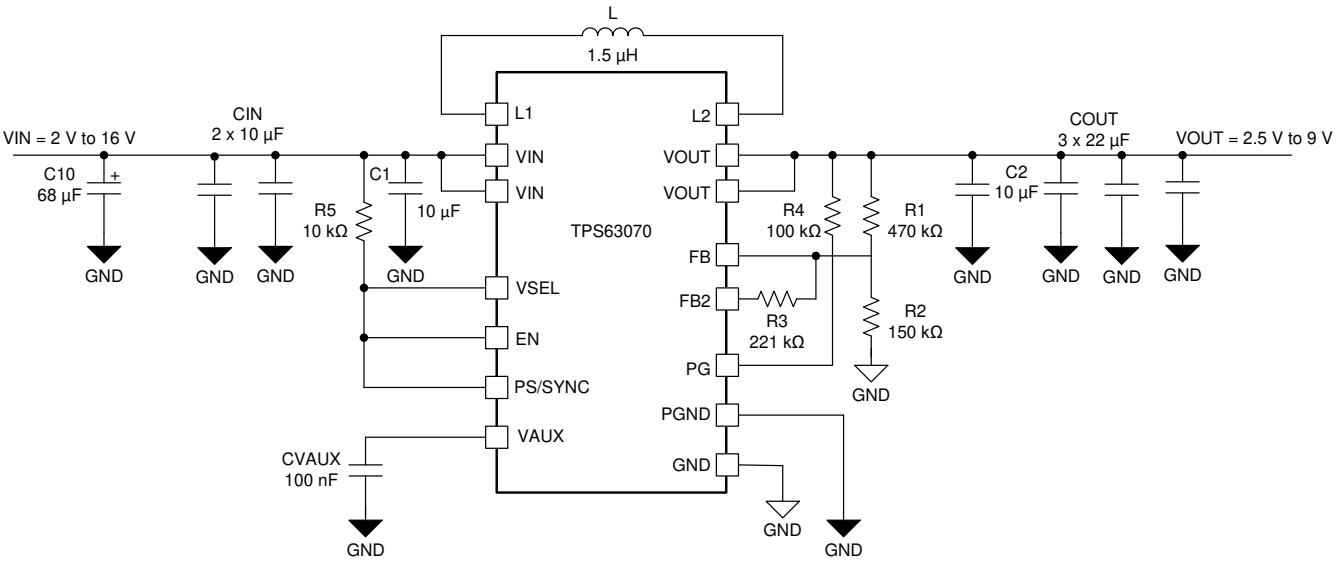

Figure 3-1. Typical Application of TPS63070

The Webench PCB layout is a two layer approach. All the planes, except the inductor ports, are kept on the top layer. The bottom layer consists of the inductor terminals and input and output planes. Optimizations can be done to the Webench layout in order to improve the radiated performance as follows:

- **Minimizing hot planes:** The area size of the nets corresponding to the input, output, inductor and other components connections should be kept as small as the design permits. Maximum area size should be assigned to the ground planes.
- **Keeping traces entirely on one layer:** Avoid as much as possible crossing between layers in the middle of a trace. This procedure reduces the number of vias and lowers the overall plane inductance.

Figure 3-2 shows the top layers of the Webench layout (left) and the optimized layout (right). It highlights the minimized planes and the lack of cross layer talk.

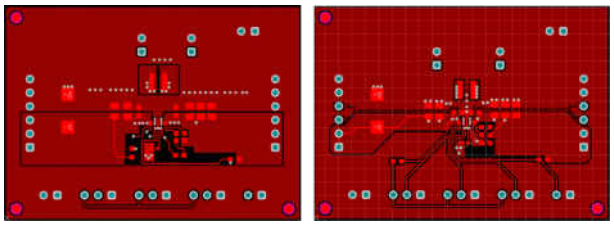

Figure 3-2. Top Layers of Webench Layout (left) Optimized Layout (right)

Figure 3-3 shows the benefits of the above mentioned improvements. The difference between the two measurements is significant and easily observable. Numerically, this difference can be as high as 10 dB at the most affected frequencies.

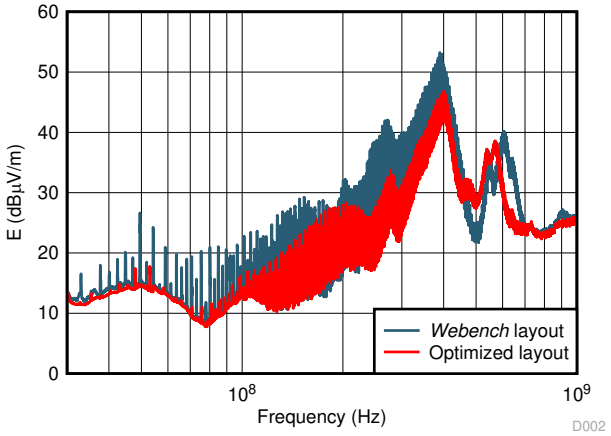

Figure 3-3. Radiated EMI Response of the Webench Layout and the Optimized Layout

4 Migration from two-layer to four-layer board

An often used design solution for minimizing radiation is the four-layer board. Adding two ground planes adjacent to the existing top and bottom layers can significantly improve the EMI performance. The new ground planes are separated by a filler material and they are kept as close as possible to the top and bottom layers. By adding the ground planes, the loop area formed by the return current is significantly reduced. As a result, the reduced loop area allows for better flux cancellation than the two-layered solution.

Figure 4-1 shows the layer stack-up of the two-layer board (left) and the four-layer one (right). The two additional ground layers significantly reduce the parasitic capacitance developed between the plates. This capacitance reduction is possible because the distance between the Signal and the GND layers is minimized. As previously mentioned and shown in Equation 3, the distance between layers is inversely proportional with the capacitance that appears between two plates.

Please note that the distance between the two signal layers remains constant in both cases.

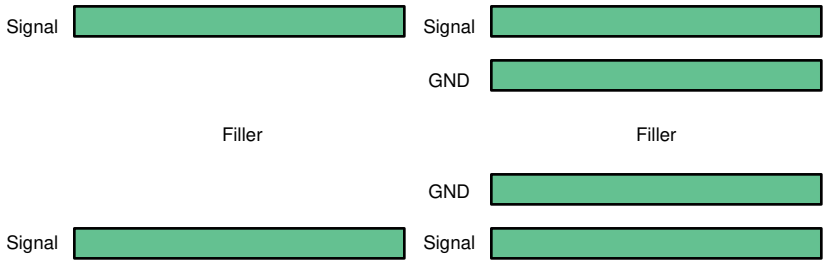

Figure 4-1. Layer Stack-up of Two Layer Board (left) and Four Layer Board (right)

The effects of the four-layer board are highlighted in Figure 4-2. Overall, the transition to a four layer PCB improves the emission performance. The reduction in radiated field varies between 4 dB up to 10 dB for the most extreme cases.

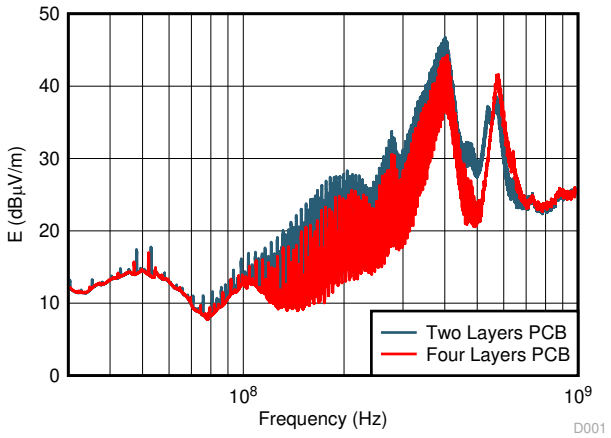

Figure 4-2. Radiated EMI Response of Two-layer and Four-layer PCB

5 Additional Capacitors to a Chassis Ground

From an antenna theory point of view, a cable is nothing more than a radiator. The chassis or the enclosure where the converter is located can serve as the reference plane for this radiator. The potential difference between the cable and the chassis is the voltage driving this antenna. Due to this phenomenon, external cables, like those used to connect to a power supply, can be a major source of radiation. To minimize these radiations, it is important to control and reduce the previously mentioned potential difference. A good way to do this is to provide a high frequency, low-impedance connection between the chassis and the PCB pins that are connected to potential radiators.

To adapt this principle to TPS63070 converter PCB, the bottom plane has been replaced by a neutral chassis ground. High-frequency capacitors have been used to connect this new ground layer to the input, output, and ground planes. This way, a low impedance path is provided for high-frequency signals.

Please be aware that these capacitors should be placed as close as possible to the cable terminations on the PCB. By doing this, we can ensure a minimal voltage difference between chassis ground and the connected plane.

Figure 5-1 shows the benefits of this solution to the overall design. The radiated field is reduced at all frequencies with no significant trade-offs. By implementing this solution, an additional 5 dB decrease in radiated emissions can be achieved.

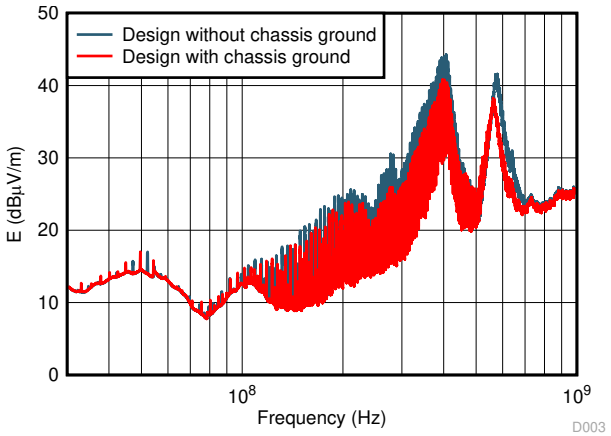

Figure 5-1. Changes in Radiated Emissions when Connecting the Chassis Ground

6 Summary

This application note focuses on showcasing three solutions that can reduce radiated electromagnetic interferences. The proposed solutions are backed up by measured data obtained in anechoic chambers, under similar measurement conditions as recommended by the CISPR standards. While the solutions described in the report show to improve EMI performance, it is worth keeping in mind that they alone cannot be a guarantee for meeting the required standards. When dealing with EMI, the auxiliaries, the power supply, the load will also have an effect over the final result and their impact needs to be taken into account.

7 References

- Texas Instruments, *TPS63070 2-V to 16-V Buck-Boost Converter with 3.6-A Switch Current Data Sheet*
- Henry W. Ott, Electromagnetic Compatibility Engineering, copyright 2009, John Wiley & Sons Inc., ISBN-13: 978-0470189306
- Mark I. Montrose, Printed Circuit Board Design Techniques for EMC Compliance, Second Edition, Copyright 2000, Institute of Electrical and Electronics Engineers Inc., ISBN: 978-0-780-35376-3
- CISPR 16-2-3:2016 Specification for radio disturbance and immunity measuring apparatus and methods - Part 2-3: Methods of measurement of disturbances and immunity - Radiated disturbance measurements

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2020) to Revision A (June 2021)	Page
• Updated the numbering format of tables, figures and cross-references throughout the document	2

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