Under the hood of a non-inverting buck-boost DC/DC converter

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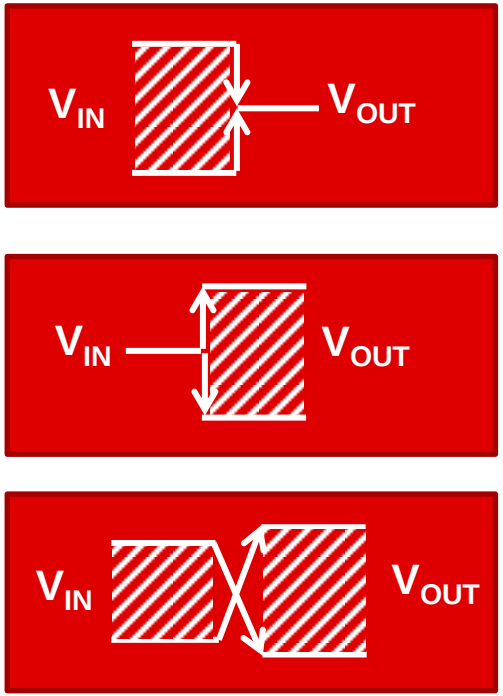
Agenda

- Buck-boost conversion
  - Buck-boost applications and approaches
  - Topology advantages and disadvantages
- 4-switch buck-boost converter
  - Basic converter operation
  - Converter design example
  - PCB layout case study

Who needs a buck-boost converter?



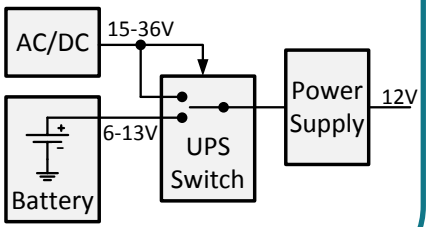
- **Fixed output / variable input:**
  - Battery input from full to minimum charge
  - Automotive cold-crank
  - AC-powered with battery back-up
- **Variable output / fixed input:**
  - GaN or Silicon power amplifier (PA)
  - Constant current LED drive
  - USB Type-C power delivery (PD)
- **Programmable output / variable input**
  - Automotive USB Type-C PD
  - Adaptive PA powered from a battery

Buck-boost applications

Industrial PCs

Application needs

- 6 V-36 V_{IN} from AC-powered supply or battery
- 12 V output, 60 W-200 W



Automotive start/stop & DVRs

Application needs

- 9 V-16 V_{IN}, 3.5 V during start
- ~12 V output, 60 W-120 W

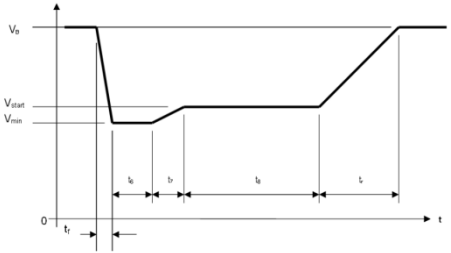


FIGURE 1: ENGINE CRANKING TEST PULSE

USB power delivery

Application needs

- 12 V bus or battery, 9V–16 V_{IN}
- 5/12/20 V_{OUT}, 10 W–100 W

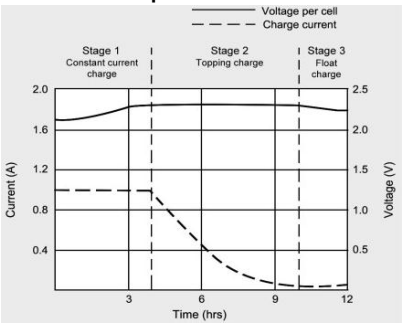
USB Power Delivery profiles

Profile	+5 V	+12 V	+20 V
1	2.0 A, 10 W	N/A	N/A
2		1.5 A, 18 W	N/A
3		3.0 A, 36 W	N/A
4			3.0 A, 60 W
5		5.0 A, 60 W	5.0 A, 100 W

Industrial & battery chargers

Application needs

- 12 V or 24 V_{IN} or DC adapter
- CC/CV up to 200 W+



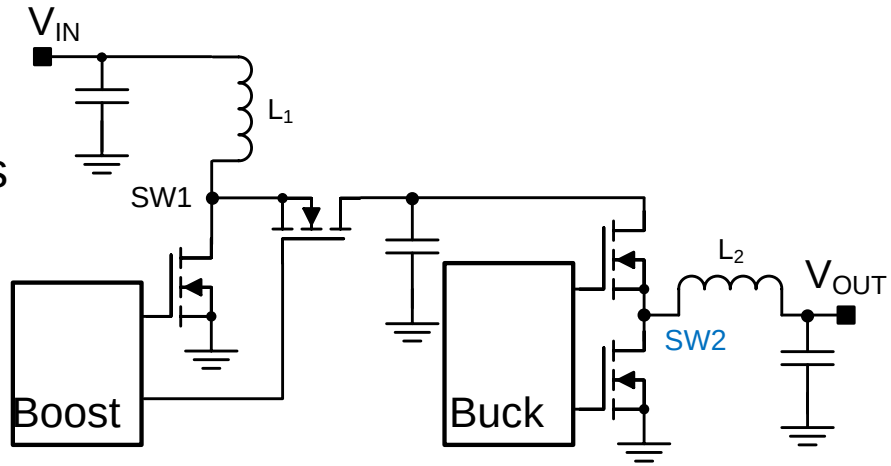
Cascaded boost + buck

Advantages

- Wide choice of buck and boost controllers
- Two simple topologies
- Low noise at both input and output
- Parallel buck stages for multiple V_{OUT} rails

Disadvantages

- Two inductors
- Two controllers
- Higher cost
- Larger solution size
- Higher losses, lower efficiency



SEPIC converter

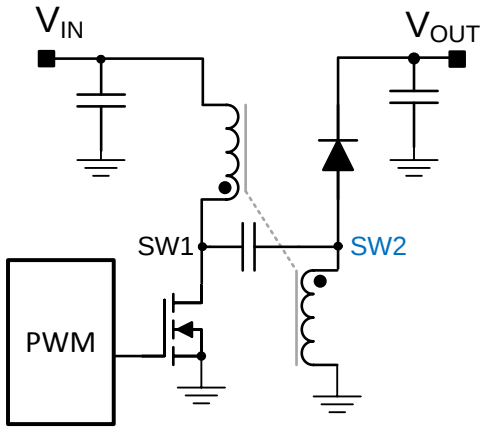
Single-ended primary inductance converter

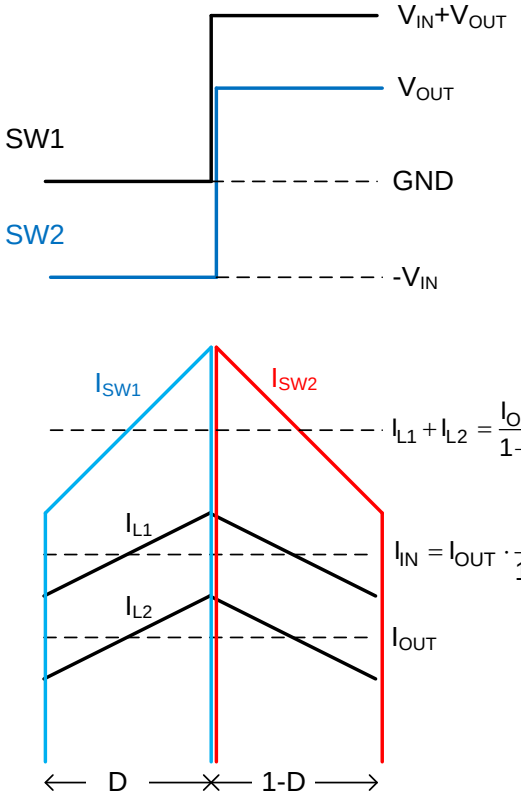
Advantages

- Only one switch plus diode
- Wide choice of controllers for a low-side control switch
- Low input noise

Disadvantages

- DC-blocking capacitor required
- Two inductors or coupled inductor
- Efficiency degrades at higher power
- High switch voltage, $V_{IN} + V_{OUT}$
- High switch current, $I_{IN} + I_{OUT}$
- Right half-plane zero





Zeta converter

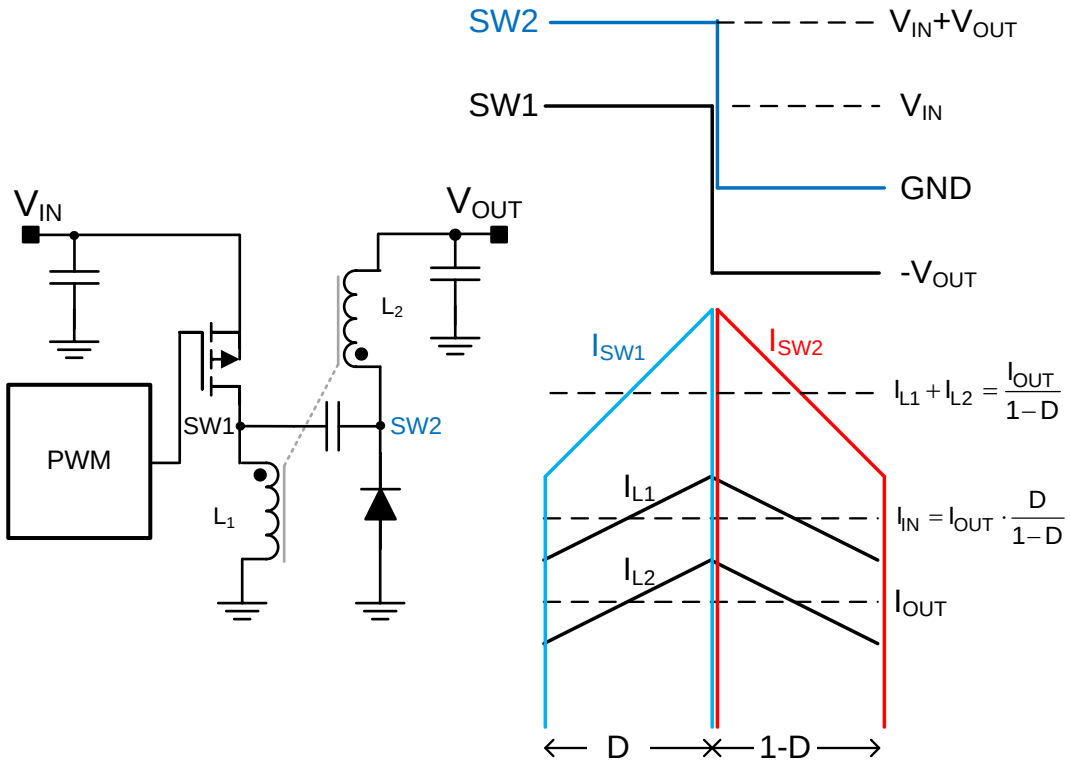
Inverted SEPIC

Advantages

- Only one switch plus diode
- Can use low-cost PFET controller
- Low output noise

Disadvantages

- DC-blocking capacitor required
- Two inductors or coupled inductor
- Efficiency degrades at higher power
- High switch voltage, $V_{IN} + V_{OUT}$
- High switch current, $I_{IN} + I_{OUT}$
- Right half-plane zero



Flyback converter

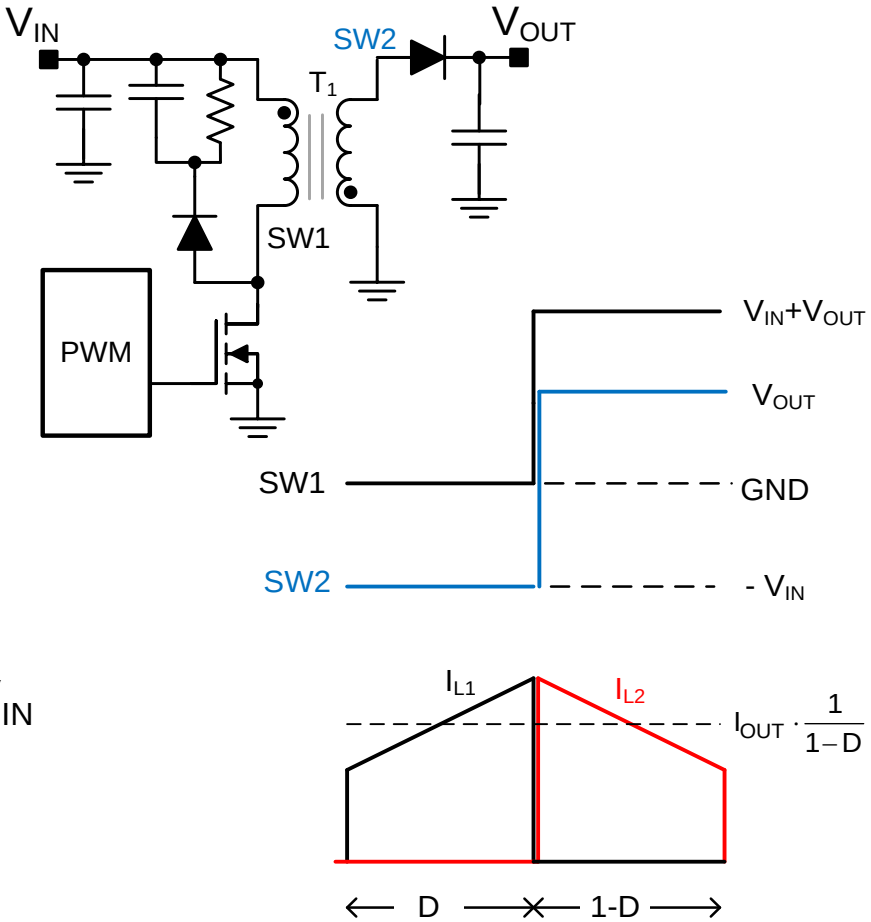
Advantages

- One switch plus diode
- Wide choice of controllers
- Higher power with larger transformer

Disadvantages

- Requires tightly-coupled transformer
- High switch voltages (V_{IN} + N_T*V_{OUT})
- Efficiency degrades at high power / low V_{IN}
- High input and output noise / ripple
- High frequency ringing on SW1

Note: N_T = Transformer Turns Ratio = N_P / N_S



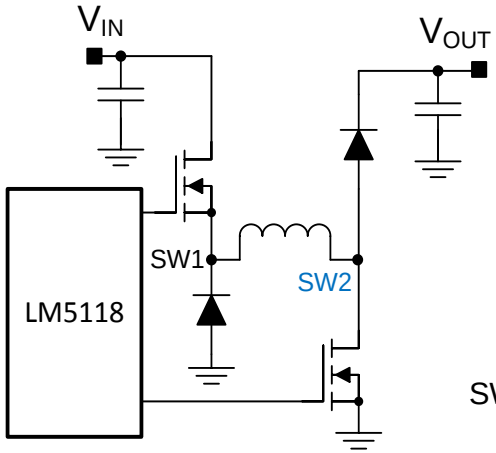
2-switch single inductor buck-boost converter

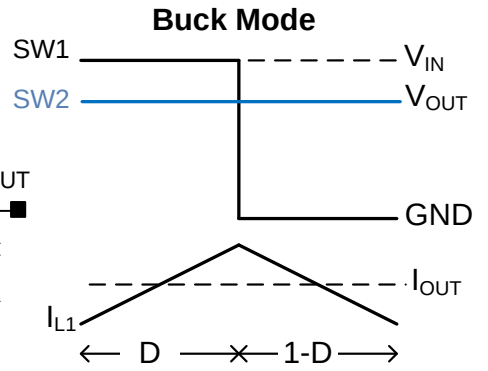
Advantages

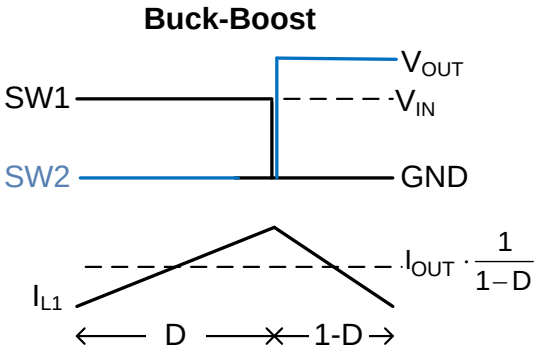
- Simple design
- Single inductor
- Only buck side operates at high V_{IN}
- Lower voltage SW2 FET

Disadvantages

- Non-synchronous design limits power
- High switch current for $V_{IN} < V_{OUT}$
- Output diode power losses
- Single control loop for buck and buck-boost







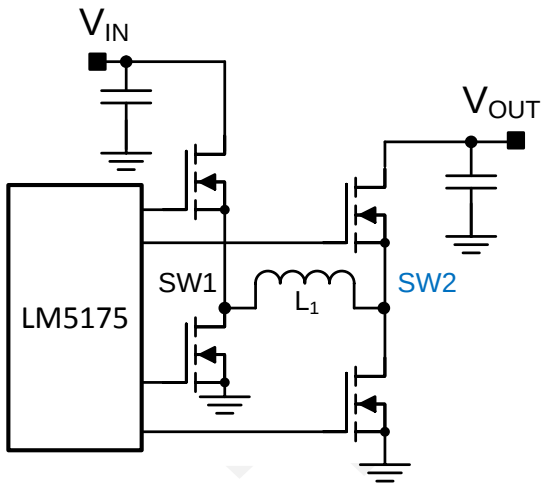
4-switch single inductor buck-boost

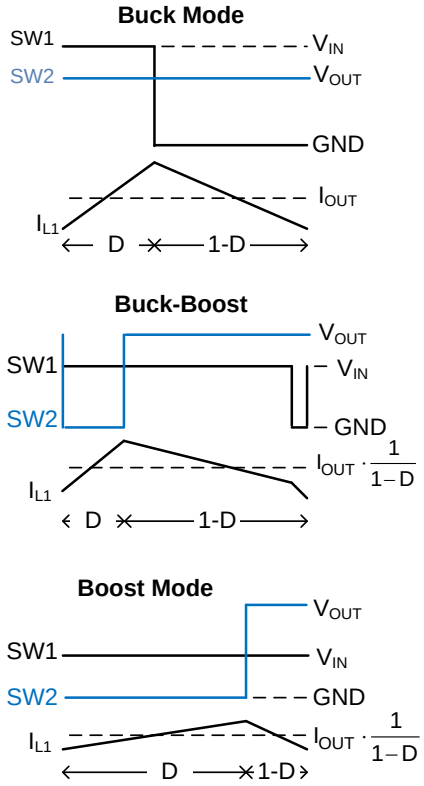
Advantages

- Single inductor / high power density
- Operates in buck mode at high V_{IN}
- Sync rectification – no diode drops
- Lower voltage SW2 FETs (V_{OUT})

Disadvantages

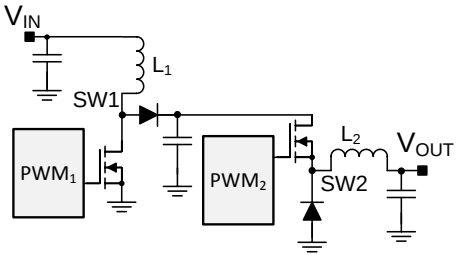
- Limited choice of controllers
- Challenging PCB layout
- Single control loop for buck and boost

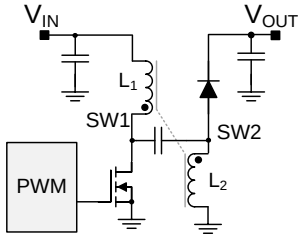


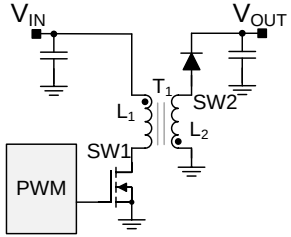


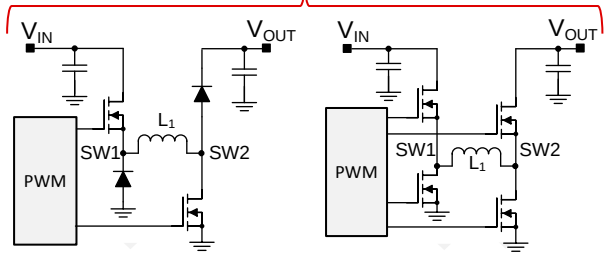
Buck-boost solutions

Single Inductor



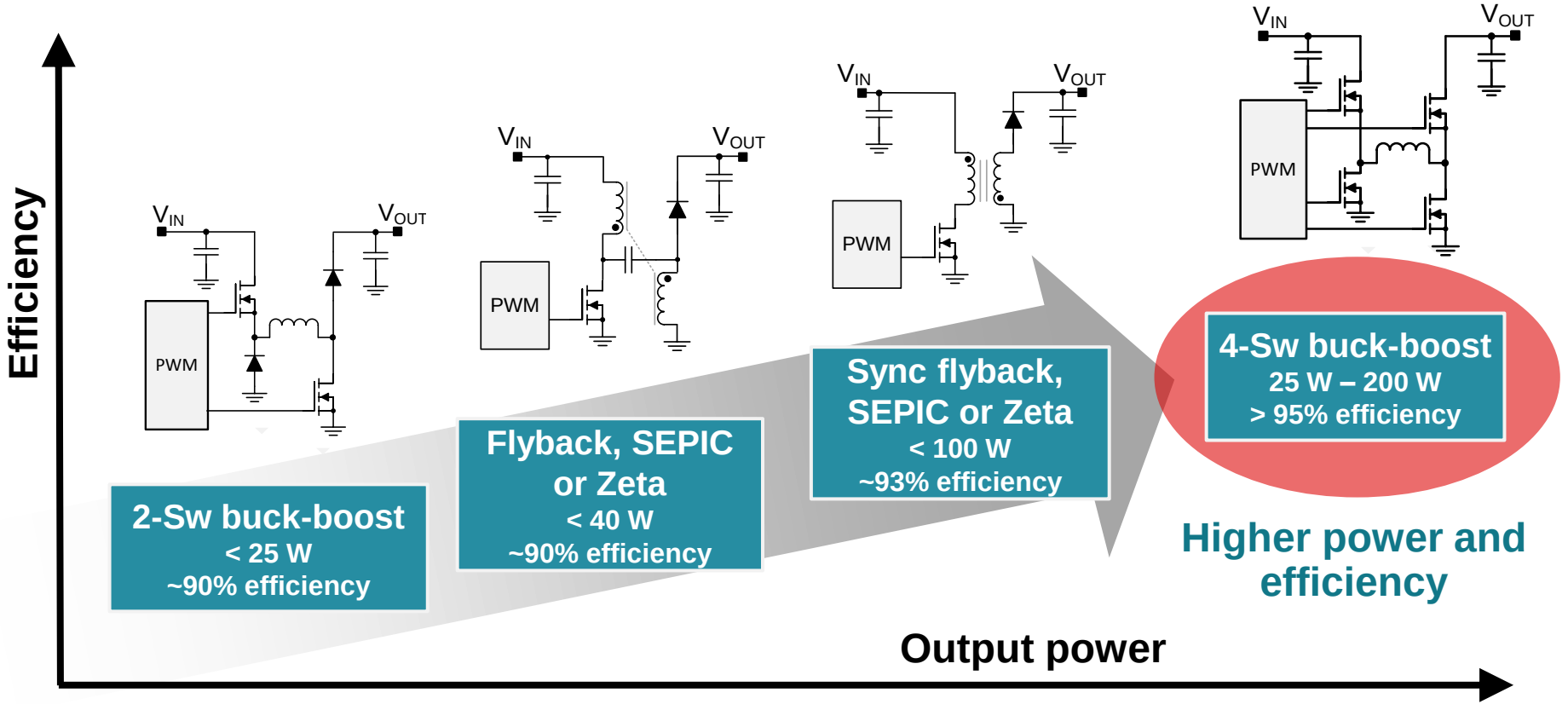




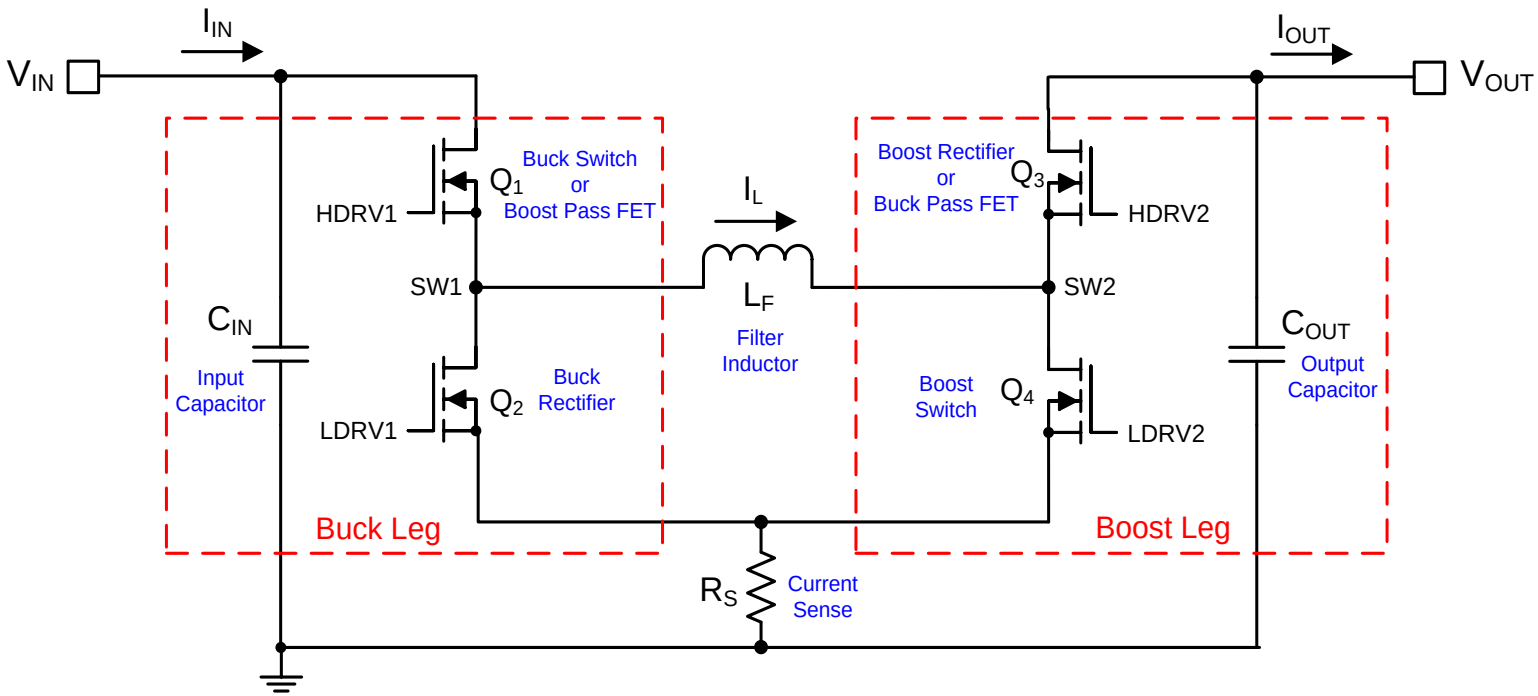


	Boost + buck	SEPIC & Zeta	Flyback ($N_T = N_P/N_S$)	2-Sw buck-boost	4-Sw buck-boost
Max V_{SW}	$SW1, SW2: \ V_{IN}$	$V_{IN} + V_{OUT}$	$V_{IN} + \frac{N_P}{N_S} V_{OUT}$	$SW1: \ V_{IN}$ $SW2: \ V_{OUT}$	$SW1: \ V_{IN}$ $SW2: \ V_{OUT}$
Max I_{SW}	$I_{OUT}\left(\frac{V_{OUT}}{V_{IN}}\right)$	$I_{IN} + I_{OUT}$	$I_{IN}\left(1 + \frac{N_S}{N_P}\frac{V_{IN}}{V_{OUT}}\right)$	$I_{IN} + I_{OUT}$	$I_{OUT}\left(\frac{V_{OUT}}{V_{IN}}\right)$
I_{L1}	$I_{OUT}\left(\frac{V_{OUT}}{V_{IN}}\right)$	$I_{OUT}\left(\frac{V_{OUT}}{V_{IN}}\right)$	$I_{OUT}\left(\frac{V_{OUT}}{V_{IN}} + \frac{N_S}{N_P}\right)$	$I_{OUT}\left(\frac{V_{OUT}}{V_{IN}} + 1\right)$	$I_{OUT}\left(\frac{V_{OUT}}{V_{IN}}\right)$
I_{L2}	I_{OUT}	I_{OUT}	$I_{OUT}\left(1 + \frac{N_S}{N_P}\frac{V_{OUT}}{V_{IN}}\right)$	–	–

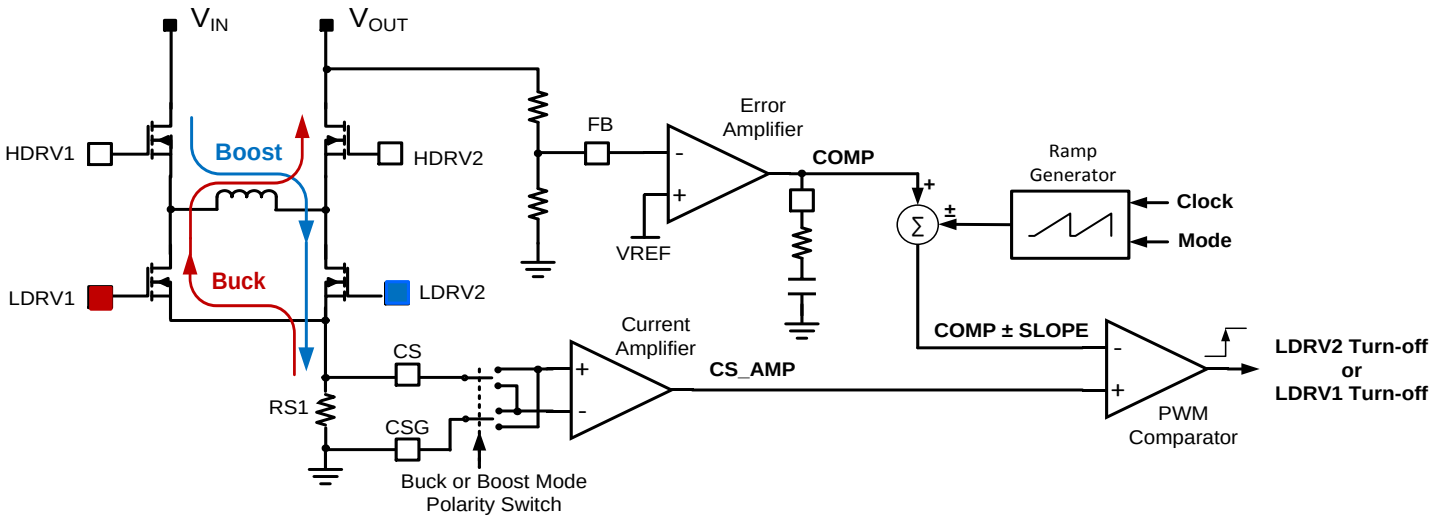
Buck-boost DC/DC converter progression

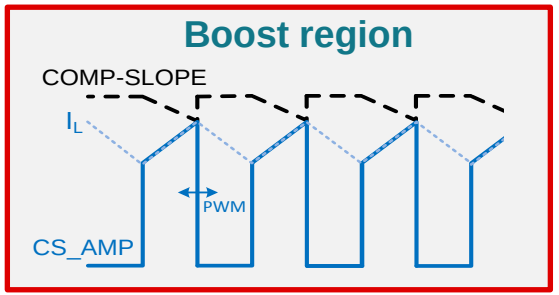


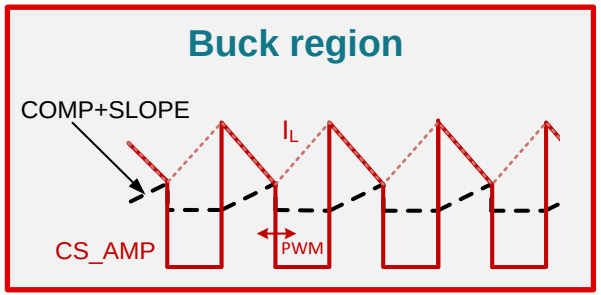
4-switch buck-boost converter power stage

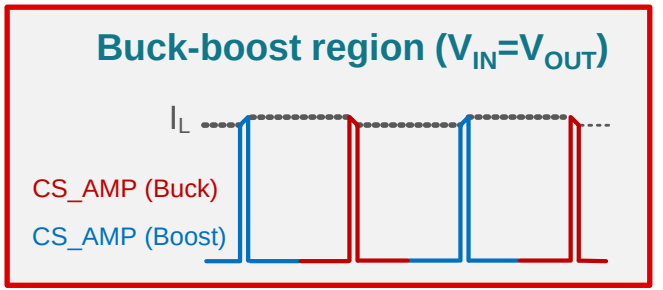


Current-mode control: peak boost and valley buck

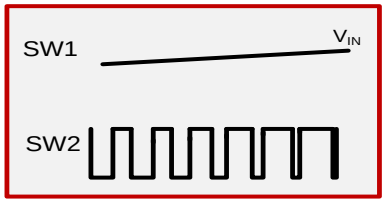


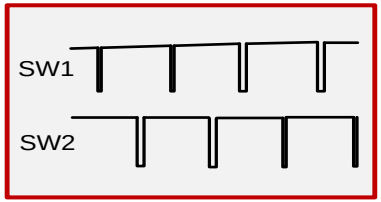


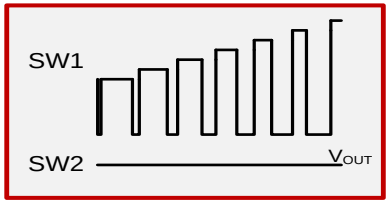


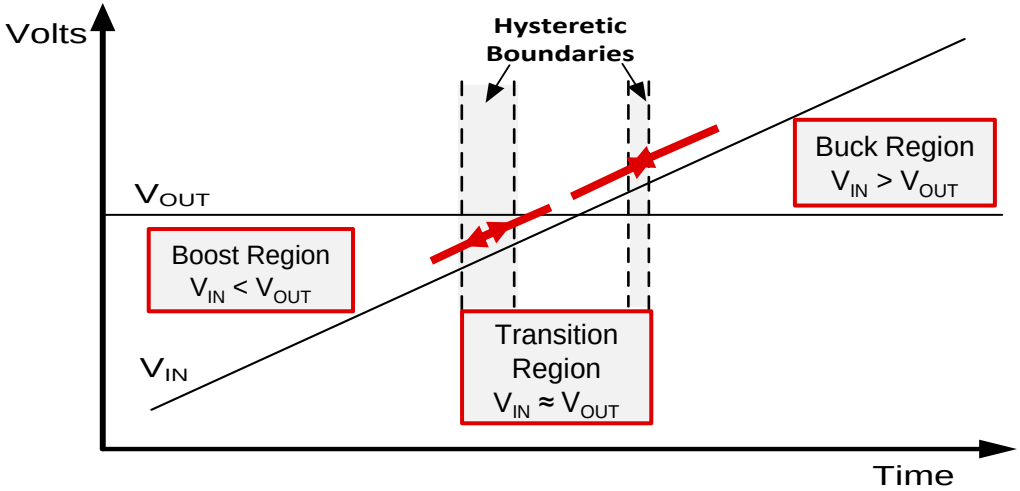


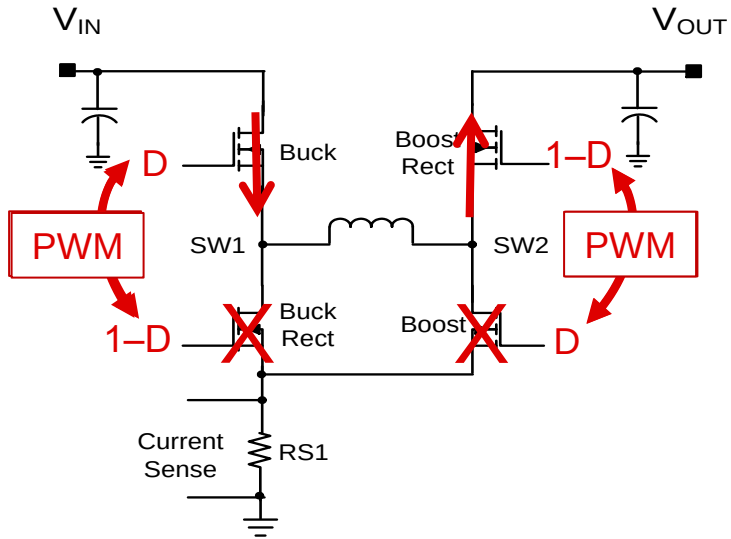
Buck-boost mode transitions











- Buck FET off-time < 250 ns ⇒ transition mode
- Boost FET on-time < 250 ns ⇒ transition mode
- Timer hysteresis eliminates chatter at boundary

4-switch buck-boost design example

Design parameters	Target specifications
Input voltage range, $V_{IN(min)}$–$V_{IN(max)}$	6 V-42 V
Output voltage, V_{OUT}	12 V
Maximum load current, $I_{OUT(max)}$	6 A
Switching frequency, F_{SW}	300 kHz
Operating mode	CCM, hiccup-mode OCP

Inductor selection

Inductance selection is based on

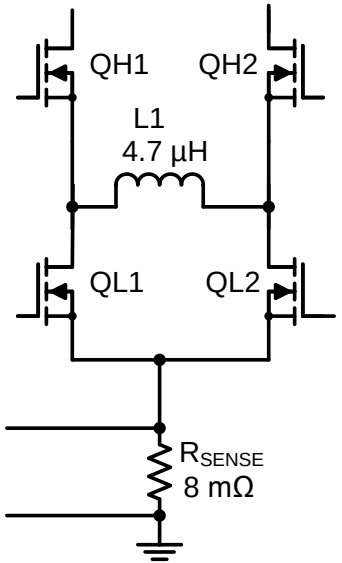
1. Target peak-to-peak ripple current
2. RMS and saturation current ratings
3. Size / cost

Set ripple current ratios in deep boost operating points at 20-40%:

$$L_{BOOST} = \frac{V_{IN(min)}^{2}\left(V_{OUT} - V_{IN(min)}\right)}{0.2 \times I_{OUT(max)} F_{sw} V_{OUT}^{2}} = 4.2\mu H$$

Select L1 = 4.7µH

V_{IN}	ΔI_{L1}
6 V	2.1 A
24 V	4.3 A
42 V	6.1 A



Inductor sat current rating:

$$I_{L(SAT)} \geq 1.5 \times \left(\frac{V_{OUT} \times I_{OUT(MAX)}}{0.9 \times V_{IN(MIN)}} + \frac{\Delta I_L}{2} \right) = 21.6A$$

$I_{IN(MAX)}$ in boost

Margin — Efficiency — Peak Ripple

C_{OUT} selection

Maximum RMS current in C_{OUT} occurs in boost mode

$$I_{COUT(rms)} = I_{OUT}\sqrt{\frac{V_{OUT}}{V_{IN}} - 1} = 6A$$

V_{OUT} ripple: related to ESR

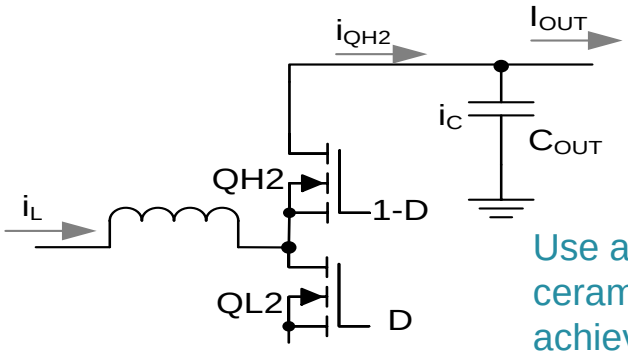
$$\Delta V_{RIPPLE(ESR)} = \frac{I_{OUT} V_{OUT}}{V_{IN(min)}} ESR$$

ESR (5 mΩ) ⟶ 60 mV

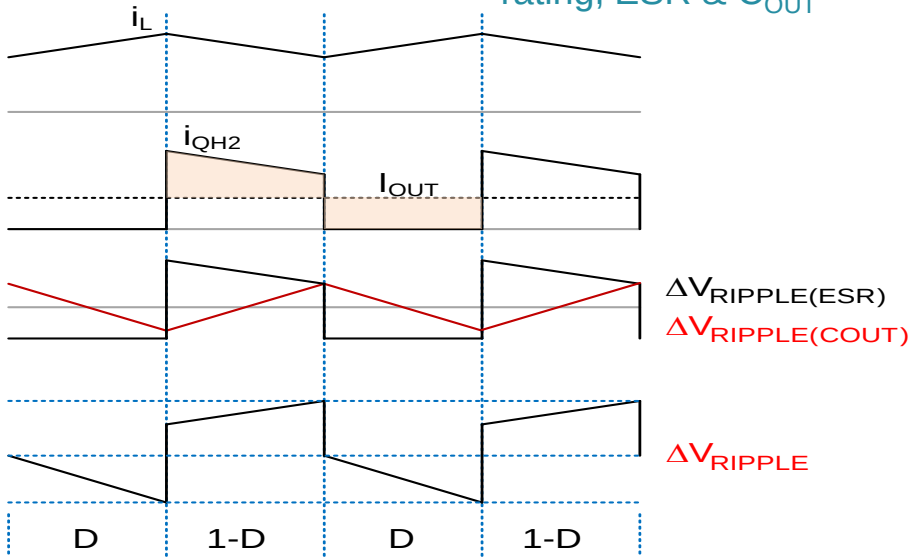
V_{OUT} ripple: related to C_{OUT}

$$\Delta V_{RIPPLE(C_{OUT})} = \frac{I_{OUT} D_{boost}}{C_{OUT} F_{sw}}$$

C_{OUT} (330µF) ⟶ 30mV



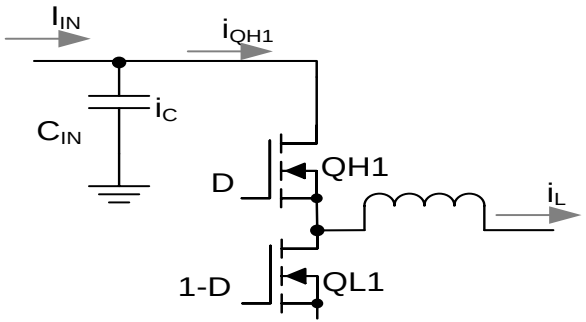
Use a combination of ceramic and bulk caps to achieve RMS current rating, ESR & C_{OUT}



C_{IN} selection

Maximum RMS current flowing in C_{IN} occurs in buck mode

$$I_{CIN(rms)} = I_{OUT}\sqrt{D(1-D)} = 3A$$



V_{IN} ripple: related to ESR

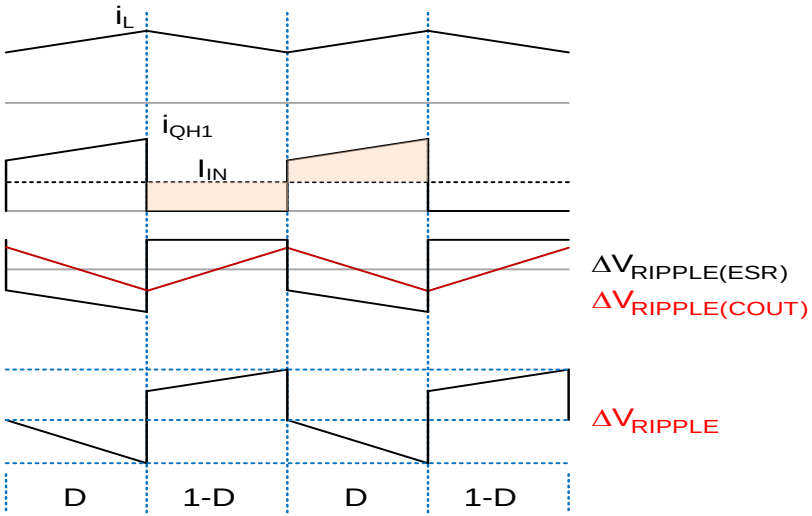
$$\Delta V_{RIPPLE(ESR)} = I_{OUT}ESR$$

ESR (25mΩ) ⟶ 150mV

V_{IN} ripple: related to C_{IN}

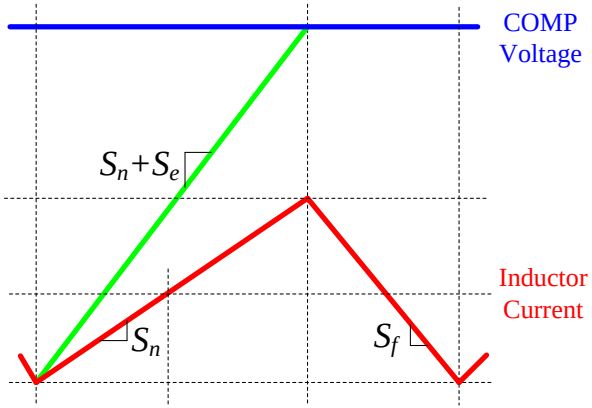
$$\Delta V_{RIPPLE(C_{IN})} = \frac{I_{OUT}D_{buck}(1-D_{buck})}{C_{IN}F_{sw}}$$

C_{IN} (68µF) ⟶ 75mV



Slope capacitance, C_{SLOPE}

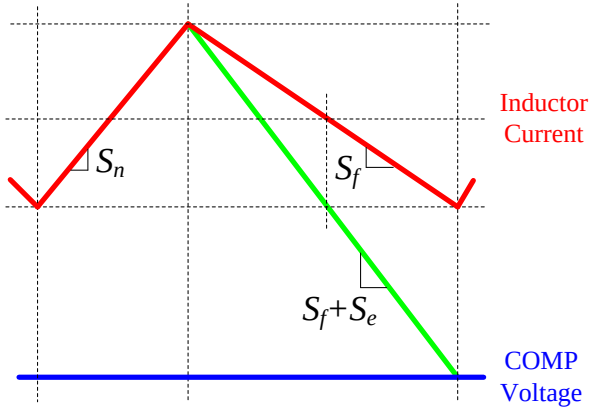
Peak current-mode boost



$$|S_n|+|S_f|=\frac{V_{in}}{L}+\frac{V_{out}-V_{in}}{L}=\frac{V_{out}}{L}$$

$$S_e=\frac{V_{out}-V_{in}}{L}$$

Valley current-mode buck



$$|S_n|+|S_f|=\frac{V_{in}-V_{out}}{L}+\frac{V_{out}}{L}=\frac{V_{in}}{L}$$

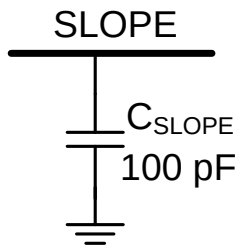
$$S_e=\frac{V_{in}-V_{out}}{L}$$

For ideal adaptive slope compensation, select

$$C_{SLOPE}=g_{m(slope)}\frac{L1}{R_{SENSE}A_{CS}}$$

$$=2\mu S\times\frac{4.7\mu H}{8m\Omega\times 5}=235\,pF$$

Select a slope cap of 100 pF to 2x calculated above
Lower C_{SLOPE} recommended for noise immunity



Converter small-signal model

Load pole

$$f_{p1(boost)} = \frac{1}{2\pi}\left(\frac{2}{R_{OUT}C_{OUT}}\right) = 398\,Hz$$

$$f_{p1(buck)} = \frac{1}{2\pi}\left(\frac{1}{R_{OUT}C_{OUT}}\right) = 199\,Hz$$

ESR zero

$$f_{z1} = \frac{1}{2\pi}\left(\frac{1}{R_{ESR}C_{OUT}}\right) = 79.6\,kHz$$

RHP zero

$$f_{zRHP} = \frac{1}{2\pi}\left(\frac{R_{OUT}\left(1-D_{Boost(max)}\right)^2}{L1}\right) = 16.9\,kHz$$

1/4 →

Target crossover frequency

$$F_c = 4\,kHz$$

Control loop compensation

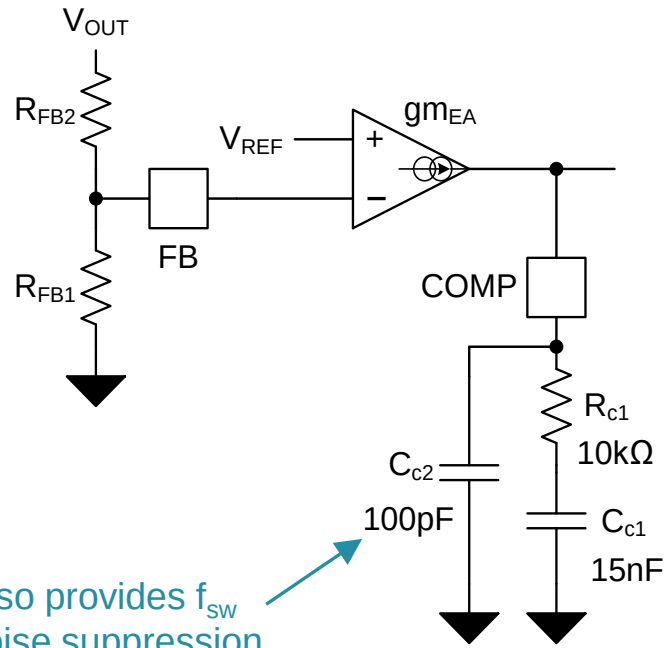
A_{CS} = 5 (current sense gain)

$$f_{zc} = 1\text{kHz}$$

$$R_{c1} = \frac{2\pi F_c}{gm_{EA}} \times \frac{R_{FB1} + R_{FB2}}{R_{FB1}} \times \frac{A_{CS} R_{SENSE} C_{OUT}}{1 - D_{max}} = 10.9\,\text{k}\Omega$$

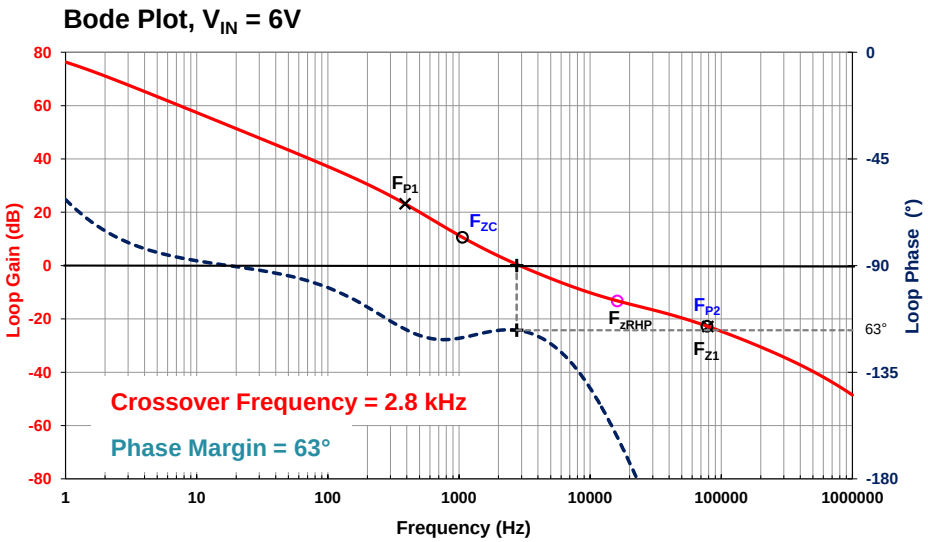
$$C_{c1} = \frac{1}{2\pi f_{zc} R_{c1}} = 15.9\,\text{nF}$$

$$C_{c2} = \frac{1}{2\pi f_{zESR} R_{c1}} = 106\,\text{pF}$$

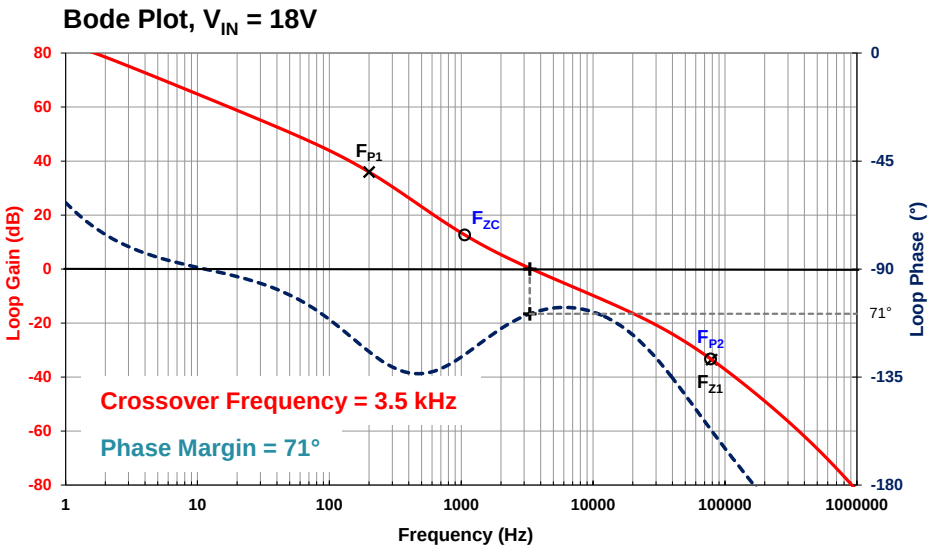


Control loop results

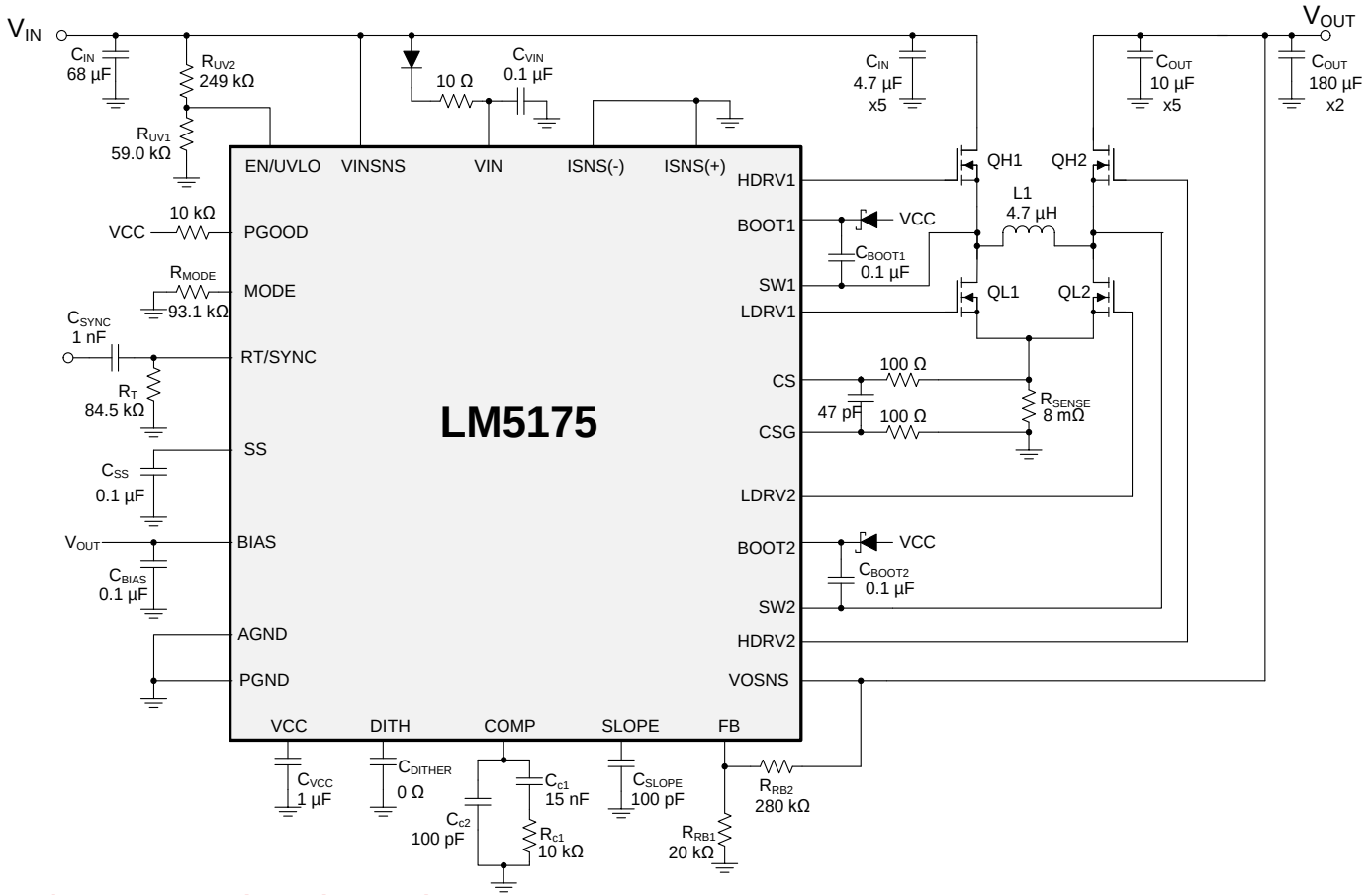
Boost-mode



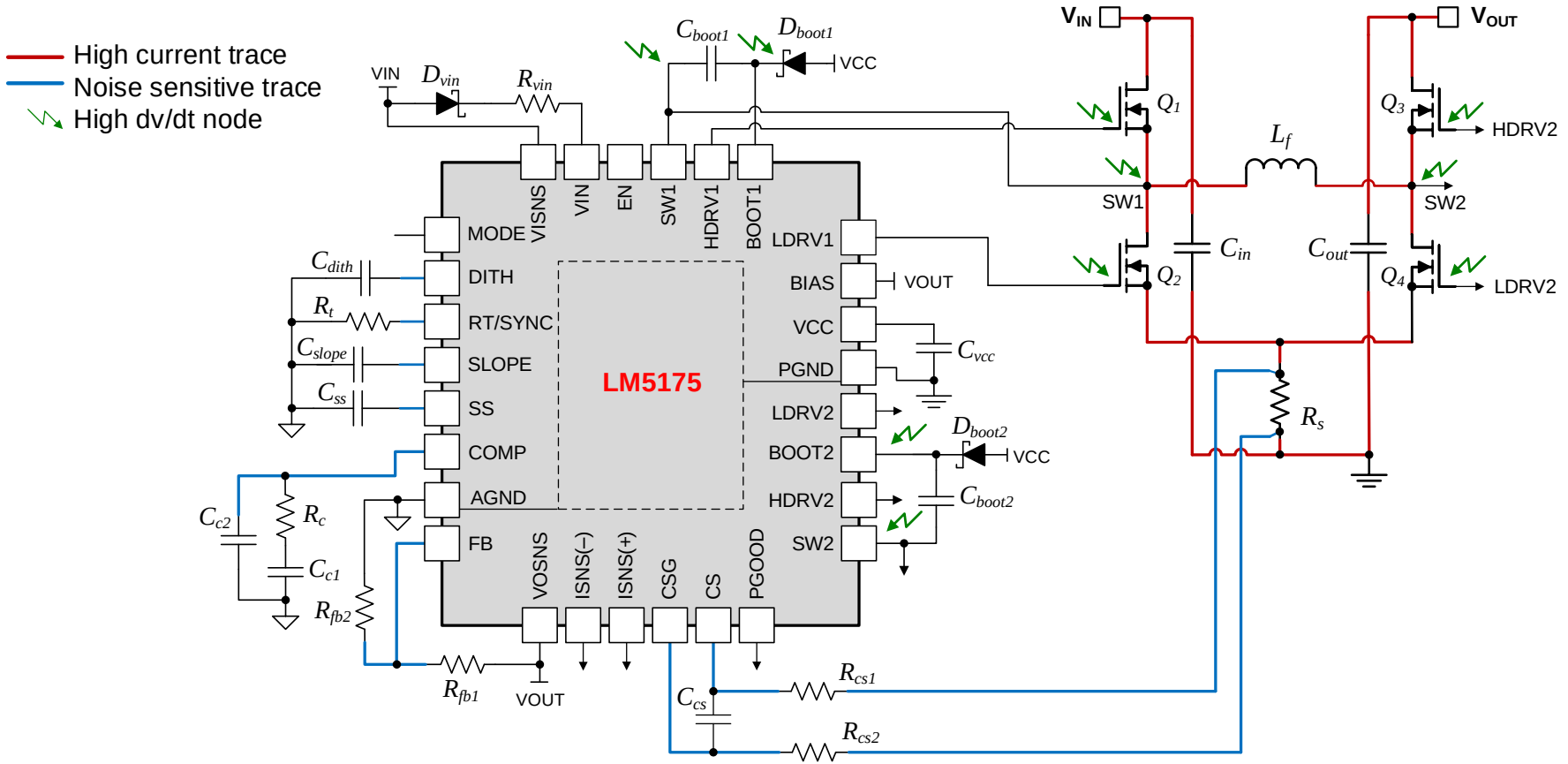
Buck-mode



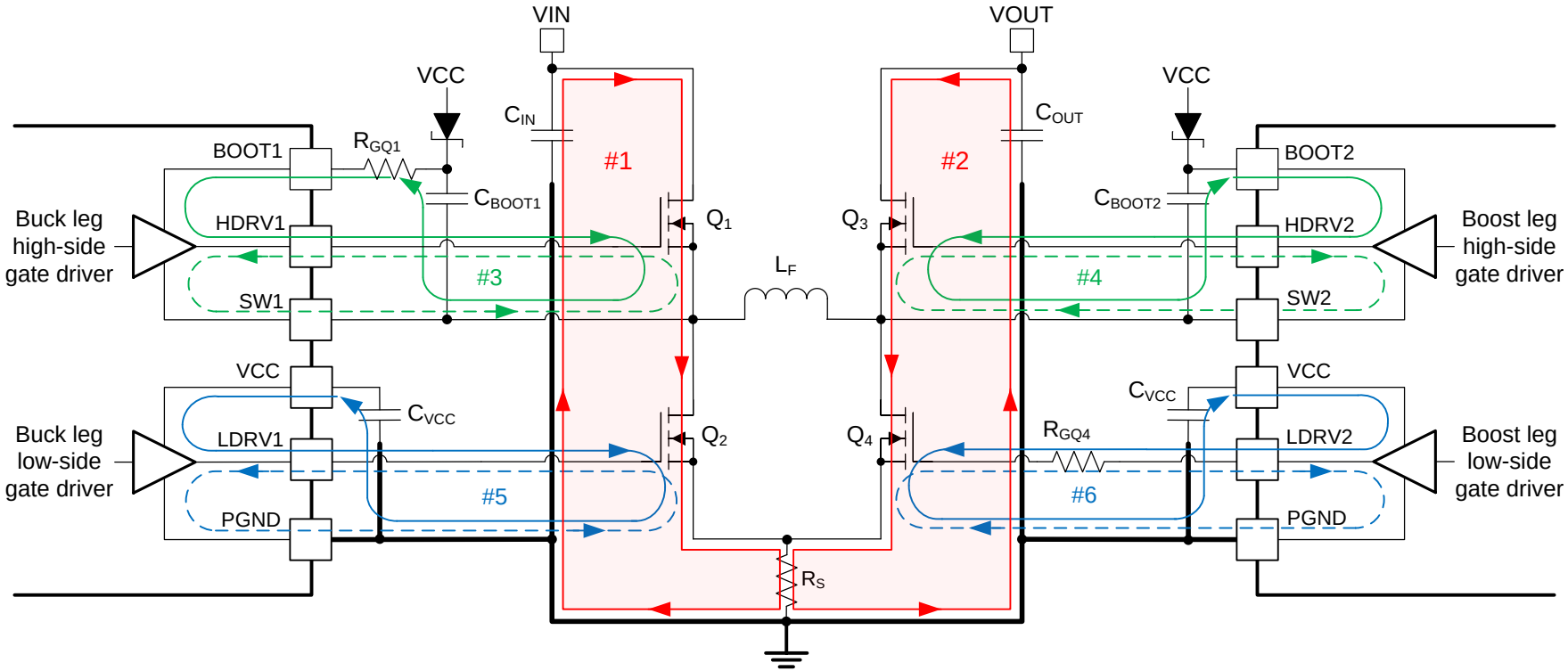
Reference schematic



Identify high di/dt and dv/dt, noise-sensitive traces



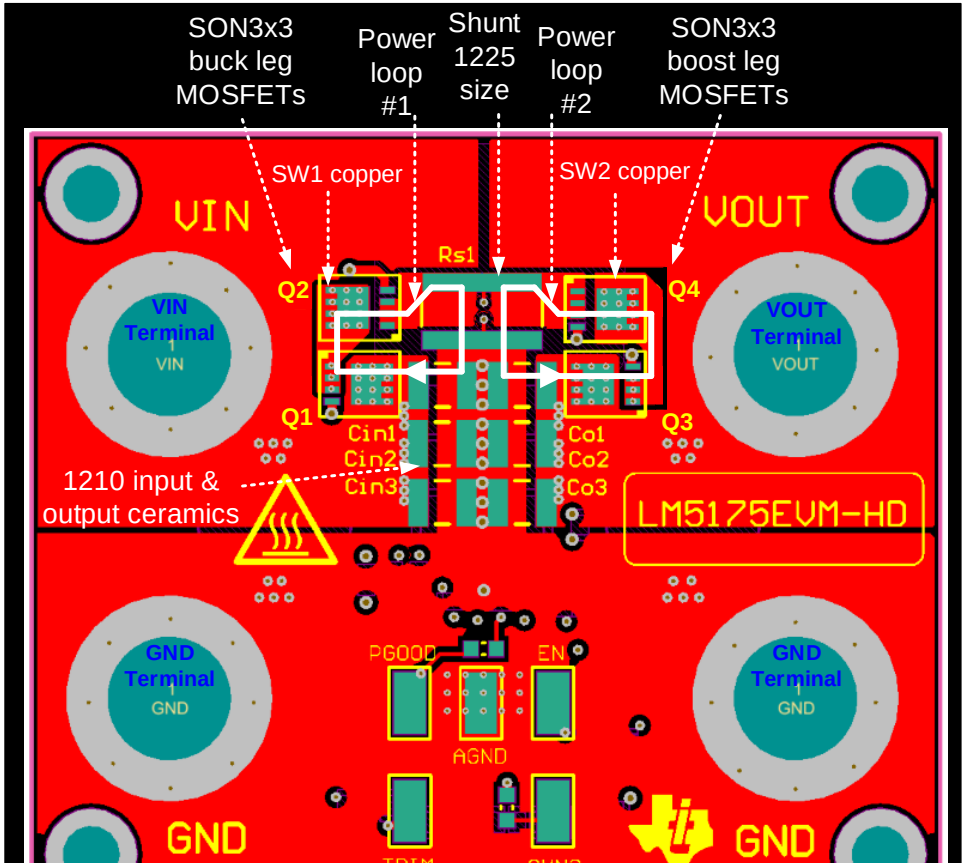
4-switch buck-boost converter “hot” loops

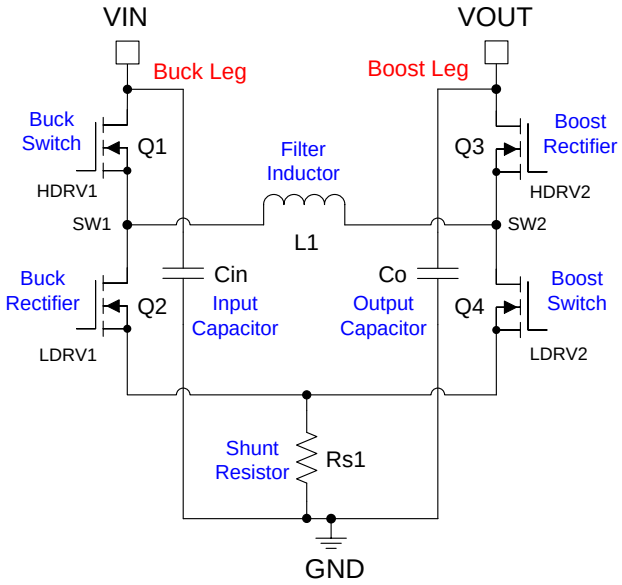


Minimizing *Power Loop* and *Gate Loop* parasitic inductances is very important

Both C_{IN} and C_{OUT} must be carefully placed in the PCB layout

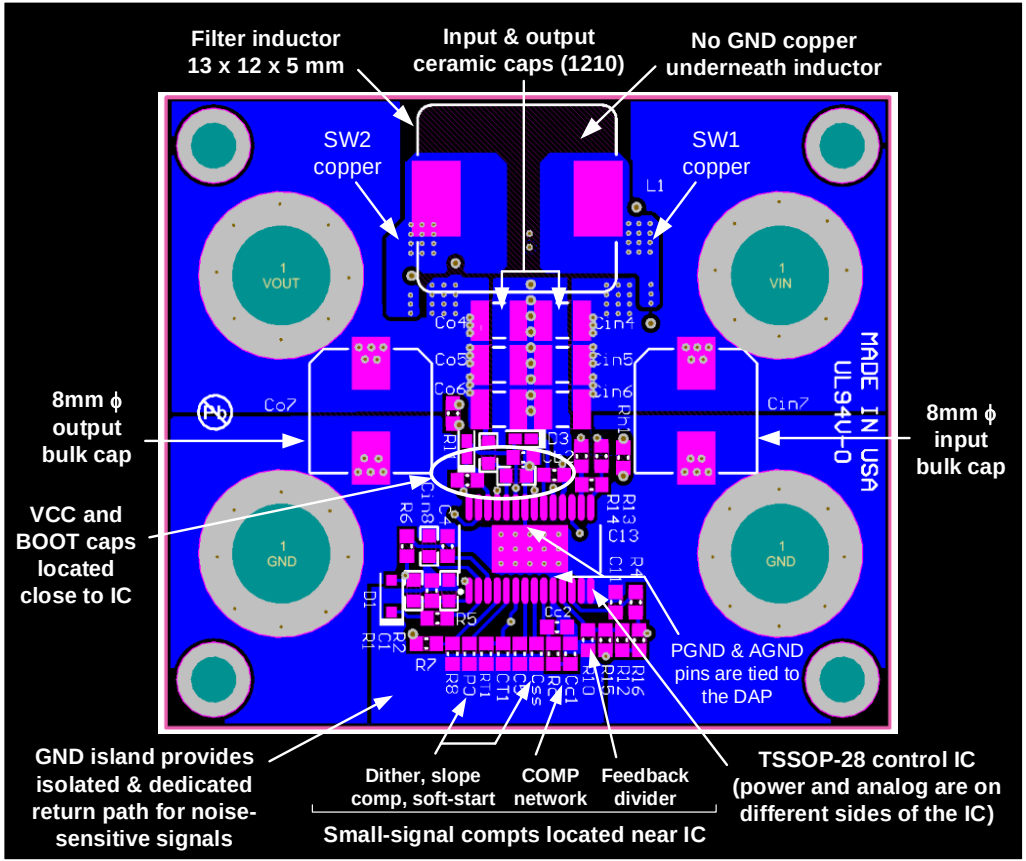
Top layer power stage routing





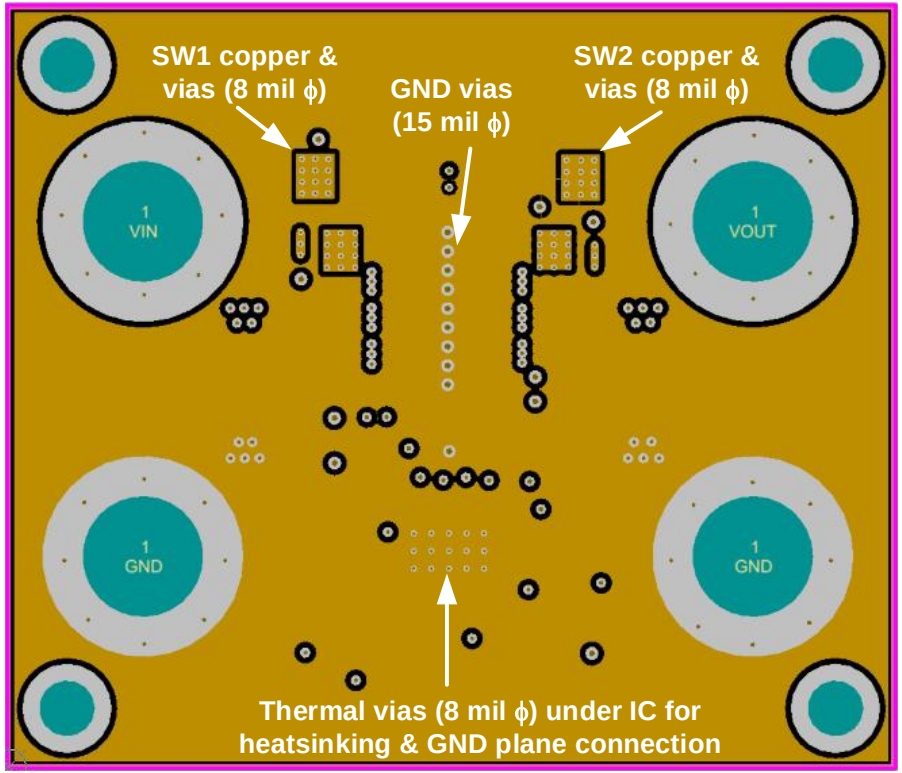
1. Place input caps close to buck leg MOSFETs
2. Place output caps close to boost leg MOSFETs
3. Keep shunt close to FETs for tight loop layout
4. VIN and VOUT planes provide heatsinking for high-side FETs

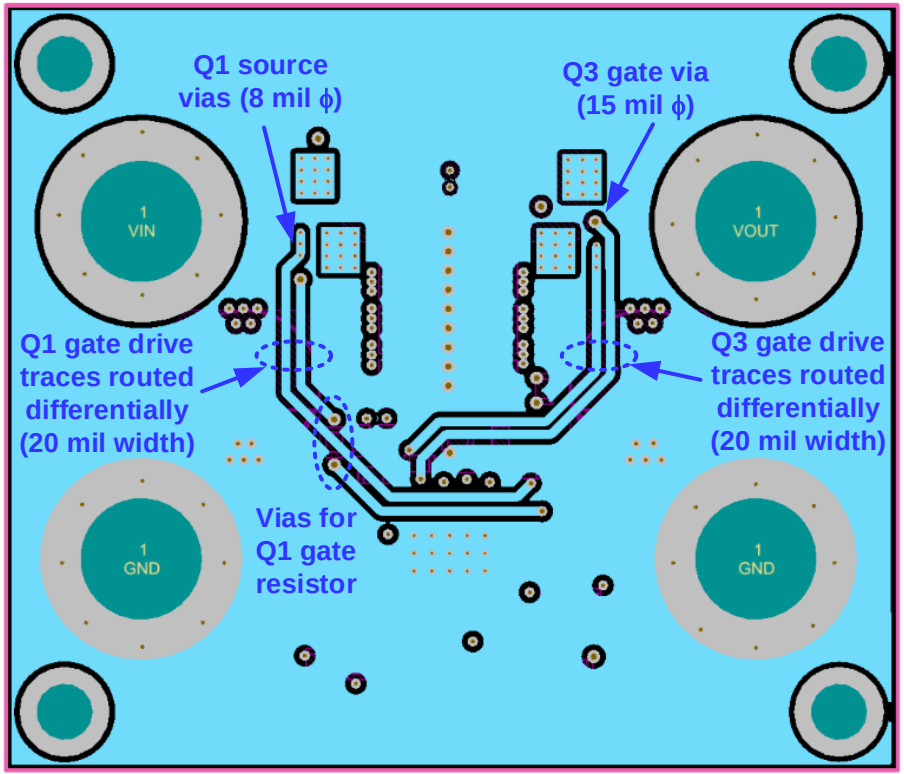
Bottom layer power stage and controller routing



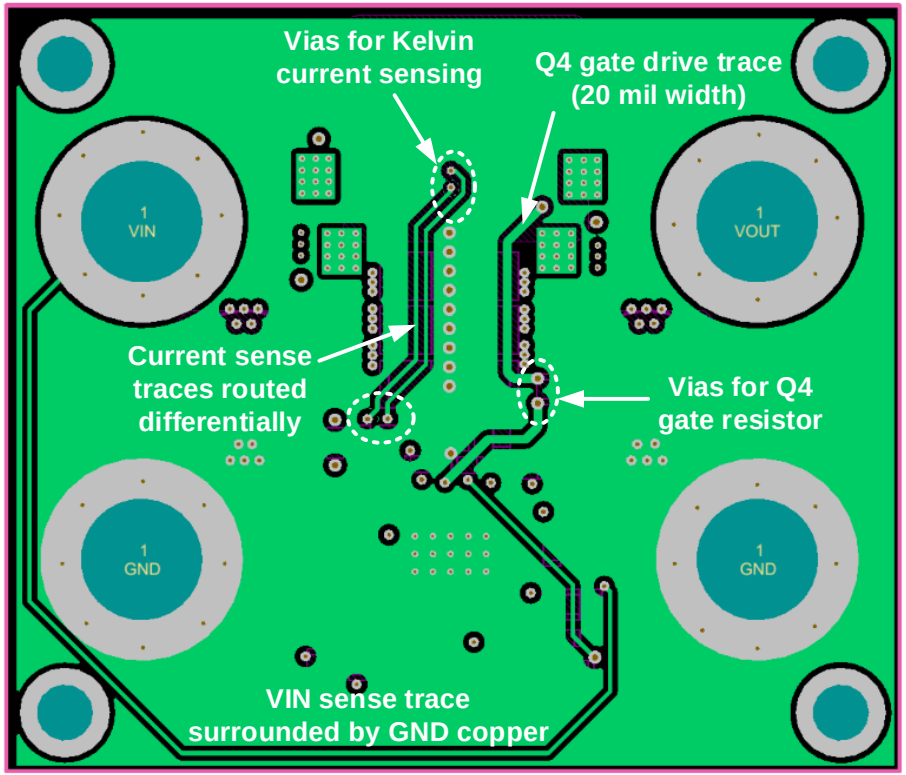
1. Connect PGND and AGND at DAP
2. Locate VCC and BOOT caps close to IC
3. Separate GND island for small-signal components
4. Current sense filter close to IC

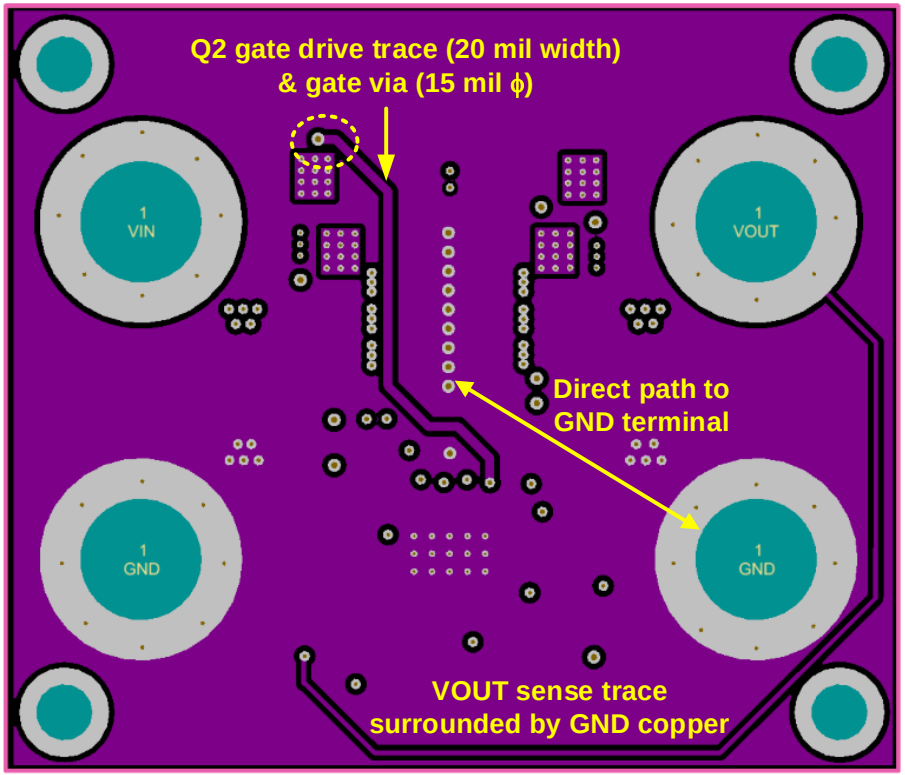
Layer 2: Solid GND plane; Layer 3: gate drives





Layers 4 & 5: Current sense and gate drives





Summary

- Buck-boost applications with step-up / step down conversion appear in many end-markets.
- Several topologies to choose from for buck-boost conversion.
  - Best fit chosen based on power level, efficiency, solution size and cost goals
- Single-inductor solutions dominate when high efficiency and output power are needed
  - 4-switch buck-boost reduces rectifier losses over entire operating range
  - Transition region switching losses are reduced when controller alternates between buck mode and boost mode.
- Application design example provided a working solution for a 12 V / 72 W converter with wide 6 V to 42 V input range.
- PC board layout design begins with identification of high dv/dt nodes and high di/dt loops. Best performance is achieved when current loops are short and sensitive nodes are spaced well away from noise generating traces.

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