

# Questions

1. **What is a computer architecture?**
  - a) The physical components that make up a computer system
  - b) The design of the software used in a computer system
  - ct* c) The way in which a computer system is organized and operated
  - d) The language used to program a computer system
2. **Which of the following is a component of the CPU?**
  - a) Hard disk
  - b) RAM
  - ct* c) Control unit
  - d) Monitor
3. **Which of the following is an example of a volatile memory?**
  - a) Hard disk
  - ct* b) RAM
  - c) CD-ROM
  - d) Flash drive
4. **Which of the following is an example of a high-level programming language?**
  - a) Assembly language
  - b) Machine language
  - ct* c) C++
  - d) Binary code
5. **Which of the following is a function of an input/output controller?**
  - a) To manage the flow of data between the CPU and memory
  - bt* b) To manage the flow of data between input/output devices and the CPU
  - c) To perform arithmetic and logical operations
  - d) To interpret and execute program instructions
6. **Which of the following is an example of a secondary storage device?**
  - a) RAM
  - bt* b) Hard disk
  - c) CPU
  - d) Cache memory
7. **What is the purpose of a compiler?**
  - at* a) To translate high-level programming code into machine code
  - b) To manage computer hardware resources
  - c) To provide security against viruses and malware
  - d) To create and edit documents
8. **Which of the following is an example of a pipelining technique used in CPU design?**
  - a) Von Neumann architecture
  - b) Reduced Instruction Set Computing (RISC)

- c) Complex Instruction Set Computing (CISC)  
 d) Superscalar execution
9. Which of the following is an example of a parallel processing technique used in computer architecture?  
a) Multitasking  
b) Multithreading  
 c) Multiprocessing  
d) All of the above
10. Which of the following is an example of a cache memory?  
a) Hard disk  
b) RAM  
c) Flash drive  
 d) CPU cache
11. Which of the following is an example of a system bus?  
a) SATA bus  
b) USB bus  
 c) PCI bus  
d) All of the above
12. Which of the following is an example of an instruction set architecture?  
a) x86  
b) ARM  
c) MIPS  
 d) All of the above
13. Which of the following is an example of a virtual memory technique used in computer architecture?  
 a) Paging  
b) Cache memory  
c) Multitasking  
d) Superscalar execution
14. Which of the following is an example of a microarchitecture design?  
a) Intel Pentium  
b) AMD Ryzen
- c) ARM Cortex-A9  
 d) All of the above
15. Which of the following is an example of an interrupt handling mechanism in computer architecture?  
 a) Interrupt service routine  
b) Input/output controller  
c) Control unit  
d) Memory management unit
16. Which of the following is an example of a register used in CPU design?  
a) Cache memory  
b) Hard disk  
 c) Accumulator  
d) CD-ROM
17. Which of the following is an example of a branch prediction technique used in CPU design?  
a) Dynamic branch prediction  
b) Static branch prediction  
 c) Both a and b  
d) None of the above
18. What is the purpose of a memory management unit (MMU) in computer architecture?  
a) To manage the flow of data between input/output devices and the CPU  
 b) To translate virtual memory addresses to physical memory addresses

- c) To interpret and execute program instructions
- d) To manage computer hardware resources

19. Which of the following is an example of a data transfer technique used in computer architecture?

- a) Direct memory access (DMA)
- b) Virtual memory
- c) Paging
- d) Branch prediction

20. Which of the following is an example of a pipelining stage used in CPU design?

- a) Fetch
- b) Decode
- c) Execute

d) All of the above

21. Which of the following is an example of a cache coherence protocol used in computer architecture?

- a) Snoopy protocol
- b) MESI protocol

c) Both a and b

- d) None of the above

22. Which of the following is an example of a processor interconnect used in computer architecture?

- a) HyperTransport
- b) PCI Express

c) Both a and b

- d) None of the above

23. What is the purpose of a branch target buffer (BTB) in CPU design?

- a) To predict the outcome of a branch instruction

- b) To store the target address of a branch instruction
- c) To store the address of the next instruction to be executed
- d) To store the result of a previous instruction

24. Which of the following is an example of a hazard in CPU design?

- a) Structural hazard
- b) Data hazard
- c) Control hazard

d) All of the above

25. Which of the following is an example of a superscalar processor?

- a) Intel Core i7
- b) AMD Ryzen 7

c) Both a and b

- d) None of the above

26. Which of the following is an example of a memory hierarchy in computer architecture?

- a) Cache memory
- b) RAM
- c) Hard disk

d) All of the above

27. What is the purpose of a system call in operating system design?

- a) To execute a program instruction
- b) To manage computer hardware resources

c) To provide an interface for user-level applications to interact with the kernel

- d) To perform arithmetic and logical operations

- 28. Which of the following is an example of a vector processor?**
- a) Intel Pentium
  - b) AMD Ryzen
  - c) NVIDIA Tesla
  - d) All of the above
- 29. Which of the following is an example of a bus arbitration technique used in computer architecture?**
- a) Round-robin arbitration
  - b) Priority arbitration
  - c) Both a and b
  - d) None of the above
- 30. Which of the following is an example of a pipeline stall in CPU design?**
- a) A data hazard occurs
  - b) A control hazard occurs
  - c) A structural hazard occurs
  - d) All of the above
- 31. Which of the following is an example of a performance metric used to evaluate CPU design?**
- a) Clock speed
  - b) Cache size
  - c) Instruction set architecture
  - d) All of the above
- 32. Which of the following is an example of a hardware-based security mechanism in computer architecture?**
- a) Firewall
  - b) Antivirus software
  - c) Trusted Platform Module (TPM)
  - d) Encryption software
- 33. Which of the following is an example of a load-store architecture?**
- a) x86
  - b) ARM
  - c) MIPS
  - d) All of the above
- 34. Which of the following is an example of a branch delay slot in CPU design?**
- a) The instruction following a branch instruction is executed before the branch instruction
  - b) The instruction following a branch instruction is not executed if the branch is taken
  - c) The instruction preceding a branch instruction is executed after the branch instruction
  - d) None of the above
- 35. Which of the following is an example of a cache replacement policy used in computer architecture?**
- a) Least Recently Used (LRU)
  - b) First In, First Out (FIFO)
  - c) Both a and b
  - d) None of the above
- 36. Which of the following is an example of a speculative execution technique used in CPU design?**
- a) Out-of-order execution
  - b) Superscalar execution
  - c) Branch prediction

- a) All of the above
37. Which of the following is an example of a power management technique used in computer architecture?  
 a) Dynamic voltage and frequency scaling (DVFS)  
b) Interrupt handling  
c) Cache coherence  
d) Direct memory access (DMA)
38. Which of the following is an example of a data hazard in CPU design?  
 a) A load instruction depends on the result of a previous store instruction  
b) Two instructions compete for the same hardware resource  
c) A branch instruction changes the flow of program execution  
d) None of the above
39. Which of the following is an example of a multiprocessor system?  
a) Symmetric multiprocessing (SMP)  
b) Asymmetric multiprocessing (AMP)  
 c) Both a and b  
d) None of the above
40. Which of the following is an example of a cache coherence protocol used in multiprocessor systems?  
a) MSI protocol  
b) MOESI protocol  
 c) Both a and b  
d) None of the above
41. Which of the following is an example of a memory consistency model used in multiprocessor systems?  
a) Sequential consistency  
b) Release consistency  
 c) Both a and b  
d) None of the above
42. Which of the following is an example of a bus-based interconnect used in computer architecture?  
a) Front-side bus (FSB)  
b) QuickPath Interconnect (QPI)  
 c) Both a and b  
d) None of the above
43. Which of the following is an example of a cache line size in computer architecture?  
a) 32 bytes  
b) 64 bytes  
c) 128 bytes  
 d) All of the above
44. Which of the following is an example of a memory access latency in computer architecture?  
a) The time it takes to access data from cache memory  
 b) The time it takes to access data from main memory  
c) The time it takes to access data from a hard disk  
d) All of the above
45. Which of the following is an example of a data cache in computer architecture?  
a) L1 cache  
b) L2 cache  
 c) Both a and b

- d) None of the above

**46. Which of the following is an example of a branch predictor in CPU design?**

- a) Two-level adaptive predictor (TAGE)
- b) Gshare predictor
- c) Both a and b
- d) None of the above

**47. Which of the following is an example of a vector instruction in CPU design?**

- a) ADD
- b) MUL
- c) Both a and b
- d) None of the above

**48. Which of the following is an example of a cache associativity in computer architecture?**

- a) Direct-mapped cache
- b) Fully associative cache
- c) Set-associative cache
- d) All of the above

**49. Which of the following is an example of a memory hierarchy in computer architecture?**

- a) Registers, cache, main memory, hard disk
- b) Main memory, cache, registers, hard disk
- c) Cache, main memory, registers, hard disk
- d) None of the above

**50. Which of the following is an example of a page table in computer architecture?**

- a) A data structure used to map virtual addresses to physical addresses
- b) A hardware component that

manages memory accesses

- c) Both a and b
- d) None of the above

**51. Which of the following is an example of a TLB (Translation Lookaside Buffer) in computer architecture?**

- a) A cache for page table entries
- b) A hardware component that translates virtual addresses to physical addresses
- c) Both a and b
- d) None of the above

**52. Which of the following is an example of a cache coherence problem in multiprocessor systems?**

- a) False sharing
- b) Cache line thrashing
- c) Both a and b
- d) None of the above

**53. Which of the following is an example of a cache write policy in computer architecture?**

- a) Write-through
- b) Write-back
- c) Both a and b
- d) None of the above

**54. Which of the following is an example of a memory access granularity in computer architecture?**

- a) Byte
- b) Word
- c) Block
- d) All of the above

**55. Which of the following is an example of a memory**

**access bandwidth in computer architecture?**

- a) The amount of data that can be transferred in a single memory access
- b) The number of memory accesses that can be performed in a given time period
- c) Both a and b
- d) None of the above

**56. Which of the following is an example of a branch target buffer in CPU design?**

- a) A cache for branch instructions
- b) A hardware component that predicts the target address of a branch instruction
- c) Both a and b
- d) None of the above

**57. Which of the following is an example of a superscalar processor?**

- a) Intel Core i7
- b) AMD Ryzen
- c) Both a and b
- d) None of the above

**58. Which of the following is an example of a pipelined processor?**

- a) Intel Pentium
- b) IBM PowerPC
- c) Both a and b
- d) None of the above

**59. Which of the following is an example of a RISC (Reduced Instruction Set Computing) processor architecture?**

- a) ARM
- b) Intel x86

c) Both a and b

d) None of the above

**60. Which of the following is an example of a CISC (Complex Instruction Set Computing) processor architecture?**

- a) Intel x86
- b) ARM
- c) Both a and b
- d) None of the above

**61. Which of the following is an example of a VLIW (Very Long Instruction Word) processor architecture?**

- a) Intel Itanium
- b) AMD Athlon
- c) Both a and b
- d) None of the above

**62. Which of the following is an example of a SIMD (Single Instruction Multiple Data) processor architecture?**

- a) Intel Xeon Phi
- b) NVIDIA GPU
- c) Both a and b
- d) None of the above

**63. Which of the following is an example of a MIMD (Multiple Instruction Multiple Data) processor architecture?**

- a) Intel Xeon
- b) IBM PowerPC
- c) Both a and b
- d) None of the above

**64. Which of the following is an example of a microcontroller?**

- a) Arduino
- b) Raspberry Pi
- c) Both a and b
- d) None of the above

**65. Which of the following is an example of a microprocessor?**

- a) Intel Core i7
- b) AMD Ryzen
- c) Both a and b
- d) None of the above

**66. Which of the following is an example of a system-on-chip (SoC)?**

- a) Qualcomm Snapdragon
- b) Apple A-series
- c) Both a and b
- d) None of the above

**67. Which of the following is an example of a memory-mapped I/O in computer architecture?**

- a) Using the same address space for both memory and I/O operations
- b) Using a separate address space for I/O operations
- c) Both a and b
- d) None of the above

**68. Which of the following is an example of a register in a computer processor?**

- a) Program Counter (PC)
- b) Instruction Register (IR)
- c) Both a and b
- d) None of the above

**69. Which of the following is an example of a cache memory?**

- a) Level 1 (L1) cache
- b) Level 2 (L2) cache
- c) Both a and b
- d) None of the above

**70. Which of the following is an example of a virtual memory management technique?**

- a) Paging
- b) Segmentation
- c) Both a and b
- d) None of the above

**71. Which of the following is an example of a RAID (Redundant Array of Inexpensive Disks) configuration?**

- a) RAID 0
- b) RAID 1
- c) Both a and b
- d) None of the above

**72. Which of the following is an example of a system call in computer architecture?**

- a) open()
- b) close()
- c) Both a and b
- d) None of the above

**73. Which of the following is an example of a privilege level in a computer processor?**

- a) User mode
- b) Kernel mode
- c) Both a and b
- d) None of the above

**74. Which of the following is an example of a pipelining hazard?**

- a) Structural hazard
- b) Data hazard
- c) Control hazard
- d) All of the above

**75. Which of the following is an example of a superscalar processor architecture?**

- a) Intel Pentium 4
- b) AMD Athlon 64
- c) Both a and b

- d) None of the above

76. Which of the following is an example of a memory hierarchy?

- a) Registers, cache, main memory, secondary storage
- b) Cache, registers, main memory, secondary storage
- c) Main memory, cache, registers, secondary storage
- d) Secondary storage, main memory, cache, registers

77. Which of the following is an example of a parallel computing model?

- a) Shared memory model
- b) Distributed memory model
- c) Both a and b
- d) None of the above

78. Which of the following is an example of a cache replacement policy?

- a) Least Recently Used (LRU)
- b) First-In-First-Out (FIFO)
- c) Both a and b
- d) None of the above

79. Which of the following is an example of a DMA (Direct Memory Access) operation?

- a) Copying data from main memory to cache
- b) Copying data from cache to a register

- e) Copying data from a peripheral device to main memory

- d) None of the above

80. Which of the following is an example of a cache coherence problem?

- a) Cache thrashing
- b) Cache contention
- c) Both a and b
- d) None of the above

81. Which of the following is an example of a data dependency in computer architecture?

- a) RAW (Read-After-Write)
- b) WAR (Write-After-Read)
- c) WAW (Write-After-Write)
- d) All of the above

82. Which of the following is an example of a pipelining stage in a computer processor?

- a) Instruction fetch
- b) Register write
- c) Both a and b
- d) None of the above

83. Which of the following is an example of a cache miss?

- a) When the requested data is present in the cache
- b) When the requested data is not present in the cache and needs to be fetched from main memory
- c) Both a and b
- d) None of the above

84. Which of the following is an example of a RISC (Reduced

**Instruction Set Computing) processor?**

- a) ARM
- b) Intel Core i7
- c) Both a and b
- d) None of the above

**85. Which of the following is an example of a CISC (Complex Instruction Set Computing) processor?**

- a) Intel Pentium
- b) ARM
- c) Both a and b
- d) None of the above

**86. Which of the following is an example of a virtual memory management technique?**

- a) Paging
- b) Segmentation
- c) Both a and b
- d) None of the above

**87. Which of the following is an example of a cache write policy?**

- a) Write-through
- b) Write-back
- c) Both a and b
- d) None of the above

**88. Which of the following is an example of a pipelining hazard?**

- a) Data hazard
- b) Control hazard
- c) Both a and b
- d) None of the above

**89. Which of the following is an example of a data hazard?**

- a) RAW (Read After Write) hazard
- b) WAW (Write After Write) hazard
- c) WAR (Write After Read) hazard

d) None of the above

**90. Which of the following is an example of a control hazard?**

- a) Branch hazard
- b) Jump hazard
- c) Both a and b
- d) None of the above

**91. Which of the following is an example of a hazard mitigation technique?**

- a) Stalling the pipeline
- b) Branch prediction
- c) Both a and b
- d) None of the above

**92. Which of the following is an example of a hardware-based speculation technique?**

- a) Speculative execution
- b) Speculative precomputation
- c) Both a and b
- d) None of the above

**93. Which of the following is an example of a software-based speculation technique?**

- a) Software pipelining
- b) Loop unrolling
- c) Both a and b
- d) None of the above

**94. Which of the following is not a typical component of a CPU?**

- a) ALU (Arithmetic Logic Unit)
- b) Control Unit
- c) Cache Memory
- d) Hard Disk Drive

**95. Which of the following is not a type of cache memory?**

- a) L1 cache

- b) L2 cache
- c) RAM cache
- d) L3 cache

96. Which of the following is not a common method for increasing CPU performance?

- a) Increasing clock speed
- b) Increasing the number of cores
- c) Increasing cache size
- d) Decreasing the amount of RAM

97. Which of the following is a type of computer memory that is non-volatile?

- a) RAM (Random Access Memory)
- b) ROM (Read-Only Memory)
- c) SRAM (Static Random Access Memory)
- d) DRAM (Dynamic Random Access Memory)

98. Which of the following is not a type of secondary storage?

- a) Hard Disk Drive (HDD)
- b) Solid State Drive (SSD)
- c) Flash Drive
- d) RAM

99. Which of the following is not a type of RAID?

- a) RAID 0
- b) RAID 1
- c) RAID 2
- d) RAID 5

100. Which of the following is not a common type of I/O device?

- a) Keyboard
- b) Monitor
- c) Printer

## ✓ CPU

101. Which of the following statements about pipelining is false?

- a) Pipelining increases the throughput of a CPU.
- b) Pipelining reduces the latency of a CPU.
- c) ✓ Pipelining increases the clock frequency of a CPU.
- d) Pipelining requires the CPU to be split into stages.

102. Which of the following stages is not typically found in a CPU pipeline?

- a) Instruction fetch
- b) Instruction decode
- c) Data memory access
- d) ✓ Disk I/O

103. Which of the following hazards can occur in a pipeline?

- a) Structural hazards
- b) Data hazards
- c) Control hazards
- d) ✓ All of the above

104. What is the purpose of branch prediction in a CPU pipeline?

- a) To prevent data hazards
- b) ✓ To prevent control hazards
- c) To prevent structural hazards
- d) To increase the clock frequency

105. What is the advantage of a superscalar pipeline over a scalar pipeline?

- a) Superscalar pipelines are faster.

- b) Superscalar pipelines are simpler.
- c) Superscalar pipelines can execute multiple instructions per clock cycle.
- d) Superscalar pipelines do not require branch prediction.

- 106. What is the purpose of instruction-level parallelism (ILP) in a CPU pipeline?**
- a) To increase the clock frequency of the CPU
  - b) To increase the size of the CPU cache
  - c) To enable the CPU to execute multiple instructions in parallel
  - d) To reduce the number of pipeline stages

- 107. Which of the following pipeline stages is responsible for executing the actual operation specified by an instruction?**
- a) Instruction fetch
  - b) Instruction decode
  - c) Execution
  - d) Writeback

- 108. Which of the following is an example of a structural hazard in a pipeline?**
- a) An instruction depends on the result of a previous instruction that has not yet completed
  - b) Two instructions require the same hardware resource at the same time

- c) The pipeline incorrectly predicts the outcome of a branch instruction
- d) A long-latency instruction stalls the pipeline

- 109. Which of the following techniques can be used to reduce data hazards in a pipeline?**
- a) Loop unrolling
  - b) Register renaming
  - c) Branch prediction
  - d) Instruction scheduling

- 110. What is the purpose of the writeback stage in a CPU pipeline?**
- a) To write the result of an instruction back to memory
  - b) To write the result of an instruction back to a register
  - c) To fetch the next instruction from memory
  - d) To decode the next instruction

- 111. Which of the following pipeline stages is responsible for fetching the next instruction from memory?**
- a) Instruction fetch
  - b) Instruction decode
  - c) Execution
  - d) Writeback

- 112. Which of the following techniques can be used to reduce control hazards in a pipeline?**
- a) Register renaming
  - b) Loop unrolling
  - c) Branch prediction

- d) Instruction scheduling
- 113. What is the purpose of forwarding in a CPU pipeline?**
- a) To reduce the latency of long-latency instructions
  - b) To prevent control hazards
  - c) To prevent data hazards
  - d) To increase the clock frequency of the CPU
- 114. Which of the following is an example of a long-latency instruction that can cause pipeline stalls?**
- a) Addition
  - b) Multiplication
  - c) Branch
  - d) Load from memory
- 115. Which of the following pipeline stages is responsible for decoding the instruction and determining the required operation?**
- a) Instruction fetch
  - b) Instruction decode
  - c) Execution
  - d) Writeback
- 116. Which of the following techniques can be used to reduce pipeline stalls due to long-latency instructions?**
- a) Loop unrolling
  - b) Register renaming
  - c) Branch prediction
  - d) Instruction scheduling
- 117. Which of the following pipeline stages is responsible for reading operands from registers or memory?**
- a) Instruction fetch
  - b) Instruction decode
  - c) Execution
  - d) Writeback
- 118. Which of the following techniques can be used to reduce the impact of branch instructions on the pipeline?**
- a) Loop unrolling
  - b) Register renaming
  - c) Branch prediction
  - d) Instruction scheduling
- 119. Which of the following pipeline stages is responsible for writing the result of an instruction back to memory?**
- a) Instruction fetch
  - b) Instruction decode
  - c) Execution
  - d) Writeback
- 120. Which of the following is an example of a data hazard in a pipeline?**
- a) A long-latency instruction stalls the pipeline
  - b) Two instructions require the same hardware resource at the same time
  - c) The pipeline incorrectly predicts the outcome of a branch instruction
  - d) An instruction depends on the result of a previous instruction that has not yet completed

- 121. Which of the following pipeline stages is responsible for checking for and resolving data hazards?**
- a) Instruction fetch
  - b) Instruction decode
  - c) Execution
  - d) Writeback
- 122. Which of the following pipeline stages is responsible for performing arithmetic and logic operations?**
- a) Instruction fetch
  - b) Instruction decode
  - c) Execution
  - d) Writeback
- 123. Which of the following pipeline stages is responsible for forwarding data to subsequent pipeline stages?**
- a) Instruction fetch
  - b) Instruction decode
  - c) Execution
  - d) Writeback
- 124. Which of the following pipeline stages is responsible for determining the target address of a branch instruction?**
- a) Instruction fetch
  - b) Instruction decode
  - c) Execution
  - d) Writeback
- 125. What is an interrupt?**
- a) A signal that indicates a program should stop running.
  - b) A signal that indicates a program should start running.
- 126. How many types of interrupts are there?**
- a) 2
  - b) 3
  - c) 4
  - d) 5
- 127. Which of the following is not a type of interrupt?**
- a) Maskable interrupt
  - b) Non-maskable interrupt
  - c) Hardware interrupt
  - d) Software interrupt
- 128. Which type of interrupt cannot be disabled?**
- a) Maskable interrupt
  - b) Non-maskable interrupt
  - c) Hardware interrupt
  - d) Software interrupt
- 129. Which interrupt has the highest priority?**
- a) Non-maskable interrupt
  - b) Maskable interrupt
  - c) Hardware interrupt
  - d) Software interrupt
- 130. Which interrupt is used for urgent tasks?**
- a) Non-maskable interrupt
  - b) Maskable interrupt
  - c) Hardware interrupt
  - d) Software interrupt
- 131. Which interrupt is initiated by the program itself?**
- a) Non-maskable interrupt
  - b) Maskable interrupt

- c) Hardware interrupt
- d) Software interrupt

132. Which interrupt is triggered by an external device?

- a) Non-maskable interrupt
- b) Maskable interrupt
- c) Hardware interrupt
- d) Software interrupt

133. Which of the following statements is true about interrupts?

- a) Interrupts can occur at any time during program execution.
- b) Interrupts can only occur at the beginning of program execution.
- c) Interrupts can only occur at the end of program execution.
- d) None of the above.

134. Which of the following is an example of a hardware interrupt?

- a) Divide-by-zero exception
- b) System call
- c) Input/output interrupt
- d) Floating-point exception

135. What is memory?

- a) A storage device that holds data and instructions for processing.
- b) A device that performs arithmetic and logic operations.
- c) A device that inputs and outputs data.
- d) None of the above.

136. How many types of memory are there?

- a) 2
- b) 3
- c) 4
- d) 5

137. Which type of memory is the fastest?

- a) Cache memory
- b) RAM
- c) ROM
- d) Virtual memory

138. Which type of memory is non-volatile?

- a) Cache memory
- b) RAM
- c) ROM
- d) Virtual memory

139. Which type of memory is used to store the operating system?

- a) Cache memory
- b) RAM
- c) ROM
- d) Virtual memory

140. Which type of memory is used to store frequently used data?

- a) Cache memory
- b) RAM
- c) ROM
- d) Virtual memory

141. Which type of memory is used to store data that is not changed?

- a) Cache memory
- b) RAM
- c) ROM
- d) Virtual memory

142. What is the difference between RAM and ROM?

- a) RAM is non-volatile and ROM is volatile.

- b) RAM is volatile and ROM is non-volatile.
- c) RAM is used for long-term storage and ROM is used for short-term storage.
- d) RAM and ROM are the same thing.

**143. What is virtual memory?**

- a) A type of memory that uses magnetic tape for storage.
- b) A type of memory that expands the available memory by using hard disk space as RAM.
- c) A type of memory that is used to store the operating system.
- d) A type of memory that is used to store frequently used data.

**144. Which type of memory is used for temporary storage during processing?**

- a) Cache memory
- b) RAM
- c) ROM
- d) Virtual memory

**145. Which of the following statements is true about memory?**

- a) Memory is a physical component of a computer.
- b) Memory can only store data and instructions temporarily.
- c) Memory is the same thing as storage.
- d) None of the above

**146. What is the unit of measurement for memory?**

- a) Gigahertz (GHz)
- b) Megabytes (MB)
- c) Kilowatts (KW)
- d) Megahertz (MHz)

**147. Which of the following is a disadvantage of using virtual memory?**

- a) It can increase the amount of available memory.
- b) It can cause the system to slow down due to disk swapping.
- c) It is more expensive than physical memory.
- d) It is less reliable than physical memory.

**148. What is the purpose of a memory controller?**

- a) To perform arithmetic and logic operations on data.
- b) To manage the flow of data between the CPU and memory.
- c) To store frequently used data.
- d) None of the above

**149. Which type of memory is the largest in size?**

- a) Cache memory
- b) RAM
- c) ROM

d) Virtual memory

**150. What is the role of the CPU cache?**

- a) To store frequently used data
- b) To store data that is not changed

- c) To store the operating system.  
d) None of the above.
- 151. Which of the following is an example of secondary memory?**
- a) RAM  
b) ROM  
c) Cache memory  
 d) Hard disk drive
- 152. What is the difference between volatile and non-volatile memory?**
- a) Volatile memory is faster than non-volatile memory.  
 b) Volatile memory loses its data when power is turned off, while non-volatile memory does not.  
c) Volatile memory is used for long-term storage,  
d) None of the above.
- 153. What is RAM in a computer?**
- a) A type of storage device  
b) A type of input device  
c) A type of output device  
d) A type of processing unit
- 154. What is the purpose of cache memory in a computer?**
- a) To store frequently used data for faster access
- b) To store long-term data that doesn't need to be accessed quickly  
c) To store instructions for the CPU  
d) To store data that has already been processed
- 155. Which of the following is an example of non-volatile memory?**
- a) RAM  
b) Cache memory  
 c) Hard disk drive  
d) Register
- 156. What is virtual memory in a computer?**
- a) A type of physical memory  
b) A type of secondary memory  
 c) A technique that allows the operating system to use more memory than is physically available  
d) A type of volatile memory
- 157. What is the purpose of the memory controller in a computer?**
- a) To manage the flow of data between the CPU and memory  
b) To perform arithmetic and logical operations  
c) To manage the input and output devices  
d) To manage the power supply

## **Answer Sheet**