Booth Multiplier

Shirsendu B Acharyya
Department of Microelectronics and
VLSI Design (MTech)
University Of Hyderabad, CASEST,
School Of Physics
Hyderabad, India
22pmmt03@uohyd.ac.in ,
bikasacharyya2405@gmail.com

***Abstract*—This paper primarily discusses about 2 electronics components namely Booth multiplier and a clock pulse generator circuit. The Booth multiplier is an FSM made using Verilog while all other analog parts are made using schematic in eSim platform. Other notable parts in the projects are the input signal stage, output signal stage and all the analog domain in facilitated by Google Skywater 130nm node.**

Keywords—Booth multiplier, Clock pulse generator, FSM, 130nm node, Verilog, Schematic.

I. INTRODUCTION

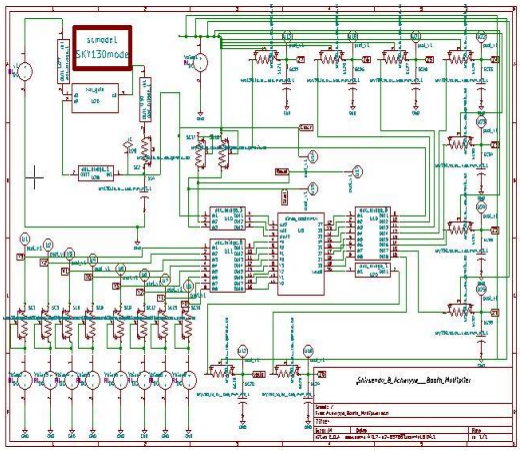
Digital Circuitry – The booth multiplier is an improved multiplier circuit through we can avoid addition whenever consecutive 0's and 1's is detected in multiplier. Basically, we inspect last 2 bit of the multiplier at a time. Now if the bits are same 00 or 11 then right shift the partial product, If the bits are 01 then we do an addition and then shift right. If the bits are 10 then we do a subtraction and then shift right. This process significantly reduces the number of addition and subtraction from the conventional method. It is to be noted that to produce a clock pulse we have used a xor gate which is also a digital component made from Verilog then converting it into spice netlist.

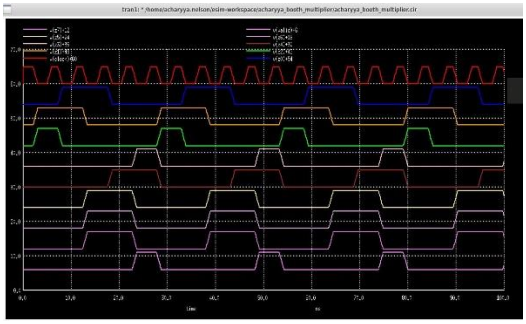
Analog Circuitry - In out circuit the analog circuitry mainly involved the p diffusion resistor and capacitor. The p diffusion capacitor is having 3 terminals where the terminal 1 and 2 goes without circuit terminal and the pin 3 goes to high Vdd connection. All the resistor and capacitor values are put to default values.

Obviously to connect the analog and digital block we will use an ADC and then an DAC bridge. These bridges are not real-life adc and dac but they help to connect the analog and digital signal such that the simulator does not produce any error.

Other notable component in the schematic is the plot_v1 which actually plots the graphical timing wave of a node with respect to ground.

II. IMPLEMENTED CIRCUIT





III. REFETENCE

1. NPTEL Lectures- Hardware Modelling using Verilog by IIT KHARAGPUR
2. https://github.com/replica455/Booth_Multiplier_For_IITB_Hackathon
3. https://www.vsdiat.com/
4. https://www.youtube.com/playlist?list=PLVORbPb_s0PsMlqyqvQ1xm9rP0bq-I6_e
5. https://electronics.stackexchange.com/questions/583958/xor-gate-frequency-generator
6. https://electrobinary.blogspot.com/2020/08/booth-multiplier-verilog-code.html