lpGBT – a User's Perspective

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on behalf of the lpGBT team

Topical Workshop on Electronics for Particle Physics

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lpGBT Team

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Finding Information

- Starting point:
  - www.cern.ch/proj-gbt
    https://espace.cern.ch/GBT-Project/LpGBT/default.aspx

- Specifications:
  - https://espace.cern.ch/GBT-Project/LpGBT/Specifications/LpGbtxSpecifications.pdf

- In this conference:
  - This presentation:
    - https://indico.cern.ch/event/697988/contributions/3075493/

  - Simulation and testing:
    - An UVM-based verification environment for the lpGBT 10 Gbps transceiver ASIC:
      https://indico.cern.ch/event/697988/contributions/3056029/

  - lpGBT-FPGA:
    - Introduction to the lpGBT-FPGA: Introduction to the lpGBT-FPGA:
      https://indico.cern.ch/event/697988/contributions/3141889/attachments/1718898/2774016/Introduction_to_the_LpGBT-FPGA_-_workshop.pptx
    - New LpGBT-FPGA IP: Simulation model and first implementation:
      https://indico.cern.ch/event/697988/contributions/3056073/

LpGBT Project Schedule

- Q1-Q3 2018:
  - Package procurement and engineering completed
  - MPW tapeout 25th July 2018
  - Test system: PCB / Software under production

- Q4 2018
  - Prototypes available (~300 ASICs)
    - Option for additional 300 if all OK

- Q1 – Q3 2019:
  - Prototype functional testing
  - Radiation qualification
  - Production testing development

- Q4 2019:
  - Engineering run

- Q3 2020
  - Engineering ASICs (~40k) available to the users

- Q3 2021:
  - Production completed (~100k ASICs)

lpGBT Link Architecture

High radiation doses

No or small radiation doses

LHC: up to 100 Mrad (10^{14} 1MeV n/cm^2)
HL – LHC: up to 1 Grad (10^{16} 1MeV n/cm^2)

Short distance optical links: 50 to 300 m

Timing & Trigger

TIA

PD

FPGA

Timing & Trigger

DAQ

lpGBT

DAQ

Slow Control

LD

LD

Slow Control

Custom ASICs

On-Detector
Radiation Hard Electronics

Off-Detector
Commercial Off-The-Shelf (COTS)

Electrical links to the frontend
modules. Lengths: *cm* to few *m*

Custom optoelectronics

What's the lpGBT?

- Data <u>transceiver</u> with <u>fixed and "deterministic" latency</u> for both up and down links.
  - Clocks and Data
- Down link:
  - 2.56 Gbps
  - FEC12
  - eLinks:
    - Bandwidth: 80/160/320 Mbps
    - Count: 16/8/4
- Up link:
  - 5.12 Gbps or 10.24 Gbps
  - FEC5 or FEC12
  - eLinks:
    - Data rates: 160 /320 / 640 / 1280 Mbps
    - Count:
      - FEC5
        - Up to 28 @ 160 Mbps
        - Up to 7 @ 1.28 Gbps
      - FEC12
        - Up to 24 @ 160 Mbps
        - Up to 6 @ 1.28 Gbps

Data rate: 160 Mbps to 1.28 Gbps
Length: cm to meters

Data rate:
  Rx: 2.56 Gbps
  Tx: 5.12 and 10.24 Gbps
Length: <200 m

Data rate: 5 - 10 Gbps
Length: few cm
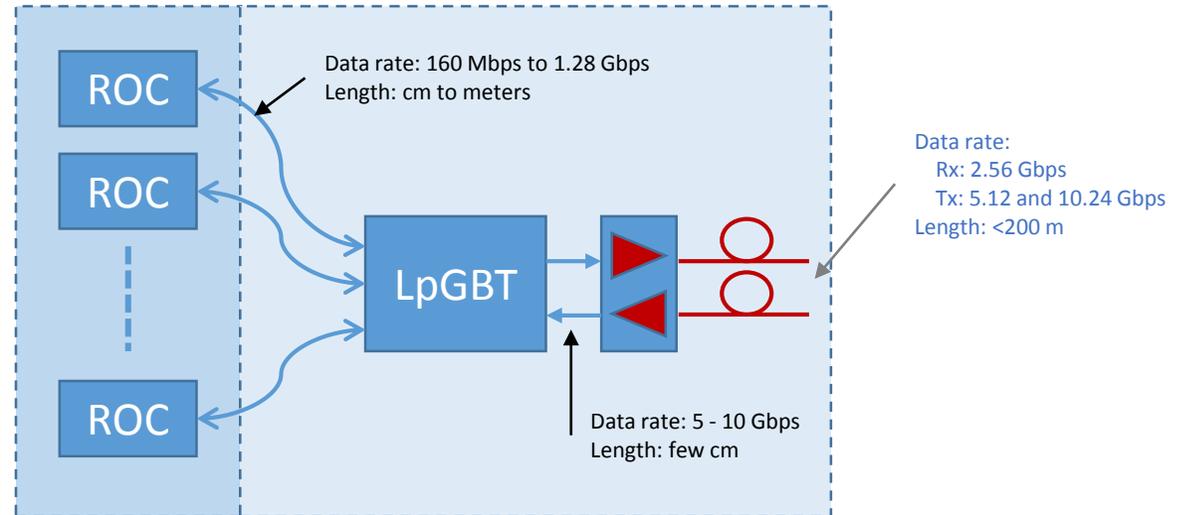
- Experiment control/monitoring functions:
  - 10-bit ADC
  - 12-bit voltage DAC
  - 8-bit current DAC
  - Temperature sensor
  - Three I2C masters
 - Programmable parallel port: 16 x GPIO
- Package:
  - 9 mm x 9 mm x 1.25 mm (pitch: 0.5 mm)
 - Pin count: 289 (17 x 17)

Radiation Environment

- The lpGBT is designed in 65 nm CMOS process

- Targets [no only] the innermost layers of the HL-LHC detectors:
  - Total Ionizing Dose (TID):
    - 200 Mrad
  - Non Ionizing Energy Loss (NIEL) radiation:
    - ~ 10^{15} 1 MeV n_{eq}/cm^2 (mainly a concern for the optoelectronics components)
  - [Over a 10 years lifetime]

- Operation robust to Single Events Upsets:
  - Triple Modular Redundancy (TMR) used in the State Machines and the "low-frequency" section of the Data Path
  - Forward Error Correction used in the "high-frequency" section of the data path and over the optical links
  - New LC-VCO architecture for increased SEU-Tolerance and low jitter.

LpGBT System Block Diagram (Simplified)

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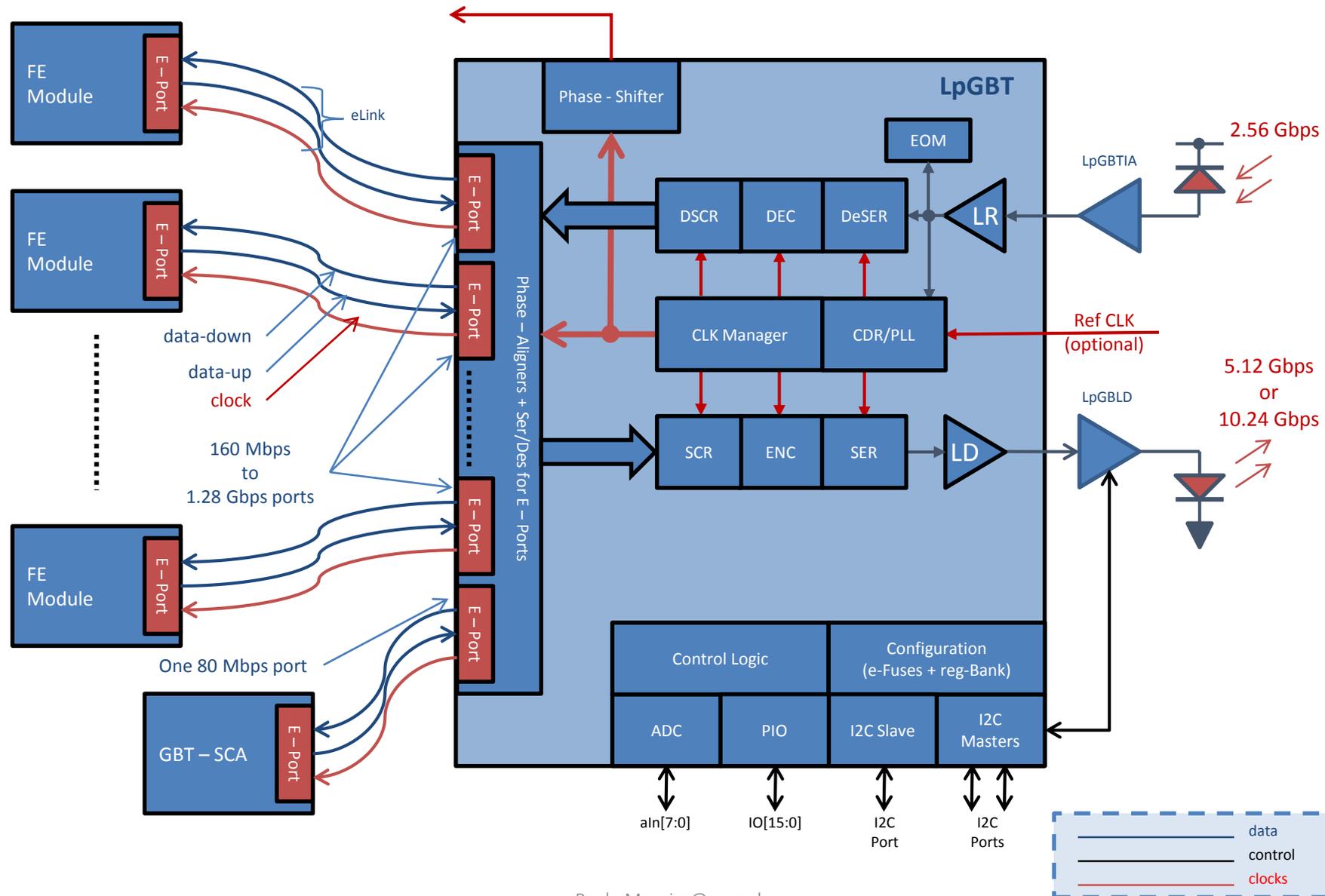
# Configuration
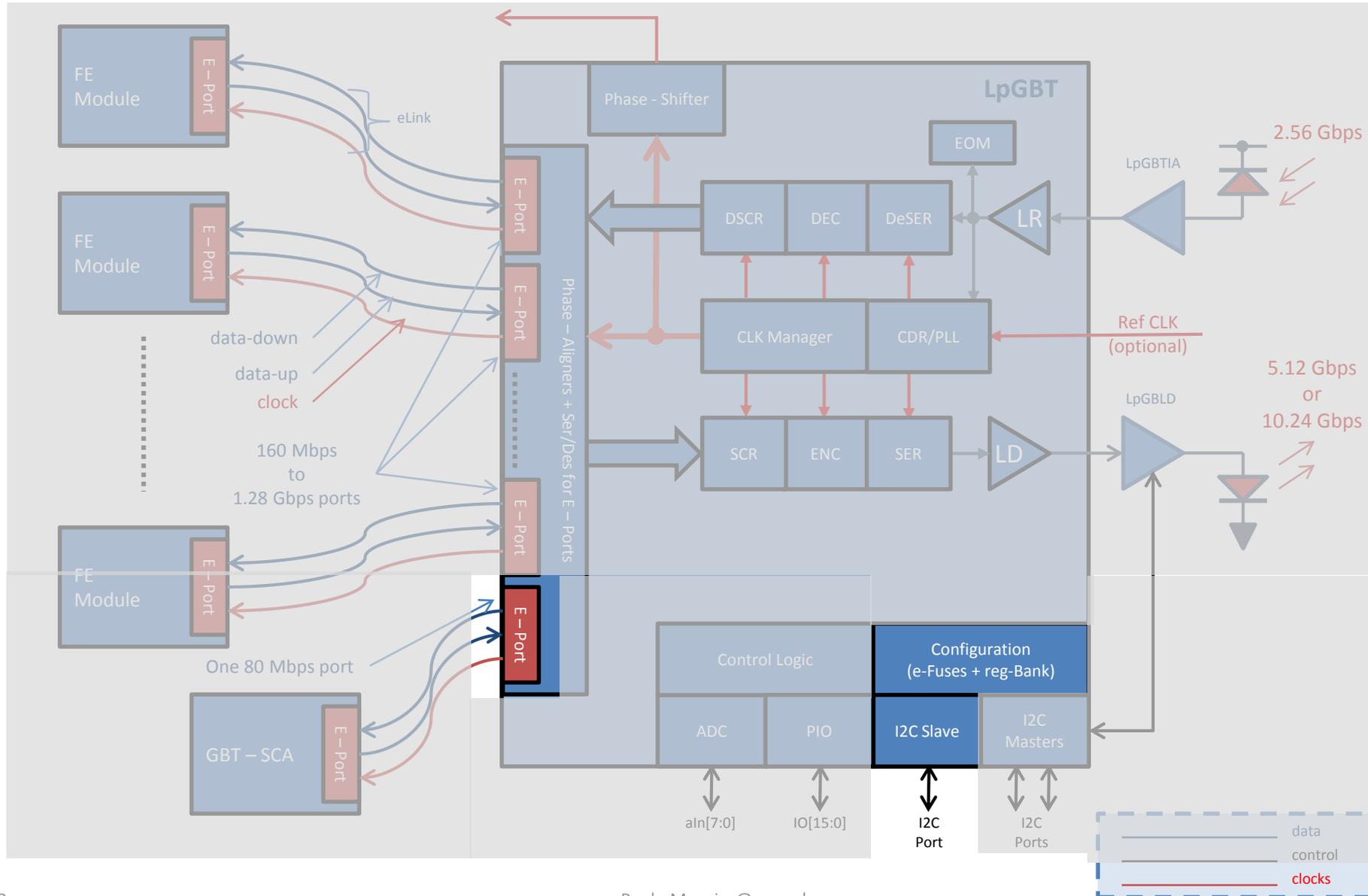
Programming the lpGBT (1/2)

- The lpGBT is a highly flexible device:
  - Transceiver modes / Locking modes / Uplink data rate / FEC coding / Clock frequencies / Clock phases / Number of active eLinks / Phase-aligner modes / Pre-emphasis / Equalization / Driving strengths / … / …

- It won't simply work by just having it installed in your system…!

- <u>It needs to be configured</u>!

- There are:
  - 11 configuration pins to be "hardwired";
  - 320 registers to be programed (240 R/W/F + 80 R/W + 142 R (status));

- Configuration pins define the "basic" operation mode;

- Configuration registers "customize" for the user application:
  - Some of them also affect the basic operation (e.g. PLLs, DLLs, startup procedure, etc.);

Programming the lpGBT (2/2)

- Several options are available to read / write the configuration registers:
  - I2C port, allways possible;
  - IC channel, only possible in Transceiver mode;
  - EC port, only possible in simplex TX or RX modes;
  - Access mode <u>needs</u> to be configured [pin "SC_I2C"].
- Optionally, the user's configuration can be "burned into" the ASIC on a bank of "eFuses" and copied at startup into the configuration registers
 - Requires additional 2.5 V supply voltage during the programming cycle.
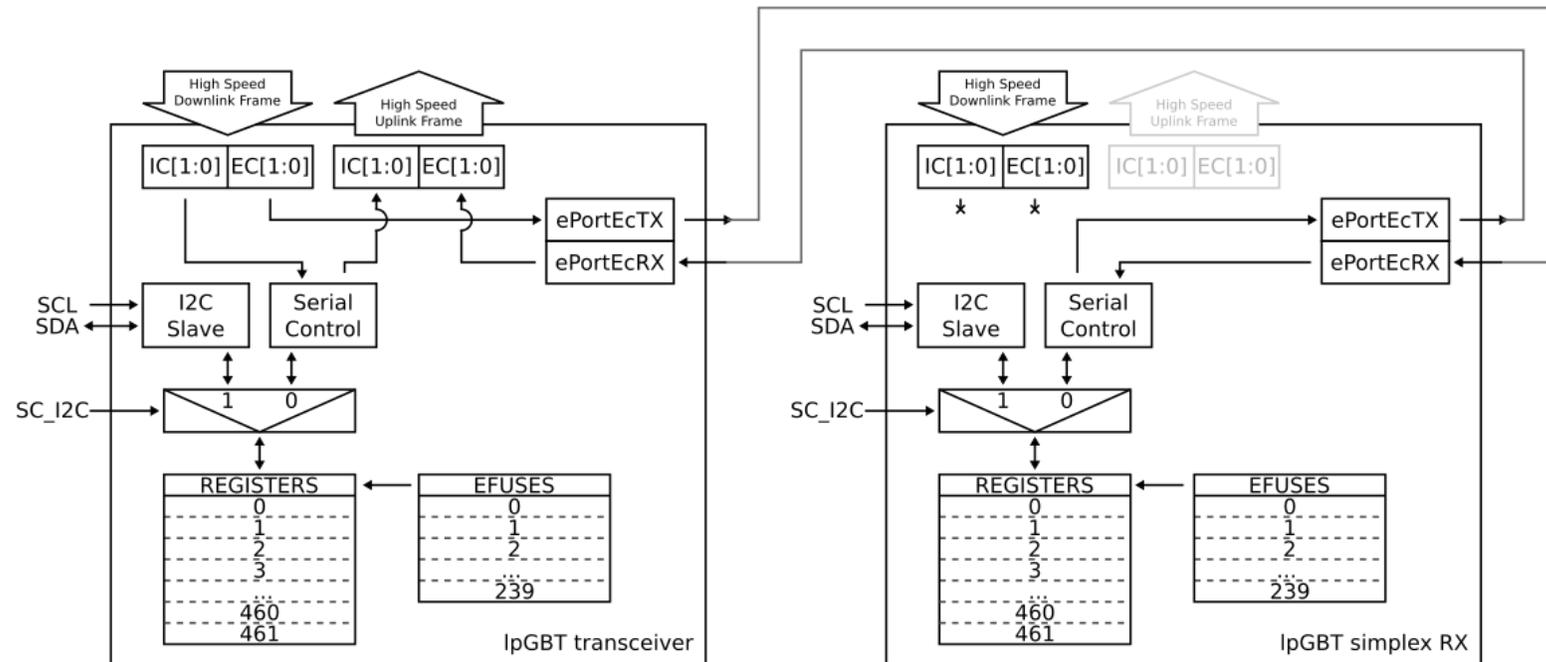
Electrically Interfacing with the Frontends
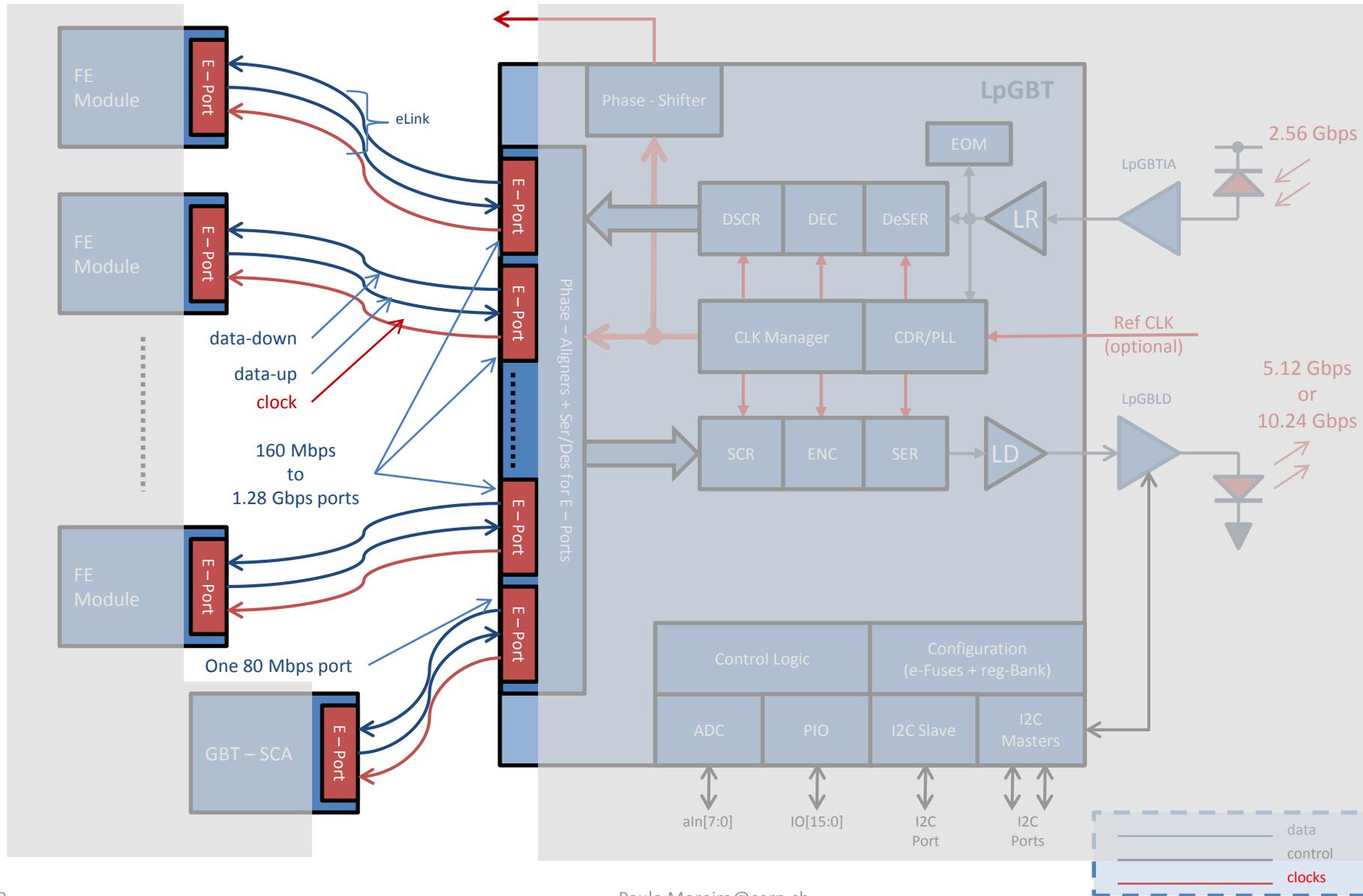
eLinks Electrical "Standard"

- CLPS "CERN Low Power Signalling"
  - [This should] avoid any confusion with LVDS or SLVS;

- Link type:
  - Point – to – point
  - Multi – drop transmitter

- Max data rate:
  - 1.28 Gbps (NRZ)

- Max clock frequency:
  - 1.28 GHz

- Programmable signalling level:
  - 100 mV to 400 mV (single-ended PP amplitude)
  - 200 mV to 800 mV (differential PP amplitude)

- Common mode voltage:
 - 600 mV (nominal)

- Load impedance:
  - 100 Ω

➢ Single-ended PP amplitude:
  - $max(V_{out}+) - min(V_{out}+)$
➢ Differential PP amplitude:
  - $max(V_{out}+ - V_{out}-) - min(V_{out}+ - V_{out}-)$

100 Ω transmission line, twisted pair, etc.

Termination load close to the last receiver in the transmission line

Common mode in the middle of the supply (Vdd/2) for best tolerance to ground fluctuations between modules;
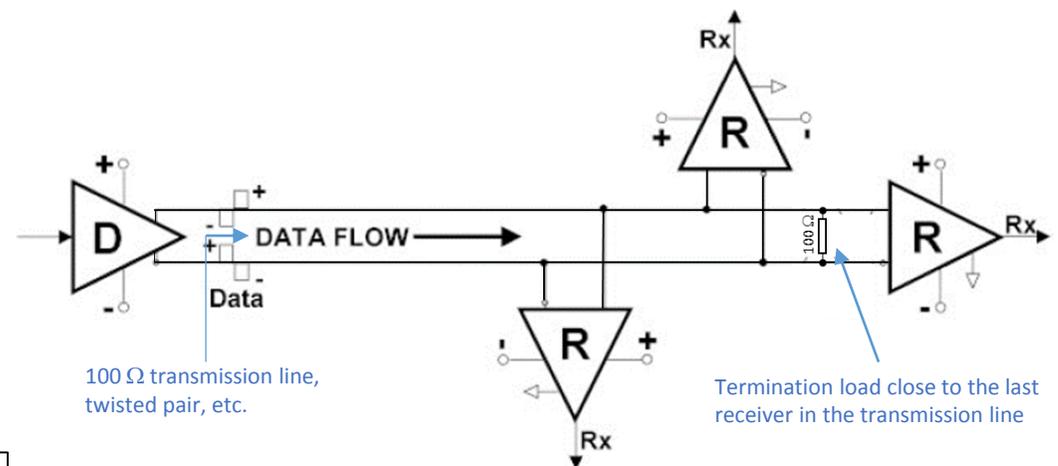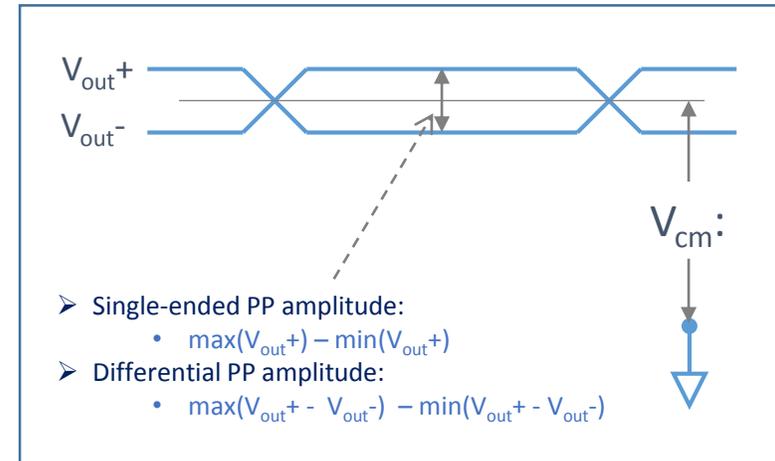
eLink Line Receiver (eRx)

Off chip capacitors if AC coupling needed!

Remember: AC coupling introduces a zero at $f = 1/(2\pi \times Cc \times 100 \ \Omega)$ reducing the number of consecutive zero and ones that can be sent over the line reliably (DC base wander).
An external termination can be used to improve this but will certainly complicate your layout.

Macro cell, available for front-end designers (upon request)

C_c

C_c

in+

in-

100 Ω

V_{CM}

Rail-to-Rail Receiver

invertData

enableTermination

eq[1:0]

setCommonMode

enableRx
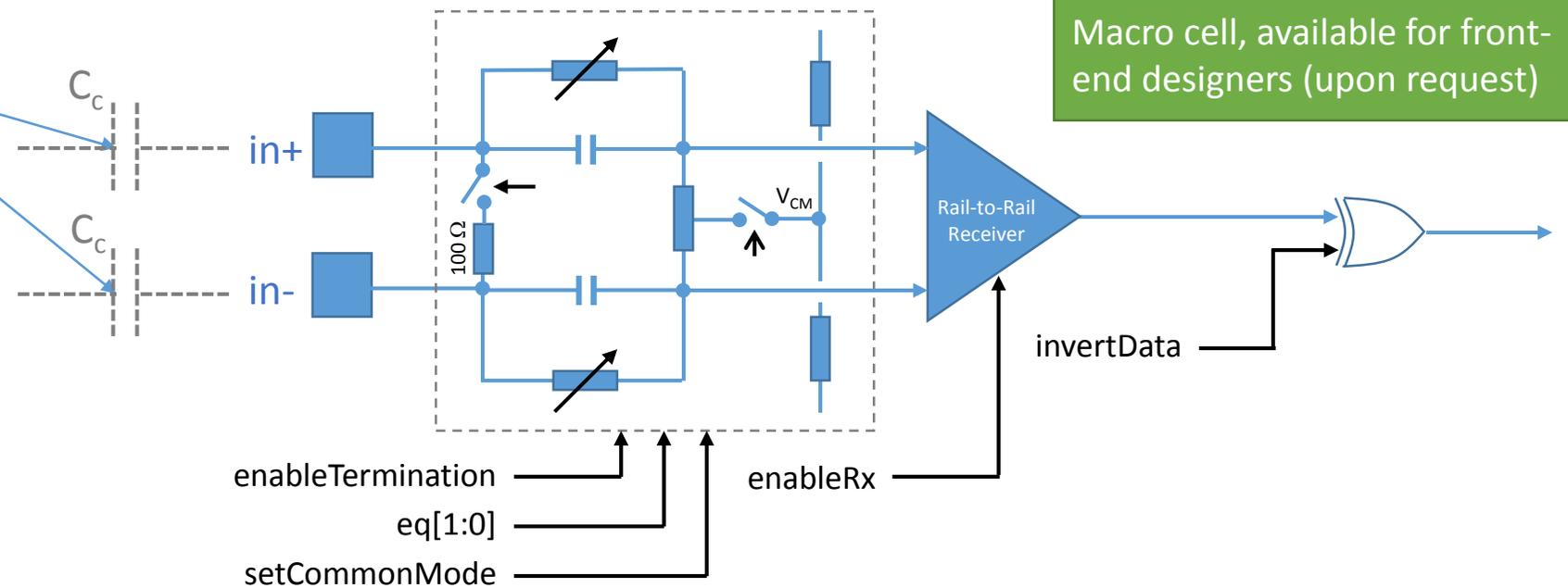
- **Specs**
  - Data rate:
    - Up to 1.28 Gbps
  - Common mode voltage range:
    - 70 mV – 1.13V
  - Differential input voltage:
    - 140 mV – 450 mV

- **Programmable**
  - ON/OFF receiver (for power saving)
  - Data polarity (to simplify routing)
  - ON/OFF termination (100 Ω)
  - ON/OFF common mode setting (for AC coupling, $V_{dd}/2$)
  - Programmable equalization:
    - Optimized for cables with bandwidths of "infinite" (equalization off), 448, 299 and 224 MHz

eLink Data Sampling and "Deserialization"

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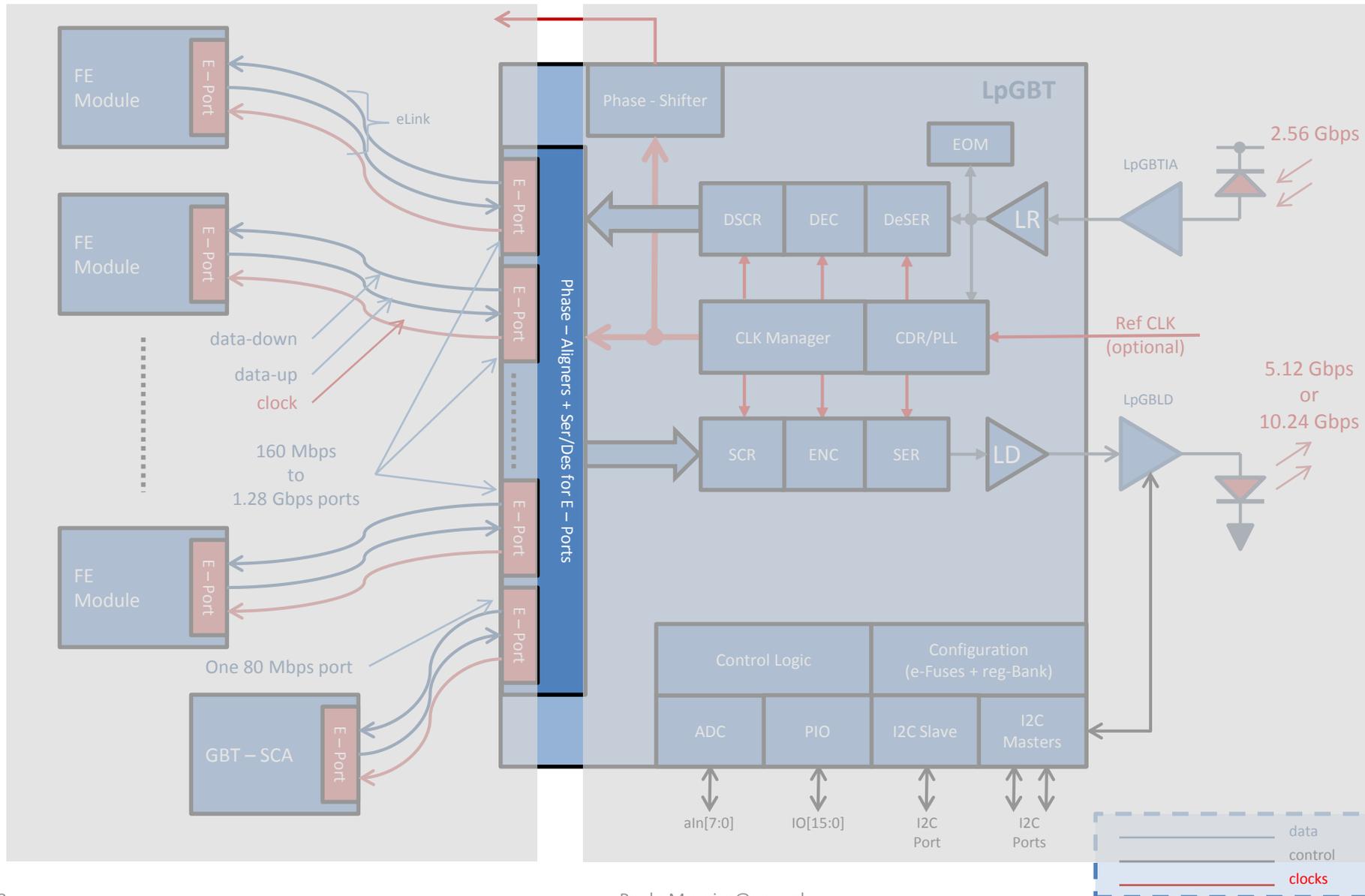
Up eLink – Phase Alignment

Clock (explicitly) provided to the front-end by an eLink clock.

Phase relationship between the received data and the internal clock unknown!

Clock embedded in the data, CDR needed at the front-end

CDR circuit in the frontend ASIC

FE – ASIC

E – Port

Phase – Aligners + Ser/Des for E – Ports

LpGBT

Good sampling instants

eLink "i"

LpGBT internal clock

Bad sampling instants
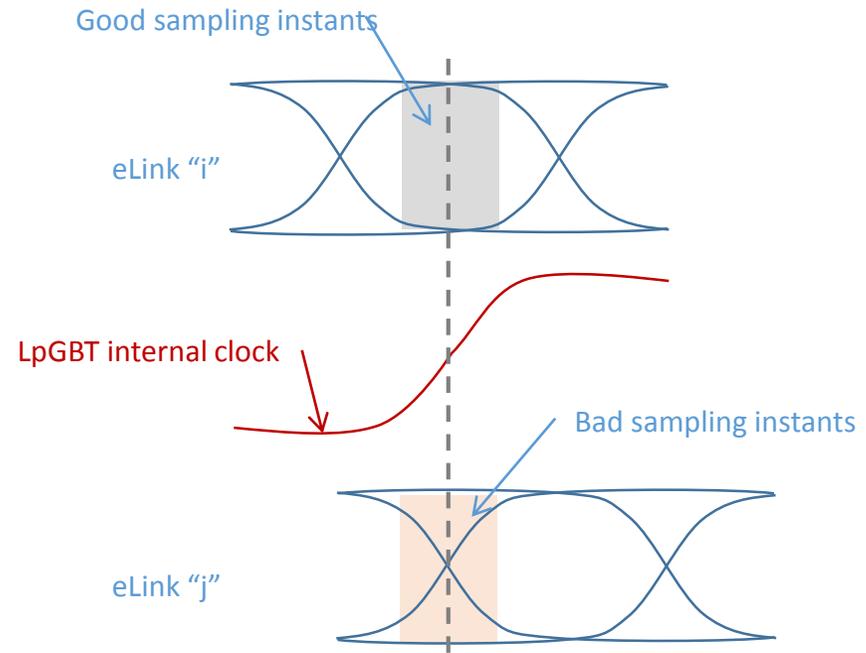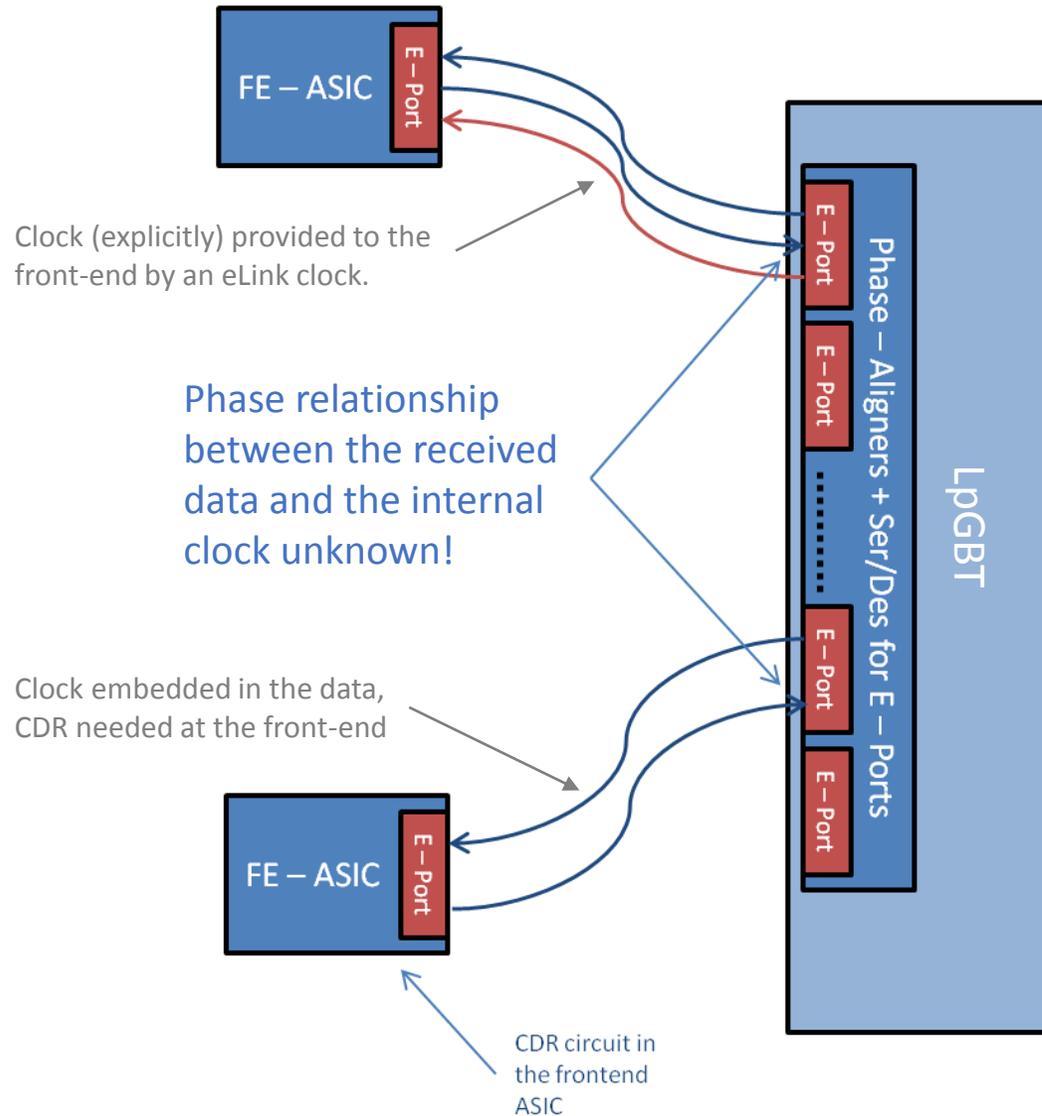
eLink "j"

- The phase of the incoming data signals is "unknown" in relation to the internal sampling clock!
- There are up to 28 eLinks inputs (potentially) all with random phase offsets
- The solution:
  - "Measure" the phase offset of each eLink input
  - Delay individually each incoming bit stream to phase align it with the internal sampling clock

Phase-Aligner Block Diagram

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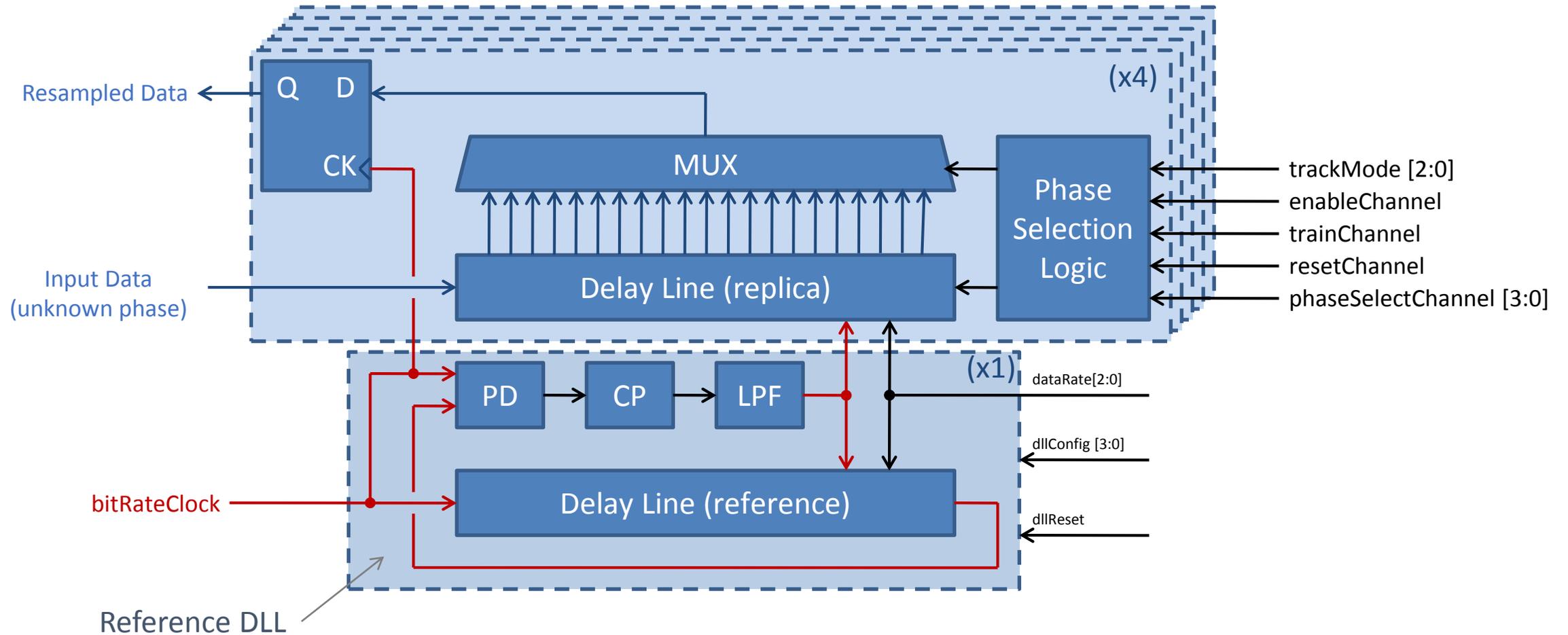
Phase - Selection

Automatic, semi-automatic or or user driven procedures:

1. "Examine" all the eLink phases

2. Detect where the data "edges" are in relation to the clock;

3. Choose the phase that has the edges better centred around the clock

4. In automatic mode:
   - Once aligned, the PA can track the data phase wanders that cover virtually a full clock cycle:
   - To allow for this, the delay line covers more than one bit period: $1.75 \times T_{bit}$
   - And, during initialization only phases 4 to 11 are allowed
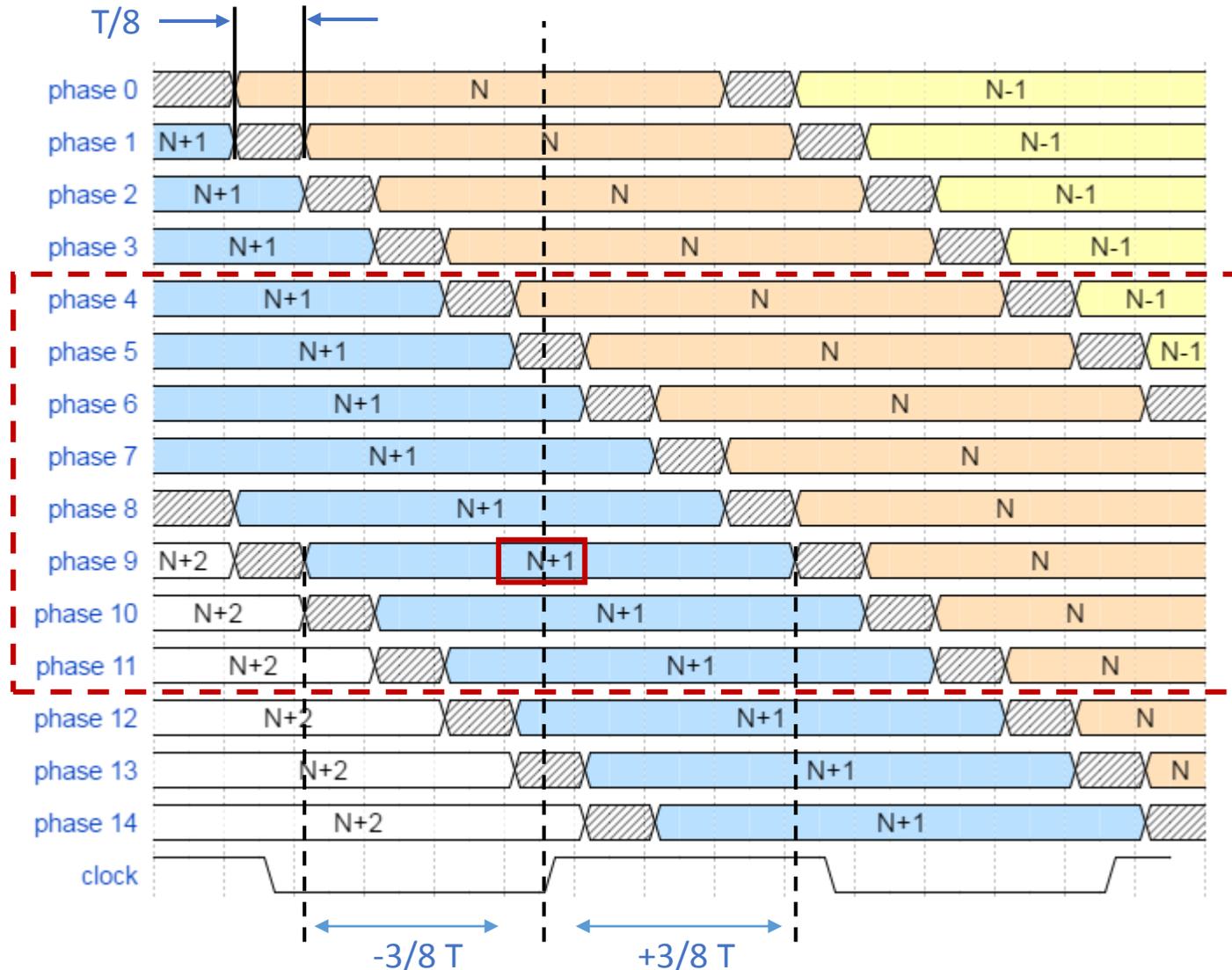
Using the Phase-Aligner(s)

- There are 8 phase-aligners in the lpGBT:
  - 7 serve 28 data eLinks;
  - 1 serves the EC eLink.

- A phase-aligner serves 4 eLink channels:
  - Called an eLink Group.

- The four channels in a Group share a calibration DLL;

- User must setup:
  - The calibration DLL
  - The individual phase-aligner channels corresponding to the eLinks in use.

Phase Aligner Check list:

- Set the group data rate;
  - This sets the maximum number of eLinks per group (see next slides);

- Configure the DLL parameters;

- Reset the DLL;

- Set the phase alignment mode:
  - Static phase selection:
    - User intervention needed.
  - Initial training with learned static phase selection:
    - User intervention needed
  - Automatic phase tracking;

- Enable and reset the channels in use;

eLink Rx Groups

- eLinks are "clustered" in groups of 4:
  - Simply called groups.
- The number of available groups is determined by the FEC uplink code in use;
- The number of available eLinks within a group is determined by the Group data rate;
- The possible data rates depend on the uplink bandwidth (5.12 or 10.24 Gbps)
- The data rate of each group can be set independently:
  - A couple of [over complicated] examples:
    - uplink 5.12 Gbps & FEC12: 8 eLinks x 160 Mbps + 4 eLinks x 320 Mbps + 2 eLinks x 640 Mbps
    - uplink 10.24 Gbps & FEC5: 8 eLinks x 320 Mbps + 4 eLinks x 640 Mbps + 3 eLinks x 1.28 Gbps

Input eLinks (uplink)											
uplink bandwidth [Gbps]	5.12						10.24				
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mbps]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

Note about eLink Input Pin Names

Input to the lpGBT

eLink

Group number: 0, 1,... 6 (there are 7 groups)

EDINGCP

Pin Polarity: P – Positive, N – Negative
(Remember: polarity can be inverted
at the output of the corresponding eRx)

Data

Channel number within a group: 0, 1, 2 or 3 (there
are 4 eLinks associated with every group)
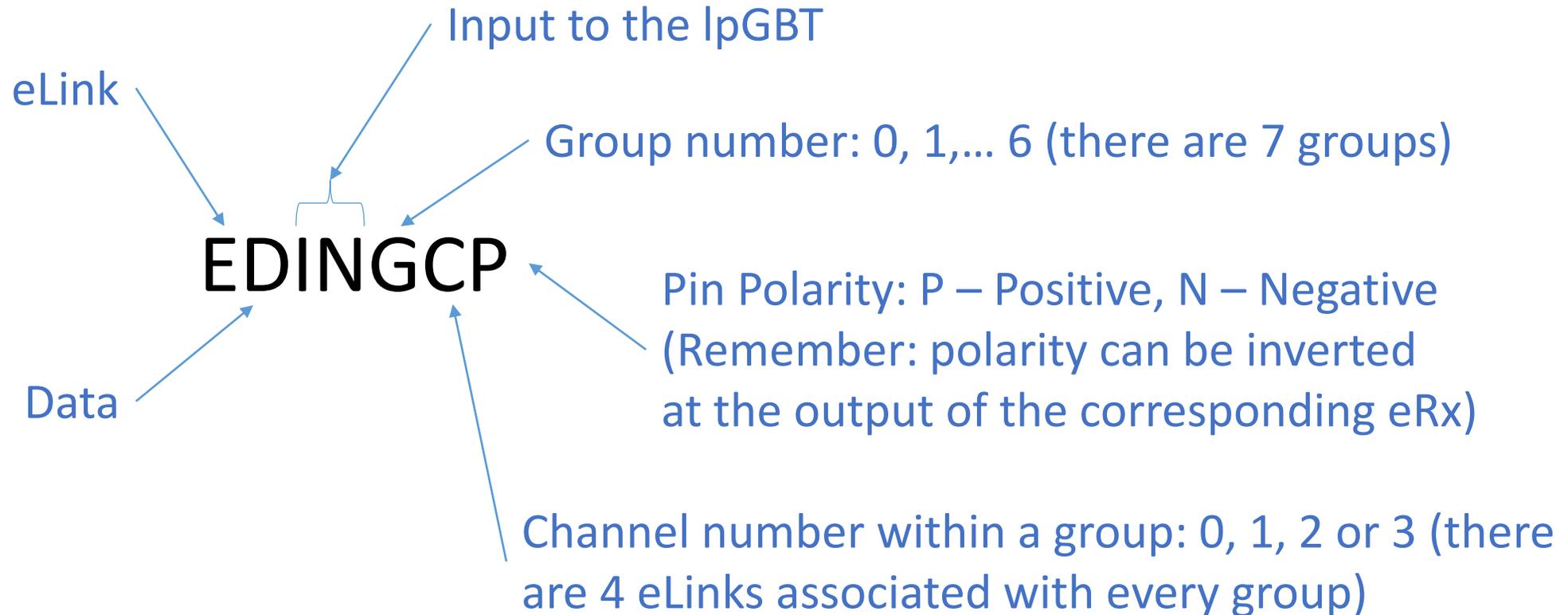
Example: EDIN32N – eLink data input group 3 channel 2 negative polarity pin

The EC "Group"

- The EC "group" is a special case!

- It is composed of a single eLink!

- It only works at 80 Mbps!

- EC channel eLink Functionality is only available in Transceiver mode;

- In transceiver mode it is always available independently of the other Groups activity;

- Its mission is to implement an "experiment control" link, however it can be used as a general purpose link;

- [As seen before, this input can be used to control the ASIC in the simplex modes (TX / RX) but not in transceiver mode]

- Pins:
  - EDINECP (eLink Data In EC channel Positive pin)
  - EDINECN (eLink Data In EC channel Negative pin)

eLink Deserialization

- eLink inputs receive serial data from the frontend devices;
- These data is de-serialized and inserted in the uplink frame to be transmitted to the counting room (more on this soon):
  - The frame is processed in parallel in the chip before it is itself serialized for uplink transmission.
- In the case of transmission at 5.12 Gbps an eLink Group is always associated with the same 16-bits in the frame, the **group bits**.
- The same is true for 10.24 Gbps but in this case the group bits are 32 (the uplink frame is twice as long)
- The user knows from the position of the bits in the frame from which eLink group the data belongs to!
- Moreover, depending on the data rate, a specific eLink is identified by the position of the corresponding bits within the "group bits" (or simply, the position within the frame).
- After the eLinks input data is de-serialized, scrambling, FEC coding, interleaving header insertion and high-speed serialization takes place in the uplink data path...

Uplink Data Path

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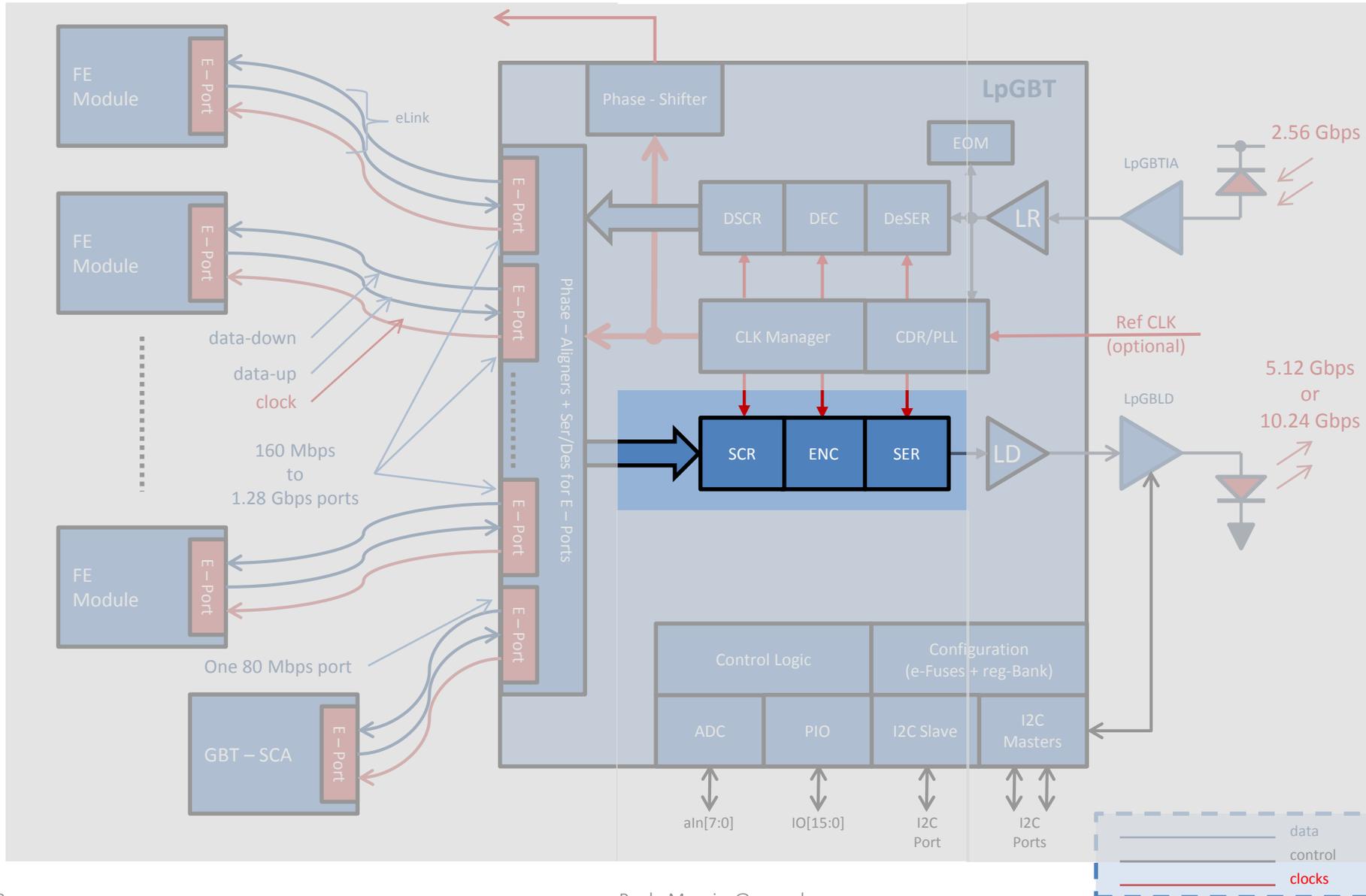
High – Speed Uplink Frame

- **The LpGBT supports the following uplink data rates:**
  - 5.12 / 10.24 Gbps
- **Data is transmitted as a frame composed of:**
  - Header
  - The data field
  - A forward error correction field: FEC5 / FEC12
- **The data field is scrambled to allow for CDR operation at no [additional] bandwidth penalty**
- **Efficiency = # data bits/# frame bits**

Data
(User data payload)

| H | Message | FEC |

Header
(Delimits the frame boundaries)

Forward Error Correction
(Allows to correct transmission errors)
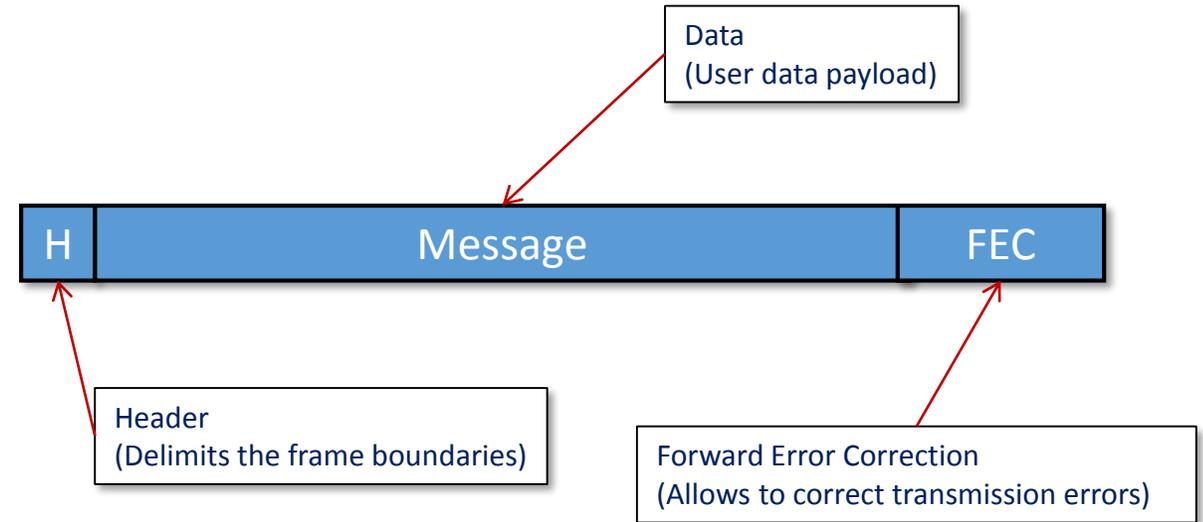
	uplink			
	5.12 Gbps		**10.24 Gbps**	
	FEC5	**FEC12**	**FEC5**	**FEC12**
Frame [bits]	128		256	
Header [bits]	2		2	
Data [bits]	116	102	232	204
FEC [bits]	10	24	20	48
Correction [bits]	5	12	10	24
Efficiency	91%	80%	91%	80%

Example: 5.12 Gbps FEC5 Uplink Frame
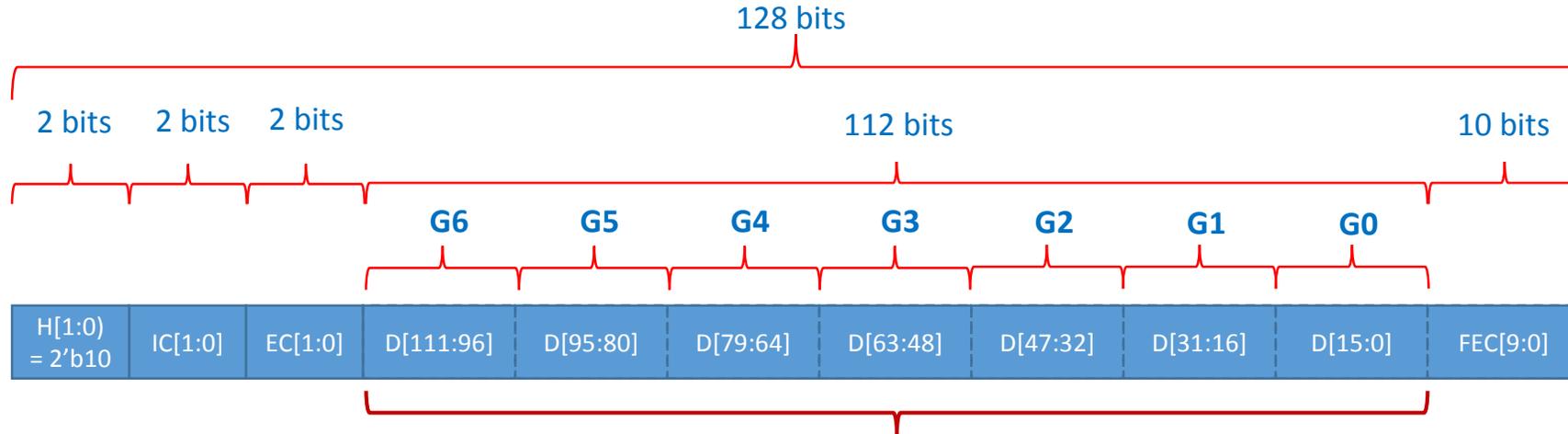
Frame	Function	I/O Group
FRMUP[9:0]	FEC[9:0]	
FRMUP[25:10]	Data[15:0]	0
FRMUP[41:26]	Data[31:16]	1
FRMUP[57:42]	Data[47:32]	2
FRMUP[73:58]	Data[63:48]	3
FRMUP[89:74]	Data[79:64]	4
FRMUP[105:90]	Data[95:80]	5
FRMUP[121:106]	Data[111:96]	6
FRMUP[123:122]	EC[1:0]	EC
FRMUP[125:124]	IC[1:0]	
FRMUP[127:126]	H[1:0] = 2'b10	HFH[1:0] = 2'b10

7 groups of 4 input e-Ports
Number of data ports:
- 28 eLinks @ 160 Mbps
- 14 eLinks @ 320 Mbps
- 7 eLinks @ 640 Mbps

Note: This is how you will see the uplink frame after it has been processed by the lpGBT-FPGA receiver but not how it is actually transmitted by the lpGBT …

Uplink data path

data[N:0] → Scrambler → Interleaving → Serializer → serialData

FEC Coding

header
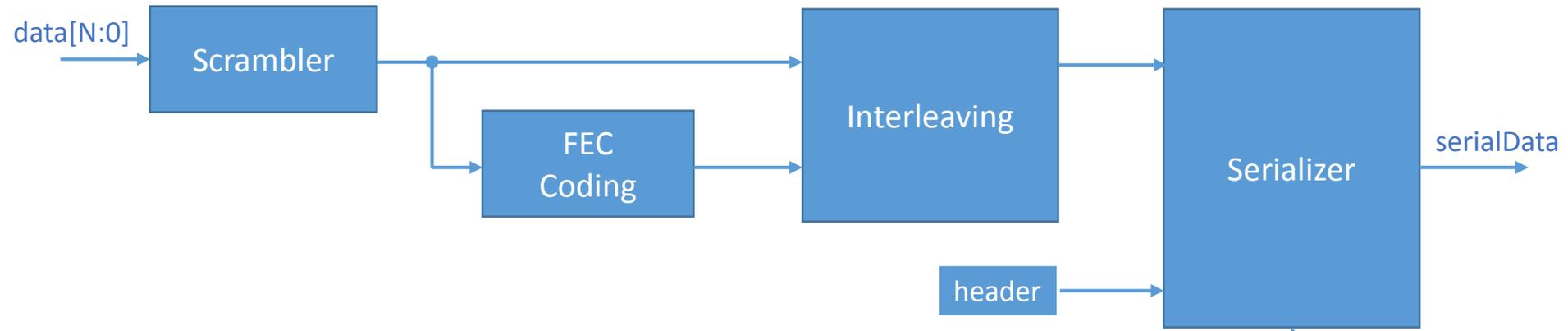
The order of operations is important

128-to-1 @ 5.12 Gbps
Or
512-to-1 @ 10.24 Gbps

We avoid the details here since you will not have to worry with them, they will be "handled" by lpGBT-FPGA

High-Speed Line Driver

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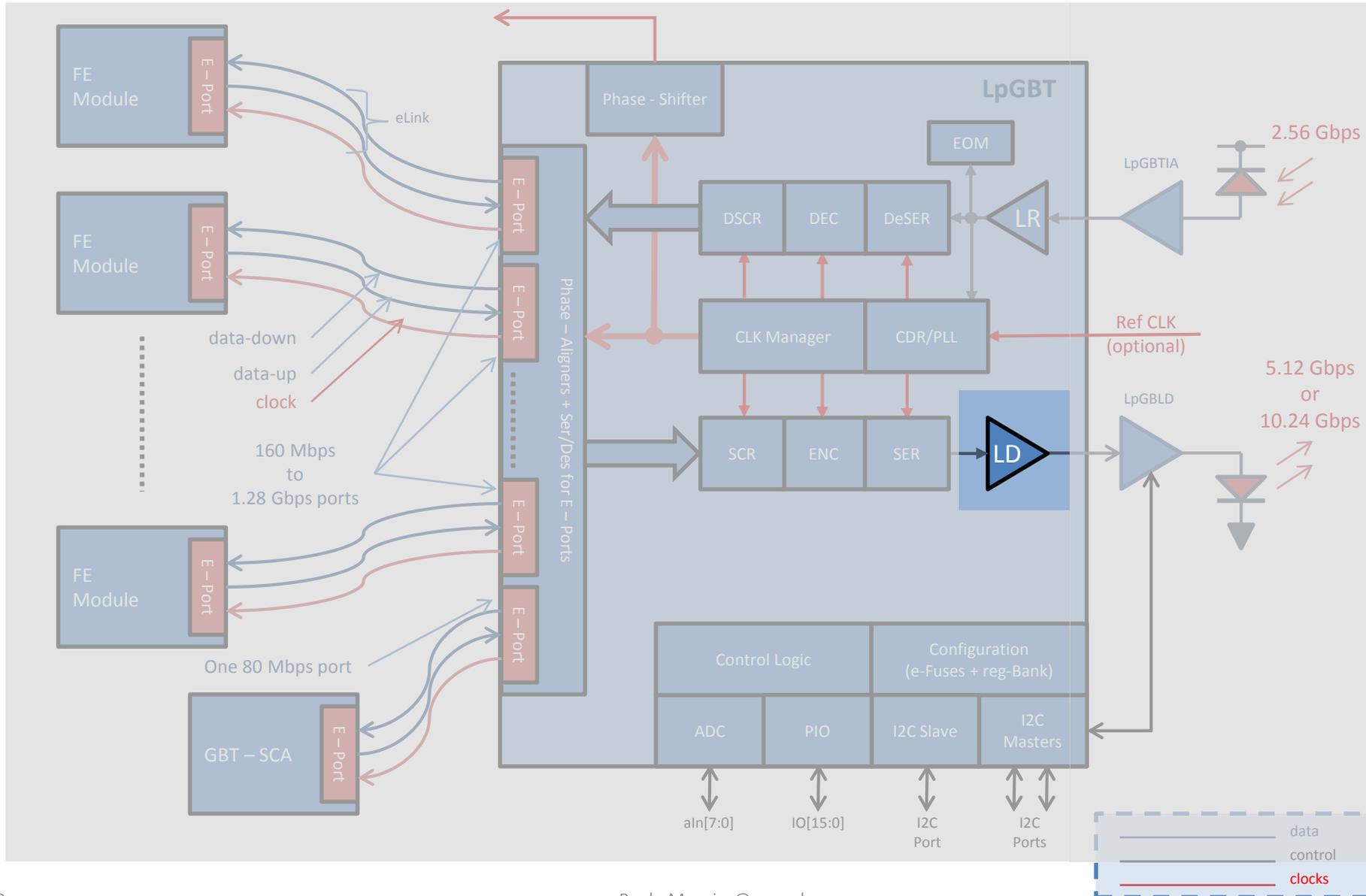
Line – Driver Topology
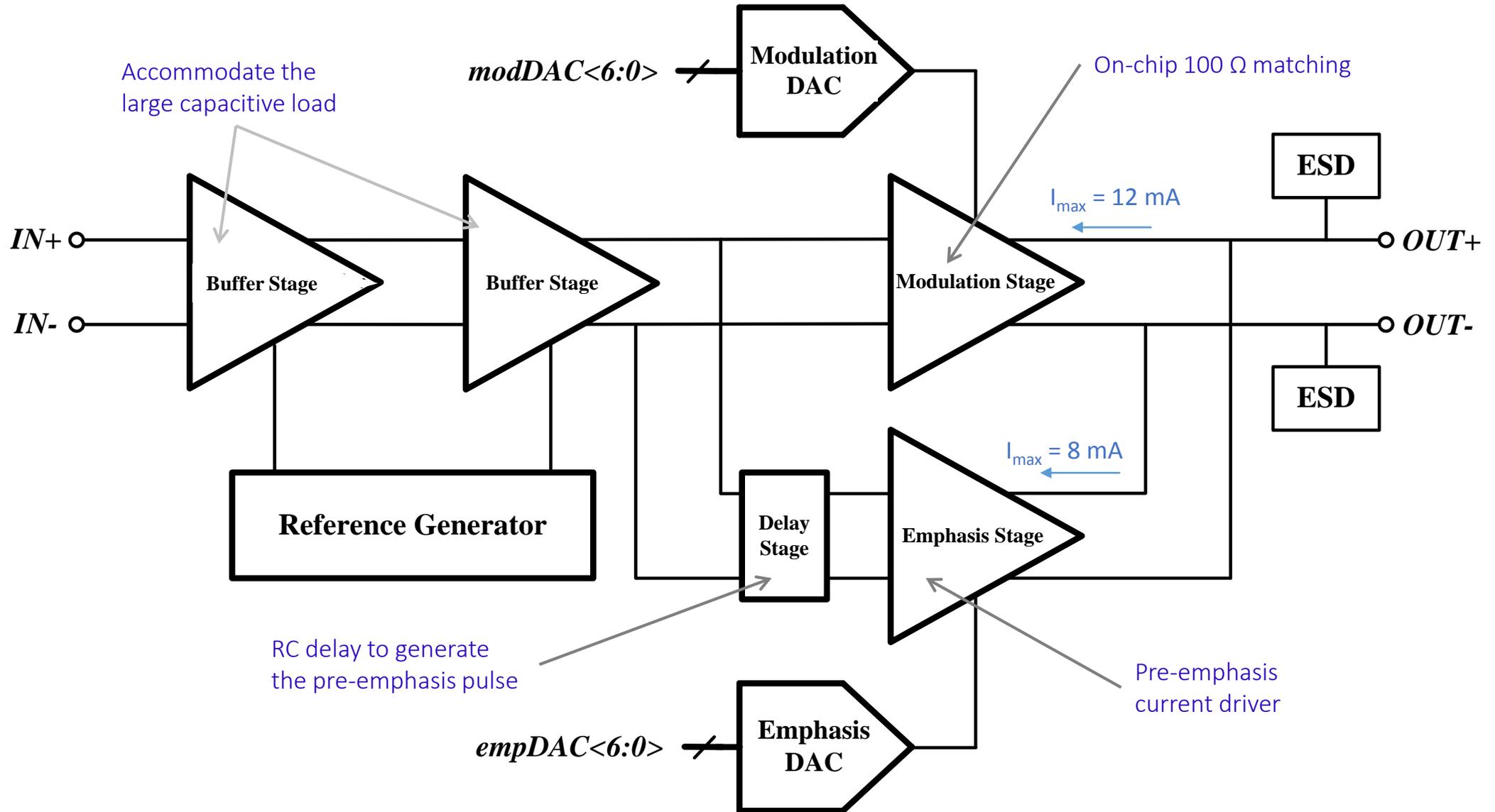
Line driver simulations (@5.12Gbps)

$I_{cc} = 40$ mA
$I_{mod} = 12$ mA
$I_{pre} = 8$ mA
$C_{out} = 500$ fF
Process: SS_100C_1.2V
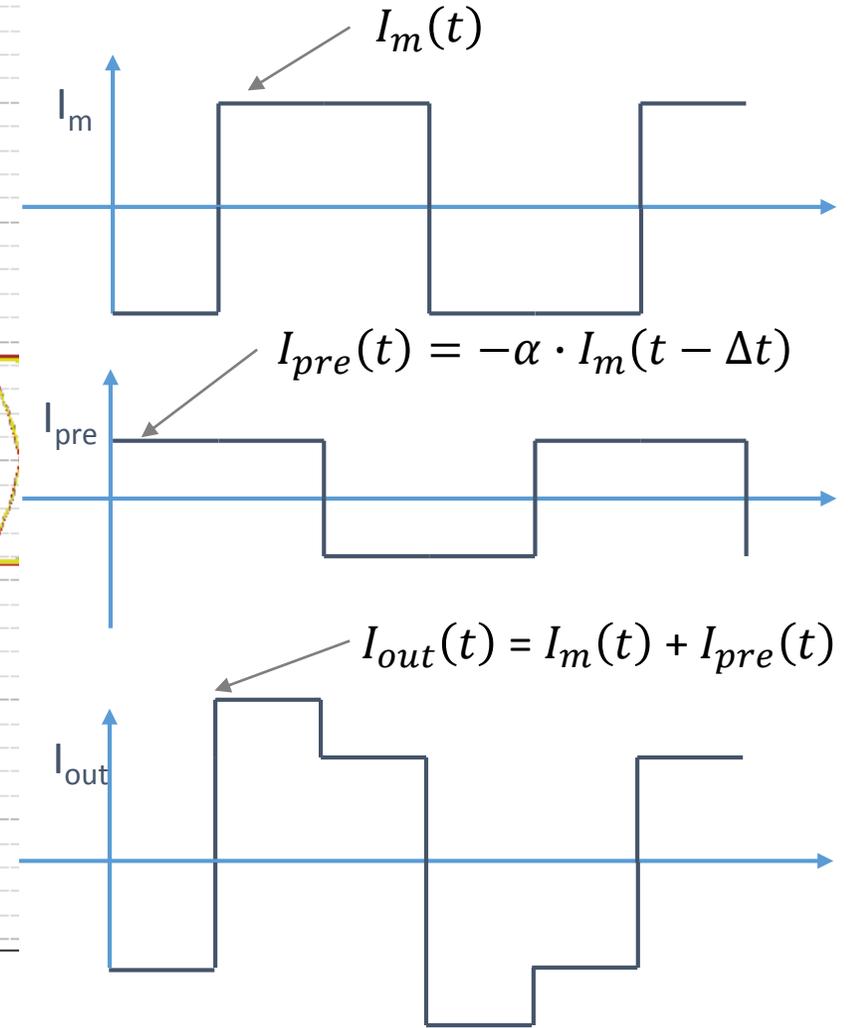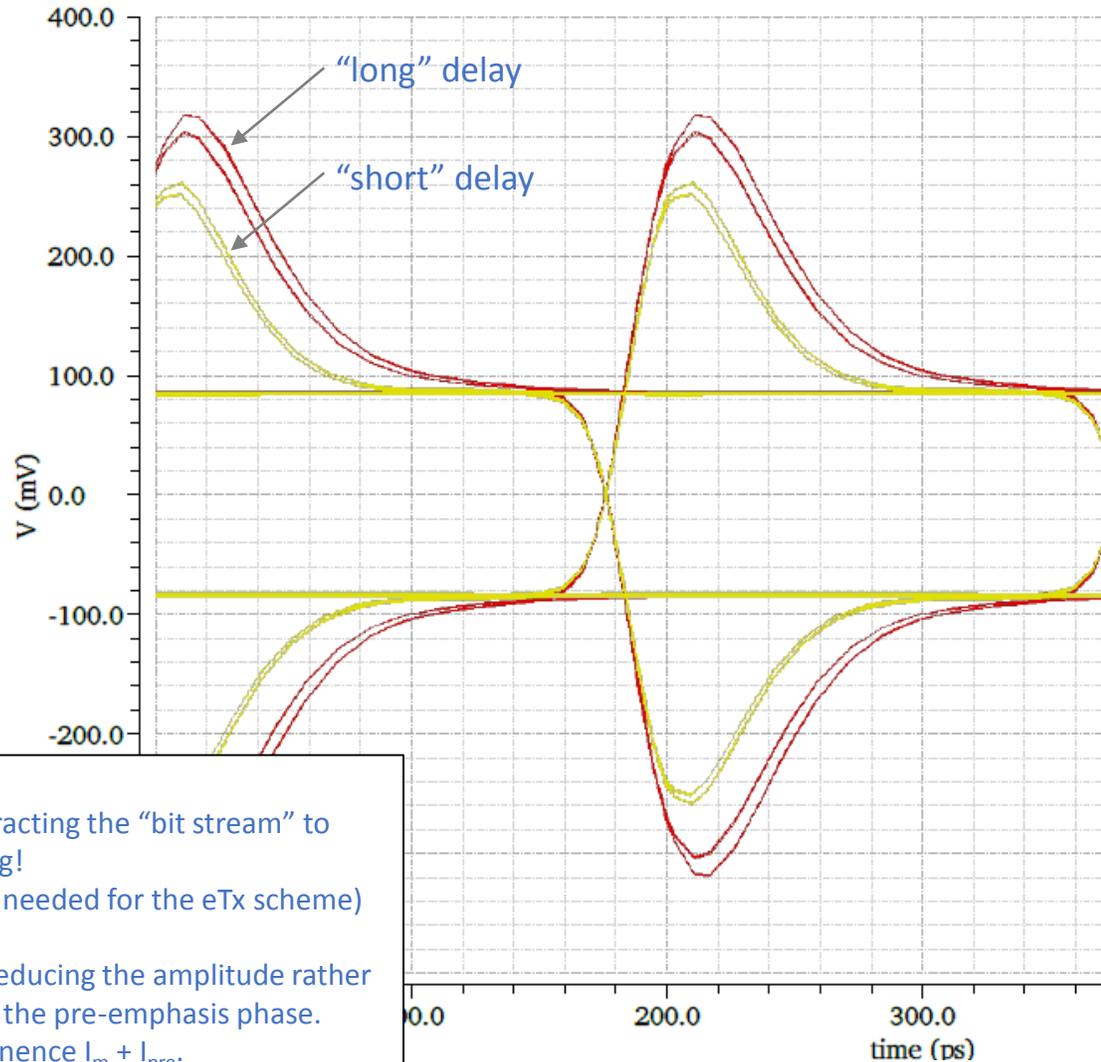
Advantage:
- Pre-emphasis is made by subtracting the "bit stream" to itself after inversion and scaling!
- No narrow pulses required (as needed for the eTx scheme)

Disadvantage:
- The pre-emphasis is done by reducing the amplitude rather than peaking the signal during the pre-emphasis phase.
- The driver consumes in permanence $I_m + I_{pre}$.

$I_m(t)$

$I_{pre}(t) = -\alpha \cdot I_m(t - \Delta t)$

$I_{out}(t) = I_m(t) + I_{pre}(t)$

High-Speed Line Receiver / Equalizer

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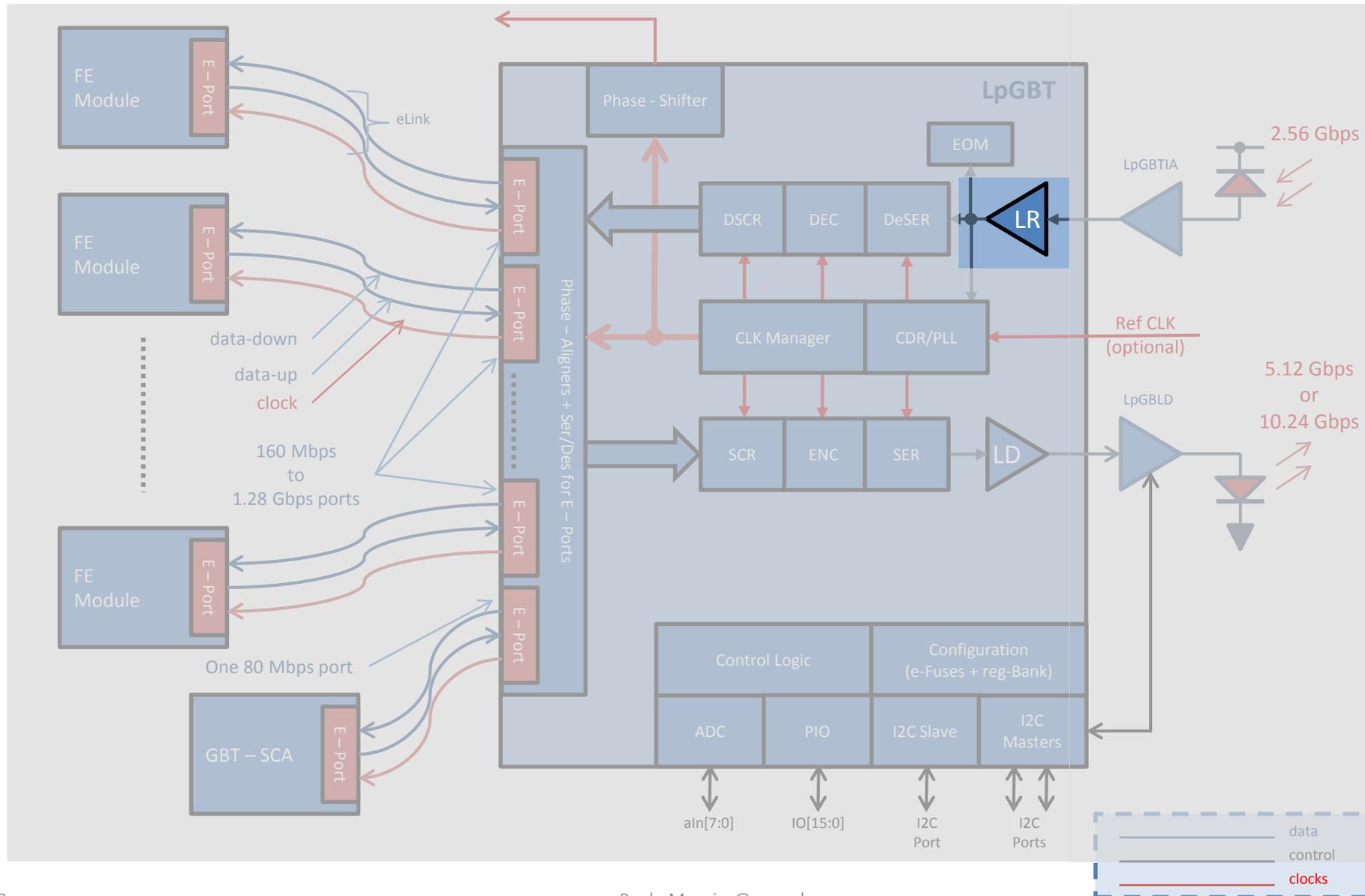
The Equalizer in the LpGBT

Att   CTLE0   CTLE1   CTLE2   CTLE3   Buffer
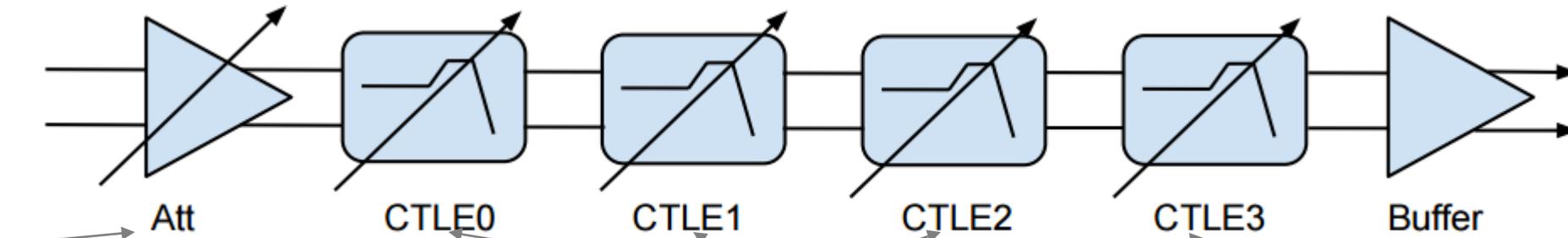
Passive attenuator: allows
to handle signals as high as 1 V
Attenuation: 0, -3.5 and -9.5 dB

Four equalizing stages allow
to flexibly control the shape
of the transfer function.

- To be used in case of "low bandwidth" downlink
  - "Bypassed" by default.
- If needed, user programs the positions of the zeros of the four CTLE stages (and the 1st stage attenuation)
- It is an iterative process in a "case-by-case" basis

75 cm of Low Bandwidth Coaxial Cable
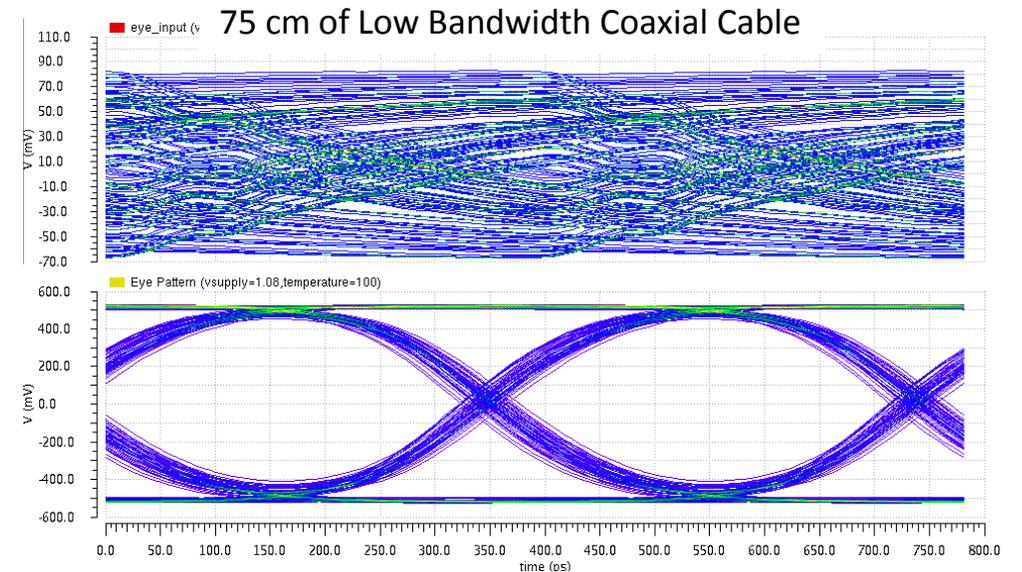
Eye Opening Monitor
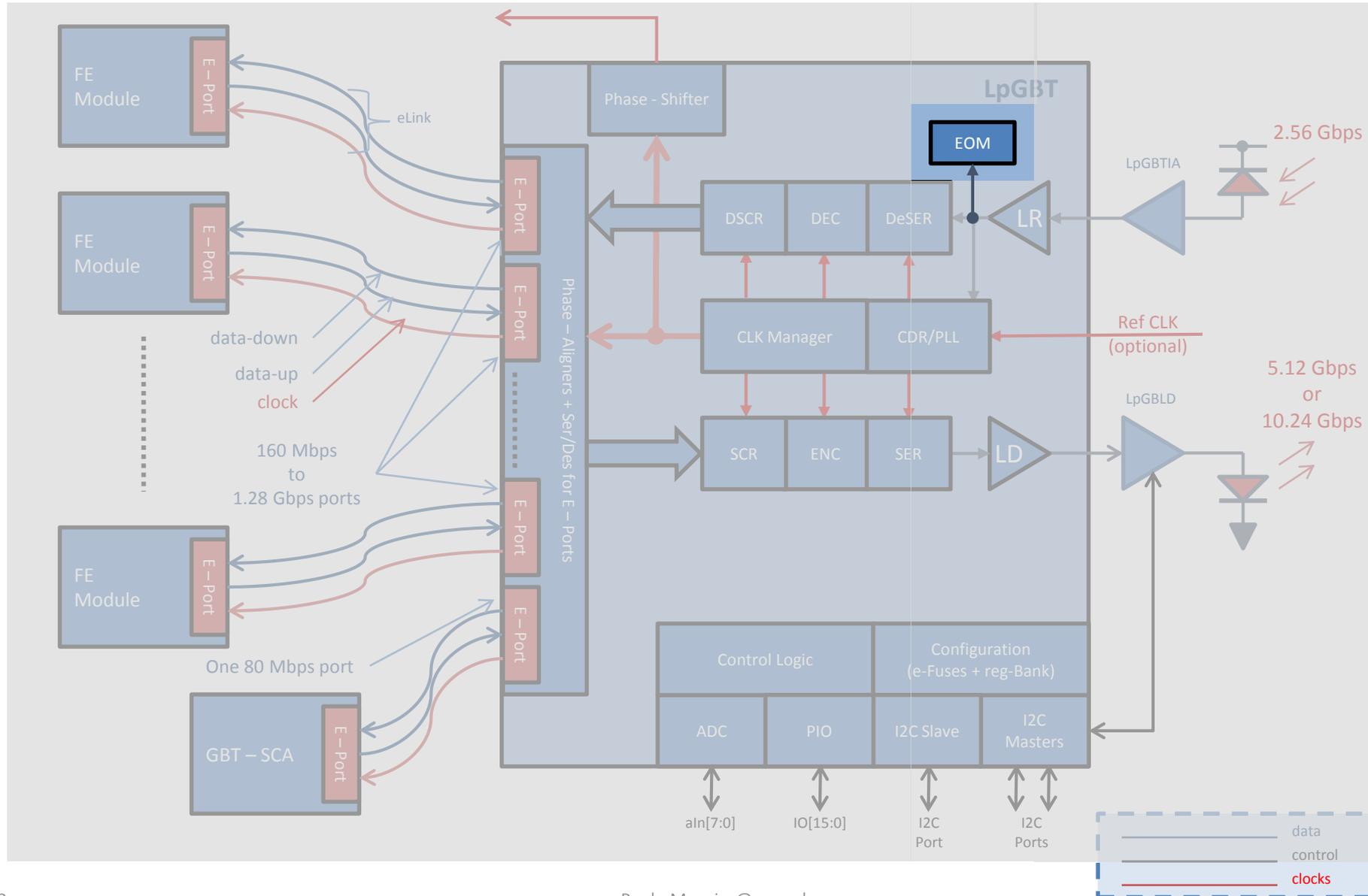
Eye Opening Monitor

- Y-axis:
  - 31 points, step = ~20 mV (covers from $V_{DD}/2$ up to V_{DD})
- X-axis:
  - 64 points, step = ~6.1 ps in typical
- Operation:
  - Controlled through the I2C interface
 - Eye reconstruction at the "backend"

In-phase Signal

EOM
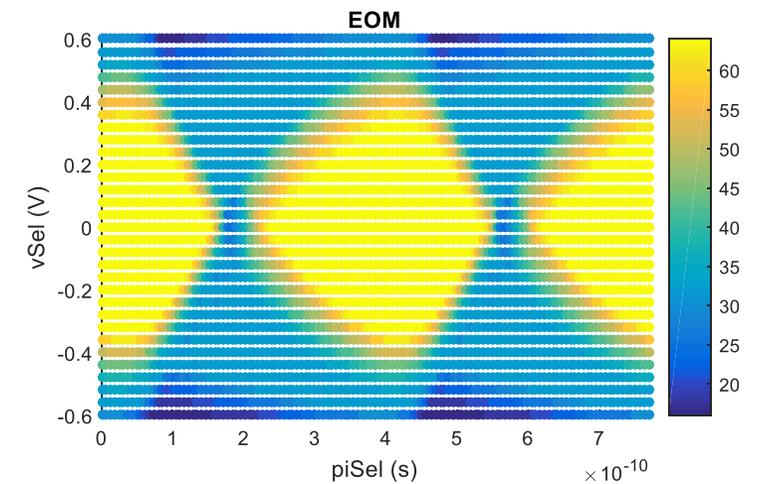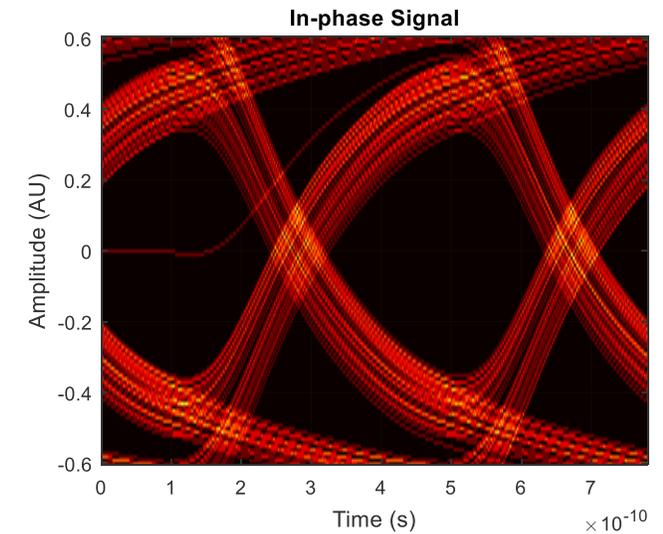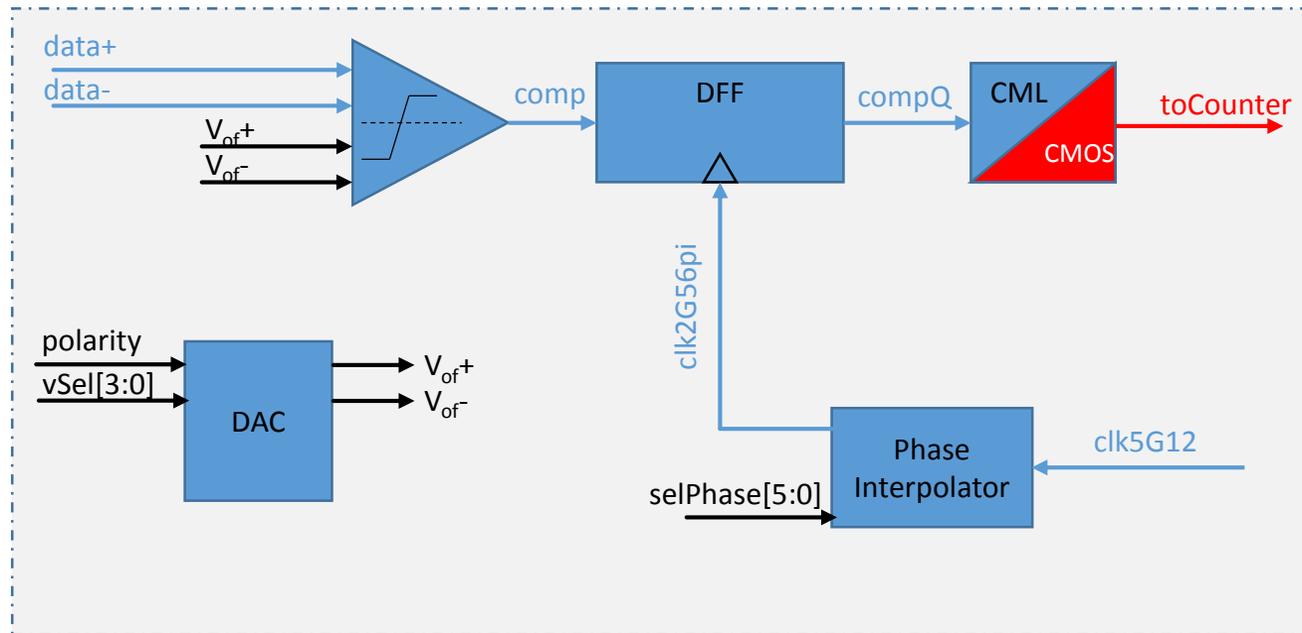
PLL / CDR and Clock Manager
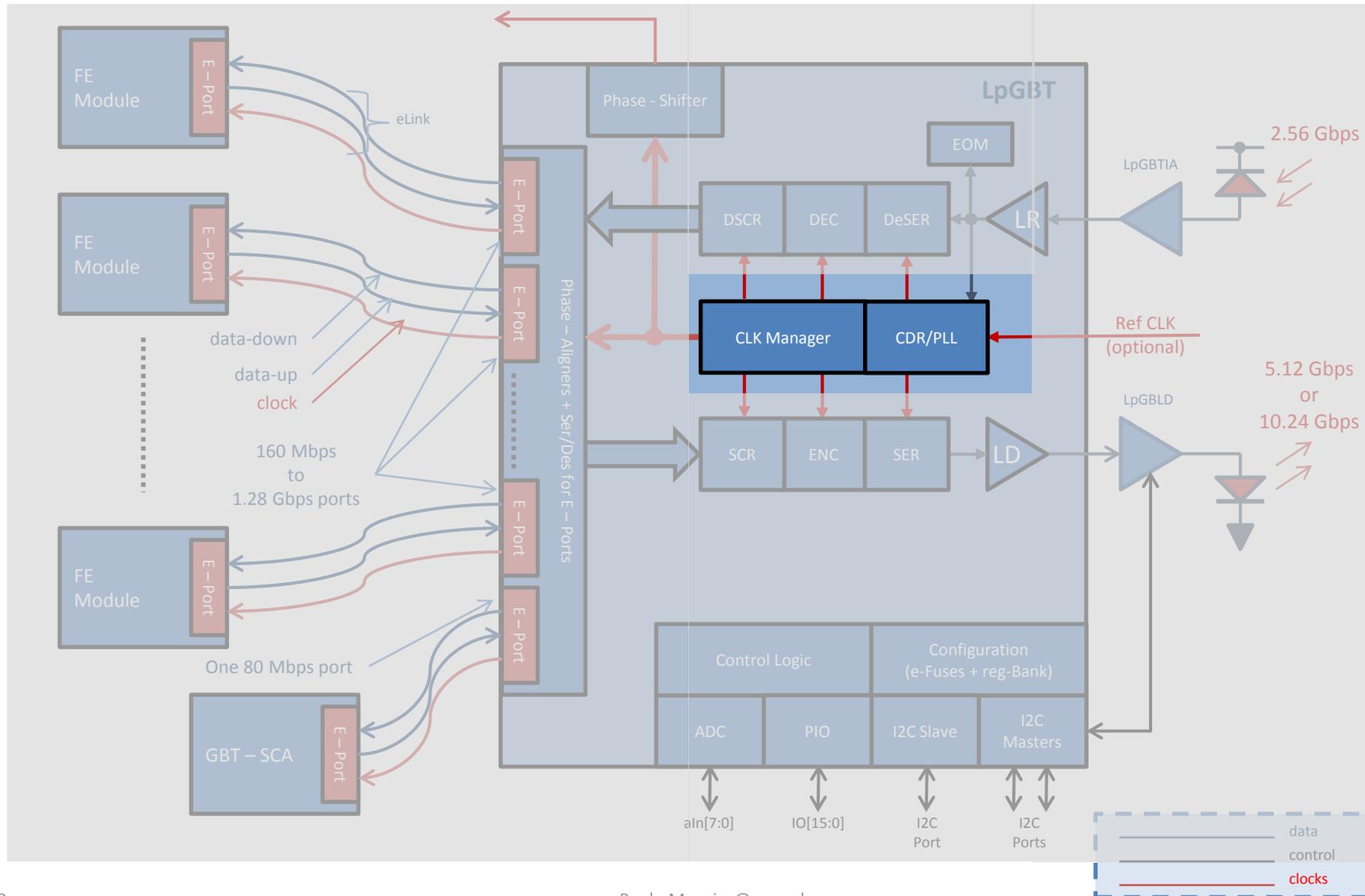
Clock Syntheses

- **This circuit generates all the clocks needed by the ASIC:**
  - 40 MHz, 80 MHz, …, 5.12 GHz
  - The 10.24 Gbps Serializer uses a DDR scheme

- **Simplex TX:**
  - A 40 MHz external reference is needed

- **Simplex RX and Transceiver:**
  - The downlink serial stream is used as a clock reference

- **CDR Locking modes:**
 - External reference aided
  - Reference-Less Locking

40 MHz → PLL / CDR + Clock Manager

2.56 Gbps → PLL / CDR + Clock Manager

Outputs: 5.12 GHz, 320 MHz, 160 MHz, 80 MHz, 40 MHz

Down Link Data Path

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Downlink Data Path

2.56 Gbps CDR circuit

data[N:0]

DeScrambler ← FEC DeCoding (error detection /correction) ← DeInterleaving ← CDR & DeSerializer ← serialData

header ←
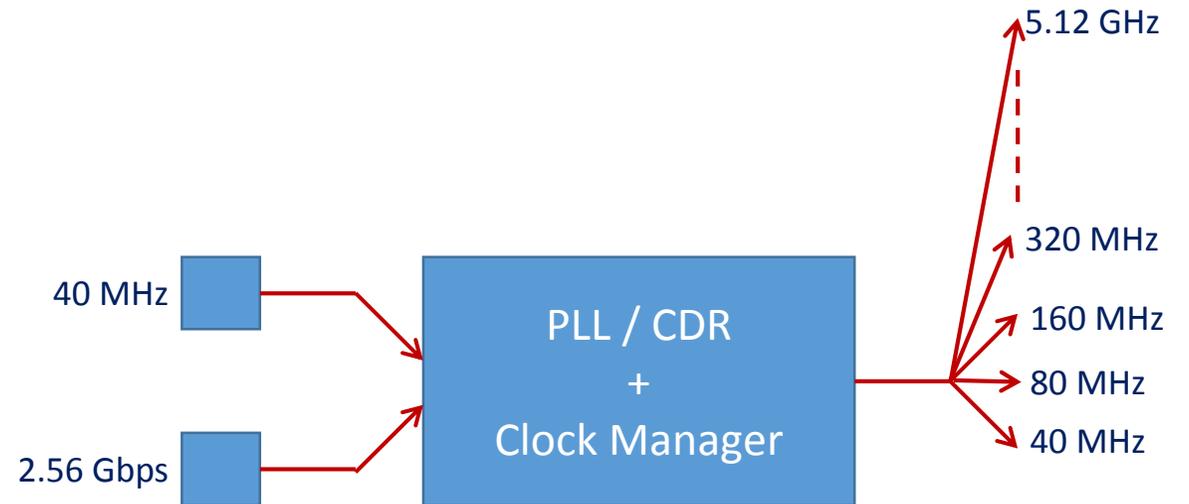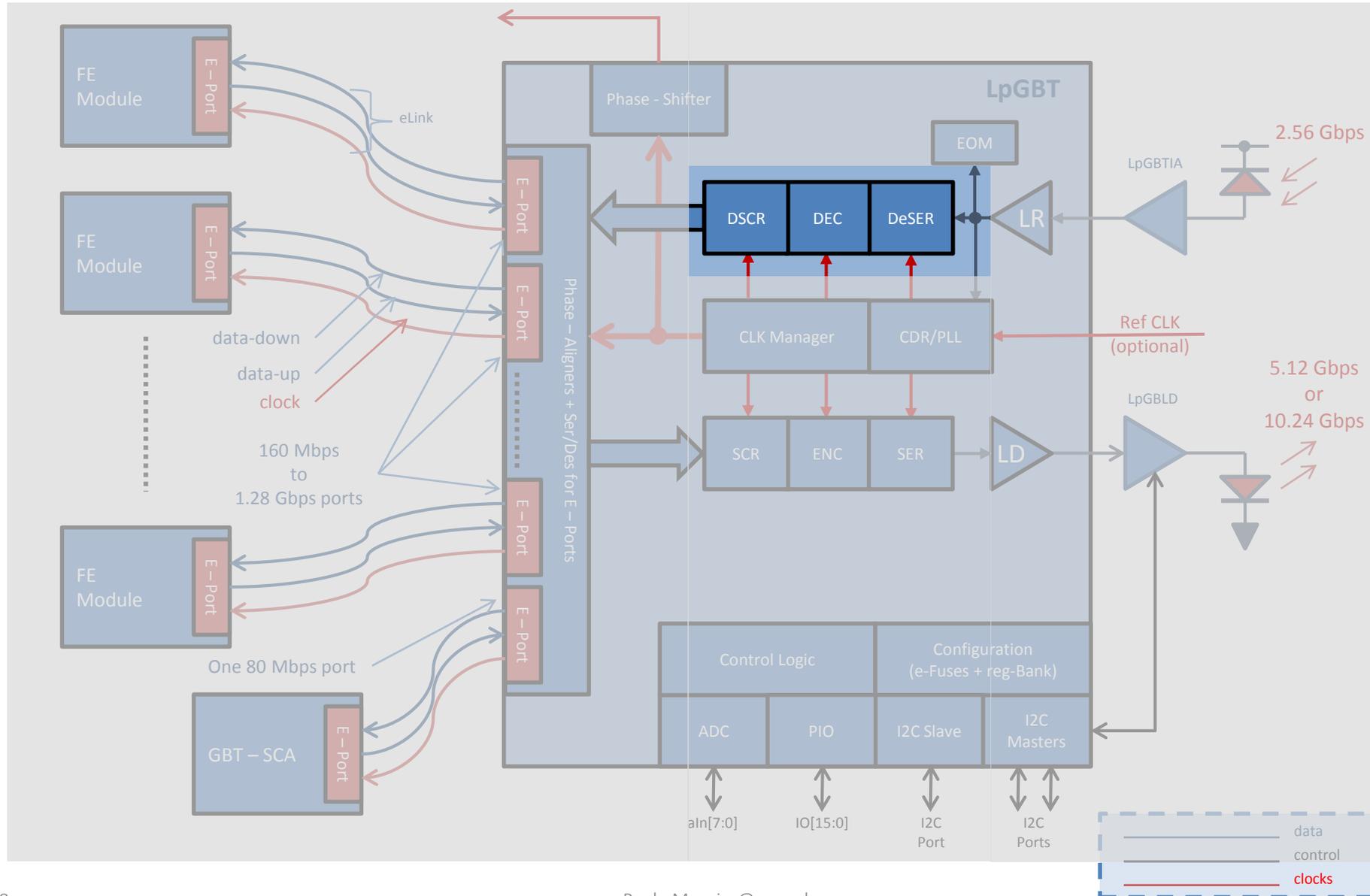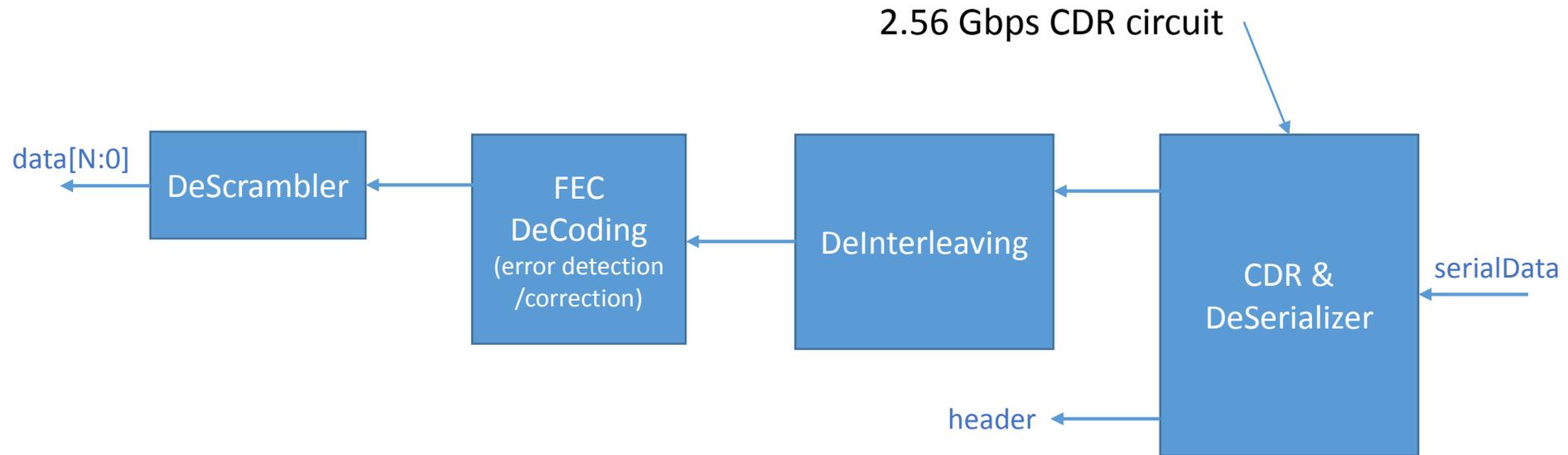
The order of operations is important

[Once again] We avoid the details here since you will not have to worry with them, they will be "handled" by lpGBT-FPGA

# eLink Groups and Serialization
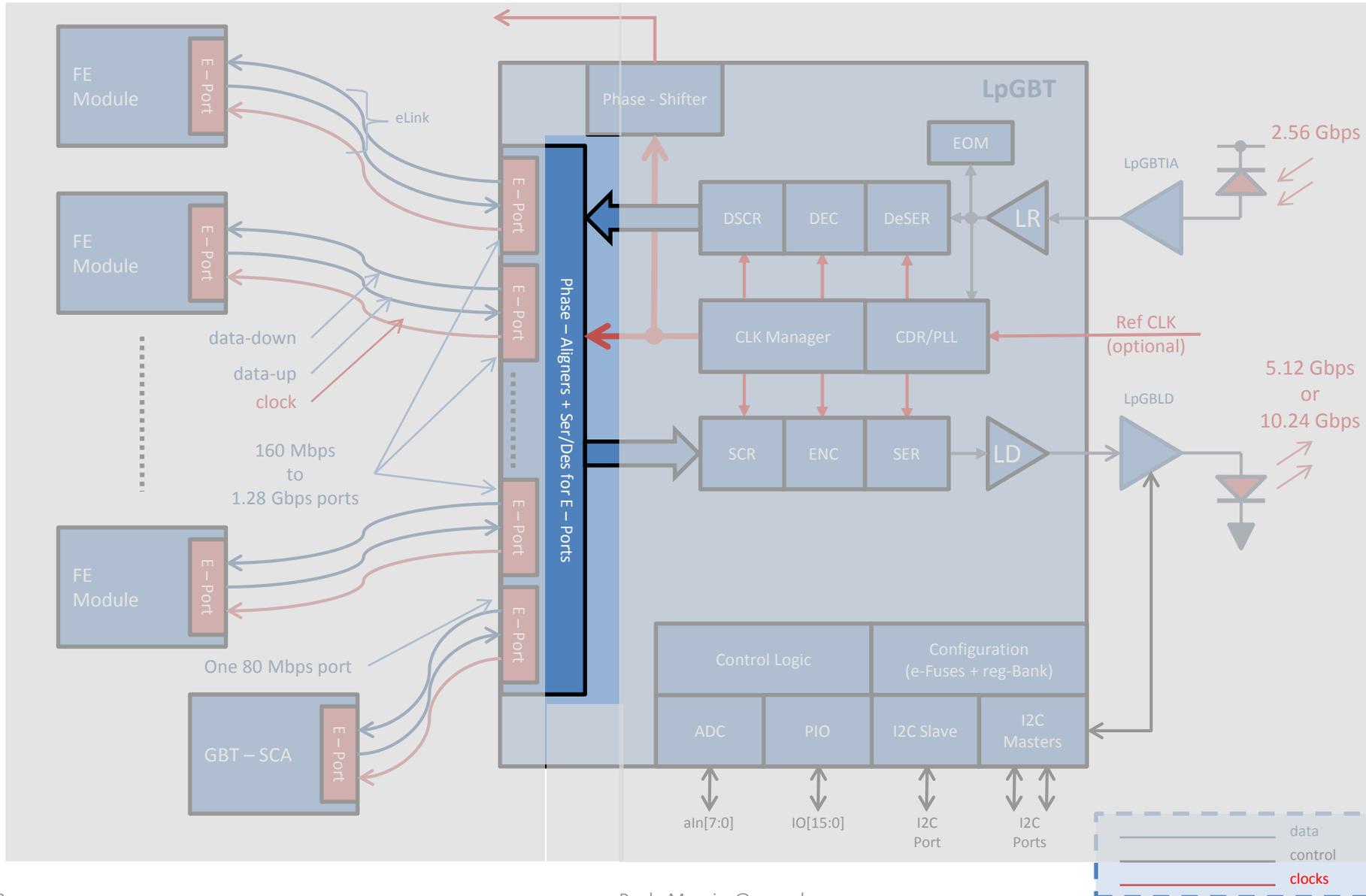
eLink Tx Groups & Serialization

- Tx eLinks are "clustered" in groups of 4 (similar to RX eLinks):
- The data rate of each group can be set independently:

    80 / 160 or 320 Mbps

- The number of available eLinks within a group is determined by the Group data rate;
- [Similar to the uplink] Tx eLinks are associated with specific bits within the downlink frame (geographical addressing):
  - The user knows, from the position of the bits (and the selected data rate) in the frame, to which eLink the data will be serialized to.
- EC outputs (pins: EOUTECP / EOUTECP) are fixed data rate (80 Mbps) that can be used for Experiment Control in Transceiver mode or participate in the control of the ASIC itself in Simplex TX or RX modes

| Output eLinks (down-link)			
Bandwidth [Mb/s]	80	160	320
Maximum number	16	8	4

eLink Tx "Mirror" function

- To help implementing broadcast of data to the frontends, a "mirror" function is implemented for the Tx eLinks:
  - Call it "buffering" if you prefer!
- Since the number of active Tx eLinks depends on the selected data rate, "unused" transmitters can be used to "repeat" the data of the active channels
- This called "mirror" function
- The possibilities are:
  - 80 Mbps:
    - No mirroring
  - 160 Mbps:
    - Each channel is [can be] available on 2 outputs
  - 320 Mbps:
    - Each channel is [can be] available on 4 outputs

eLink Line Transmitter (eTx)

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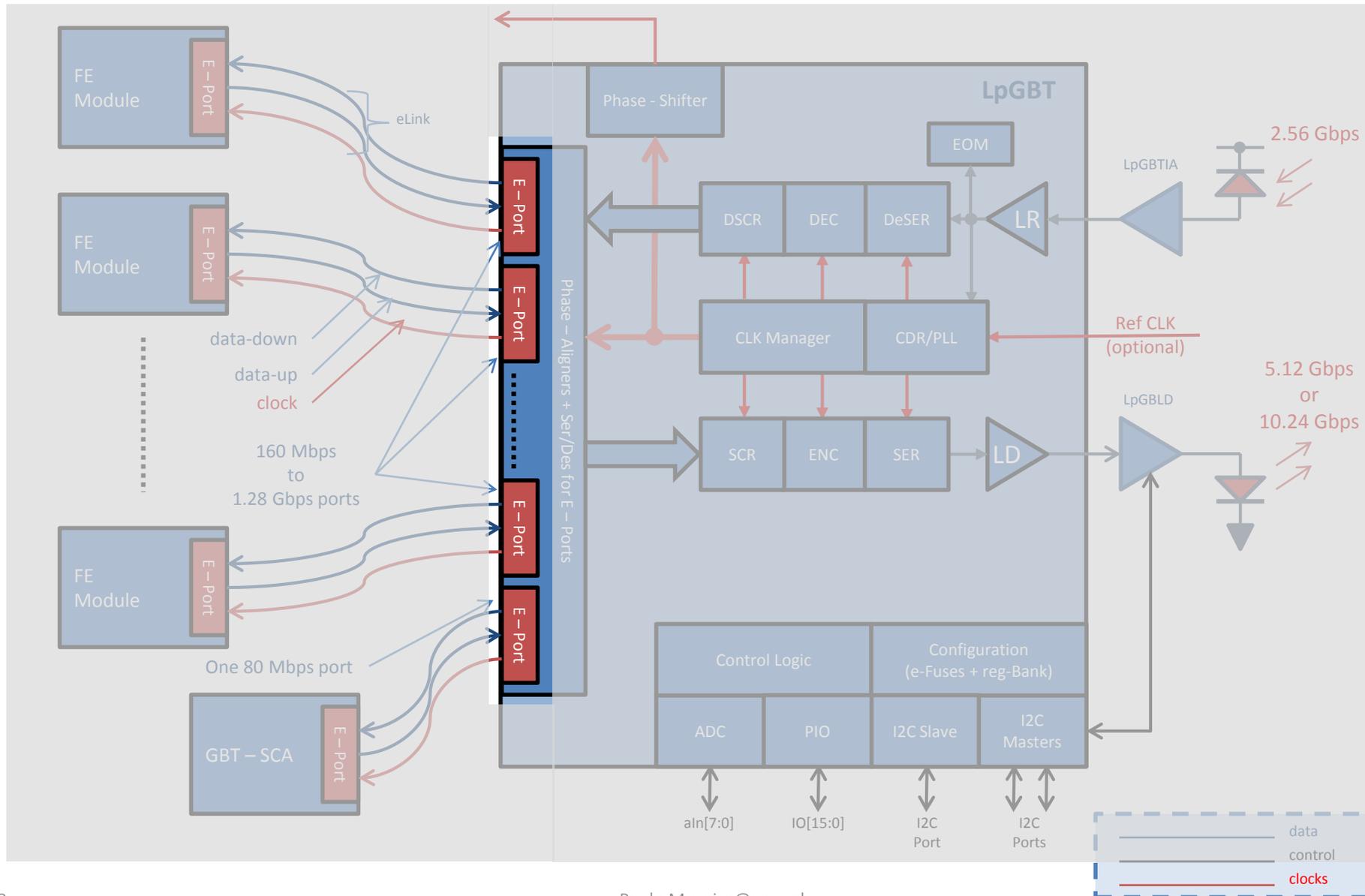
eLink Driver

- Data rate:
  - Up to 1.28 Gbps
- Clock frequency:
  - Up to 1.28 GHz
- Driving current:
  - Programmable: 1 to 4 mA in 0.5 mA steps
- Receiving end termination:
  - 100 Ω
- Voltage amplitude in 100 Ω:
  - 100 mV to 400 mV (SE PP amplitude)
  - 200 mV to 800 mV (DIFF PP amplitude)
- Common mode voltage:
  - 600 mV
- Selectable polarity
- Pre-emphasis:
  - Driving current: 1 to 4 mA in 0.5 mA steps
  - Pulse width:
    - Externally timed
    - Self timed: 120 ps to 960 ps in steps of 120 ps
    - Clock timed: $T_{bit} / 2$
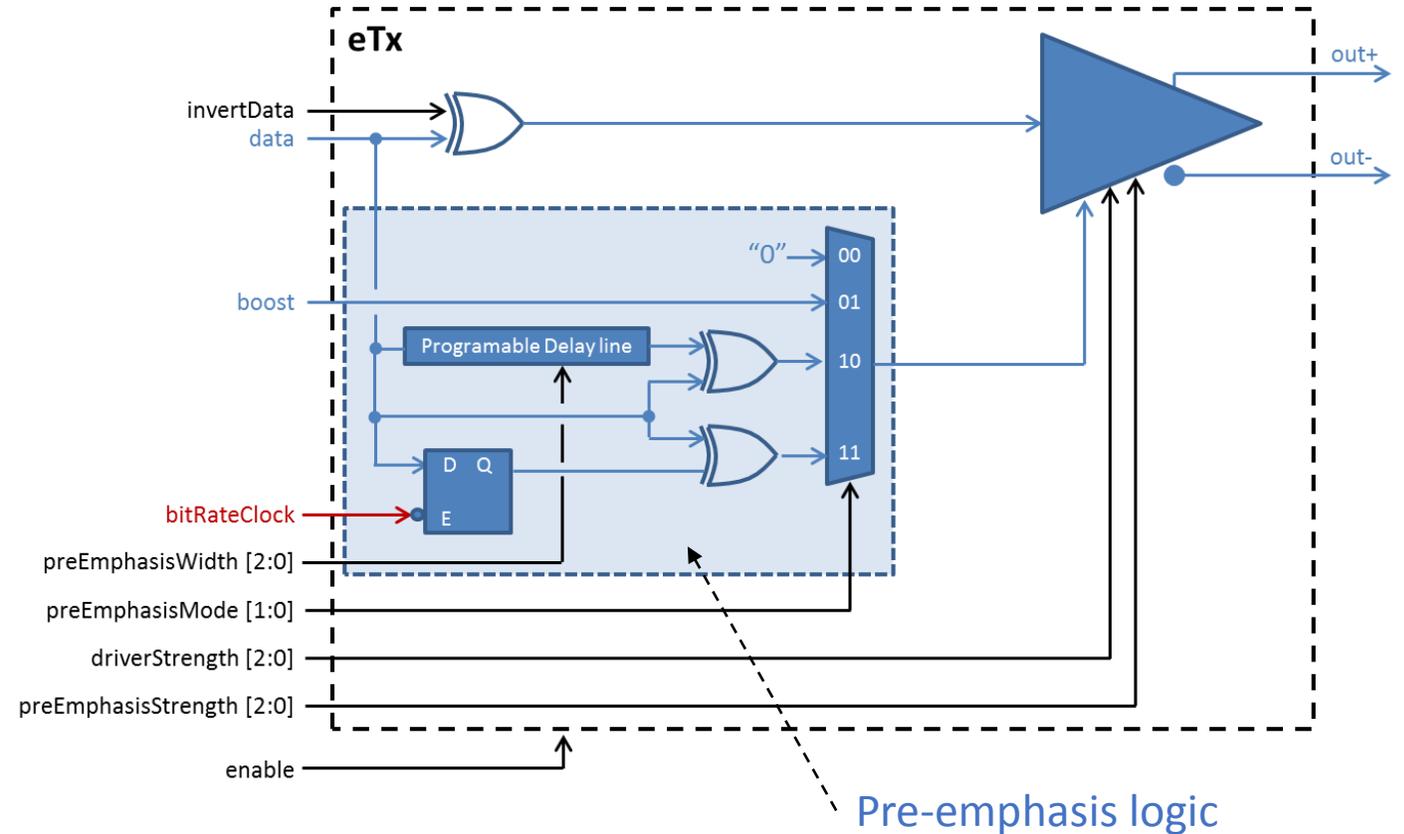
Pre-emphasis logic

Macro cell, available for front-end designers (upon request)

eTx Functionality

Controls the polarity of the driver

Half bit period pre-emphasis pulse width

Pre-emphasis self-timed pulse width selectable

Pre-emphasis mode selectable

Pre-emphasis amplitude programmable
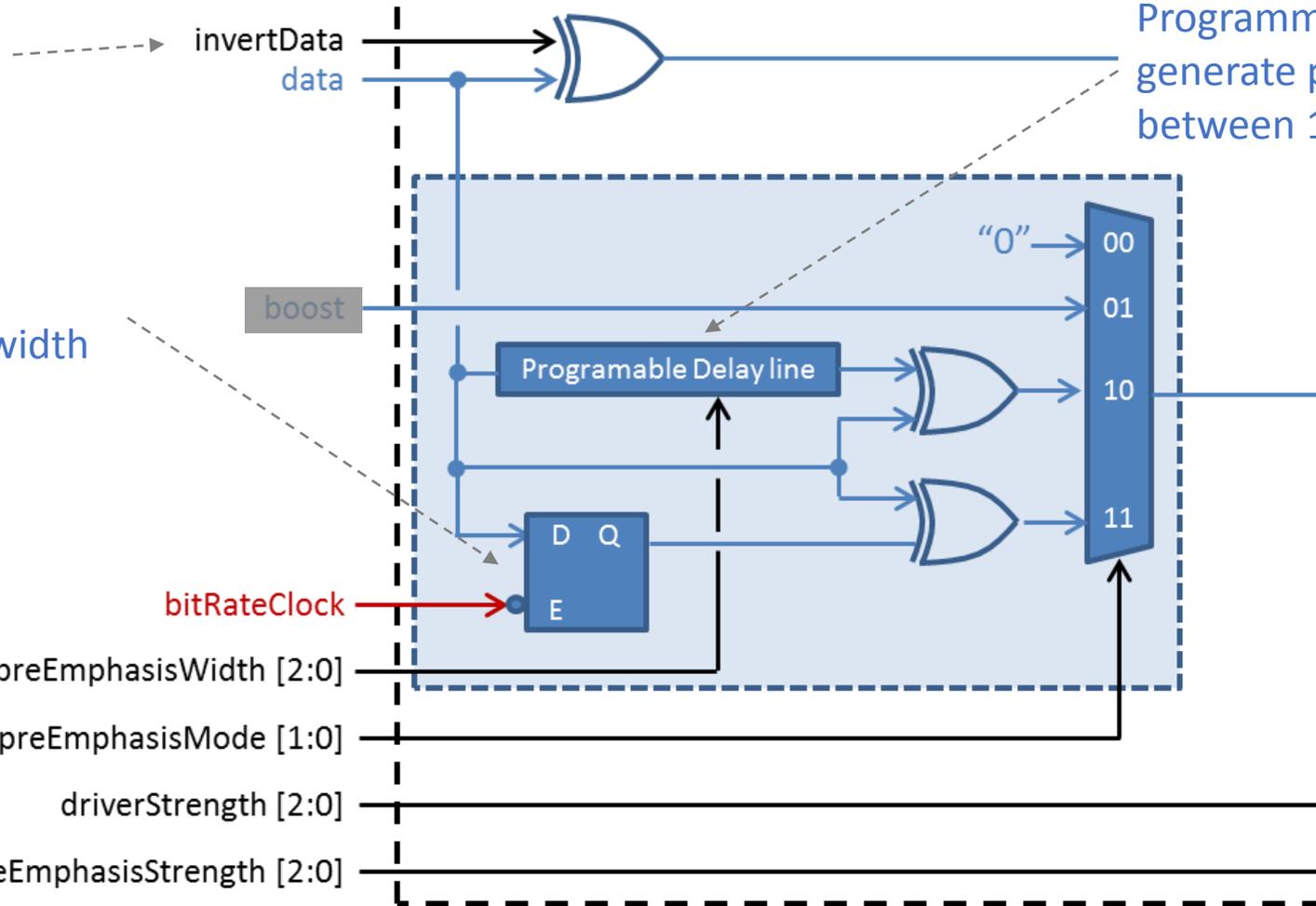
Programmable delay line allows to generate pre-emphasis pulse widths between 120 and 960 ps

Pre-emphasis pulse

invertData
data
boost
"0"
00
01
Programable Delay line
10
11
D Q
bitRateClock
E
preEmphasisWidth [2:0]
preEmphasisMode [1:0]
driverStrength [2:0]
preEmphasisStrength [2:0]

eTx – Pre-Emphasis

Data: PRBS 7
Data rate: 2.56 Gb/s
C_L = 2 x 5 pF

No Pre-Emphasis
    Driver Strength = 2 mA
    Pre-Emphasis Strength = 0 mA
    Pulse width = n.a.

With Pre-Emphasis
    Driver Strength = 2 mA
    Pre-Emphasis Strength = 2 mA
    Pulse width = T/2
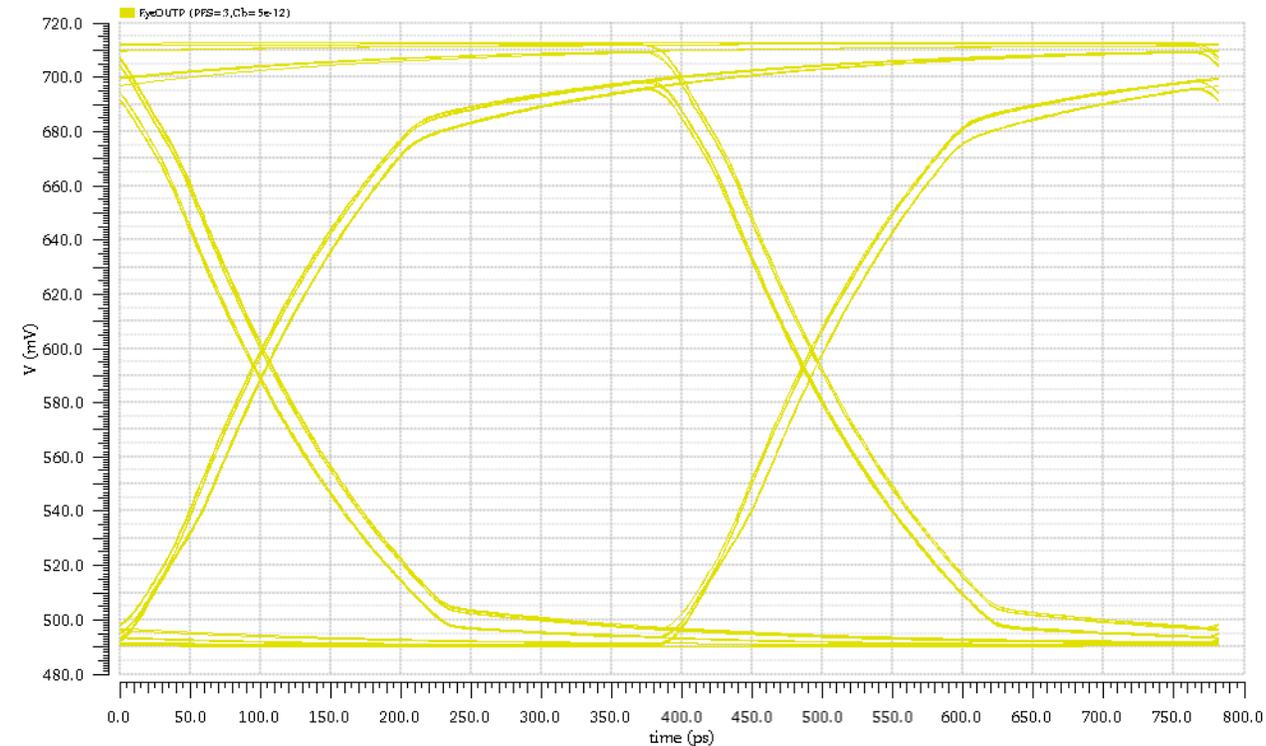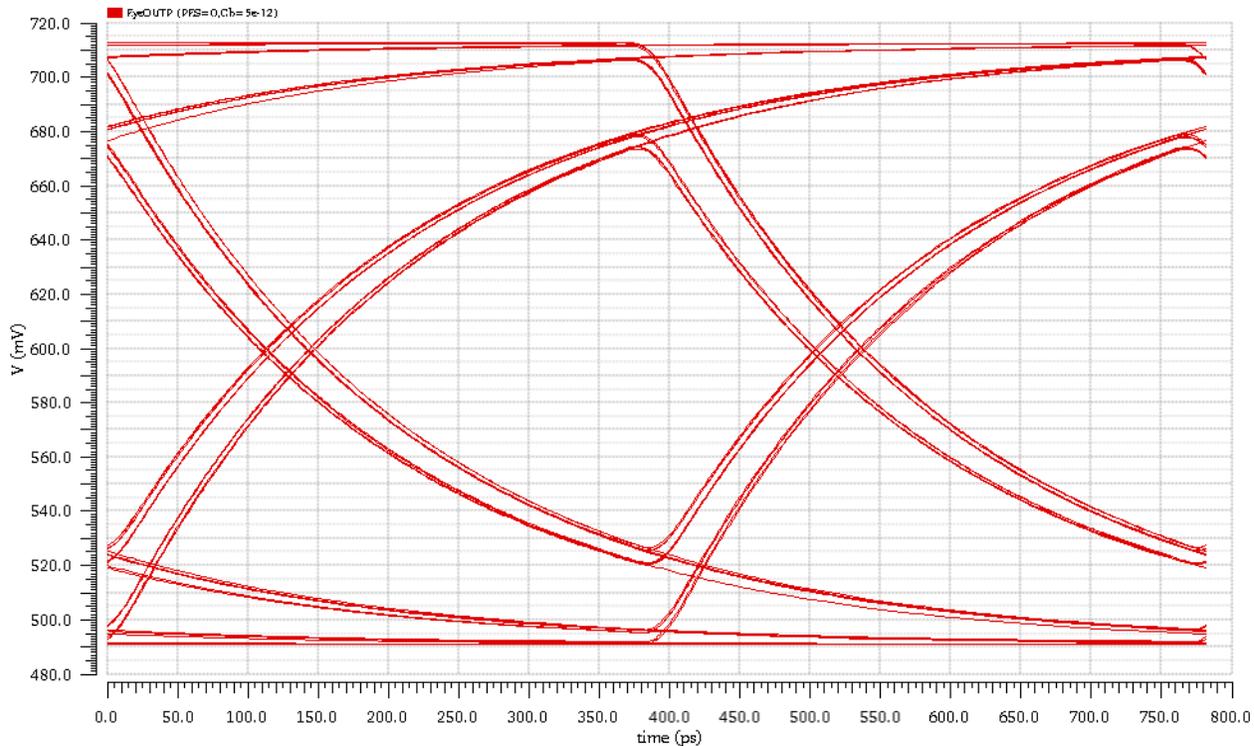
Note about eLink Output Pin Names

Output from the lpGBT

eLink

Group number: 0, 1, 2 and 3 (there are 4 groups)

EDOUTGCP

Data

Pin Polarity: P – Positive, N – Negative
(Remember: polarity can be inverted
at the output of the corresponding eTx)

Channel number within a group: 0, 1, 2 or 3 (there
are 4 eLinks associated with every group)
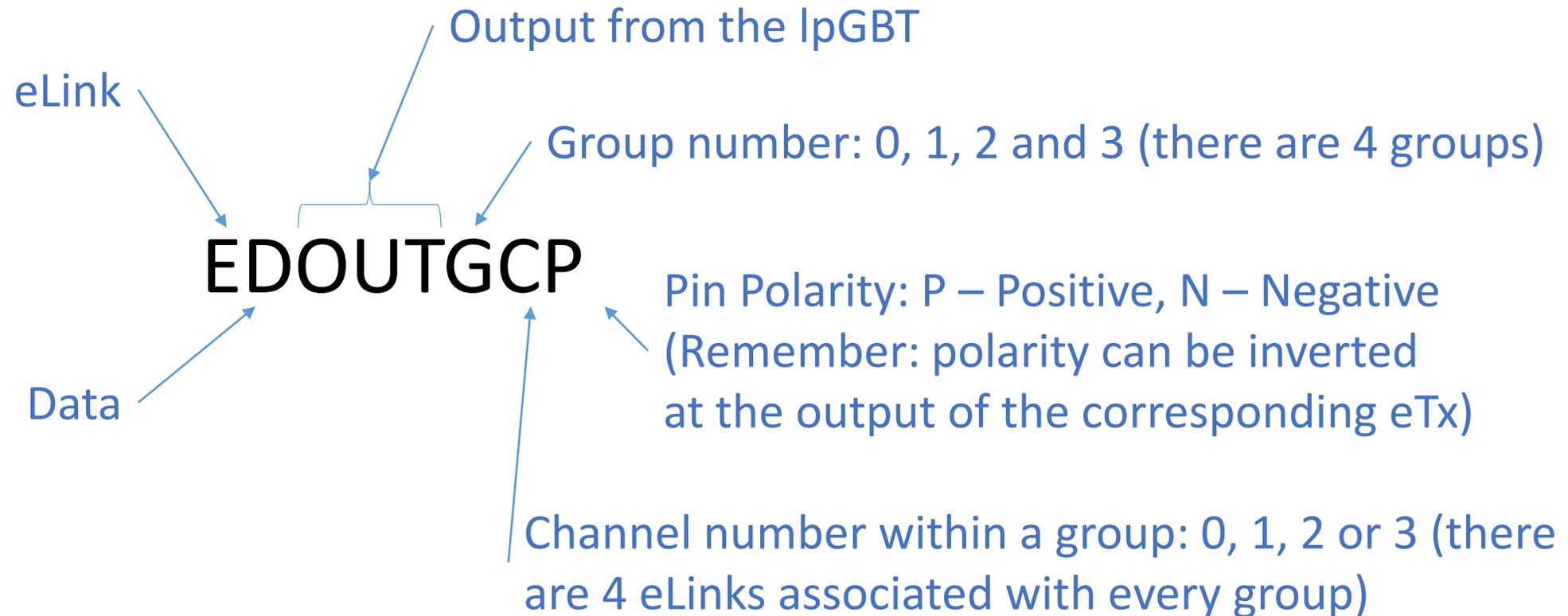
Example: EDOUT32N – eLink data output group 3 channel 2 negative polarity pin

eLink Clocks
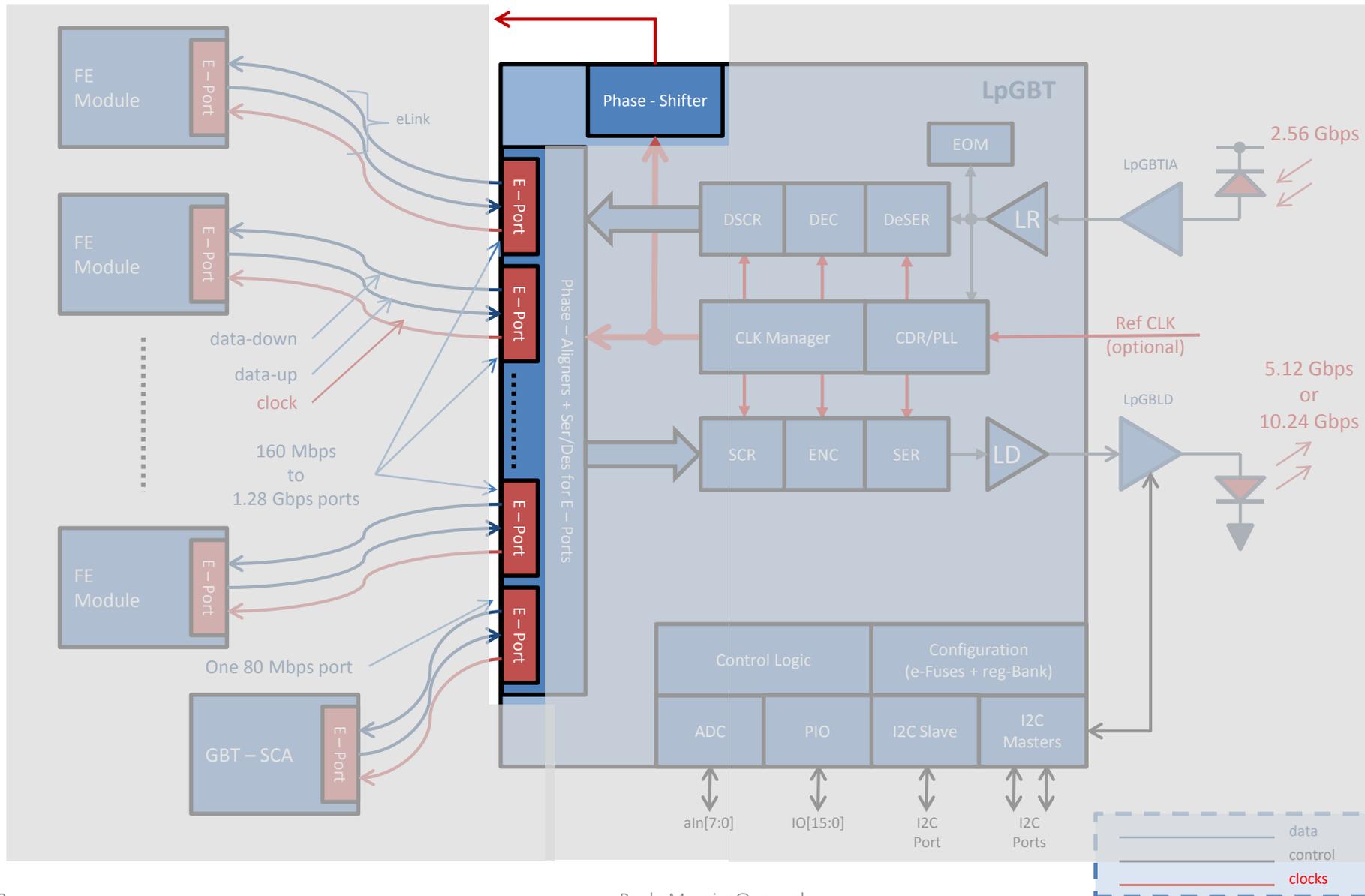
eLink Clocks

- Same drivers as for the Tx data eLinks, thus:
  - Programmable: polarity, driving strength and pre-emphasis

- 4 programmable Phase/Frequency clocks:
  - 4 independent
  - Phase resolution: 50 ps
  - Frequencies: 40 / 80 / 160 / 320 / 640 / 1280 MHz

- eLink Clocks:
  - 28 independent
  - Fixed phase
  - Frequency programmable
 - Frequencies: 40 / 80 / 160 / 320 / 640 / 1280 MHz
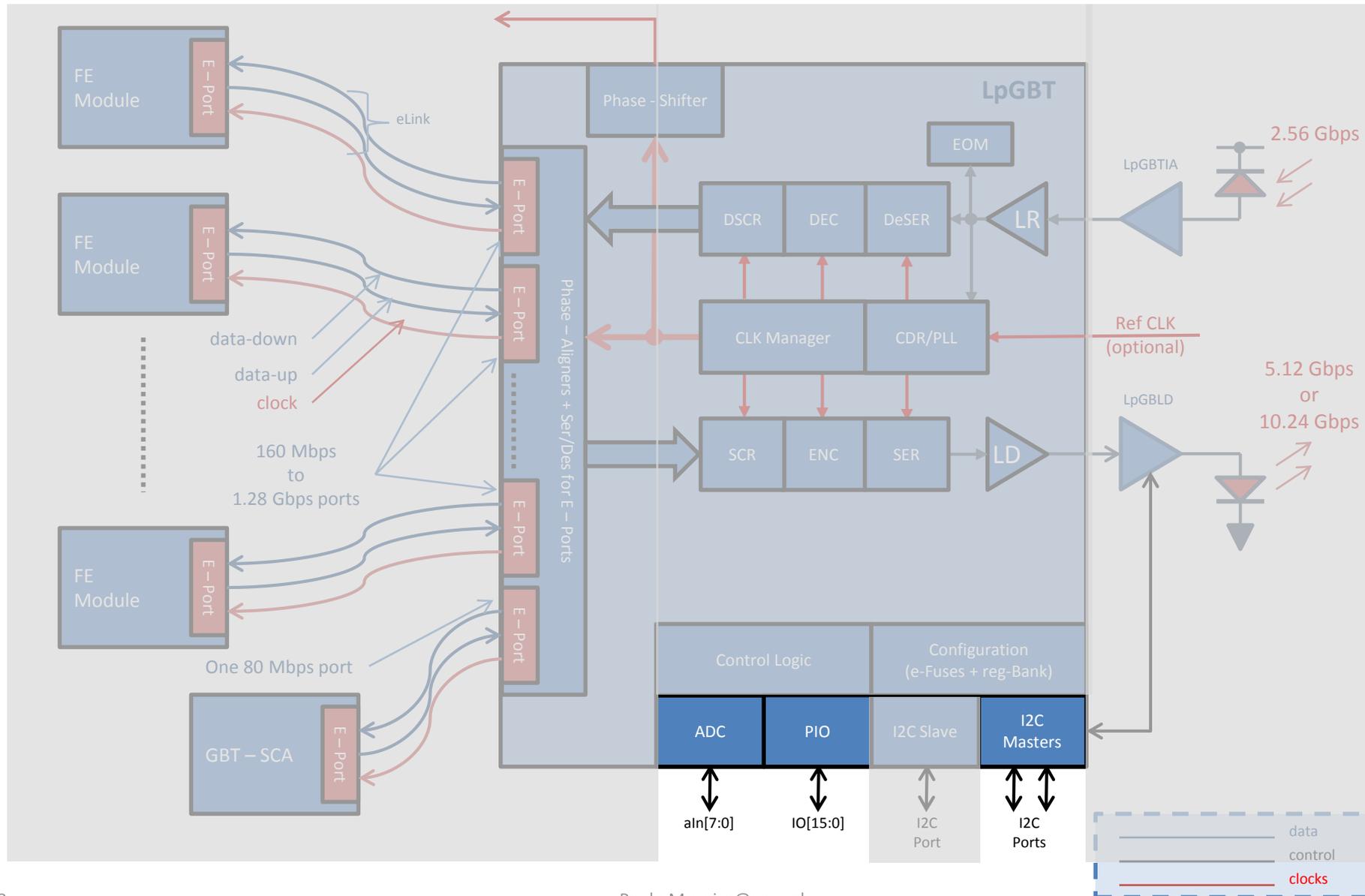
Digital

- Three I2C Masters:
  - Three general purpose masters
    - But one typically dedicated to control the laser driver (LDQ10)
  - Transfer rates: 100 KHz, 200 KHz, 400 KHz, 1 MHz
  - 7-bit and 10-bit addressing standards
  - Single-byte and multi-byte I2C read/write bus operations
  - Masters themselves controlled by:
    - The I2C slave port (always possible)
    - The IC – channel (only possible in transceiver mode)
    - The EC – port (Only possible in Simplex RX or TX mode)

- General Purpose I/O
  - 16-bit I/O port
  - Optional internal pull-up / pull-down resistors
  - Controlled by the same means as the I2C masters

- Output reset pin
  - Active low
  - Programmable pulse duration

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Analogue Peripherals
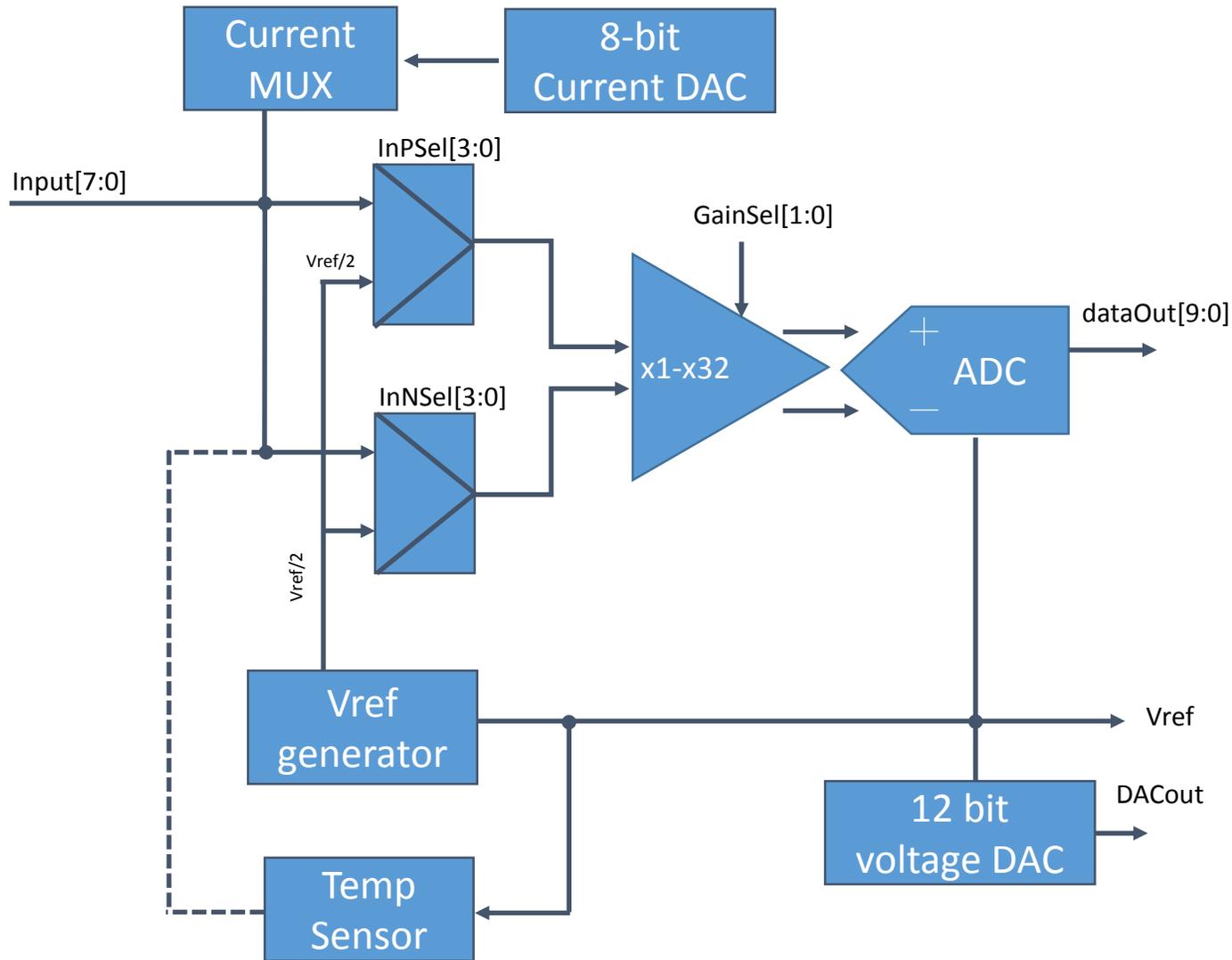
- 10 bit ADC
  - Core: fully differential SAR
  - 8 channels (single ended or differential)
  - Voltage amplifier (x1 .. x32)
  - Sampling rate up to ~ 1MSps (limited by the control channel)
  - Monitoring of internal signals (like VDD)

- 12 bit voltage DAC

- 8 bit current DAC
  - can be attached to any analog input
  - range: 0-1mA (8bit)

- Temperature sensor

# Example: Using an External Temperature Sensor
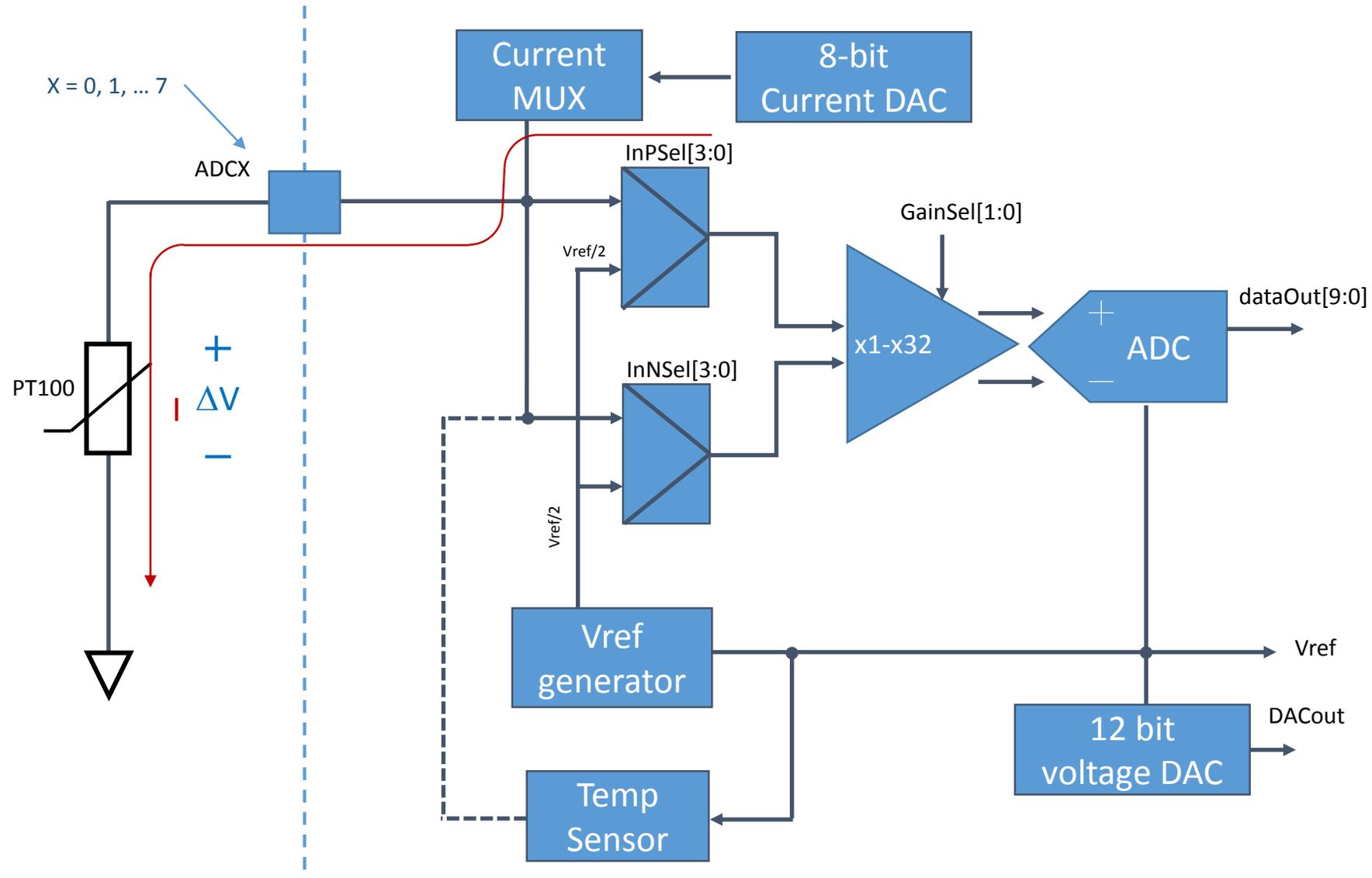
Package

- Small Footprint BGA package:
  - Size: 9 mm x 9 mm x 1.25 mm
  - Fine Pitch: 0.5 mm
  - Pin count: 289 (17 x 17)
- Routing of high speed signals optimized and simulated
  - Very small loss @ 10GHz
  - Models used for line driver simulations

Dimension A = 1.243mm (max.)
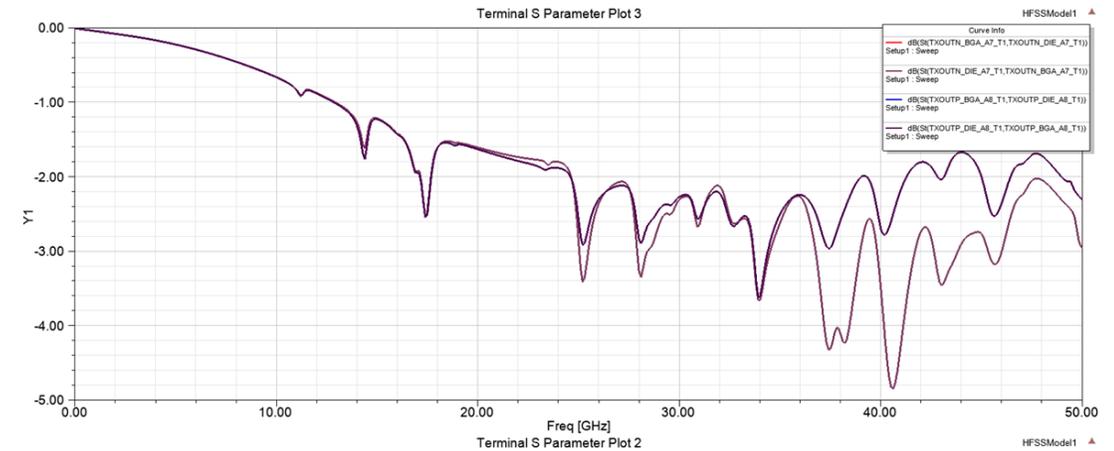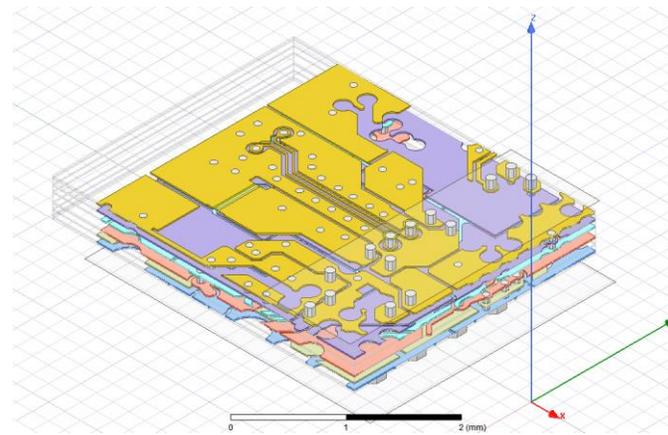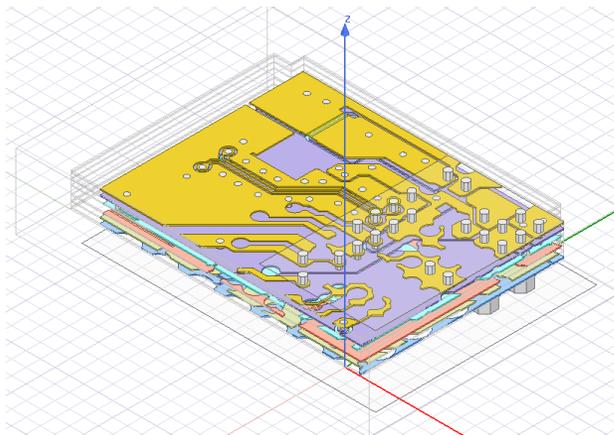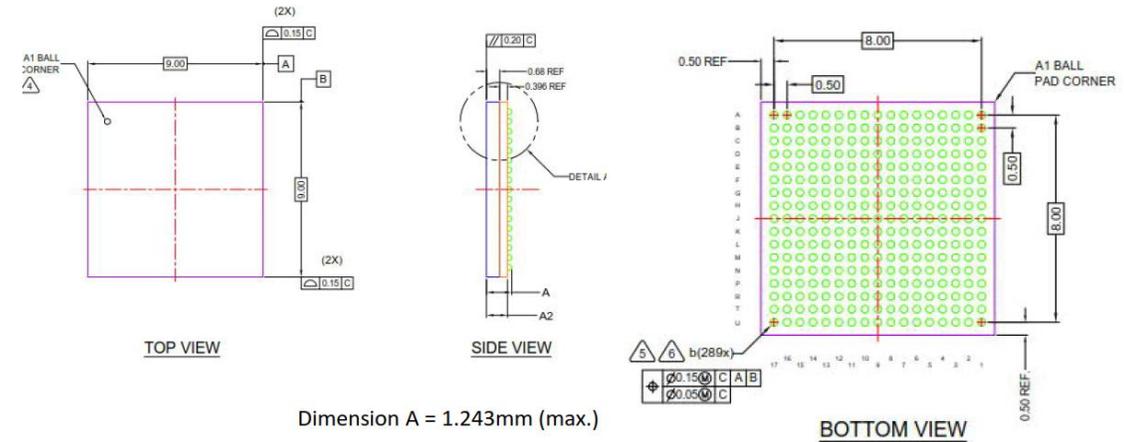
lpGBT FPGA

- The lpGBT-FPGA provides a back-end counterpart to the lpGBT ASIC

- Warning:
  - "Strategy" departures from that used for the GBT-FPGA
  - Not a single generic "block";
  - But a set:
    - Of modules;
    - Of implementation examples;
    - Of reference notes.
  - To help the user designing its own system!
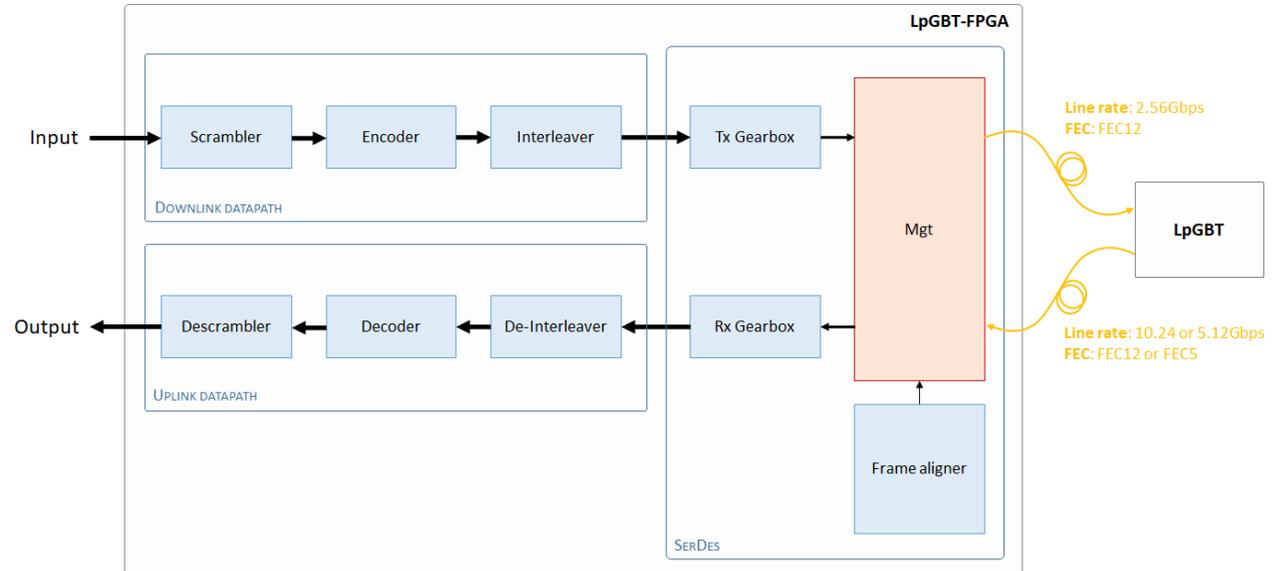
lpGBT Simulation Model

- The lpGBT model (will be) available to the users:
  - To simplify the design and verification of front-end (ASIC) and back-end (FPGA) systems
- Contains all essential features related to the data transition and slow control interfaces:
  - Some of the chip's analogue features are not modelled:
    - e.g.: pre-emphasis, equalization, analogue I/O (ADC,DAC), pull up/down resistors;
- "Distributed" as one System Verilog file, compatible with:
  - Cadence Incisive
  - Mentor Questa
  - Synopsys VCS

"Additional" Slides

Using the eRx(s)

Equalization:

- Should only be used if needed (low bandwidth transmission line)
- Only effective for the high bit rates
- Equalization has (only) three coarse settings
- User must choose the most appropriate!
- This requires a verification / scanning procedure from the user:
  a) Ideally the front-end designer implements a PRBS7 that the lpGBT can automatically verify;
  b) The user verifies the transmitted data at the counting room;
  c) A detailed scan procedure will also be proposed by the lpGBT team…

eRx Check list:

- Turn ON the receivers corresponding to the eLinks in use.
  - Obviously the others should be OFF
- Choose the polarity (non-invert / invert)
- Turn on the termination:
  - Most likely the case (unless the chip in a multiple drop configuration – unlikely, or AC coupling to be optimized)
- Enable the internal bias, if using AC coupling
- Choose the appropriate equalization setting

Using the Line Driver

The user must:

- Enable the line driver for Transceiver and Simplex Transmitter modes:

- Enable the pre-emphasis if needed;

- Set the amplitude of the:
  - Modulation current;
  - Pre-emphasis current.

- Set the pre-emphasis pulse duration;

- It is possible to invert HS output polarity to simplify the PCB design:
  - The inversion is done @40M (before the Serializer) at the frame level.

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