Clock and Data Recovery for a 6 Gbps SerDes Receiver

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***Abstract*— This paper presents the design and implementation of a 6 Gbps clock and data recovery (CDR) system for Serial Advanced Technology Attachment (SATA) standard. The CDR incorporates half rate phase detector and is realized using a 2 loop PLL consisting of a coarse loop and a fine loop. Fast frequency acquisition is acquired through coarse loop and fine phase alignment is performed through a half rate fine loop. While the coarse loop can recover clock ranging from 2.5 GHz to 3.2 GHz the fine loop has an acquisition range of 200 KHz. The design has been implemented in IBM 0.13um CMOS technology. Verilog AMS and Matlab were used for front end design and Cadence for schematic and layout implementation. The overall silicon area of the CDR is approximately 108 X 244 um^2 excluding loop filter capacitors.**

Keywords-Clock recovery, half-rate CDR, Serial ATA communication, oscillators, phase detectors, PLLs, Comparator

I. INTRODUCTION

The demand for high data rate and higher clock frequencies has grown steadily over the past decade. Communication networks such as Ethernet, SONET/SDH, ATM, SATA require higher bandwidth and greater efficiency to support its growing traffic. Parallel interconnects failed to serve this ever increasing bandwidth requirement mainly due to the length of the interconnect wire, crosstalk, skew adjustment and board space. This lead to the development of the serial data transfer technology protocol. A serial data transceiver is commonly called as SerDes (Serializer-Deserializer). The main task of a Serdes system is to transmit data at high rate (Serializer) over a wired interconnect and to receive it reliably at the receiver (Deserializer) end. This paper presents the design, verification and physical realization of a high speed clock and data recovery circuit with an operation range of 5Gbps to 6.4 Gbps implemented in IBM 0.13um technology. The design is fully differential and the layout consists of symmetrical blocks with special low power digital and analog layout techniques.

II. GENERAL ARCHITECTURE

A typical block diagram of a SerDes communication system is shown as follows:

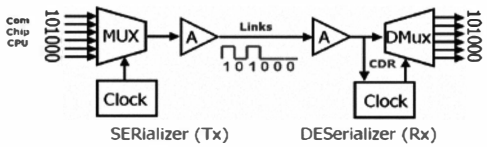

Figure 1. SerDes Transceiver block diagram

The sender which can be a router, CPU, I/O chip, etc sends parallel data to the transmitter. The parallel data is then multiplexed (MUX) by the transmitter and converted to a serial data stream [1]. At the receiver end this serial data is recovered by a clock and data recovery circuit present in the Deserializer and again demultiplexed (DEMUX) into the original parallel data stream. The MUX-DEMUX performs the parallel to serial at transmitter and serial to parallel at receiver conversion. The MUX-DEMUX should be synchronized to system clock which is a high frequency clock generated from a Phase Locked loop [1].

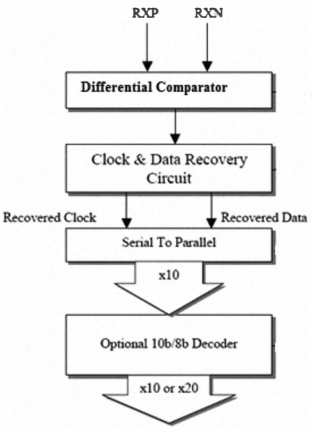

Figure 2. Deserializer unit block diagram

The block diagram of a typical SerDes receiver is shown in the Fig. 2. A serial data stream is generally a non-return-to-zero (NRZ) digital stream to increase the data rate of a serial communication. However if a transmitted NRZ data stream has long runs of 1 or 0 pattern, CDR fails to recover clock and data synchronization due to intersymbol interference (ISI) [1]. Transmitter and receiver also use different clocks, making the task of CDR more difficult. In order to deal with this problem, transmitted data is generally encoded to have equal numbers of 1 or 0. A typical encoding

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method used is called 8B/10B coding which consists of mapping an 8-bit word to a 10-bit word [1]. 8b/10b decoding removes baseline wander and guarantees that there are sufficient transitions in the transmitted data stream and the receiver recovers the clock from this serial data stream reliably. This project employs an 8B/10B encoder implemented in Verilog-AMS for generating the test vectors for testing the design. As show in Fig. 1 the main focus of the project is designing and implementing the differential comparator and the clock and data recovery circuit. The following sections describe the architectural details of these two main blocks.

The differential receiver function can be explained as follows:

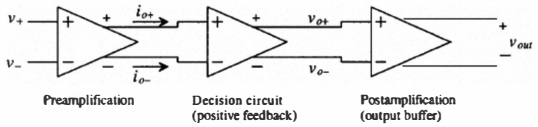


Figure 3. Differential receiver

The comparator consists of NMOS differential amplifiers to achieve the SATA bandwidth of 6Gbps data transfer. The comparator compares the differential signals received from the transmitter and gives rail to rail outputs which are then fed to the clock and data recovery circuit. The input signal is at a common mode voltage of 250mV and a differential mode voltage of 250mV peak-peak. The comparator consists of three stages Preamplification stage, Decision circuit stage and Postamplification stage. The first stage is level shifting stage, the second stage is the NMOS differential comparator and the third stage is the output buffer stage. The decision circuit has been implemented using NMOS transistors in order to achieve speed. The simulation results are shown in experimental results.

The following section describes the architectural details of the Clock and Data recovery circuit which is the most important and complex block of the receiver design.

III. Linear Charachterization Of PLL

A 2-Loop PLL was chosen for realizing the CDR circuit. Two loops are necessary because a phase-locked loop alone has a slow and unreliable frequency acquisition range. The diagram of the 2- Loop PLL is as shown below [2]:

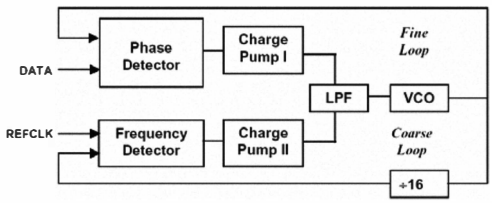


Figure 4. 2- Loop PLL block diagram

The first loop is for frequency acquisition, called "coarse loop", it helps VCO clock frequency to reach data frequency by bigger steps initially. Second loop is for providing the fine phase alignment called "fine loop", it aligns the clock to sample the data in the middle of the data eye [2]. In initial stages of the design the PLL has been modeled using Matlab and Verilog - AMS. The basic building blocks of a PLL are: (a) Phase- Frequency Detector for coarse loop (b) Charge pump for coarse loop (c) Phase detector for fine loop (c) charge pump for fine loop (d) Interpolation VCO (e) differential Loop filter. The open loop phase transfer function and closed loop phase transfer function of the PLL can be written as equations (1) and (2) respectively [3].

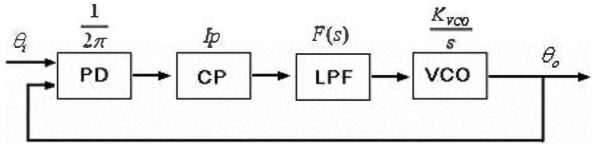


Figure 5. PLL linear model

$$G_o(s)=\frac{\frac{I_pK_{VCO}}{2\pi}(sRC_1+1)}{s^3RC_1C_2+s^2(C_1+C_2)}=\frac{s\frac{I_pK_{VCO}R}{2\pi}+\frac{I_pK_{VCO}}{2\pi C_1}}{s^3mRC_1+s^2(m+1)} \quad (1)$$

$$G_c(s)=\frac{s\frac{I_pK_{VCO}R}{2\pi}+\frac{I_pK_{VCO}}{2\pi C_1}}{s^3mRC_1+s^2(m+1)+s\frac{I_pK_{VCO}R}{2\pi}+\frac{I_pK_{VCO}}{2\pi C_1}} \quad (2)$$

$$\omega_n^2=\frac{I_pK_{VCO}}{2\pi C_1} \quad (3)$$

$$2\xi\omega_n=\frac{I_pRK_{VCO}}{2\pi} \quad (4)$$

The PLL has three important loop parameters that determine the overall system performance,

- *Natural frequency (n),*
- *Damping ratio (ξ) and,*
- *Capacitance ratio m (C1/C2)*

The Loop parameters for the PLL used in this project have been determined using the above loop equations with the help of Matlab. Next section describes the architecture level details of some important blocks in the design.

IV. Building Blocks

A. Voltage Controlled Oscillator (VCO)

Choice of VCO architectures falls into two broad categories-LC VCO and Ring oscillators. While LC VCO has good stability characteristics, good long term jitter filtering and low phase noise it requires a huge area, has a very small frequency tuning range and is complex in design. This project was design in CMOS 0.13um technology, hence to achieve a very wide tuning range and to cover all process variations was the main objective of the design. A 4-stage ring oscillator VCO has been designed to operate at a center frequency of 3 GHz. The VCO has been implemented using

the method of interpolation [4]. As shown in Fig. 6, each stage consists of a fast and a slow path whose outputs are summed together. All four stages in the ring are loaded by identical buffers to achieve equal rise and fall times and thus improve the jitter performance. The current source bias circuit is based on a replica of half the buffer stage and a single stage differential amplifier of the NMOS current source so that the voltage at the output of the replicated load element is equal to the control voltage as described in [5]. The amplifier adjusts the current output which is required for correct symmetric load swing limits. The result is that the output current of the NMOS current source is independent of the supply voltage and is established by the load element [5]. As the supply voltage changes, the drain voltage of the NMOS current source device changes however, the gate bias is adjusted by the amplifier to keep the output current constant, counteracting the effect of the finite output impedance [5].

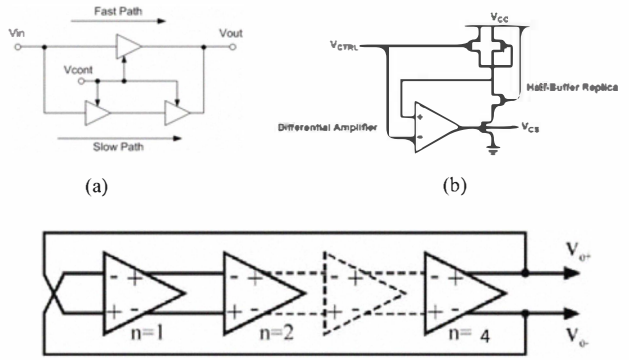
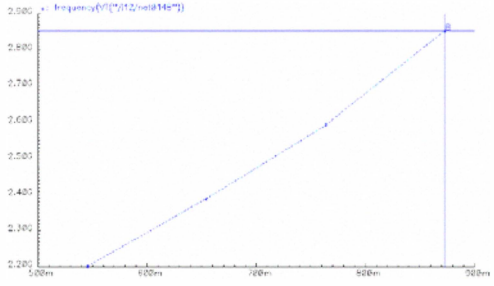


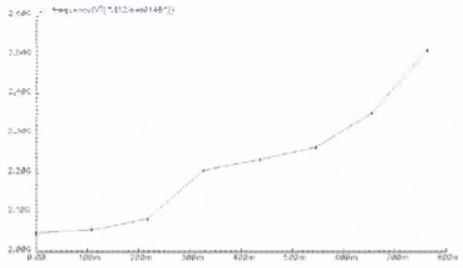
Figure 6. (a) Delay cell of VCO (b) Self Bias circuit

(c) 4- Stage Differential VCO architecture

The VCO of the system is common for both coarse and fine loops. The VCO has differential control voltages and differential output as the rest of the system blocks. A digital buffer chain amplifies the VCO output in order to obtain a rail-to-rail clock output and a high drive capability. The coarse control provides a gain of 2.5 GHz/Volts and the fine control exhibits a gain of 600 MHz/V.



(a)



(b)

Figure 7. VCO gain (a) Coarse Loop Gain 2.5 GH/V (b) Fine loop gain 600MHz/ V

B. Half Rate Phase Detector

For linear phase comparison between data and a half-rate clock, each transition of the data must produce an "error" pulse whose width is equal to the phase difference [4]. Furthermore, to avoid a dead zone in the characteristics, a "reference" pulse must be generated whose area is subtracted from that of the error pulse, thus creating a net value that falls to zero in lock [4].

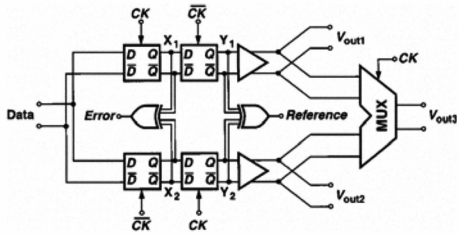


Figure 8. (a) Half Rate Phase Detector (b) Waveforms

The above observations lead to the PD topology shown in Fig. 8. The circuit consists of four latches and two XOR gates. The data is applied to the inputs of two sets of cascaded latches, each cascade constituting a flipflop that retimes the data. Since the flip-flops are driven by a half-rate clock, the two output sequences are the demultiplexed waveforms of the original input sequence if the clock samples the data in the middle of the bit period. It is important to note that the XOR gates in Fig. 8 must be symmetric with respect to their two differential inputs. Otherwise, differences in propagation delays result in systematic phase offsets [4].

C. Charge Pump, Common Mode Feedback and LPF

Fig. 9 shows the implementation of the differential charge Pump used in the fine loop. Both matching and

channel-length modulation of transistors in Fig. 9 impact the residual phase error in locked condition. Thus, their lengths and widths are relatively large to minimize these effects. The circuit receives the differential Error and Reference signals generated by the half rate PD which controls the amount of charge deposited on the low pass filter capacitor node. The design of the fine loop charge pump (CP) has been tweaked from the conventional CP mentioned in [4] in order to reduce the size of the low pass filter capacitor size and achieve optimum damping at the same time. Initially the coarse loop controls the fast path Vp (fast path) and Vn (slow path) of the differential signals to VCO for fast acquisition. Then the fine loop takes over and provides fine adjustment by controlling only the Vn of the differential signaling. This results in better loop stability when the clock is sampling the data in the middle of the data eye. A common-mode feedback (CMFB) circuits has been implemented to sense and correct the differential output of the charge-pump circuit. The passive loop filter is also designed as a fully differential circuit.

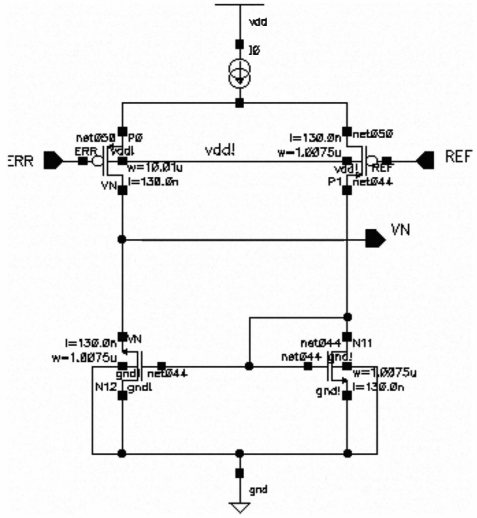


Figure 9. Single ended differential Charge Pump

The closed-loop unity-gain bandwidth is approximated as equation (1) and based on the SATA specifications [4]:

$$_{3\text{-db}} = R.\,K_{vco}.\,K_{pd}.\,G_m \qquad (1)$$

Where Kvco and Kpd are the gains of the VCO and PD, respectively, and Gm denotes the conversion gain of the charge pump. Equation (1) can be used to determine the value of R in low pass filter. The amount of the jitter peaking (JP) in the closed-loop transfer function can be approximated as (2) [4]:

$$JP = 1 + 1/(\ _{3\text{-db}}.R.C) \qquad (2)$$

In order to obtain greater suppression of high-frequency jitter, a second capacitor is added in parallel with the series combination of R and C.

V. Top Level Design Considerations

The top-level layout of the CDR circuit is shown in Fig. 10. Note that the circuit has a very symmetric layout structure, with the VCO, CMFB and the divide-by-16 circuits placed in the center. Coarse-loop and fine-loop controls, as well as the loop filter components are placed on both sides of the symmetry axis. The circuit has an external low pass filter. Analog layout techniques such as VCO interleaving for 50% duty cycle and Guard rings for resistors were implemented

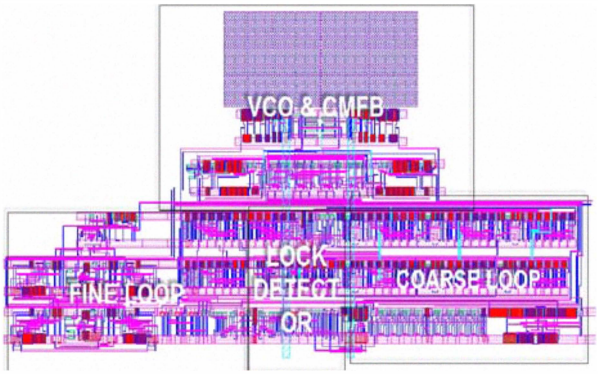
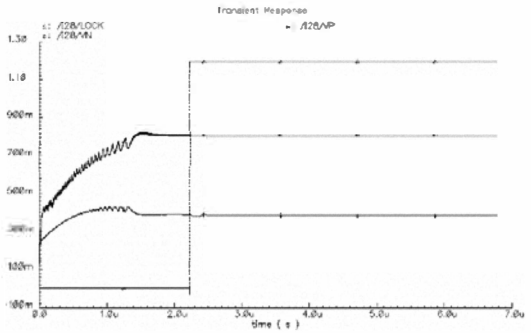


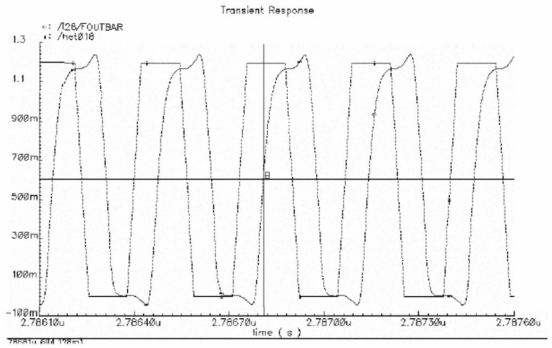
Figure 10. CDR Chip Layout

VI. Experimental Results

Simulation results have been shown for different clock and data rates. Fig. 12(a) shows the control signals to the voltage controlled oscillator (Vp and Vn) and the lock signal. As expected the lock signal is pulled high and the control is passed to the fine loop when the clock frequency of 3 GHz is reached. After the fine loop takes over it provides phase alignment with the input data rate of 6 Gbps. After the fine loop locks, the edges of the clock are in the middle of the data coming from the comparator as shown in figure 12 (b). The error and reference signal are constant as the fine loop acquires lock. Figure 12 (b) shows the recovered data and clock.



(a)



(b)

Figure 11. Simulation waveform for 6.4 Gbps (a) VCO control voltage and Lock Signal (b) Output Data & Clock

The CDR has been implemented using a fully differential charge pump, Phase frequency detector, common mode feedback circuit, Frequency divider VCO and digital lock detector. The coarse loop has been designed to eliminate dead zone region and its operation range is 2.5 GHz to 3.2 GHz. The fine loop has an acquisition range of 200 KHz. The calculated Jitter Tolerance at 2 MHz is 0.15 UI. The calculated Jitter Peaking is 3 dB with Bandwidth of 3.5 MHz and a Duty Cycle of 50 %. The locking time of CDR is 5 us.

VII. SUMMARY

Demand for high speed communication channels has increased steadily in the last decade with advent of high speed internet. This project has presented the design and verification of a monolithic high-speed clock and data recovery circuit with an operation range of 5 -6.4 Gbps. The circuit has been implemented in IBM 0.13 um technology. The overall power consumption is simulated as 20 mW at 3.2 GHz sampling rate. The overall silicon area of the CDR is approximately 108 X 244 um^2 without its loop filter capacitors

ACKNOWLEDGMENT

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