Available online at www.sciencedirect.com
ScienceDirect
ELSEVIER
December 2011, 18(6): 122–126
www.sciencedirect.com/science/journal/10058885
The Journal of China Universities of Posts and Telecommunications
http://jcupt.xsw.bupt.cn

Jitter analysis and modeling of a 10 Gbit/s SerDes CDR and jitter attenuation PLL

WANG Hui[1], CHEN Ying-mei[1] (✉), YI Lv-fan[2], WEN Guan-guo[2]

1. Institute of RF- & OE-ICs, Southeast University, Nanjing 210096, China
2. Zhongxing Telecom Equipment Corporation, Shenzhen 518055, China

Abstract

Jitter analysis and a linear model is proposed in this paper which predicts the characteristics of serial-deserial (SerDes) clock and data recovery circuit, and the characteristics include jitter transfer, jitter tolerance and jitter generation are particularly analyzed. The simulation results of the clock data recovery (CDR) model show that the jitter specifications exceed the mask of ITU-T optical transport network (OTN) G.8251 recommendations. The whole systems are validated by 9.95–11.5 Gbit/s CDR and the jitter attenuation phase locked loops (PLL) circuits using TSMC 65 nm CMOS technology.

Keywords OTN, SerDes, Jitter, CDR, PLL

1 Introduction

Due to the continuous growth of broadband data communications, optical systems have been driven to operate at ten of gigabits per second. SerDes is becoming a main transportation interface technology because it can change the traditional parallel interface technology into serial one. Fig. 1 shows the structure of SerDes in which the CDR is the core part, and the CDR directly impacts on the performances of the deserializing receiver.

The key specifications of clock and data recovery are jitter transfer, jitter tolerance, jitter generation, acquisition time and capture range, among which jitter characteristics are the major and most important CDR specifications [1]. Traditional simulator such as SPICE takes great time and resources of CPU in CDR transistor level circuit design. Moreover, The jitter is incident due to an undesired variation in the time of events at the output of the CDR, and it is difficult to predict with traditional circuit simulators. Therefore the prediction of jitter through justifiable model is necessary and crucial.

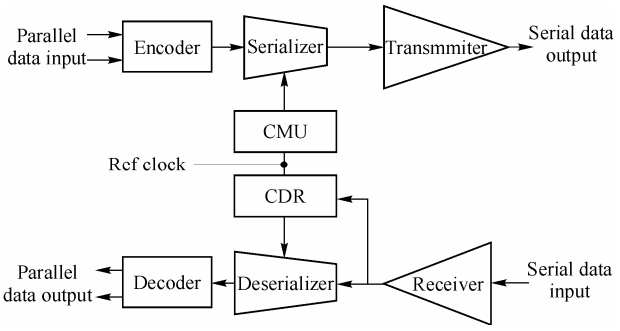


Fig. 1 The architecture of SerDes

The next section of this paper researches the basic jitter characteristics of CDR for SerDes application. Sect. 3 develops the model and simulation results of the CDR, and the jitter specifications exceed the mask of G.8251. Sect. 4 validates the model with CDR circuit using TSMC 65 nm CMOS technology and the last section gives conclusions.

2 Jitter characteristics

The jitter performances of a CDR are commonly characterized by jitter generation, jitter transfer and jitter tolerance. Normally, jitter tolerance and jitter generation are the performance requirements for high speed link CDRs which are used in chip-to-chip communication, and it does not need to meet jitter transfer specification.

Received date: 15-04-2011
Corresponding author: CHEN Ying-mei, E-mail: njcym@seu.edu.cn
DOI: 10.1016/S1005-8885(10)60130-6

However, for those applications where the CDR is used in a repeater, as the case in synchronous optical network (SONET) systems, all three jitter performances are needed [2].

Fig. 2 shows the phase-domain model of a traditional PLL CDR loop. Where k_{PD} is the gain of PFD and CP, I_{noise_PD} is the noise of PFD and CP, K_{VCO} is the tuning gain of VCO and P_{noise} is phase noise of VCO. The phase-domain model allows using of small-signal analysis to better simulate the behavior and performance of CDR circuit.

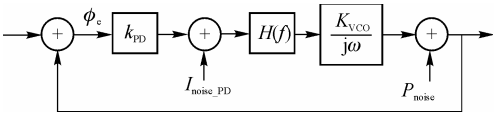


Fig. 2 Phase-domain model of a single CDR loop

The jitter transfer of a CDR circuit represents that how much jitter passes through the system from its input to its output. There are two difficult specifications in jitter transfer which must be met due to the requirement of optical standards such as SONET. One specification is bandwidth, and the other is jitter peaking. The amount of jitter peaking must be less than 0.1 dB. In order to meet the requirement of little jitter peaking, a damping factor above 4–6 must be adopted. We can approach a single-pole response from the following equation:

$$\omega_{BW} \approx 2\zeta\omega_n \tag{1}$$

$$\omega_n = \sqrt{\frac{2I_p K_{VCO}\alpha_{DTD}}{2\pi C_0}} \tag{2}$$

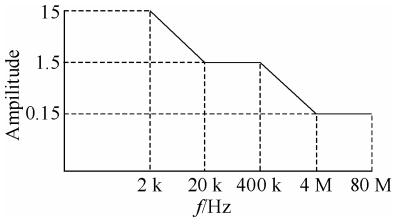
$$\zeta = \frac{R_0 C_0}{2}\omega_n \tag{3}$$

Where ω_{BW} is -3 dB bandwidth of the CDR jitter transfer function, K_{VCO} is the gain of VCO, ω_n is the natural angular frequency, and α_{DTD} is the average data transition density. In Eq. (2), the charge pump current I_p is double due to a Hogge PD so that a current variation of $2I_p$ corresponds to 2π-radians of the data phase [3].

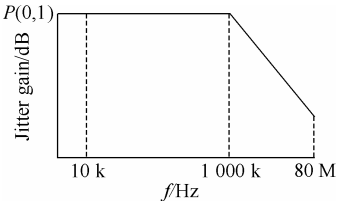
The jitter tolerance measures the ability of a CDR to operate properly when the input contain jitter, and it is usually specified as minimum jitter amplitude that must be tolerated while not exceeding a specific BER. In a PLL CDR, jitter tolerance is defined by the function of the jitter transfer. In order to track high-frequency jitter on the input data, the CDR is desirable to have a large jitter tolerance bandwidth. We can describe the frequency response of jitter tolerance by the following function:

$$G_{JT}(s) = \frac{0.5}{1 - H(s)} \tag{4}$$

From this function, we can recognize an important trade-off between jitter transfer and jitter tolerance in CDR loop design. Figs. 3(a) and (b) show the relevant masks for OTU2 jitter tolerance and jitter transfer. These masks are defined in G.8251 [4]. It is important to note that the 0.15UI corner of jitter tolerance mask is at 4 MHz, while the -3 dB corner frequency of jitter transfer curve is 1 MHz. In order to meet the jitter tolerance mask, the CDR PLL must be designed that the closed-loop bandwidth is higher than the 0.15UI corner frequency of jitter tolerance. However, in this case, the CDR loop cannot meet jitter transfer mask. So the requirements in Fig. 3 suggest that a single CDR loop cannot simultaneously meet jitter tolerance and jitter transfer mask.



(a) Jitter tolerance mask of G.8251



(b) Jitter transfer mask of G.8251

Fig. 3 The jitter masks for OTU2

Jitter generation is the measure of the intrinsic jitter produced by the CDR. The traditional way of predicting jitter generation is to calculate the width of the probability density function of the total jitter in an RMS sense. The sources of jitter in CDR circuit can be abstracted as following:

1) VCO phase noise.

2) Frequency modulation resulting from ripple on the VCO control voltage.

3) Supply and substrate noise.

4) Coupling of data transition.

3 Modeling and simulation results of CDR and jitter attenuation PLL

According to the above analysis of jitter characteristic, we find that a single CDR loop cannot simultaneously meet jitter transfer and jitter tolerance mask of G.8251. There are several ways to solve this problem, such as using DPLL structure [5–7] which needs high delay gain to decouple the jitter transfer and jitter tolerance corner frequencies. Another scheme is to introduce a jitter-tolerance-enhanced CDR using a GDCO-based phase detector but which cannot meet jitter peaking [8].

As is the case with PLL, the jitter transfer exhibits a low-pass characteristic. So in general PLL CDR, we focus on meeting jitter tolerance, and we need additional low-pass filtering on the recovery clock for jitter transfer. Due to those analyses, we design the architecture of a CDR and an additional jitter attenuation PLL as shown in Fig. 4. The CDR PLL employs a dual-loop architecture which includes a frequency-acquisition loop and a phase-acquisition loop. When the frequency error drops to a sufficiently small value, lock detector disable frequency-acquisition loop and enable phase-acquisition loop.

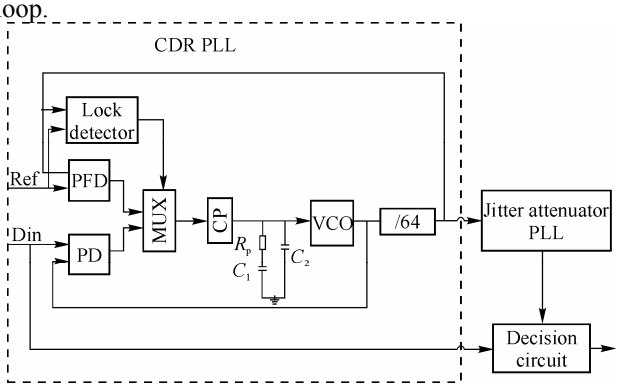


Fig. 4 Architecture of the CDR and jitter attenuation PLL

The bandwidth of this CDR PLL is designed to be above 4 MHz in order to meet jitter tolerance mask. An additional jitter attenuation PLL is used to meet jitter transfer specification, and it is a traditional second order PLL whose bandwidth is set to be below 1 MHz. Fig. 5 gives the structure of jitter attenuation PLL.

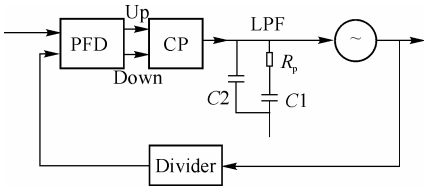


Fig. 5 The structure of the jitter attenuation PLL

Fig. 6 is the phase-domain model of CDR and jitter attenuation PLL. According to this model, a first-pass design of system and circuit parameters such as closed-loop bandwidth, charge-pump current and loop-filter component can be acquired.

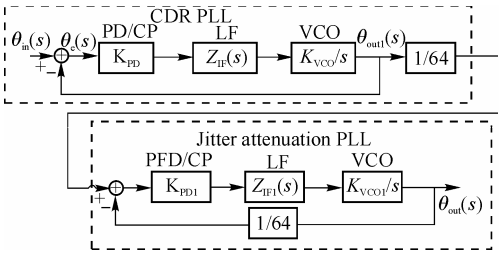


Fig. 6 The model of CDR and jitter attenuation PLL

The CDR PLL loop transfer function is as follows:

$$H_1(s)=\frac{\theta_{out1}(s)}{\theta_{in}(s)}=\frac{K_{PD}K_{VCO}Z_{LF}(s)}{s+K_{PD}K_{VCO}Z_{LF}(s)} \tag{5}$$

Also the transfer function of jitter attenuation PLL is:

$$H_2(s)=\frac{\dfrac{\theta_{out}(s)}{\theta_{out1}(s)}}{64}=\frac{K_{PD1}K_{VCO1}Z_{LF1}(s)}{s+\dfrac{K_{PD1}K_{VCO1}Z_{LF1}(s)}{64}} \tag{6}$$

Then the whole system transfer function can be obtained:

$$H(s)=\frac{K_{PD}K_{VCO}Z_{LF}(s)}{s+K_{PD}K_{VCO}Z_{LF}(s)}\frac{K_{PD1}K_{VCO1}Z_{LF1}(s)}{64s+K_{PD1}K_{VCO1}Z_{LF1}(s)} \tag{7}$$

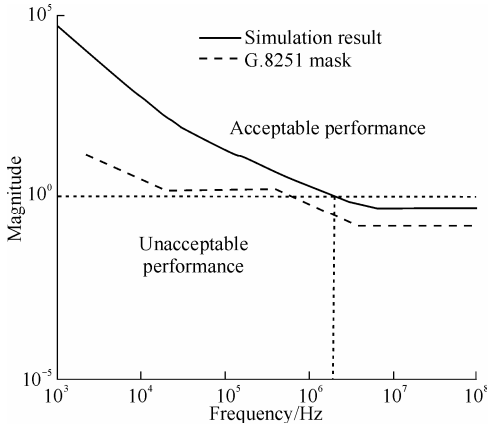
Jitter tolerance specification requires the bandwidth of CDR loop to be above 4 MHz. However, the loop bandwidth must be little in order to suppress the input data jitter as a result of the low-pass characteristic, so the bandwidth of CDR loop is defined at the range of 4 MHz–5 MHz. The Eq. (7) shows that the whole system transfer function is the multiplication of two loops. So jitter peaking of each loop must be designed much less than 0.1 dB, only in this way the jitter peaking of the whole system can meet G.8521 mask. The little jitter peaking constraint demands careful attention to the poles and zeros of transfer function.

The loop parameters can be calculated through Matlab simulation soft as shown in Table 1:

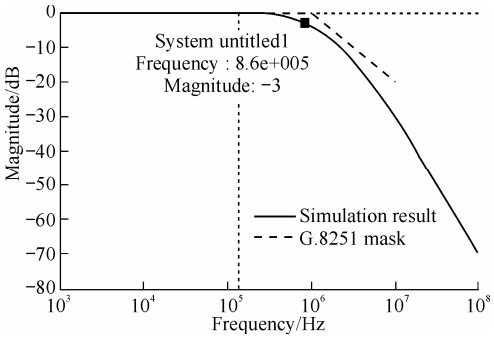
Table 1 Parameters of the whole system

Parameters	CDR PLL	Jitter attenuation PLL
K_{VCO} (MHz·V^{-1})	550–720	550–720
I_p / μA	80	80
C_1/nF	15	6
C_2/pF	20	15
R_p / Ω	400	6 500
Bandwidth/MHz	4.3	0.9

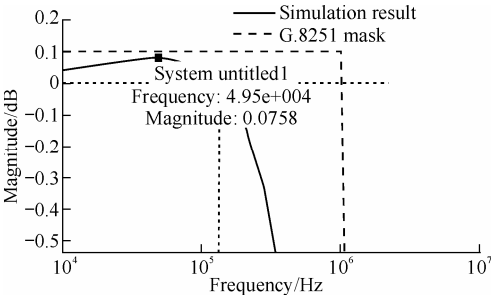
To test and verify the calculated parameters, we use Matlab linear analysis tools to simulate the jitter tolerance and jitter transfer of the whole system as showed in Fig. 7. In Fig. 7(a), the dotted line is G.8251 mask for jitter tolerance, and the simulation result is above the mask. So the result suffice G.8251 standard. Fig. 7(b) shows the jitter transfer simulation result, and its bandwidth is 860 kHz which meet the requirement of 1 MHz bandwidth. Another requirement of jitter transfer is jitter peaking, and Fig. 7(c) shows that the jitter peaking is 0.075 8 dB which is less than 0.1 dB.



(a) Jitter tolerance



(b) Jitter transfer bandwidth



(c) Jitter peaking

Fig. 7 Simulation results

In order to get jitter generation, a time-domain behavioral level simulation must be developed. Fig. 8 shows the simulation results of jitter generation. The retimed data exhibits a peak-to-peak jitter of 1.089 ps with a 10 Gbit/s data input, and its RMS jitter is 0.291 5 ps.

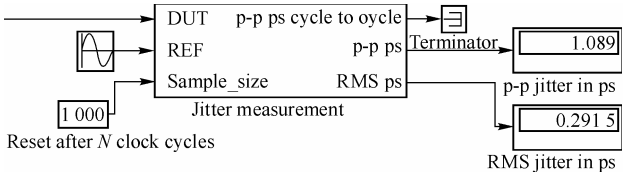


Fig. 8 Simulation results of jitter generation

4 Circuit implemention

The transistor level design using TSMC 65 nm CMOS technology based on the above analysis and the simulation results have been given. The data input is expected to be a non-return-to-zero (NRZ) data pattern at a rate between 9.95 and 11.5 Gbit/s. The CDR PLL employs a dual-loop architecture in which the frequency-acquisition loop is used to lock the output frequency to the reference-clock frequency as shown in Fig. 4. When the output frequency of the CDR PLL is within 1 200 ppm of the reference clock, lock detector will switch the frequency-acquisition loop to the phase-acquisition loop which utilizes a basic Hogge PD. The 10 GHz VCO, charge pump, and loop filter are shared between the frequency-acquisition and phase- acquisition loops. The jitter attenuation PLL which is added to meet jitter transfer mask includes the 10 GHz VCO, off-chip loop filter, PFD, charge pump, and divider.

Fig. 9 shows the layout of the CDR and jitter attenuation PLL. The whole chip occupies an area of 0.87 5 mm× 0.97 5 mm. The whole system consumes 72 mW power from a 1 V supply excluding output buffers.

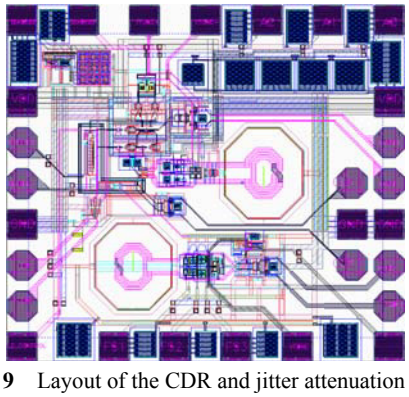


Fig. 9 Layout of the CDR and jitter attenuation PLL

Fig. 10 depicts the eye diagram of the recovered full-rate retimed date (11.2 Gbit/s) with 5×10^{-17} F load

capacitance. The retimed data exhibits 280 mV output swing and a peak to peak jitter of 2.3 ps. G.8251 specifies 0.15 unit interval (UI) as the maximum peak-to-peak jitter on recovered data, and the simulation results meet the requirements of G.8251.

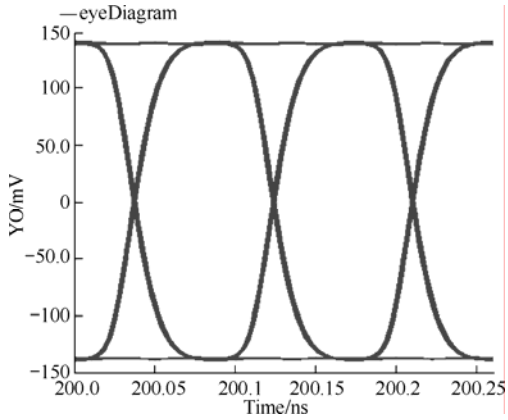


Fig. 10 Eye diagram of the recovered data

Fig. 11 shows eye diagram of the recovery clock, exhibiting a peak to peak jitter of 5.17 ps. G.8251 specifies 0.1UI as the maximum peak-to-peak jitter on the recovery clock, and the measured jitter meet the requirements of G.8251.

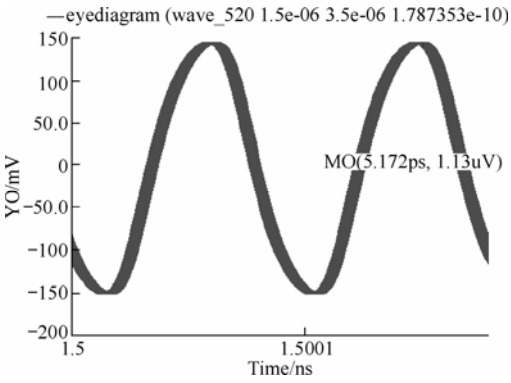


Fig. 11 Eye diagram of the recovery clock

5 Conclusions

This paper demonstrates a linear model of 9.95–11.5 Gbit/s CDR and the detailed jitter analysis results. To simultaneously meet jitter tolerance and jitter transfer specifications defined in G.8251 of optical transport network, an additional jitter attenuation PLL is introduced. The simulation results are validated by 10 Gbit/s CDR and jitter attenuation PLL circuits using TSMC 65 nm CMOS technology. The jitter performance of the recovered data and clock meet the requirements of G.8251.

Acknowledgements

This work was supported by the National Natural Science Foundation of China (60976029), and the Research Foundation of Zhongxing Telecom Equipment Corporation.

References

1. Frequency agile jitter measurement system. Application Note 1267. Santa Clara, CA, USA: Agilent Technologies. 2005
2. Razavi B. Design of integrated circuits for optical communications. New York, NY, USA: McGraw Hill, 2003
3. Greshishchev Y M, Schvan P. SiGe clock and data recovery IC with linear-type PLL for 10-Gb/s SONET application. IEEE Journal of Solid-State Circuits, 2000, 35(9): 1353–1359
4. ITU-T G.8251. The control of jitter and wander within the optical transport network. 2001
5. Lee T, Bulzacchelli J. A 155-MHz clock recovery delay-and phase-locked loop. IEEE Journal of Solid-State Circuits, 1992, 27(12): 1736–1746
6. Dalton D, Chai K, Evans E, et al. A 12.5 Mb/s to 2.7Gb/s continuous-rate CDR with automatic frequency acquisition and data-rate readback. IEEE Journal of Solid-State Circuits, 2005, 40(12): 2713–2725
7. Kenney J, Dalton D, Eskiyerli M, et al. A 9.95 to 11.1 Gb/s XFP transceiver in 0.13-μm/spl μm/m CMOS. Proceedings of the IEEE International Solid-State Circuits Conference, Digest of Technical Papers (ISSCC'06), Feb 6–9, 2006, San Francisco, CA, USA. Piscataway, NJ, USA: IEEE , 2006: 864–873
8. Liang C F, Hwu S C, Liu S I. A jitter-tolerance-enhanced CDR using a GDCO-based phase detector. IEEE Journal of Solid-State Circuits, 2008, 43(5): 1217–1226

(Editor: ZHANG Ying)