(a) hit: write back 写到 cache. 脏数据写回内存

miss: write allocate 读到 cache. 再写

total cycle = 读到cache 读到cache
$3\times100 + 3\times1 + 100 + 100 = 503$

(b) cache line size = 16 bytes

total cycle = $\frac{1}{4}\times3\times100 + 3\times1 + \frac{1}{4}\times100 + 100 = 203$

(c) cache line size = 64 bytes

total cycle = $\frac{1}{16}\times3\times100 + 3\times1 + \frac{1}{16}\times100 + 100 = 103 + \frac{400}{16} = 128$

(d) direct-mapped. size: 2048 bytes miss rate 为 1

average cycle = $3\times100 + 3\times1 + 100 + 100 = 503$