Dark Current in Silicon Photomultiplier Pixels: Data and Model

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***Abstract*—The dark current behavior of the pixels forming the Si photomultiplier as a function of the applied overvoltage and operation temperature is studied. The data are modeled by assuming that dark current is caused by current pulses triggered by events of diffusion of single minority carriers injected from the peripheral boundaries of the active area depletion layer and by thermal emission of carriers from Shockley–Read–Hall defects in the active area depletion layer.**

***Index Terms*—Dark count (DC) rate, dark current, gain, silicon photomultiplier (PM) (SiPM), single pixels, temperature.**

I. Introduction

SILICON PHOTOMULTIPLIERS (PMs) (SiPMs) are a very promising alternative to conventional vacuum tube PMs: They are insensitive to magnetic fields; hence, they can be used in environments with high fields. Their operation voltage is far lower than PMs, and they ensure better robustness and reliability and are much cheaper than their traditional counterpart [1], [2].

SiPM structure consists in a parallel array of equal single pixels, each one made up of a silicon p-n junction avalanche photodetector with an integrated resistor. The SiPM is biased above the breakdown (BD) voltage $V_{\rm BD}$ of the p-n junction, i.e., each pixel is operated in Geiger mode. The junction is carefully doped in order to have an avalanche BD (not Zener) only in the central active area of the pixel, used for the photon detection. To understand the single photon detection concept, let us assume to bias such junction above BD with a fast voltage step. In this condition, if no carrier is present in the depletion region, the junction is highly sensitive to the detection of single photons. In fact, if the photon is absorbed by creating an electron–hole (e–h) pair, both carriers will start to drift in the high-field region of the depletion layer, and being the voltage above BD, this drift will result with a 100% probability in the impact generation of a second e–h pair, and so on, up to the buildup of the junction avalanche. The avalanche is limited by the buildup of a limiting space charge in the depletion layer which decreases the field [3]. Moreover, since the photodetector has a resistor in series, when the avalanche current flows through the resistor, the voltage applied to the junction drops below $V_{\rm BD}$. This quenches the avalanche; thus, the current decreases to zero, and the voltage across the p-n junction increases again above $V_{\rm BD}$. The pixel is then ready to detect the arrival of a new photon. Clearly, all the transients recorded are the result of both capacitive and (generally faster) avalanche buildup characteristic times.

Such ideal picture is strongly modified by the occurrence of phenomena leading to dark current, generally attributed to generation effects from Shockley–Read–Hall (SRH) defects in the depletion layer, afterpulsing effects, and diffusion of carriers from the quasi-neutral boundaries of the p-n junction [4].

The purpose of this work is to understand the behavior of dark current in single pixels of SiPMs, by separately taking into account the contribution given by the avalanche buildup and quenching and the effect of generation/diffusion of carriers in the depletion layer, in order to provide a detailed understanding of the current–voltage (I–V) curves. We propose a physical model of the I–V above BD, able to reproduce the voltage and temperature dependences of the current for the studied devices.

II. Experimental Setup

A. Device Description

Devices were fabricated by STMicroelectronics on silicon n-type wafers in order to improve the photon-timing resolution. In fact, the additional epilayer–substrate p-n junction that will be formed, if polarized, prevents the photogenerated carriers in the substrate to reach the epilayer [5]. The implanted p^+ region on the p-type epitaxial layer forms an enrichment region which defines both the active area and the BD voltage $V_{\rm BD}$ of the p-n junction. n-type implanted guard rings prevent lateral BD [6]. The p^+ epitaxial buried layer forms a low-resistive path to the lateral anode ohmic contact. Sinkers created around the photodiode active area by means of a high-dose boron implantation form the anode contacts. The cathode is realized by diffusion of arsenic from an *in situ* doped thin polysilicon layer deposited on the top of the structure. The quenching resistor, made of lightly doped polysilicon, is integrated on the cathode of the pixel itself. Deep optical trenches filled with oxide and metal surround the pixel active area in order to reduce electro-optical coupling effects (crosstalk) between adjacent microcells.

Manuscript received February 8, 2012; revised May 10, 2012; accepted June 15, 2012. Date of current version August 17, 2012. This work was supported in part by IMS R&D, STMicroelectronics under Grant CDR.ST.CNR-IMM.MATIS.24.02.2010.002. The review of this paper was arranged by Editor J. R. Tower.

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Digital Object Identifier 10.1109/TED.2012.2205689

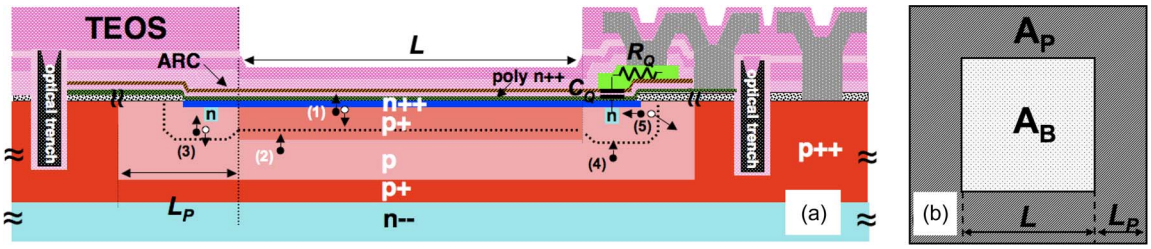

Fig. 1. (a) Schematic cross section of the SiPM pixel described in the text. The dotted line is the boundary of the depleted region. L is the active area length, and L_P is the perimeter length extension. (1)–(5) are the current components. (b) Front-side view of the SiPM pixel. A_B and A_P are the active and the perimeter areas of the pixel, respectively.

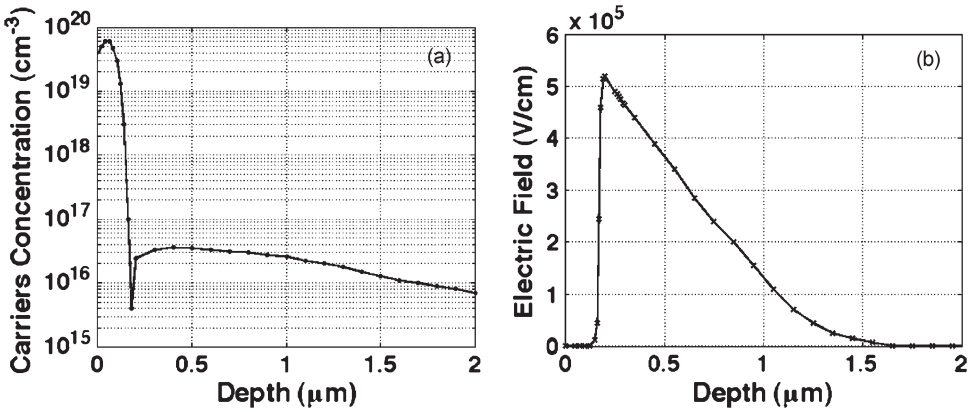

Fig. 2. (a) SRP measurement of the final doping concentration and (b) simulated electric field, at reverse bias of −30 V, of the SiPM pixel along the vertical dimension in the active volume.

A double-layer antireflective coating, made of silicon oxide and silicon nitride, enhances the spectral response of the device in the blue and near ultraviolet wavelength ranges. The pixels have a square geometry with an active area of $40 \times 40\ \mu\text{m}^2$ [7]. Fig. 1(a) shows a schematic drawing of the pixel cross section. The dotted line indicates the boundaries of the depleted region. The depletion region relevant for photon detection is the one below the enrichment layer, where the field is higher, being the doping level larger than in the perimeter area. The numbers [from (1) to (5)] shown in the figure refer to the current components and will be explained after. Fig. 1(b) shows a front-side view of the pixel.

Fig. 2(a) shows the vertical dopant concentration profile in the cell for the first 2-μm Si layer below the Si/SiO_2 interface in the active region as measured by spreading resistance profiling (SRP). Fig. 2(b) shows the electric field profile for a reverse polarization of −30 V, i.e., 2 V above the BD voltage, as calculated by using the ATLAS—SILVACO simulation software. The maximum peak of the electric field is located at $\sim$0.2 μm from the Si/SiO_2 interface, i.e., at the metallurgical junction.

B. Measurement Setup

Electrical characterization was performed at wafer level using a Cascade Microtech Probe Station *11000*. The probe was shielded from visible electromagnetic radiation by means of a dark plastic cover so as to provide the required dark condition. The samples were cooled using a Temptronic *TPO 3200A* ThermoChuck that can provide a stabilized temperature between −60 °C and 200 °C. Current versus voltage measurements were acquired using an *HP 4156B* precision semiconductor parameter analyzer using an integration time of 1 s, sufficient to correctly measure the current even at low temperature.

The dynamic current, i.e., the current versus time trace, was obtained using a Tektronix *DPO 7104* Digital Oscilloscope with 1-GHz bandwidth and 20 GSa/s working in average mode. The pixel was reverse biased by applying a constant negative voltage larger than the V_{BD} to the anode contact using the *HP4156B*. The current is measured through the voltage drop across a 50-Ω series resistance R_S, i.e., the oscilloscope input impedance, connected to the device under test.

The dark count (DC) rate was measured using the experimental setup discussed earlier. It is defined as the average number of dark pulses of amplitude exceeding half of the mean dark pulse amplitude (see Figs. 4 and 5) in a time interval of 1 s.

III. Reverse Static Characteristics

The current–voltage curves of 30 devices consisting in SiPM single pixels with active area of $40 \times 40\ \mu\text{m}^2$, distributed in a 6-in wafer, reverse biased from 0 to −40 V, in dark, at 25 °C are shown in Fig. 3. The mean BD voltage V_{BD} is -28.3 ± 0.2 V. In general, the I–V characteristics show excellent reproducibility, denoting a remarkable uniformity over the whole wafer area. As an example, the dark current for a bias voltage of −30 V has a mean value of 1.1 ± 0.3 nA.

The I–V curves in reverse bias are characterized by three distinct regions. The first, which extends from 0 V up to V_{BD} and is referred to as "*leakage current*" in the following, is on the order of 10 fA at 25 °C. It consists of different geometrical components [8]: the area component I_A, the perimeter leakage current I_P, and a possible corner contribution I_C. The area

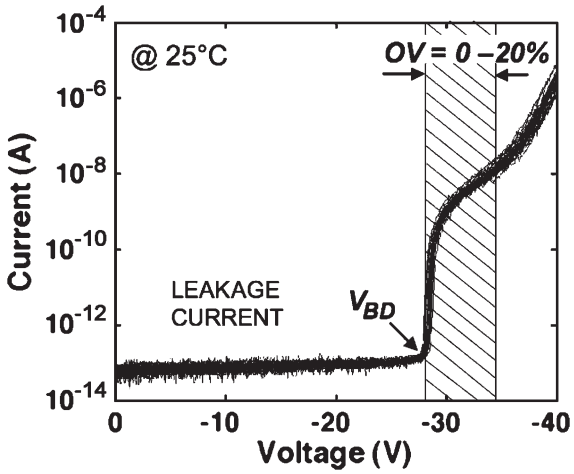

Fig. 3. I–V characteristics in reverse polarization of 30 pixels distributed in a 6-in wafer at 25 °C. The mean $V_{\rm BD}$ is −28.35 V.

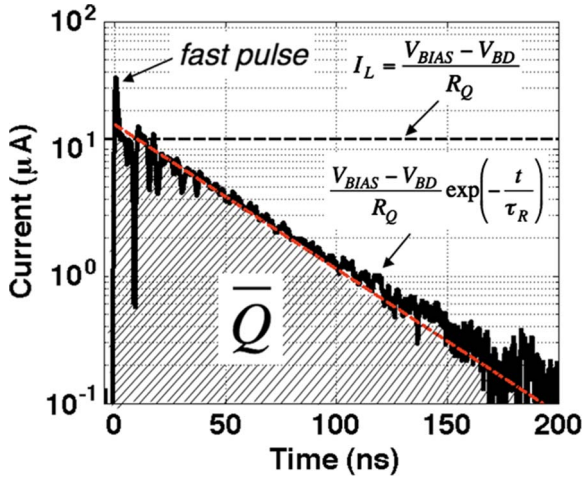

Fig. 4. Dark pulse at room temperature. I_L is the latch current (see text). The red dashed line is the recharging current expressed by (2). The shaded area is the mean charge delivered in a dark pulse.

component I_A depends on both generated carriers and diffused carriers in the bulk [components are indicated as (1) and (2), respectively, in Fig. 1(a)], while the perimeter leakage I_P consists of peripheral bulk generation, a peripheral diffusion, and a surface generation current at Si-SiO_2 interface [9] [components are indicated as (3)–(5), respectively, in Fig. 1(a)]. The leakage current below $V_{\rm BD}$ is completely dominated by the perimeter component, and it is uncorrelated to that leading to the current above $V_{\rm BD}$, as it will be demonstrated in the following. It is important to underline now that this current clearly is not in a multiplication regime due to avalanche, since, below $V_{\rm BD}$, the electric field in the depletion layer is everywhere well below the critical BD field.

The second region is the most interesting voltage range for the single photon detection application, which is the focus of this paper. At room temperature, it extends from −28 to −34 V and corresponds to 0%–20% of the OV defined as $OV = (V_{\rm BIAS} - V_{\rm BD})/V_{\rm BD}$, where $V_{\rm BIAS}$ is the externally applied bias voltage. It is interesting to note that, in this region, the dark current as a function of the bias voltage is characterized by a cubic growth.

In this region, the static current–voltage characteristics can be modeled as the mean charge (Q) delivered per pulse times the frequency of pulses. The former divided by the elementary charge (q) is the mean gain $(G = Q/q)$, while the latter is the *DC* rate of the single pixel. The current is, then, given by

$$I = Q \cdot DC = q \cdot G \cdot DC. \tag{1}$$

Depending on both the mean gain and the DC rate behavior with respect to the bias voltage, the static current–voltage characteristics show a defined shape. In the tested devices, as we will discuss in the following, the mean gain has a parabolic dependence on the bias voltage, while the DC is linear; therefore, the product of these two terms explains the cubic dependence of the current with respect to the applied voltage in this region.

At bias voltages larger than −34 V (third region in the I–V curve), the current increases more rapidly than a cubic law. This is mainly due to the increase of the afterpulsing (see after) and to the inefficiency of the quenching mechanism at such high voltages. In fact, at high voltages, secondary carriers generated during the primary avalanche cascade can be trapped in shallow levels and then rapidly detrapped triggering a new avalanche discharge, because of the high electric field in the depleted region, before the bias across the junction is restored to the supply voltage. This phenomenon, referred to as afterpulsing in the literature, produces, in our devices, above −34 V, a consistent increase in the DC term. Moreover, the quenching mechanism due to the series resistance may not be totally efficient at higher voltages. In fact, at high voltages, the time needed to quench the avalanche increases; hence, the avalanche current is self-sustaining for a longer period [10], thus producing a distorted pulse and a higher mean charge. This implies an increase of the mean gain, with a voltage dependence more than cubic, as experimentally observed.

IV. Gain Derivation From Dark Pulses

Fig. 4 shows in a semilogarithmic scale the average of 1000 dark current pulses stored by the digital oscilloscope at 25 °C and at $V_{\rm BIAS} = -31$ V.

The measured signal presents a fast pulse (having a duration of a few nanoseconds) and a slow exponential decrease. The fast pulse is related to the presence of a number of phenomena. First, in the depletion layer region where the electric field is above the critical BD field, in correspondence with the device active area, the avalanche process will build up creating a space charge region and/or a decrease of the depletion layer charge which will decrease the field below the critical BD field. It will occur in a time constant on the order of the transit time, i.e., W/v_s with W as the depletion layer width and v_s as saturation velocity $(W/v_s \cong 20$ ps). Second, such discharge lowers the voltage across the junction capacitance C_D and discharges the parasitic capacitance C_Q in parallel to the quenching resistance R_Q. Indeed, the polysilicon quenching resistance lays on top of the junction area [see Fig. 1(a)]; thus, a direct capacitive coupling exists between the resistor itself and the diode [11], [12], resulting in the parasitic C_Q. During

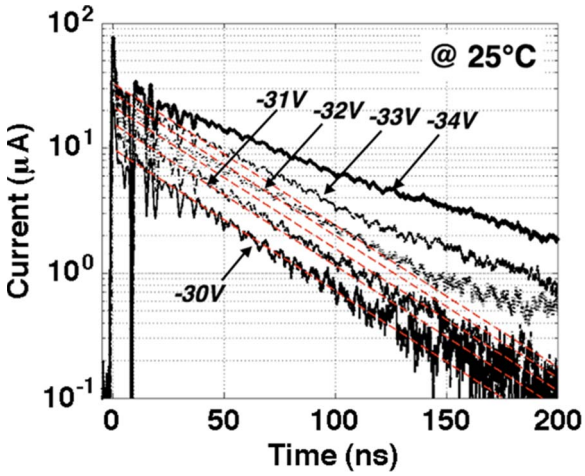

Fig. 5. Dark pulses at room temperature as a function of the bias voltage. Red dashed lines are the recharging current expressed by (2).

the avalanche process, C_Q discharges through the diode series resistance R_D, thus providing a fast pulse governed by the time constant $R_D C_Q$. At 25 °C, R_D is estimated to be at least 1 kΩ or more, and $C_Q \sim 20$ fF giving a time constant of ∼20 ps. Hence, the avalanche buildup in the space charge region and the discharge of C_Q will require approximately 0.1 ns to take place. Since our time resolution is of about 1 ns, the pixel discharge is expected to be detected as a current peak of amplitude $C_D \times (V_{\rm BIAS} - V_{\rm BD})/1$ ns ≈ 160 μA. The peak current actually observed (see Fig. 4) is lower (40 μA), and this discrepancy can be attributed to inductive effects in the circuit setup.

When the current reaches the level $I_L = (V_{\rm BIAS} - V_{\rm BD})/R_Q$ (dashed line in Fig. 4), the avalanche process is quenched, and the pixel capacitance starts recharging through R_Q with the time constant $\tau_R = C_D \cdot R_Q \sim 37$ ns (R_Q is ∼220 kΩ at 25 °C and C_D is ∼170 fF as determined by capacitance–voltage measurements [13]). Fig. 4 also shows (dashed red line) the theoretical recharging current I_R, according to the equation

$$I_R(t) = \frac{V_{\rm BIAS} - V_{\rm BD}}{R_Q} \exp\left(-\frac{t}{\tau_R}\right). \qquad (2)$$

After $\sim 3\tau_R$ (∼110 ns at 25 °C), the diode capacitance is fully recharged. The pixel therefore returns in quiescent state biased above $V_{\rm BD}$ with a trascurable current (ideally zero) flowing until a new free carrier triggers a new avalanche.

The area subtended by the dark current pulse in such time window is the mean gain of the pixel. The described behavior was observed at lower overvoltages for temperatures ranging from −25 °C to 65 °C. At higher bias voltages, the slope of the recharging phase deviates from the exponential law of (2), showing a higher recharging time constant. This effect is clearly visible in Fig. 5, where the mean current pulses at 25 °C for bias voltages from −30 to −34 V are shown. The recharging phase is perfectly described by (2) (dashed red lines) with a time constant $\tau_R = C_D \cdot R_Q$ up to $V_{\rm BIAS} = -31$ V ($OV = 3$ V). At higher OV, the probability for the first dark pulse to be followed by a secondary pulse with lower amplitude increases. The

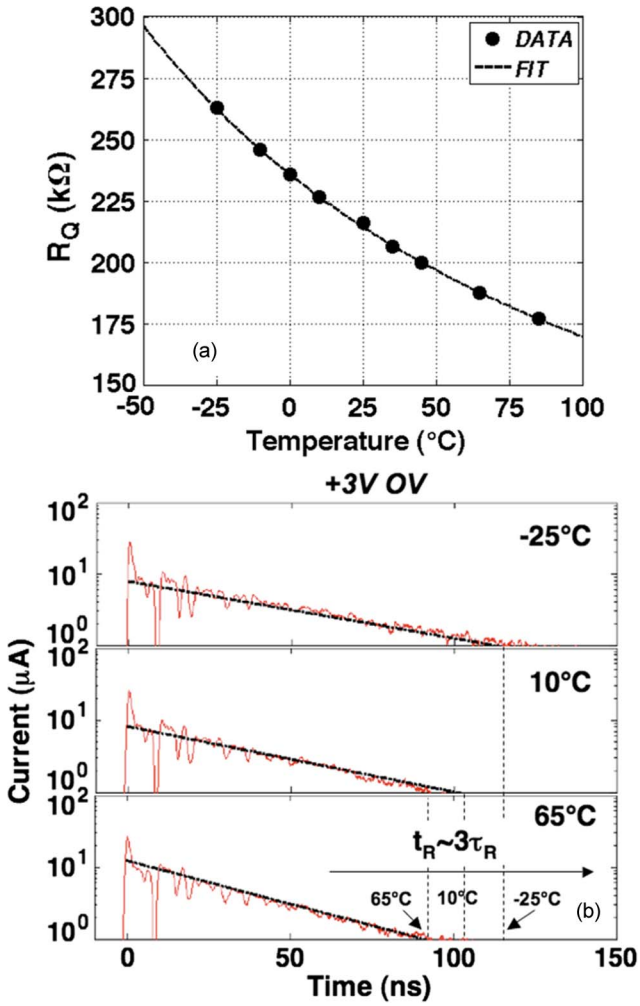

Fig. 6. (a) Quenching resistance as a function of the temperature of a pixel of SiPM. Dashed line is exponential fit of the experimental data. (b) Dark Pulses versus temperature at constant 3 V of OV and three different temperatures: (Up) −25 °C, (center) 10 °C, and (bottom) 65 °C. Dashed lines are the recharging current expressed by (2). The recharging time (t_R) is lower at high temperature due to the R_Q decrease.

afterpulsing probability is known to increase with the OV [4] thus producing a mean average recharging time dependent on the bias. It is to be noted that this is an apparent recharging time, due to the effect of averaging the signal stored by the oscilloscope. The resulting gain is, therefore, the mean gain produced by the first free carrier that initiates the avalanche. The gain exhibits a linear dependence from voltage, as reported in the literature [14]–[16] and as described by the equation $G = C_D\ (V_{\rm BIAS} - V_{\rm BD})/q$. If secondary effects take place (e.g., afterpulsing and/or crosstalk), the gain trend is not linear anymore, but it is superlinear, as discussed in [17].

The recharging time constant τ_R of the pixel is also temperature dependent. Indeed, it is well known that a resistance made with a polysilicon layer decreases exponentially as the operation temperature increases [18]. The experimental R_Q, measured from the forward $I-V$ characteristics of the pixel, as explained in [7], for temperatures ranging from −25 °C to 65 °C, is shown in Fig. 6(a). The dashed black line is the exponential fit of the measured R_Q. At 25 °C, $R_Q \sim 220$ kΩ.

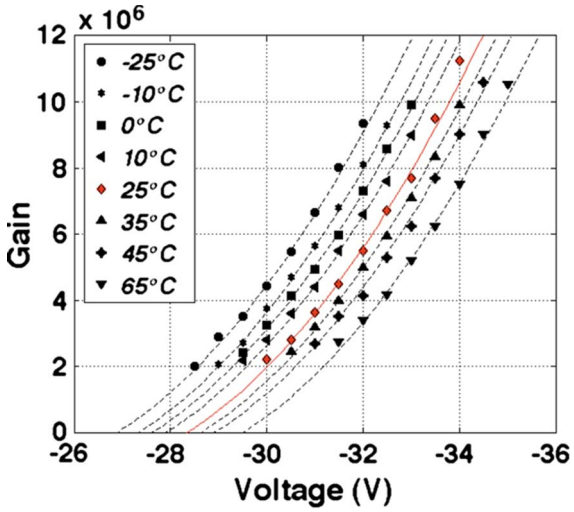

Fig. 7. Experimental mean gain of the pixel as a function of the bias voltage for different temperatures ranging from (circles) −25 °C up to (downward triangles) 65 °C. Dashed lines are the quadratic fits of the data.

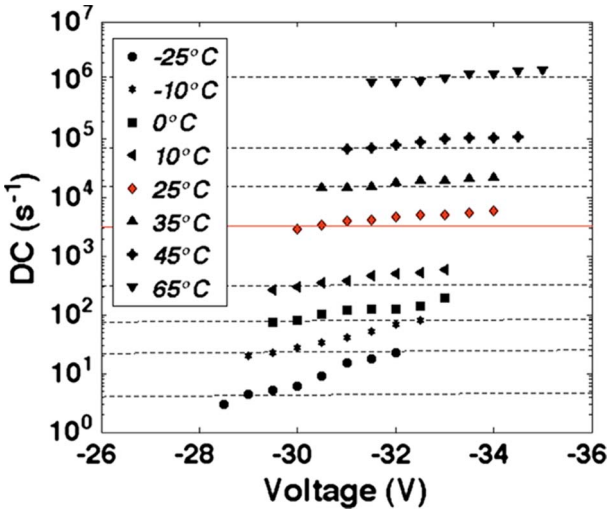

Fig. 8. (Symbols) DCs and (dashed lines) model from (6) as a function of the temperature and voltage for an SiPM pixel.

The reduction of R_Q in the measured temperature range ($\sim$75 kΩ) produces a lowering of the pixel recharging time ($t_R \sim 3^* \tau_R$) from $\sim$135 ns at −25 °C to $\sim$95 ns at 65 °C. In Fig. 6(b), the mean dark pulses at three different temperatures (−25 °C, 10 °C, and 65 °C, going from up to down in the figure) and at the same OV (+3 V) are compared. The relatively low OV value was chosen in order to avoid afterpulsing effects. The dashed black lines are the recharging current given by (2) providing the corresponding t_R values.

The pixel mean gain $\overline{G}$ can be evaluated as the integral of the mean dark current pulses per electron charge q, in the time windows from zero to t_R as a function of the temperature and at different $V_{\rm BIAS}$'s. Fig. 7 shows the results obtained for temperatures ranging from −25 °C up to 65 °C and for different bias voltages. $\overline{G}$ shows a superlinear behavior with respect to the bias. Indeed, by increasing the voltage, the afterpulse probability increases, thus leading to a longer mean recharging time constant and the consequent superlinear behavior of the gain with respect to the bias voltage. In particular, $\overline{G}$ is well fitted by the same quadratic function in the full temperature range studied (dashed lines) rigidly shifted with respect to the voltage, to take into account the $V_{\rm BD}$ shift with temperature (−29 mV/°C). In fact, for the same bias, the gain decreases with temperature since higher energy is required for impact ionization due to the larger electron–phonon energy loss. The same voltage dependence of $\overline{G}$ was found measuring the gain with independent methods, as reported in [19] and [20].

V. DCs and Dark Currents

The other device parameters that we studied were the DC rate and the dark currents of the single pixels. The DC rate at OV ranging from 0% to 20% and temperatures from −25 °C to 65 °C is shown in Fig. 8. The DC varies from 10 s^{-1} at −25 °C (circles) to 10^6 s^{-1} at 65 °C (downward triangles). The DC temperature dependence is very strong, while on the contrary, the dependence on voltage is relatively weak. Fig. 8 also shows (dashed lines) the calculated DC behavior as a function of voltage and temperature according to a model described hereinafter.

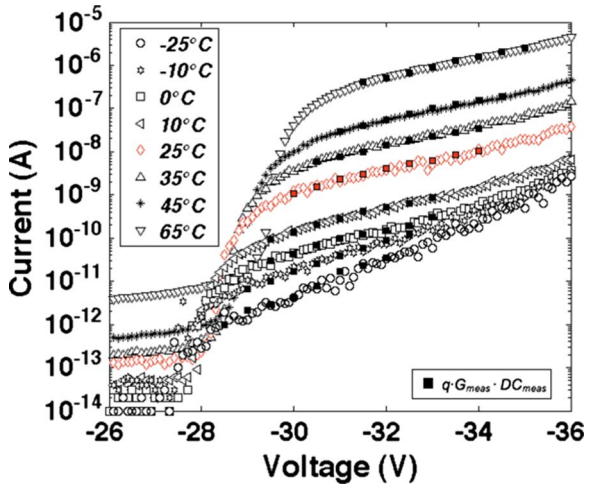

Fig. 9. (Open symbols) Dark current and (filled squares) experimental model (see text) of (1) of an SiPM pixel. In red, the data at room temperature are plotted.

As discussed earlier (1), in the operative-voltage range (0%–20% OV), the dark current of a pixel can be modeled as the product of the average charge delivered during the pixel discharge and the recharge $Q = q \cdot G$ times the average DC.

The experimental validation of this model is shown in Fig. 9, which reports the measured pixel dark current for temperatures ranging from −25 °C up to 65 °C in the operative-voltage range (open symbols) compared with the model of (1) (filled squares), where $G_{\rm meas}$ and $DC_{\rm meas}$ are the experimental gain and DC of Figs. 7 and 8, respectively.

We note that an excellent match between the model of (1) (squares) and the experimental dark current in the full temperature and voltage ranges was explored.

From such observation, we can conclude that, as an example, by measuring only the dark currents and the gain as a function of voltage and temperature, it is possible to extract the voltage and temperature dependences of the DC rate.

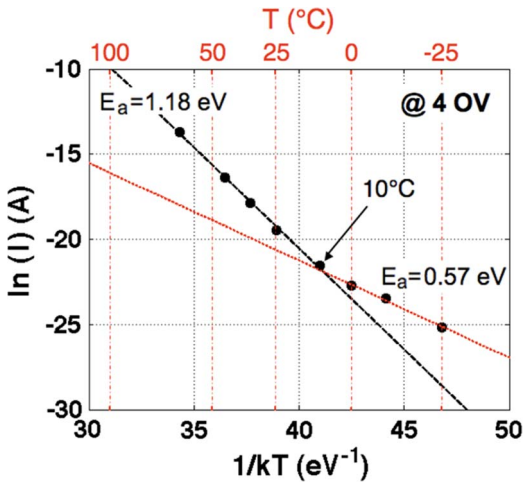

Fig. 10. Arrhenius plot of the dark current at a fixed $+4\ OV$. Black dashed line is the fit of the experimental data for temperature higher than 10 °C. Red dotted line is the fit of the experimental data for temperature lower than 10 °C.

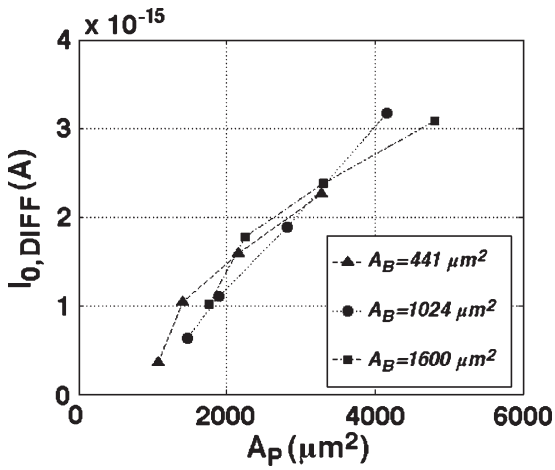

Fig. 11. $I_{0,\mathrm{DIFF}}$ as a function of the perimeter area A_P of an SiPM pixel for three active areas A_B: (Triangles) 441, (circles) 1024, and (squares) 1600 μm^2 from forward $I-V$ intercept at 25 °C.

We now discuss the DC model. Ideally, if no SRH center generating free carriers sits in the active volume, the average DC rate per unit area $\overline{DC}$ should be equal to the frequency of free carrier injection from the quasi-neutral boundaries, given by the well-known expression

$$\overline{DC}_{\mathrm{DIF}} = \frac{n_i^2 D_n}{N_a L_n} = \sqrt{\frac{D_n}{\tau_n}} \cdot \frac{n_i^2}{N_a} \tag{3}$$

where n_i is the intrinsic carrier concentration, N_a is the doping concentration at the depletion layer boundary of the enrichment, D_n is the electron diffusivity, L_n is the diffusion length, and τ_n the minority carrier lifetime.

If we assume the presence of defects, the related emission frequency is given by the well-known SRH expression

$$\overline{DC}_{\mathrm{SHR}} = N_{\mathrm{def}} \cdot W \cdot \gamma_{\mathrm{n}} \cdot \sigma_{\mathrm{n}} \cdot T^2 \cdot \exp\left(-\frac{E_c - E_T}{kT}\right) \tag{4}$$

where N_{def} is the defect concentration, W is the depletion layer width, γ_n is a universal constant, σ_n is the defect cross section, $E_C - E_T$ is the defect ionization energy, T is the temperature, and k the Boltzmann's constant.

According to (1), the dark current is

$$I = q \cdot G \cdot DC \propto q \cdot G \cdot T^{\gamma} \exp\left(-\frac{E_a}{kT}\right) \tag{5}$$

where $\gamma \sim 3$ for diffusion and ~ 2 for generation. G, as discussed previously, for a fixed OV is constant. The temperature dependence of the term T^{γ} is not important compared with the exponential term [21]. Then, the slope of the logarithm of the dark currents at fixed OV as a function of $1/kT$ provides the activation energy E_a.

The activation energy observed in the Arrhenius plot of the dark current at +4-V OV, shown in Fig. 10, is close to the energy bandgap of silicon for temperatures above 10 °C, evidencing that the diffusion of carriers is the dominant process. At temperatures below 10 °C, the slope of the Arrhenius plot provides an activation energy of 0.57 eV, close to half of the Si energy gap. The observed activation energy at low temperatures implies the presence of traps with ionization energies close to the Si midgap, acting as efficient SHR generation centers.

The DC rate given in (3) can be experimentally measured by the I–V characteristics in forward bias. In fact, in this voltage region, $I \approx q \cdot A \cdot \overline{DC}_{\mathrm{DIF}} \cdot \exp(qV/kT)$; hence, from the intercept of the forward bias I–V curves with the I-axis in semilogarithmic scale [22], we can evaluate the product $A \cdot \overline{DC}_{\mathrm{DIF}}$, see after for the calculation.

Fig. 11 shows $I_{0,\mathrm{DIF}} = q \cdot A \cdot \overline{DC}_{\mathrm{DIF}}$, derived from forward bias I–V curves (not shown) as a function of the perimeter area (A_P), at 25 °C for three different active areas (A_B). It is immediately visible that $I_{0,\mathrm{DIF}}$ is independent from A_B, while it increases almost linearly as a function of A_P, suggesting that the diffusion of minority carriers in such pixel structure is dominated by the perimeter area of the pixel. Moreover, the DC rate $(A \cdot \overline{DC}_{\mathrm{DIF}})$ evaluated from $I_{0,\mathrm{DIF}}$ for the SiPM pixel investigated in this work ($A_B = 1600$ μm^2 and $A_P = 1764$ μm^2) is 6.25×10^3 s^{-1}, in perfect agreement with the measured DC at high OV and at the same temperature (see Fig. 8, diamond symbols) confirming the accuracy of such analysis.

From the aforementioned discussion, it can be concluded that the DC of the single pixel at any temperature is due to the diffusion of minority carriers in the perimeter area of the pixel and to the SHR generation inside the depleted region of the active area of the pixel. In symbols

$$DC = \overline{DC}_{\mathrm{DIF}} \cdot A_P + \overline{DC}_{\mathrm{SHR}} \cdot A_B \tag{6}$$

where $\overline{DC}_{\mathrm{DIF}}$ and $\overline{DC}_{\mathrm{SHR}}$ are given by (3) and (4), respectively, A_P is the perimeter area, and A_B is the active area of the pixel [see Fig. 1(b)].

The comparison between the experimental DC (symbols) and (6) (dashed lines) is shown in Fig. 8. The agreement between data and model is extremely good. We fit the data both as a function of voltage and as a function of temperature by assuming the well-known relationship between carrier diffusitvity and mobility and assuming $\tau_n = 10$ μs, $\mu_n = 1500$ cm^2/V $\cdot$ s, $N_a = 1 \times 10^{15}$ cm^{-3} in (3), $N_{\mathrm{def}} = 10^9$ cm^{-3}, $E_C - E_T =$

0.55 eV, $\sigma_n = 1.6 \times 10^{-15}$ cm^2, with the universal constant $\gamma_n = 1.78 \times 10^{21}$ cm$^{-2} \cdot$ s$^{-2} \cdot$ K^{-2} as reported in [22], for the SHR generation of (4). The remarkable agreement between data and model is obtained by assuming quite reasonable values of the fit parameters, and this suggests that the present model catches quite well the behavior of the device. The small difference between data and model as a function of voltage is due to the triggering probability P_t that was not taken into account in (6). A more detailed analysis needs to implement P_t [23]. Moreover, these devices exhibit a dark current only limited by carrier diffusion already at quite low temperatures, essentially almost at 10 °C, indicating a remarkably low SRH defect concentration (on the order of 10^9 cm^{-3}).

VI. Conclusion

In this paper, we have reported on the characterization of SiPM pixels. We described a physical model of the dark current of SiPM single pixels and used it to fit the experimental data taken on SiPM single pixels realized by STMicroelectronics. The model fits nicely the data and demonstrates that state-of-the-art SiPM can have, at room temperature, a dark current rate limited only by carrier diffusion at the perimeter area of the pixel.

References

[1] G. Bondarenko, B. Dolgoshein, V. Golovin, Ilyin, R. Klanner, and E. Popova, "Limited Geiger-mode silicon photodiode with very high gain," *Nucl. Phys. B, Proc. Suppl.*, vol. 61, no. 3, pp. 347–352, Feb. 1998.

[2] N. Otte, B. Dolgoshein, J. Hose, S. Kleminin, E. Lorentz, R. Mirzoyan, E. Popova, and M. Teshina, "The potential of SiPM as photo detector in astroparticle physics experiments like MAGIC and EUSO," *Nucl. Phys. B., Proc. Suppl.*, vol. 150, pp. 144–149, 2006.

[3] S. Cova, M. Ghioni, A. Lacaita, C. Samori, and F. Zappa, "Avalanche photodiodes and quenching circuits for single photon detection," *Appl. Opt.*, vol. 35, no. 12, pp. 1956–1976, Apr. 1996.

[4] E. Sciacca, A. C. Giudice, D. Sanfilippo, F. Zappa, S. Lombardo, R. Cosentino, C. Di Franco, M. Ghioni, G. Fallica, G. Bonanno, S. Cova, and E. Rimini, "Silicon planar technology for single-photon optical detectors," *IEEE Trans. Electron Devices*, vol. 50, no. 4, pp. 918–925, Apr. 2003.

[5] A. Lacaita, M. Ghigni, and S. Cova, "Double epitaxy single-photon avalanche diode performance," *Electron. Lett.*, vol. 25, no. 13, pp. 841–843, Jun. 1989.

[6] A. Rochas, M. Gösch, A. Serov, P. A. Besse, R. S. Popovic, T. Lasser, and R. Rigler, "First fully integrated 2-D array of single-photon detectors in standard CMOS technology," *IEEE Photon. Technol. Lett.*, vol. 15, no. 7, pp. 963–965, Jul. 2003.

[7] M. Mazzillo, G. Condorelli, D. Sanfilippo, G. Valvo, B. Carbone, G. Fallica, S. Billotta, M. Belluso, G. Bonanno, L. Cosentino, A. Pappalardo, and P. Finocchiaro, "Silicon photomultiplier technology at STMicroelectronics," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 4, pp. 2434–2442, Aug. 2009.

[8] A. Poyai, E. Simeon, C. Claeys, and A. Czerwinski, "Silicon substrate effects on the current–voltage characteristics of advanced p-n junction," *Matter Sci. Eng. B*, vol. 73, no. 1, pp. 191–196, Apr. 2000.

[9] H. Aharoni, T. Ohmi, M. M. Oka, A. Nakada, and Y. Tamai, "Analysis of n^+p silicon junctions with varying substrate doping concentrations made under ultra-clean processing technology," *J. Appl. Phys.*, vol. 81, no. 3, pp. 1270–1288, Feb. 1997.

[10] R. H. Haitz, "Model for the electrical behavior of a microplasma," *J. Appl. Phys.*, vol. 35, no. 5, pp. 1370–1376, May 1964.

[11] C. Piemonte, R. Battiston, M. Boscardin, G. Dalla Betta, A. Del Guerra, N. Dinu, A. Pozza, and N. Zorzi, "Characterization of the first prototypes of silicon photomultiplier fabricated at ITC-irst," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 1, pp. 236–244, Feb. 2007.

[12] H. Otono, H. Oide, S. Yamashita, and T. Yoshioka, "On the basic mechanism of pixelized photon detector," *Nucl. Instrum. Methods A*, vol. 610, no. 1, pp. 397–399, 2009.

[13] M. Mazzillo, G. Condorelli, D. Sanfilippo, G. Valvo, B. Carbone, A. Piana, G. Fallica, A. Ronzhin, M. Demarteau, S. Los, and E. Ramberg, "Timing performances of large area silicon photomultipliers fabricated at STMicroelectronics," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 4, pp. 2273–2279, Aug. 2010.

[14] P. Buzhan, B. Dolgoshein, A. Ilyin, V. Kantserov, V. Kaplin, A. Karakash, A. Pleshko, E. Popova, S. Smirnov, Y. Volkov, L. Filatov, S. Klemin, and F. Kayumov, "An advanced study of silicon photomultiplier," *ICFA Instrum. Bull.*, vol. 23, pp. 28–41, 2001.

[15] K. Yamamoto, K. Yamamura, K. Sato, T. Ota, H. Suzuki, and S. Ohsuka, "Development of multi-pixel photon counter (MPPC)," in *Proc. IEEE Nucl. Sci. Symp.*, 2006, pp. 1094–1097.

[16] D. Renker and E. Lorenz, "Advances in solid state photon detectors," *J. Instrum.*, vol. 4, no. 4, pp. P04 004–P04 052, Apr. 2009.

[17] Y. Musienko, S. Reucroft, and J. Swain, "The gain, photon detection efficiency and excess noise factor of multi-pixel Geiger-mode avalanche photodiodes," *Nucl. Instrum. Methods Phys. Res. A*, vol. 567, no. 1, pp. 57–61, 2006.

[18] H. M. Chuang, "Temperature-dependent characteristics of polysilicon and diffused resistor," *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1413–1415, May 2003.

[19] R. Pagano, S. Libertino, G. Valvo, G. Condorelli, B. Carbone, A. Piana, M. Mazzillo, D. N. Sanfilippo, G. G. Fallica, G. Falci, and S. Lombardo, "Dark count in single photon avalanche Si detectors," in *Proc. SPIE*, 2010, vol. 7598, pp. 75980Z-1–75980Z-8.

[20] R. Pagano, S. Lombardo, S. Libertino, G. Valvo, G. Condorelli, B. Carbone, D. N. Sanfilippo, and G. Fallica, "Understanding dark current in pixels of silicon photomultipliers," in *Proc. 40th IEEE ESSDERC*, 2010, pp. 265–268.

[21] S. M. Sze, *Physics of Semiconductors Devices,* 2nd ed. Hoboken, NJ: Wiley, 1981, p. 88.

[22] K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. Hoboken, NJ: Wiley, 2006.

[23] W. J. Kindt and H. W. van Zeij, "Modelling and fabrication of Geiger mode avalanche photodiodes," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 3, pp. 715–719, Jun. 1998.

Authors' photographs and biographies not available at the time of publication.