retroSoC Mini Series Gen1/Gen2

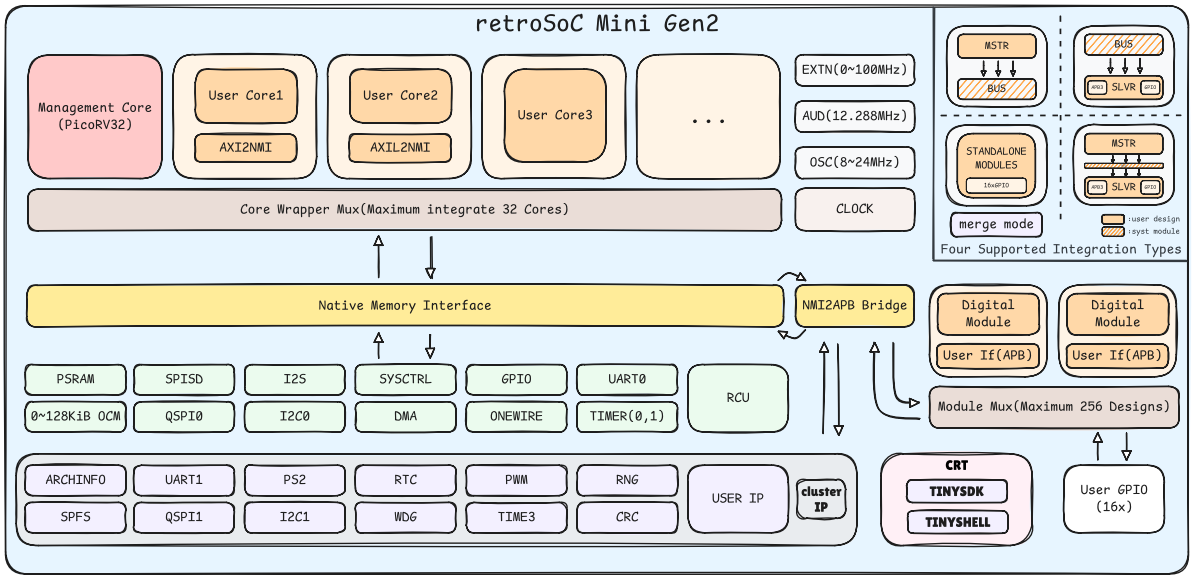
LOGO

Product Brief (rev.2 – 2025.12.02)

A **Lightweight** RV32I/EMC **MCU Framework** with **16MiB** NOR Flash Ext. Ctrl., **128KiB** OCM, 1xSPFS, 1xPS2, 2xUART, 3xTIMER, 1xRNG, 4xPWM, 1xARCHINFO, 1xRTC, 1xWDG, 1xCRC, 2xI2C, 2xQSPI, 1xSPISD, 1xI2S, 1xONEWIRE 1xPSRAM, 1xDMA, 1xRCU, 1xSYSCTRL, 24xGPIO (8+16), 1xGDS MERGE DESIGN

Feature

- Core – PicoRV32
  - **196MHz** maximum frequency
  - 2-pipeline RV32I/E[MAC], 16xIRQ
  - Hardware multiplication and division
- Memories
  - **16MiB** extern flash memory
  - **0~128KiB** On-Chip-RAM **(OCM)**
  - **32MiB (8MiBx4)** PSRAM Controller
- Bus – Async. **No-burst** Protocol
  - Native Memory Interface **(NMI)**
  - AXI4-Lite master, APB3 slave
  - NMI, AXI4L, APB3 Interconnect
- Reset Clock Unit **(RCU)**
  - **4~50MHz** Active Crystal Oscillator
  - PLL for core clock **(24~192MHz)**
  - PLL or Bypass mode
- SPISD (SDHC, 4~32GB)
  - **1GiB** Memory-mapped access
  - 1-line SPI compatible with **SD v2.0**
  - 512B cache, **50MHz** maximum freq.
- I2S (HQ, Hi-Res audio)
  - **48KHz**, **16-bit**, **Stereo** input/output
  - Half-duplex, I2S Phillips only
- QSPI
  - Half-duplex, SPI/QSPI/QPI mode
  - 32x32b TX/RX dual FIFO Integrated
- Other Communication Interfaces
  - 2xUARTs (FIFO/**No** FIFO)
  - 3xTIMER, 1xRTC, 1xWDG, 4xPWM
  - 1xRNG, 1xARCHINFO, 1xSYSCTRL
  - 2xQSPI, 1xONEWIRE, 1xCRC
  - 30xGPIO, 2xI2C, 1xPS2, 1xDMA
- **GDS Merge Template**
  - **0~32** master designs (Core)
  - **0~256** slave designs (IP, digital module)
  - **16**xGPIO, max 5000 cells per design
- Development
  - **Open source** and full synthesizable
  - Static synchronous design
  - **ICS55**, S110, IHP130 PDK support
  - RV32I/E[MAC] C Running Time **(CRT)**
- Tools & Flows
  - VCS, Verilator (TBD), iVerilog (TBD)
  - Yosys, iEDA, Pristine (TBD)
  - **QFN128** (12.3x12.3mm) Package
- Application
  - **Wearables**, IoT services, E-readers
  - Education, ASIC Prototype



Overview

retroSoC is a fully open-source and customizable ASIC framework for "***retro-style***" applications. It is both straightforward to use and highly compatible with EDA toolchains — specifically targeting open-source EDA **(iEDA, OpenROAD, etc)**.

Additionally, retroSoC can also serve as a flexible, reconfigurable ***SoC template*** for end customers or students who want to integrate their own design into a shared fabrication wafer **(shuttle)**.

The ***retroSoC Mini Series*** is a family of highly integrated, lightweight MCU designed for Internet of Things **(IoT)** scenarios. ***retroSoC Mini Gen2*** adopts the PicoRV32 core and integrates DMA, SPISD, I2S and QSPI multimedia IPs. It can be used for a wide variety of applications as wearables, education or ASIC prototype verification.

Product Series

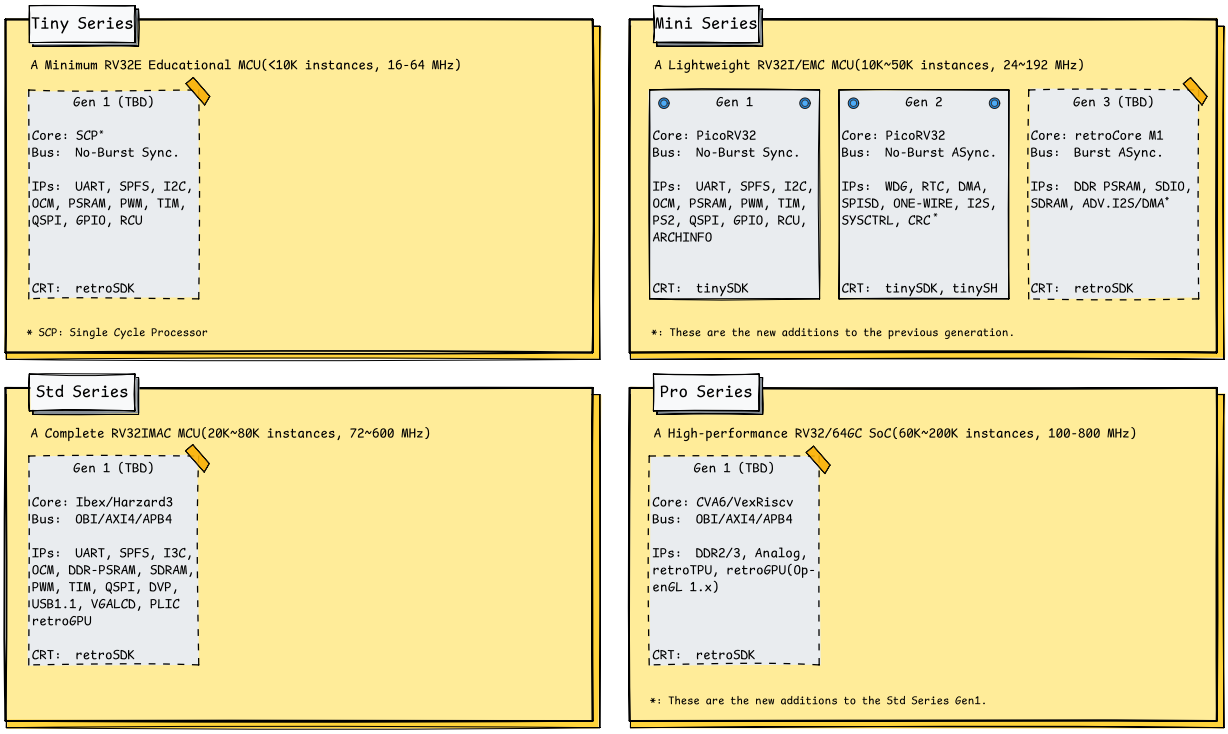


Figure 01. retroSoC product series

Roadmap

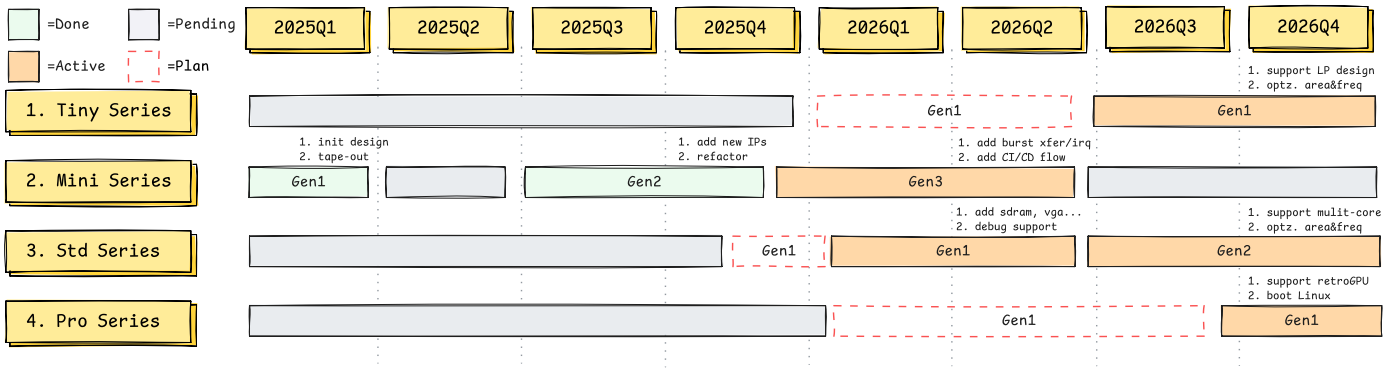


Figure 02. retroSoC product roadmap

Revision History

Date	Version	Release Notes
2025-09-28	v0.1	Create document
2025-12-02	v0.2	Initial draft
2026-01-xx	v0.x	Initial release

Contents