SNAP+
Data Sheet

Revision 1.17

profichip®
automation in silicon

Liability Exclusion

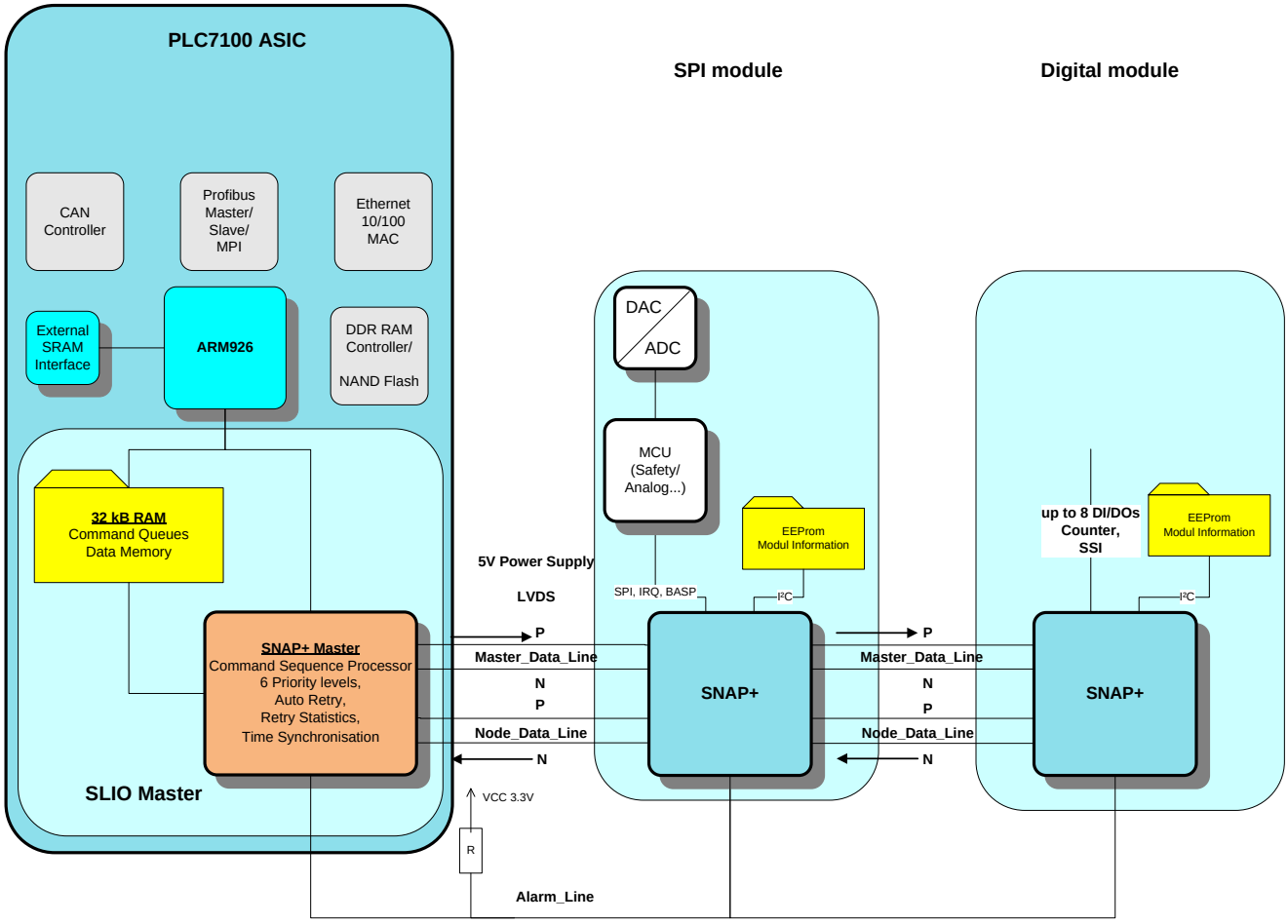
We have tested the contents of this document regarding agreement with the hardware and software described. Nevertheless, there may be deviations and we do not guarantee complete agreement. The data in the document is tested periodically, however. Required corrections are included in subsequent versions. We gratefully accept suggestions for improvements.

Copyright

This document is subject to technical changes without prior notice.

1 Overview

1.1 SNAP+ Typical Application



1.2 SNAP+ Features

Basic SliceBus information:

- Single master system
- Up to 64 slaves (SNAP+ modules) stations
- Asynchronous, serial data transmission with 48 MBit/s over Point to Point LVDS physic
- Additional alarm line for initialization and asynchronous event communications from SNAP+ module (slave at SliceBus) to SNAP+ Master
- Full system detection from SNAP+ Master without external information on module configuration

Error detection mechanism:

- CRC code with Hamming distance 4 for every telegram (all 3 bit errors will be detected)
- Watchdog function inside every SNAP+ module for SNAP+ Master observation
- “Auto shut down” in case of SNAP+ Master malfunction
- Retry statistic for early detection of possible transmission issues

Time Synchronization:

- Every SNAP+ module has its own clock with 1µs resolution
- All SNAP+ module clocks are synchronized with the SNAP+ Master (accuracy <100ns)
- Option for clock synchronization from SNP+ Master to SNAP+ Master via different protocols (Profibus DP V2, PROFINET, EtherCAT,...)

Technological functions in SNAP+:

- Standard I/O function: 8 digital I/O or 16DI or 16DO with shift register
- Integrated digital input filter function
- Asynchronous event signaling with µsec time stamping for advanced SNAP+ modules
- Two advanced counters with AB oversampling, latch, reset, output, hysteresis, compare value, repetitive/endless counting and additional time stamp information
- SSI function with time stamp information (speed calculations: counter difference/time)
- Pulse Width Modulation with 20ns resolution
- Frequency measurement mode
- Special digital I/O time stamp modules (ETS: Edge Time Stamp System) for input edge and output control with 1µs resolution (independent from fieldbus cycle!)

SPI interface in SNAP+ for analog I/O / safety / serial CP with external MCU:

- 2.6 MBit/s SPI interface for external microcontroller
- Up to 192 Byte for parameters, up to 16 byte In / 16 byte Out data for external microcontroller
- Alarm function and watchdog function

Performance:

- Different „Speed Grades“ for data transmission
- Multi-module telegrams for maximum efficiency:
  - ➔ read 32x1byte from digital inputs + write 32x1 byte from digital outputs
    1.) transmission time with module presence check: 44.4 µsec
    2.) transmission time without module presence check: 33.1 µsec

Mechanical and electrical specification SNAP+:

- I/O voltage: 3,3V, typ. 16mA, core voltage: 1,8V, typ. 16mA
- DI8 or DO8 module without I/O load: typical: 5V, 32mA
- LQFP 48 package, 9x9mm², pitch 0,5mm

2 Pin Description

2.1 General Statements and Notes

- All LVTTL outputs: 12 mA driver strength and slew rate limited switching characteristic
- All LVTTL inputs: Schmitt-Trigger characteristic

Notes:

VCCCORE	+ 1.8 V
VCCXTAL	+ 1.8 V
VCCPLL	+ 1.8 V
VCCIO	+ 3.3 V
GND	0 V
(pp)	push/pull
(LVDS)	LVDS buffer
(S)	LVTTL Input buffer with Schmitt-Trigger
(P)	Internal Pull Up Resistor

2.2 Pin Assignment

Pin	Signal	Direction	Description
1	GND		
2	SBUS_MDLI_P	IN (LVDS)	SliceBus: Master-Data-Line-IN positive (LVDS)
3	SBUS _MDLI_N	IN (LVDS)	SliceBus: Master-Data-Line-IN negative (LVDS)
4	SBUS _MDLO_P	OUT (LVDS)	SliceBus: Master-Data-Line-OUT positive (LVDS)
5	SBUS _MDLO_N	OUT (LVDS)	SliceBus: Master-Data-Line-OUT negative (LVDS)
6	VCCIO		
7	GND		
8	SBUS _NDLI_P	IN (LVDS)	SliceBus: Node-Data-Line-IN positive (LVDS)
9	SBUS _NDLI_N	IN (LVDS)	SliceBus: Node-Data-Line-IN negative (LVDS)
10	SBUS _NDLO_P	OUT (LVDS)	SliceBus: Node-Data-Line-OUT positive (LVDS)
11	SBUS _NDLO_N	OUT (LVDS)	SliceBus: Node-Data-Line-OUT negative (LVDS)
12	VCCIO		
13	DIO_7	INOUT (S)	DI / DO / Technological Function (depends on configuration)
14	DIO_6	INOUT (S)	DI / DO / Technological Function (depends on configuration)
15	DIO_5	INOUT (S)	DI / DO / Technological Function (depends on configuration)
16	DIO_4	INOUT (S)	DI / DO / Technological Function / SPI (depends on configuration)
17	VCCIO		
18	DIO_3	INOUT (S)	DI / DO / Technological Function / SPI (depends on configuration)

19	DIO_2	INOUT (S)	DI / DO / Technological Function / SPI (depends on configuration)
20	DIO_1	INOUT (S)	DI / DO / Technological Function / SPI (depends on configuration)
21	DIO_0	INOUT (S)	DI / DO / Technological Function / SPI (depends on configuration)
22	GND		
23	VCCCORE		
24	DO_DIS_N	OUT (pp)	Disable Outputs (active low)
25	DIAG_N	IN (S)(P)	Request Diagnosis (active low) (Pull up)
26	CLKOUT	OUT (pp)	Clock Output (12 MHz)
27	I2C_SCL	OUT (pp)	I2C bus to EPROM: clock
28	I2C_SDA	INOUT (S)	I2C bus to EPROM: data
29	VCCIO		
30	RESET_N	IN (S)(P)	Reset (active low) (Pull up) 10nF 0402 capacitor to Pin 29 recommended
31	STATUS1_N	OUT (pp)	Status LED 1 (active low)
32	STATUS0_N	OUT (pp)	Status LED 0 (active low)
33	GND		
34	XTALIN	IN (S)	XTAL input (24 MHz) or 1.8V CLK (48 MHz or 96 MHz)
35	XTALOUT	OUT	XTAL output
36	VCCXTAL		
37	GNDPLL		
38	VCCPLL		
39	GND		
40	VCCCORE		
41	POR_DIS	IN	Connect to VCCIO
42	CLK_SEL0	IN	Connect to GND / See Clock Source
43	CLK_SEL1	IN	Connect to GND / See Clock Source
44	CLK_SEL2	IN	Connect to GND
45	VCCIO		
46	TEST_0	IN	Connect to GND
47	TEST_1	IN	Connect to GND
48	SBUS_ALARM	OUT (pp)	SliceBus: alarm line

2.3 Clock Source

Clock Source	CLK_SEL0	CLK_SEL1
24 MHz crystal	GND	GND
48 MHz oscillator (1.8V) at XTALIN	+ 3.3V	GND
96 MHz oscillator (1.8V) at XTALIN (bypass PLL)	+ 3.3 V	+ 3.3V

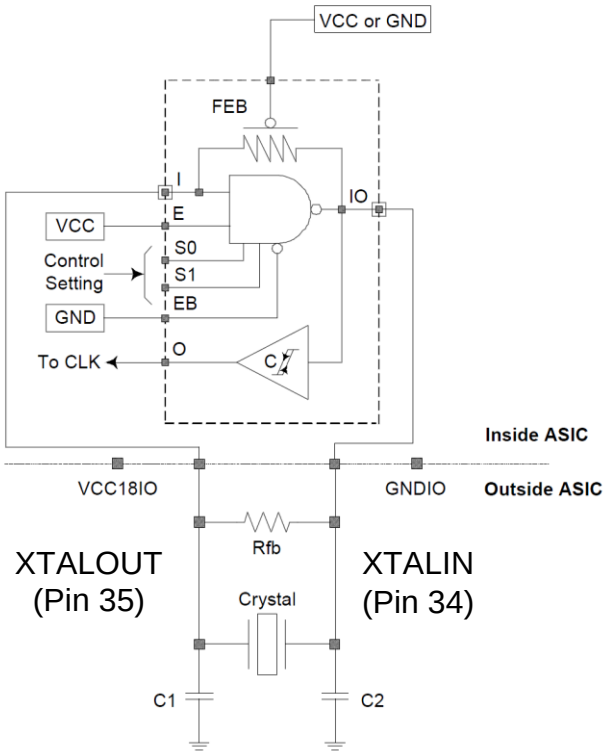


Figure 2-1: 24 MHz Crystal

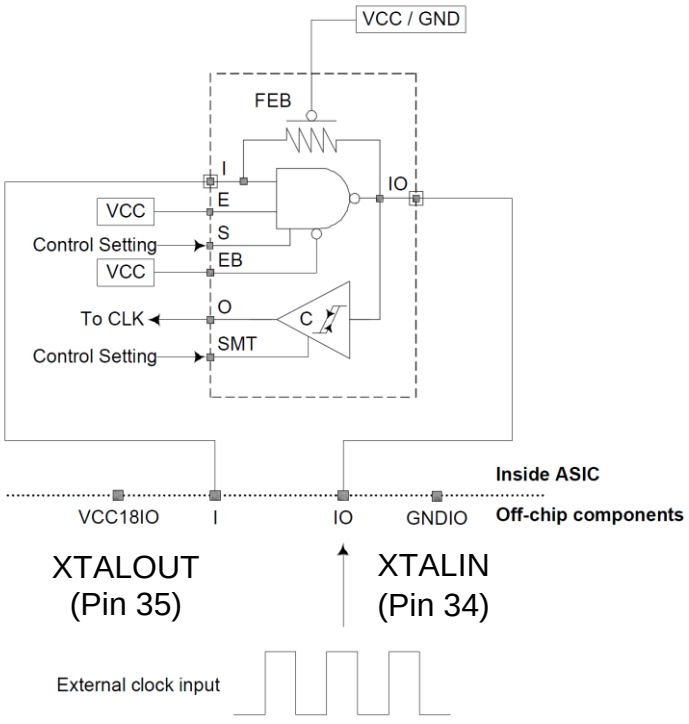
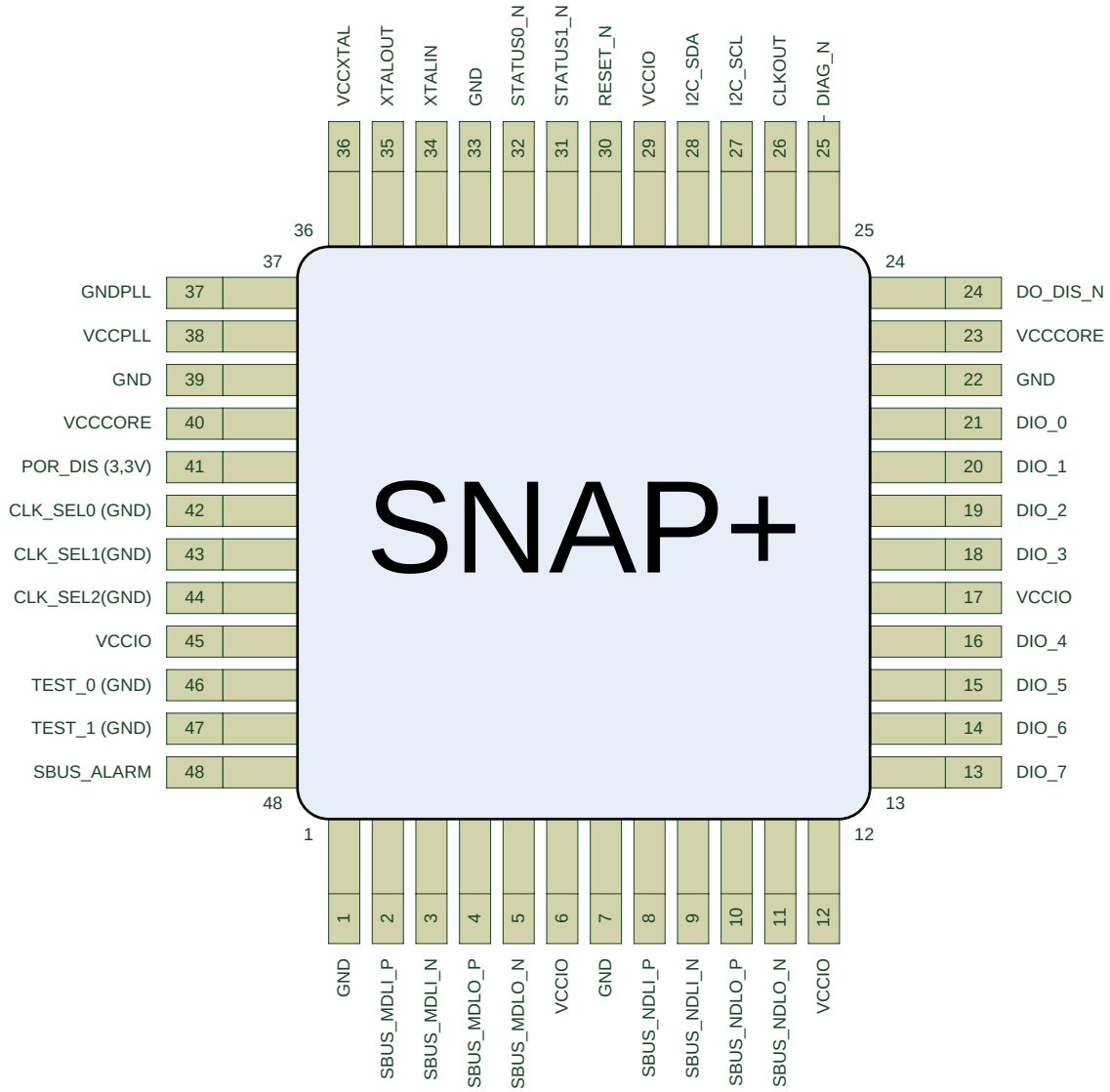


Figure 2-2: External Oscillator (48 or 24 MHz)

2.4 Symbol



3 Operational Specifications

3.1 Absolute Maximum Ratings

Permanent damages on devices may occur if the absolute maximum ratings are exceeded. These are only stress ratings, and the functional operations should be restricted within the recommended operating conditions. Exposure to the absolute maximum rating conditions for extended periods of time may affect the reliability of the devices.

Parameter	Symbol	Limits	Unit
Core power supply	VCCCORE	-0.5 to 2.5	V
IO power supply	VCCIO	-0.5 to 4.6	V
Input voltage	V_{IN}	-0.5 to 4.6	V
DC input current per I/O pin	I_{IN}	50	mA
Output short circuit current per I/O pin	I_{OUT}	50	mA
Storage temperature	T_{STG}	-65 to +150	°C

Figure 3-1: Absolute Maximum Ratings

3.2 Thermal Characteristics

Parameter	Symbol	Value	Unit
thermal resistance junction to case	$R_{th\ JC}$	27.88	K/W
thermal resistance junction to ambient	$R_{th\ JA}$	72.25	K/W

Figure 3-2: Thermal Characteristics

3.3 Reliability Information

Parameter	Symbol	Value	Unit
Failure in Time (FIT) at 125°C (Failure in 10^9 Hours) HTOL (High Temperature Operating Live)	FIT	50.9	

Figure 3-3: Reliability Information

3.4 Recommended Operating Conditions

Parameter	Symbol	MIN	MAX	Unit
Core power supply	VCCCORE	1.62	1.92	V
IO power supply	VCCIO	2.97	3.60	V

Input voltage	V_{IN}	0	3.63	V
Junction Temperature	T_J	-40	+125	°C

Figure 3-4: Recommended Operating Conditions

3.5 DC Characteristics of LVTTL IO cells

The table below refers to the run within the recommended operating conditions.

Parameter	Symbol	MIN	TYP	MAX	Unit
Input LOW voltage	V_{IL}			0.8	V
Input HIGH voltage	V_{IH}	2.0			
Switching threshold	V_T		1.5		V
Schmitt trigger negative going threshold voltage	V_{T-}	0.8	1.1		V
Schmitt trigger positive going threshold voltage	V_{T+}		1.6	2.0	V
Output LOW voltage (I_{NOM} = 12 mA)	V_{OL}			0.4	V
Output HIGH voltage (I_{NOM} = 12 mA)	V_{OH}	2.4			V
Nominal output current	I_{NOM}		12 mA		
Input leakage current	I_{In}	-10	±1	+10	µA
Tri-state leakage current	I_{OZ}	-10	±1	+10	µA
Input capacitance	C_{IN}		2.2		pF
Output capacitance	C_{OUT}		2.2		pF
Bi-directional buffer capacitance	C_{BID}		2.2		pF
Internal Pull Up Resistor to 3.3V	R_{pu}	40	75	190	kΩ

Figure 3-5: DC Characteristics of LVTTL IO cells

3.6 DC Characteristics of SNAP+ ASIC

Preconditions:

- DIO_0 ... DIO_7 inactive
- STATUS0_N, STATUS1_N inactive

Parameter	Symbol	MIN	TYP	MAX	Unit
Current consumption (3.3V)	I_{A33}		16	28	mA
Current consumption (1.8V)	I_{A18}		16	28	mA

Figure 3-6: DC Characteristics of SNAP+ ASIC

3.7 Package

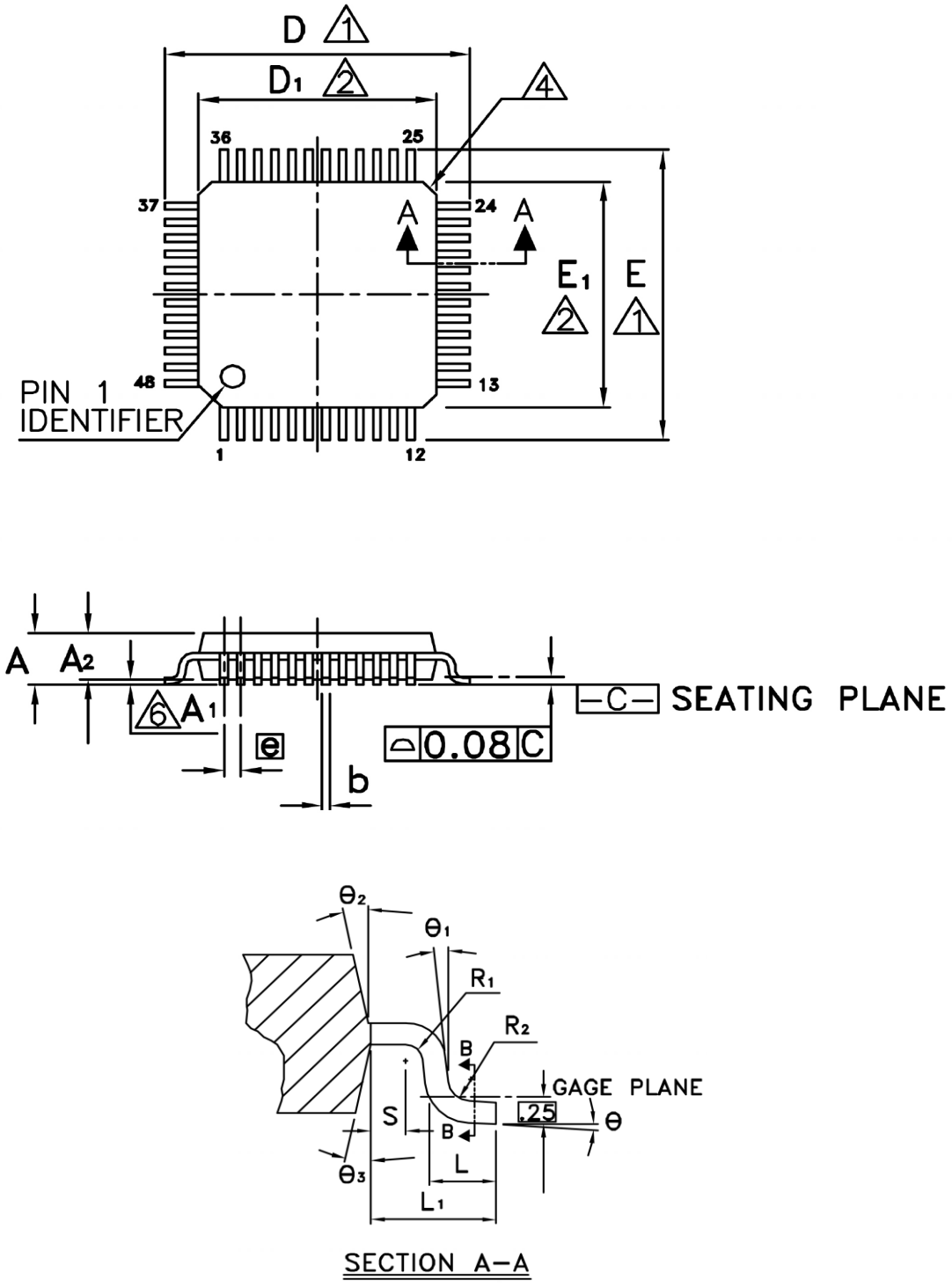


Figure 3-7: Package Drawing

Symbol	Dimensions in mm		
	MIN	NOM	MAX
A			1.60
A_1	0.05		0.15
A_2	1.35	1.40	1.45
b	0.17	0.22	0.27
b_1	0.17	0.20	0.23
c	0.09		0.20
c_1	0.09		0.16
D	9.00 BSC		
D_1	7.00 BSC		
E	9.00 BSC		
E_1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L_1	1.00 REF		
R_1	0.08		
R_2	0.08		0.20
S	0.20		
Θ	0°	3.5°	7°
$Θ_1$	0°		
$Θ_2$	12° TYP		
$Θ_3$	12° TYP		

Figure 3-8 : Package Dimensions and Tolerances

4 LVDS Characteristics

4.1 LVDS Schematic and Termination

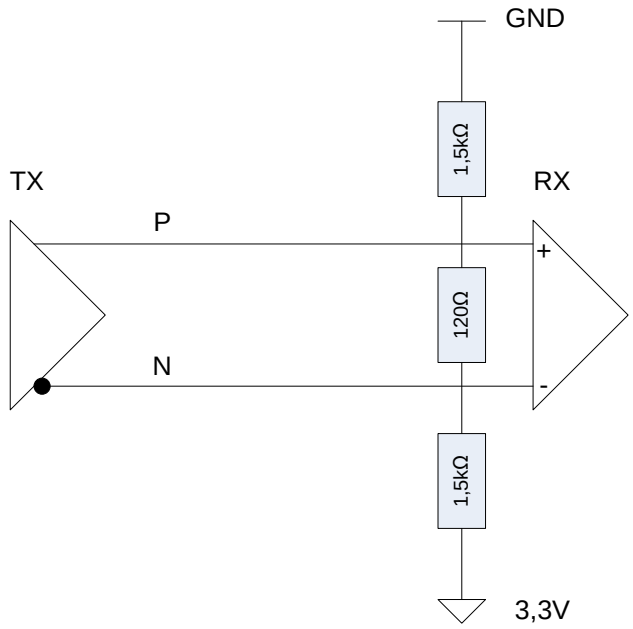


Figure 4-1: LVDS Termination

The pull up and pull down resistors at the LVDS RX buffer are used to force a negative Voltage (U = 127mV) at the LVDS input. That's necessary to set the input at a defined level for the case of open inputs.

4.2 DC/AC Characteristics of LVDS IO cells

LVDS Input

Parameter	Symbol	MIN	TYP	MAX	Unit
Differential input voltage P-N	V_{ID}	±100			mV
Input common-mode voltage	V_{IC}	$\|V_{ID}\| / 2$	1.25	$2.2 - \|V_{ID}\| / 2$	V

Figure 4-2: Characteristics of LVDS input cells

LVDS Output

Parameter	Symbol	MIN	TYP	MAX	Unit
Steady-state common-mode output (R_L = 100Ω , C_L = 50 pF)	$V_{OC(SS)}$	1.125	1.25	1.375	mV
LVDS driver output current	I_o		±3		mA

Figure 4-3: Characteristics of LVDS output cells

4.3 LVDS Signal Characteristics

Assembly

- the input signal is measured at the LVDS termination resistor of the SNAP+ at its Master-Data-Line input

Measurement

- random data pattern are transmitted
- the rising and the falling edges are overlaid
- positive input voltages larger than +100 mV will cause a “high” level at the LVDS input buffer
- negative voltages smaller than -100mV will cause a “low” level at the LVDS input buffer
- any voltage between -100mV and +100mV will cause a undefined level (“high” or “low”)

Result

- the negative offset is caused by the pull up and pull down resistors at the LVDS input
- eye width (P7) of 20.45 nsec was measured (q.v. figure Figure 4-4)

Note

- if the measured eye with is smaller than 20 nsec (e.g. cause by reflection), it is recommended to enable the data line synchronizer in both modules, the LVDS transmitter and the LVDS receiver

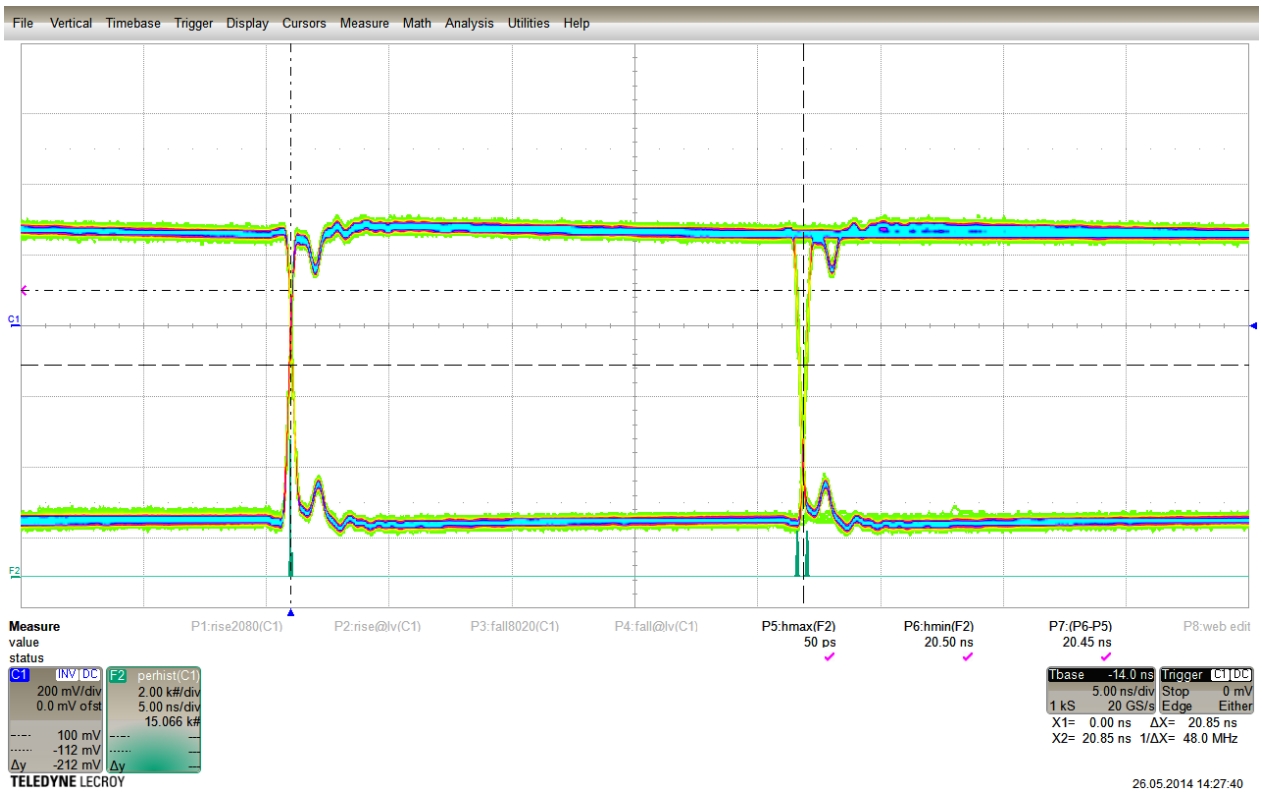


Figure 4-4: LVDS Signal

5 Layout and Schematic Recommendations

5.1 Layout Example

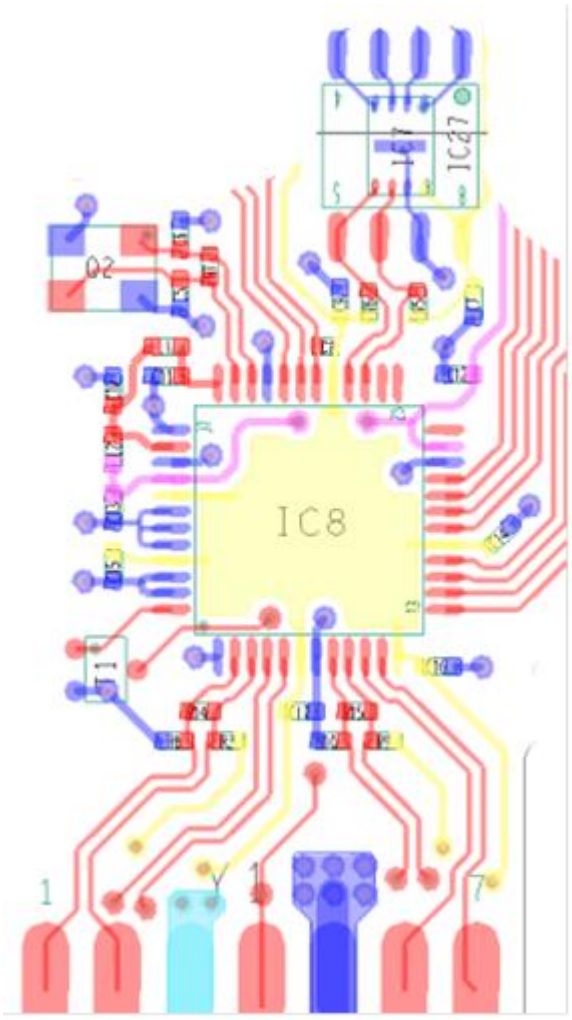


Figure 5-1: Layout Example: IC8: SNAP+, Q2 Crystal; IC27: EEPROM

5.2 Schematic Example

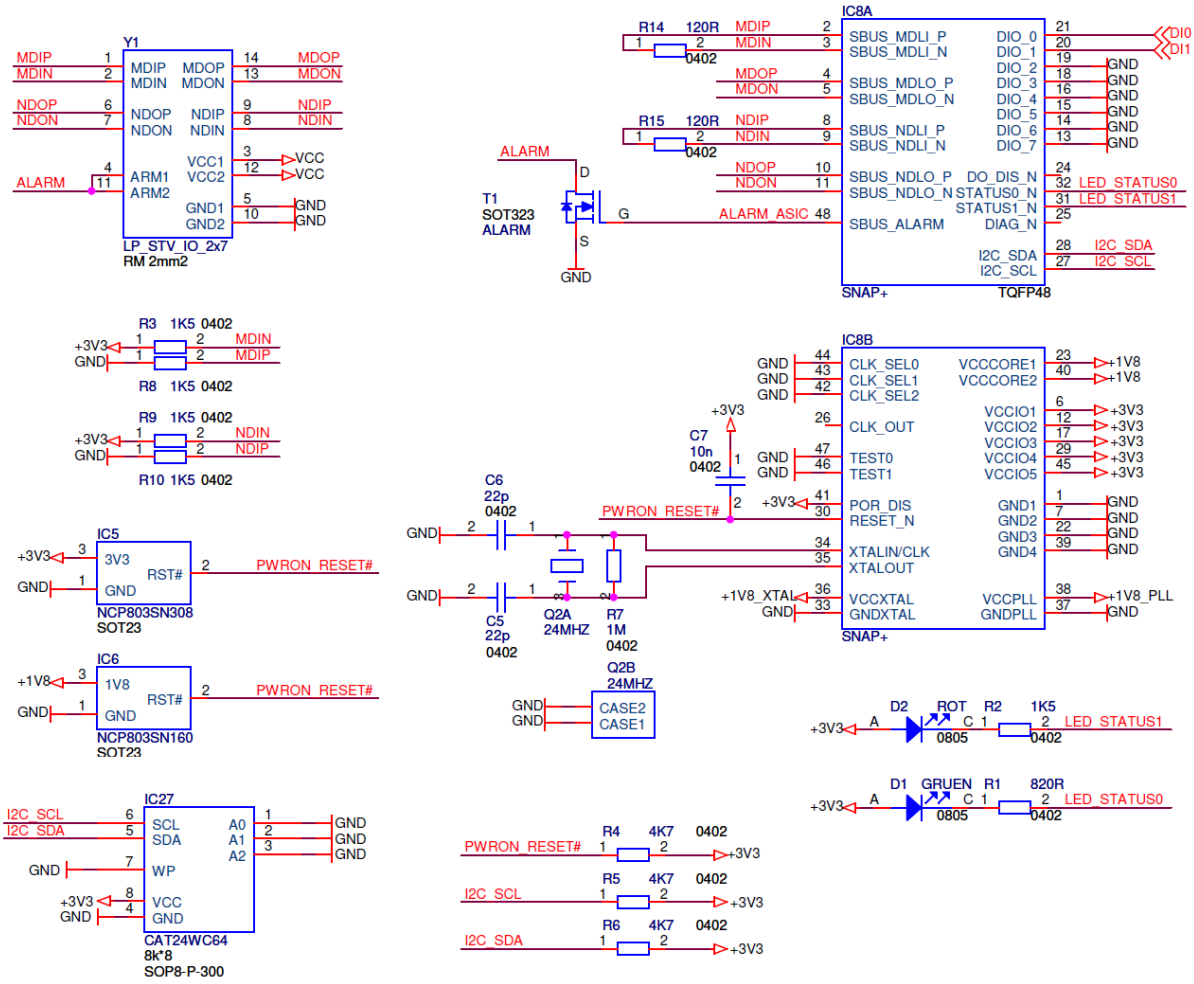


Figure 5-2: Schematic example

5.3 Note on crystal as clock source

When using a crystal as clock source for the SNAP+ device, circuitry as shown in Figure 5-3 is necessary.

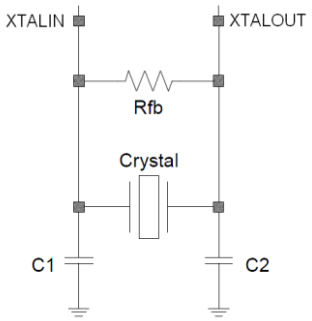


Figure 5-3: Circuit for 24 MHz crystal

With C_1 and C_2 the effective oscillator frequency can be controlled.
Higher values will slightly reduce the frequency. Lower values will raise the frequency.
Choosing the right capacitances is mandatory for correct functionality of the SNAP+ device.
The optimal value for the capacitors depends on the specific crystal oscillator in use (refer to manufacturers datasheet).
C_1 and C_2 should always be equal.

The value can be calculated using the formula

$$C_1 = C_2 = 2C_L - (C_P + C_I)$$

C_I : port capacitance (= **2.4 pF** for SNAP+)
C_P : line capacitance
C_L : load capacitance (found in datasheet of crystal oscillator)

Recommended values for C_1, C_2:	12 pF - 27 pF

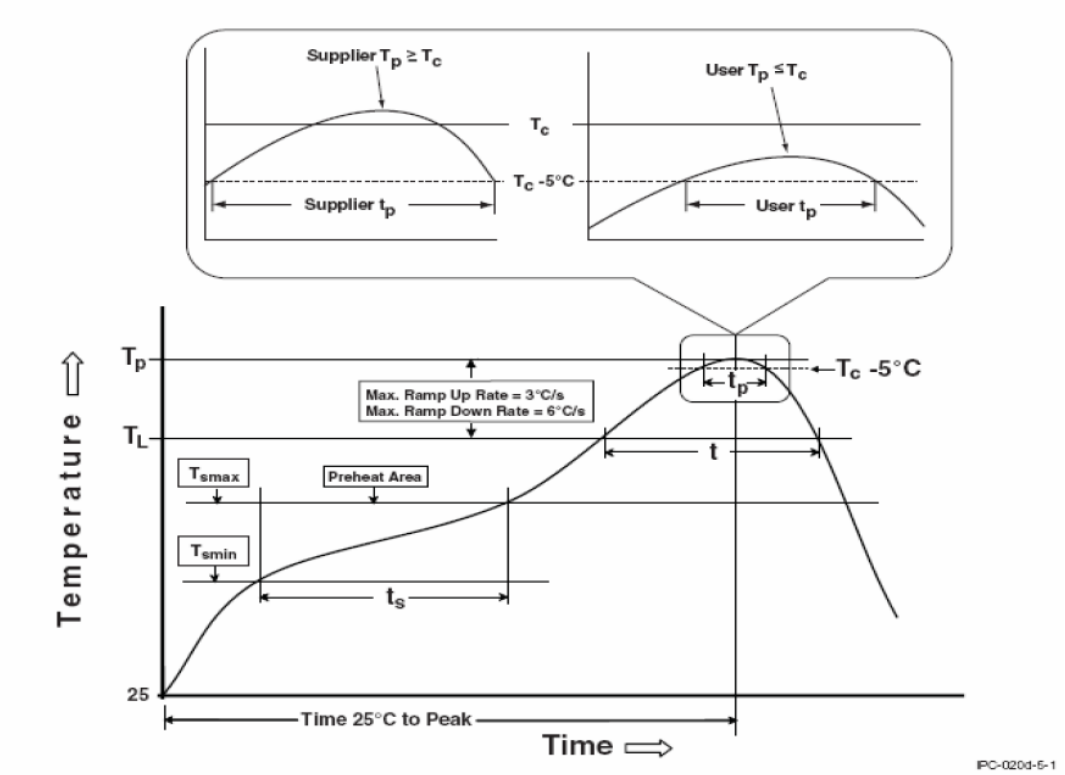
Example:

C_I = 2.4 pF
C_P = 1.0 pF
C_L = 12.0 pF

➔ $C_{1/2}$ = 20,6 pF (choose capacitors with 22 pF)
(R_{fb} may be 1 MΩ)

6 Soldering Profile

Profichip Green Package Reflow Profile
based on IPC/JEDEC J-STD-020D



Profile Feature	Pb-Free Assembly (260°C)
Preheat and Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 150 °C 200 °C 60-120 seconds
Average ramp-up rate Time (T_{smax} to T_p)	 3 °C/second max.
Liquid temperature (T_L) Time at liquid (t_L)	217 °C 60-150 seconds
Peak package body temperature (T_p)*	260°C
Time (t_p) ** within 5 °C of the specified classification temperature (T_c)	30** seconds.
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.
Time 25 °C to peak temperature	8 minutes max.
* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.	

7 Order Information

Order Code:

PA007713

Delivery form:

Tray

8 Appendix

8.1 Revision History

Version	Date	Page	Remarks
V1.00	08.03.2011		First release
V1.01	12.04.2011		Added Layout Example
V1.02	29.04.2011		Added Thermal Resistance, Changed SPI Speed Value, Added Schematic, Added LVDS Schematic, added LVDS Signals, Changed current consumption to typical
V1.03	05.05.2011		Added Soldering Profile, replaces Figure 4-3
V1.04	05.05.2011		No 32 Bit Option in Shift Register Mode, Added SNAP+ Symbol
V1.05	06.05.2011		Added Order Information
V1.06	27.05.2011	17 13 6,8 9 18 10	Fixed Soldering Information (one Line to much) Added Output Driver Current Value Fixed Pins VCC XTAL and GND XTAL Added Reliability Information Added Delivery form: Tray Added max. Current Consumption
V1.07	10.01.2012	6,7 8 14 16	Signal names modified Signal names modified Signal names modified Schematic example modified
V1.08	04.05.2012	6,7,10 13	Added internal Pull Up at DIAGN_N and RESET_N Pins Corrected Schematic for LVDS Schematic: now consistent with figure 5-2 and 4-3
V1.09	09.08.2012	Chapter 2	Added information for usage of oscillator instead of crystal
V1.10	10.10.2012	Chapter 2.x	Added Information for crystal and oscillator Input Added comment to RESET_N input Fixed naming issues in symbol 2.3
V1.11	20.12.2012	1.2	new read/write access example added
V1.12	21.01.2013	3	Operational specifications modified
V1.13	07.02.2013		Added Note on crystal as clock source
V1.14	08.02.2013	18	Fixed Note on crystal as clock source
V1.15	20.03.2013	Chapter 5 Chapter 2	Layout and schematic example modified: C = 10 nF added according to PIN assignment (PIN 30) General statements added, push/pull outputs marked
V1.16	11.11.2015	Chapter 4	4.1: description added 4.3: eye width specified
V1.17	07.08.2017	Chapter 4	4.2: LVDS output characteristic added

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Preliminary