REVANTH KODURU

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EDUCATION

Purdue University, Electrical and Computer Engineering — West Lafayette, IN
PhD, VLSI and Circuit Design, GPA: 4.00/4.00 — Expected May 2025

Indian Institute of Technology Madras, — Chennai, India
B.Tech., Electrical Engineering, GPA: 9.16/10 — May 2018

RESEARCH EXPERIENCE

Research Scholar, *Semiconductor Research Corporation (SRC)* — January 2021 – Present

- Student member of SRC centers: Center for Brain Inspired Computing (C-BRIC), Center for the Co-Design of Cognitive Systems (CoCoSys), Logic and Memory Devices (LMD)

Graduate Research Assistant, *Purdue University* — West Lafayette, IN
Advisor: Prof. Sumeet Gupta — January 2021 – Present

- Developed comprehensive models of HfO_2-based ferroelectric devices incorporating wide spectrum of materials characteristics of HfO_2 in a self-consistent manner.
- Investigated the intrinsic physical mechanisms dictating the operation of ferroelectric devices, delving into the intricate relationship between device characteristics and material and device non-idealities.
- Explored the impact of material non-idealities on device level performance for multi-level non-volatile memory applications, leading to the formulation of application specific circuit and device level optimization strategies.

Undergraduate Research Assistant, *Indian Institute of Technology, Madras* — Chennai, India
Advisor: Prof. Janakiraman — October 2017 – May 2018

- Developed an approach combining analytical and non-linear optimization techniques to extract statistical parameters characterizing process variations from wafer performance data.
- Reduced prediction error to < 3% when working with performance data exhibiting skew-Gaussian distribution.

Research Intern — Chennai, India
Defense Research and Development Organization — May 2016 – July 2016

- Improved reliability of LEON3 processor under high-temperature and radiation conditions, achieving a reduction in failure rate by 30%, through usage of redundancy techniques.

PROFESSIONAL EXPERIENCE

Silicon Debug and Applications Engineer, *High Speed Converters group* — Bangalore, India
Texas Instruments — June 2018 – July 2020

- Led the characterization and post-silicon debugging efforts for transmitters in Quad transceiver ICs, ensuring their optimal performance and reliability.
- Built an FPGA-based data capture system to facilitate high-speed communication with transceivers reaching speeds up to 30Gbps.
- Collaborated as a key member of a 3-person team, delivering valuable customer support for debugging issues arising during production.
- Acknowledged with 'Global Recognition Award' for instrumental contributions that enabled a customer to move into production within a span of 6 months.

Digital Design Intern, *Precision DAC group* — Bangalore, India
Texas Instruments — May 2017 – July 2017

- Devised an architecture agnostic layout optimization technique for Digital-to-Analog Converters (DACs) to decrease the performance degradation due to process variations by 20%.

SKILLS

Programming languages: Python, MATLAB, Verilog, and C, Verilog-A.

Software and Applications: Cadence virtuoso, Spectre, Hspice, COMSOL.

Data analysis and Statistical modeling, Handling of Electrical Characterization equipment.

PUBLICATIONS AND CONFERENCES

- R. Koduru et al., "Phase-field simulations of polarization variations in polycrystalline Hf0.5Zr0.5O2 based MFIM: Voltage dependence and dynamics," *J. Appl. Phys.*, 2023.
- R. Koduru et al., "Variation and Stochasticity in Polycrystalline HZO based MFIM: Grain-Growth Coupled 3D Phase Field Model based Analysis," *IEEE International Electron Devices Meeting (IEDM)*, 2021.

- R. Koduru, T. K. Paul, and S. K. Gupta, "Material, Device and Circuit-Compatible Modeling of Ferroelectric Devices," *IEEE Nanotechnology Magazine*, 2023.
- R. Koduru and V. Janakiraman, "Statistical compact model extraction for skew-normal distributions," *IET Circuits, Devices & Systems*, 2020.

RELEVANT COURSEWORK

- MOS VLSI design.
- CMOS analog IC design.
- Advanced VLSI design.
- Solid State Devices.
- System-on-Chip design.
- Digital design automation.
- Numerical Analysis.
- Deep Learning.

ACADEMIC PROJECTS

Neural Network Inference Accelerator, *System-on-Chip Design*

- Accelerated MLP and CNN based neural network inference through software profiling, designing custom instructions and hardware acceleration techniques, ensuring accuracy and reduced latency.
- Conducted comprehensive performance analysis, providing summary of improvements achieved and tradeoffs.

SAT Solver Implementation, *Digital Systems design automation*

- Implemented a SAT solver using DPLL algorithm as the fundamental framework, along with various heuristics such as BCP, branching heuristics, DLIS to enhance the solver performance.
- Carried out the performance testing on diverse benchmarks, evaluating the solver's effectiveness in solving Boolean satisfiability problems.

SRAM-based In-memory Computing, *MOS VLSI Design*

- Implemented an 8T SRAM array storing 128 words of 16-bits, optimizing the layout to minimize the 8T cell and the overall array area.
- Designed bitline drivers, sense-amplifiers for SRAM array tailored to support in-memory NOR operation.

Analysis of Width Scaling in Schmitt Trigger SRAM Cell, *Advanced VLSI Design*

- Conducted comprehensive analysis of width scaling in Schmitt trigger-based SRAM bit cells, evaluating various aspects such as static noise margins, access times and leakage.
- Compared and contrasted different SRAM bit cell architectures, examining their merits and demerits in terms of performance metrics and failure probabilities.

VOLUNTEERING AND SERVICES

Reviewer

- IEEE Journal of Exploratory Solid-State Computational Devices and Circuits.
- IEEE Electron Device Letters.
- IEEE Transactions on Electron Devices.

Class representative*, EE class of 2018* Chennai, India
Indian Institute of Technology, Madras Aug 2014 – May 2015

- Served as representative for a class of 100 students in the dean's academic council, conveying student concerns and presenting viable solutions.

Academic Buddy*, Mitr* Chennai, India
Indian Institute of Technology, Madras Aug 2015 – Dec 2015

- Provided mentorship and academic guidance to a group of five freshmen students, supporting them in both their academic pursuits and transition to university life.