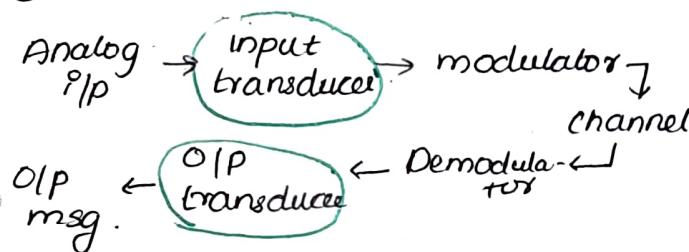


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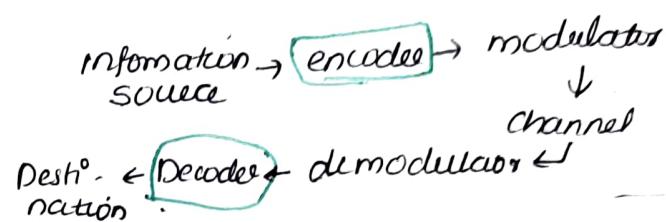
## Assignment II

- ① List the difference b/w analog and digital communication?

### Analog



### Digital



- ② Analog sig is used for information transmission

Digital signal is used for information transmission

- ③ Amplitude varies continuously.

2 level, either high or low noise is less

- ④ noise in channel is high

it can broadcast large no. of channels simultaneously error is low

- ⑤ Only limited no. of channel

good noise immunity

can broadcast simultaneously

coding is possible & different coding techniques can be used to detect & correct code.

- ⑥ Error probability is high

separating noise and signal in digital communication is possible

- ⑦ noise immunity is poor

Time division multiplexation used

- ⑧ coding is not possible

cost is high

- ⑨ separating out noise and signal in analog communication is not possible.

low power consumption

- ⑩ FDM multiplexing is used

synchronisation is easier

low cost

high bandwidth required

power consumption is high

- ⑪ synchronisation problem

portability is high

- ⑫ low bandwidth required

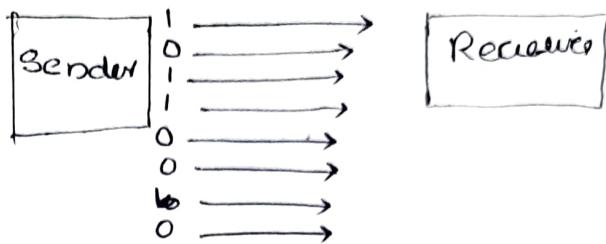
less portable.

② List the difference between serial and parallel communication?

### Serial communication

1. Sender   
bit by bit. 00101100

### Parallel communication



2. Bit by bit in sequence using a single channel.

Data as whole byte using multiple channels.

3. Single communication link or wire to either transfer or receive data.

It uses multiple communication links or wires.

4. Full duplex communication

Half duplex communication

5. Start and stop bit or external clock to synchronize the data.

No need to synchronize, whole byte receive in single clock.

6. It is slower at a short distance and low frequency.

Fast at short distance and low frequency.

7. Efficient at long distance & high frequency.

Not efficient for long distance and high frequency.

8. Not affected by cross talk.

Vulnerable to cross talk & skewing.

9. Simple and cost-effective

Expensive having complex chips.

10. Eg: USB, SATA, I2C, SPI etc..

Computer & printer & communication b/w Es ~~internal~~ internal components

③ List the difference between Baud rate and Bit rate?

### Bit rate

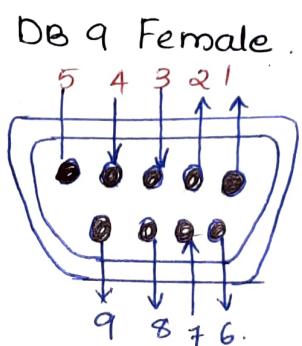
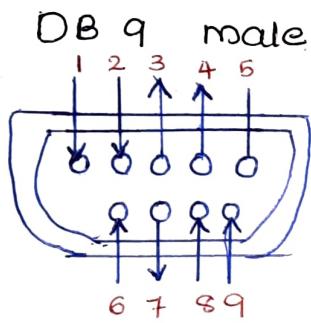
### Baud rate

1. Bit rate defined as the transmission of number of bits per second.
2. Per second travel no. of bits

5. What is RS 232? With neat diagram explain the RS 232 DB9 pins and its handshaking process with modem?

RS 232 is one of the standard protocol in telecommunication which is used for serial communication of data. It is the process of connecting signals between data terminal equipment DTE for eg: file server, receiver, application server such as modem.

RS 232 is used in computer ports. It involves serial & parallel communication.



1. → CD carrier Detect
2. ← RXD Receive data
3. → TXD transmit Data
4. → DTR Data terminal ready (A)
5. - ground
6. ← DSR Data set ready (B)
7. ← RTS Request to send (C)
8. → CTS Clear to send (D)
9. → RI Ring indicator

1. ← CD - carrier detect
2. → TXD - Transmit data
3. RXD ←
4. DTR →
5. GND -
6. DSR ←
7. CTS →
8. RTS ←
9. RI ←.

Slow rate: The rate at which signal level changes, the maximum slow rate in RS 232 is 30 v/ms.

Line impedance: between the wire DTE & DCE is 3 to 7 Ω.

procedure specification:

It is the pattern of operations that are carried out when DCE & DTE wires are connected.

Ready to send

1. When source (DTE) sends information, the modem becomes ready to receive, it sends a DCE ready signal.
2. When router ready to send data, it sends ready to send signal. Clear to (Request to send)
3. The modem further sends a signal called clear to send shows the data can be send by the router.
4. Lastly DTE sends information to TD line to the modem.

The process of transmitting and receiving which uses different identifications altogether & backed up by another process called Handshaking

Handshaking is a process that actually places the parameters of a communication between the transmitter and receiver before communication begins. The requirement of handshaking is dependent on the speed of the transmitter at which it sends data to the receiver and the speed at which the receiver receives. There is no requirement of handshaking in case of asynchronous transmission.

In few txns, handshaking is not used and the receiver DCE should read the data already received by it before DTE sends next data. There is a receiver buffer to store the data before DCE reads. It is a single bit register, so data if the present data is not clear or read, it will overwritten along with new data.

Q) What are DTE and DCE equipments. Give examples.

→ DTE (Data terminal equipment) is a device that is information source or information sink. (binary digital)

- produces the data & transfers them to a DCE with essential control characters.
- No co ordination is required between DTE devices

Eg: all Routers and computers.

connected through the help of DCE network.

### DCE

- It is the device used as an interface between a DTE. (Digital or analog)
- It converts signal to a format appropriate to the transmission medium and introduces it on to the network line.
- DCE devices must be coordinated in order to communicate.
- Eg: Modem.
- DCE network act as a medium of two DTE

new.

⑦ If baud rate is 9600, how much time is required to transmit a single bit?

9600 Baud rate means, 9600 Bits per second.

The frequency is 9600 and time is  $\frac{1}{9600}$ .

So  $\frac{1}{9600}$  sec is required to transmit a single bit.

⑧ What is SPI? List its features.

Serial peripheral interface is serial communication protocol.

- Synchronous serial communication
- full duplex communication
- master slave type protocol
- simple and cost effective interface between a microcontroller and peripheral
- used for interfacing microprocessor or microcontroller with memory like EEPROM, RTC (real time clock)

ADC, DAC, displays like LCDs, Audio ICs, Sensors like temperature and pressure, memory cards like mme or SD or even other micro controllers.

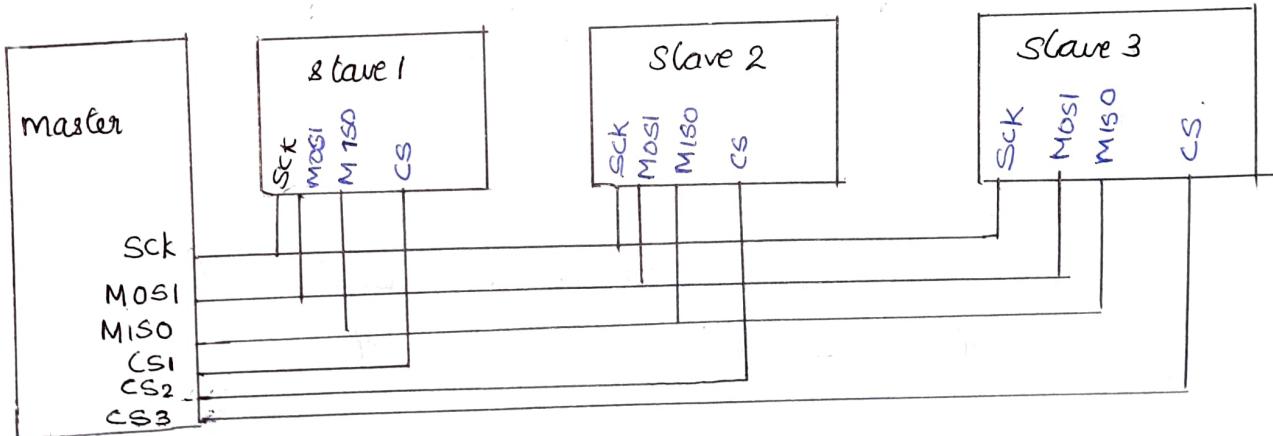
→ Data can be send or receive in continuous streams w/o interruption.

9. With a neat diagram explain the working of SPI in multislave mode?

SPI can be setup with single master and single slave, and it can be setup with multiple slaves controlled by single master.

Multislave mode has 2 configuration → independent slave and daisy chain.

### Independent slave configuration

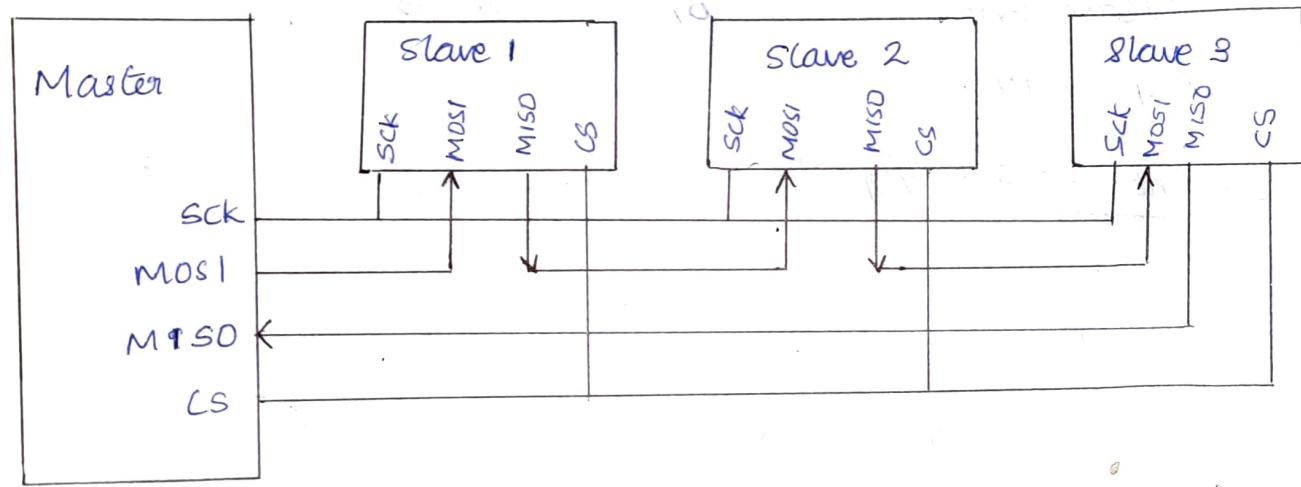


In independent slave configuration, there is an independent chip select line for each slave. The master assert only one chip select at one time.

Since the MISO pins of the slaves are connected together, they are required to be tristate pins (high, low or high impedance). When the high impedance output must be applied when the slave is not selected. Slave devices not supporting tristate may be used in independent slave configuration by adding a tristate buffer chip controlled by chip select signal.

10. With neat diagram, explain the working of SPI in daisy chain configuration?

Some products that implement SPI may be connected in daisy chain configuration. The first slave O/P to 2nd slave input. The whole chain act as a communication shift register. Daisy chaining is often done with shift register to provide bank of input or output through SPI. Each slave copies input to output in the next clock until active low SS line goes high. This only requires single SS line from the master, rather than single SS line for in line.

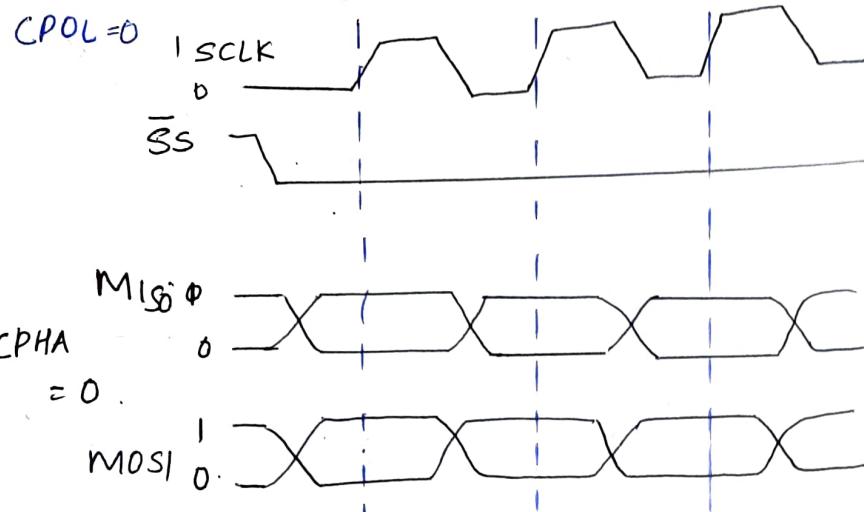


11. Explain with a timing diagram, how CPOL and CPHAES work in SPI. What is the purpose of CPOL and CPHASE.

SPI interface allows to transmit and receive data simultaneously on two lines (MOSI and MISO). Clock polarity (CPOL) and clock phase (CPHA) are the main parameters that define a clock format to be used by SPI bus. Depending on CPOL parameter, SPI clock may inverted or non-inverted. CPHA used to shift sampling phase.

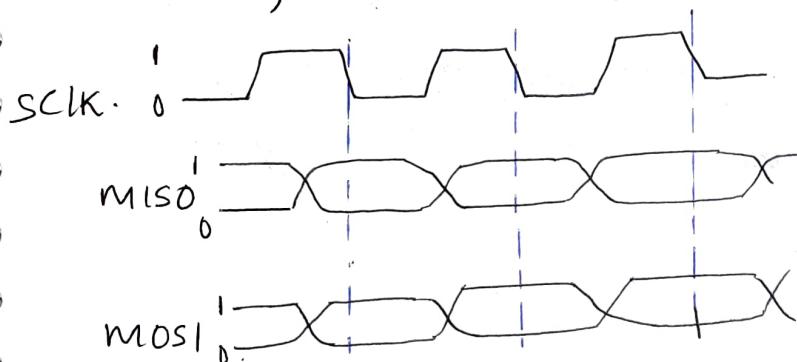
If CPHA=0, the data are sampled on leading clock edge.

$C_{POL} = 0, C_{PHA} = 0$



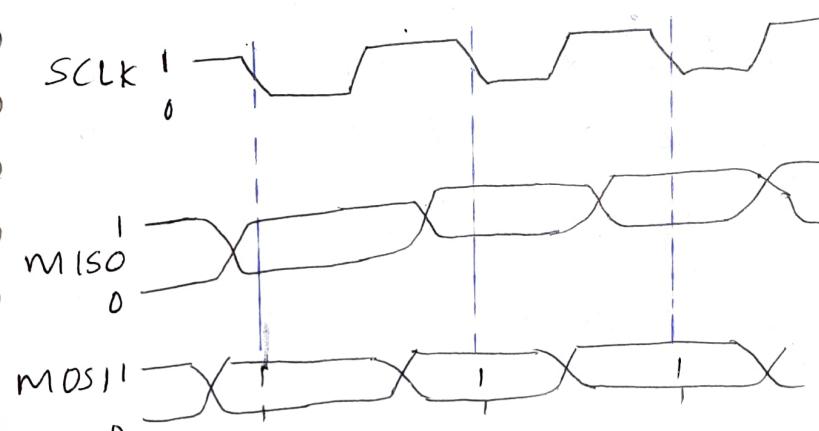
idle slate is zero.  
slable when clock is  
high and can be  
changed when  
clock is low.

$C_{POL} = 0, C_{PHA} = 1$



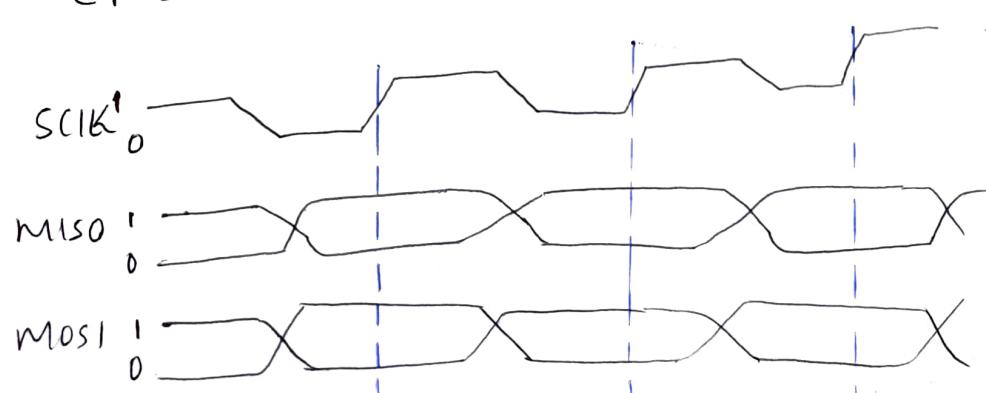
The clock idle slate is zero  
when clock is low, data  
is slable and data  
change when clock is  
high.

$C_{POL} = 1 \quad C_{PHA} = 0$



The data is captured  
on the clock's high-to-low  
transition and propagated  
on low-to-high clock  
transition

$C_{POL} = 1 \quad C_{PHA} = 1$



The clock idle slate  
is one.

The data must  
be slable when clock is  
high ~~high~~ and change at  
clock is ~~low~~ high, low

⑫ What is I<sub>2</sub>C protocol and explain its features?

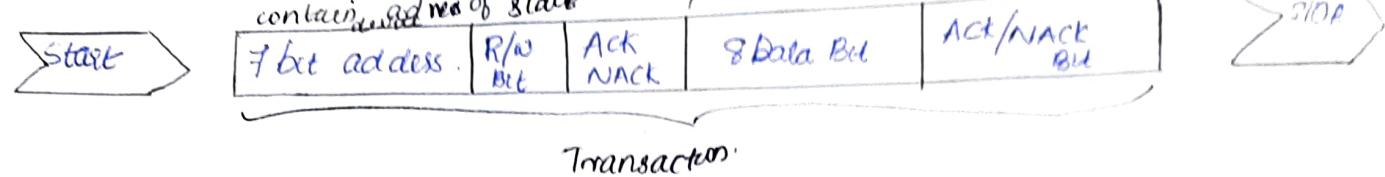
I<sub>2</sub>C communication is the short form for Inter-Integrated Circuit. It is a communication protocol developed by Philips for transfer of data between a CPU and multiple ICs on same circuit board using just 2 common wires. Owing to its simplicity, it is widely adopted for communication between microcontrollers and sensors, displays, IoT devices, EEPROMs etc.

This is a type of synchronous serial communication protocol. It means that data bits are transferred one by one at regular interval of time set by a reference clock line.

### Features:

- 2 common lines lines required to connect any device/IC on I<sub>2</sub>C.
- no need of prior agreement on data rate like UART communication. So <sup>data thr</sup> speed can be adjusted whenever required.
- Simple mechanism for validation of data transferred.
- uses 7 bit address line to target a specific device/IC on I<sub>2</sub>C lines.
- I<sub>2</sub>C now are easy to scale. new device can simply connect to new common lines.

### 13. Explain I<sub>2</sub>C protocol.



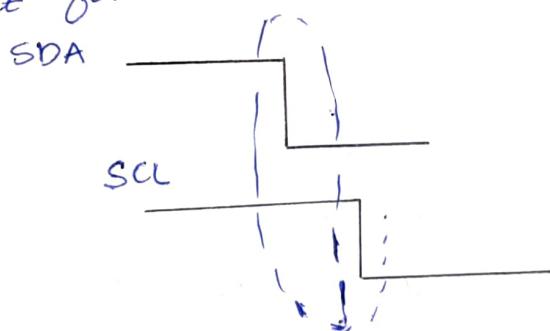
#### 1. Address block

It comprises of 7 bits are filled with the address of slave device to/from which the master device needs send/receive data. All slaves on I<sub>2</sub>C bus compare these address with their address.

#### 2. Start condition

When a master device/IC decides to start a transaction, it switches the SDA line from high voltage level to a low voltage level before the SCL line switches from high to low.

Once a start condition is sent by the master device, all slaves devices get active even if they are sleep mode and wait for the address.



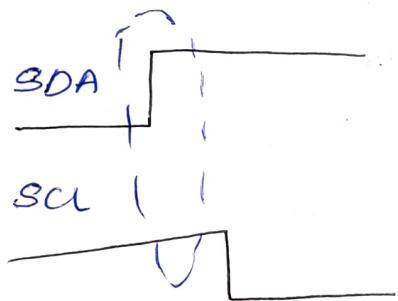
**3. Read/write Bit:** The last specifies the direction of data. If the master device/IC need to send data to a slave device, this bit is set to 0 and if master IC need to receive data from slave, it is set to 1.

**4. ACK/NACK Bit:** It stands for acknowledged/not acknowledged bit. If the physical address of any slave device coincides with the address broadcasted by the master device. The value of this bit is set to 0 by the slave device. Otherwise it remains logic 1.

**Data Block:** It consists of 8 bits and they are set by the sender, with the data bit 110 needs to transfer to the receiver. This block followed by an ACK/NACK bit and is set to 0, by the receiver, if it successfully receives data. Otherwise stays at 1.

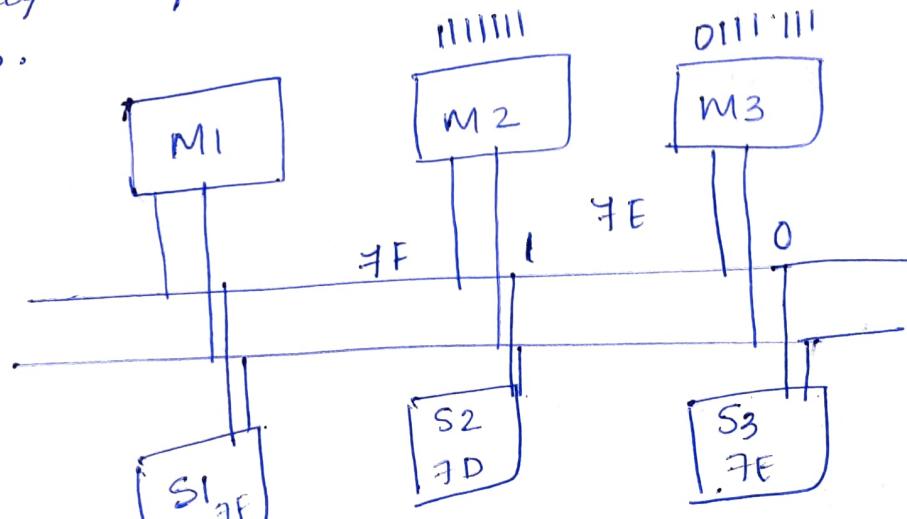
The combination of data-bit block followed by ACK/NACK bit is repeated until the data is completely transferred.

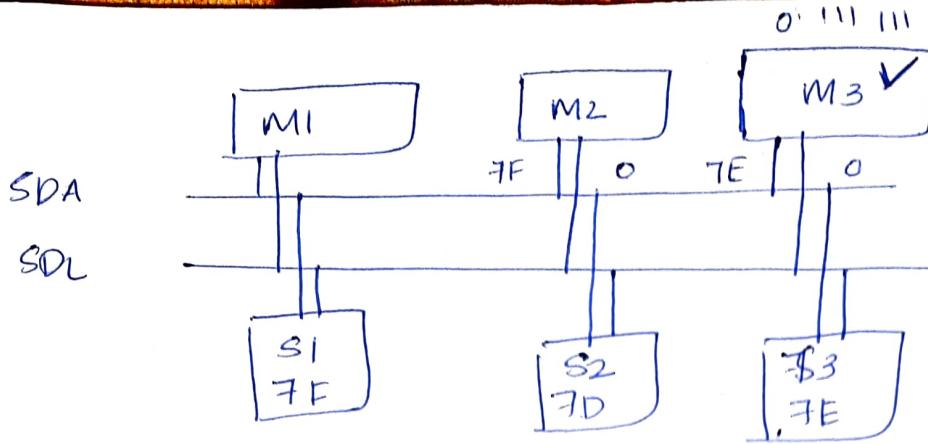
**Stop condition:** After sending data blocks are transferred to the SDA line, the master devices switches the SDA line from low voltage level to high voltage level before the SCL line switches from high to low.



⑭. Explain the arbitration process in I2C?

The arbitration occurs when two masters start a transfer at a same time. During the transfer the masters constantly monitor SDA and SCL. If one of them detects that SDA is low when it should actually be high, it assumes that another master is high active and immediately stops its transfer. This process is called arbitration.

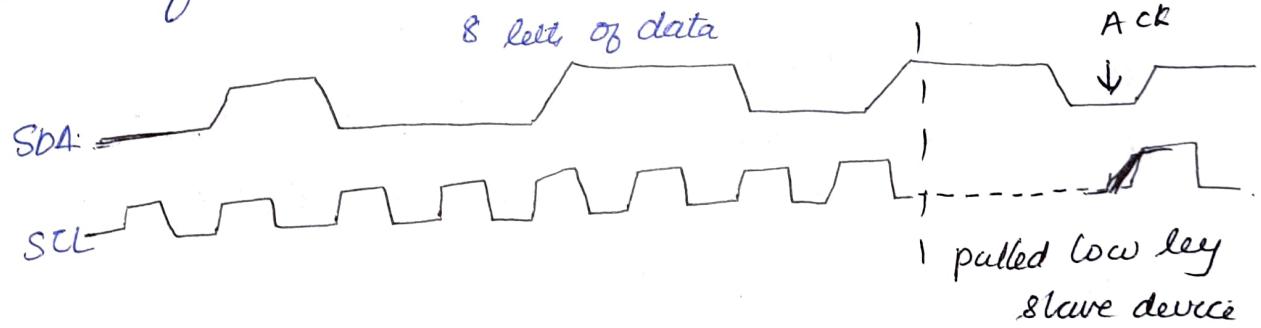




Here both M<sub>2</sub> and M<sub>3</sub> wants to send data, but here M<sub>3</sub> will get the bus and M<sub>2</sub> will wait until the M<sub>3</sub> completes its process.

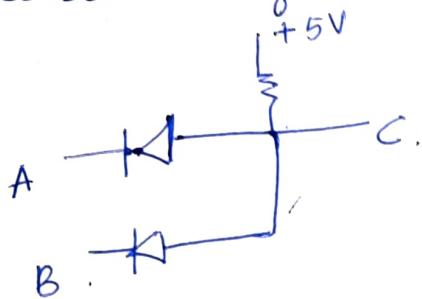
- 15 Explain the process of clock stretching in I<sub>2</sub>C with neat diagram?

I<sub>2</sub>C device can slow down its communication by stretching SCL. During an SCL low phase, any I<sub>2</sub>C device on the bus may additionally hold down SCL to prevent it from rising again, enabling to slow down the SCL clock rate or to stop I<sub>2</sub>C communication for a while. This is also referred as clock synchronization.



16. Explain the WIRED AND logic, how it is used in SPI?

The wired AND connection is a form of AND gate. It uses pull up resistors and one diode per input to achieve this fn.



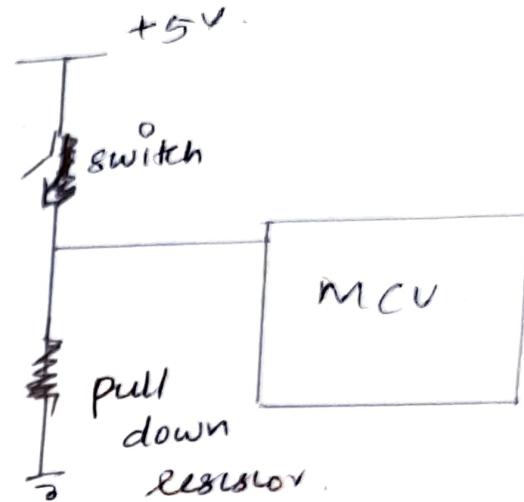
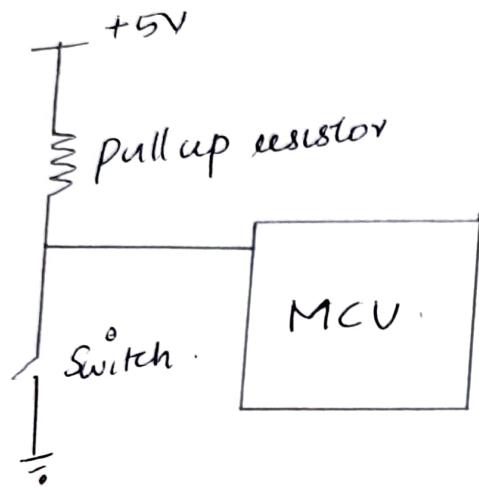
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

one pulled low  
then wire stays  
low

⑭ Explain How open drain helps in I<sub>2</sub>C.

I<sub>2</sub>C bus drivers are open drains, meaning that they can pull the corresponding signal line low, but cannot drive it high. Thus there can be no bus contention where one device is trying to drive the line while another tries to pull it low, eliminating the potential for damage to the devices or excessive power dissipation. Each line has a pull up resistor on it, to release the signal to high when no device is asserting it low.

(18)



There are some cases, we need to change the pins from 0 to 1 or 1 to 0. In either case we need to hold the digital pin either 0 and then change the state to 0 or we need to hold 1 and then change to 1. Both the cases we need to change pin high or low.

A pullup resistor is used to make default state of digital pin as High or to the logic level and a pulldown resistor make the default state Low.