KiCad PCB Design Checklist - ESP32-S3 Industrial IoT

Pre-Design Setup

KiCad Installation & Configuration	
☐ Install KiCad 7.0 or later	
■ Download ESP32-S3 symbol and footprint libraries	
Configure design rules for 4-layer PCB	
Set up component libraries (Digikey, Mouser, etc.)	
Configure 3D model libraries for visualization	
Project Setup	
Create new KiCad project	
Set up Git repository for version control	
Create project folder structure	
Configure project-specific libraries	
Set up design rule check (DRC) rules	
Schematic Design Checklist	
1. ESP32-S3 Module Section	
Components:	
■ ESP32-S3-WROOM-1 module (or ESP32-S3-WROOM-1U for external antenna)	
■ 10µF + 100nF decoupling capacitors on VDD	
\square 10k Ω pull-up on EN (enable) pin	
\square 470 Ω series resistor on USB D+/D- if using USB	
\blacksquare Boot mode resistors (10k Ω pull-up on GPIO0, pull-down on GPIO46)	
Schematic Requirements:	
All power pins connected to appropriate rails	
Proper decoupling capacitor placement	
■ Boot and reset circuitry	
■ Programming interface (USB-C or UART)	
☐ Unused pins properly handled (pulled up/down or left floating per datasheet)	

2. Power Management System

Battery Charging Circuit (MCP73831):
■ MCP73831T-2ACI/OT Li-Po charging IC $ 2kΩ \text{ resistor (PROG pin) for 500mA charge current} $ $ 4.7μF \text{ input capacitor} $ $ 4.7μF \text{ output capacitor} $ $ Status \text{ LED with } 470Ω \text{ resistor} $ $ Thermal pad connection to ground plane $
3.3V Regulation (AMS1117-3.3):
 AMS1117-3.3 linear regulator 10μF input capacitor (tantalum or ceramic) 22μF output capacitor Power LED with 1kΩ resistor Thermal considerations for continuous operation
Power Distribution:
 □ Battery voltage rail (VBAT) - 3.7V nominal □ Regulated 3.3V rail (VDD) - main system power □ Sensor power rail (VSENSOR) - switchable sensor power □ Load switches (AP2112K) for sensor power control □ Power selection circuit (battery vs USB)
3. Sensor Interface Circuits
I2C Interface (BME280 Environmental Sensor):
 BME280 or SHT30 sensor footprint 4.7kΩ pull-up resistors on SDA and SCL 100nF bypass capacitor on sensor VDD ESD protection diodes (optional) Address selection jumper (if applicable)
SPI Interface (ADXL345 Accelerometer):
□ ADXL345 or ICM-20948 sensor footprint □ 100nF bypass capacitor on sensor VDD □ Series resistors on SPI lines (22Ω) for signal integrity □ Chip select pull-up resistor ($10k\Omega$) □ Interrupt pins routed to ESP32-S3 GPIO

ADC Interface (ACS/12 Current Sensor):
 □ ACS712-05B current sensor IC □ 100nF bypass capacitor □ 1µF filter capacitor on output □ Voltage divider for ADC scaling (if needed) □ TVS diode for input protection
4. Industrial I/O Section
Connectors:
 USB-C connector for programming and charging 3.5mm screw terminals for sensor connections 2.54mm header for GPIO expansion SWD programming header (Tag-Connect or standard)
User Interface:
□ Power LED (green) with $1k\Omega$ resistor □ Status LED (blue) with 470Ω resistor □ Error LED (red) with 470Ω resistor □ Reset button (tactile switch) with $10k\Omega$ pull-up □ Boot button (tactile switch) with $10k\Omega$ pull-up
Protection Circuits:
 Reverse polarity protection (P-channel MOSFET) Overcurrent protection (PTC fuse, 1A) ESD protection on all external interfaces TVS diodes on power inputs
5. Schematic Review Checklist
Power System:
 All ICs have proper power connections Decoupling capacitors on all power pins Power-on reset circuits properly implemented Current consumption calculated and within limits
Signal Integrity:
☐ High-speed signals kept short

Proper impedance matching considered
☐ Clock signals properly routed
☐ Unused pins properly handled
Component Selection:
☐ All components available from reliable suppliers
☐ Temperature ratings suitable for application
Package sizes suitable for hand assembly
Cost optimization completed
Design Rules:
☐ Electrical Rules Check (ERC) passed
☐ All nets properly named
Component values and part numbers specified
☐ Footprint assignments completed
PCB Layout Design Checklist 1. PCB Stackup Configuration
4-Layer Stackup:
Layer 1 (Top): Signal + Components [0.035mm Cu]
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Crystal/oscillator components close to IC pins
☐ Power management ICs near power input
☐ Heat-sensitive components away from power ICs
Placement Rules:
☐ Components oriented for easy hand assembly
☐ Test points accessible for debugging
☐ Connectors at board edges
LEDs visible when assembled
☐ Buttons accessible for user interaction
3. Power and Ground Plane Design
Ground Plane (Layer 2):
Solid ground plane with minimal splits
☐ Ground plane connected to all ground pins
☐ Thermal relief on ground connections
☐ Via stitching between ground planes
Ground plane extends under all ICs
Power Plane (Layer 3):
Power Plane (Layer 3): ☐ Separate power islands: +3.3V, +VBAT, +VSENSOR
-
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Separate power islands: +3.3V, +VBAT, +VSENSOR Power planes sized for current requirements Thermal vias under power ICs Power plane clearance from ground plane Power plane connected via multiple vias 4. High-Speed Signal Routing ESP32-S3 Critical Signals: SPI flash signals kept short (<10mm) USB differential pair routed as 90Ω differential
Separate power islands: +3.3V, +VBAT, +VSENSOR Power planes sized for current requirements Thermal vias under power ICs Power plane clearance from ground plane Power plane connected via multiple vias 4. High-Speed Signal Routing ESP32-S3 Critical Signals: SPI flash signals kept short (<10mm) USB differential pair routed as 90Ω differential High-speed GPIO signals have controlled impedance
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 Minimize layer changes on critical signals Proper termination on long traces Avoid routing under crystal/oscillator Ground return path provided for all signals
5. Sensor Interface Routing
I2C Bus Routing:
 SDA and SCL routed parallel with same length Pull-up resistors close to bus master (ESP32-S3) Bus traces away from switching circuits Proper ground return path ESD protection at connector interfaces
SPI Bus Routing:
 Clock signal routed first with shortest path Data signals length-matched to clock Chip select signals properly routed Ground plane under SPI traces Series termination resistors if needed
ADC Signal Routing:
 Analog signals away from switching circuits Proper ground plane separation (analog/digital) Filter capacitors close to ADC inputs Shielded or differential routing if needed Reference voltage properly filtered
6. Power Distribution Network
Power Routing:
Power traces sized for current requirements Multiple vias for power connections Decoupling capacitors optimally placed Power and ground planes properly connected Thermal management for power ICs

Current Calculations:

 Trace width calculated for maximum current Via current capacity verified Thermal rise calculated for power dissipation Voltage drop analysis completed
Power budget analysis documented
7. EMI/EMC Considerations
EMI Reduction:
 Proper ground plane coverage (>80%) High-frequency bypass capacitors Ferrite beads on power lines Avoid antenna-like trace structures Proper shielding of high-speed signals
EMC Compliance:
 All external cables properly filtered ESD protection on all interfaces Proper ground connection strategy Avoid ground loops Clock signals properly contained
8. Manufacturing Considerations
Design for Manufacturing (DFM):
 Minimum trace width: 0.1mm (4 mil) Minimum via size: 0.2mm (8 mil) drill Minimum spacing: 0.1mm (4 mil) Solder mask sliver: >0.1mm Silkscreen text: >0.15mm height
Assembly Considerations:
 Components oriented for pick-and-place Fiducial markers for automated assembly Panel design for multiple PCBs Test points for automated testing Proper solder mask openings

9. Testing and Debug Features

Test Points:
Power rail test points (VDD, VBAT, etc.) Critical signal test points Ground test points ADC reference test points Communication bus test points
Debug Features:
 SWD programming header accessible UART debug pins available LED indicators for system status Jumpers for configuration changes Spare GPIO pins brought out for expansion
10. Final Design Verification
Design Rule Check (DRC):
 All DRC violations resolved Minimum trace width/spacing verified Via size and drill size verified Solder mask clearance verified Component clearance verified
Electrical Verification:
 Net connectivity verified Power and ground connections verified Signal integrity analysis completed Impedance calculations verified Thermal analysis completed
Manufacturing Files:

Component Selection Database

ESP32-S3 Module Options:

- ESP32-S3-WROOM-1: PCB antenna, 16MB Flash, 8MB PSRAM
- ESP32-S3-WROOM-1U: U.FL connector, 16MB Flash, 8MB PSRAM
- **ESP32-S3-MINI-1**: Smaller footprint, 8MB Flash, 8MB PSRAM

Power Management ICs:

- MCP73831T-2ACI/OT: 500mA Li-Po charger, SOT-23-5
- **AMS1117-3.3**: 1A LDO regulator, SOT-223
- AP2112K-3.3: 600mA LDO regulator, SOT-23-5
- TPS63070: Buck-boost converter for battery operation

Sensor Components:

- **BME280**: Environmental sensor (temp/humidity/pressure)
- SHT30: High-accuracy temperature/humidity sensor
- **