ΘΈΜΑ ΠΤΥΧΙΑΚΉΣ ΕΡΓΑΣΊΑΣ :

ΥΛΟΠΟΙΗΣΗ ΚΑΙ ΠΡΟΣΟΜΟΙΩΣΗ ΤΟΥ MICROBLAZE ΕΠΕΞΕΡΓΑΣΤΗ ΣΕ FPGA

ΑΡΙΘΜΌΣ ΜΗΤΡΏΟΥ :

2026202100134

ΟΝΟΜΑΤΕΠΏΝΥΜΟ :

ΑΝΑΣΤΆΣΙΟΣ ΠΟΥΤΑΧΊΔΗΣ

ΠΑΝΕΠΙΣΤΉΜΙΟ :

Πελοποννήσου.

ΤΜΉΜΑ :

Ψηφιακών Συστημάτων.

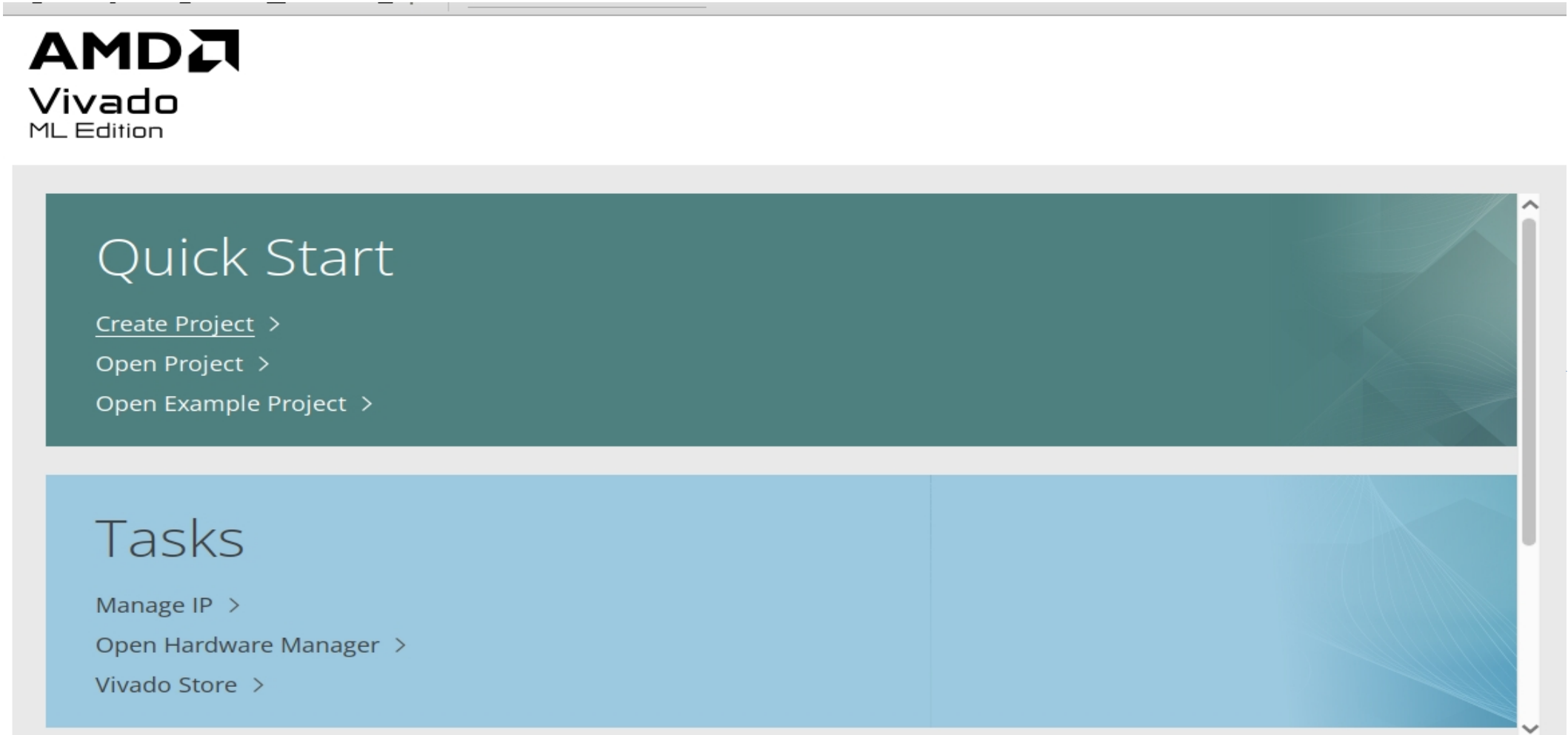
ΠΑΡΟΥΣΊΑΣΗ :

Πτυχιακής Εργασίας 20'.

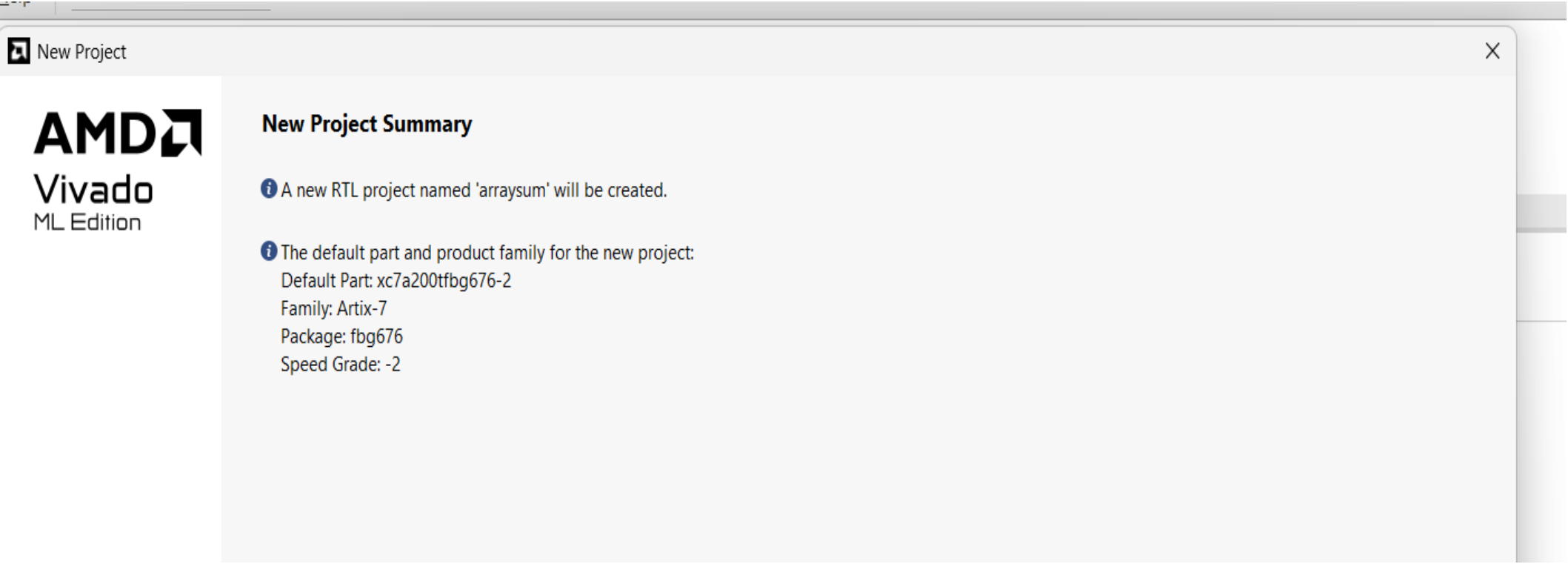
ΕΡΓΑΛΕΊΑ ΥΛΟΠΟΊΗΣΗΣ :

Vitis(SW DEVELOPER)2023.2

Click : Create Project > .



Project Name : arraysum
Xilinx Board Part : xc7a200tfbg676-2



Create Block Design :
Add MicroBlaze and Run Block Automation.

arraysum - [C:/Users/znkr_/Desktop/arraysum/arraysum.xpr] - Vivado 2023.2

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready

Default Layout

Flow Navigator

- **PROJECT MANAGER**
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- **IP INTEGRATOR**
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- **SIMULATION**
  - Run Simulation
- **RTL ANALYSIS**
  - Run Linter
  - Open Elaborated Design
- **SYNTHESIS**
  - Run Synthesis
  - Open Synthesized Design
- **IMPLEMENTATION**
  - Run Implementation
  - Open Implemented Design

BLOCK DESIGN - design_1 *

Sources | Design | Signals

design_1

microblaze_0 (MicroBlaze:11.0)

Properties

Select an object to see properties

Diagram | Address Editor

Default View

Designer Assistance available. Run Block Automation

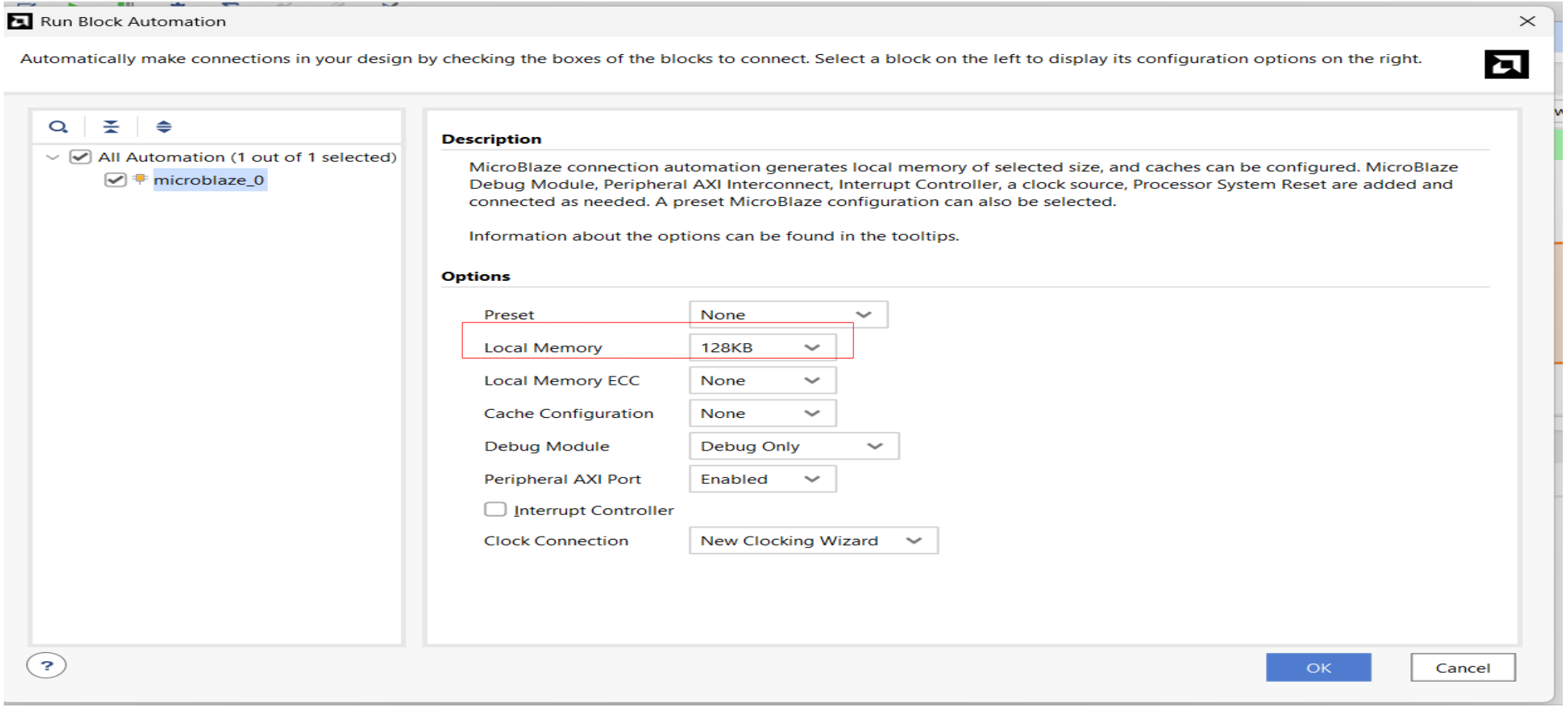
Tcl Console | Messages | Log | Reports | Design Runs

```
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2023.2/data/ip'.
create_project: Time (s): cpu = 00:00:14 ; elapsed = 00:00:06 . Memory (MB): peak = 1418.355 ; gain = 0.000
set_property target_language VHDL [current_project]
create_bd_design "design_1"
Wrote  : <C:\Users\znkr_\Desktop\arraysum\arraysum.srcs\sources_1\bd\design_1\design_1.bd>
update_compile_order -fileset sources_1
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:microblaze:11.0 microblaze_0
endgroup
```

Type a Tcl command here

Set : Local Memory 128KB and Click OK.

(Improves Performance).



Click : Run Connection Automation.

arraysum - [C:/Users/znkr_/Desktop/arraysum/arraysum.xpr] - Vivado 2023.2

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready

Default Layout

Flow Navigator

- **PROJECT MANAGER**
  - Settings
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BLOCK DESIGN - design_1 *

Sources | Design | Signals

- design_1
  - Interface Connections
  - Nets
  - clk_wiz_1 (Clocking Wizard:6.0)
  - mdm_1 (MicroBlaze Debug Module (MDM):3.2)

Block Properties

clk_wiz_1

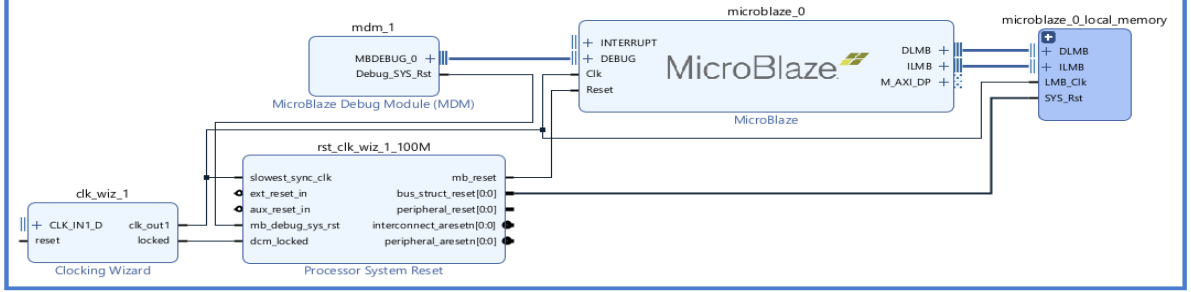
Name: clk_wiz_1

General | Properties | IP

Diagram | Address Editor

Default View

Designer Assistance available. Run Connection Automation

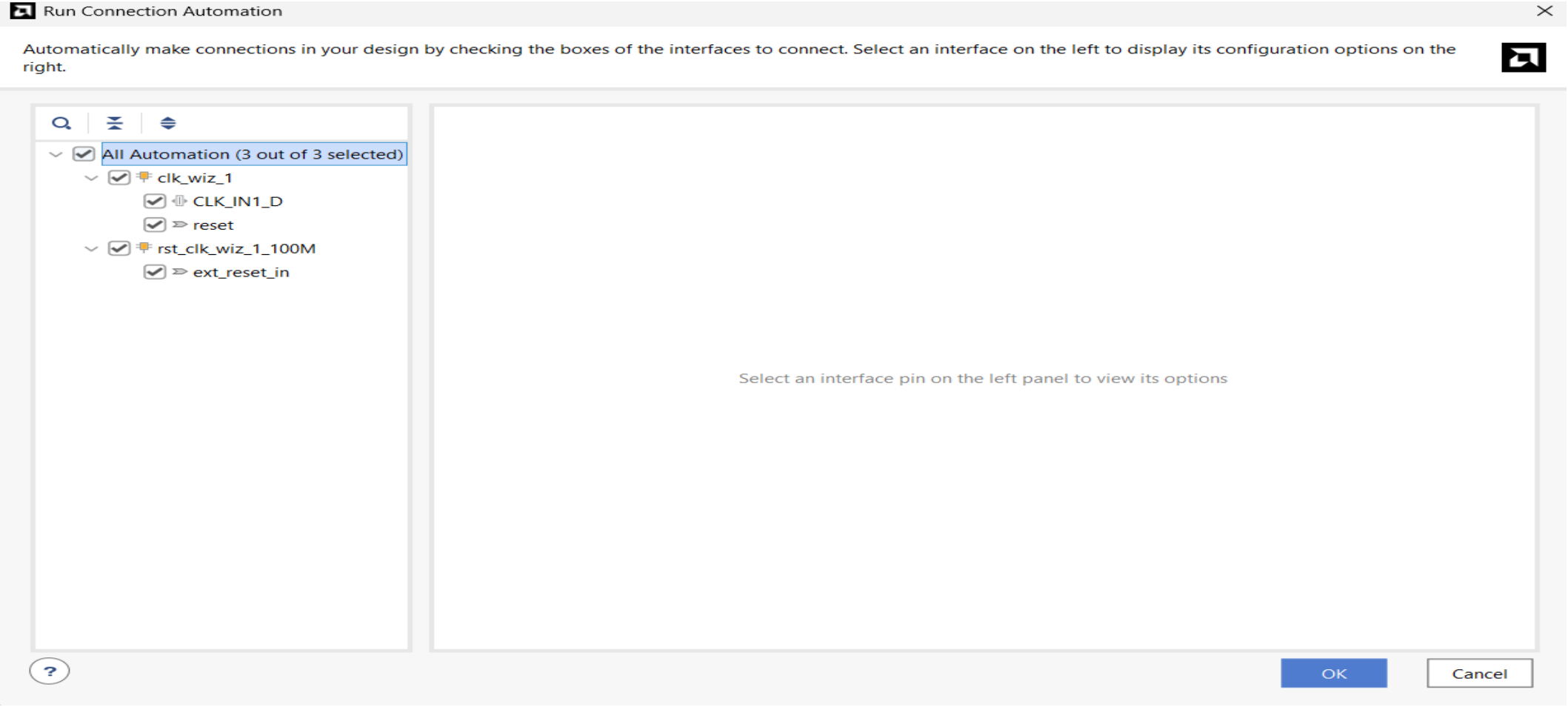


Tcl Console | Messages | Log | Reports | Design Runs

```
update_compile_order -fileset sources_1
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:microblaze:11.0 microblaze_0
endgroup
apply_bd_automation -rule xilinx.com:bd_rule:microblaze -config { axi_intc {0} axi_periph {Enabled} cache {None} clk {New Clocking Wizard} cores {1} debug_module {Debug On
INFO: [Device 21-403] Loading part xc7a200tfbg676-2
create_bd_cell: Time (s): cpu = 00:00:10 ; elapsed = 00:00:22 . Memory (MB): peak = 1907.121 ; gain = 446.688
WARNING: [BD 5-700] No address spaces matched 'get_bd_addr_spaces /microblaze_0'
apply_bd_automation: Time (s): cpu = 00:00:22 ; elapsed = 00:00:34 . Memory (MB): peak = 1907.121 ; gain = 488.766
regenerate_bd_layout
```

Type a Tcl command here

Select : All(3 out of 3 selected) <u>and</u> Click OK.



Add BRAM and Run Connection Automation.

(BRAM : boosts system performance by minimizing the delay in data access).

arraysum - [C:/Users/znkr_/Desktop/arraysum/arraysum.xpr] - Vivado 2023.2

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready

Default Layout

Flow Navigator

- PROJECT MANAGER
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
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  - Open Implemented Design

BLOCK DESIGN - design_1 *

Sources | Design | Signals

- design_1
  - External Interfaces
  - Interface Connections
  - Ports
  - Nets

Block Properties

clk_wiz_1

Name: clk_wiz_1

General | Properties | IP

Diagram | Address Editor

Default View

Designer Assistance available. Run Connection Automation

axi_bram_ctrl_0 (S_AXI, s_axi_aclk, s_axi_aresetn, BRAM_PORTA, BRAM_PORTB) — AXI BRAM Controller

mdm_1 (MBDEBUG_0, Debug_SYS_Rst) — MicroBlaze Debug Module (MDM)

microblaze_0 (INTERRUPT, DEBUG, Clk, Reset, DLMB, ILMB, M_AXI_DP) — MicroBlaze

clk_wiz_1 (CLK_IN1_D, reset, clk_out1, locked) — Clocking Wizard

rst_clk_wiz_1_100M (slowest_sync_clk, ext_reset_in, aux_reset_in, mb_reset, bus_struct_reset[0:0], peripheral_reset[0:0])

diff_clock_rtl_0

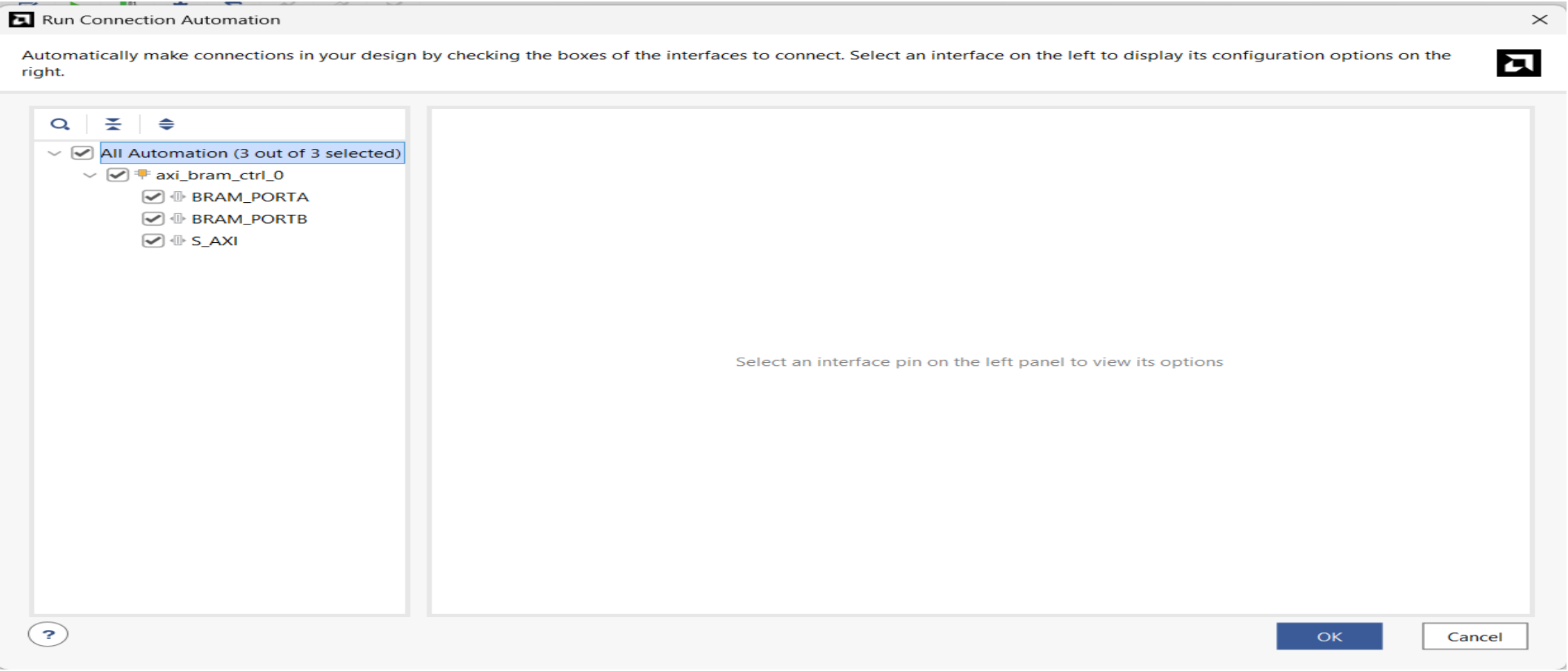
reset_rtl_0

Tcl Console | Messages | Log | Reports | Design Runs

```
INFO: [BoardRule 102-7] set_property CONFIG.POLARITY ACTIVE_LOW /reset_rtl_0
INFO: [BoardRule 102-15] connect_bd_net /reset_rtl_0 /rst_clk_wiz_1_100M/ext_reset_in
INFO: [BoardRule 102-19] set_property CONFIG.POLARITY ACTIVE_LOW /reset_rtl_0
endgroup
regenerate_bd_layout
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:axi_bram_ctrl:4.1 axi_bram_ctrl_0
INFO: [xilinx.com:ip:axi_bram_ctrl:4.1-2] design_1_axi_bram_ctrl_0_0: In IP Integrator, please note that memory depth value gets calculated based on the Data Width of the
INFO: [xilinx.com:ip:axi_bram_ctrl:4.1-1] design_1_axi_bram_ctrl_0_0: In IP Integrator, The Maximum address range supported is 2G. Selecting the address range more than 2G
endgroup
```

Type a Tcl command here

Select : All(3 out of 3 selected) <u>and</u> Click OK.

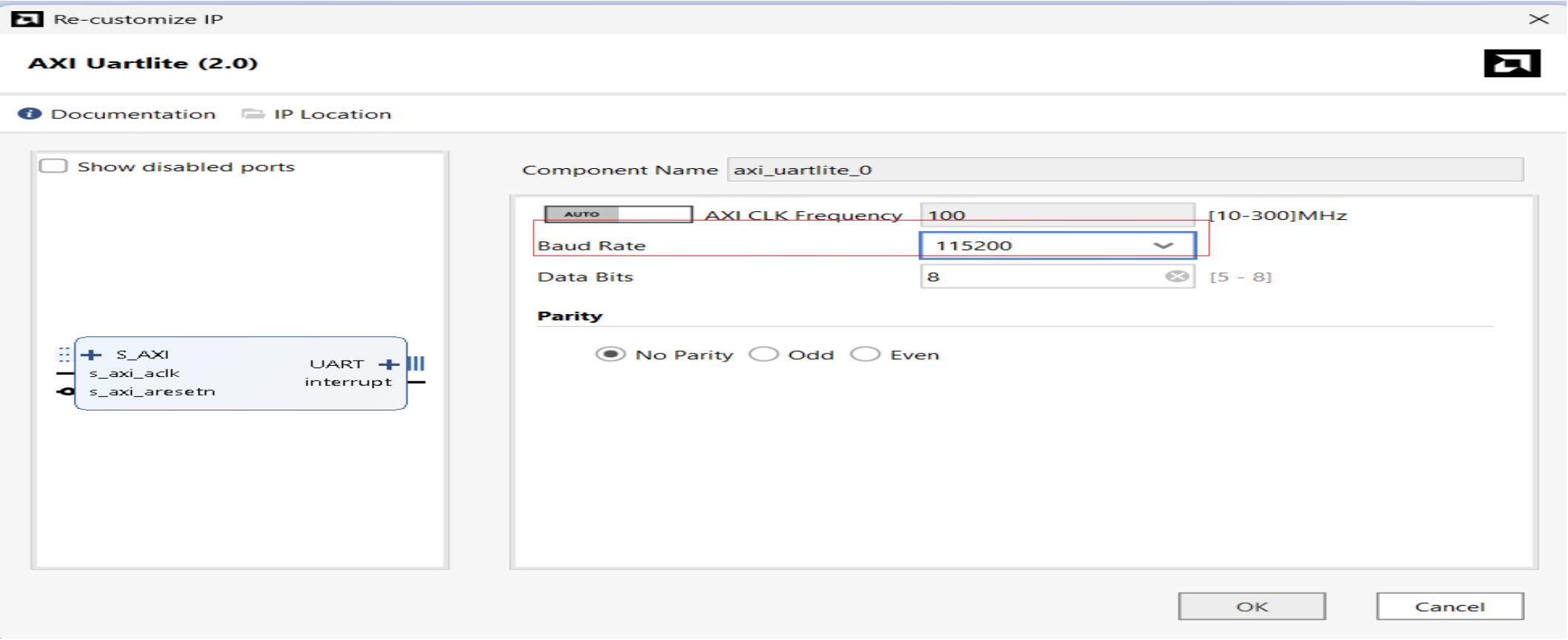


Add UART and Set : Baud Rate 115200.

Baud Rate:
Symbols/Second

(My testbench is written for this baud rate).

(UART : MicroBlaze can send and receive serial data with external devices).



Click : Run Connection Automation.

arraysum - [C:/Users/znkr_/Desktop/arraysum/arraysum.xpr] - Vivado 2023.2

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready

Default Layout

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- PROJECT MANAGER
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
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BLOCK DESIGN - design_1 *

Sources | Design | Signals

- design_1
  - External Interfaces
  - Interface Connections
  - Ports
  - Nets

Block Properties

axi_uartlite_0

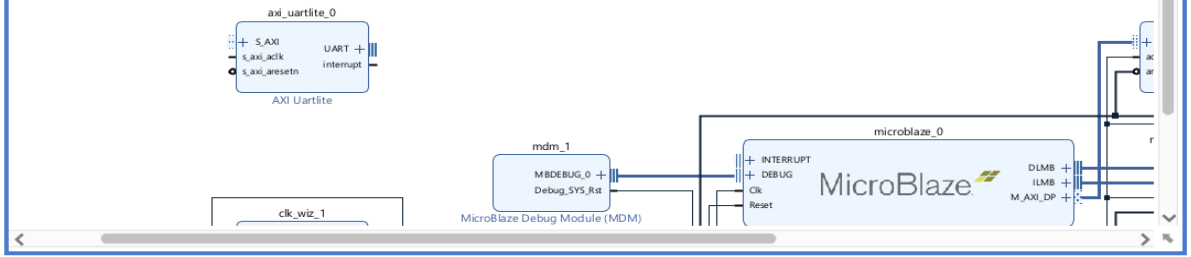
Name: axi_uartlite_0

General | Properties | IP

Diagram | Address Editor

Default View

Designer Assistance available. Run Connection Automation

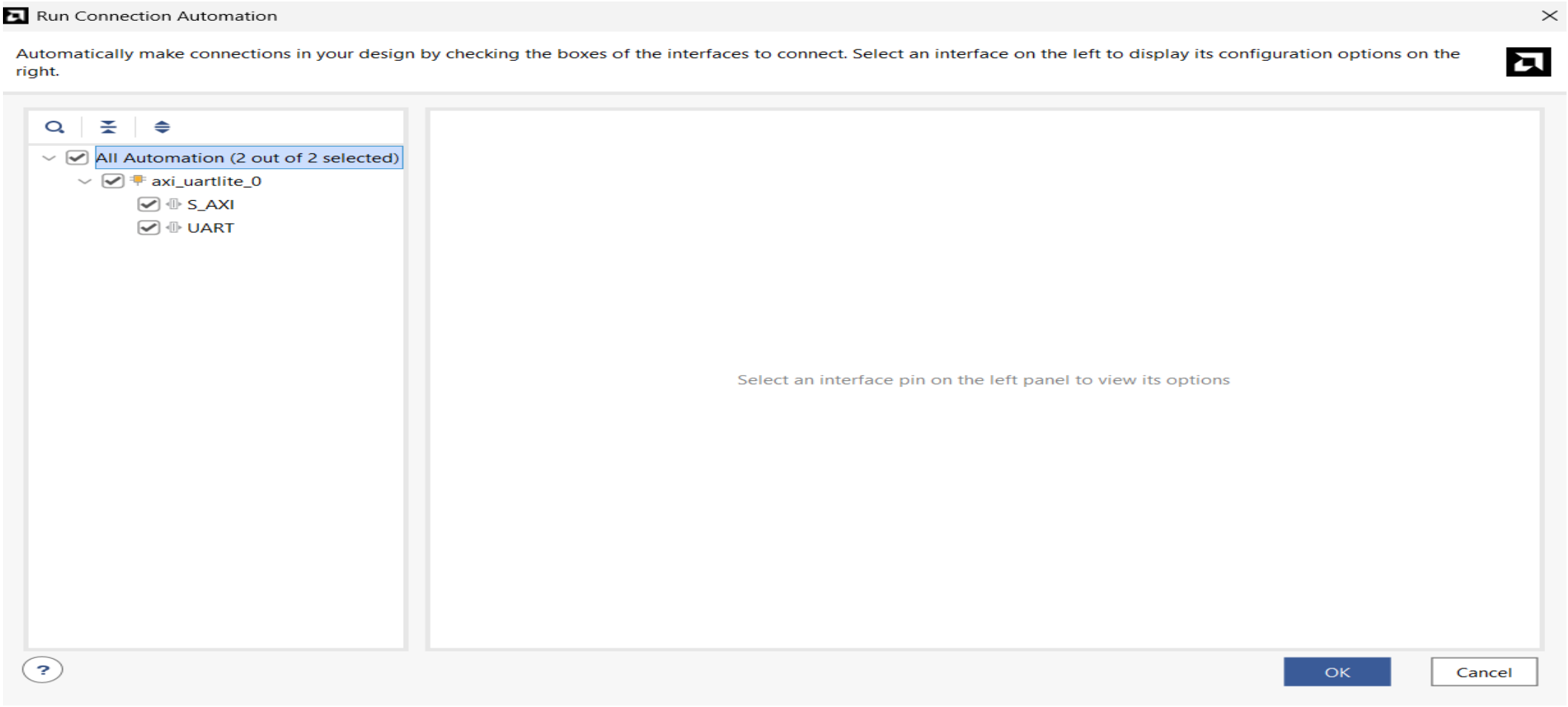


Tcl Console | Messages | Log | Reports | Design Runs

```
apply_bd_automation -rule xilinx.com:bd_rule:bram_cntlr -config {BRAM "Auto" }  [get_bd_intf_pins axi_bram_ctrl_0/BRAM_PORTB]
apply_bd_automation -rule xilinx.com:bd_rule:axi4 -config { Clk_master {/clk_wiz_1/clk_out1 (100 MHz)} Clk_slave {Auto} Clk_xbar {Auto} Master {/microblaze_0 (Periph)} Sla
Slave segment '/axi_bram_ctrl_0/S_AXI/Mem0' is being assigned into address space '/microblaze_0/Data' at <0xC000_0000 [ 8K ]>.
endgroup
regenerate_bd_layout
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:axi_uartlite:2.0 axi_uartlite_0
endgroup
set_property location {2 392 81} [get_bd_cells axi_uartlite_0]
set_property CONFIG.C_BAUDRATE {115200} [get_bd_cells axi_uartlite_0]
```

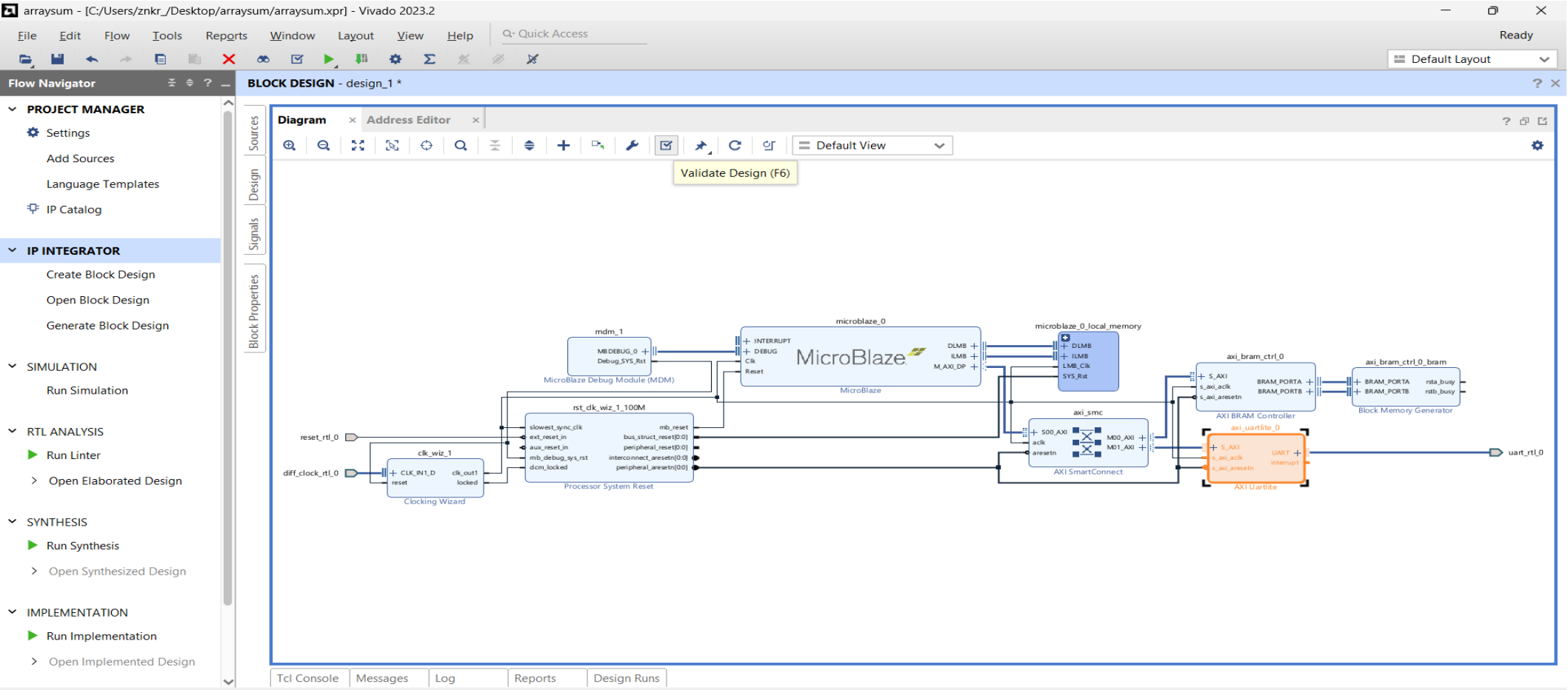
Type a Tcl command here

Select : All(3 out of 3 selected) <u>and</u> Click OK.



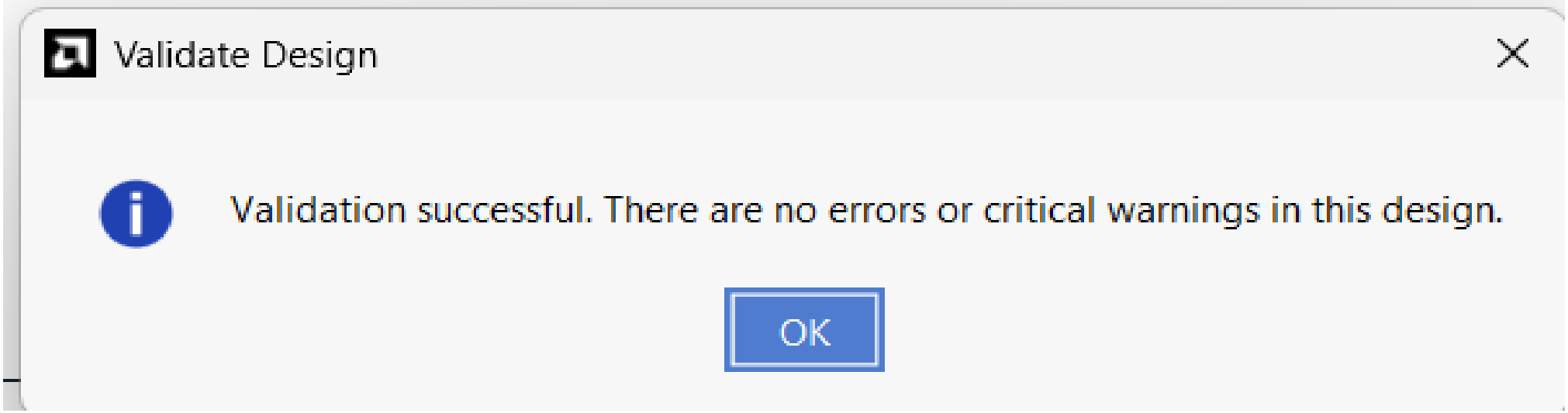
Click : Validate Design (F6).

(Given : The Form Of The Block Design).



Click : OK. <u>If</u> <u>The</u> Validation <u>Is</u> Successful.

<u>(This window will open).</u>



Click : Generate Output Products…

(For synthesizing the design and implementing it to test the system).

arraysum - [C:/Users/znkr_/Desktop/arraysum/arraysum.xpr] - Vivado 2023.2

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready

Default Layout

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- PROJECT MANAGER
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
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BLOCK DESIGN - design_1 *

Source File Properties

Sources | Design | Signals

- Design Sources (1)
- Constraints
- Simulation Sources (1)
  - sim_1 (1)
    - design_1 (design_1.bd
- Utility Sources

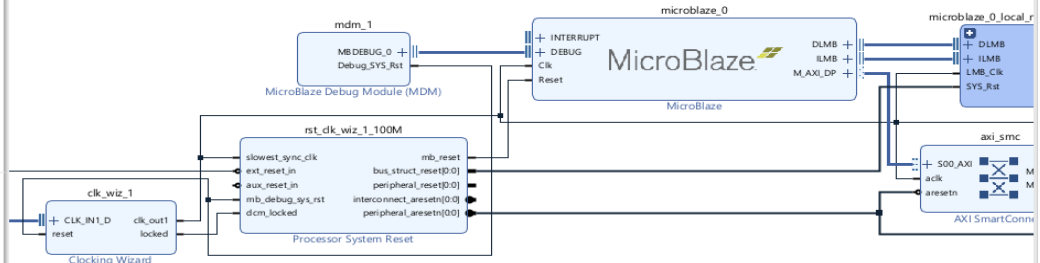
Hierarchy | IP Sources | Libraries

Tcl Console | Messages | Log

Source Node Properties... Ctrl+E
Open File Alt+O
Open With
Create HDL Wrapper...
View Instantiation Template
Generate Output Products...
Reset Output Products...
Replace File...
Copy File Into Project
Copy All Files Into Project Alt+I
Remove File from Project... Delete
Enable File Alt+Equals
Disable File Alt+Minus
Hierarchy Update
Refresh Hierarchy
IP Hierarchy
Set as Top
Add Module to Block Design
Set File Type...
Set Used In...
Copy Constraints Set...
Edit Constraints Sets...
Edit Simulation Sets...
Associate ELF Files...

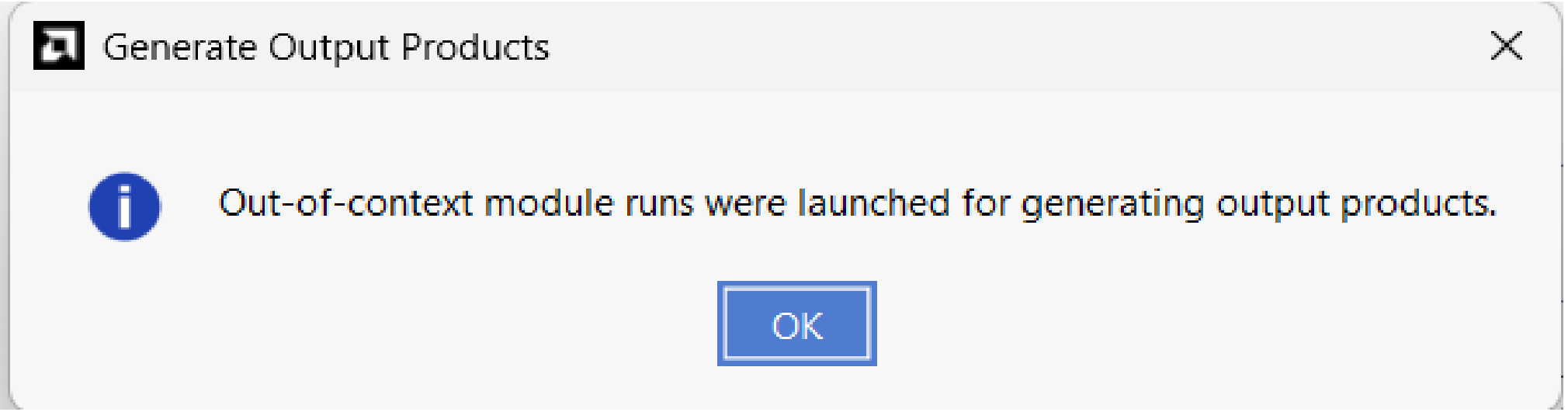
Diagram | Address Editor

Default View



Click : OK. *<u>If the</u>* ***synthesis*** *<u>and</u>* ***implementation*** *<u>are</u>* ***successful.***

<u>(This window will open).</u>



Click : Create HDL Wrapper…

(Manages the design within the FPGA).

arraysum - [C:/Users/znkr_/Desktop/arraysum/arraysum.xpr] - Vivado 2023.2

File Edit Flow Tools Reports Window Layout View Help Quick Access

Running multiple block runs Cancel

Default Layout

Flow Navigator

- **PROJECT MANAGER**
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
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BLOCK DESIGN - design_1

Source File Properties

Sources | Design | Signals

- Design Sources (1)
- Constraints
- Simulation Sources (1)
  - sim_1 (1)
    - design_1 (design_1.bd)
- Utility Sources

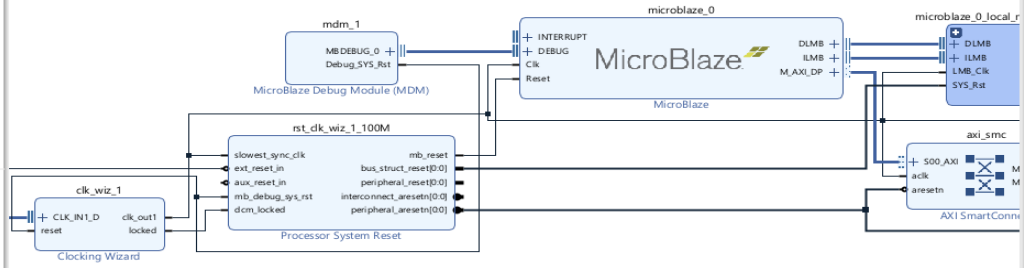
Hierarchy | IP Sources | Libraries

Tcl Console | Messages | Log

Diagram | Address Editor

Default View

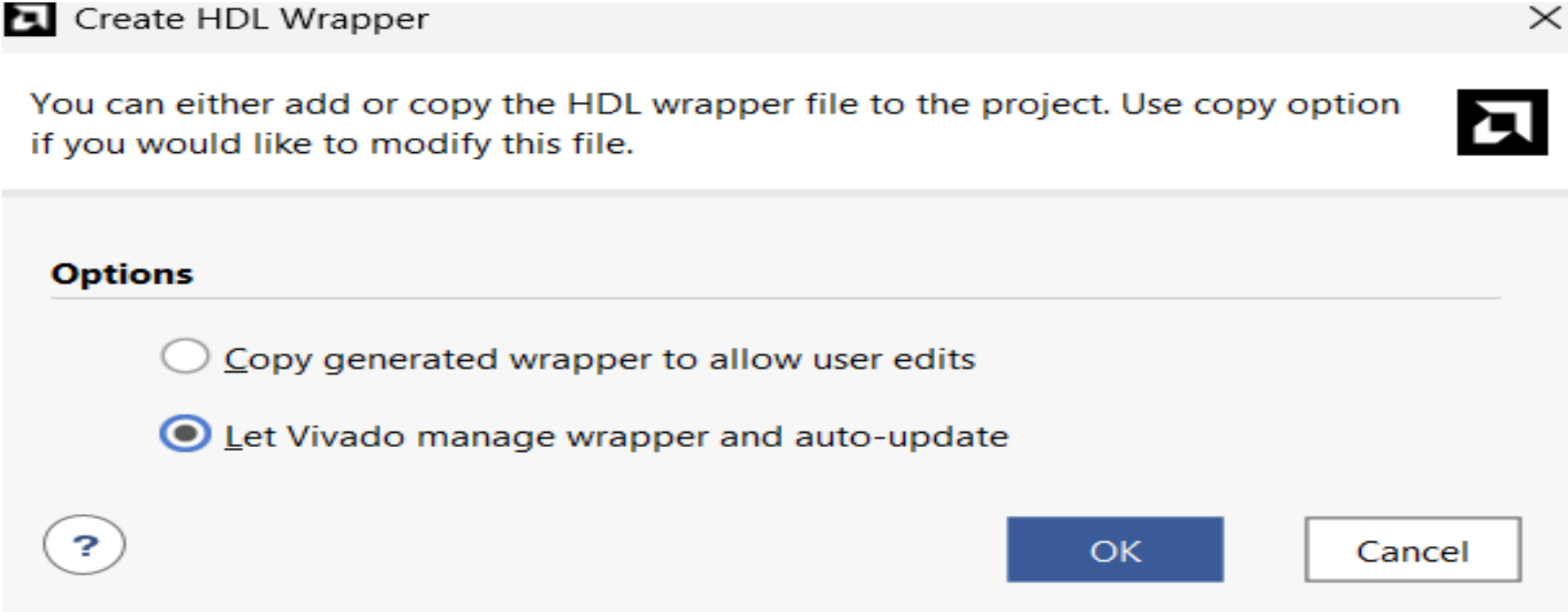
- Source Node Properties... Ctrl+E
- Open File Alt+O
- Open With
- Create HDL Wrapper...
- View Instantiation Template
- Generate Output Products...
- Reset Output Products...
- Replace File...
- Copy File Into Project
- Copy All Files Into Project Alt+I
- Remove File from Project... Delete
- Enable File Alt+Equals
- Disable File Alt+Minus
- Hierarchy Update
- Refresh Hierarchy
- IP Hierarchy
- Set as Top
- Add Module to Block Design
- Set File Type...
- Set Used In...
- Copy Constraints Set...
- Edit Constraints Sets...
- Edit Simulation Sets...
- Associate ELF Files...



Generate HDL wrapper file and copy into project

Click : OK.

(Let Vivado manage wrapper and auto-update).



HDL Wrapper Generated.

(With name : design_1_wrapper.vhd).

arraysum - [C:/Users/znkr_/Desktop/arraysum/arraysum.xpr] - Vivado 2023.2

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready

Default Layout

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  - Settings
  - Add Sources
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BLOCK DESIGN - design_1

Source File Properties

Sources | Design | Signals

- Design Sources (1)
- Constraints
- Simulation Sources (1)
  - sim_1 (1)
    - **design_1_wrapper**(STRUCTURE) (design_1_wrapper.vhd) (1)
      - design_1_i : design_1 (design_1.bd) (1)
        - design_1(STRUCTURE) (design_1.vhd) (9)
- Utility Sources

Hierarchy | IP Sources | Libraries | Compile Order

Diagram | Address Editor | design_1_wrapper.vhd

c:/Users/znkr_/Desktop/arraysum/arraysum.gen/sources_1/bd/design_1/hdl/design_1_wrapper.vhd

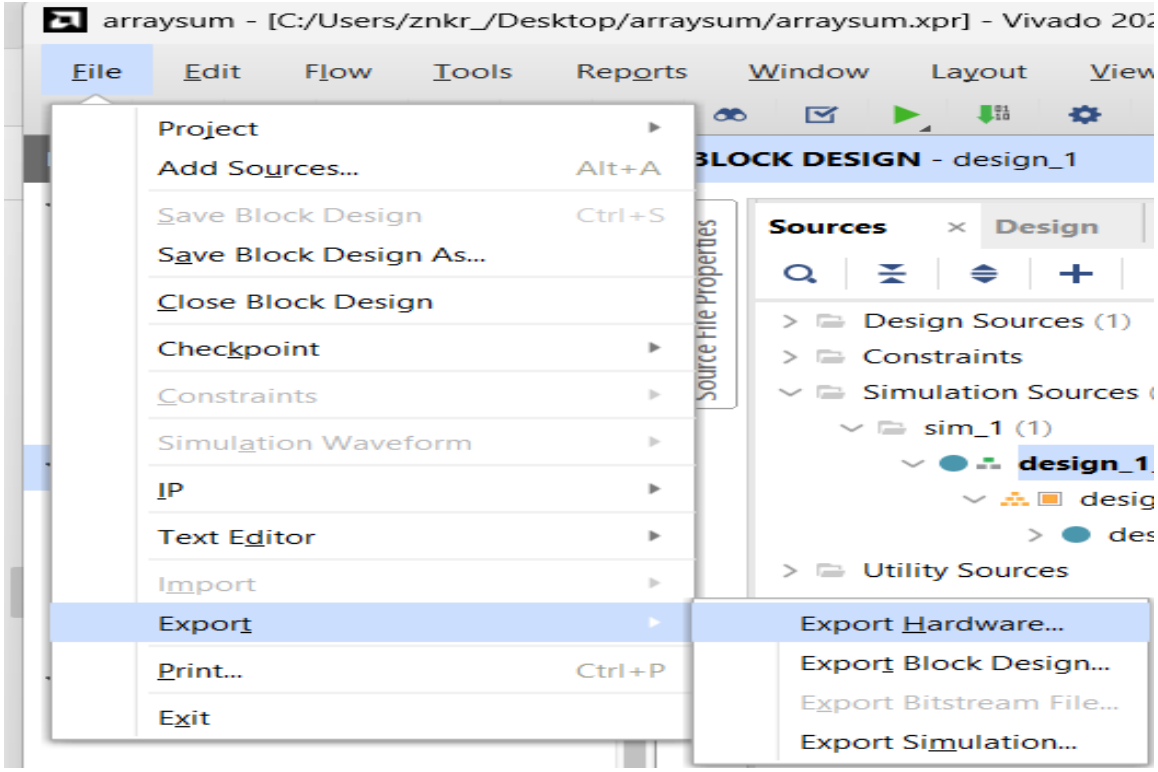
```vhdl
--Copyright 1986-2022 Xilinx, Inc. All Rights Reserved.
--Copyright 2022-2023 Advanced Micro Devices, Inc. All Rights Reserved.
--------------------------------------------------------------------------------
--Tool Version: Vivado v.2023.2 (win64) Build 4029153 Fri Oct 13 20:14:34 MDT 2023
--Date         : Fri Dec 27 16:52:20 2024
--Host         : rev_sharped running 64-bit major release  (build 9200)
--Command      : generate_target design_1_wrapper.bd
--Design       : design_1_wrapper
--Purpose      : IP block netlist
--------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
library UNISIM;
use UNISIM.VCOMPONENTS.ALL;
entity design_1_wrapper is
  port (
    diff_clock_rtl_0_clk_n : in STD_LOGIC;
    diff_clock_rtl_0_clk_p : in STD_LOGIC;
    reset_rtl_0 : in STD_LOGIC;
    uart_rtl_0_rxd : in STD_LOGIC;
    uart_rtl_0_txd : out STD_LOGIC
  );
end design_1_wrapper;

architecture STRUCTURE of design_1_wrapper is
  component design_1 is
  port (
    diff_clock_rtl_0_clk_n : in STD_LOGIC;
    diff_clock_rtl_0_clk_p : in STD_LOGIC;
    reset_rtl_0 : in STD_LOGIC;
    uart_rtl_0_rxd : in STD_LOGIC;
    uart_rtl_0_txd : out STD_LOGIC
```

Tcl Console | Messages | Log | Reports | Design Runs

25:1 Insert VHDL

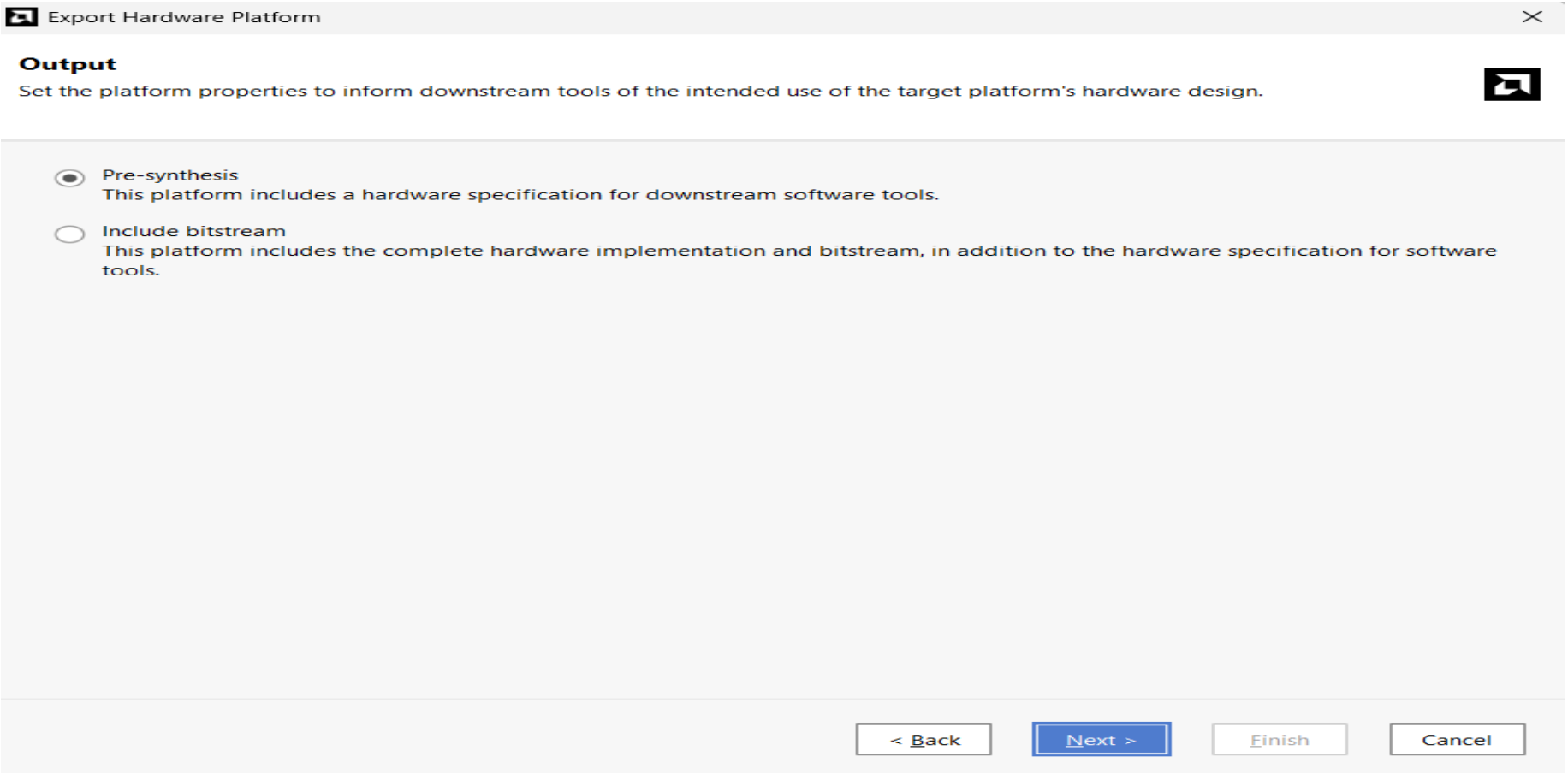
Click : Export Hardware…

(implementing the design on an FPGA).



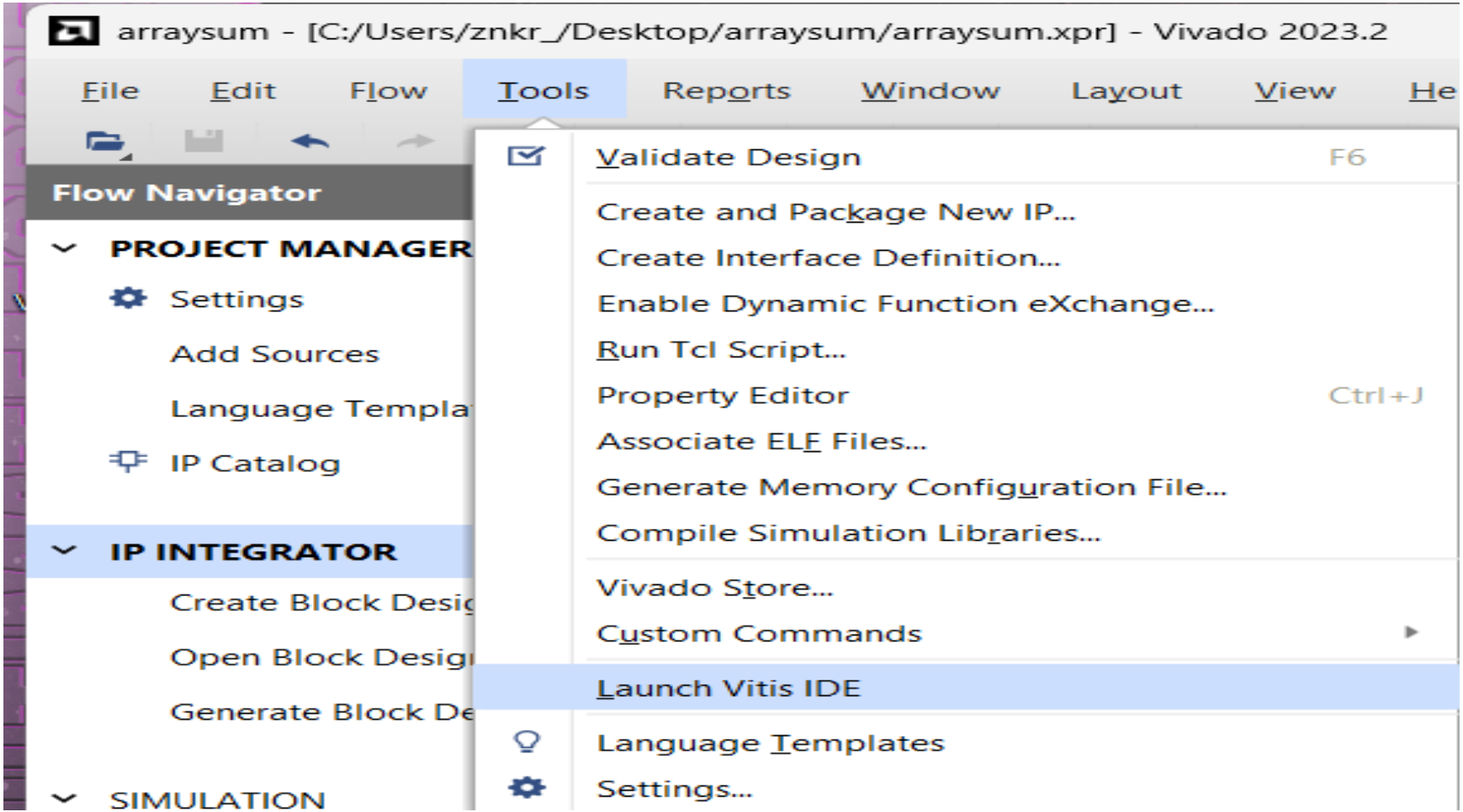
Click : Next > .

(pre-synthesis ensures that the hardware is ready for software development).



Click : Launch Vitis IDE .

(Make sure .xsa file is exported successfully).



Open the project workspace and create a platform.

(Platform : based on the .xsa file).

File Edit Selection View Go Terminal Help Vitis

vitis-comp.json - arraysum - Vitis Unified IDE 2023.2

VITIS COMPONENTS

ARRAYSUM

platform [Platform]

Settings

vitis-comp.json

Sources

Output

FLOW

Component platform

Build

Welcome | vitis-comp.json

platform > vitis-comp.json

platform

microblaze_0

standalone_microblaze_0

Platform - platform

Name platform

Hardware Specification design_1_wrapper.xsa Switch XSA Hardware Specification

Description Description

OUTPUT PROBLEMS

Vitis Server

```
17:29:20 INFO  : -- Build files have been written to: C:/Users/znkr_/OneDrive/Desktop/arraysum/platform/microblaze_0/standalone_microblaze_0/bsp/
17:29:20 INFO  : Successfully created Domain at C:/Users/znkr_/OneDrive/Desktop/arraysum/platform/microblaze_0/standalone_microblaze_0/bsp
17:29:20 INFO  : Successfully Generated Domain C:\Users\znkr_\OneDrive\Desktop\arraysum\platform\microblaze_0\standalone_microblaze_0\bsp
17:29:20 INFO  : Domain standalone_microblaze_0 added successfully.
17:29:20 INFO  : Platform creation finished successfully.
17:29:20 INFO  : Platform Quick Build initiated.
17:29:20 INFO  : Generating Export directory
17:29:20 INFO  : Generated platform metadata for creating application(s) based on platform platform.
```

Vitis Server

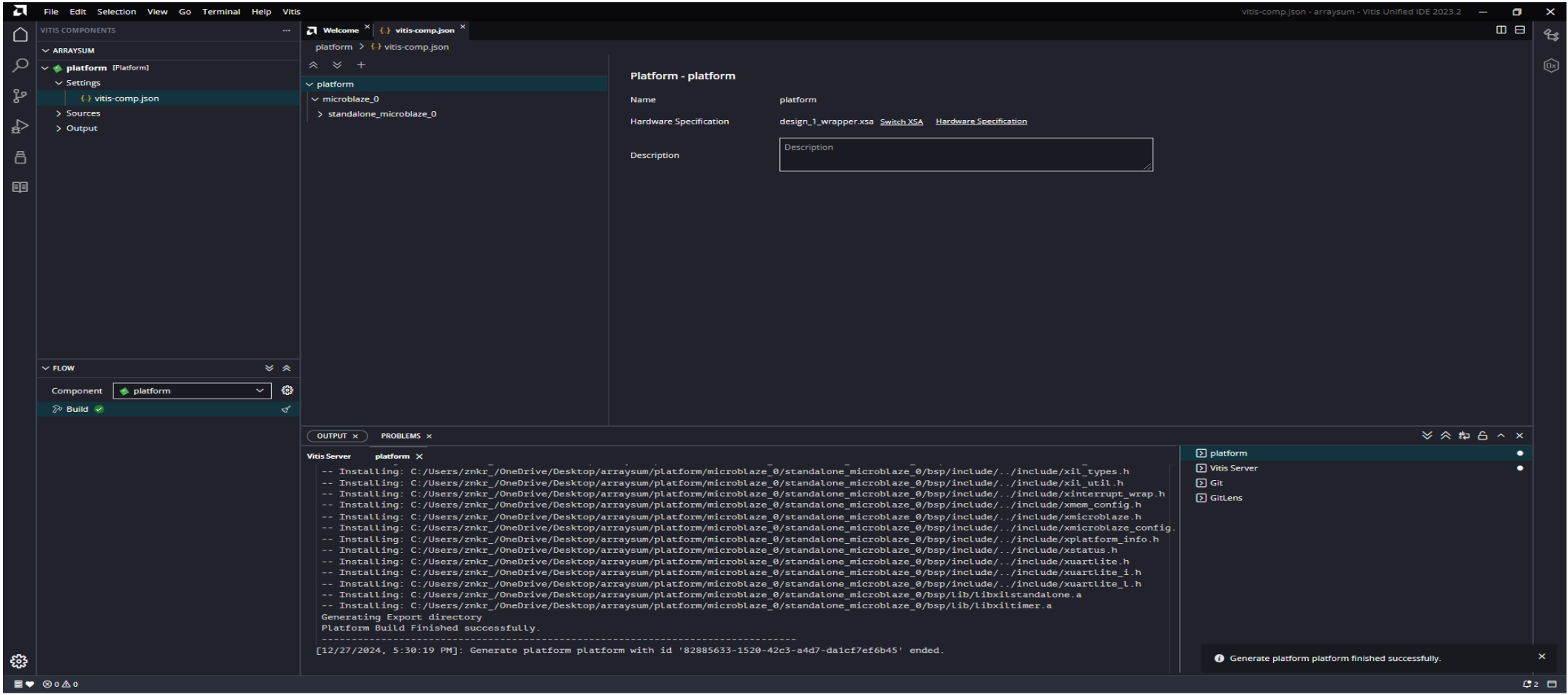
Git

GitLens

Created platform: platform

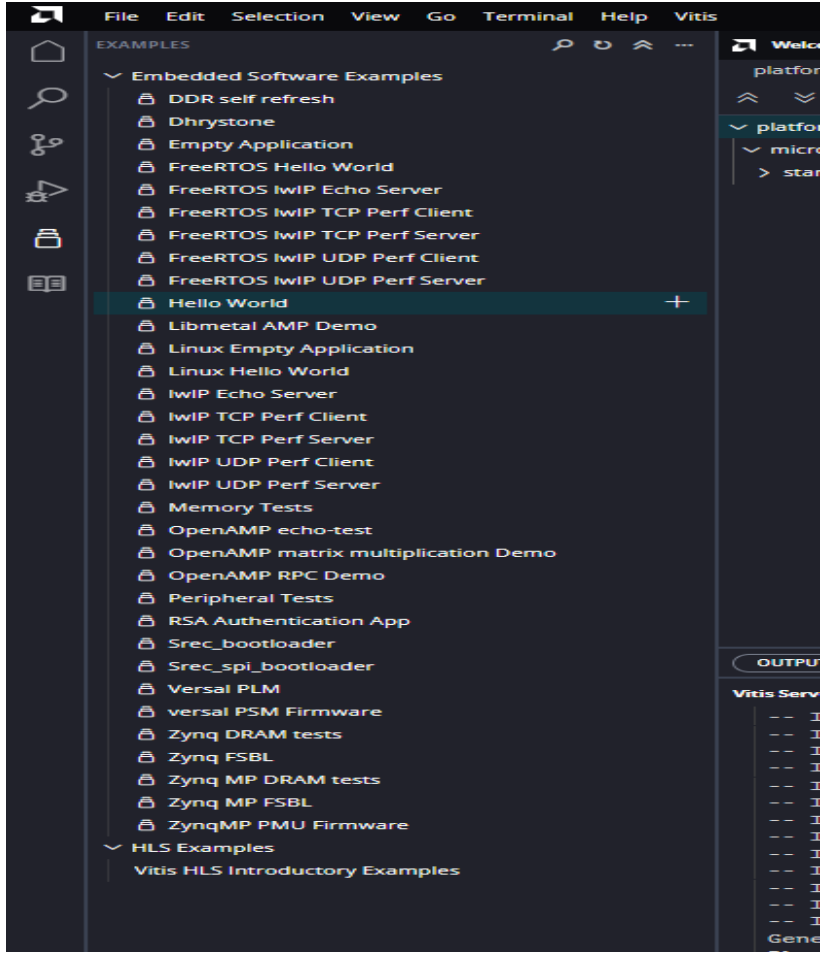
Click : Build.

(Build : To build the platform).



Select : Hello World Application From Templates.

(Renamed: Array_sum_sdk).



Program : helloworld.c

(Calculates the sum of an array of nine floats, stores the result in BRAM and prints the sum via UART).

helloworld.c - arraysum - Vitis Unified IDE 2023.2

Array_sum_sdk > src > helloworld.c > ...

```c
#include <stdio.h>              // Standard Input/Output library for printf
#include "platform.h"           // Used for platform initialization and cleanup
#include "xil_printf.h"         // Provides functions for printing via UART
#include "xil_io.h"             // Provides functions for hardware register read/write (BRAM, IP)
#include "xparameters.h"        // Contains base addresses for hardware resources (BRAM, IP)

int main()
{
    init_platform();            // Initializes the platform (e.g., UART, STDIN/STDOUT)

    char buff[11];              // Buffer to store the result as a string (up to 10 characters + null terminator)

    // Define a static array of 9 float values
    static float arr[9] = {1.0, 2.0, 3.0, 4.0, 5.0, 6.0, 7.0, 8.0, 9.0};

    // Union for converting between unsigned int and float
    union {
        unsigned int a;         // 32-bit unsigned integer
        float b;                // Float value
    } itof;

    float sum = 0.0;            // Variable to store the sum of the array elements

    // **Write array values to BRAM and calculate the sum**
    for (int i = 0; i < 9; i++) {
        itof.b = arr[i];        // Copy the current float element into the union
        // Write the value (converted to unsigned int) to the BRAM address
        Xil_Out32(XPAR_AXI_BRAM_0_BASEADDRESS + (4 * i), itof.a);
        sum += arr[i];          // Calculate the sum of the elements
    }

    itof.b = sum;               // Store the result (sum) in the union

    //Print the result via UART:
    sprintf(buff, "%f", itof.b);        //Convert the result (float) to a string and store it in buff
    xil_printf("Sum = %s\n\r", buff);   // Print the result string via UART

    //MY_OUTPUT_SIGNAL FROM THIS SIMULATION: charbuffer[1:20] : WROTE AS A STRING AND AFTER SOME SECONDS PRINTED RESULT IN TCL CONSOLE!

    cleanup_platform(); // Cleanup the platform
    return 0;
}//*IN SHORT:
//1.This program CALCULATES the SUM of an ARRAY OF FLOATS.
//2. Stores the VALUES and RESULT in BRAM.
//3. Prints the SUM via UART
```

OUTPUT × PROBLEMS ×

No problems have been detected in the workspace so far.

Click : Build.

(Build : To build the Application and generate ELF File).

File Edit Selection View Go Terminal Help Vitis

helloworld.c - arraysum - Vitis Unified IDE 2023.2

VITIS COMPONENTS

ARRAYSUM

- Array_sum_sdk [Application]
  - Settings
  - Includes
  - Sources
    - src
      - helloworld.c
      - lscript.ld
      - platform.c
      - platform.h
  - Output
- platform [Platform]

FLOW

Component: Array_sum_sdk

- Build
- Run
- Debug

Welcome | vitis-comp.json platform | Hello World | vitis-comp.json Array_sum_sdk | helloworld.c | xil_io.h | xpseudo_asm.h

Array_sum_sdk > src > helloworld.c > ...

```c
#include <stdio.h>              // Standard Input/Output library for printf
#include "platform.h"           // Used for platform initialization and cleanup
#include "xil_printf.h"         // Provides functions for printing via UART
#include "xil_io.h"             // Provides functions for hardware register read/write (BRAM, IP)
#include "xparameters.h"        // Contains base addresses for hardware resources (BRAM, IP)

int main()
{
    init_platform();            // Initializes the platform (e.g., UART, STDIN/STDOUT)

    char buff[11];              // Buffer to store the result as a string (up to 10 characters + null terminator)

    // Define a static array of 9 float values
    static float arr[9] = {1.0, 2.0, 3.0, 4.0, 5.0, 6.0, 7.0, 8.0, 9.0};

    // Union for converting between unsigned int and float
    union {
        unsigned int a;         // 32-bit unsigned integer
        float b;                // Float value
    } itof;

    float sum = 0.0;            // Variable to store the sum of the array elements

```

OUTPUT | PROBLEMS

Vitis Server | Array_sum_sdk:: | platform | HLS Pragma Language Server

```
-- Generating done
-- Build files have been written to: C:/Users/znkr_/OneDrive/Desktop/arraysum/Array_sum_sdk/build
C:/Xilinx/Vitis/2023.2/tps/win64/cmake-3.24.2/bin/cmake.exe -SC:/Users/znkr_/OneDrive/Desktop/arraysum/Array_sum_sdk/src -BC:/Users/znkr_/OneDri
C:/Xilinx/Vitis/2023.2/tps/win64/cmake-3.24.2/bin/cmake.exe -E cmake_progress_start C:/Users/znkr_/OneDrive/Desktop/arraysum/Array_sum_sdk/build
make  -f CMakeFiles/Makefile2 all
make[1]: Entering directory 'c:/Users/znkr_/OneDrive/Desktop/arraysum/Array_sum_sdk/build'
make  -f CMakeFiles/Array_sum_sdk.elf.dir/build.make CMakeFiles/Array_sum_sdk.elf.dir/depend
make[2]: Entering directory 'c:/Users/znkr_/OneDrive/Desktop/arraysum/Array_sum_sdk/build'
make[2]: Leaving directory 'c:/Users/znkr_/OneDrive/Desktop/arraysum/Array_sum_sdk/build'
make  -f CMakeFiles/Array_sum_sdk.elf.dir/build.make CMakeFiles/Array_sum_sdk.elf.dir/build
make[2]: Entering directory 'c:/Users/znkr_/OneDrive/Desktop/arraysum/Array_sum_sdk/build'
[ 33%] Building C object CMakeFiles/Array_sum_sdk.elf.dir/helloworld.c.obj
C:/Xilinx/Vitis/2023.2/gnu/microblaze/nt/bin/mb-gcc.exe  -isystem C:/Users/znkr_/OneDrive/Desktop/arraysum/platform/export/platform/sw/standalon
[ 66%] Building C object CMakeFiles/Array_sum_sdk.elf.dir/platform.c.obj
C:/Xilinx/Vitis/2023.2/gnu/microblaze/nt/bin/mb-gcc.exe  -isystem C:/Users/znkr_/OneDrive/Desktop/arraysum/platform/export/platform/sw/standalon
[100%] Linking C executable Array_sum_sdk.elf
C:/Xilinx/Vitis/2023.2/gnu/microblaze/nt/bin/mb-gcc.exe  -O2 -mlittle-endian -mxl-soft-mul -mcpu=v11.0 -DSDT  -MMD -MP -specs=C:/Users/znkr_/One
mb-size --format=berkeley Array_sum_sdk.elf
   text       data     bss     dec     hex filename
  95040       2104    2144   99288   183d8 Array_sum_sdk.elf
mb-size --format=berkeley Array_sum_sdk.elf > C:/Users/znkr_/OneDrive/Desktop/arraysum/Array_sum_sdk/build/Array_sum_sdk.elf.size
make[2]: Leaving directory 'c:/Users/znkr_/OneDrive/Desktop/arraysum/Array_sum_sdk/build'
[100%] Built target Array_sum_sdk.elf
make[1]: Leaving directory 'c:/Users/znkr_/OneDrive/Desktop/arraysum/Array_sum_sdk/build'
C:/Xilinx/Vitis/2023.2/tps/win64/cmake-3.24.2/bin/cmake.exe -E cmake_progress_start C:/Users/znkr_/OneDrive/Desktop/arraysum/Array_sum_sdk/build
Build Finished successfully
[12/27/2024, 6:00:04 PM]: Build for Array_sum_sdk:: with id '65b1a4b7-e5b6-449f-9d99-b44222e703c9' ended.
```

- Array_sum_sdk
- Vitis Server
- clangd
- Git
- GitLens
- HLS Pragma Language Server
- platform

0 0 clangd: idle

Ln 45, Col 30 LF UTF-8 Spaces: 4 C 6

Right-click : Block design and associate ELF files.

(Apply the ELF file from SDK only to the simulation sources).

arraysum - [C:/Users/znkr_/OneDrive/Desktop/arraysum/arraysum.xpr] - Vivado 2023.2

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready

Default Layout

Flow Navigator

- PROJECT MANAGER
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Run Linter
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design

PROJECT MANAGER - arraysum

Sources

- Simulation Sources (2)
  - sim_1 (2)
    - **design_1_wrapper**(STRUCTURE) (design_1_wrapper.vhd) (1)
      - design_1_i : design_1 (design_1.bd) (1)
        - design_1(STRUCTURE) (design_1.vhd) (9)

Hierarchy | IP Sources | Libraries | Compile Order

Source File Properties

design_1.bd

Enabled

Location: C:/Users/znkr_/OneDrive/Desktop/arraysum/arraysum.srcs/sources_1/bd

General | Properties

Associate ELF Files

Associate an ELF file with a processor instance (Address Map). ELF files are available after running generate on your embedded design sources. Only processors that are visible from the active top of the design will be shown.

Processors/Address Maps	Associated ELF File
Design Sources	
design_1	
microblaze_0	mb_bootloop_le.elf
Simulation Sources	
design_1	
microblaze_0	Array_sum_sdk.elf

OK Cancel

Not started

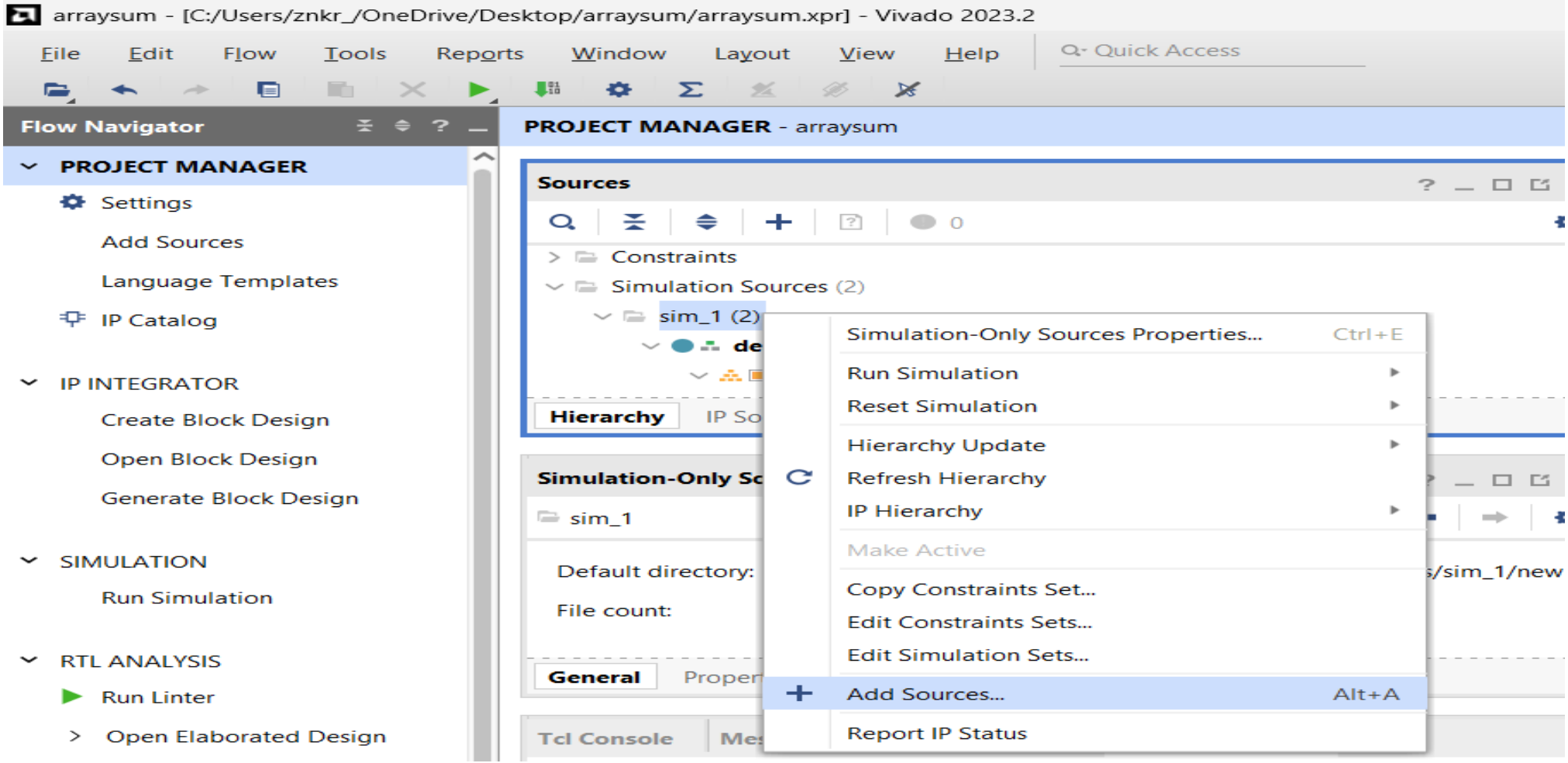
No errors or warnings

Tcl Console | Messages | Log | Reports | **Design Runs**

Name	Constraints	Status	WNS	TNS	...	LUT	FF	BRAM	URAM
synth_1 (active)	**constrs_1**	**Not started**							
impl_1	constrs_1	Not started							
Out-of-Context Module Runs									
design_1		Submodule Runs Complete							

Associate ELF Files

Right-click : Simulation Sources and Add Sources…



Click : Create Source File.

(File name : testbench).

Add Sources

Add or Create Simulation Sources

Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.

Specify simulation set: sim_1

Use Add Files, Add Directories or

Add Files | Add Directo

Scan and add RTL include files into project

Copy sources into project

Add sources from subdirectories

Include all design sources for simulation

Create Source File

Create a new source file and add it to your project.

File type: VHDL

File name: testbench

File location: <Local to Project>

OK | Cancel

< Back | Next > | Finish | Cancel

Click : Run Behavioral Simulation.

(The testbench contains VHDL code for UART communication and displaying data in the TCL Console).

arraysum - [C:/Users/znkr_/OneDrive/Desktop/arraysum/arraysum.xpr] - Vivado 2023.2

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready

Default Layout

Flow Navigator

- PROJECT MANAGER
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
  - Run Behavioral Simulation
  - Run Post-Synthesis Functional Simulation
  - Run Post-Synthesis Timing Simulation
  - Run Post-Implementation Functional Simulation
  - Run Post-Implementation Timing Simulation
- RTL ANALYS
  - Run Lint
  - Open El
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design

PROJECT MANAGER - arraysum

Source File Properties

Sources

- Design Sources (1)
  - design_1_wrapper(STRUCTURE) (design_1_wrapper.vhd) (1)
- Constraints
- Simulation Sources (2)
  - sim_1 (2)
    - testbench(my_testbench) (testbench.vhd) (1)
    - ELF (1)
- Utility Sources

Hierarchy | IP Sources | Libraries | Compile Order

Project Summary | testbench.vhd

C:/Users/znkr_/OneDrive/Desktop/arraysum/arraysum.srcs/sim_1/new/testbench.vhd

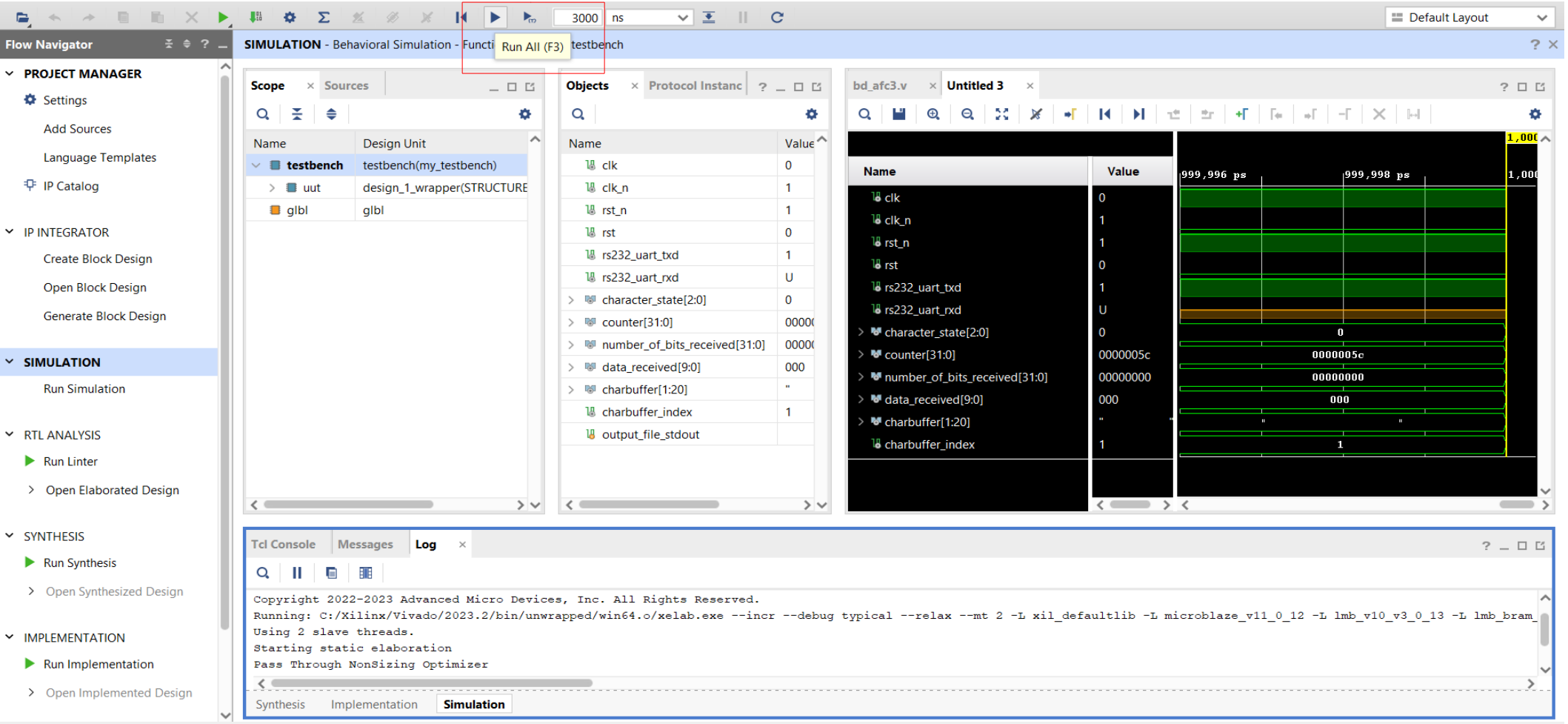
```
89          when "011" =>
90              if counter = x"00000364" then -- middle of stop character
91                  -- report "received " & integer'image (to_integer (unsigned (data_received(9 downto 2)
92                  -- write (line1, character'val(to_integer(unsigned(data_received(9 downto 2)))));
93                  -- writeline (output_file_stdout, line1);
94                  if (charbuffer_index = 19) then
95                      charbuffer (1) <= character'val(to_integer(unsigned(data_received(9 downto 2))));
96                      charbuffer_index <= 2;
97                      write (line1, charbuffer, left);
98                      writeline (output_file_stdout, line1);
99                  elsif (10 = to_integer(unsigned(data_received(9 downto 2)))) then
100                     charbuffer_index <= 1;
101                     write (line1, charbuffer, left);
102                     writeline (output_file_stdout, line1);
103                 else
104                     charbuffer(charbuffer_index) <= character'val(to_integer(unsigned(data_received(9
105                     charbuffer_index <= charbuffer_index + 1;
106                 end if;
107                 character_state <= "000";
108                 counter <= x"00000000";
109             end if;
110         when others =>
111             counter <= x"00000000";
112             data_received <= "0000000000";
113             number_of_bits_received <= x"00000000";
114             character_state <= "000";
115     end case;
116     end if;
117 end if;
118 end process;
119
120 end architecture my_testbench;
```

Tcl Console | Messages | Log | Reports | Design Runs

Vivado Simulator

Click : Run All (F3).

(Simulation launched).

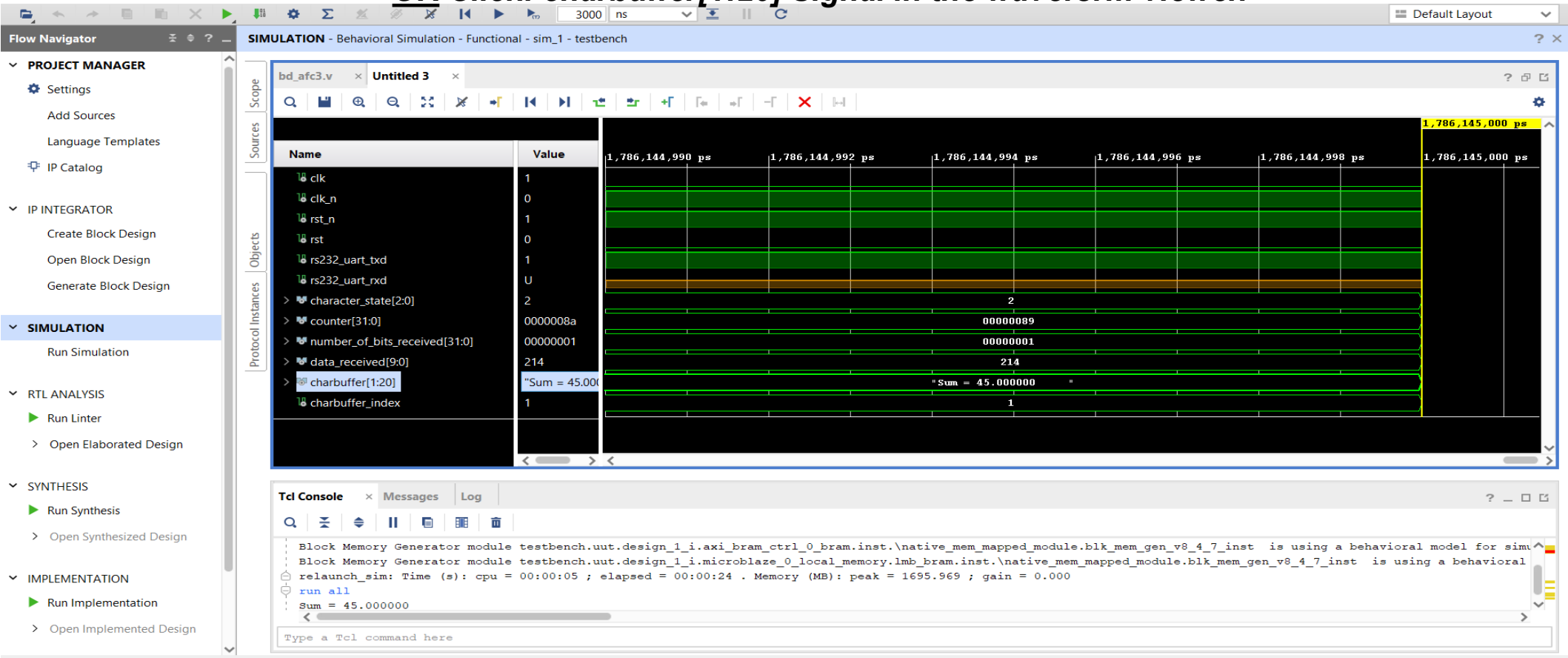


Click : TCL Console to see the result.

It may take some time; please be patient.

(Sum = 45.000000).

OR Click: charbuffer[1:20] Signal in the waveform viewer.



Using TinyAES In SDK for Data Encryption | Decryption.

File Edit Selection View Go Terminal Help Vitis

helloworld.c - arraysum - Vitis Unified IDE 2023.2

VITIS COMPONENTS

ARRAYSUM

- array_sum_sdk [Application]
  - Settings
  - Includes
  - Sources
    - src
      - aes.c
      - helloworld.c
      - lscript.ld
      - platform.c
      - platform.h
  - Output
- platform [Platform]

FLOW

Component: array_sum_sdk

- Build
- Run
- Debug

Welcome | helloworld.c

array_sum_sdk > src > helloworld.c > main

```c
        itof.b = arr[i];
        Xil_Out32(XPAR_AXI_BRAM_0_BASEADDRESS + (4 * i), itof.a); // Writing to BRAM.
        sum += arr[i]; //Calculates Sum.
    }

    itof.b = sum; //Saving : Result : In : UNION
    Xil_Out32(XPAR_AXI_BRAM_0_BASEADDRESS + (4 * 9), itof.a); //Write The sum to BRAM.


    //PRINTING ORIGINAL : SUM RESULT :
    sprintf(buff, "%f", itof.b);//CONVERT FLOAT of ITOF.B TO a STRING and store it in BUFF
    xil_printf("Sum= %s\n\r", buff);//Print The formatted STRING stored in BUFF to the UART

    //AES ENCRYPTION : SUM RESULT :
    struct AES_ctx ctx; //AES : context
    AES_init_ctx(&ctx,key); //Initialize AES context with the key
    memcpy(data,&itof.b,sizeof(itof.b));//Copy the float sum into the data buffer
    AES_ECB_encrypt(&ctx,data);//Encrypt the data buffer
    xil_printf("EncSum= "); //Print the encrypted SUM. (IN HEXIDECIMAL)
    for(int i=0;i<16;i++){
        xil_printf("%02x ",data[i]);//Print each byte of the encrypted data
    }
    xil_printf("\n\r");

    //AES DECRYPTION : SUM RESULT :
    AES_ECB_decrypt(&ctx,data); //Decrypt the data buffer
    memcpy(&itof.b,data,sizeof(itof.b));//Copy the decrypted data back into the union (float)
    sprintf(buff,"%f",itof.b);//CONVERT FLOAT of ITOF.B TO a STRING and store it in BUFF
    xil_printf("DecSum= %s\n\r", buff); //Print the descrypted SUM.

    cleanup_platform();
    return 0;
}
```

OUTPUT | PROBLEMS

Vitis Server | array_sum_sdk::

```
make[2]: Leaving directory 'c:/Users/znkr_/Downloads/arraysum/array_sum_sdk/build'
make  -f CMakeFiles/array_sum_sdk.elf.dir/build.make CMakeFiles/array_sum_sdk.elf.dir/build
make[2]: Entering directory 'c:/Users/znkr_/Downloads/arraysum/array_sum_sdk/build'
[ 25%] Building C object CMakeFiles/array_sum_sdk.elf.dir/helloworld.c.obj
C:/Xilinx/Vitis/2023.2/gnu/microblaze/nt/bin/mb-gcc.exe  -isystem C:/Users/znkr_/Downloads/arraysum/platform/export/platform/sw/standalone_micro
[ 50%] Linking C executable array_sum_sdk.elf
C:/Xilinx/Vitis/2023.2/gnu/microblaze/nt/bin/mb-gcc.exe  -O2 -mlittle-endian -mxl-soft-mul -mcpu=v11.0 -DSDT  -MMD -MP -specs=C:/Users/znkr_/Dow
mb-size --format=berkeley array_sum_sdk.elf
   text    data     bss     dec     hex filename
 103732    2104    2148  107984   1a5d0 array_sum_sdk.elf
mb-size --format=berkeley array_sum_sdk.elf > C:/Users/znkr_/Downloads/arraysum/array_sum_sdk/build/array_sum_sdk.elf.size
make[2]: Leaving directory 'c:/Users/znkr_/Downloads/arraysum/array_sum_sdk/build'
[100%] Built target array_sum_sdk.elf
make[1]: Leaving directory 'c:/Users/znkr_/Downloads/arraysum/array_sum_sdk/build'
C:/Xilinx/Vitis/2023.2/tps/win64/cmake-3.24.2/bin/cmake.exe -E cmake_progress_start C:/Users/znkr_/Downloads/arraysum/array_sum_sdk/build/CMakeF
Build Finished successfully
[1/6/2025, 6:27:45 PM]: Build for array_sum_sdk:: with id 'e7dbec4c-b83c-49dc-85d2-33744a77fda6' ended.
```

array_sum_sdk

- Vitis Server
- clangd
- Git
- GitLens
- HLS Pragma Language Server

0 0 clangd: idle

Ln 63, Col 2 LF UTF-8 Spaces: 4 C 1

Simulation Results: Original Sum | Encrypted Sum | Decrypted Sum

arraysum - [C:/Users/znkr_/Downloads/arraysum/arraysum.xpr] - Vivado 2023.2

File Edit Flow Tools Reports Window Layout View Run Help

Flow Navigator

PROJECT MANAGER
- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR
- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION
- Run Simulation

RTL ANALYSIS
- Run Linter
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IMPLEMENTATION
- Run Implementation
- Open Implemented Design

SIMULATION - Behavioral Simulation - Functional - sim_1 - testbench

testbench.vhd | testbench_behav.wcfg

Name	Value
counter[31:0]	0003ee8f
number_of_bits_received[31:0]	00000000
data_received[9:0]	034
charbuffer[1:20]	" ecSum= 45.
charbuffer_index	3

12,958,755,000 ps

12,958,754,990 ps | 12,958,755,000 ps | 12,958,755,010 ps | 12,958,755,020 ps | 12,958,755,030 ps

0003ee8e | 00000000 | 034 | " ecSum= 45.000000 " | 3

Tcl Console | Messages | Log

```
launch_simulation: Time (s): cpu = 00:00:15 ; elapsed = 00:01:31 . Memory (MB): peak = 2632.020 ; gain = 0.000
run all
Sum= 45.000000

EncSum= 32 AD AC
B9 81 4E 0E 4A 21
2F 47 54 50 D7 C9
BA 47 54 50 D7 C9

DecSum= 45.000000
INFO: [Common 17-41] Interrupt caught. Command should exit soon.
run: Time (s): cpu = 00:06:58 ; elapsed = 00:20:26 . Memory (MB): peak = 2632.020 ; gain = 0.000
INFO: [Common 17-344] 'run' was cancelled
```

Type a Tcl command here

Sim Time: 12958755 ns

Thank you for your participation.