國立清華大學資訊工程學系

CS 4100 ---計算機結構

102學年度下學期

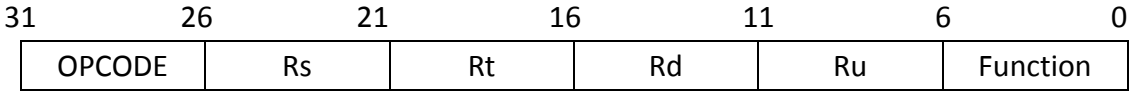
Homework #7

(Due: 2014/05/01 10:10am)

1. (50%) Figure 1 shows the basic single-cycle MIPS implementation. New instructions can be added to an existing ISA, but the decision whether or not to do that depends, among other things, on the cost and complexity such an addition introduces into the processor data-path and control. The following problem refers to this new instruction:

Instruction	Interpretation
add3 Rd, Rs, Rt, Ru	Reg[Rd] = Reg[Rs] + Reg[Rt] + Reg[Ru]

The instruction format:



1.1 Please modify single-cycle MIPS architecture for this new instruction and describe your modification. Your answer should be drawn like Figure1.

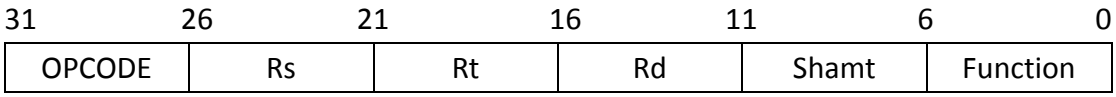
Please use a different color to highlight your modification.

1.2 Describe the control-signals for “add3”.

2. (50%) The following problem in this exercise refers to this new instruction:

Instruction	Interpretation
ams Rd, Rs, Rt	Reg[Rd] = (Reg[Rs]+Reg[Rt]) * (Reg[Rs]-Reg[Rt])

The instruction format:



2.1 Please modify single-cycle MIPS architecture for this new instruction and describe your modification. Your answer should be drawn like Figure1.

Please use different colors to highlight your modification.

2.2 Describe the control-signals for “ams”.

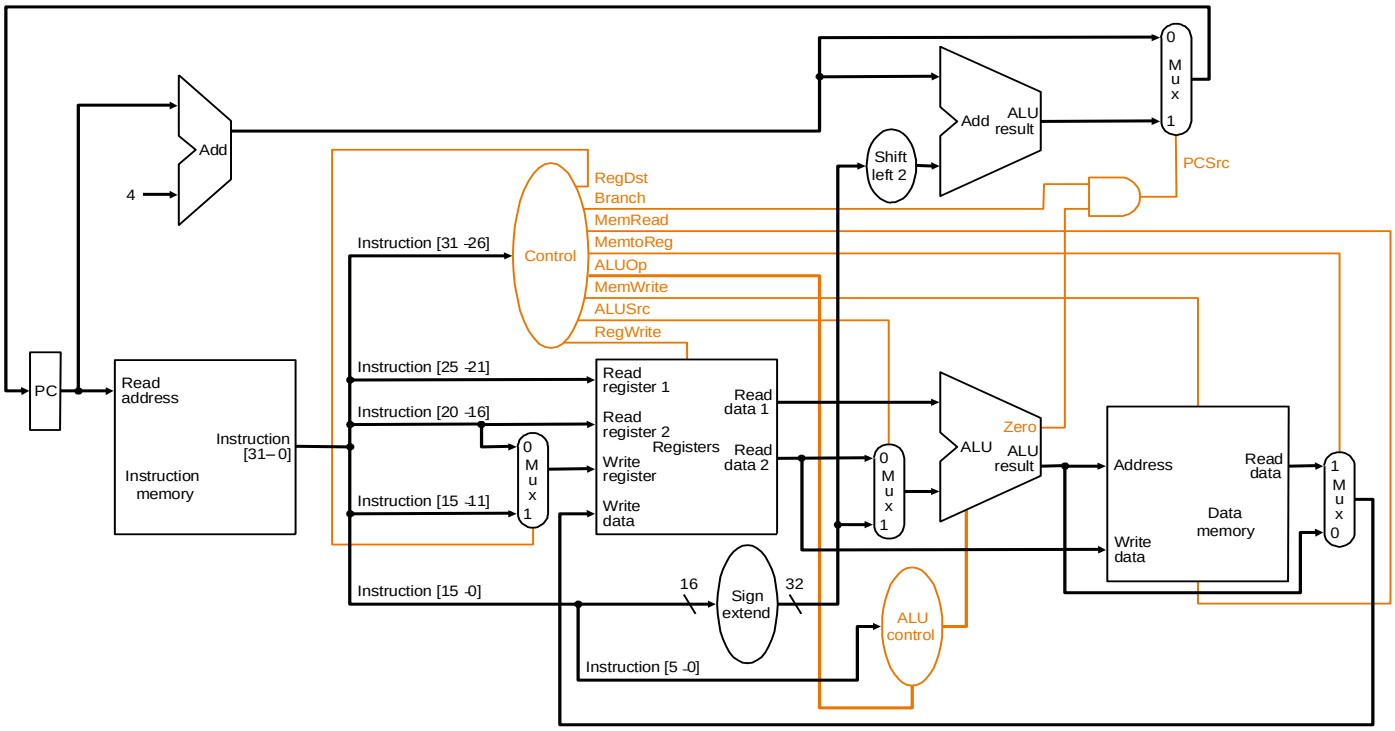


Figure 1: Single-cycle MIPS implementation